THE DESIGN OF GAAS HEMT AND HBT BESSEL-TYPE TRANSIMPEDANCE AMPLIFIERS

A Thesis

by

OLUWAFEMI IBUKUNOLUWA ADEYEMI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2006

Major Subject: Electrical Engineering

THE DESIGN OF GAAS HEMT AND HBT BESSEL-TYPE TRANSIMPEDANCE AMPLIFIERS

A Thesis

by

OLUWAFEMI IBUKUNOLUWA ADEYEMI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Approved by:

Chair of Committee,	Aydin Karsilayan
Committee Members,	Jose Silva-Martinez
	Laszlo Kish
	Ibrahim Karaman
Head of Department,	Costas Georghiades

December 2006

Major Subject: Electrical Engineering

ABSTRACT

The Design of GaAs HEMT and HBT Bessel-Type Transimpedance Amplifiers.

(December 2006)

Oluwafemi Ibukunoluwa Adeyemi, B.S., University of Houston

Chair of Advisory Committee: Dr. Aydin Karsilayan

The need of the everyday user to transfer large amounts of data is driving the need for larger data transfer capacity. Optical communication networks can satisfy this need. To be economically viable, optical transceivers must be integrated onto chips at low cost, using relatively cheap semiconductor processes.

The optical preamplifier (transimpedance amplifier) receives optical information and converts it to a useful electrical form. It must operate at high speed, contribute little distortion to the input signal, and add little electrical noise to the incoming signal.

This thesis investigates the design techniques in the literature, and proposes new architectures. Two high performance preamplifiers are designed, one using GaAs HEMTs, and the other using GaAs HBTs, each with different circuit techniques.

The HEMT preamplifier has a transimpedance gain of 1.4 kΩ, the highest in the literature for 10 Gb/s operation, along with a low input referred noise current of about 15 $pA/Hz^{1/2}$ at a bandwidth of 6.3 GHz. The HBT preamplifier also has a transimpedance gain of 1.5 kΩ, with a low input referred noise current of about 7 $pA/Hz^{1/2}$. Both have clear, open eye-diagrams with a 10 Gb/s bit stream input, and are suitable for integration on a chip.

The HEMT preamplifier was implemented as a common-gate, common-source amplifier cascade with a darlington output driver for a 50 Ω load. The HBT preamplifier was implemented as common-emitter darlington amplifier with shunt peaking, and a simple emitter degenerated output driver for a 50 Ω load.

Both implementations exceeded the bandwidth, transimpedance gain and noise performance typically expected of the transistor technologies used. It is shown that the transimpedance limit can be circumvented by the use of novel architectures and shunt peaking.

DEDICATION

To God and my parents

ACKNOWLEDGEMENTS

This thesis would not have been possible without the support of several people. Many thanks to my advisor Dr. Aydin Karsilayan for input as to the direction of this work, and countless hours spent on numerous revisions.

I also acknowledge the contributions of my committee members, particularly Dr. Jose Silva-Martinez and Dr. Laszlo Kish. The insights I received in their courses and their helpful comments on the thesis went a long way. Discussions with Haitao Tong on the pioneering work he did in this research area were very helpful.

I would like to thank Deana Totzke, who I had the pleasure of working for. Without the support I received, completing this degree would have been difficult at best.

Finally I thank my parents for their financial and inspirational support, my friends for easing the drudgery, and most importantly God, without whom this thesis would never have been started, or completed.

TABLE OF CONTENTS

Page

LIST OF FIGURES

FIGURE Page

LIST OF TABLES

CHAPTER I
INTRODUCTION

The exponential growth of Information Technology applications drives the need to transmit larger amounts of information faster. Traditionally, information has been transmitted wirelessly from point to point. While capable of transmitting data at fast speeds, these are inefficient for present-day demands.

The need for high-speed, high-capacity communications is more widespread today, due to the need of the average user. Real-time streaming applications such as teleconferencing, and the need to transfer larger multimedia files quicker drives the need for communications systems that are low cost, easy to integrate and immune to interference from weather conditions such as lightning, and electromagnetic interference from other high-speed data links. Optical fiber communication, using light to transmit information, satisfies the need for speed, capacity and interference immunity [1].

1.1. Overview of Fiber Optic Communication Systems

The potential information carrying capacity of light dwarfs all other known methods of communication. One popular wavelength for optical communication is 1.5μm, corresponding to a frequency of about 200THz [1]. Considering that the bandwidth of the human voice is about 20KHz, approximately 10 billion conversations can be transmitted at once. Even if only a fraction of this bandwidth is used due to practical constraints, the capacity is still large.

This thesis follows the style of the IEEE Journal of Solid-State Circuits.

Fig. 1.1 illustrates a digital fiber-optic communication system.

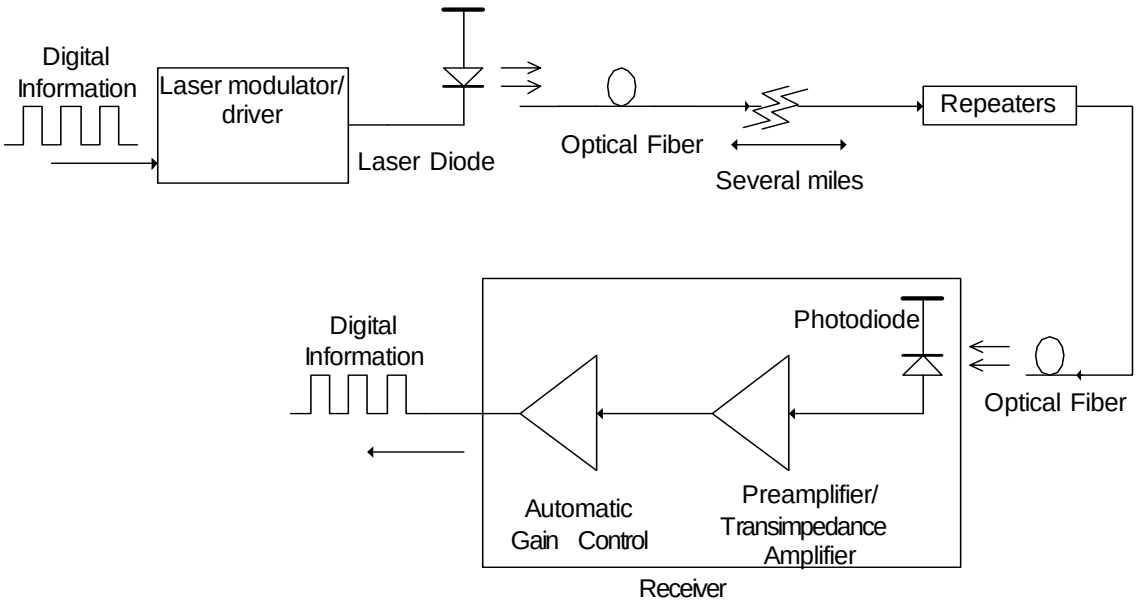

Fig. 1.1. Illustration of a Digital Fiber-Optic Communication System.

Fig. 1.1 shows how a laser diode capable of emitting light under the electrical stimulus of a laser driver is modulated with input digital information, and transmitted over optical fiber. Due to the large distances involved, optical repeaters are placed along the optical fiber path to restore signal strength due to attenuation in the optical fiber [2]. These repeaters are optical amplifiers, regenerating the incoming optical signals without the need for opto-electronic and electro-optical signal conversions.

The light signal reaches the receiver, with a front-end consisting of a photodiode and a preamplifier. The photodiode converts the input light signal into electrical current impulses, which are converted to voltage pulses by the preamplifier. Since the preamplifier converts an input current into an output voltage, it will be referred to as a transimpedance amplifier (TIA). The input signal strength is unknown, and can range

from a few microamperes to several milliamperes, so an automatic gain control (AGC) circuit is placed after the preamplifier to modify the effective gain of the receiver according to the input signal strength.

1.2 Requirements of Transimpedance Amplifiers

After traveling long distances, the light signal becomes weak due to attenuation. The signal conversion to current by the photodiode results in weak current pulses. Furthermore, frequency dispersion in the optical fiber introduces distortion into the digital signal [2]. This signal characteristic places limitations on the nature of the TIA.

The TIA must contribute very little current noise, otherwise it risks swamping the weak signal current, causing information loss. Furthermore, the bandwidth of the TIA must be wide enough to allow for good reproduction of the high-speed current pulses, usually transmitted at a rate of 2.5Gb/s - 40Gb/s. These restrictions impose challenges in the design of high-speed TIAs.

1.3 Aim and Organization of Thesis

The objective of this thesis is to design TIAs with low noise signature, comparable to that in the research literature, and capable of operating at high speeds with little signal distortion. The TIA architectures designed will allow high-speed operation without the need for expensive semiconductor processes.

Chapter II reviews the Figures of Merit (FOM) for optical receivers, and their relationships to physical transistor parameters.

Chapter III deals with the Gallium Arsenide (GaAs) semiconductor technology used, various TIA topologies, and their theory of operation. The advantages and shortcomings of these TIA topologies are highlighted.

Chapter IV introduces the TIAs designed in the course of research, along with the design methodologies used. Schematic and layout simulation results are then presented.

Chapter V will compare the design results with other designs in the literature, draw conclusions based on the new designs, and highlight possible uses and future improvements.

CHAPTER II
FIGURES OF MERIT FOR TRANSIMPEDANCE AMPLIFIERS

2.1 Analog and Digital Receivers

Receivers can be broadly classified as analog or digital, based on the manner in which the information transmitted is coded into the signal waveform. Analog receivers are concerned with the reception of continuous time waveforms, and are typically used in broadband systems where analog to digital conversion is impractical [1]. Examples include traditional TV and cable systems. Analog receiver performance is concerned with signal reception and reproduction with little distortion and noise.

Digital receivers, on the other hand, are used when information is transmitted as a stream of bits. Digital receiver performance, is therefore concerned with the error involved in misinterpreting the bits in a digital stream. The bit error rate (BER) quantifies this, and is defined as the average number of misinterpreted bits per a certain number of bits transmitted. A BER of 10^{-9} for example, implies one erroneous bit per 1 billion bits in a digital stream.

2.2 The Bit Error Rate

A digital receiver's performance can be measured by how low its BER is. It should be noted that the BER is an average quantity, and in reality, is a time varying quantity. This is because optical signals experience a time varying signal attenuation due to turbulent weather and polarization in the optical fibers used for transmission [1]. Still, the average BER provides a good figure of merit for digital receivers.

An alternative term to the BER is sensitivity. It is defined as the minimum input signal required to generate a given BER.

2.3 Digital Receiver Data Formats

The input signal to a receiver consists of a series of binary pulses representing either a **1** or a **0**. There are several modulation schemes for the transmission of these pulses, including the non-return-to-zero (NRZ) and return-to-zero (RZ) schemes.

In the NRZ scheme, a pulse is generated to signify a **1**, and no pulse is generated to signify a **0**, as illustrated in Fig. 2.1.

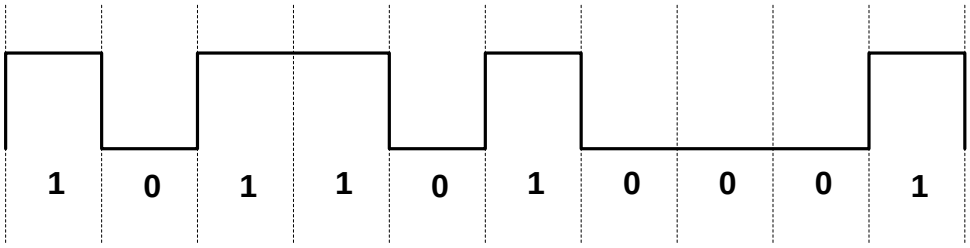

Fig. 2.1. NRZ Representation of the Binary Sequence 1011010001.

The RZ modulation scheme represents a binary **1** by a pulse for half the signal period, and then returns to zero for the remainder of the period. A **0** is represented by an absence of any pulse over the whole bit period. The RZ format is illustrated in Fig. 2.2.

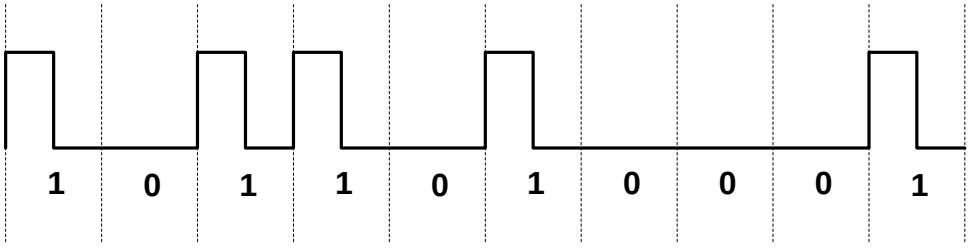

Fig. 2.2. RZ Representation of the Binary Sequence 1011010001.

For a 10Gb/s bit pattern, the NRZ format produces a 5GHz pulse train, while the RZ format produces a 10GHz pulse train. The NRZ format therefore eases the bandwidth requirement, and more information can be packed into a channel.

However, the RZ format is more suitable for long distance transmission, as the narrowness of each bit pulse causes it to stand out, making it easier to detect the signal in the presence of significant noise and frequency dispersion [2]. The data format assumed in this thesis will be random NRZ signals, except where noted. The results are equally applicable to most data coding schemes.

2.4 Data Recovery and Its Effect on TIA Design

In amplifying the input digital signal, the front-end of a digital receiver, the TIA, will add some noise to the amplified signal. This noise corrupts the digital signal levels, as well as the zero crossing of the data. There are two main methods of extracting clean signals from the output of the TIA/AGC block: asynchronous and synchronous. Both determine the bandwidth requirements of the TIA.

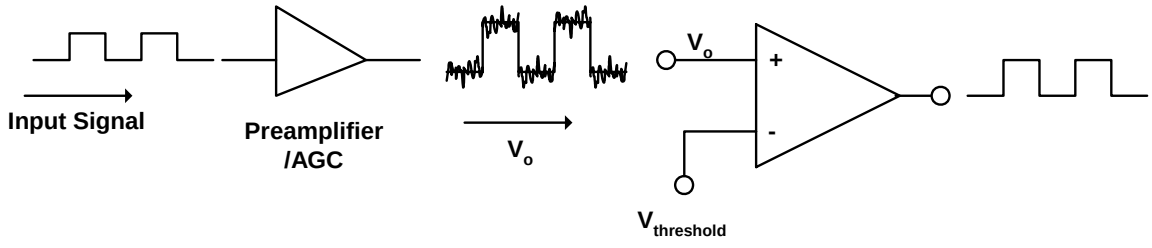

Fig. 2.3. Asynchronous Data Recovery.

In asynchronous data recovery (Fig. 2.3), the noisy signal at the output of the TIA is compared with a threshold voltage, which is usually midway between the high and low

signal levels. The output is a clean digital signal, which can be used by further processing blocks.

A disadvantage of this scheme is that the TIA's bandwidth must be about twice that of the signal, in order for the rise time (0.17 times the bit period [3]) of the output digital pulse to be small enough to allow the pulse to settle quickly. As will be seen later, this wide bandwidth requirement makes the TIA design difficult, as it introduces substantial noise into the circuit.

The synchronous detection scheme eases TIA design requirements, and is illustrated in Fig 2.4.

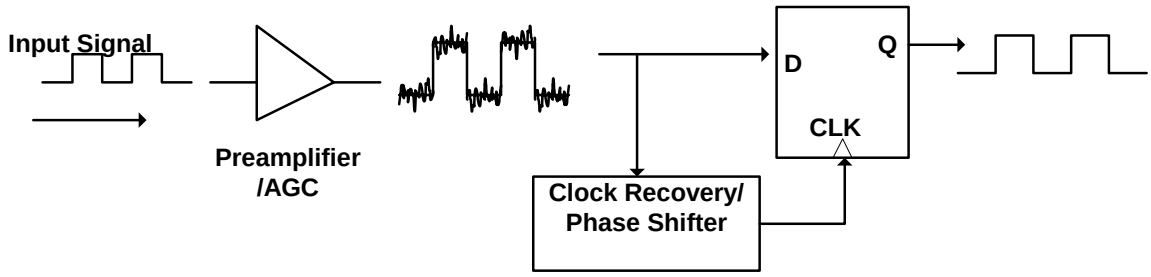

Fig. 2.4. Synchronous Data Recovery.

In Fig. 2.4, a clock recovery circuit is used to generate a clock signal at the frequency of the digital signal. This clock is then phase shifted by 90°, and used to sample the noisy data at its midpoint.

The midpoint sampling method is better, because slower rise times can be tolerated. For such synchronous receivers, the bandwidth of the TIA only has to be 0.5-0.7 times the bandwidth of the input signal. If the TIA bandwidth is 0.56 times of the signal

bandwidth of the NRZ data, the rise time is now 0.6 times the bit interval, but the noise bandwidth is now only 28% of the asynchronous detector [3].

2.5 Factors Affecting BER and Sensitivity

Two quantities that indicate the BER and sensitivity of a receiver are noise and bandwidth. Sensitivity relates to the inherent receiver noise, and quantifies the smallest signal that can be detected by the receiver, without being swamped by the receiver noise. Bandwidth is a measure of the speed of a receiver, an indication of the fastest pulse it can amplify without significant distortion.

2.5.1 Noise

The TIA in the digital receiver is the primary source of noise added to the output signal, which can result in bit errors, as in Fig. 2.5.

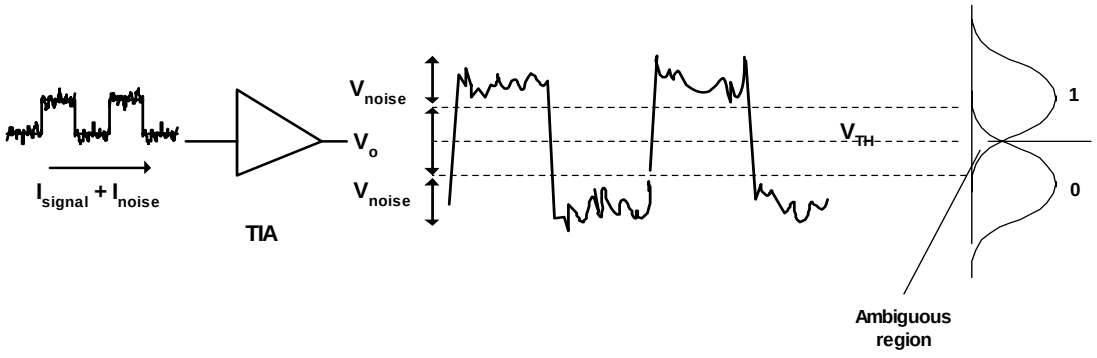

Fig. 2.5. Illustration of the Gaussian Spread of the Output Voltage of a Noisy TIA.

An input NRZ current signal I_{signal} and some photodiode current noise $\bar{I}_{noise}$ are applied to the input of the TIA. The TIA converts this input current to a voltage v_o, along with

some noise voltage $\bar{v}_{noise}$. The output noise voltage comes from the TIA and the amplified current noise of the photodiode. If the noise distribution is assumed Gaussian and signal independent [2], the variance of the output voltage level can be represented by two overlapping Gaussian curves, one for a binary **1**, and another for a binary **0**. The Gaussian curves represent the spread of the instantaneous output voltage level due to noise at any point in time. The peaks of the Gaussian curves correspond to voltage levels without any noise, the ideal case.

In order to determine if a binary signal is a **1**, or a **0**, the signal is sampled midway through the period of each pulse. For an ideal NRZ signal without noise, a voltage above the threshold voltage V_{TH} can be reliably detected as a **1**, and a voltage below V_{TH} can be reliably detected as a **0**. The addition of noise to the output voltage corrupts this certainty, and if the noise fluctuation is large enough, a binary **1** can be misinterpreted as a binary **0** and vice versa. The probability of this bit-error occurring is represented numerically by the overlap of the two Gaussian curves in Fig. 2.5, designated as the ambiguous region.

Summing up the overlapping area, the BER can be derived as [2]:

$$BER = \frac{1}{2} erfc\left(\frac{Q}{2}\right) \approx \frac{1}{\sqrt{2\pi}} \frac{\exp\left(-Q^2/2\right)}{Q} \tag{2.1}$$

where $Q = \frac{i_s^{\,pp}}{2 i_n^{\,rms}}$, $i_s^{\,pp}$ is the peak-to-peak signal current, and $i_n^{\,rms}$ is the average input referred noise current.

Equation (2.1) suggests that lowering the output noise voltage, or increasing the peak-to-peak signal level can reduce the BER. Although (2.1) shows that we can arbitrarily reduce the BER, this is not the case in practice. A BER plot for a typical receiver is shown in Fig. 2.6.

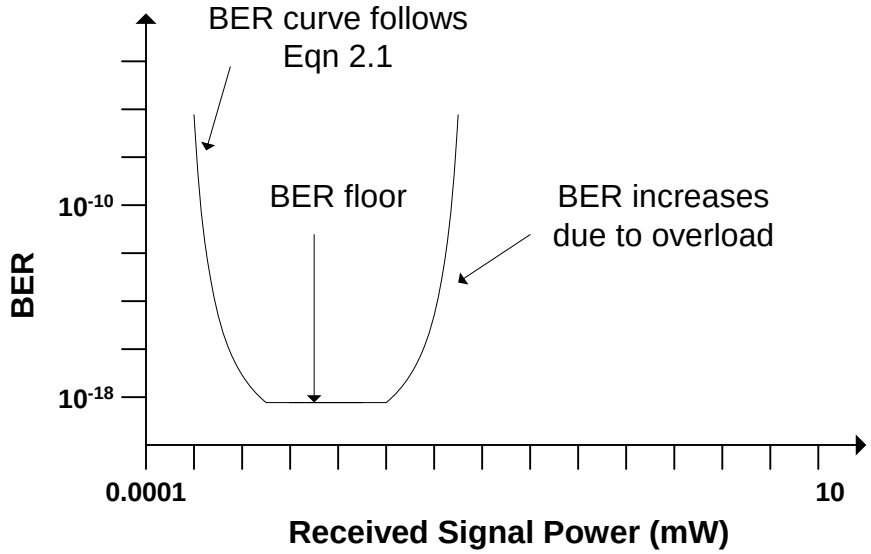

Fig. 2.6. Practical BER Curve Showing Deviation of Actual BER From (2.1).

The BER floor indicates that beyond a certain input signal power, the BER cannot be made smaller. This is missing from (2.1) because it assumes signal independent noise, an assumption that does not hold for avalanche photodiodes for example [1]. Other causes of the BER floor include clock jitter and setup/hold-time violations in digital circuits [2]. A further increase of signal power overloads the receiver, which has a finite dynamic range. This results in a BER increase.

2.5.2 Bandwidth

2.5.2.1 Low pass Filtering and Inter-Symbol Interference

The bandwidth of the receiver, and in particular, the input TIA affects the quality of the digital signal produced at the output of the receiver. Consider a bandwidth-limited TIA with a first-order transfer function that can be modeled by *H(s)* in (2.2).

$$H(s) = \frac{V_o}{I_{in}} = \frac{R_T}{1 + \frac{s}{\omega_o}} \tag{2.2}$$

where

V_o is the output voltage,

I_{in} is the input current of the TIA,

R_T is DC transimpedance gain,

and $\omega_o = 2\pi f_o$ is bandwidth of the TIA represented by the transfer function *H(s)*.

Using Simulink, the output voltage V_o in response to an input current I_{in} at 1 bit/s is plotted for several values of the bandwidth f_o, varying from 0.1Hz to 1Hz in Fig. 2.7. The DC transimpedance gain R_T has been set to unity.

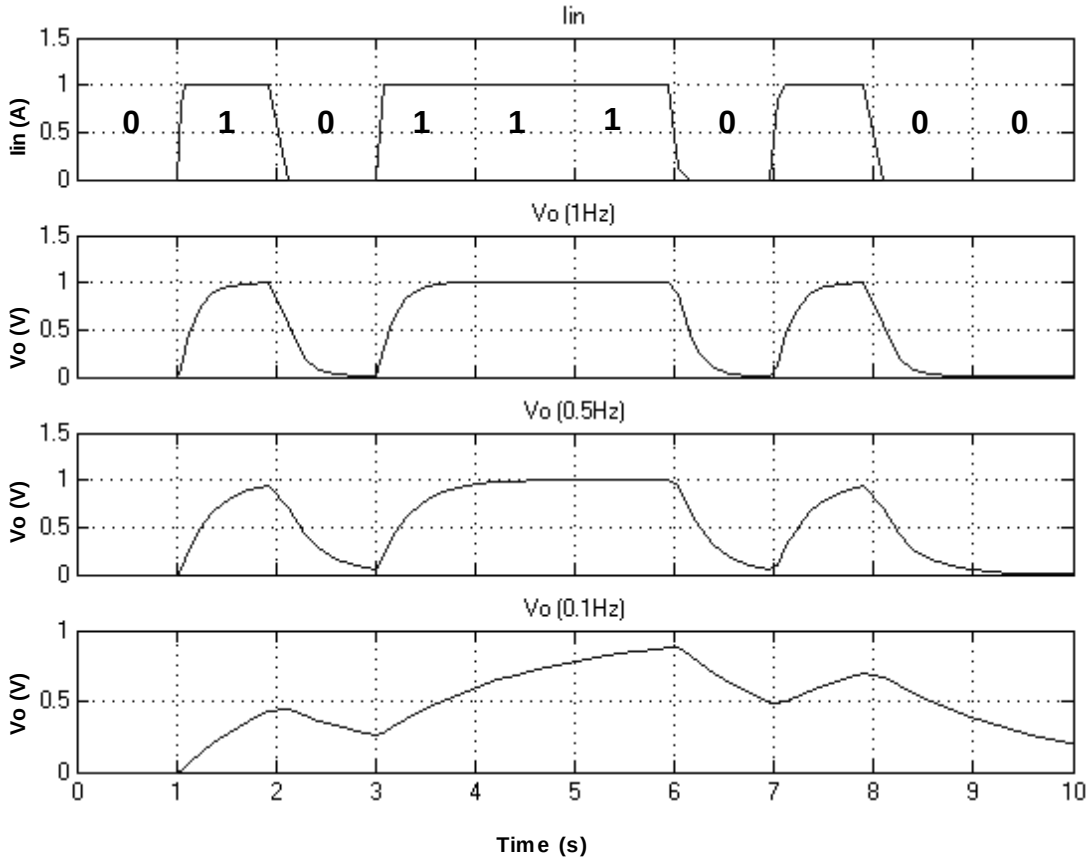

Fig. 2.7. Effect of Bandwidth-Limited TIA On Output Voltage Signal.

It can be seen that the effect of a low bandwidth is to prevent the waveform from rising fast enough, causing a synchronous detector to potentially misread a **0** as a **1**. This waveform distortion is known as Inter Symbol Interference (ISI). Typically, the bandwidth of the TIA is chosen to be about 0.75 times the bit rate of the input digital signal. However, practical input signals for photodiodes are not rectangular pulses, but have a rise/fall time that is about 40% of the bit period [2]. Therefore, a bandwidth as low as 0.6 times the bit rate is sufficient to capture the high frequency energy [3].

2.5.2.2 High pass filtering and baseline wander [4]

In high-speed amplifier design, critical amplifying transistors are typically biased with off-chip DC voltages through an inductor. The inductor is chosen such that its AC impedance is large at signal frequencies. The input signal is then coupled through a large coupling capacitor. This causes a zero at DC in the transimpedance transfer function *H(s)*. In integrated circuits, this coupling capacitor cannot be made arbitrarily large, due to area constraints. This means that the low frequency pole associated with the coupling cannot be made arbitrarily low. Modifying (2.2) to include a zero, and an additional low frequency pole, the transfer function of the TIA can be re-written as:

$$H(s) = \frac{s\ R_T}{(s+\omega_o)(s+\omega_{bias})} \tag{2.3}$$

where

$\omega_{bias} = 2\pi f_{bias}$ is pole associated with the bias implementation.

Again, a test input current is at 1 bit/s is applied to the modified TIA with unity DC gain. Here f_o is set to 1Hz, with f_{bias} varied from 0.05Hz to 0.1Hz. The results are plotted in Fig. 2.8.

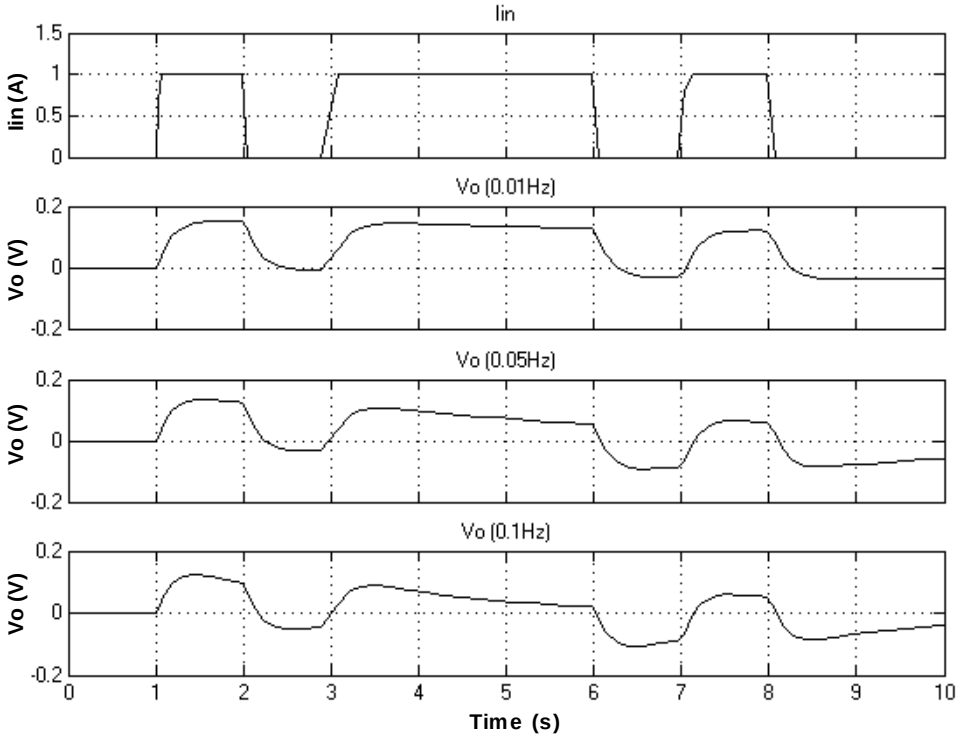

Fig. 2.8. Effect of Low Frequency Pole and Zero at DC on Signal Output.

As $\omega_{bias} = 2\pi f_{bias}$ becomes significant, the DC content of the output signal starts to droop. This is also referred to as baseline wander [4]. Conservative designs usually set the bias pole to be about 30kHz, for a 10Gb/s TIA. For this reason, it is desirable to DC-couple the input signal to the TIA to avoid any drooping, or wasting of large chip area for coupling.

2.6 Eye Diagrams

Eye diagrams are useful visual aids, to see the effects of noise and bandwidth on a digital signal. An eye diagram is formed by folding the time axis of the digital signal on itself, a whole number of bit periods at a time.

2.6.1 Transfer Functions and Jitter Analysis Using Eye Diagrams

To demonstrate the usefulness of eye diagrams, a typical 10Gb/s TIA is analyzed with Simulink using Fig. 2.9, and the results are interpreted with eye diagrams. In Fig. 2.9 below, a pseudo-random bit signal generator is used to mimic a typical 10Gb/s NRZ signal. The bit pattern is random for the first 2^{10}-1 bits. The results are displayed in Fig. 2.10.

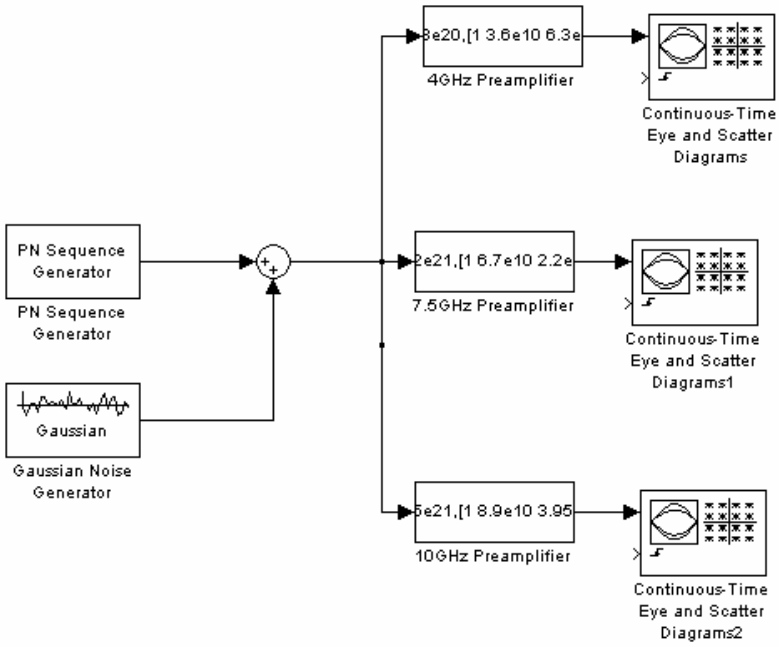

Fig. 2.9. Simulink Simulation Setup.

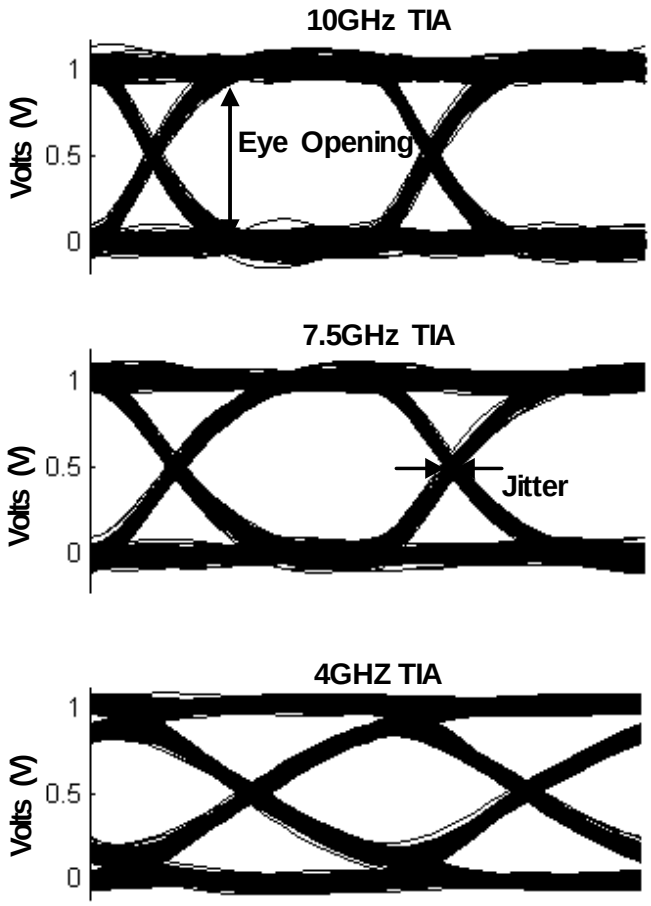

Fig. 2.10. TIA Output Voltage Eye Diagrams.

The eye opening of the eye diagrams indicates the level of ISI. The eye diagrams also reveal the amount of jitter present in the output voltage, which is the randomness of the zero crossing of the NRZ data. This is caused by additive Gaussian noise.

Fig. 2.10 illustrates the usefulness of the eye diagram. The eye closure and jitter give quick information about the frequency and noise performance of a TIA.

CHAPTER III
COMPOUND SEMICONDUCTORS AND TIA DESIGN TECHNIQUES

3.1 Compound Semiconductor Technology

Compound semiconductors such as Gallium Arsenide (GaAs) and Indium Phosphide (InP) are widely used in optical devices, because they are direct bandgap materials. This makes them more efficient at emitting and absorbing photons. Ternary compounds like Gallium Aluminum Arsenide (GaAlAs) have high quantum efficiency in the 1.0μm to 1.6μm wavelength region [5] used for optical communications. These ternary compounds can be combined in stoichiometric ratios that allow them to be lattice-matched to semi-insulating GaAs substrates. This lattice matching is critical for optimal carrier mobility [5]. Silicon (Si) is not a direct-bandgap material. This implies that optical devices like photodiodes, which require GaAs or InP substrates, have to be fabricated on a separate wafer, and then connected to a Si-based TIA on a Si wafer. The interconnect parasitics are large, and severely degrade TIA performance

This thesis uses GaAs-based technology. High-speed photoreceivers with a P-I-N photodiode integrated on the chip have been demonstrated in GaAs [6]. Laser diodes have also been fabricated on chip, alongside integrated circuits. This, along with the development of optical waveguides and modulators on chip means that integrated optical transceivers can be fabricated on the same GaAs substrate [7].

3.2 High Electron Mobility Transistors (HEMT)

HEMTs are field-effect transistors, with the gate in direct contact with a heterostructure (compound) semiconductor. It is known that high levels of doping reduce carrier mobility due to impurity scattering. The HEMT architecture circumvents this by placing a doped wide bandgap material (AlGaAs) underneath a metal gate. This is followed by a layer of narrow bandgap GaAs [5]. Application of a voltage to the gate causes carriers to be deflected from the doped AlGaAs into the undoped GaAs, where they can be used as carriers with high mobility.

The major source of noise is channel noise, which can be referred to the input as an equivalent voltage noise source, as shown in Fig. 3.1.

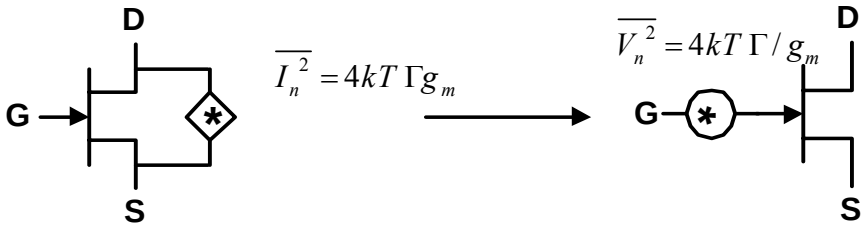

Fig. 3.1. Noise Models for the HEMT.

In Fig. 3.1, $\overline{I_n^2}$ is the HEMT channel current noise spectral density in A^2/Hz,

$\overline{V_n^2}$ is the input-referred voltage noise spectral density in V^2/Hz,

Γ is the HEMT channel noise factor which is slightly less than unity,

and g_m is the transconductance in A/V.

3.3 Heterojunction Bipolar Transistors (HBT)

In bipolar transistors, it is desirable that the base resistance r_b be small, to increase the transistor's maximum frequency of oscillation $f_{\max} = \frac{1}{2}\sqrt{\frac{f_T}{2\pi r_b C_{bc}}}$, and reduce its noise contribution. To do so, the base can be highly doped. This measure will however increase the carrier transit time τ_F through the base, and reduce the unity gain frequency $f_t \approx \frac{1}{\tau_F}$.

To ease these design constraints, HBTs have their base and emitter formed from materials with different bandgaps. This can be engineered to create a steep well in the energy band between emitter and base, allowing carriers from the emitter to flow into the base very easily, while the carriers from the base cannot overcome the energy barrier and flow into the emitter. This improves emitter injection efficiency and allows the base to be doped more heavily to reduce the base resistance of the transistor, and improve f_{max}. The heterojunction also allows the base to be made thinner, improving the base transit frequency. This shows up as an increase in f_t.

The HBT has several major noise sources, but an equivalent transformation can be done, as in the case of HEMTs [8], to refer them to the input. Fig. 3.2 below shows a corresponding noise transformation for the HBT.

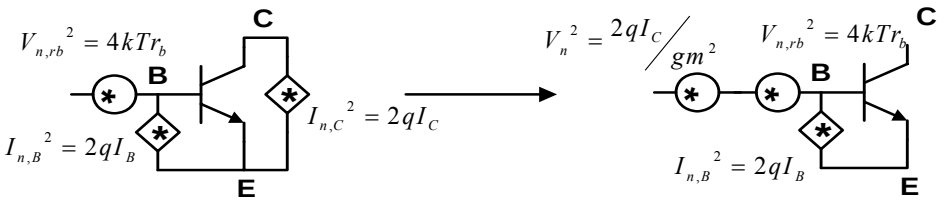

Fig. 3.2. Noise Models for the HBT.

3.4 Advantages of HBTs Over HEMTs

In spite of its worse noise properties, HBTs enjoy more popularity for optical receiver design. HBTs have better current carrying capabilities, as the current through the transistor flows vertically, perpendicular to the plane of the substrate. In HEMTs, the flow is lateral, along the surface of the substrate in a relatively thin conducting channel.

Furthermore, the critical dimensions of the HBT are formed by epitaxial growth, rather than by lithographic processes as is the case for FETs. Therefore the critical dimensions (such as base width) can be made much smaller with a cheaper process. This results in HBTs being more cost-effective than HEMTs and sub-micron CMOS.

3.5 Output Noise Dependence on Bandwidth

The noise currents and voltages represent spectral power density functions, and have units of A^2/Hz and V^2/Hz. This is because noise is statistical in nature, and its value at any instant is random. For comparison with circuit voltages and currents, a root-mean-square value can be obtained by integrating the noise spectra over the bandwidth of interest, as in (3.1).

$$\overline{I_{n,RMS}} = \sqrt{\int_{BW} \overline{I_n^2}\, df} \tag{3.1}$$

Equation (3.1) emphasizes the need to keep the bandwidth of the TIA as low as possible, to reduce the output noise.

3.6 TIA Architectures

3.6.1 Open-Loop Resistive TIA

The simplest TIA is a resistor, which performs the necessary conversion of current to voltage. A schematic is shown in Fig. 3.3.

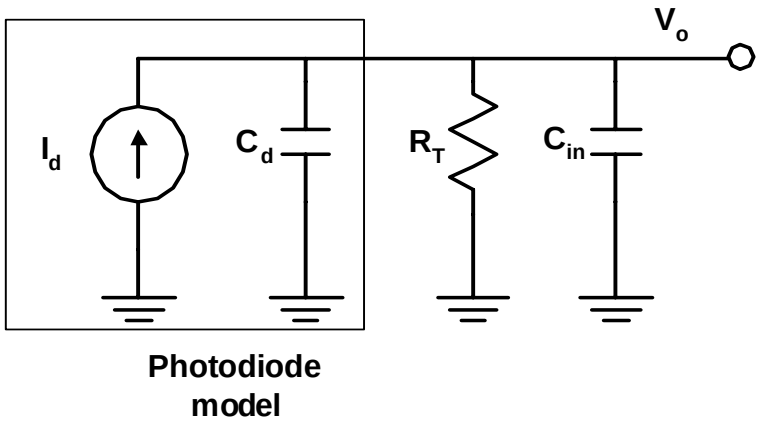

Fig. 3.3. Open-Loop Resistive TIA.

The photodiode can be modeled as a current source I_d with a parasitic capacitance C_d. R_T is the transimpedance resistance, and C_{in} represents the input capacitance of the next stage amplifier.

The transimpedance gain can be derived as

$$Z_T(s) = \frac{V_o}{I_d} = \left[R_T \parallel \frac{1}{sC_T} \right] = \frac{R_T}{1 + sC_T R_T} \tag{3.2}$$

where $C_T = C_d + C_{in}$ is the total capacitance the node V_o.

The resistance R_T contributes noise, which degrades the TIA sensitivity. We can find the equivalent input-referred noise current of this TIA by finding the output noise voltage due to R_T, and dividing by the transimpedance gain of the TIA. The output noise voltage can be derived as:

$$\overline{V_{no}^{\,2}} = \overline{I_{n,R}^{\,2}}\left[R_T \parallel \frac{1}{sC_T}\right]^2 = \frac{4kTR_T}{(1+sC_TR_T)^2} \tag{3.3}$$

Since other architectures will be considered, for a fair comparison, the output noise voltage is referred to the input. Equation (3.4) is the same as the current noise density of R_T. This result is expected since this current noise is parallel to the input current signal.

$$\overline{I_{n,ref}^{\,2}} = \frac{\overline{V_{no}^{\,2}}}{Z_T(s)^2} = \frac{4kT}{R_T} \tag{3.4}$$

To increase the sensitivity of the TIA, R_T must be large to reduce the input referred noise, from (3.4). However, (3.1) shows that doing so reduces the bandwidth of the TIA, as the pole $\omega_o = 1/R_TC_T$ decreases. Therefore, this architecture, while simple, suffers from severe design constraints. It cannot be made sensitive and fast at the same time.

3.6.2 Open-Loop Common-Gate TIA

To allow for a larger transimpedance bandwidth, a common-gate architecture is often used, as depicted in Fig. 3.4. An N-channel HEMT has been used in this design.

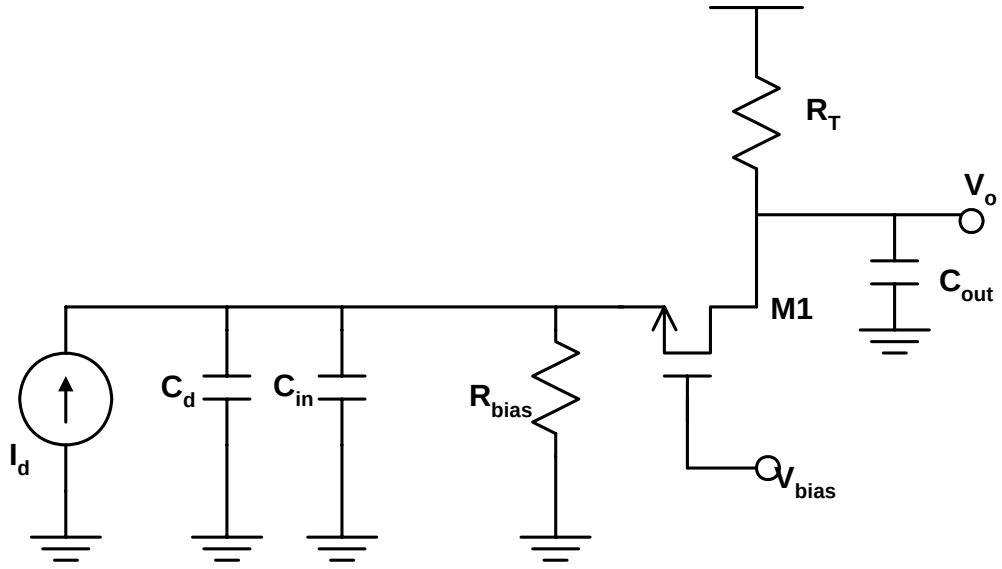

Fig. 3.4. Open-Loop Common-Gate TIA.

The input impedance looking into the transistor is now $1/g_{m1}$, where g_{m1} is the transconductance of transistor M_1. Therefore the input pole is at a very high frequency. Solving for the transimpedance gain,

$$Z_T(s) = \frac{R_T}{\left(1 + sC_T/g_{m1}\right)\left(1 + sC_{OUT}R_T\right)} \approx \frac{R_T}{\left(1 + sC_{OUT}R_T\right)} \tag{3.5}$$

Fig. 3.5 below can be used for noise analysis.

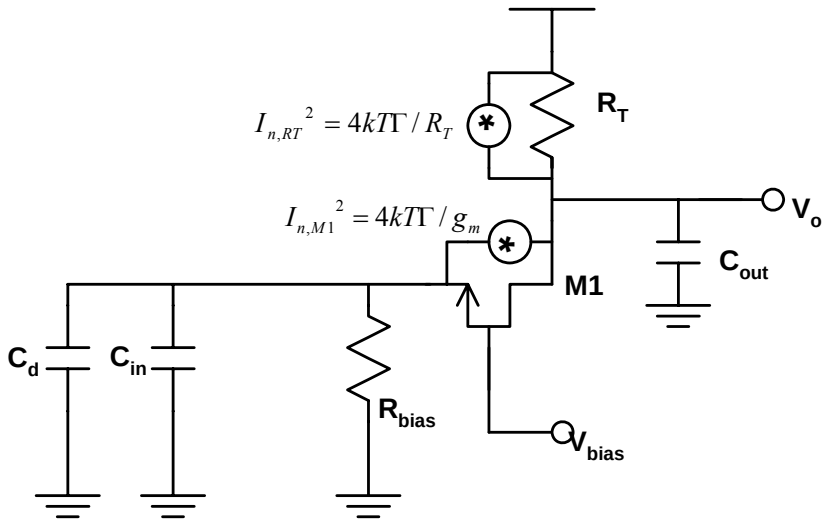

Fig. 3.5. Schematic for Noise Analysis of Open-Loop Common-Gate TIA.

To simplify the noise analysis, several assumptions are made. The bias resistor R_{bias} is much greater $1/g_{m1}$, and the impedance of the total input capacitance $C_T = C_{in} + C_d$ is smaller than R_{bias} at high frequencies. This is the primary reason for using the bias resistor in place of a current source, as its noise contribution can be neglected. The output noise voltage is given by (3.6).

$$\overline{V_{no}^2} \approx \overline{I_{n,M1}^2}\left[\frac{\frac{1}{g_{m1}}}{\frac{1}{sC_T}+\frac{1}{g_{m1}}}\right]^2\left[R_T \parallel \frac{1}{sC_{OUT}}\right]^2 + \overline{I_{n,RT}^2}\left[R_T \parallel \frac{1}{sC_{OUT}}\right]^2 \tag{3.6}$$

The input referred noise current can therefore be approximated as:

$$\overline{I_{n,ref}^2} \approx 4kT\left(\Gamma g_{m1} + \frac{1}{R_T}\right) \tag{3.7}$$

Equation (3.7) shows that the channel noise of the HEMT adds directly to the input referred noise current. Even though the pole at the input is now at a high frequency, R_T cannot be increased arbitrarily, since the capacitance C_{OUT} at the output will cause a new low frequency pole to appear. If C_{OUT} is the gate-source capacitance of an amplifying transistor, the frequency response of this architecture is degraded.

Furthermore, all the noise sources of the subsequent stage, like R_T, will appear at the input without attenuation. Therefore, the open-loop common-gate amplifier is not substantially better than its resistive counterpart. Its main advantage is to isolate the photodiode and wiring parasitics from the transimpedance load.

3.6.3 Feedback TIAs

By using feedback, high sensitivity and bandwidth can be obtained at the same time. Fig. 3.6 shows the concept of the feedback TIA.

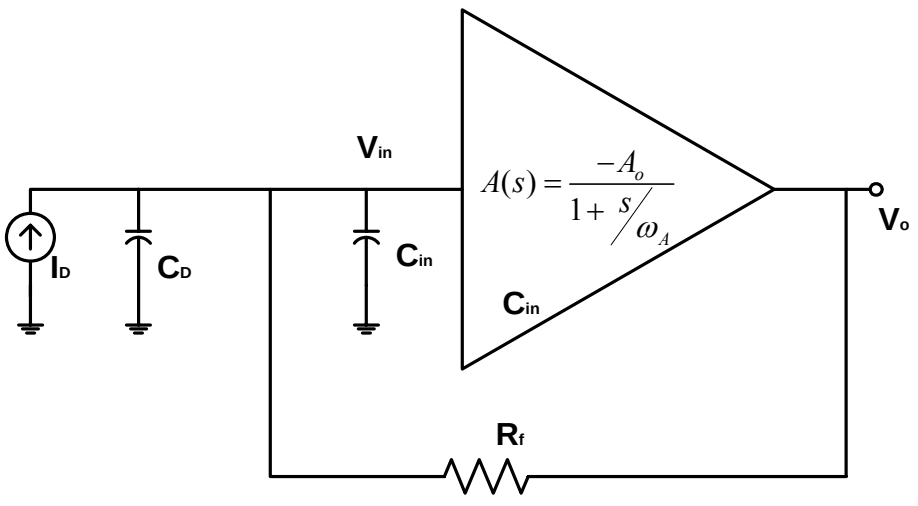

Fig. 3.6. Feedback TIA.

In Fig. 3.6, a bandwidth limited amplifier has been placed in a feedback loop. The role of the amplifier is to take the voltage V_{in}, amplify it and reverse its phase, so that V_{in} and V_o are out of phase.

If the bandwidth ω_A of the amplifier and the capacitances are initially ignored, it can be seen that this amplifier causes a current of magnitude $\frac{V_{in} + A_o V_{in}}{R_f}$ to flow through the resistor R_f to the output. This forced current comes primarily from the photodiode. Therefore, at DC and low frequencies,

$$I_D = \frac{V_{in}(1 + A_o)}{R_f} \Rightarrow I_D \propto \frac{A_o}{R_f} \tag{3.8}$$

Equation (3.8) is an advantage of the feedback TIA. The capacitors C_D and C_{in} act as low impedances at high frequency, and share the photodiode current with R_f. The output voltage is generated only by the current which passes through the feedback resistance R_f. As the frequency of operation increases, the capacitive impedances become smaller, and less useful current reaches the output. If this is taken into account, (3.8) can be rewritten as

$$I_{D,Rf} = I_D \frac{1}{1 + sC_T R_f} \frac{V_{in}(1 + A_o)}{R_f} \tag{3.9}$$

$I_{D,Rf}$ is the useful current flowing through R_f. From (3.9), the gain of the amplifier can be used to offset the low frequency pole formed at the input of the TIA, to produce more useful current at the output.

Equivalently, the input impedance of the TIA has been reduced, from R_f to $\frac{R_f}{1+A_o}$ and therefore achieves low noise and wide bandwidth simultaneously.

The limitation to the feedback TIA comes from the bandwidth of the amplifier itself, which has been neglected. The bandwidth limitation of the amplifier causes its gain to decrease with frequency, which causes the input impedance of the TIA to increase with frequency. It can therefore be said that the input impedance of the TIA is inductive in nature. To illustrate, the TIA in Fig. 3.6 is simulated using an amplifier with a 1GHz bandwidth and a voltage gain of 10. The input capacitance is 0.1pF, and the feedback resistance is 500Ω. The result is shown in Fig. 3.7.

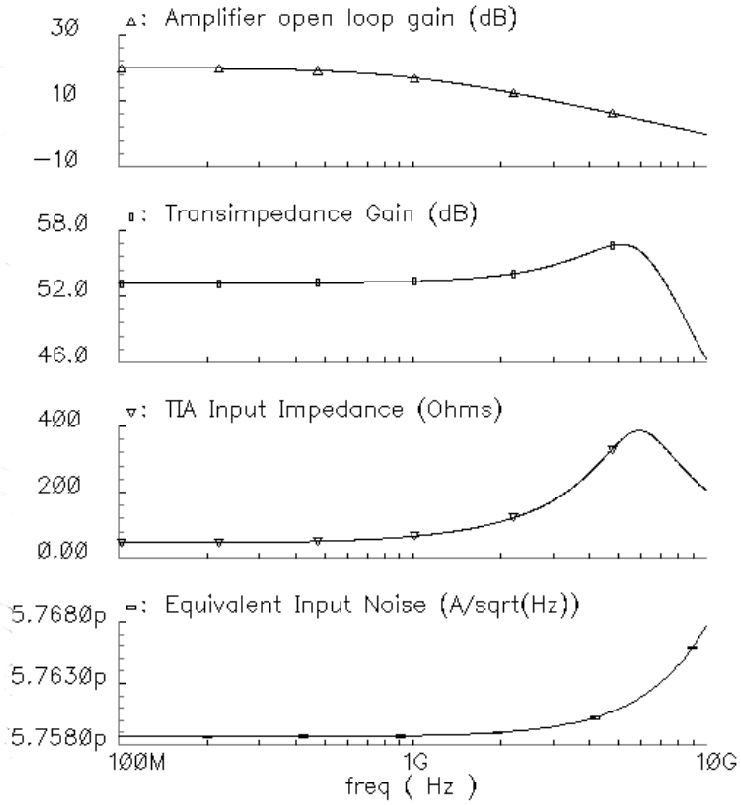

Fig. 3.7. Feedback TIA Characteristics.

As the amplifier open loop gain starts to decrease due to the pole at 1GHz, the transimpedance transfer function starts to rise. This is because the input impedance starts to rise, as the amplifier gain decreases. Eventually, the parasitic capacitances cause the input impedance and transimpedance to start to decrease again. The equivalent input referred noise current has also been plotted. It increases with frequency, because the gain decreases with frequency while the input current noise is constant. Fig. 3.7 indicates that for a realistic feedback TIA, the transfer function is at least second-order.

Solving the amplifier structure for the transimpedance gain [2],

$$R_T = \frac{A_o}{A_o + 1} Rf \frac{1}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o{}^2}} \tag{3.10}$$

where $\omega_o = \sqrt{\frac{(A+1)\omega_A}{R_f(C_D + C_{in})}}$, $Q = \frac{\sqrt{\frac{(A+1)R_f(C_D + C_{in})}{\omega_A}}}{R_f(C_D + C_{in}) + \frac{1}{\omega_A}}$

To design a TIA with a maximally flat (Butterworth) response ($Q = 1/\sqrt{2}$) and prevent peaking, from (3.10) [2],

$$\omega_A = \frac{2A_o}{R_F C_T} \tag{3.11}$$

Therefore the amplifier bandwidth must be twice the open-loop gain-bandwidth (GBW). For a Bessel response, the amplifier bandwidth must be three times the open-loop GBW [2]. This highlights the need for very fast amplifiers if ISI is to be avoided.

The amplifier bandwidth is not independent of its gain. They are related by the unity gain frequency $\omega_T \approx A_o \omega_A$. It can be shown that the limit of the feedback resistor for a TIA response without peaking is given by [2]:

$$R_f \leq \frac{\omega_T}{C_T \omega_A^{\,2}} \tag{3.12}$$

We therefore expect transistors in faster technologies to allow greater feedback resistance, with improved sensitivity and BER.

Common-source HEMT and common-emitter HBT versions of the TIA are shown below.

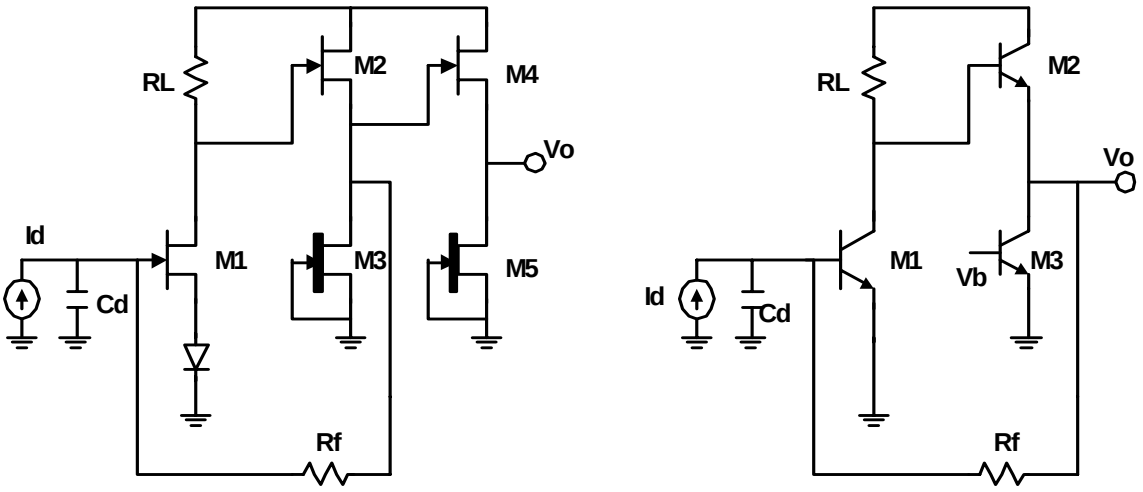

Fig. 3.8. HEMT and HBT Feedback TIAs.

The input referred noise of Fig. 3.8 TIAs can be approximated as:

$$I_{n,ref}{}^2 \approx \frac{4kT\,\Gamma}{g_{m1}}\left(\frac{1}{R_F{}^2} + (2\pi C_T)^2 f^2\right) \tag{3.13a}$$

$$I_{n,ref}{}^2 \approx \frac{2qI_C}{g_{m1}{}^2}\left(\frac{1}{R_F{}^2} + (2\pi C_T)^2 f^2\right) \tag{3.13b}$$

3.7 Difficulties Designing HEMT and HBT TIAs

3.7.1 Amplifier Front-End Capacitance

Equation (3.13) shows an f^2 component, caused by the total capacitance C_T at the input. This increases the importance of reducing the front-end capacitance. The photodiode capacitance is typically fixed, and the other option is to size the input transistor M1 for a small gate-source or base-emitter capacitance. However, reducing this capacitance will also decrease g_m, for a fixed unity gain frequency $\omega_T \approx g_m / C_{be} \equiv g_m / C_{GS}$. The lower g_m will cause the noise quantities in (3.13) to increase.

If the derivative of (3.13) is taken with respect to C_T and equated to zero, it can be proven that the minimum input-referred noise current density is obtained when the input capacitance of M_1 is equal to the photodiode capacitance. This is easier to implement with HEMTs than HBTs.

For HEMTs, the input capacitance C_{GS} is proportional to the transistor width. The width can be reduced to match C_{GS} to C_D. The drain current can then be increased, to keep g_m constant (within the limits of transistor saturation).

For HBTs, the base-emitter capacitance consists of a fixed depletion capacitance, and a diffusion capacitance that increases with current. For a particular emitter size, the capacitance has a minimum value. Attempting to increase the drain current to increase g_m will also increase the total capacitance. It is therefore harder to manipulate the input capacitance of the HBT TIA.

3.7.2 Effect of Resistive Load on Voltage Supply, Noise and Bandwidth

The loads of the amplifiers are resistors, instead of current sources. P-type HEMTs and HBTs are very slow, and are not used in high frequency design. These resistors also exhibit lower noise properties than corresponding current sources. However, they occupy more voltage headroom than active current sources, which only need a saturation voltage drop. This affects HEMTs more than HBTs. For HEMTs, the drain current of M1 must be high, to ensure sufficient transconductance. This will drop a large voltage across R_L, necessitating a larger voltage supply.

Although HBTs can use smaller currents to achieve the same transconductance, leading to a reduction in the voltage across the load resistor, the supply voltage tends to be larger. The base-emitter threshold voltage is about 1.3V for AlGaAs HBTs, while the threshold voltage for E-Mode HEMTs is about 0.3V. Therefore, typical HBT designs use 6.5V power supplies, compared to 5V for HEMTs.

Also, since HBTs have higher transconductances per unit collector current, the load resistance can be reduced to achieve a particular gain. This smaller resistance forms a higher frequency pole with the capacitance of the next stage emitter follower. Therefore, HBT TIAs have better frequency performance per unit power than HEMTs.

3.7.3 P-I-N Diode Input Impedance

The input impedance of the P-I-N diode has been assumed to be purely capacitive. However, parasitics such as bondwires and P-I-N diode packaging make the input impedance more complex. A more accurate model is shown in Fig. 3.9 [2].

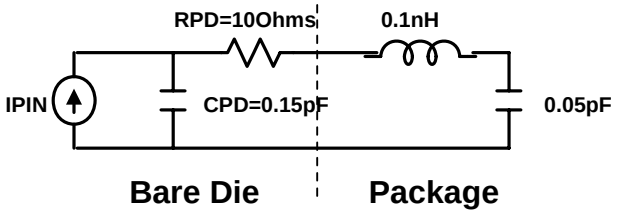

Fig. 3.9. Photodiode Equivalent.

The inductance cannot always be ignored, especially for receivers pushing the limits of the technology. This inductance causes a second-order TIA response to become a fourth order one. The effect of the inductance can be approximated using Simulink, by replacing a second order Butterworth TIA with a fourth order Butterworth TIA. The coefficient of the highest power in the denominator is then increased by 50% to simulate ringing caused by bondwire inductance. The second-order Butterworth TIA is compared with the new TIA transfer function in Fig. 3.10.

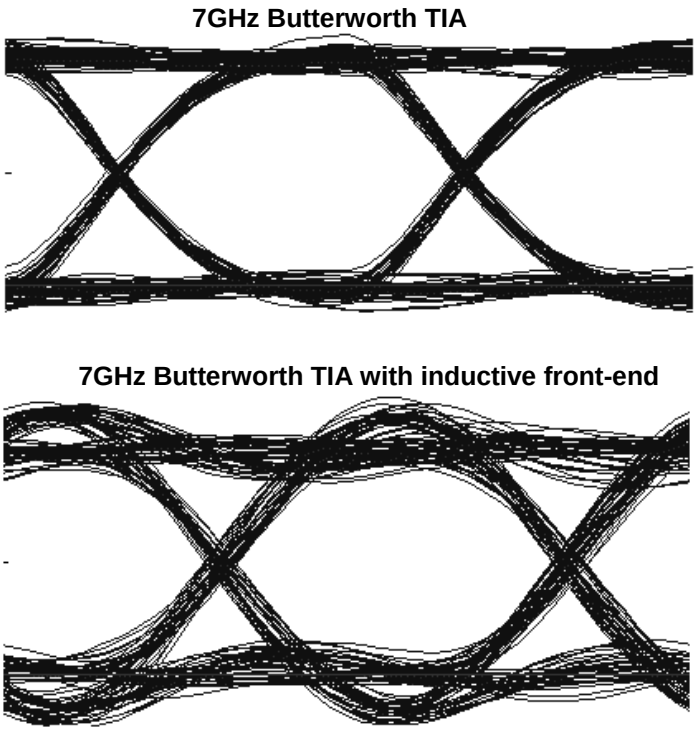

Fig. 3.10. Effect of Bondwire Inductance on 10Gb/s Eye-Diagrams.

The presence of the bondwire causes ringing, and degrades the eye diagram.

3.8 Techniques for Improving TIA Performance

3.8.1 Bandwidth Enhancement

If the bandwidth of the amplifier can be increased without decreasing gain, we can potentially increase the TIA's sensitivity and reduce ISI. Techniques such as positive feedback [9] and Vadipour's base-collector capacitance nullification [10], while capable of increasing bandwidth, are hard to control, and tend to cause too much gain peaking in the transimpedance transfer function, leading to ISI.

Inductors and ft-doubler architectures are typically used to partially cancel the effects of parasitic capacitances and reduce them respectively. Two examples are shown in Fig. 3.11.

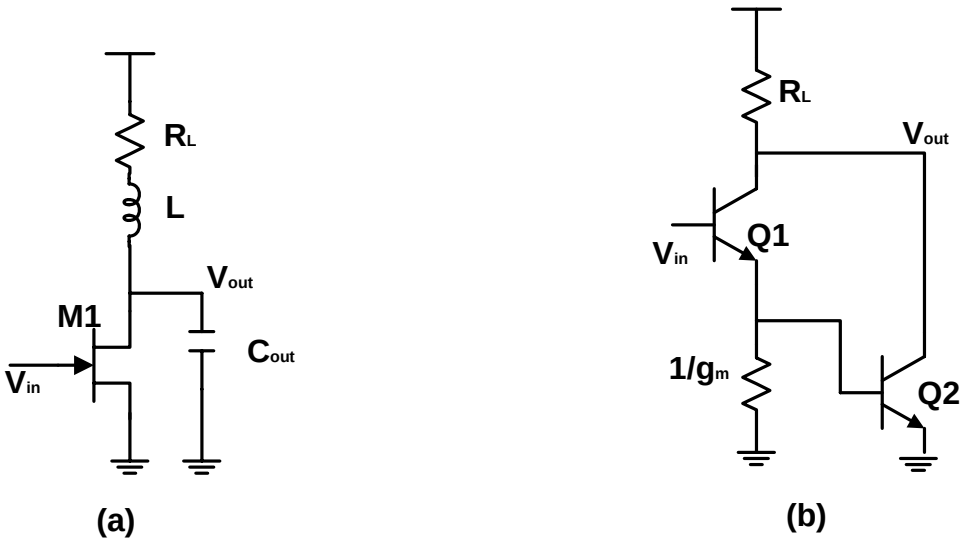

Fig. 3.11. Bandwidth Enhancement Techniques.

The HEMT amplifier in Fig. 3.11(a) uses an inductor to partially cancel the effect of the output capacitance. The price for this bandwidth extension is that the first order voltage gain transfer function becomes second order. This is an example of increasing bandwidth at the output of the amplifier.

The ft-doubler in Fig. 3.11(b) is popular in HBT designs, due to the HBT's inherently high transconductance. The voltage at the degeneration resistor is approximately half that at the input (neglecting Q_2's base resistance). This is an example of increasing bandwidth by compensating parasitics at the input of the amplifier. The input capacitance is approximately half of Q_1's input capacitance. A cascode transistor can be added to both designs to reduce the Miller effect.

CHAPTER IV
HEMT AND HBT BESSEL-TYPE TIA DESIGN

4.1. Advantages of a Bessel-Type TIA

If the circuit parasitics and bondwire inductance are taken into account, and used to design a Bessel TIA, ISI can be significantly reduced. Using Simulink, second-order and fourth-order Bessel TIAs are simulated. Also, the fourth-order TIA transfer function is modified to simulate the addition of a bondwire. Fig. 4.1 illustrates the results.

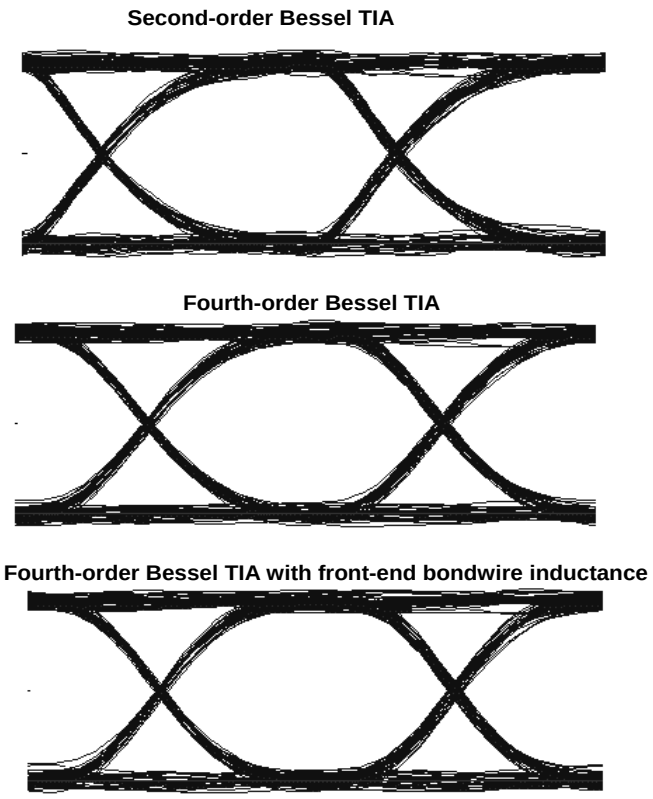

Fig. 4.1. Effect of Bondwire Inductance on Bessel TIAs.

Fig. 4.1 shows that the ISI is minimal, compared to the Butterworth TIA. There is little degradation from second-order to fourth-order in the presence of inductive parasitics, as the eye diagrams for both fourth-order transfer functions are almost the same.

The nature of the Bessel transfer function makes it relatively immune to parasitics that can cause ringing. This is a huge advantage for integrated circuit design, where the circuit parameters of the fabricated chip vary from the ideal schematic simulation, and output terminations are never purely resistive.

The fourth-order Butterworth TIA is compared with a fourth-order Bessel TIA, both operating at 5GHz. Lower bandwidths imply lower integrated noise, at the expense of increased ISI. Fig. 4.2 investigates the effect of low TIA bandwidth on Butterworth and Bessel TIAs.

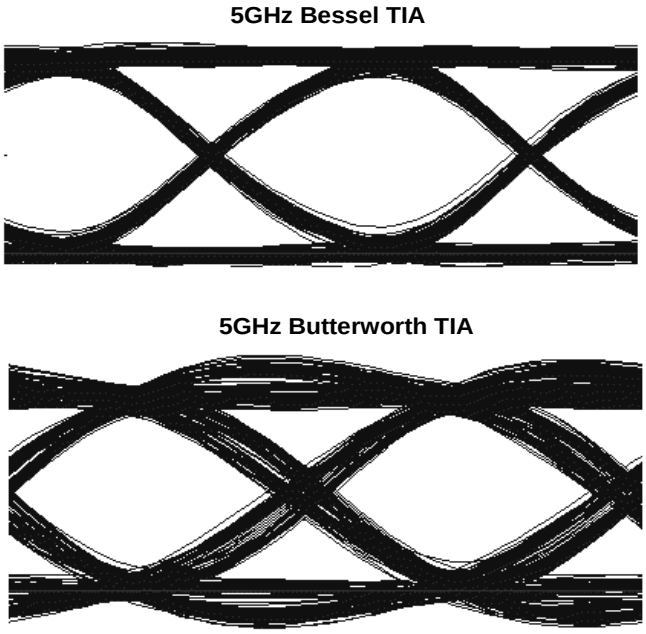

Fig. 4.2. Effect of Low Bandwidth on Butterworth and Bessel TIAs.

Even with a bandwidth at half the speed of the input signal, the Bessel TIA still has an open eye, compared with that for a Butterworth TIA. This is because as the order of the Bessel TIA increases, the constancy of its group delay over its bandwidth gets better.

4.2. Approach to Bessel TIA Design

Several attempts have been made in the literature to design Bessel TIAs. One method was to tune the poles and zeros of the TIA transfer function to obtain a constant group delay over the TIA bandwidth [11]. This approach requires accurate knowledge of all parasitics, otherwise the group delay will not be constant after fabrication.

Another approach is to solve the transfer function of the TIA with parasitics included explicitly, and then match the coefficients of a fourth-order Bessel function to the transfer function derived [12]. The method requires the use of a common source amplifier, with the bandwidth pushed to the limit. The bondwire inductance must also be known beforehand, and the sensitivity of the architecture is low due to a low feedback resistance.

This work uses a two-stage architecture, in which a fourth-order Bessel TIA is realized from two low-Q second-order stages. The stages interact in such a way that the peaking occurring in one stage can be compensated for in the other stage. Two stages, a common-base stage, and a common-emitter feedback TIA stage are used.

4.2.1 Re-Analysis of the Feedback TIA and the Resistive Peaking Effect

A popular variant of the feedback TIA introduced by Ohhata et al [13] is shown in Fig. 4.3(a).

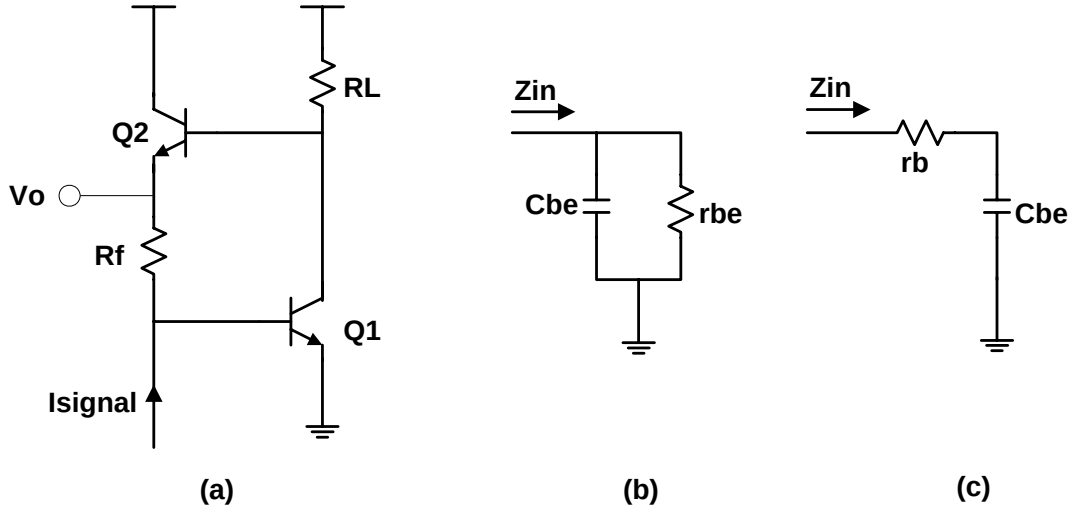

Fig. 4.3. Feedback TIA and Input Impedance. (a) Ohhata's Emitter Feedback TIA. (b) Input Impedance of HBT Used in [13]. (c) Input Impedance of HBT Used in This Work.

Q_1 and R_L form the core amplifier, with Q_2 acting as an emitter follower. In analyzing this architecture, Ohhata et. al. used Fig. 4.3(b) to represent the input impedance of transistor Q_1. The TIA transfer function was found to be second-order. However, the input impedance used neglects the base resistance, and instead includes the base-emitter resistance.

The base resistance is typically about 60Ω-100Ω and cannot be neglected in high-speed design. Furthermore, the base-emitter resistance is shunted by the base-emitter capacitance and is insignificant after a few hundred megahertz.

Secondly, the analysis in [13] assumes only one pole, at the input, formed by the base resistance and the base-emitter capacitance. The pole at the load resistor is assumed to be at a very high frequency and is ignored. This assumption is only justifiable if the load resistor R_L is small. The reasoning behind this is the intuitive need to make the frequency response of the core amplifier as fast as possible.

Re-solving the equations with Fig. 4.2(c) results in a first-order transfer function. Yet, we observe from simulation that the TIA does exhibit peaking similar to that of second-order functions. The second-order behavior comes from the input impedance of the emitter of Q_2, which has been assumed to be $1/g_{m2}$. Due to gyration by an HBT with finite transit frequency, the load resistance R_L will cause an inductive component in the input impedance of Q_2's emitter. We can designate this inductance as $L_f = \frac{R_L}{\omega_T}$.

This suggests that increasing R_L, and therefore, making the pole at that node significant, will not degrade the amplifier performance as much as was originally thought. The new transfer function parameters are displayed along with Ohhata's equations.

This work $\omega_o = \sqrt{\omega_T \omega_{RfCL}}$ $Q = \sqrt{\frac{\omega_T}{\omega_L}\frac{R_L}{R_f}}$ (4.1a)

Ohhata et. al. $\omega_o = \sqrt{\omega_T \omega_{rbCbe}\frac{R_L}{R_f}}$ $Q = \sqrt{r_b g_m \frac{R_L}{R_f}}$ (4.1b)

From (4.1a), the natural frequency ω_0 is the geometric mean of the unity gain frequency ω_T and ω_{RfCL} . In the Ohhata's solution, this other pole is dependent on the parasitic

parameters of the HBT (r_b, C_{be}). This is not as flexible for design. Equation (4.1a) suggests that we can increase R_f beyond the transimpedance limit in (3.12).

In [13], only the terms r_b, C_{be} and g_m can be used to form valid simultaneous equations to solve for ω_0 and Q. In the literature, the effect of using the assumptions in [13] is that the feedback resistance designed by different authors with different processes is almost the same for a particular operating speed.

The new equations give more freedom to use R_f and R_L in achieving a transfer function. To see the advantage of this derivation, a new transimpedance limit is derived by setting ω_0 equal to the TIA bandwidth. It should be noted that both limits are valid only for bandwidths well below the transition frequency.

$$R_f \le \frac{f_T}{2\pi C_T f_{3dB}} \quad \text{- old transimpedance limit} \tag{4.2a}$$

$$R_f \le \frac{f_T}{2\pi C_L f_{3dB}} \quad \text{- this work's transimpedance limit} \tag{4.2b}$$

where C_T is the total capacitance at the photodiode node, and C_L is the total capacitance at the common-emitter amplifier load node.

The new transimpedance limit depends on the parasitic load capacitance, while the old limit depended on the total capacitance at the input of the TIA. The new limit is therefore an order of magnitude greater than the old limit.

An intuitive way to see why this is so is to imagine the large load resistance R_L as a counterpart of the capacitive peaking method [14]. Capacitive peaking extends

bandwidth by placing a pole in an open loop amplifier with an explicit capacitance. When the amplifier is connected in feedback, this pole appears as a zero in the feedback function. To an extent, the increase in R_L also creates a lower frequency pole that can be used to peak the feedback transfer function. A larger R_f is then needed to prevent the frequency response from peaking. The same derivations can be performed using HEMTs, with the difference being that the input gate resistance and gate pole can be ignored (small gate resistance). The results are the same. Using the analysis in [13] will result in a different transfer function for HEMTs.

4.2.2 Analysis of the Common-Base Stage With Bondwire at the Input

Although the two stages of the fourth-order Bessel TIA can be implemented with two cascaded sections of the second-order architecture described earlier, a better alternative that will be immune to the front-end parasitics, while maintaining good ISI performance is needed.

The common-base architecture can achieve some parasitic immunity by keeping the signal in current mode. To this end, the common-base stage in Fig. 4.4 is investigated.

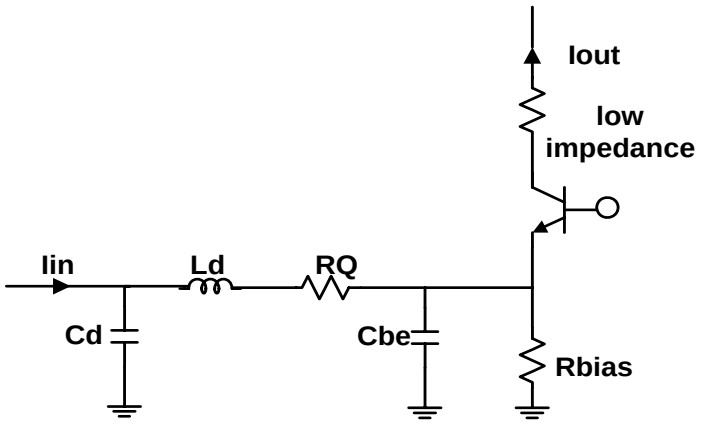

Fig. 4.4. Common-Base Input With Bondwire and Dampening Resistor.

A resistor R_Q has been added to dampen the peaking that will otherwise occur due to L_d and C_d interacting. L_d can include bondwire, packaging and explicit inductances. The resistance R_Q represents the parasitic emitter resistance, and the parasitic series resistance of the inductance L_d.

The transfer function can be expressed as:

$$\frac{I_{out}}{I_{in}} \approx \frac{1+\frac{s}{\omega_T}}{\frac{s^2}{\omega_o{}^2}+\frac{s}{\omega_o Q}+1} \tag{4.3}$$

where

$$\omega_o = \frac{1}{\sqrt{C_D\left[\frac{R_Q}{\omega_T}+L_d\right]}} \equiv \frac{1}{\sqrt{LC}} \tag{4.4a}$$

$$Q = \frac{\sqrt{\frac{\frac{R_Q}{\omega_T}+L_d}{C_d}}}{\frac{1}{g_m}+R_Q+\frac{1}{\omega_T C_D}} \equiv \frac{Z_n}{Z_{in}} \tag{4.4b}$$

Equation (4.4) shows that the second-order transfer function parameters can also be thought of in terms of an *L*-*C* natural frequency and characteristic impedance.

4.3 Two-Stage Bessel TIA With HEMTs

The two second-order stages (common-gate and common-source) investigated in 4.2 are combined to form a fourth-order Bessel TIA as in Fig. 4.5.

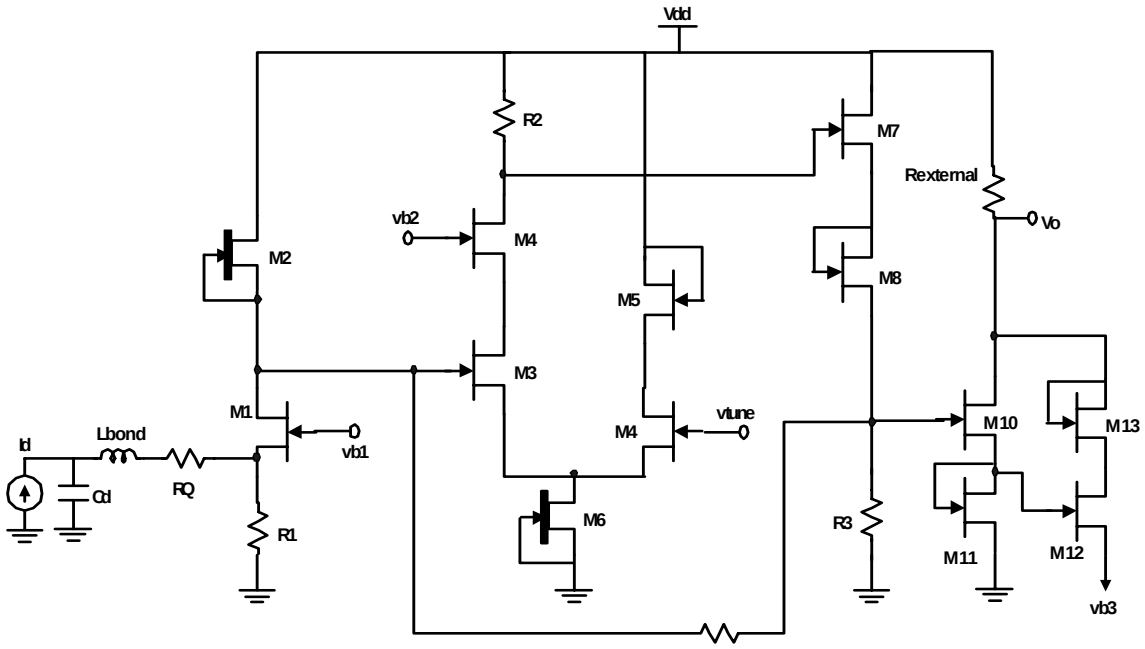

Fig. 4.5. Schematic Representation of the Two-Stage HEMT Bessel TIA.

4.3.1 Overview of HEMT Bessel TIA

The common-gate input of the TIA, along with the bondwire inductance and dampening resistor R_Q forms a second-order transfer function as discussed before. Transistor M_2 is used as a current source to supply transistor M_1. The alternative is to allow the drain current of M_1 to flow through the feedback resistor R_f [15]. This requires R_f to carry a voltage $V_{Rf} = I_{D1}R_f$. Since M_1 must be biased with a high current to present a low input impedance at its source, the power supply V_{dd} would have to be increased significantly.

The peaked current flows from the drain of M_1 into the common-source amplifier, consisting primarily of common-source transistor M_3, load R_2, feedback source-follower M_7 and resistor R_f. The cascode transistor M_4 broadens the frequency response of the common-source amplifier by reducing the Miller effect at the gate of M_3.

GaAs processes are relatively immature compared to their silicon counterparts. For HEMTs especially, transistor size precision is low, and can vary up to 40%. However, the precision of the ratio of the HEMT transistor sizes is high. In order to reduce the quiescent point variability due to manufacturing, transistors M_4, M_5 and M_6 are added to the common-source amplifier. Transistor M_6 is a current source. The amount of current flowing through the common-source amplifier is determined by the voltage v_{tune} at the gate of M_4. M_5 is used to drop the voltage at the drain of M_4. This method is preferred to using level-shifting diodes to bias the source of transistor M_3. These level shifting diodes have to be bypassed with a large capacitor, otherwise, they severely degrade the amplifier's group delay. The input impedance of the source of M_4 can be made arbitrarily low, and has little effect on the group delay. Similarly, the voltage drop at the source follower is implemented with a gate-drain connected transistor rather than a level shifting diode, due to the self-bypassing action of its gate-source capacitance.

Typically, the output of a standalone TIA chip is a common-source driver, which must be capable of driving 25Ω - 50Ω [4]. The driver transistor must be large enough to sustain a substantial drain current. This large driver input capacitance interacts with the source-follower of the TIA, causing peaking and degrading the group delay. In the literature, several source followers are used to isolate this driver. This is usually ineffective, as the drain current of these source followers must be reduced to dampen peaking. Cascading several of these results in severe gain and bandwidth loss. Instead, a resistor R_3 was used as the current source to provide more damping. The driver M_{10} is degenerated, to reduce the input capacitance presented to the source follower. In order to

reduce quiescent current consumption, the output of the driver is open-collector, to be connected to an external 50Ω output. A disadvantage of the open-collector configuration is the possibility of jitter and ringing at the output [4].

In order to fully realize the bandwidth of the TIA, the gates of the input and cascode transistors must be at a low impedance over a broad range of frequency [16]. Fig. 4.6 shows several methods used for cascode and common-gate transistor biasing.

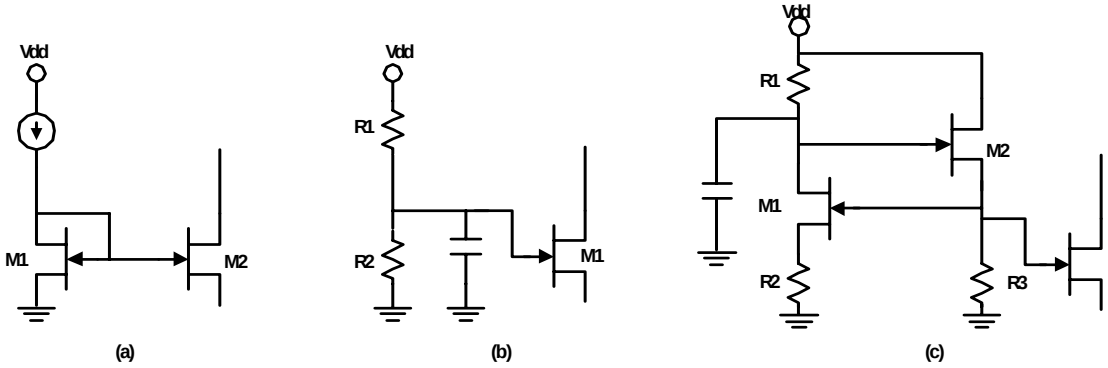

Fig. 4.6. Techniques for Cascode and Common-Gate Transistor Biasing.

Fig. 4.6(a) is typical for low frequency biasing. However, the impedance at the gate is not low enough at high frequencies. Fig. 4.6(b) is a resistive divider, with a capacitor to roll off the impedance of $R_1 \| R_2$ at high frequencies. In order to maintain low AC impedance, this capacitance must be large. Since resistors R_1, R_2 are usually large to reduce current consumption from the power supply, the capacitance must be on the order of 50pF-100pF.

Fig. 4.6(c) uses a current mirror biasing technique for BJTs, along with a capacitance reduction concept from Rodwell [16]. The source follower presents a low, relatively frequency-independent input impedance over a broad range of frequencies. The bias

resistor R_1 appears as an inductance at the source of M_2. Its effect is reduced by a small capacitance, about 5pF. This architecture performs better than the regulated cascode approach [17], [18] from a group delay and noise performance perspective.

4.3.2 Fourth-Order Bessel Filter Design

A fourth-order Bessel transfer function can be separated into a cascade of two second-order transfer functions as in (4.5).

$$\frac{V_{out}}{I_{in}} = \frac{R_f}{1 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4} = R_f \frac{1}{\frac{s^2}{\omega_{o1}^2} + \frac{s}{\omega_{o1} Q_1} + 1} \frac{1}{\frac{s^2}{\omega_{o2}^2} + \frac{s}{\omega_{o2} Q_2} + 1} \tag{4.5}$$

Using MATLAB, the parameters ω_{o1}, Q_1, ω_{o2}, Q_2 were determined for (4.5) using MATLAB for a bandwidth of 7GHz in Table 4.1.

The common-gate stage of 4.2.2 is more suited to high bandwidth, high Q amplifier design and is used to implement stage 1. The common-source stage of 4.2.1 is used to implement stage 2.

TABLE 4.1

SECOND ORDER FILTER PARAMETERS FOR A FOURTH–ORDER BESSEL FILTER WITH A BANDWIDTH OF 7GHZ

Second-order parameter	Calculated value
ω_{o1} (stage 1)	11 GHz
Q_1 (stage 1)	0.81
ω_{o2} (stage 2)	9.9 GHz
Q_2 (stage 2)	0.52

Stage 1 in Fig. 4.5 comprises of the photodiode model (C_d, L_d, and R_Q), and the common-gate amplifier (M_1, M_2, R_1). The second-order transfer function parameters (ω_{o1}, Q_1) for the current gain from the photodiode to the drain of M1 are expressed in (4.4). Stage 2 in Fig. 4.5 comprises of the common-source amplifier (M_2 - M_8, R_2, R_3, and R_f). The second-order transfer function parameters (ω_{o2}, Q_2) for the voltage gain from the gate of M3 to the source of M8 is expressed in (4.1). Table 4.2 lists the circuit parameters calculated according to Table 4.1, (4.1) and (4.4).

TABLE 4.2

COMPONENT DESIGN PARAMETERS FOR THE HEMT TIA IN FIG. 4.5

M1	60µm/6
M2*	18µm /6
M3, M4, M5, M5a, M7, M8, M10	30µm /6
M6	54µm /6
M9	54µm /6
M11 - M14	30µm /6
Lbond	1.1nH
RQ	10 Ω
Cd	100fF
Rf	2.8kΩ
R1	500Ω
R2	400Ω
R3	800Ω

* A small 5µm DFET not shown was inserted above M2, to provide bias and prevent DC current flow through R_f.

4.3.3 Layout of the HEMT Bessel TIA

The layout, extraction and verification of the HEMT Bessel TIA in Fig. 4.7 were done using Cadence.

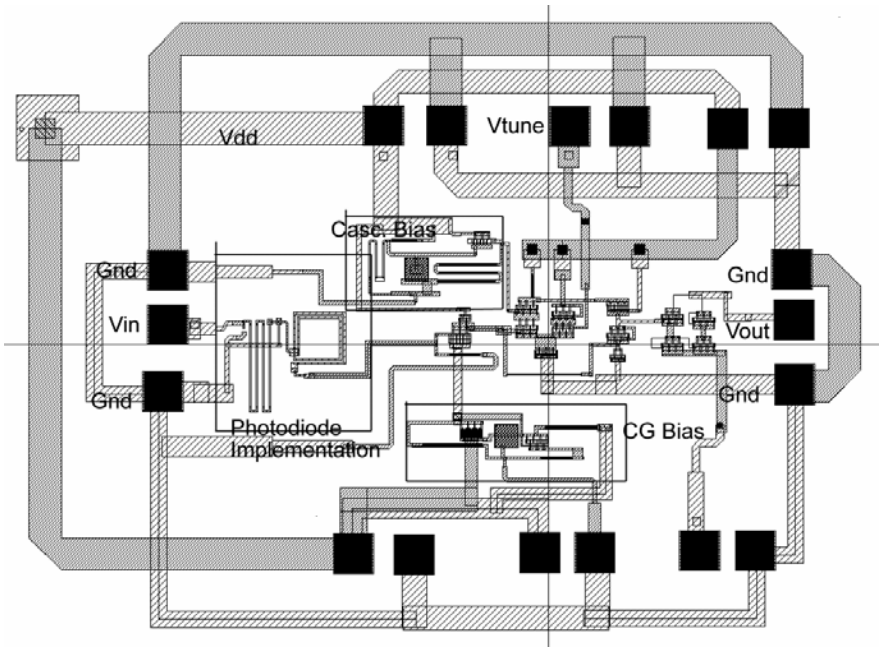

Fig. 4.7. Layout of the Bessel Type HEMT TIA.

The photodiode was implemented on chip with a 10kΩ resistor and 100fF capacitance [11]. The bondwire was implemented as a spiral inductor. Since the inductor's parasitic resistance can be lumped with R_Q, more attention was paid to reducing its parasitic capacitance by reducing the line width to the minimum allowed by the technology.

The input and output signals use a Ground-Signal-Ground (G-S-G) configuration to minimize parasitic inductance in their paths.

4.3.4 Simulation and Results

The TIA was simulated using Triquint's 0.5μm 33GHz HEMT process in Cadence and Agilent's ADS. S-parameter simulations and curve fitting in ADS were used to extract the transistor's physical parameters. The layout was drawn in Cadence, exported to a GDSII format, and the parasitics extracted with an electromagnetic simulation in

Momentum ADS. Only node capacitances were extracted to reduce simulation time. The metal-insulator-metal (MIM) capacitors were found to be fairly ideal and were simulated separately to verify their properties. The anticipated parasitic inductance of the long NiCr resistors was reduced by using a serpentine structure.

In optimizing the design, more attention was paid to optimizing the group delay than to the bandwidth. Fig. 4.8 shows the AC response.

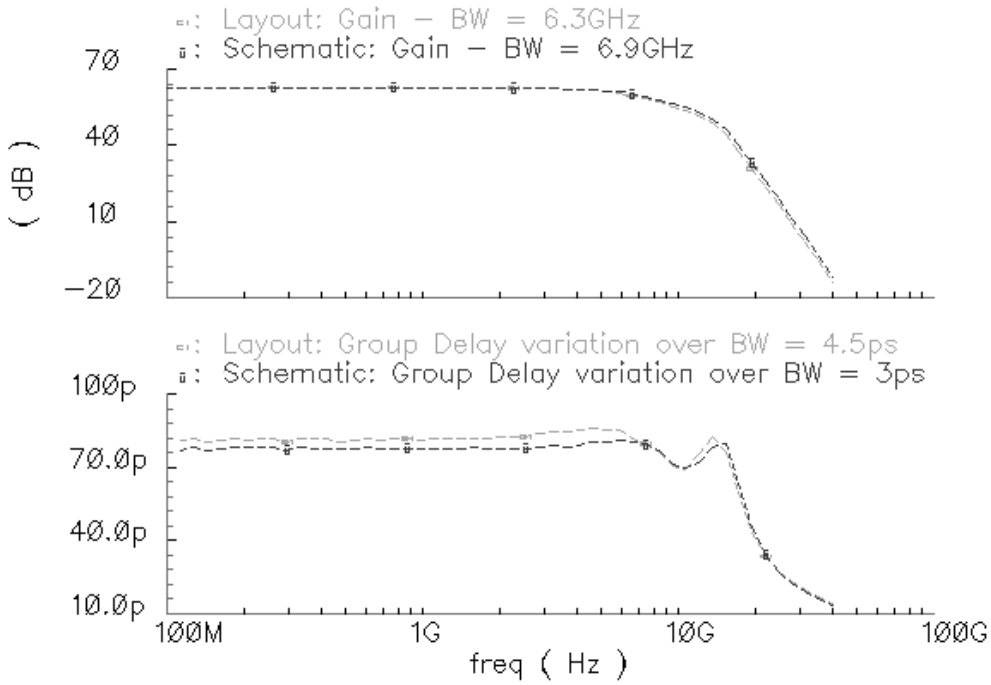

Fig. 4.8. AC Response of the HEMT TIA.

The bandwidth reduces drastically with the inclusion of layout parasitics. It is difficult to reduce this effect, due to the multiple-gated transistors used. The multiple gates are connected with the lowest level metal (local interconnect), and make up an un-modifiable bulk of the layout capacitance [19].

Fig. 4.9 compares the step response of the schematic and layout.

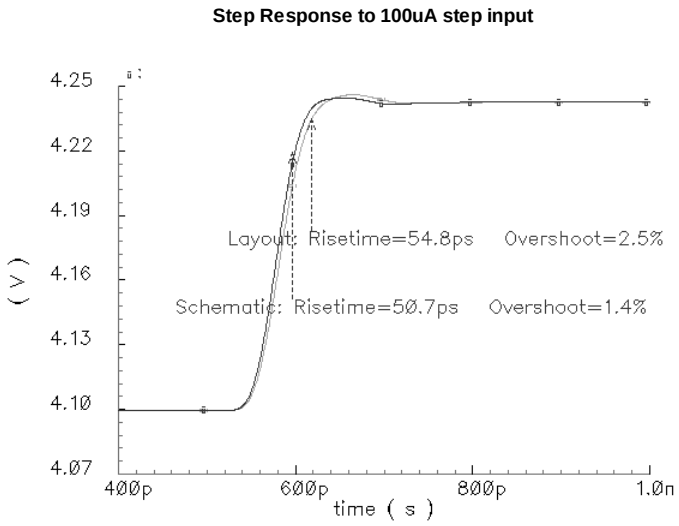

Fig. 4.9. Step Response of the HEMT TIA.

As expected, there is little overshoot in the step response due to the constant group delay over the amplifier bandwidth. Fig. 4.10 shows the output voltage noise power spectra of the HEMT TIA layout.

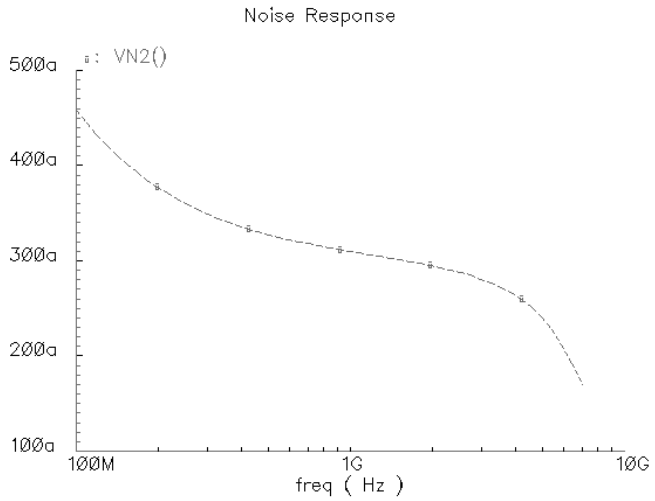

Fig. 4.10. Output Noise of the HEMT TIA (Layout).

As expected, in Fig. 4.10, the output noise decreases with frequency due to the shunting effect of parasitic capacitances.

Fig. 4.11 shows the eye diagram of the TIA layout output in response to a 2^{11} –1 pseudo-random bit sequence at 10Gb/s. Fig. 4.11 shows that the TIA exhibits almost no eye closure

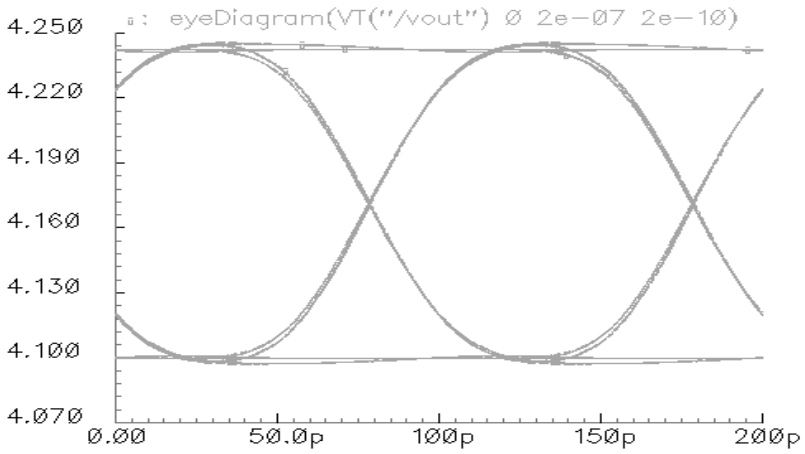

Fig. 4.11. Eye Diagram of the HEMT TIA.

The results are tabulated in Table 4.3.

TABLE 4.3

POST-LAYOUT SIMULATION RESULTS FOR THE HEMT TIA

Bandwidth	6.3 GHz
Input Referred Current Noise	11 $pA/\sqrt{Hz}$
Transimpedance Gain	1.4kΩ (Rf=2.8kΩ)
Group Delay Variation Over Bandwidth	4.5ps
Power Consumption	200mW
Power Supply	5V
Risetime	47.7ps
Chip Area	$3mm^2$

4.4. Ft-Doubler Bessel-Type HBT TIA With Shunt Peaking

The architecture used for the HEMT TIA can also be applied to HBTs. However, it is not as efficient. The base-emitter capacitance of the HBT is much larger, and increases with collector current. This leads to significant bandwidth reduction at the common-base/common-emitter TIA interface.

Furthermore, a low-noise, single transistor current source is not possible with HBTs, as only n-p-n transistors are available. This presents biasing problems. Finally, the input impedance of the AlGaAs HBT is more complicated and the assumptions made in Section 4.2 are only valid until about a third of the unity gain frequency [20].

It is difficult to derive simple transfer functions with sufficient accuracy for the performance level needed. Instead, the HBT TIA is designed with an alternate definition of the Bessel transfer function.

As long as the group delay is fairly constant over the bandwidth of interest, we can approximate a Bessel type response with little overshoot. This is evident from Gaussian and Pade group delay approximations, which are not Bessel transfer functions, but nevertheless have good group delay and time response characteristics.

The common emitter TIA (CETIA) is re-investigated. The primary problem with the CETIA is that the capacitance of the input transistor adds directly to the capacitance of the photodiode, and reduces the size of the feedback resistor for a particular bandwidth. This in turn reduces the TIA's sensitivity.

A current-mirror ft-doubler configuration is used, to reduce the input capacitance. The Darlington configuration, while providing a very low input capacitance, suffers from stability problems, resulting in severe ringing [21]. Fig. 4.12 illustrates several architectures.

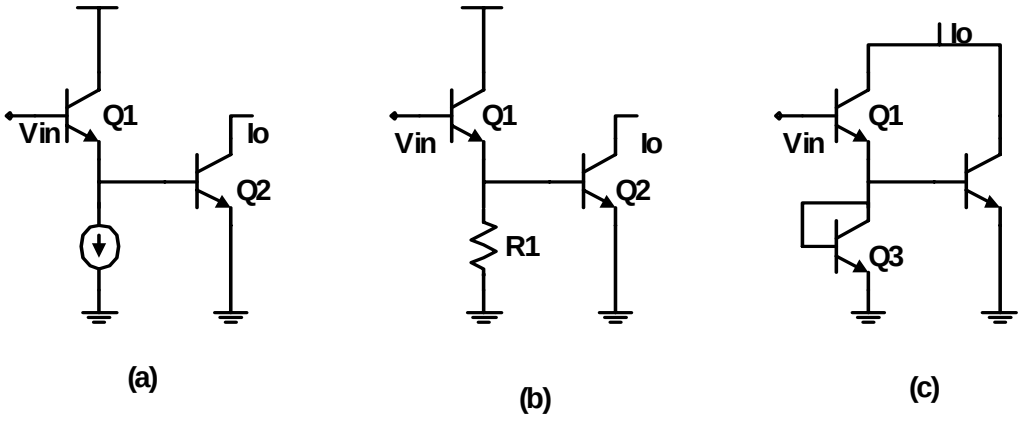

Fig. 4.12. Design Evolution of the Current-Mirror Ft-Doubler.

Fig. 4.12(a) shows the Darlington configuration. Although the input capacitance can be reduced to very small values, it comes at the price of severe ringing. The transfer function for the each of the architectures can be approximated by $H(s) = \frac{1}{a_2 s^2 + a_1 s + 1}$ [22]. Using the method of open-time constants (MOTC), Agarwal [23] showed that although the Darlington configuration increased the bandwidth, a_2 increases too, resulting in severe peaking in the transfer function. Since the emitter-follower Q_1 is driving a capacitance, the input impedance has a frequency dependent negative resistance, which can only be compensated for with a huge series base resistance [21].

To reduce the peaking, Fig. 4.12(b) can be used, where R_1 is a small bias resistor. This significantly improves switching time. This can be modified by using transistor Q_3 for bias, and connecting the collector of Q1 and Q2 together. It can be shown by MOTC and current gain analysis that this introduces a zero, which partially offsets the pole introduced by the configuration [22], [23]. This is referred to as the current-mirror ft-doubler. This second-order front-end can be used in a common-emitter TIA to give a fourth-order Bessel type response. The full architecture is shown in Fig. 4.13.

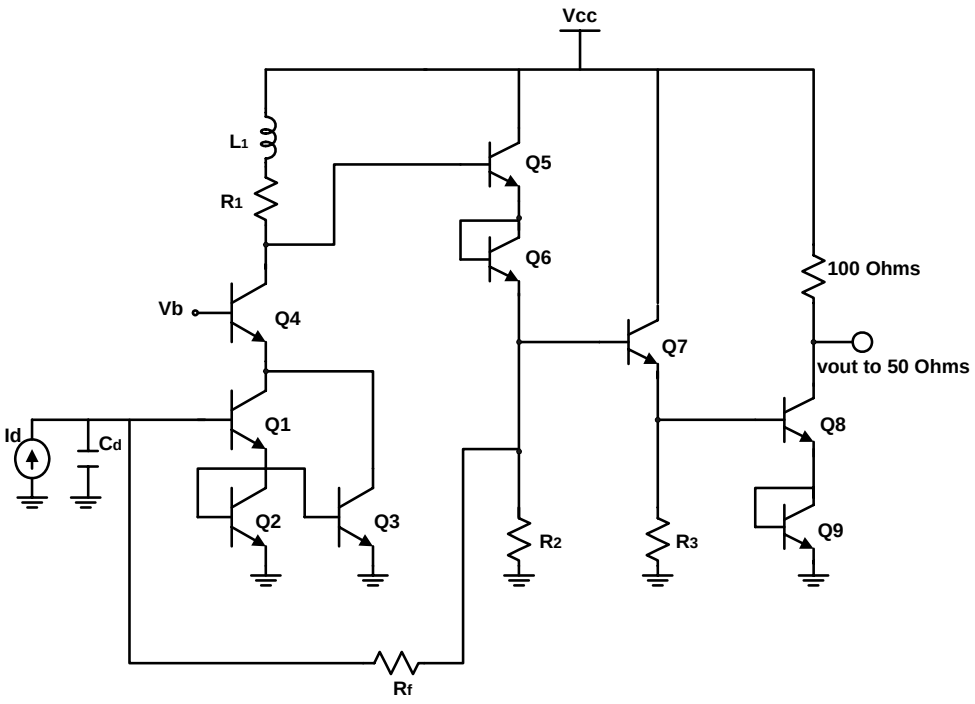

Fig. 4.13. HBT TIA Using an Ft-Doubler and Shunt Peaking.

4.4.1 Overview of HBT Bessel TIA

In Fig. 4.13, the input bondwire is considered to be negligible. This is the case if the shortest possible bondwire is used, or flip-chip bonding is used. In either case, simulations show that a larger feedback resistor can offset the effect of the bondwire. In order to reduce the noise added by the extra front-end transistor, shunt peaking is used at the collector of Q4 to broaden bandwidth, allowing a larger feedback resistor to be used. This in turn improves noise performance.

Transistors Q_1, Q_2, Q_3 form the input current-mirror ft-doubler, and the cascode transistor Q_4 reduces the Miller effect, thereby broadening bandwidth. Inductor L_1 allows the collector current of Q_4 to charge the load capacitance more quickly, by initially isolating the load resistor R1 from the current coming out of the collector of Q_4.

The source follower Q_5 is biased with a resistor instead of a current source. This helps reduce the ringing that occurs in driving the large base emitter capacitance of the driver Q_8. The output load is 100Ω, to interface to a 50Ω load. The load is 100Ω instead of 50Ω, to reduce the quiescent current requirement [4], and dampen possible jitter caused by off-chip inductances [11]. Q_9 is used for biasing, and to reduce the input capacitance of the driver.

All transistors run at about 65% of the maximum current density allowed (0.2mA/μm^2), for peak f_t.

4.4.2 Fourth-Order Bessel Filter Design

As in 4.3, a fourth-order Bessel transfer function can be derived from Fig. 4.13. The transconductance of the current-mirror ft-doubler (Q_1, Q_2, *and* $Q3$) can be approximated by [22]

$$G_m = \frac{g_{m1}}{1 + \frac{2s}{f_t}} \tag{4.6}$$

Solving for the transimpedance gain of Fig. 4.13,

$$\frac{V_{out}}{I_{in}} = \frac{R_f\left(1 + s\frac{L_1}{R_1}\right)}{1 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4} \tag{4.7}$$

where $a_4 = \dfrac{2R_f C_L L_1 (C_d + C_{in})}{g_{m1} R_1 \omega_T}$,

$$a_3 = \frac{2C_L L_1 + 2C_d C_L R_f R_1 + 2C_{in} C_L R_f R_1 + C_d C_L L_1 R_f \omega_T + C_{in} C_L L_1 R_f \omega_T}{g_{m1} R_1 \omega_T} ,$$

$$a_2 = \frac{2C_d R_f + 2C_{in} R_f + 2C_L R_1 + C_L L_1 \omega_T + C_L R_1 R_f \omega_T (C_d + C_{in})}{g_{m1} R_1 \omega_T} ,$$

$$a_1 = \frac{2 + g_{m1} L_1 \omega_T + C_d R_f \omega_T + C_{in} R_f \omega_T + C_L R_1 \omega_T}{g_{m1} R_1 \omega_T} ,$$

C_L = Total node capacitance at the base of Q_5 and

C_{in} = Total node capacitance at the base of Q_1.

Ignoring the high frequency zero in (4.7), the coefficients in (4.7) must be matched to the coefficients of the MATLAB derived fourth-order Bessel filter with a bandwidth of 7GHz in (4.8).

$$\frac{V_{out}}{I_{in}} = \frac{1}{1 + 2.08*10^{11} s + 1.95*10^{22} s^2 + 9.46*10^{32} s^3 + 1.97*10^{43} s^4} \tag{4.8}$$

Four simultaneous equations, in which R_f, R_1, C_L and L_1 are unknowns can be formulated. Since C_L is dependent on parasitic capacitances, several iterations are needed. The parasitic substrate capacitances of L_1 which were ignored in the derivation of (4.7) cause the simulated transfer function to deviate from that expected, necessitating further tuning of R_f and R_1. To ease tuning, the constancy of the group delay of the transimpedance gain is used as the benchmark, rather than the gain. The values designed are tabulated in Table 4.4.

TABLE 4.4

COMPONENT DESIGN PARAMETERS FOR HBT TIA IN FIG. 4.13 (TRANSISTOR DIMENSIONS ARE OF THE FORM FINGERS X EMITTER WIDTH X EMITTER LENGTH)

Q1, Q2, Q3	1x3µmx5µm
Q4	2x3µmx5µm
Q5, Q6, Q7	1x3µmx7µm
Q8, Q9	2x3µmx5µm
Rf	1.6kΩ
R1	170Ω
R2	1.2kΩ
R3	1kΩ
L1	1nH

4.4.3 Layout of the HBT Bessel TIA

The layout illustrated in Fig. 4.14 was drawn, extracted and verified with Cadence.

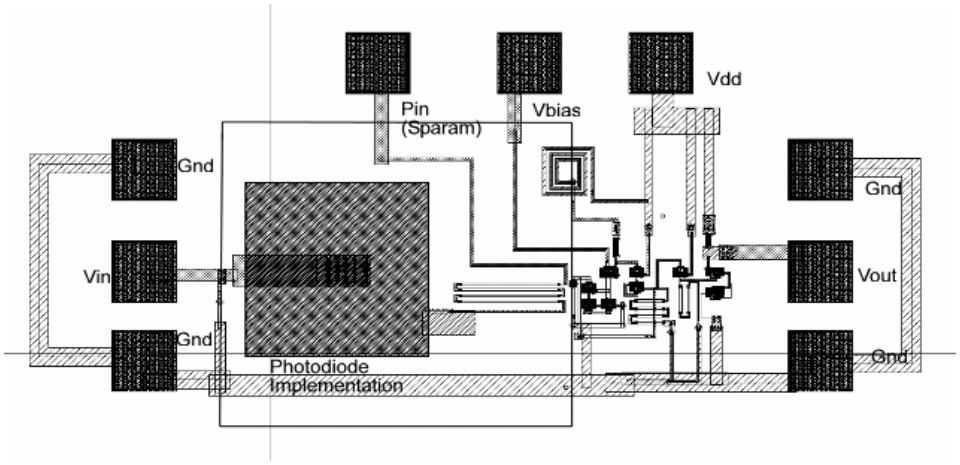

Fig. 4.14. HBT TIA Layout.

The photodiode in the layout above has a huge input capacitance (100pF) for DC bias blocking, as the base current of the HBT is large enough to cause a DC shift at the input.

4.4.4 Simulation and Results

Triquint's 40GHz AlGaAs HBT process was used for the design, simulation and layout of the HBT TIA. Fig. 4.15 shows the AC response of the HBT TIA.

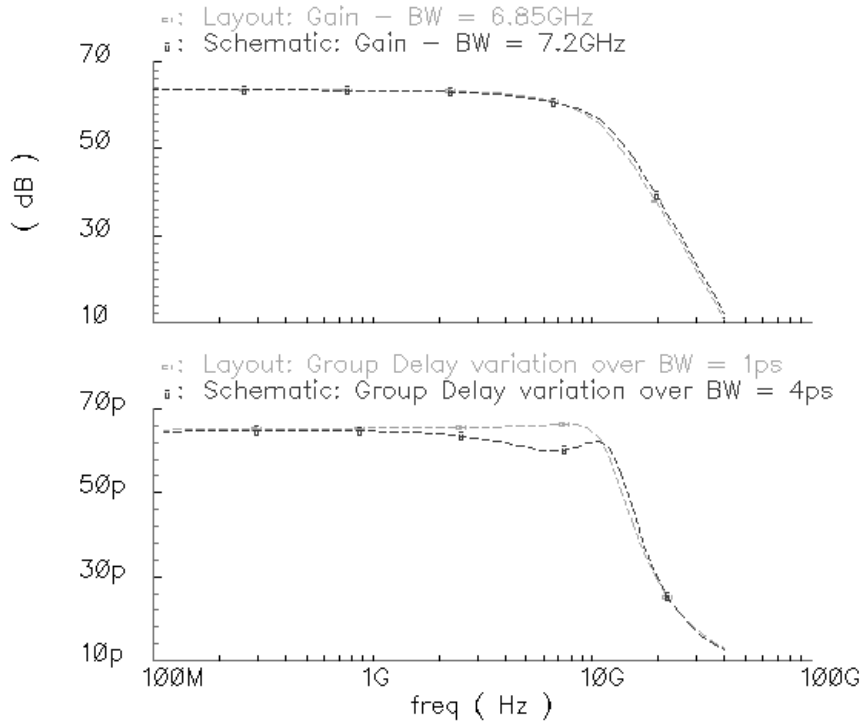

Fig. 4.15. AC Response of the HBT TIA.

The group delay with the parasitics exhibits better Bessel properties because the feedback resistance was purposely increased to reduce the peaking effect of the parasitic capacitances. The bandwidth of the layout was close to that of the schematic because the highest level interconnect (*Metal2*) was used as often as possible. The local interconnect *Metal0* was avoided as much as possible.

Fig. 4.16 shows the step response of both the schematic and layout.

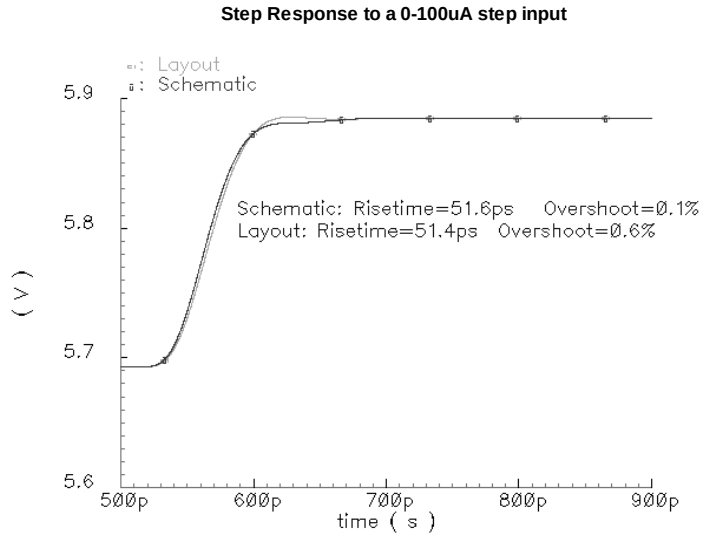

Fig. 4.16. Step Response of the HBT TIA.

There is very little ringing in the step response as expected. Fig. 4.17 shows the output noise spectral density of the HBT TIA layout.

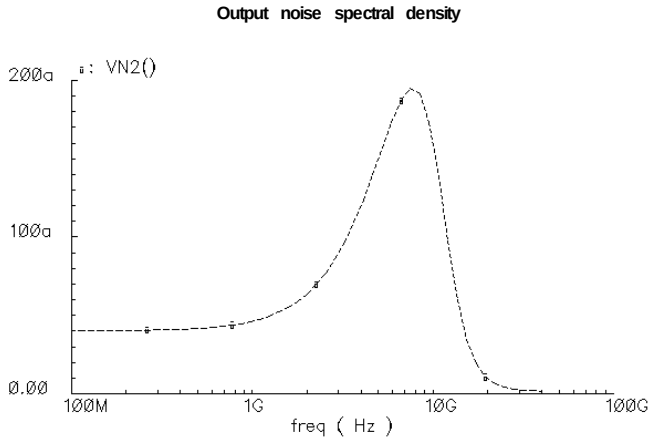

Fig. 4.17. Output Noise of the HBT TIA (Layout).

Fig. 4.17 shows that the output voltage noise power spectra of the HBT TIA layout increases initially. This is expected, as the inductor creates a zero in the transfer function from the channel noise of Q_1 to the output. Fig. 4.18 shows the eye diagram of the HBT TIA output, under simulation conditions similar to that of the HEMT TIA.

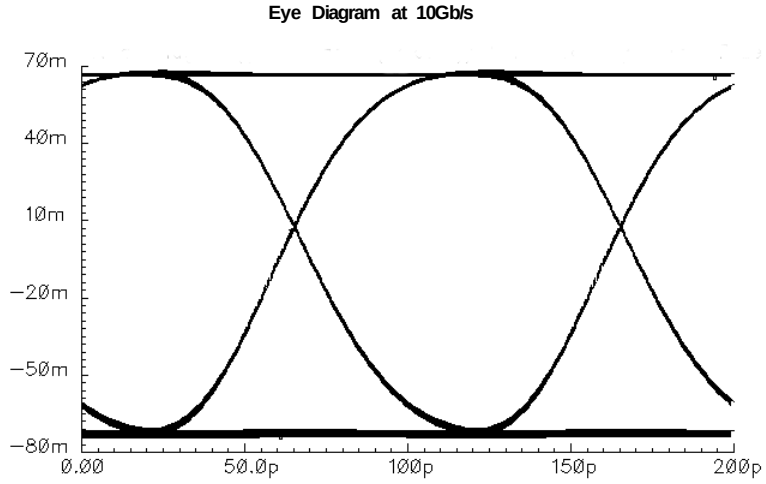

Fig. 4.18. Eye Diagram of the HBT TIA (Layout).

The eye diagram again exhibits almost no eye closure, as expected. The results are tabulated in Table 4.5.

TABLE 4.5

POST-LAYOUT SIMULATION RESULTS FOR THE HBT TIA

Bandwidth	6.85 GHz
Input Referred Current Noise	7 $pA/\sqrt{Hz}$
Transimpedance Gain	1584Ω (Rf=1.6kΩ)
Group Delay Variation Over Bandwidth	1ps
Power Consumption	140mW
Power Supply	6V
Risetime	51.4ps
Chip Area	0.84mm^2

CHAPTER V
CONCLUSION

5.1. Comparison With Results in the Literature

Table 5.1 shows that the bandwidth and noise performance of the TIAs designed are comparable to those in the literature.

TABLE 5.1

COMPARATIVE LISTING OF THE PERFORMANCE OF VARIOUS TIA DESIGNS

Technology	Bandwidth	Gain	Input-Referred Noise (*rms*)	Input Capacitance Cd
[24] 0.3μm Si Bipolar/ f_t = 35GHz (measured)	10.5GHz	1kΩ	12pA/Hz$^{1/2}$	150fF
[25] 0.1μm HEMT/ f_t = 85GHz (measured)	8GHz	600Ω	6.5pA/Hz$^{1/2}$	250fF
[11] Si Bipolar/ f_t = 23GHz (measured)	7.8GHz	710Ω	9pA/Hz$^{1/2}$	100fF
[26] SiGe HBT/ f_t = 47GHz (measured)	9.8GHz	233 Ω	12pA/Hz$^{1/2}$	280fF
This work: 0.5um HEMT f_t = 33GHz (simulated post-layout)	6.3GHz	1.4kΩ	11pA/Hz$^{1/2}$	100fF
This work: AlGaAs HBT f_t = 40GHz (simulated post-layout)	6.85GHz	1.58kΩ	7pA/Hz$^{1/2}$	100fF

The lower bandwidth of this work's designs is attributed to the low f_t of the transistors used, and the need to have the amplifier response be a Bessel type. The simulation results of this thesis are being compared with experimental results. It is expected that the experimental results of this thesis will show some performance degradation.

The designed TIAs have the highest transimpedance gain for 10Gb/s to date. The input referred noise was not commensurately low, due to the low f_t transistors used. The equivalent input referred noise density considers output noise over the bandwidth of the TIA, as is the practice in the literature.

The HBT TIA uses less power than the HEMT TIA as expected, and has a lower input referred noise due to its common-emitter architecture. The HEMT TIA highlights the effectiveness of the common-gate TIA. Using a process with lower f_t, the performance of the HBT TIA was nearly matched.

5.2. Possible Uses of the Designed TIAs

The relatively inexpensive semiconductor process used to design the 10Gb/s TIAs means that these TIAs can be produced in large quantities, for low-end users. It should be noted that while an excellent 10Gb/s TIA can be designed in a 33GHz f_t process, a wide dynamic range AGC operating at 10Gb/s may be impossible to design in the same process. These designs are therefore more suited to optical receivers that will use limiting post-amplifiers.

5.3. Improvements to the TIA Design

The inductors used in the HBT TIA could be replaced with air-bridge inductors to reduce parasitic capacitance. With reduced capacitance, shunt-series peaking and T-coil compensation techniques [21] become effective. This also highlights the need for semiconductor processes with thick interconnects high above the substrate. In optical communications design, the limiting factor in amplifier performance is therefore the quality of the passives, and not the transistors themselves.

REFERENCES

[1] S. Alexander, *Optical Communication Receiver Design*, Washington: SPIE Optical Engineering Press., 1997.

[2] E. Sackinger, *Broadband Circuits for Optical Fiber Communication*, New Jersey: John Wiley and Sons Inc., 2005.

[3] G. Williams, "*Lightwave Receivers*," in *Topics in Lightwave Transmission Systems*, T. Li, Ed., New Jersey: Academic Press, Inc. 1991. pp79-148.

[4] B. Razavi, *Design of Integrated Circuits for Optical Communications*, New York: McGraw Hill Companies Inc., 2003.

[5] S.M Sze, *Semiconductor Devices: Physics and Technology*, 2nd. ed., New York: John Wiley and Sons, 2002.

[6] S. Miura, O. Wada, H. Hamaguchi, M. Ito, M. Makiuchi, K. Nakai, T. Sakurai, "A Monolithically Integrated AlGaAs/GaAs p-i-n/FET Photoreceiver by MOCVD," *Electronic Device Letters, IEEE,* vol. 4, issue 10, pp. 375-376, Oct. 1983.

[7] U. Koren, "Optoelectronic Integrated Circuits," in Optoelectronic Technology and Lightwave Communications Systems, C. Lin, Ed., New York: Van Nostrand Reinhold, 1989.

[8] H. Rohde and W. Dahlke, "Theory of Noisy Fourpoles," *Proc. IRE*, vol. 44, pp. 811–818, June 1956.

[9] F. Centurelli, R. Luzzi, M. Olivieri, A. Trifiletti, "A Bootstrap Technique for Wideband Amplifiers," Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] , vol.49, no.10, pp. 1474-1480, Oct 2002.

[10] M. Vadipour, "Capacitive Feedback Technique for Wide-Band Amplifiers," *IEEE Journal of Solid-State Circuits,* vol.28, no.1, pp.90-92, Jan 1993.

[11] M. Neuhauser, H.-M Rein, H. Wernz, "Low-Noise, High-Gain Si-Bipolar Preamplifiers for 10 Gb/s Optical-Fiber Links - Design and Realization," *IEEE Journal of Solid-State Circuits,* vol.31, no.1, pp.24-29, Jan 1996.

[12] Haitao Tong, Dept. Of Electrical Engineering, Texas A&M University, Private Communication.

[13] K. Ohhata, T. Masuda, E. Ohue, K. Washio, "Design of a 32.7-GHz Bandwidth AGC Amplifier IC with Wide Dynamic Range Implemented in SiGe HBT," *IEEE Journal of Solid-State Circuits,*, vol.34, no.9, pp.1290-1297, Sep 1999.

[14] Feng-Tso Chien; Yi-Jen Chan, "Bandwidth Enhancement of Transimpedance Amplifier by a Capacitive-Peaking Design," *IEEE Journal of Solid-State Circuits*, vol.34, no.8, pp.1167-1170, Aug 1999.

[15] S.M. Park, C. Toumazou, "Gigahertz Low Noise CMOS Transimpedance Amplifier," *Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on*, vol.1, pp.209-212 , 9-12 Jun 1997.

[16] M. Rodwell, J.F. Jensen, W.E. Stanchina, R.A. Metzger, D.B. Rensch, M.W. Pierce, T.V. Kargodorian, Y.K. Allen, "33-GHz Monolithic Cascode AlInAs/GaInAs Heterojunction Bipolar Transistor Feedback Amplifier," *IEEE Journal of Solid-State Circuits,* vol.26, no.10, pp.1378-1382, Oct 1991.

[17] Sung Min Park; Hoi-Jun Yoo, "1.25-Gb/s Regulated Cascode CMOS Transimpedance Amplifier for Gigabit Ethernet Applications," *IEEE Journal of Solid-State Circuits,* vol.39, no.1, pp. 112- 121, Jan. 2004.

[18] S.M. Park, C. Toumazou, "Low Noise Current-Mode CMOS Transimpedance Amplifier for Giga-Bit Optical Communication," *Circuits and Systems, 1998. ISCAS '98,* vol.1, pp.293-296. 31 May-3 Jun 1998.

[19] A. Hastings, *The Art of Analog Layout*, New Jersey: Pearson Education, Inc., 2nd. ed., 2006.

[20] C. Searle, A. Boothroyd, E. Angelo, P. Gray, and D. Pederson, *Elementary Circuit Properties of Transistors*, New York: John Wiley and Sons, 1964.

[21] D. Feucht, *Handbook of Analog Circuit Design*, San Diego: Academic Press Inc., 1990.

[22] C.D. Hull, R.G. Meyer, “Principles of Monolithic Wideband Feedback Amplifier Design,” *Int. J. High-Speed Electron.*, Vol. 3, no. 1, pp. 53-93, 1992.

[23] B. Agarwal, Thesis - *Analog Integrated Circuits with AlInAs/GaInAs Transferred-Substrate HBTs*, University of California, Santa Barbara, March 1998.

[24] K. Ohhata, T. Masuda, K. Imai, R. Takeyari, K. Washio, "A Wide-Dynamic-Range, High-Transimpedance Si Bipolar Preamplifier IC for 10-Gb/s Optical Fiber Links," *IEEE Journal of Solid-State Circuits,* vol.34, no.1, pp.18-24, Jan 1999.

[25] H. Ikeda, T. Ohshima, M. Tsunotani, T. Ichioka, T. Kimura, "An Auto-Gain Control Transimpedance Amplifier With Low Noise and Wide Input Dynamic Range for 10-Gb/s Optical Communication Systems," *IEEE Journal of Solid-State Circuits,* vol.36, no.9, pp.1303-1308, Sep 2001.

[26] D. Guckenberger, K. Kornegay, "Novel Low Voltage, Low-Power, Gb/s Transimpedance Amplifier Architecture," *Prcoc. SPIE*, vol. 5117, pp. 274-285, 2003.

VITA

Name: Oluwafemi Ibukunoluwa Adeyemi

Address: Department of Electrical Engineering, Texas A&M University
TX, 77843-3128

Email Address: oluwafemi@gmail.com

Education: B.S., Electrical Engineering, University of Houston, 2002
M.S., Electrical Engineering, Texas A&M University, 2006