FRACTIONAL-N PLL WITH 90^{o} PHASE SHIFT LOCK AND ACTIVE SWITCHED-CAPACITOR LOOP FILTER

A Dissertation

by

JOOHWAN PARK

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2005

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Franco Maloberti
Committee Members,	Robert D. Nevels
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	Cesar Malave
Head of Department,	Chanan Singh

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ABSTRACT

Fractional-N PLL with 90^{o} Phase Shift Lock and Active Switched-Capacitor Loop Filter.

(August 2005)

Joohwan Park, B.En.; M.En., Hanyang University

Chair of Advisory Committee: Dr. Franco Maloberti

Phase locked loops (PLL) are used in a variety of RF integrated applications because of their ability to generate precise clock signals. These applications include clock recovery systems, frequency synthesizers and frequency multipliers.

In order to achieve small size and low cost targets, the PLLs must be fully integrated on-chip with all the necessary components. Unfortunately, the filtering requirement for the low pass filter (LPF) demands a large silicon area, or the use of external capacitors. Moreover, high-density recording and high data rates for image transfer systems in wireless communication require more fully integrated LSI.

The main goal of this study is to find area efficiency with fully on-chip design, and to provide a solution to improve the phase noise level without occupying a large area or using off-chip components. Moreover, to reduce the phase noise level, it is necessary to desensitize the VCO control when the loop is in the “lock zone”. The introduced phase noise enhancement (PNE) will smartly reduce the phase noise without degrading the settling time by reducing the loop gain in the lock conditions.

To my parents,

To my wife,

To my daughter

ACKNOWLEDGMENTS

My greatest appreciation goes to my advisor, Dr. Franco Maloberti, for his patience and support during my Ph.D. work. He has provided a strong basis for my knowledge in the field of Analog Circuit Design. In particular, he gave me many valuable suggestions for improving my ability to solve problems.

I would also like to express my gratitude to Dr. Robert D Nevels. He is always willing to help me, not only with academic improvement, but also with suggestions for my personal development.

Thanks are also deserved by Dr. Takis Zourntos for serving on my Ph.D. committee.

Finally, I am thankful to Dr. Cesar Malave in the Industrial Engineering Department for the time he has devoted to me.

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CHAPTER I

INTRODUCTION

1.1 Frequency Synthesizer

Phase locked loops (PLL) are used in a variety of RF integrated applications because of their ability to generate precise clock signals. These applications include clock recovery systems, frequency synthesizers and frequency multipliers.

PLLs can be used to generate a local oscillation frequency, for instance in a wireless application where there is a need for a well-designed frequency synthesizer to aid the transmitting and receiving paths to quickly settle onto the new required frequencies [1]. In most cases, the frequency must operate within the required small and precise steps. Current wireless standards require minimum channel spacing of 30 kHz. In addition to accuracy and channel spacing, other specifications of synthesizers must be achieved, such as phase noise, settling time and fractional spurs [2].

In order to achieve small size and low cost targets, the PLLs must be fully integrated on-chip with all the necessary components. Unfortunately, the filtering requirement for the low pass filter (LPF) demands a large silicon area, or the use of external capacitors [3]. Moreover, high-density recording and high data rates for image transfer systems in wireless communication require more fully integrated LSI.

This dissertation follows the style and format of *IEEE Journal of Solid State Circuits*.

Table 1. PLL applications for RF band

	Tx Band	Rx Band	Channel BW
Cellular (DCS)	824-849 MHz	869-894MHz	30 KHz
IS-95	824-849 MHz	869-894 MHz	1.25 MHz
GSM	890-915 MHz	935-960 MHz	200 KHz
DECT	1.88-1.9 GHz	1.88-1.9 GHz	1.728 MHz

Since 1980, PLLs have been used in high frequency applications, such as RF and wireless transceivers and optical fiber receivers, microprocessors and DVD clocks [1], [4], [5]. Some systems require an output waveform whose frequency must be very accurate and which can be varied in very fine steps. Commonly in wireless transceivers, such requirements can be met through frequency multiplication by phase locked loop.

Table 1 lists the current RF application frequencies and bandwidths [6]. As can be seen, CMOS frequency synthesizers achieving several gigahertz output have been reported. However, key issues such as power dissipation, noise and chip size continue to challenge synthesizer designers.

While PLLs can be used in a wide range of RF applications, they still have a critical drawback in fully on-chip designs because of the low pass filter requirement. Moreover, many PLL designs employ a dual path filter [7]-[9] or programmable hardware [10] to get improved phase noise levels. This increases both the circuit complexity and the required chip area.

1.2 Research Goal and Contribution

Mobile communication architectures use PLLs for compliance with the frequency hopping requirements, and provide low phase noise output in the IF receiver and the up conversion transmitter. The targets must be accomplished with all the components fabricated in a single chip. This is not always possible, since the filtering requirements for the low-pass filter often need external capacitors or demand a large silicon area, which in turn, increases the cost.

The main goal of this study is to find area efficiency with fully on-chip design, and to provide a solution to improve the phase noise level without occupying a large area or using off-chip components [11]-[13].

The current work involves the use of a modified fractional-N PLL structure which uses a PFD with 90º phase-shift lock. This feature reduces the rise and fall time influence and enhances the charge pump linearity. Moreover, the 90º phase-shift enables operation in the sampled-data domain. Thus, it is possible to implement the active loop filter using the switched capacitor (SC) technique and to obtain on-chip filtering functions which can be digitally programmable. A switched capacitor LPF enables on-chip implementation, since it requires a total capacitance of just 50pF for a fully differential LPF. This value is at least ten times smaller than that in continuous-time architecture. Moreover, the use of an active sampled-data control, instead of a simple continuous-time filter, provides good flexibility and programmability.

In order to reduce the phase noise level, it is necessary to desensitize the VCO control when the loop is in the “lock zone”. This has been achieved by using digitally

programmable multiple charge pumps [14]. The introduced phase noise enhancement (PNE) will smartly reduce the phase noise without degrading the settling time by reducing the loop gain in the lock conditions. The proposed approach, and its experimental verifications, should provide a new perspective for the design of a fully integrated Fractional-N PLL. The PLL employs a source couple multi-vibrator with 133-MHz free running frequency. However, the approach can be used with other types of VCO and higher operating frequency.

1.3 Dissertation Outline

Chapter II reviews previous work in PLL architectures. It also describes the PLL design procedure and low pass filter requirements.

Chapter III and IV describe the drawbacks of the conventional PLL design. Also the proposed technique is described in detail.

Chapter V examines the macro model simulation to verify the proposed solution. The results are then compared to those from systems using the conventional architecture. Issues related to filter size and noise immunity from noise sources are also discussed.

Chapter VI describes circuit level design. The operation amplifier and the voltage controlled oscillator are specifically discussed in detail. Simulated results of the proposed solution are presented to verify the performance improvement over conventional solutions.

Chapter VII provides the experimental results and a comparison to the results of a system without PNE. Finally, conclusions are presented in Chapter VIII.

CHAPTER II

GENERAL PLL STRUCTURE

This chapter discusses general architectures for generating a precise clock signal. PLLs are called this because they are based on a feedback loop system to correct the excess phase of nominally periodic signals. PLLs are widely used for their high quality and low cost. For instance, they are used for clock recovery from digital data signals and frequency modulations. As PLLs have increased in quantity, their quality has also improved. For example, the sigma-delta modulator in fractional-N architecture makes well defined channel spacing and reduces the occurrence of spurious sidebands. In this architecture, the PLL forces the output of a feedback signal to equal the input clock so that the oscillation frequency is then equal to the fraction of clock period over the divider value.

Figure 1 shows a PLL as a frequency multiplier. The basic feedback loop consists of a phase frequency detector which generates an error signal based on the phase frequency difference between the clock signal and feedback signal. This error is integrated, sent through a low pass filter, and fed to the oscillator as a control signal. The obtained control signal then adjusts the operating frequency of the oscillator. This goes on until the feedback frequency becomes identical to the reference frequency. Once the two frequencies are equal, the phase difference is zero and no change occurs in the system.

The order of the PLL is defined as the highest order of s in the denominator of

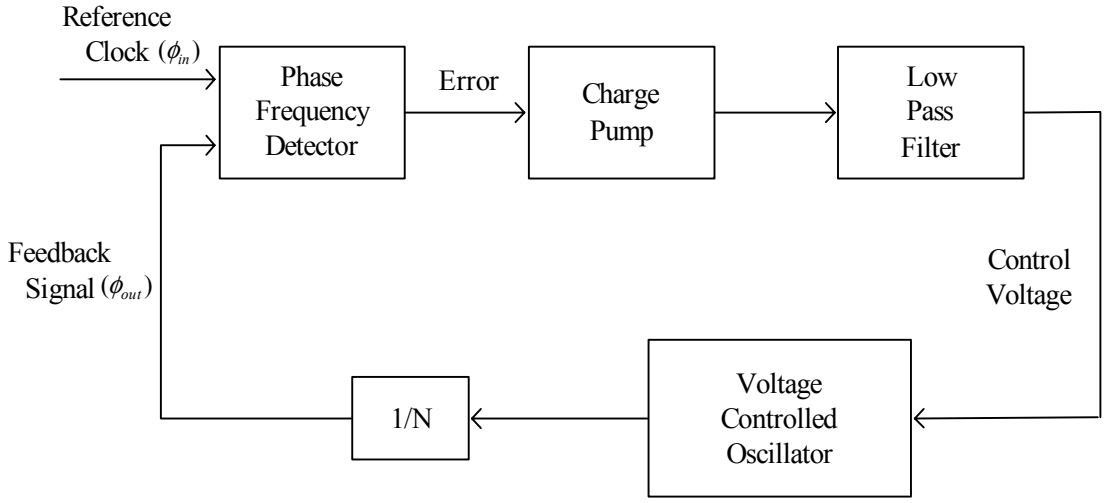

Figure 1. PLL as a frequency multiplier

the loop transfer function [15]. Usually, PLLs are of the 2nd or 3rd order and these would be primary focus of the current study. As could be expected, as the PLL's order is increased, it tends to compensate for an instantaneous change in the higher derivative of the input.

2.1 Second Order PLL

Early PLLs in used have been of the second order. In such a system, the phase-frequency detector (PFD) compares input reference phase (ϕ_{in}) with feedback phase (ϕ_{out}) as shown in Figure 2 (a), and then sends the amount of phase difference to the low pass filter [16].

In a second order system, the low pass filter (LPF) consists of a series connection of a resistor and a capacitor. The LPF blocks high frequency components of the voltage

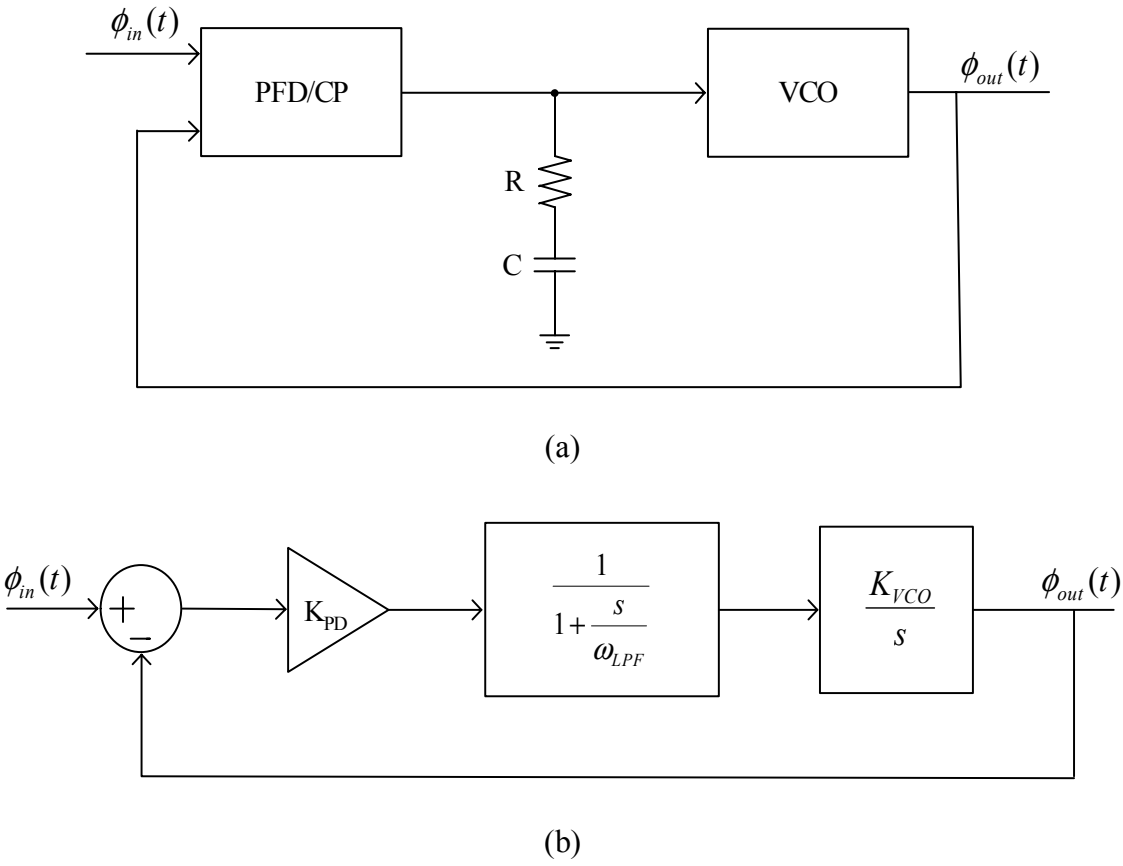

Figure 2. Second order PLL and linear model

across it, without attenuating its dc value. Since the bandwidth of LPF closely relates to the locking time, spurious and noise effect, it should be well considered. Either a passive or an active filter can be used in a PLL block [15]. These send some control voltage for VCO to produce the output frequency which the system needs. To provide zero phase error in the PFD, the loop filter must provide integration. At low frequency, the capacitor's impedance of the low pass filter dominates and thus the LPF behaves as an integrator, as shown in Figure 2 [17].

At high frequency, the capacitor's impedance is negligible and thus the resistor dominates the LPF's total impedance. The PFD output contains dc component, as well as high frequency components, which are suppressed by the LPF. The closed loop transfer function is given as

$$H(s)_{closed} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} \tag{1}$$

The closed loop PLL has $\phi_{in} = \phi_{out}$ when s $\rightarrow$ 0. This means that, if the input excess phase changes slowly, then the output phase fully follows the input variation. The PFD output contains a DC component equal to $K_{PFD}(\phi_{in} - \phi_{out})$ and a high frequency component. Because the high frequency components are suppressed by LPF, it can be assumed that the PFD is a subtractor [16], [18]. Thus, Equation (2) can be rewritten as follows

$$H(s)|_{closed} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2}$$

where

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \tag{3}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}} \tag{4}$$

where ζ is damping ratio and ω_n is the natural frequency. It is possible to choose a natural frequency as low as a one one-hundredth of the reference input clock of the phase frequency detector to guarantee stability.

2.2 Third Order PLL

Third order PLLs provide the desired characteristic of being able to track an accelerating frequency input [17]. In communication systems, this phenomenon occurs

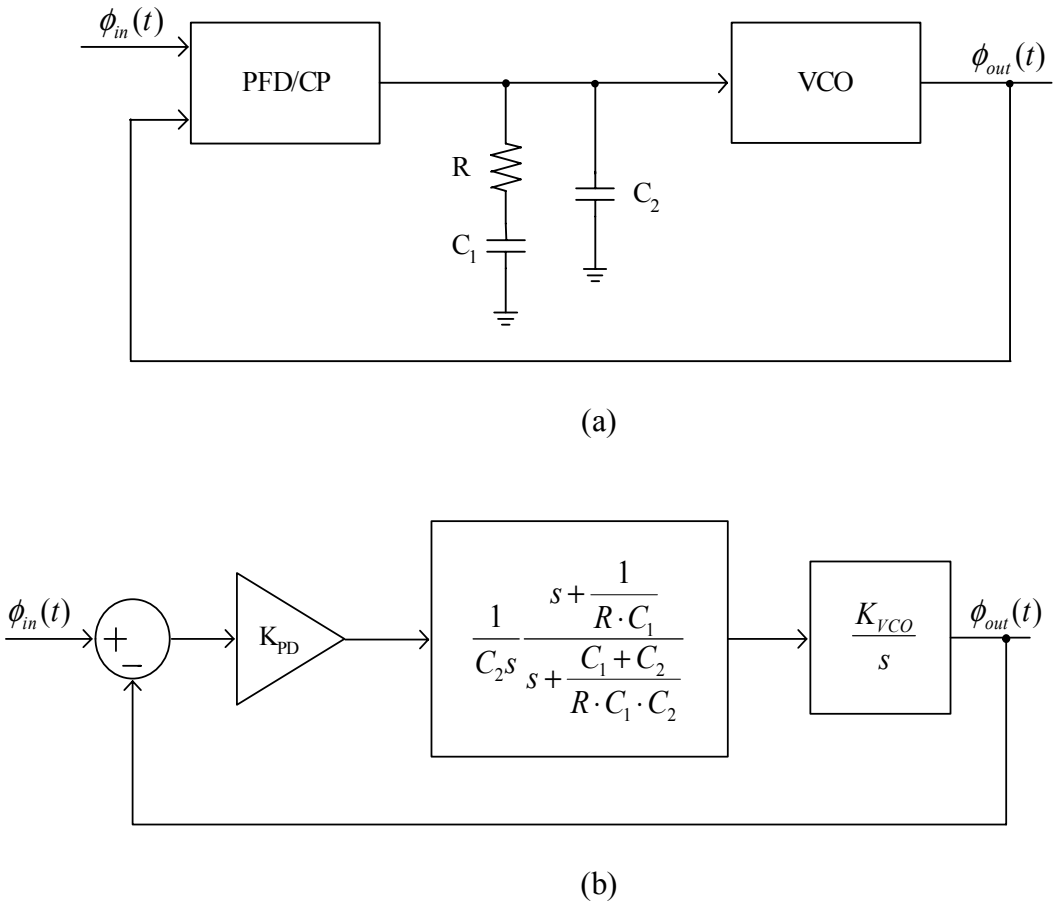

Figure 3. Third order PLL and linear model

frequently when the receiver of a transmitter is in motion. Also, it has the advantage that the filter can be used to optimize the phase noise performance of the loop. The third order loop has additional freedom to optimize the phase noise contributions from different sources. The 2nd order PLL has a serious drawback caused by the PFD and the charge pump as follows: current injections into the resistor-capacitor network result in serious jumps in the control voltage; also, charge pump mismatches and noise effects cause unexpected variation. A third order PLL architecture is shown in Figure 3. To remedy these drawbacks, a second capacitor, C_2, can be added to the low pass filter. This type of architecture is widely used today [17], [18].

2.3 Integer and Fractional-N Synthesizer

An RF synthesizer often requires the output of a PLL to be at a higher frequency than the input reference frequency. As shown in Figure 4, the divider must be inserted

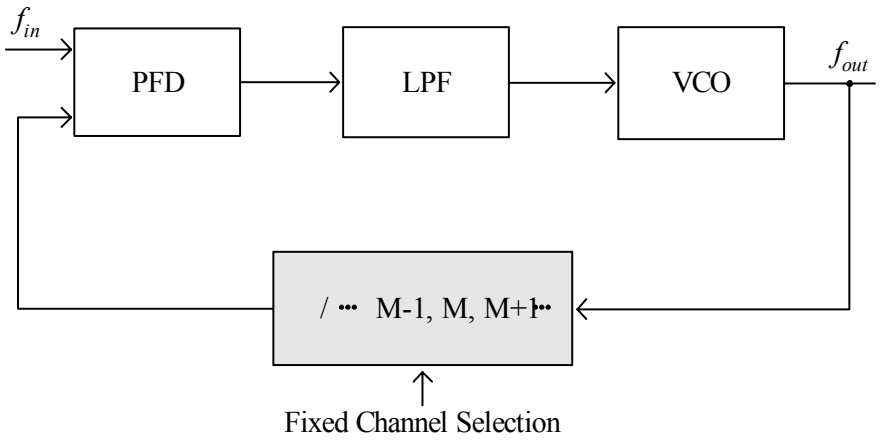

Figure 4. Integer-N synthesizer

in the feedback loop to achieve this. In the locked zone, the two inputs of the PFD become $\omega_{in} = \omega_{fb}$ and hence $\omega_{out} = M \cdot \omega_{in}$.

In the integer-N architecture, the output frequency can be a multiple of the input frequency, $f_{out} = M \cdot f_{in}$. In other words, $f_{out} = f_o + k f_{ch}$, where k is integer variation and f_{ch} is channel step. The k is a channel selection and the base station assigns a certain channel for receiving and transmitting. It is imperative to maintain the input frequency equal to the channel space, $f_{in} = f_{ch}$. Also the loop stability limits the bandwidth of the PLL to roughly lower than $f_{in}/10$ [16]. This results in a slow settling rate, which is undesirable.

All these drawbacks can be corrected using a fractional-N structure where the output can vary by a fraction of the input reference frequency. To illustrate, let us consider a simple case. Say, 100-kHz channel spaces are allowed by using 1-MHz or higher input. Assume f_{REF} = 1-MHz and divider is either 10/11 dual divider. Divider 10 is used for 9 reference cycles and 11 for 1 cycle. Hence, the total output pulses are 101, and the output frequency is 10.1-MHz. If the divider divides by N for A output pulses and by N+1 for B output pulses, then the equivalent divide ratio is equal to (A+B)/[A/N+B/(N+1)]. The value range will be between N and N+1 by choice of modulus control as shown in Figure 5 [18].

The fractional-N synthesizer has many advantages over the integer-N one, such as wider loop bandwidth and faster settling time. However, a fractional-N synthesizer also suffers from fractional spurs. These can be suppressed by randomizing the choice of the divider value. A Sigma delta (ΣΔ) modulator is able to convert fractional spurs to

random noises, as explained in later chapters [19]. Figure 6 shows the synthesizer as a local oscillator in an RF transceiver so as to achieve a precise selection of the output frequency [6].

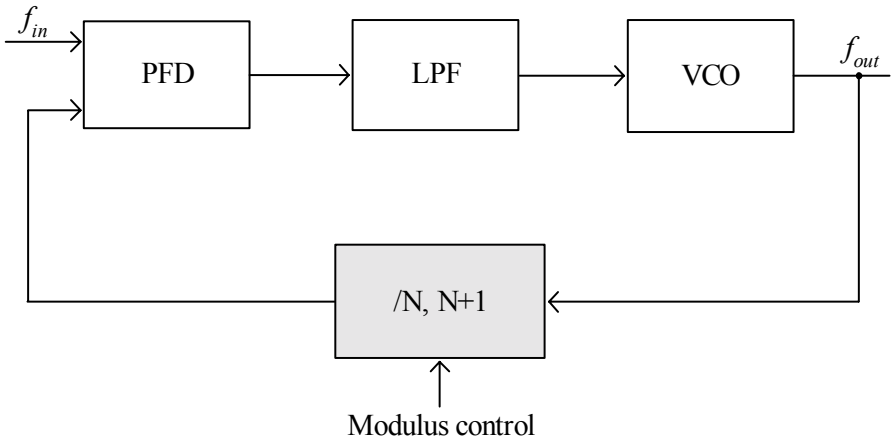

Figure 5. Frequency synthesizer

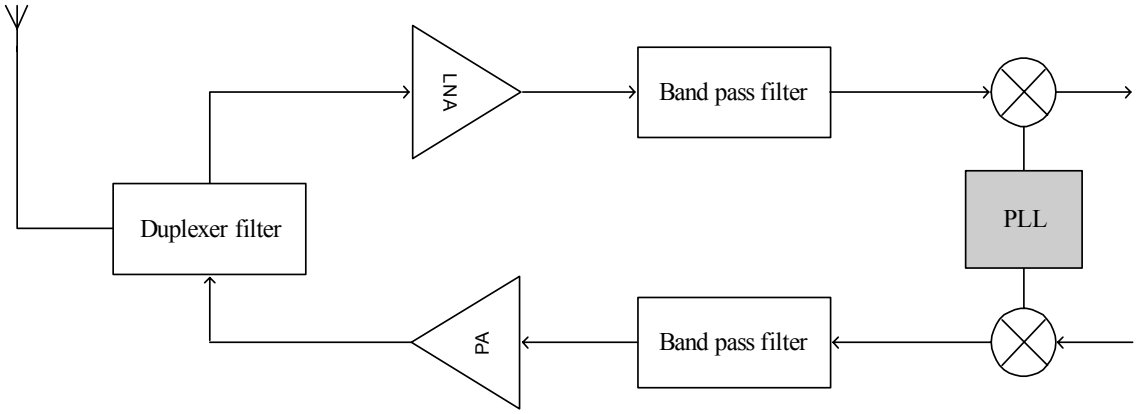

Figure 6. Channel selection as a local oscillator

CHAPTER III

PROPOSED PHASE LOCKED LOOP 1

This chapter discusses the proposed ideas to overcome the deficiencies in conventional PLLs. Current die trends in ICs require small size and high quality. When the PLLs are used in the cell phone for frequency tuning, a fully on-chip design without any external components, will guarantee high performance and low cost. Moreover, noise between each cell phone unit should be well controlled, due to the ever-increasing functionalities provided on the units [20].

This chapter also contains a description of some drawbacks of the conventional continuous time operation method which has some difficulties in accommodating on-chip design and noise improvement.

Also discussed is a new method with a 90^{o} phase shift lock, which permits a fully on-chip design. This concept will introduce the discrete time operation using switched capacitor filters. Subsequent chapters will present the simulation and test results of this proposed method which show an improvement in the overall performance.

In addition, a method that combines a discrete-time filter operation for on-chip design with phase noise enhancement (PNE) technique is described. The key idea is that the digitally controlled variable gain block allows the VCO variation to desensitize when the loop is locked. This improves the phase noise level. Typically, the control block for a PNE is composed of a standard digital cell. This circuitry consists of either an external loop filter, a dual path filter [8], [9], or a programmable charge pump current [19]. The

main drawbacks are the additional hardware requirement and increased circuit complexity. Moreover, problems associated with the uncertainty between acquisition mode and phase lock mode lead to a longer PLL settling time.

The current study presents a relatively low frequency operation to alleviate the problems discussed above. This new idea can also be adapted to a higher frequency by using an LC oscillator or other kinds of high frequency oscillators. The main goal of this study is to find a method of improving phase noise without using a huge silicon area or off-chip components.

3.1 Problems Associated with Conventional PFD

The closed loop feedback forces the output of the oscillator to be equal to the targeted frequency. So, the feedback system compares the output phase to the input phase on every clock cycle. The basic feedback loop consists of a phase comparator that generates an error signal based on the phase difference between the clock signal and the feedback signal. Until a non-zero phase difference exists, the oscillation frequency will be adjusted by the phase locked loop. This error signal is integrated and filtered, and then presented to the oscillator as a control signal [21].

Figure 7 shows the behavioral model of the PFD. A PFD with three states is widely used because of its wide linear range and ability to capture phase and frequency. The circuit consists of two edge-triggered D flip-flops. The PFD response of the two input signals is illustrated in Figure 8. When the loop is locked, the PFD output pulses are short time periods that produce a small change in the phase. Due to the finite rise-

time and fall-time resulting from the parasitic capacitances, the pulse may fail to activate the charge pump switches when the phase difference is minute (Figure 9).

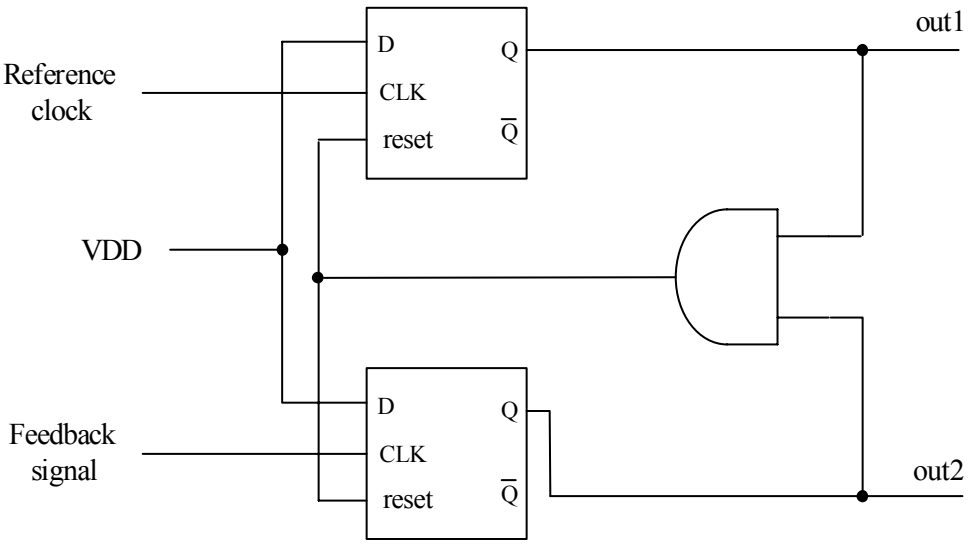

Figure 7. Conventional phase frequency detector

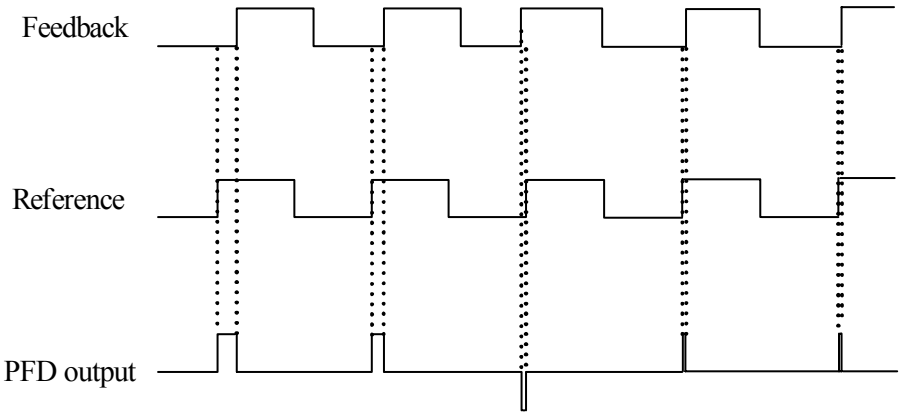

Figure 8. Conventional PFD response

This region is referred to as the “dead zone”. Also, when the frequency detector misses the rising edge, possibly caused by high noise, it causes an incorrect charge injection to LPF. These effects are reflected around the center frequency as phase noise as shown in Figure 10.

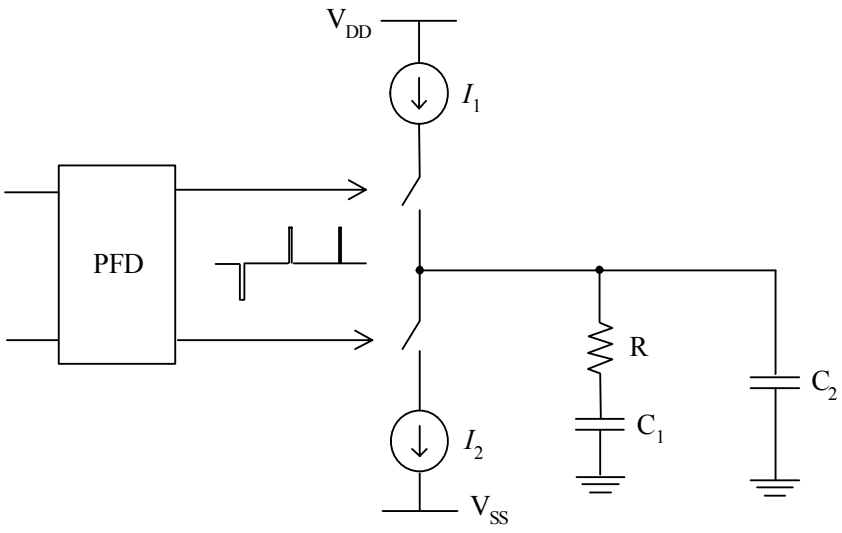

Figure 9. Continuous charge pump PLL structure

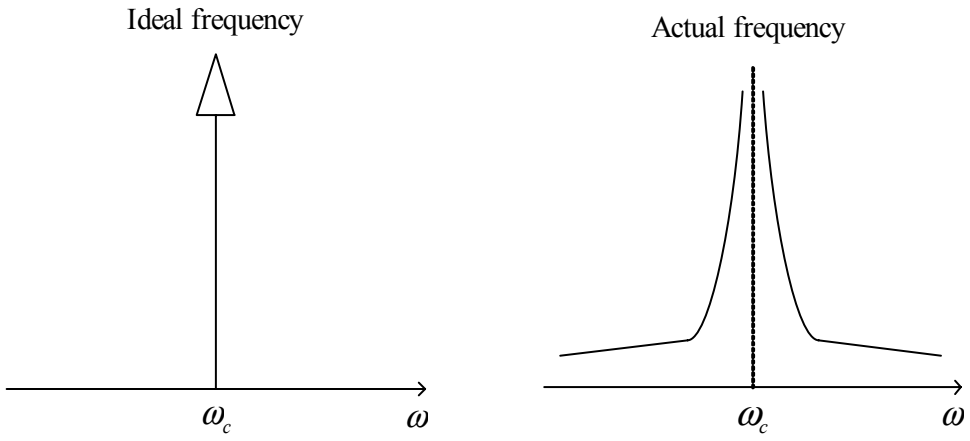

Figure 10. Phase noise around target frequency

3.2 Proposed PFD and Sampling Capacitor

Figure 11 shows a proposed PFD, consisting of two AND gates and two inverters instead of D flip flops which are used in a continuous time synthesizer. The proposed PFD forces the output of feedback signal to be at a 90^{o} phase shift to the input reference clock so that the PFD provides enough time for control over the CMOS switches, as shown in Figure 12. In order to avoid the limits of the phase lock operation in conventional application, the PFD sequentially switches the upper current generator and the lower one equally across the input period. The two inputs of a PFD are used as the reference and the output of the fractional divider. In the lock conditions, the frequencies of the two inputs are equal and a possible phase shift is used to control the VCO. We observe that the reference can be the basis for a clock. We assume a 90º phase shift between the PFD inputs (REF and Output) as shown in Figure 12 [13]. A third switch resets the integrating capacitor at the end of the half-period of the reference.

A 90° phase shift lock produces pulses that are long enough to make the rise on

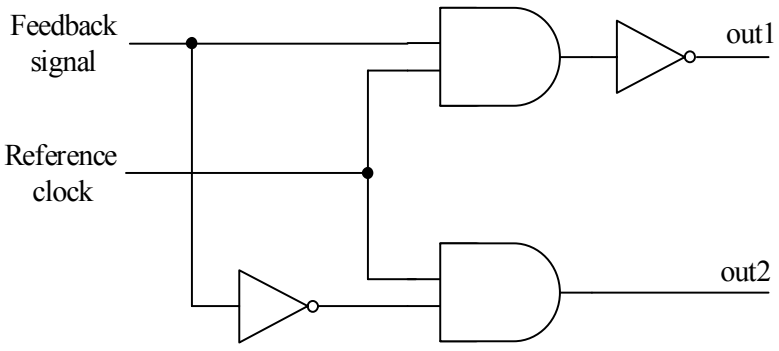

Figure 11. Modified simple PFD

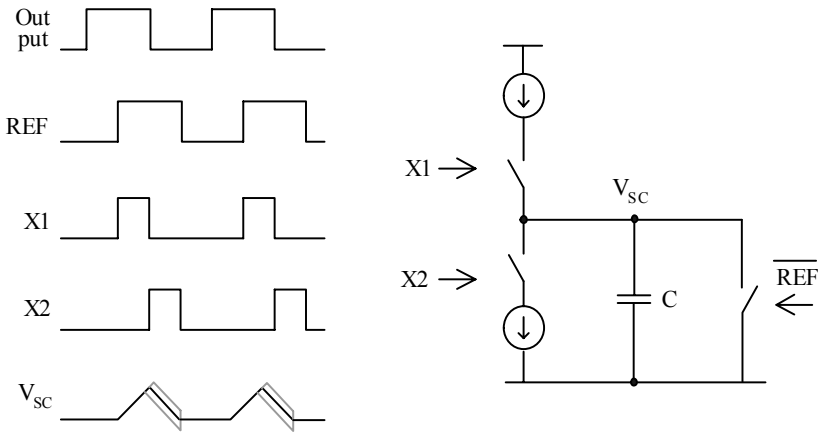

Figure 12. Illustration of the basic concept

J. Park and F. Maloberti, "Fractional-N PLL with 90^o phase shift lock and active switched-capacitor loop filter," in *Proc. CICC,* ©[2005] IEEE.

and off transients negligible. This strategy permits us to avoid the gain loss that occurs in the conventional PFD for phase shifts that are close to zero. The main difference between the conventional charge pump and the proposed one is shown in the waveforms in Figure 8 and Figure 12.

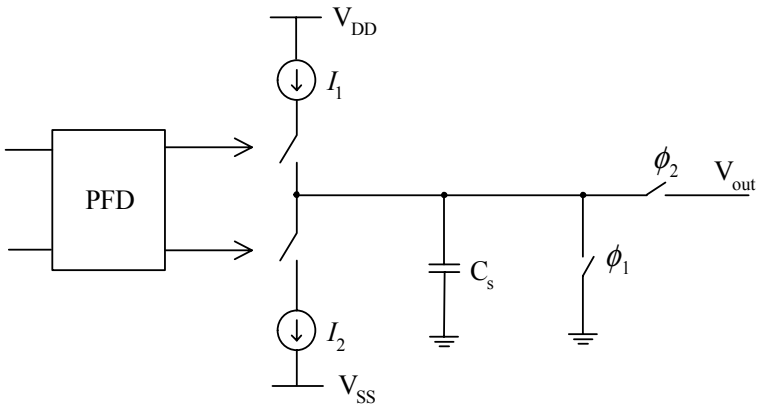

Figure 13. Sampling capacitor

Now, we introduce the sampling capacitor and switching operation as shown in Figure 13. The basic idea of the proposed solution lies in enriching the signal in the sampled-data domain before moving into the continuous-time domain. To achieve this, it is necessary to produce sampled data signals at the output of the charge pump. This sampled data can then be processed by a switched capacitor network. Figure 13 shows the structure that is used to achieve the goal. The current from the generators controlled by the PFD is integrated on capacitor C_s. During phase 2, the charge is transferred to a switched capacitor network followed by the resetting of the sampling capacitor C_s during phase 1.

The sampling capacitor can be made to support a more advanced switching operation as shown in Figure 14. During phase 1, the charge pump switches are activated so that the current I_1 is accumulated and the current I_2 is discharged from the sampling capacitor. During phase 2, the remainder of the charge is transferred to a switched

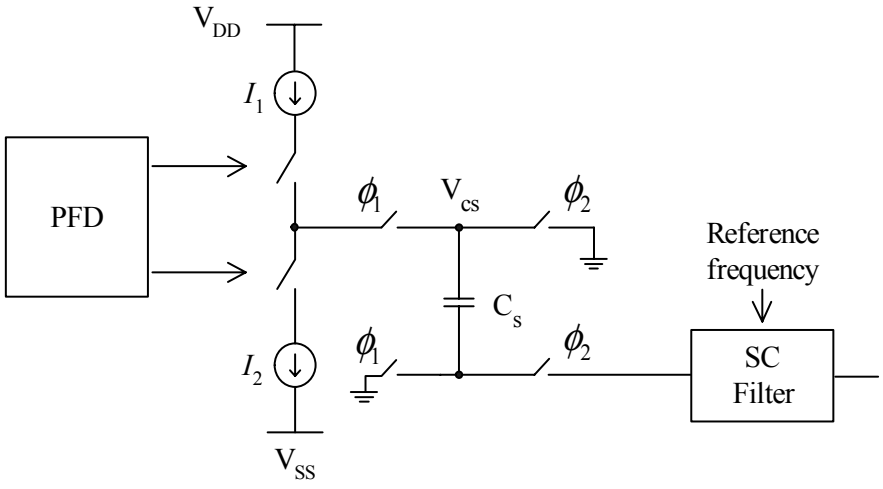

Figure 14. Switched capacitor operation

capacitor (SC) filter block. The switching speed is synchronized with the reference clock. Capacitor C_s can eventually be used as the input element of a switched capacitor filter.

3.3 Switched Capacitor Filter

The reset of the sampled data signal implies the use of a switched capacitor filter, thereby allowing a significant reduction of the total capacitance required for active implementation. The most critical design point is the optimization of the switched capacitor loop filter. The switched capacitor operation converts a continuous time integrator to a sampled data system.

Before we proceed further, it is beneficial to review the sampled data systems. For instance, the role of a resistor is to move a certain amount of charge from node A to node B every second. This function can also be achieved using a capacitor. Say, a capacitor C_s is alternately connected to nodes A and B at a clock rate f_{ck}. The average current equals the average charge moved in a single clock period [16].

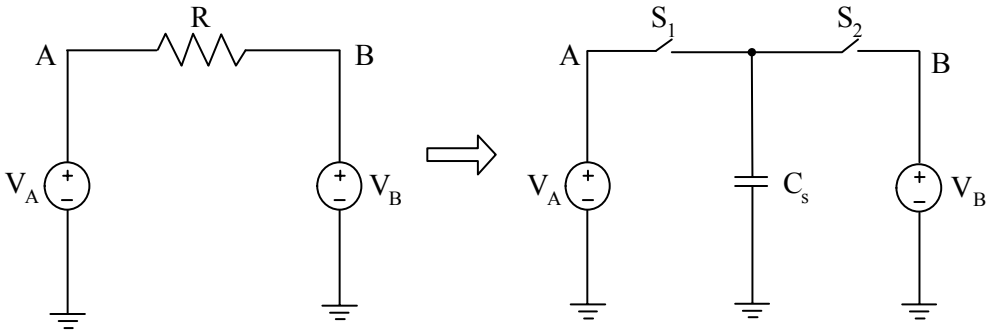

Figure 15. Discrete time resistor

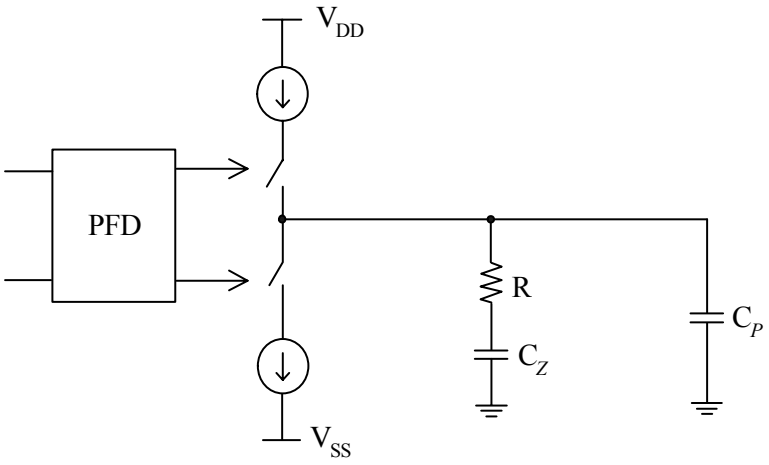

Figure 16. Passive low pass filter

This circuit is shown in Figure 15. Therefore, a resistor can be replaced by its discrete time equivalent with the Equation (5).

$$R = \frac{1}{C_S \cdot f_{ck}} \qquad C_S = \frac{1}{R \cdot f_{ck}} \tag{5}$$

Now, let's consider the pole and zero locations in both the continuous and discrete time solutions. The loop filter design is one of the most challenging, as it determines the phase noise characteristic and settling time. Also, it requires the biggest chip area, due to the use of large capacitances. The widely used type-2, third order

$$\begin{aligned} \omega_Z &\approx \left(R \cdot C_Z\right)^{-1} \\ \omega_P &\approx \left(R \cdot C_P\right)^{-1} \end{aligned} \tag{6}$$

passive filter is shown in Figure 16. Pole and zero are located as shown in Equation (6).

This passive structure is a simple configuration, but has a limited linear region because of finite impedance of the charge pump. An active loop filter is used to alleviate this drawback [22]. In the continuous-time PLL, the PFD operation can be critical when the loop is locked, due to finite pulse durations. To reduce noise from the PFD and input reference jitter, a narrow bandwidth loop filter is needed. However, small resistor values to satisfy the thermal noise constraints will increase the capacitor sizes.

To alleviate these noise constraints at high frequency, another pole is inserted at the output of the active filter. This solution leads to another huge capacitance, which makes integration of all components in a single chip impossible. To alleviate this problem, a new technique using a switched capacitor LPF was devised that keeps the same filter function with a drastically reduced. The sampling capacitor operation makes the PLL usable with discrete time filters. The pole-zero locations are given in Equation (7).

$$\begin{aligned} \omega_Z &\approx \left((C_S \cdot f_{ck})^{-1} \cdot C_Z \right)^{-1} \\ \omega_P &\approx \left((C_S \cdot f_{ck})^{-1} \cdot C_P \right)^{-1} \end{aligned} \tag{7}$$

The frequency response of the whole loop, with third order LPF continuous time PLL, is analyzed in Equation (8), where I_{CH} is the charge pump current and K_{VCO} is gain of voltage controlled oscillator. It can be seen that the loop gain is proportional to the values of current and capacitors.

$$H(s)|_{close} = \frac{\frac{I_{CH}}{2\pi} \cdot \frac{1}{C_2} \cdot \frac{s + \frac{1}{RC_z}}{s \cdot \left(s + \frac{1}{RC_p} \right)} \cdot \frac{K_{VCO}}{s}}{1 + \frac{1}{M} \cdot \frac{I_{CH}}{2\pi} \cdot \frac{1}{C_2} \frac{s + \frac{1}{RC_z}}{s \left(s + \frac{1}{RC_p} \right)} \cdot \frac{K_{VCO}}{s}} \tag{8}$$

$$\frac{\phi_{out}}{\phi_{in}} \propto \frac{I_{CH}}{2\pi \cdot C_p} \tag{9}$$

The bilinear transformation with a discrete time LPF maps the s-plane into z-plane as

$$H(z) = H(s) \mid s = 2f_s \cdot \frac{z-1}{z+1} \tag{10}$$

Because the size of C_2 will be drastically reduced by using a switched capacitor implementation, I_{CH} should be decreased by the same ratio to retain the transfer function. This decreased power will compensate for the increased power consumption in the active filter. Figure 17 shows the fully differential architecture of the proposed charge pump and the low pass filter block. The fully differential operation will have benefits compared to conventional single ended structure, such as noise rejection from power supply and other sources. Also, Table 2 compares the capacitive loads from previous work to the current work.

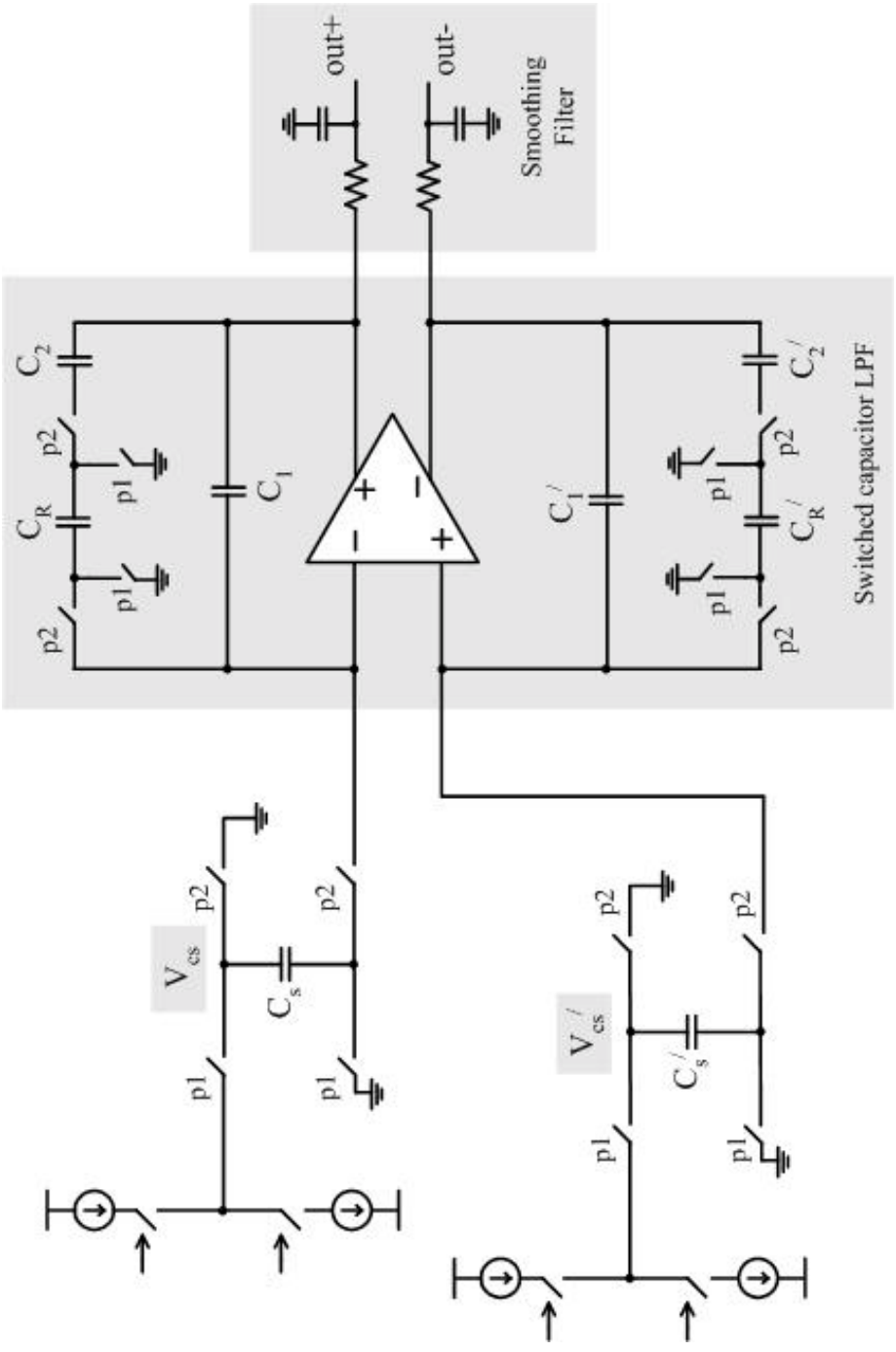

Figure 17. Differential switched capacitor filter

Table 2. Comparison with previous work

	W.Chen 1999 [23]	D. Boerstler 1999 [14]	B. Muer 2002 [19]	Proposed work
Capacitance	700pF	900pF	1.4nF	50pF
Size	$4300\times4300um^2$	$1040\times640um^2$ (off chip)	$2000\times2000um^2$ (off chip)	$1700\times1700um^2$
Type of PLL	Fractional-N	Integer-N	Fractional-N	Fractional-N

CHAPTER IV

PROPOSED PHASE LOCKED LOOP 2

In the previous chapter, we devised a method to reduce the dead-zone and the capacitor sizes by introducing a 90^{o} phase shift lock and employing a switched capacitor active filter.

This section details more about the fractional-N synthesizer operation, and then introduces an effective technique to reduce the signal noise using a smart variable gain block. Discussion on the spurs cancellation technique and the sigma-delta modulator follows.

In the integer-N architecture, the loop bandwidth is limited due to the dependence of the input reference frequency on the channel space. On the other hand, a fractional-N synthesizer can vary by a fraction of the input reference frequency. It, therefore, has a better frequency resolution and wider loop bandwidth than the integer-N synthesizer [16].

Figure 18 depicts the settling response of an integer-N and a fractional-N synthesizer [13]. In both cases, a large transient of the VCO control voltage characterizes the acquisition period. After this period (which must be small in frequency hopping applications), the constant divider factor used in integer-N synthesizer makes the control flat. In contrast, to obtain fractional frequency, the division factor periodically changes between two (or more) integer numbers. Thus, the control voltage fluctuates continuously in the fractional-N synthesizer generating phase noise. This fluctuation is

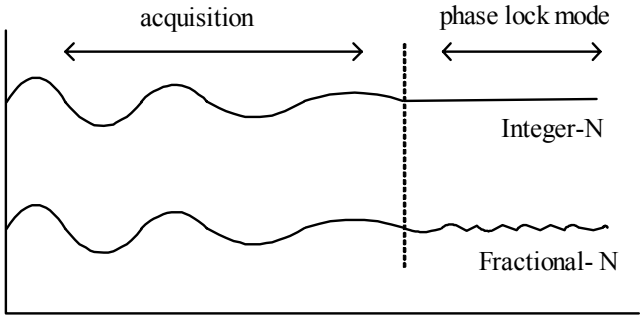

Figure 18. Different settling situation

J. Park and F. Maloberti, "Phase noise improvement in fractional-N synthesizer with 90^o phase shift lock," in *Proc. ISCAS*, ©[2003] IEEE .

necessary to get the fractional frequency, however, it also generates noise around the target frequency.

For example, to get a fractional frequency such as 100.5MHz, the divider uses discrete values of 100% & 101% with 1MHz reference. The idea is to get the average output equal to the desired value, but the individual values occur during a short time period. Depicted in Figure 19, such a synthesizer requires use of a modulus control.

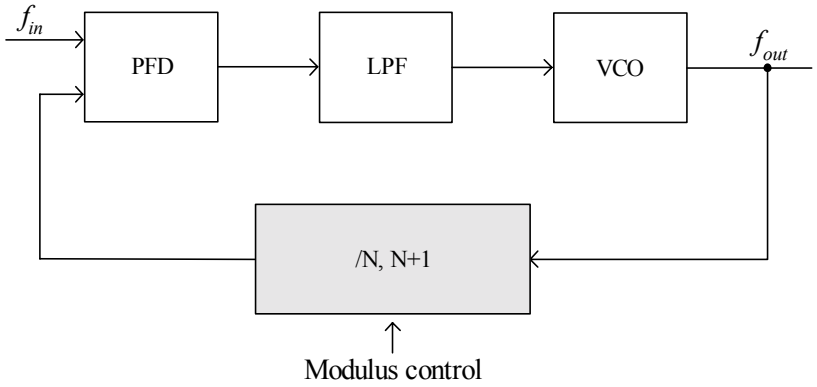

Figure 19. Fractional N synthesizer using dual modulus

In a conventional PLL, the charge pump injects a positive or negative current into the loop filter. The output of the charge pump is a sequence of pulses which has very short durations in the lock mode, as shown in Figure 8. In a 90^o phase shift lock, the output of the charge pump is integrated over a sampling capacitor to generate the input for the loop filter as shown in Figure 12 of the previous chapter.

The information in the conventional case is incorporated in the signs of the current pulses and in the pulse duration. The information in the proposed one is in the sign of the voltage across the storing capacitor and its amplitude.

The capacitor transforms the charge pump current into voltage. Large pulse durations, or large amplitudes, mean a significant change of the VCO. Therefore, those situations are likely to occur in the acquisition. Short pulses or small amplitudes cause fine change of the VCO. Therefore, those circumstances indicate a phase lock state. In order to reduce the phase noise, it is necessary to desensitize the VCO control when the loop filter input is in the lock zone.

4.1 Phase Noise Enhancement (PNE)

This section shows a method to improve the phase noise of a fractional-N synthesizer in the phase lock mode. The technique exploits the features of a 90^o phase shift. The basic idea is to insert a variable gain block between charge pump and LPF. The variable gain stage reduces the phase noise in the lock mode, while it maintains the full functionality in the acquisition mode (i.e. when the PLL is tracking the desired frequency).

The improvement in phase noise is achieved by 90^o phase shift lock and discrete time domain loop characteristics. The use of an active sampled-data control, instead of a simple continuous-time filter, provides good flexibility and programmability. In order to reduce the phase noise, it is necessary to desensitize the VCO control when the loop is in the lock zone. This was what was done in [14] using digitally programmable multiple charge pumps. The action is equivalent to a programmable gain in the signal at the output of the charge pump. This chip includes a gain control section, which also decouples the charge pump section by the loop SC filter.

The circuit schematic is shown in Figure 20 and includes two operational transconductance amplifiers (OTA) [13]. The first is used in an inverting unity-gain buffer. The second is used in an *SC* loop filter which has a programmable gain. A sensing block detects the voltage level at the output of the buffer and changes the gain, for example 6dB. The control is simple but suitable for demonstrating the flexibility of the used approach. The PNE block is placed between the charge pump and low pass filter. The total charge delivered to C_b is given as

$$V_a = \frac{Q_{in}}{C_a} \tag{11}$$

$$Q_b = C_b \cdot V_a = \frac{C_b}{C_a} \cdot Q_{in} \tag{12}$$

where Q_{in} is charge amount at sampling capacitor, C_s.

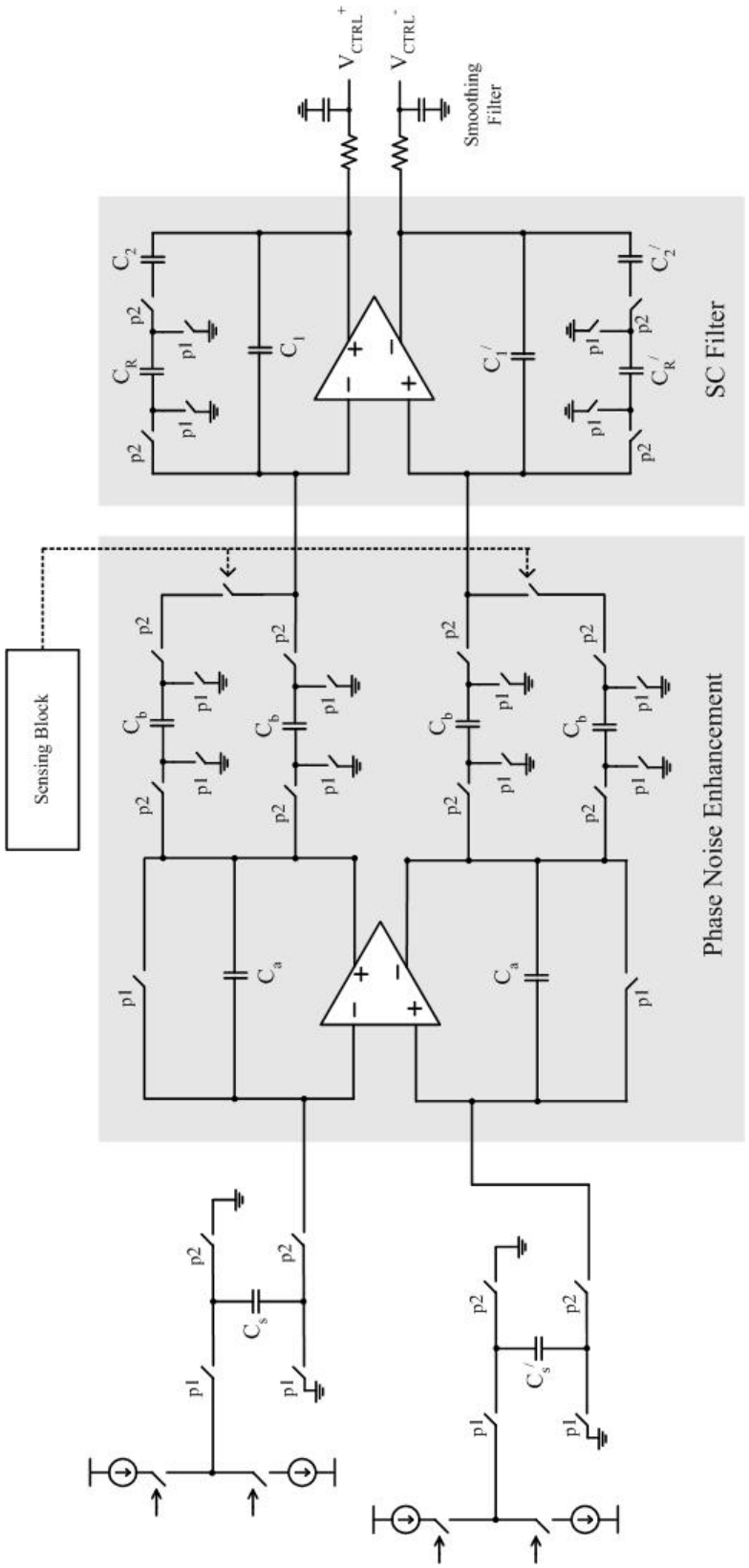

Figure 20. Phase noise enhancement and fully differential LPF

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In the acquisition mode, the switches of the noise enhancement block are closed such that the sum of the two parallel capacitors, $2C_b$ becomes identical with C_a. Below the lock zone threshold, only the charge of one element of C_b is transferred to the SC filter. Thus, the forward gain in the lock mode reduces to half of that in the acquisition mode. The signal at the output of the PNE must be large enough to ensure that the locking is not lost. The closed loop gain is

$$H(s)|_{close} = \frac{\alpha \cdot \frac{I_{CH}}{2\pi} \cdot \frac{1}{C_2} \cdot \frac{s + \frac{1}{RC_z}}{s \cdot \left(s + \frac{1}{RC_p} \right)} \cdot \frac{K_{VCO}}{s}}{1 + \frac{1}{M} \cdot \frac{I_{CH}}{2\pi} \cdot \frac{1}{C_2} \frac{s + \frac{1}{RC_z}}{s \left(s + \frac{1}{RC_p} \right)} \cdot \frac{K_{VCO}}{s}} \tag{13}$$

The bilinear transformation with a discrete time LPF maps the s-plane into z-plane as

$$H(z) = H(s) \mid s = 2f_s \cdot \frac{z-1}{z+1} \tag{14}$$

Figure 21 shows the plot of the forward signal as a function of the sensing voltage [13]. The response is non-linear, with a jump at the transition points. The region with low gain denotes operation in the locked mode. The threshold is ±5mV and is big enough to account for the fluctuations due to noise and spurs contributions. A signal above |5mV| indicates the transient mode, where the gain jumps by 6 dB.

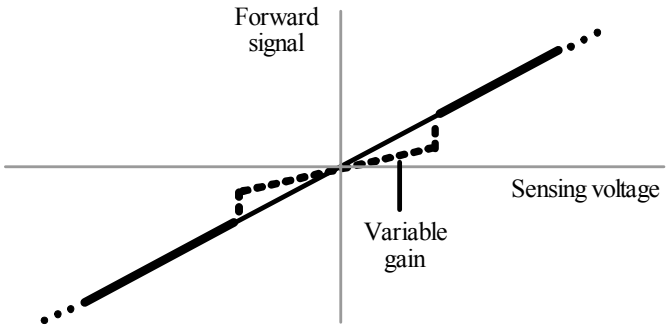


Figure 21. Variable gain

J. Park and F. Maloberti, "Fractional-N PLL with 90^{o} phase shift lock and active switched-capacitor loop filter," in *Proc. CICC,* ©[2005] IEEE.

4.2 Digital Sigma Delta Modulation

Even though the fractional-N synthesizer has many benefits, it has one serious drawback - fractional spurs. If the output of the VCO is to be equal to (N+α) f_{REF}, then the LPF output will be a repetitive wave form. Such a repetitive form would modulate the VCO, which creates sidebands with respect to the center frequency.

Fractional-N spurs can be suppressed by randomizing the choice of the divider value, as shown in Figure 22. Sigma delta modulation is able to convert fractional spurs to random noises [24]-[26]. The idea is that an average divider ratio is equal to desired value, but the individual divider values occur over a short time period. So the random and short period divider ratios reduce fractional spurs around center frequency as shown in Figure 23. Figure 24 shows the second order sigma delta modulator. The generated binary stream represents a well defined average value accompanied by quantization

noise. Suppose the average modulus is equal to $N+\alpha$, and the value is between N and N+1, the instantaneous division ratio can be written as $N+b(t)$, where $b(t)$ is a binary modulus control generated by the sigma-delta modulator. Thus, the feedback frequency is $f_{fb}(t) = f_{out}/[N+b(t)]$ [16].

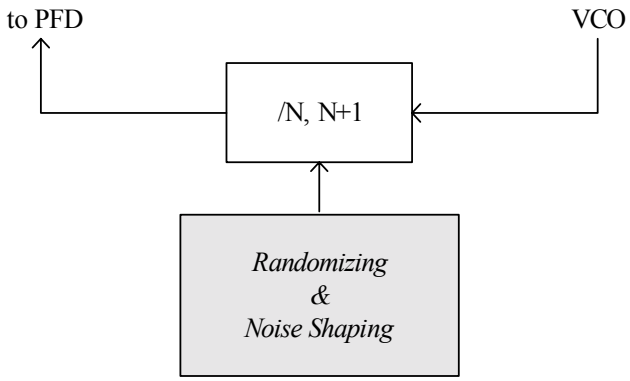


Figure 22 Noise shaping by using sigma-delta modulation

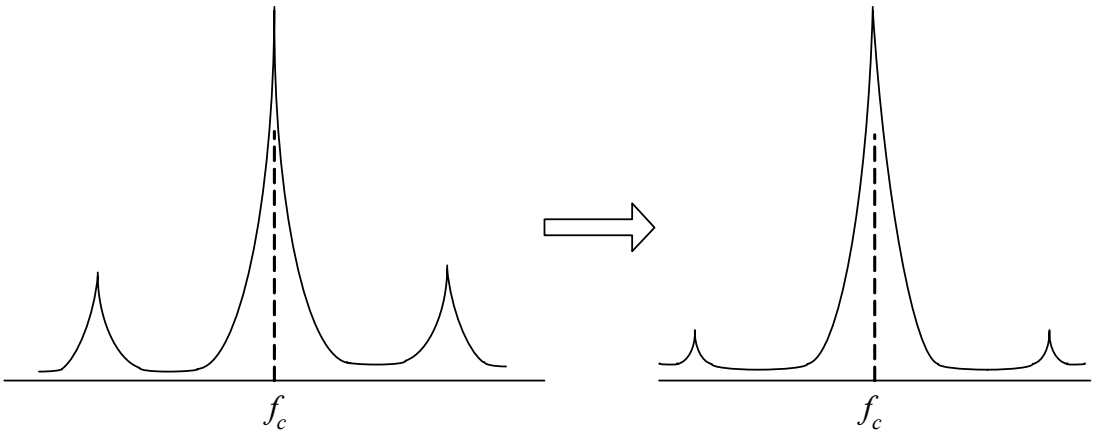


Figure 23. Reduced fractional spurs

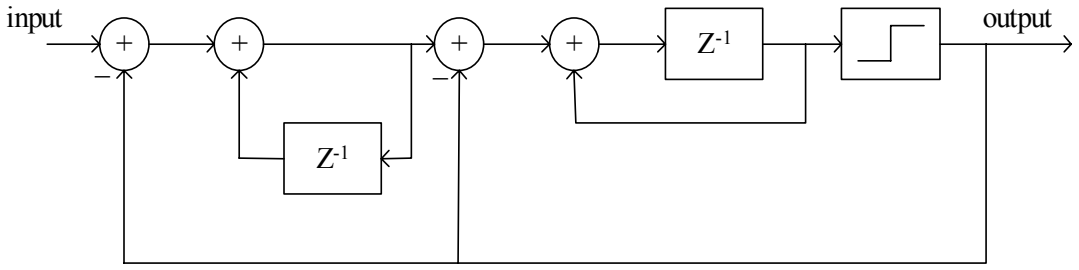


Figure 24. Second order sigma-delta modulation

As we know, the bit stream can be decomposed into an average value α and sigma delta quantization noise q(t). Therefore, the feedback frequency can be expressed as $f_{fb}(t)=fout/[N+\alpha+q(t)]$. The quantization noise is shown as

$$n(t) = f_{fb}(t) - \frac{f_{out}}{N+\alpha} = -\frac{f_{out}}{N+\alpha}\cdot\frac{q(t)}{N+\alpha+q(t)} \tag{15}$$

The power spectrum density of the noise can be simplified as

$$S_n(f) = \frac{f_{out}^2}{(N+\alpha)^2}\frac{Q^2(f)}{N^2} \tag{16}$$

The Equation (16) denotes noise shaping at higher frequencies [18]. A general first or second order sigma-delta modulator still has residual spurs which makes the technique more complicated, similar to that in multi bit high order architecture.

Let us illustrate the time domain behavior using circuit level simulation. The output y[n] takes on values of 1.5 and -1.5, 1 bit signal to control digital divider. For a

DC input x[n] = 1.5 (high level), all the modulator output values will be 1.5. For a DC input of -1.5 (low level), all the values will be -1.5. For a zero DC input, half of the modulator output values would be at 1.5 and the other half at -1.5 [27]. By averaging the modulator output over a period of time, we can approximate the input. In other words, over a period of time, the proportion of high and low values will be related to the DC input value. For larger inputs, the output consists of more high levels than low levels, and for smaller inputs, the output consists of more low levels than high levels. For the digital sigma delta modulator input, offset binary numbers are used as shown in Table 3. Figure 25 is the macro model schematic of the digital Σ-Δ modulation, which is implemented with a combination of adders and flip-flops.

Table 3. Offset binary numbers

Number	4-bit	3-bit
+5	1101	
+4	1100	
+3	1011	111
+2	1010	110
+1	1001	101
0	1000	100
-1	0111	011
-2	0110	010
-3	0101	001
-4	0100	000
-5	0011	
-6	0010	

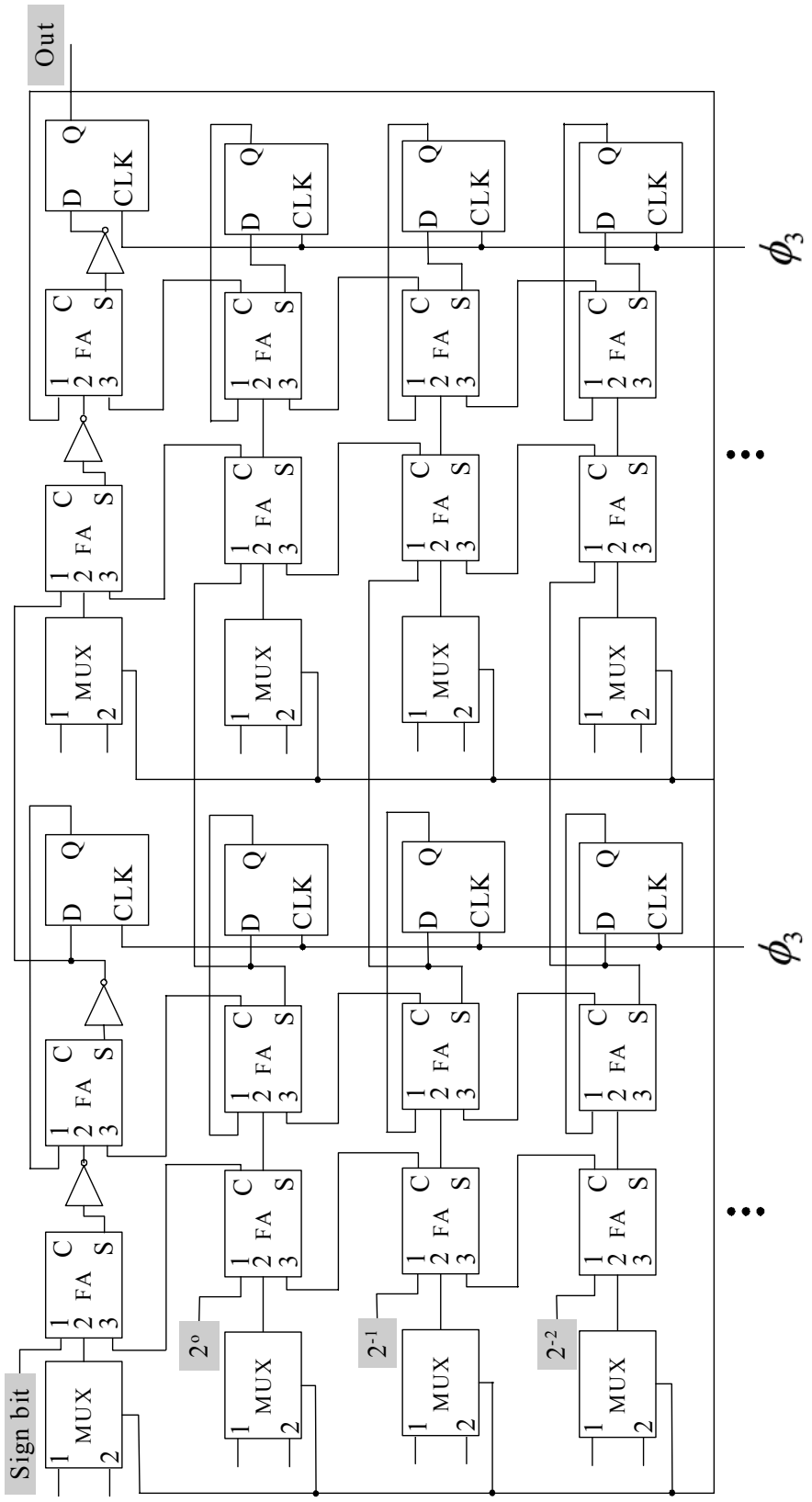


Figure 25. Circuit level digital sigma delta modulator

CHAPTER V

MACRO MODEL SIMULATION

5.1 Macro Model Implementation

In this chapter, we will first discuss how to implement behavioral simulation with Matlab Simulink before moving onto circuit level simulation. The behavioral simulation is convenient as it models the electrical circuitry using mathematical equations and can be used to predict essential system characteristics. We can also model non-idealities or random sources like noise. The phase locked loop model with Matlab Simulink is shown in Figure 26. Phase frequency detector, divider and sigma-delta modulator can be designed with digital blocks, and the low pass filter can be replaced by the transfer function shown in Figure 27.

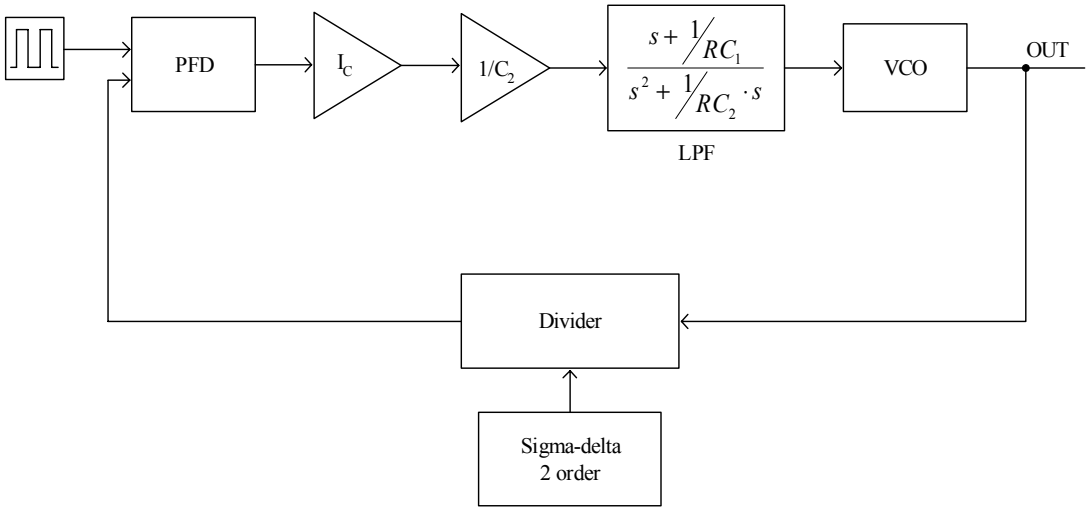


Figure 26. Macro model in Matlab Simulink

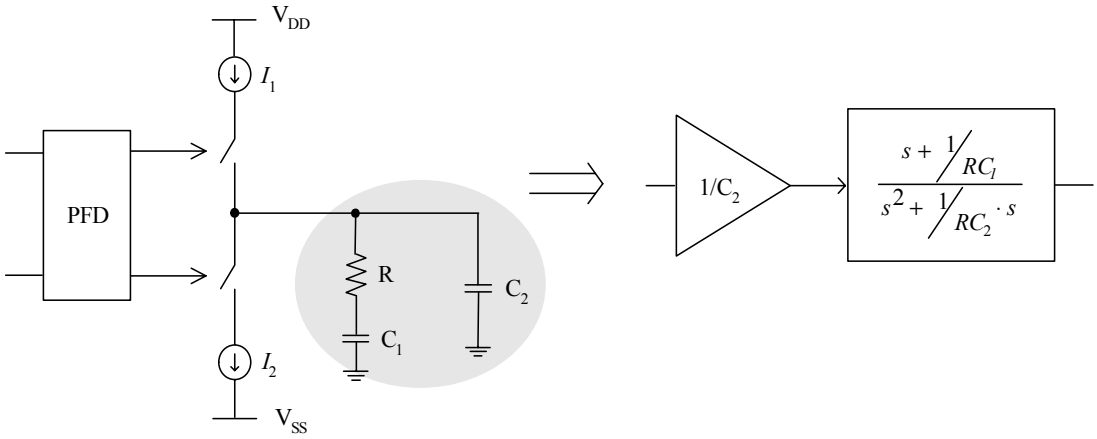


Figure 27 LPF transfer function

The LPF converts a current signal to a voltage signal for controlling the VCO output frequency. The characteristics of the loop depend directly on the pole and zero positions of the LPF. The output from the VCO can be expressed as a sinusoidal function which includes free running frequency and phase difference, as shown in Equation (17). The behavioral model is shown in Figure 28.

$$y(t) = A\cos(\omega_{FR}t + K_{VCO}\int V_{cont}\,dt) \tag{17}$$

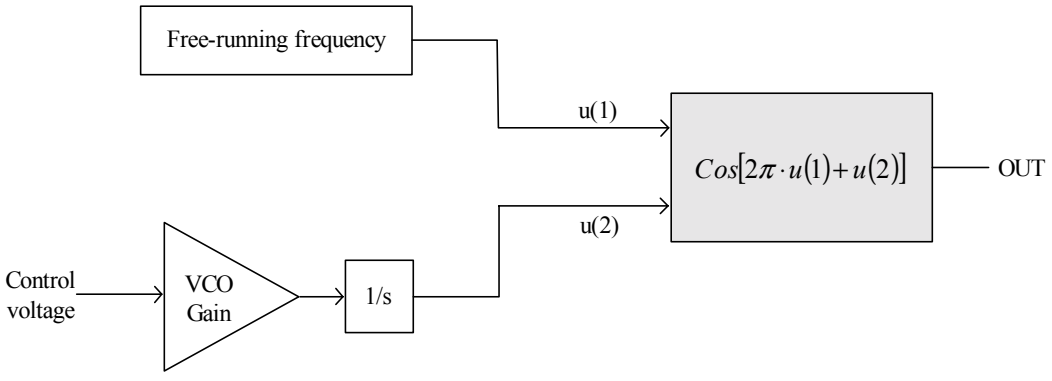


Figure 28. Macro modeling of VCO

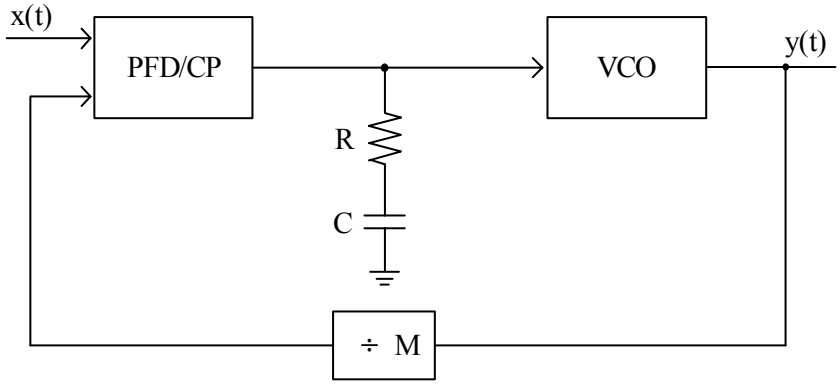


Figure 29. Second order PLL

5.2 Basic Linear Model

Let us now construct a linear model of the PLL as a frequency multiplier assuming a second order type PLL, as shown in Figure 29. The simple structure is good enough to give us an indication of the design rule, without a complex equation. The PLL open-loop transfer function and closed loop transfer functions are as follows:

$$H(s)\,|_{open} = \frac{I}{2\pi}\left(R + \frac{1}{sC}\right)\frac{K_{VCO}}{s} \tag{18}$$

$$H(s) = \frac{\frac{I}{2\pi}\left(R + \frac{1}{sC}\right)\frac{K_{VCO}}{s}}{1 + \frac{1}{M}\frac{I}{2\pi}\left(R + \frac{1}{Cs}\right)\frac{K_{VCO}}{s}} = \frac{\frac{I \cdot K_{VCO}}{2\pi \cdot C}(sRC + 1)}{s^2 + \frac{I}{2\pi}\frac{K_{VCO}}{M}R \cdot s + \frac{I}{2\pi \cdot C}\frac{K_{VCO}}{M}} \tag{19}$$

$$\omega_n = \sqrt{\frac{I}{2\pi \cdot C}\frac{K_{VCO}}{M}} \tag{20}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{I \cdot C}{2\pi}\frac{K_{VCO}}{M}} \tag{21}$$

As we can see in Equation (21), the damping ratio is dependent on R, C, I, K_{VCO} and the divider values. There exists a critical trade off between the settling speed and phase noise characteristic.

The LPF is the main block for specifying the characteristics of the PLL circuit. The loop bandwidth has an inverse dependence on both the high frequency noise produced by the PFD and the settling time.

On the other hand, maximizing the bandwidth of the PLL helps to minimize the noise component which alters VCO frequency. If the input clock generator is noise free, or even just less noisy than the VCO itself, there will be a great improvement. However, if the input clock is noisy, then the high bandwidth loop will consistently be damaged by this noise [28].

5.3 Sampled Domain Solution

The modified PFD and z-domain LPF are the main design issues for discrete time simulation. The behavioral model of the 90^o phase shift lock PLL is illustrated in Figure 30. The bilinear transformation maps the s-plane into the z-plane as

$$H(z) = H(s) \mid \quad s = 2f_s \frac{z-1}{z+1} \tag{22}$$

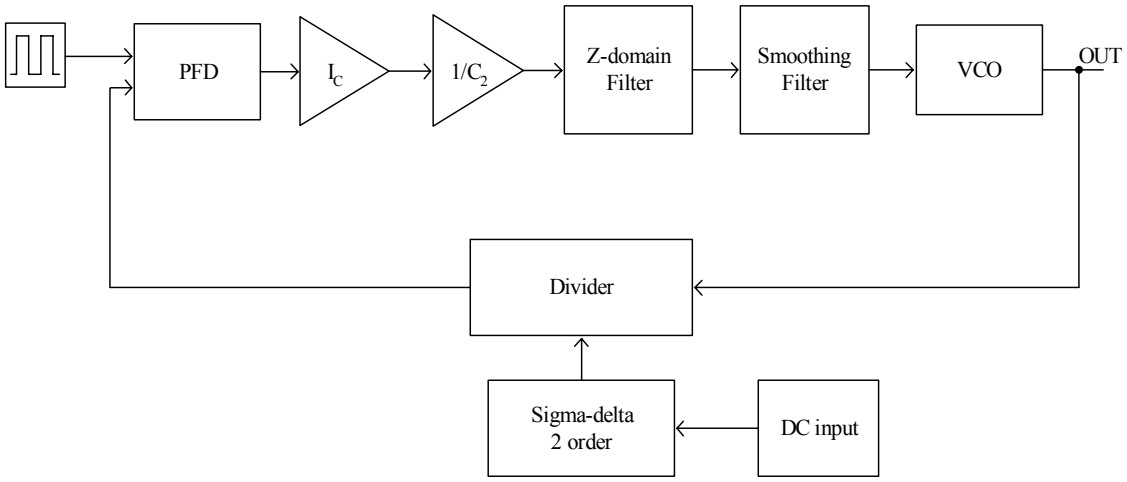


Figure 30. Z-domain macro model in Matlab Simulink

A smooth filter is followed by the sampling domain filter to minimize spurious noise at the VCO input and its -3dB frequency is 1/17 to keep it from affecting the low pass filter response, while providing adequate noise filtering.

The switched capacitor gives rise to a total rms noise factor of $\sqrt{kT/C}$. Because the transistors are used as switches, the on-resistor introduces thermal noise (Figure 31).

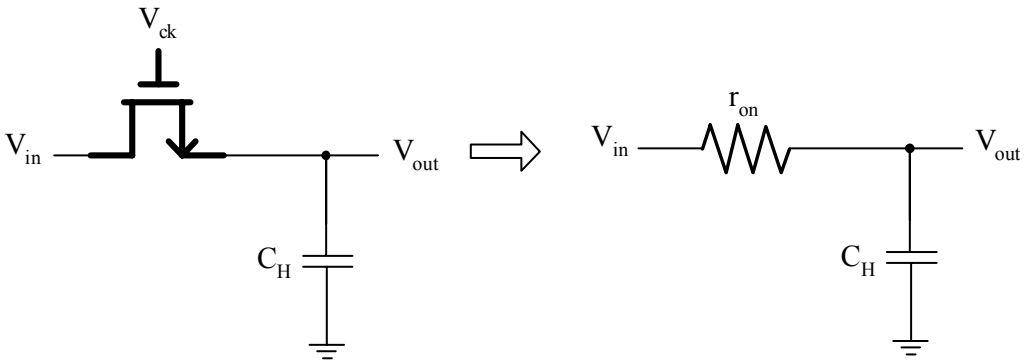


Figure 31. kT/C noise

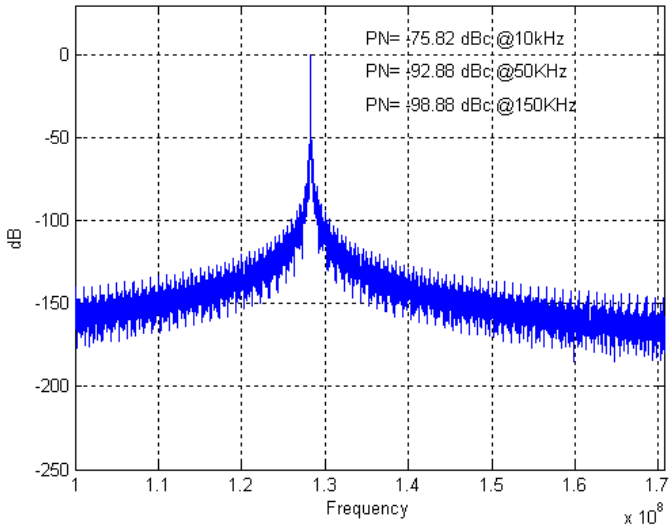
The noise is stored on the capacitor when the switch is off, and can be decreased by increasing the capacitor size [16]. The speed depends on the on-resistance and sampling capacitor size. The on-resistance, R, and sampling capacitor, C, should track input with a negligible phase shift. The on- resistance is expressed as

$$R_{on} = \frac{1}{\mu_n c_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{23}$$

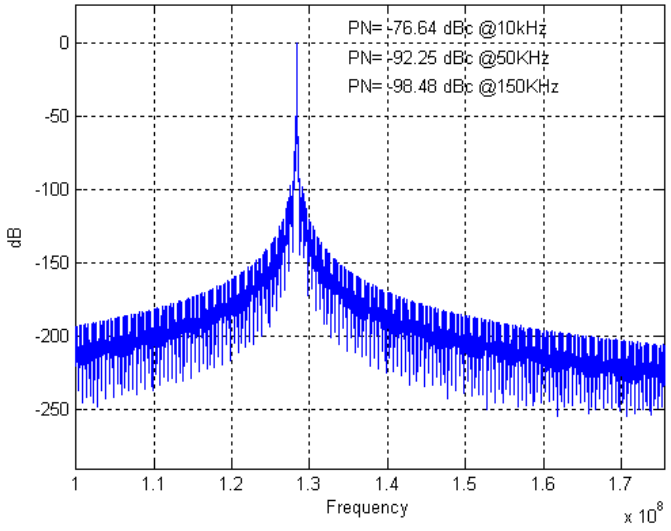
5.4 Macro Model Simulation

Here we discuss the simulation results of the macro model on the conventional architecture and the switched-capacitor-based architecture. The most critical design point concerns the optimization of the switched capacitor loop filter. The switched capacitor filter has been designed using the bilinear transformation of the continuous-time counterpart. By proper scaling of capacitor values, the power spectral density of both the continuous architecture and the proposed one become identical, as shown in Figure 32.

The two solutions have 75dBc at 10kHz, 92 dBc at 50kHz, and 98 dBc at 150 kHz, respectively. However, the two solutions have very different noise floors (a difference of about 50 dB) because the sampling capacitor in the proposed solution removes the high frequency noise in advance of LPF. The optimized capacitor values, when the phase noise is identical, are given in Table 4.



(a) Conventional architecture



(b) Proposed architecture

Figure 32. Power spectral density

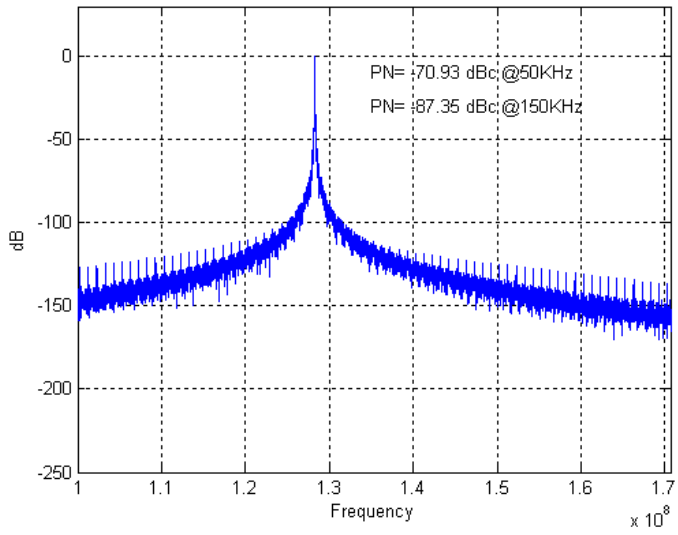
Table 4. Comparison of two different solutions

	Continuous	Proposed
R_C	100KΩ	1pF
C_1	300pF	15pF
C_2	30pF	1.5pF

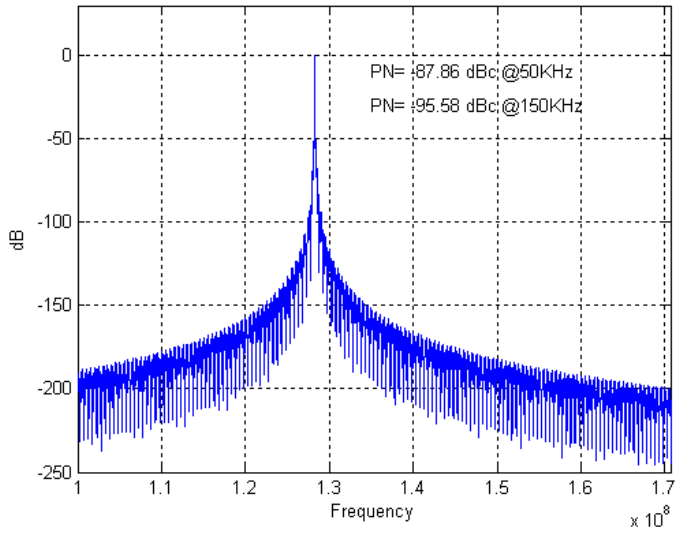
As we can see, the proposed method has around 20 times less capacitance size and thus a 100 kΩ can be replaced with only 1pF. Moreover, the wider bandwidth helps to alleviate the VCO noise and provides faster settling time.

The output frequency is around 128.3 MHz with the fractional modulator. A reference frequency of 1 MHz is used and a 128 and 129 dual divider is used for the divider.

When the two solutions have identical phase noise, as in Figure 32, one interesting point is how the solution reacts with input reference jitter. Figure 33 shows the output spectrum with random reference jitter of 0.5% of the pure signal.



(a) Conventional



(b) Proposed architecture

Figure 33. PSD with input reference jitter

Table 5. Phase noise level with different bandwidths

Bandwidth	@ 50 kHz	@ 150 kHz
80 kHz	-84.11 dBc	-98.63 dBc
40 kHz	-88.70 dBc	-104.14 dBc
20 kHz	-93.92 dBc	-110.35 dBc

Table 5 illustrates the phase noise values according to the different loop bandwidth when the VCO is less noisy than other parts. As expected, the narrow bandwidth has a slow settling time, but it has better noise performance.

Figure 34 shows the PSD of the 90^{o} phase shift lock with phase noise enhancement block. The spectrum shows improved phase noise around the center frequency, because it desensitizes VCO when loop is locked.

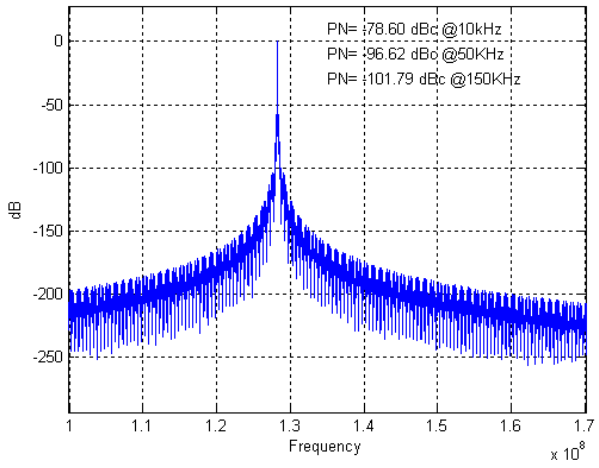


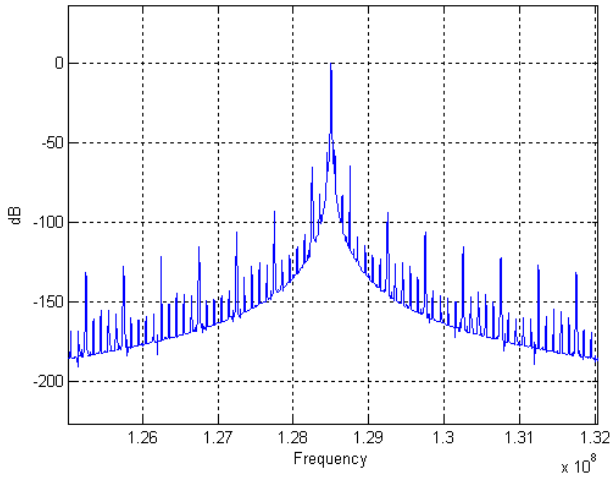
Figure 34. PSD with error correction block

Table 6 shows the phase noise improvements for the two cases. Clearly, the benefits depend on the specific gain of the lock zone used. However, the results provide an indication of the effectiveness of the 90^{o} phase shift lock and the PNE block.

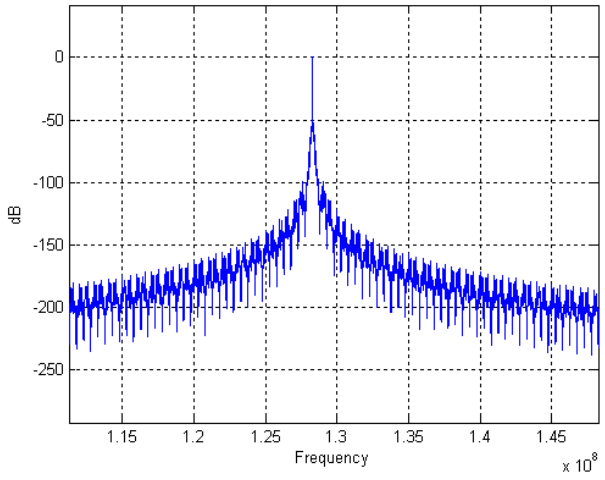
Table 6. Phase noise improvement by using PNE block

	@ 10 kHz	@ 50 kHz	@150 kHz
Without PNE	76.64 dB	92.25 dB	98.48 dB
With PNE	78.60 dB	96.62 dB	101.79 dB

Figure 35 consists of micro model simulations without sigma delta modulation (a) and with sigma delta modulation (b). In the scheme shown in Figure 35(a), strong fractional spurs are found around -70 dB. However, the fractional spur is suppressed to the normal noise level, as shown in Figure 35(b).



(a) Fractional spurs without sigma delta modulator



(b) PSD with sigma delta modulator

Figure 35. Behavioral simulation of spurs in fractional-N architecture

CHAPTER VI

CIRCUIT LEVEL DESIGN

This chapter discusses the circuit level design and simulation result by using 0.25-um CMOS technology. Of all the analog circuits, primarily the OpAmp design for the active filter and VCO design will be discussed. The schematic simulation results illustrate the output performance difference found when using error correction enhancement block and without it.

6.1 Operational Amplifier

The OpAmp is one of the key building blocks of the active filter and directly

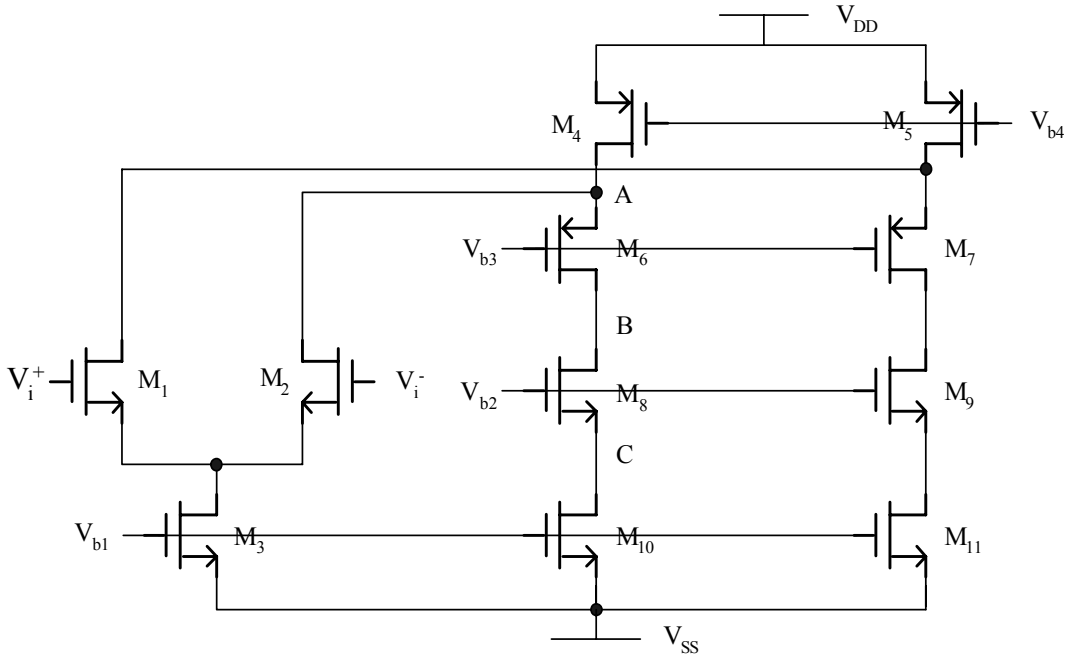


Figure 36. Folded cascade amplifier

affects the performance of the integrator. Fast clocks require extremely fast OpAmp with sufficient phase margin. A fully differential OpAmp, such as a folded cascade amplifier, is used due to the wide common mode input voltage. Figure 36 is the schematic of the fully differential OpAmp.

(a) Small Signal Analysis

In this section, we look at the frequency response of the circuit design. Although the precise calculation of frequency responses is most often left to computer simulations, there is much insight that can be obtained by finding the dominant frequency effects in the circuit. The s-domain transfer function of the amplifier is derived from the small signal analysis. The location of the dominant pole, 2nd pole and the zero is estimated

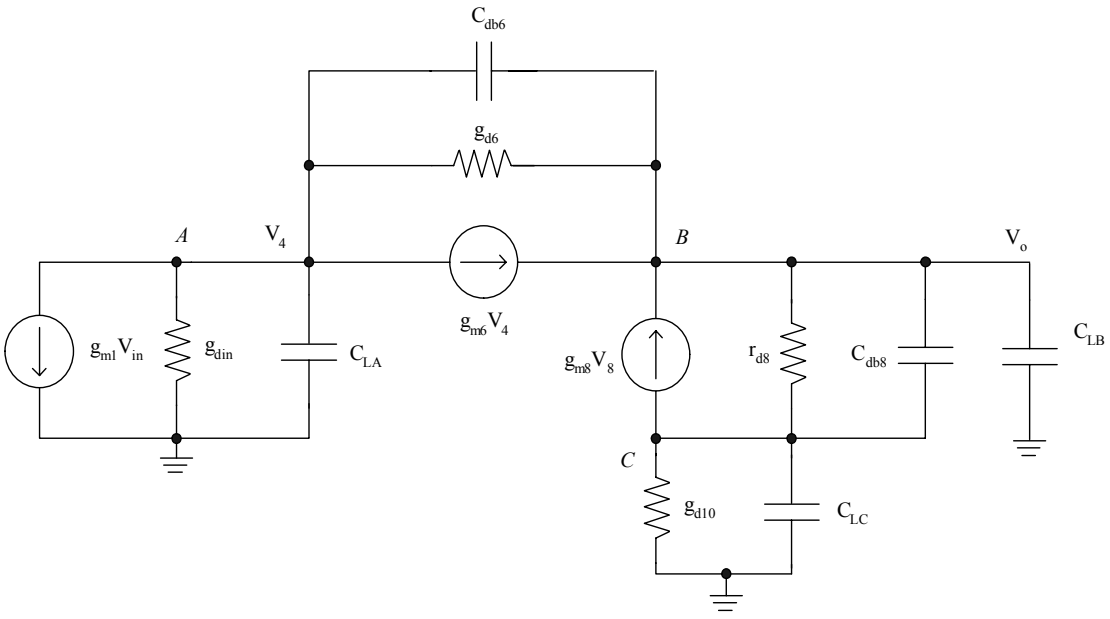


Figure 37. Small signal analysis

from the small signal equivalent circuit, which is shown in Figure 37. Node equations at node A, B and C are given as follows:

$$\text{A}: g_{m1}V_{in} + \frac{V_4}{g_{din}} + \frac{V_4}{sC_{LA}} + g_{m6}V_4 + \frac{V_4 - V_{out}}{g_{d6}} + \frac{V_4 - V_{out}}{sC_{db6}} = 0 \tag{24}$$

$$\text{B}: -g_{m6}V_4 + \frac{V_{out} - V_4}{g_{d6}} + \frac{V_{out} - V_4}{sC_{db6}} - g_{m8}V_8 + \frac{V_{out} - V_8}{r_{d8}} + \frac{V_{out} - V_8}{sC_{db8}} + \frac{V_{out}}{sC_{LB}} = 0 \tag{25}$$

$$\text{C}: g_{m8}V_8 + \frac{V_8 - V_{out}}{r_{d8}} + \frac{V_8 - V_{out}}{sC_{db8}} + \frac{V_8}{g_{d10}} + \frac{V_8}{sC_{LC}} = 0 \tag{26}$$

The capacitances C_{LA}, C_{LB} and C_{LC} represent the total capacitances at nodes A, B and C, respectively. These capacitances are related to the device capacitance as shown the following equations, where C_L is the external capacitance at the output terminal [29].

$$C_{LA} = C_{gd4} + C_{db4} + C_{db1} + C_{gs6} + C_{gb6} + C_{gd1} \tag{27}$$

$$C_{LB} = C_{gd8} + C_{gd6} + C_{db14} + C_{gs14} + C_{gb14} + C_L \tag{28}$$

$$C_{LC} = C_{db10} + C_{gd10} + C_{gs8} + C_{gb8} \tag{29}$$

Solving for the node equations and by approximation results in:

$$A_d = -\frac{g_{m1}g_{m6}g_{m8}\left(1 + \frac{sC_{db6}}{g_{m6}}\right)\left(1 + \frac{s(C_{LC} + C_{db8})}{g_{m8}}\right)}{P_1(s) + P_2(s)} \tag{30}$$

$$P_1(s) = g_{d8} g_{d10} g_{m6} \left(1 + \frac{sC_{db8}}{g_{d8}}\right)\left(1 + \frac{sC_{LC}}{g_{d10}}\right)\left(1 + \frac{s(C_{LA} + C_{db6})}{g_{m6}}\right) \tag{31}$$

$$P_2(s) = g_{din} g_{d6} g_{m8} \left(1 + \frac{sC_{LA}}{g_{in}}\right)\left(1 + \frac{sC_{LC}}{g_{m8}}\right)\left(1 + \frac{s(C_{LB} + C_{db6})}{g_{d6}}\right) \tag{32}$$

After manipulating the denominator, the following equations are obtained. The dominant pole and non-dominant pole is given as

$$p_1 = -\frac{1}{R_0 C_{LB}} \tag{33}$$

$$p_2 = -\frac{g_{m6}}{C_{LA}} \tag{34}$$

and unite gain frequency is

$$\omega_t = \frac{g_{m1}}{C_{Lc}} \tag{35}$$

In order to evaluate the various OpAmp characteristics, transistor levels DC and AC, transient response and noise simulation are performed using Spectra. The major specifications are 65 dB DC gain, 80^o phase margin and 45 MHz gain bandwidth, as shown in Figure 38. The slew rate simulation of the OpAmp is shown in Figure 39. Table **7** is a summary of the folded cascade amplifier design. The slew rate has a trade off with the DC gain. In addition, further increasing the slew rate results in a big bias

current which increases the power consumption of the OpAmp.

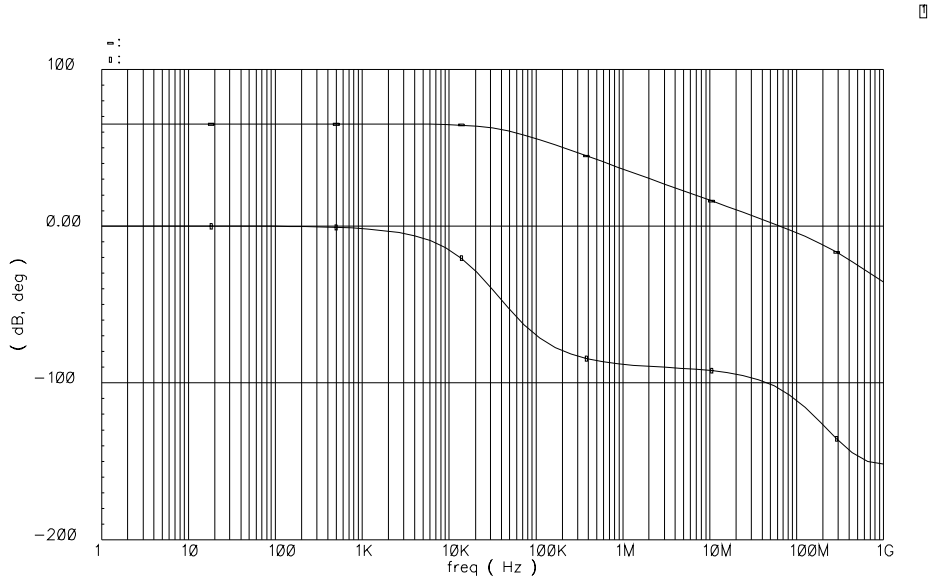


Figure 38. AC response of Opamp

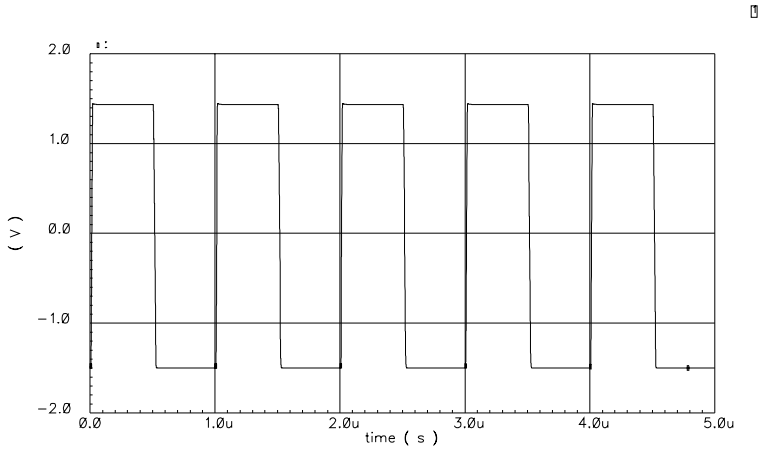


Figure 39. Transient response for slew rate

Table 7. OpAmp simulation summary

Items	
DC Gain	65 dB
Phase margin	80 deg
Gain Bandwidth	45 MHz
Slew Rate	480 V/us
Power Consumption	5.4 mW
Input Referred Noise	3.1×10^{-9}

(b) Noise Analysis

Today's analog designs deal with the noise problem because noise limits the minimum signal level, linearity, etc. In this section, we describe the phenomenon of noise and its effect on analog circuits. The objective is to provide sufficient understanding of the problem so that development of analog circuits can take noise into account. In this section, we consider methods of representing noise in circuit. We introduce thermal noise and 1/f noise, and describe how to reduce the noise effect with the used folded cascade differential amplifier. The main thermal noises come from $M_{4,5}$, $M_{10,11}$ and $M_{1,2}$ (input stages).

$$\overline{V_{n,out|M4,M5}^2} = 2 \cdot 4kT \frac{2}{3} g_{m4,5} \cdot R_{out}^2 \tag{36}$$

$$\overline{V_{n,out|M10,M11}^2} = 2 \cdot 4kT \frac{2}{3} g_{m10,11} \cdot R_{out}^2 \tag{37}$$

$$\overline{V_{n,out|M1,M2}^2} = 2 \cdot 4kT \frac{2}{3} g_{m1,2} \cdot R_{out}^2 \tag{38}$$

To compute the total input referred thermal noise, the above equations should be divided by its gain, $g_{m1,2}^2 R_{out}^2$.

$$\overline{V_{n,in}^2} = 8kT \left(\frac{2}{3g_{m1,2}} + \frac{2g_{m4,5}}{3g_{m1,2}^2} + \frac{2g_{m10,11}}{3g_{m1,2}^2} \right) \tag{39}$$

The flicker noise is expressed as

$$\overline{V_{n,in4,5}^2} = \frac{2k_p}{c_{ox}(wL)_{4,5}} \frac{1}{f} \frac{g_{m4,5}^2}{g_{m1,2}^2} \tag{40}$$

$$\overline{V_{n,in10,11}^2} = \frac{2k_n}{c_{ox}(wL)_{10,11}} \frac{1}{f} \frac{g_{m10,11}^2}{g_{m1,2}^2} \tag{41}$$

$$\overline{V_{n,in1,2}^2} = \frac{2k_n}{c_{ox}(wL)_{1,2}} \frac{1}{f} \tag{42}$$

The total input referred flicker noise is given as

$$\overline{V_{n,in}^2} = \frac{2}{c_{ox}} \frac{1}{f} \left(\frac{k_p \cdot g_{m4,5}^2}{(wL)_{4,5} g_{m1,2}^2} + \frac{k_n \cdot g_{m10,11}^2}{(wL)_{10,11} g_{m1,2}^2} + \frac{k_n}{(wL)_{1,2}} \right) \tag{43}$$

• Thermal noise can be minimized by making [30]

1. The g_m of the input transistor as large as possible, and
2. The W and L ratio of the gain stage as small as possible

• The flicker noise can be minimized by making

1. The area of the input transistors as large as possible, and
2. The length of the gain stage as long as possible

(c) Common Mode Feedback Circuit (CMFB)

The fully differential circuit has many advantages over the single ended design, such as greater output swing and avoidance of mirror pole. However, differential circuits require common-mode feedback.

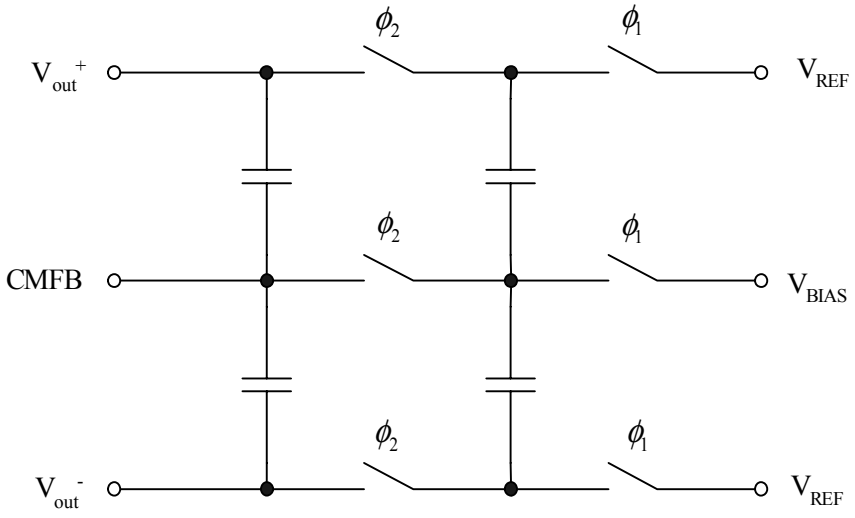


Figure 40. Discrete common mode feedback circuit

A switched capacitor CMFB is used to control the common mode level in this research. A switched capacitor CMFB is especially good for low voltage and high speed switched capacitor circuits, since it does not require extra power consumption and allows large output swing. The basic operation of the CMFB, shown in Figure 40, is that it generates a dynamic bias, which, together, make the actual common mode voltage equal the desired common mode voltage. Small size capacitors are used, as big capacitors can

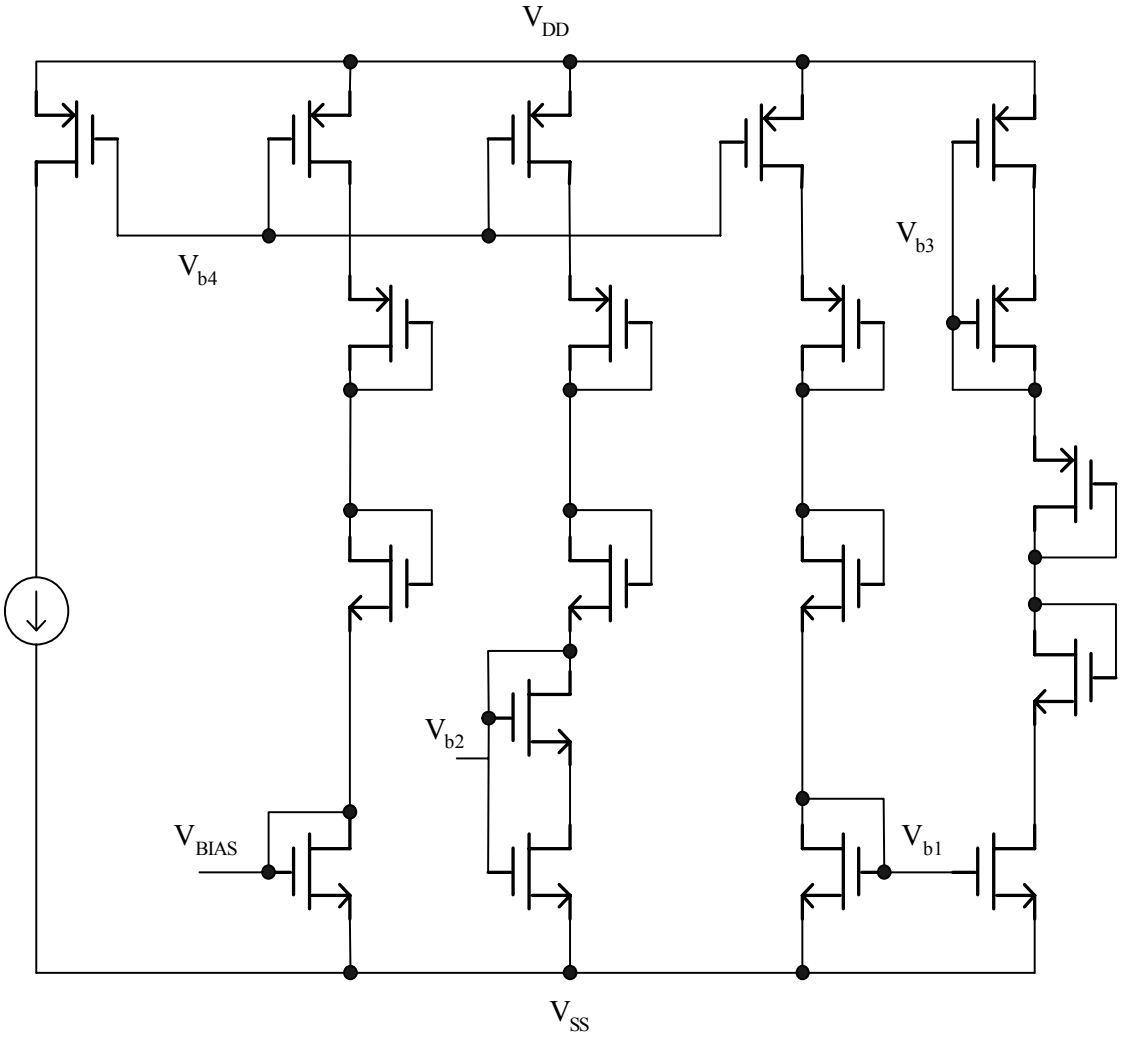


Figure 41. Bias generation circuit

overload the amplifier. The size of the switches and capacitors should be chosen carefully. To achieve a higher speed, a large aspect ratio and a small capacitor must be used.

(d) Bias Generator

A bias generator is designed for the OpAmp, in order to internally bias the loads and the cascade transistors. Also the common mode control voltage is generated from the bias generator. In particular, all desired bias voltages are generated by mirroring a single current 110uA. Figure 41 is the schematic of the bias generator.

6.2 Voltage Controlled Oscillator

In RF transceivers, we observe the use of an oscillator in both transmit and the receive paths. The PLL, including oscillator, provides the carrier signal for both the receive and transmit paths.

This section deals with the design of oscillators for RF communication to verifying this research idea. It emphasizes monolithic implementation and well controlled frequency tuning. It will begin with a description of the basic oscillator circuit used to generate initial frequency. Then it will show how the oscillator tunes operation frequency with the current control circuit.

Figure 42 shows the basic circuit configuration of the emitter-coupled multivibrator [31]-[33]. It is the CMOS version of a well know bipolar configuration. The oscillation frequency depends on the capacitor size and the amount of current

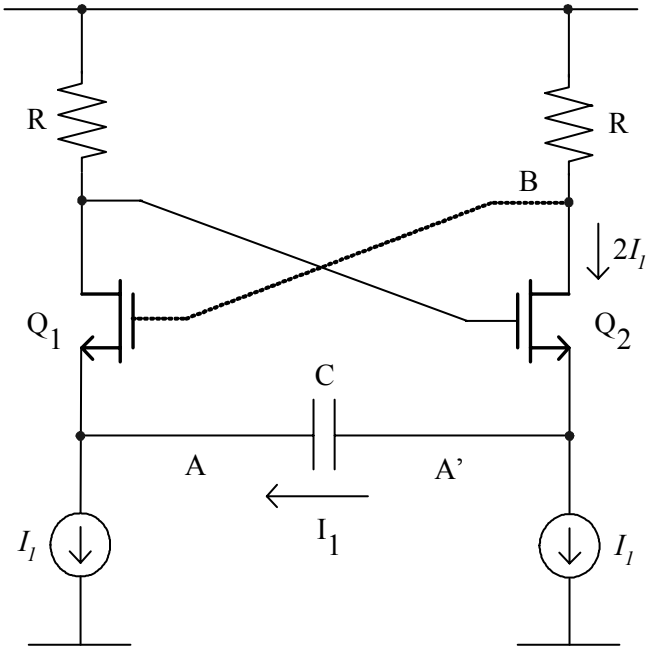


Figure 42. Emitter coupled oscillator

passing through it.

The circuit is comprised of a pair of gain stages made up of Q1 and Q2, which are then cross coupled with each other. The gain stages have equal load resistor, R. The sources of Q1 and Q2 are biased with matched constant current stages and are coupled through the timing capacitor, C.

The operation of the circuit can be briefly explained as follow. The cross coupling between Q_1 and Q_2 assures that either Q_1 or Q_2 is on at any given time, but not both. In this manner, the timing capacitor C is alternately charged with equal but opposite currents, first through Q_1 and then through Q_2, in alternate half cycles of oscillator operation. Assuming, for the moment, that during one half cycles, Q_1 is off and

Q_2 is conduction, then the equivalent circuit in this state appears as shown in Figure 42. Q_2 conducts a total current of $2I_1$, where one-half of the current is forced through the capacitor, C, in the direction indicated [31].

This condition assures that the total voltage swing at the collector of Q_2 to V_{CC}-($2I_1 \cdot R$). Under this condition, the gate of Q_1 is ϕ ($=2I_1 \cdot R$) drop below V_{CC} and the gate of Q_2 is V_{CC}. Since Q_1 is off, the current I_1, charging the capacitor C, is obtained from the source of Q_2. This current causes the voltage level, $V_{A,}$ at the source of Q_1 to ramp down with a constant slope of I_1/C, until the voltage level at the source of Q_1 becomes equal to V_{gs1}. At this point, the transistor Q_1 will turn on and Q_2 will turn off. The circuit stays in this state until the voltage level at the source of Q_2 ramps downward

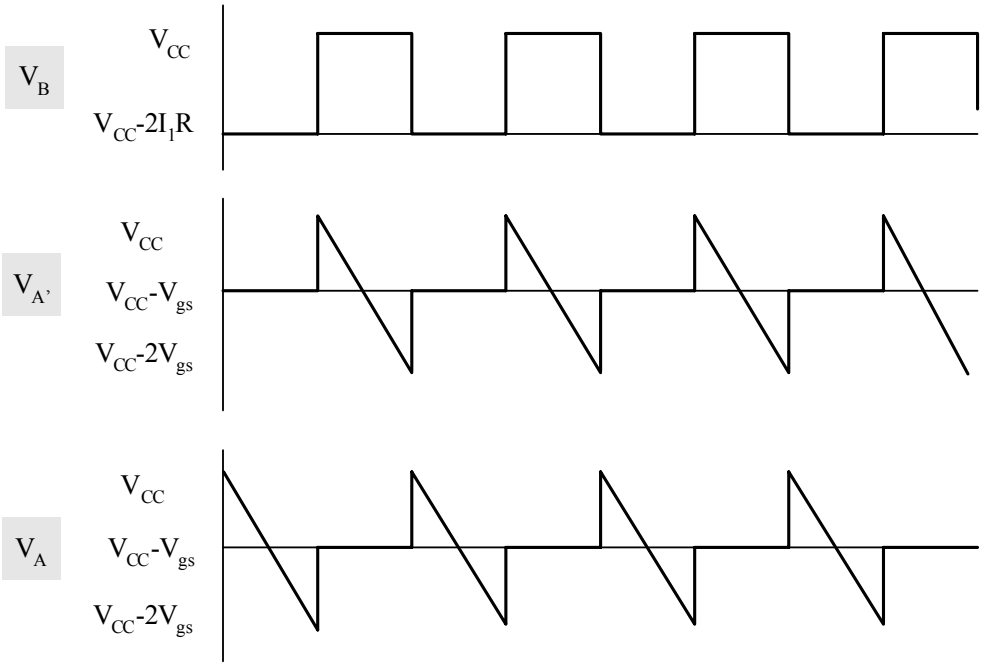


Figure 43. Waveforms of the emitter-coupled oscillator circuit

by an amount equal to V_{gs}. Figure 43 shows the basic waveforms of certain nodes in the circuit during the transitions between the two states. For the lower frequency, the current through the capacitor must be small, so that the ramp down slope will be slow.

The functions in the two additional sections (in the dashed blocks) enable the frequency control (Figure 44) [13]. These two functions change the core bias currents in a positive or negative direction under the control of a differential signal. The symmetric charge control block is designed to adjust the core VCO current so that the slope, I_1/C, is varied with the differential control voltage from LPF. For example, if V_{CTRL}^{+} goes up and V_{CTRL}^{-} goes down, some current I_3 is provided from capacitor.

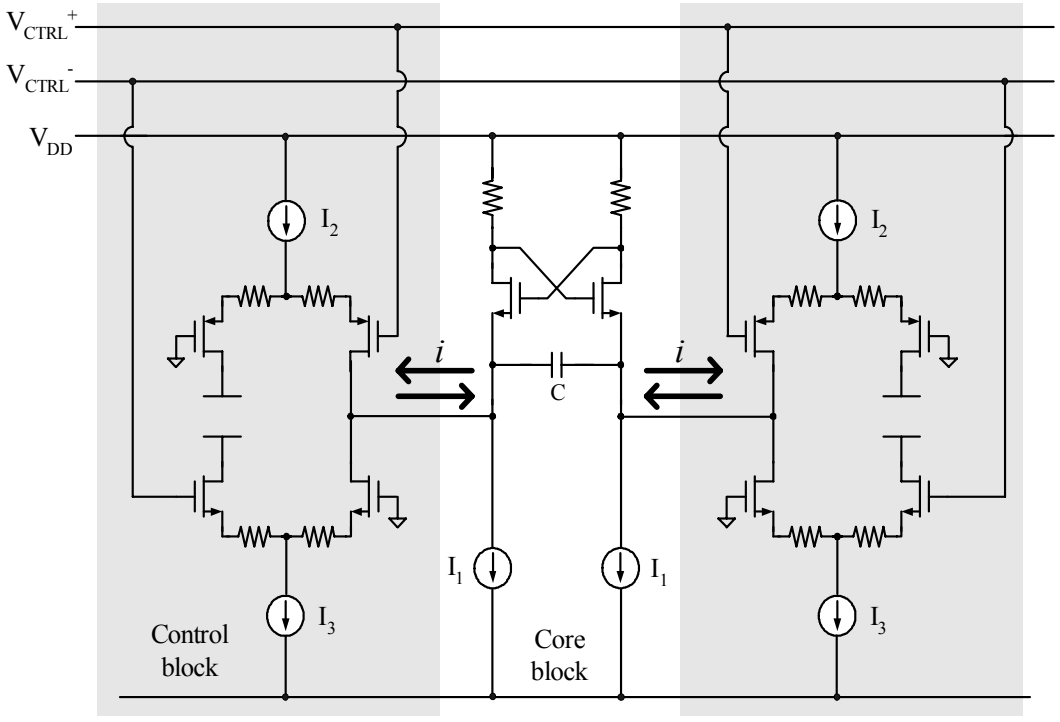


Figure 44. Frequency tuning circuit by using current control

J. Park and F. Maloberti, "Fractional-N PLL with 90° phase shift lock and active switched-capacitor loop filter," in *Proc. CICC,* ©[2005] IEEE.

It will produce more current at the core block and then make the frequency higher.

The capacitance C is 1.1pF, and the currents I_1 and I_2 are 1mA and 0.2mA respectively. The resulting range of frequency variation is ±25MHz. The degeneration resistances in the additional blocks help in improving the linearity of the control block. Simulation results show that their values are optimized by the transistor sizes for minimizing the 1/f noise, while keeping the speed leads to good linearity and reasonable phase noise.

Figure 45 shows the phase noise plot with schematic simulation. It follows that the phase noise is -117 dBc/Hz at 100 kHz offset.

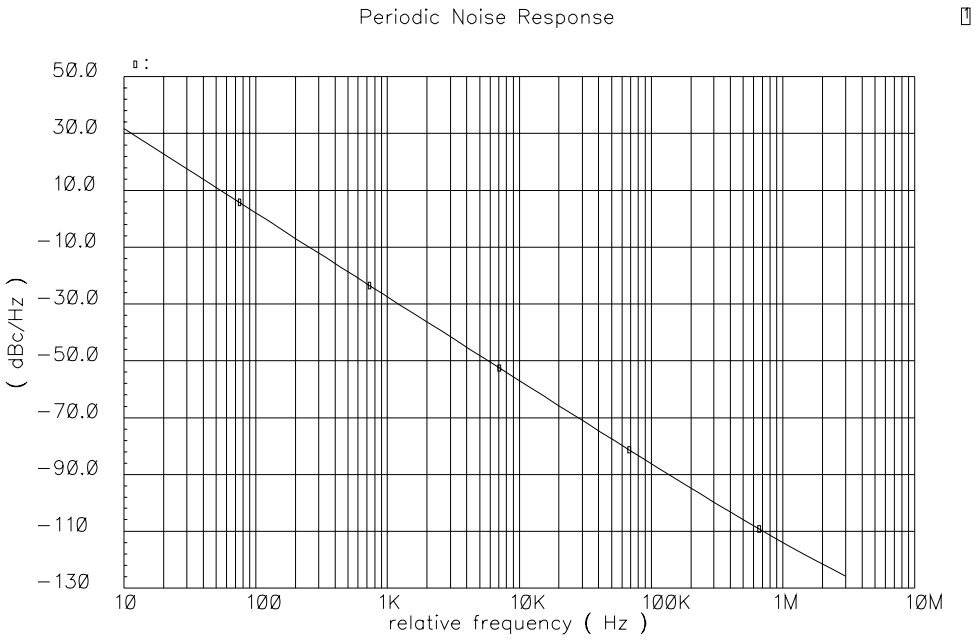


Figure 45. Phase noise plot

6.3 Digital Block Design

(a) Clock Generator

As we can see from the previous chapter, a switched capacitor base active filter is used. Each switch in the schematic is controlled by one of two clock phases, ϕ_1 and ϕ_2.

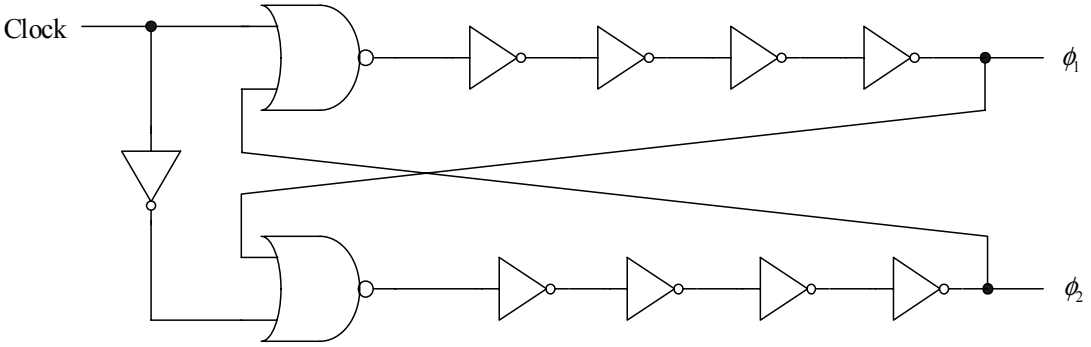


Figure 46. Non-overlapping clock generator

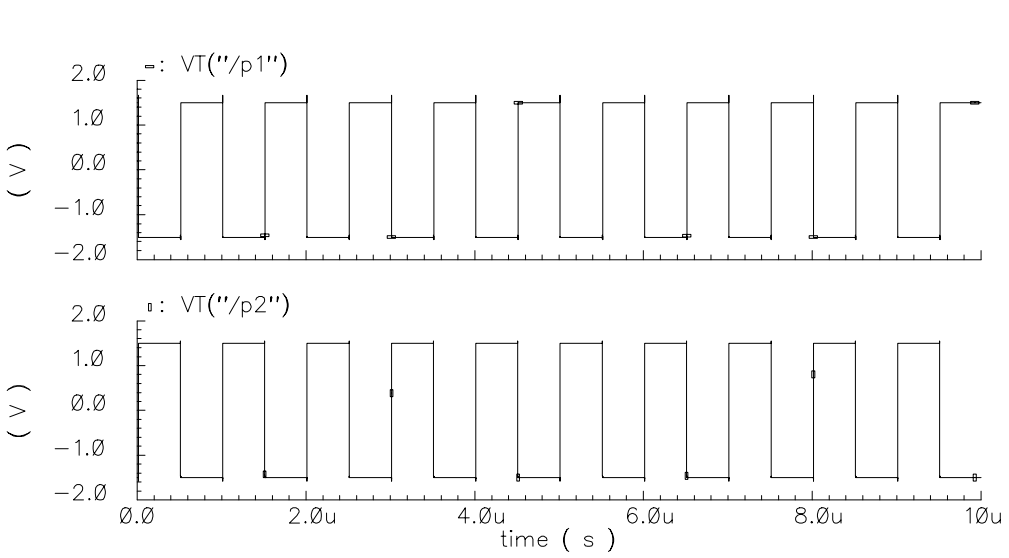
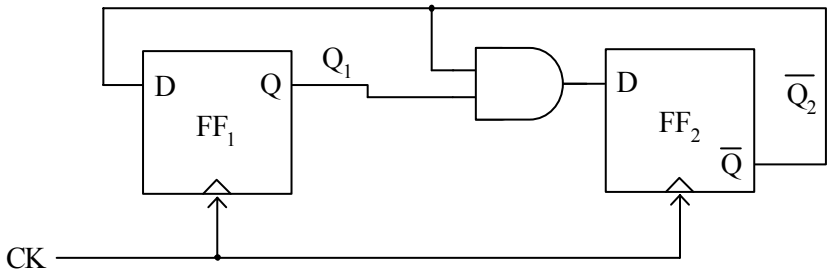


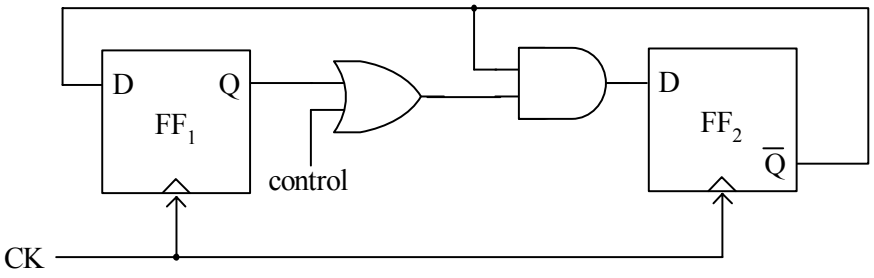
Figure 47. Clock waveform

We will assume that each switch is closed when its controlling clock signal is high and open when its clock signal is low. Since ϕ_1 and ϕ_2 are never both high at the same time, the switches controlled by one clock phase are never closed at the same time as the switches controlled by the other clock phase.

Figure 46 shows a simple digital circuit which is capable of generating the desired clock waveforms. The waveform ϕ_1 does not overlap with ϕ_2 as shown in Figure 47.



(a) Divider /3

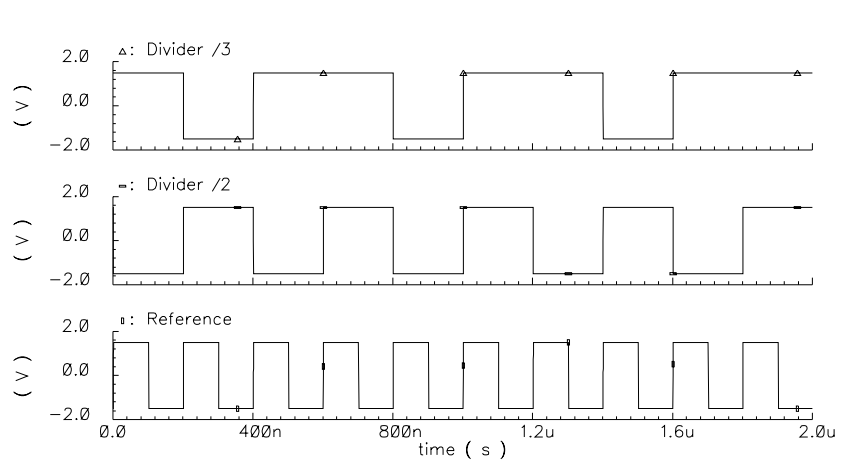


(b) Dual divider /2, /3

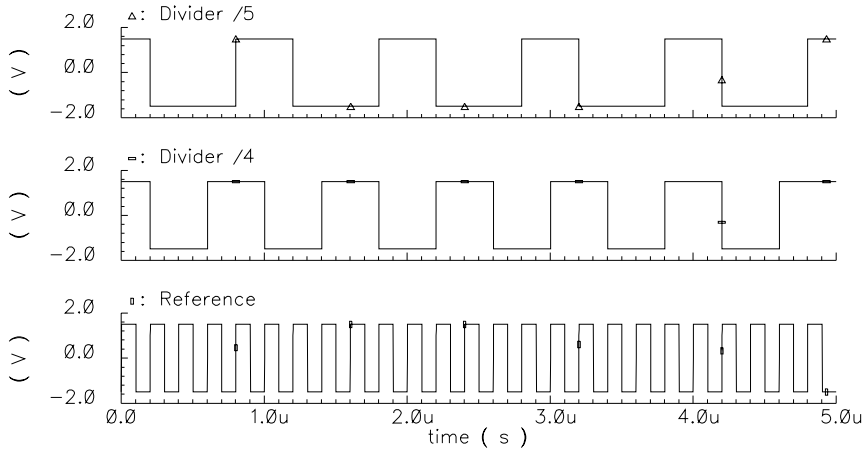
Figure 48. Digital divide

(b) Divider

Most phase locked synthesizers incorporate high speed dual or multimodulus dividers. Such a circuit divides the input frequency by one of the moduli according to a



(a) Dual divider /2,/3



(b) Dual divider /4,/5

Figure 49. Waveforms of dual divider

control signal. A commonly used dual modulus divider is a circuit which divides by 2 or 3. Figure 48(b) shows such a circuit, which is a modified version of Figure 48(a). This divider is configured as a $\div 2$ circuit when control is high and a $\div 3$ circuit when control is low.

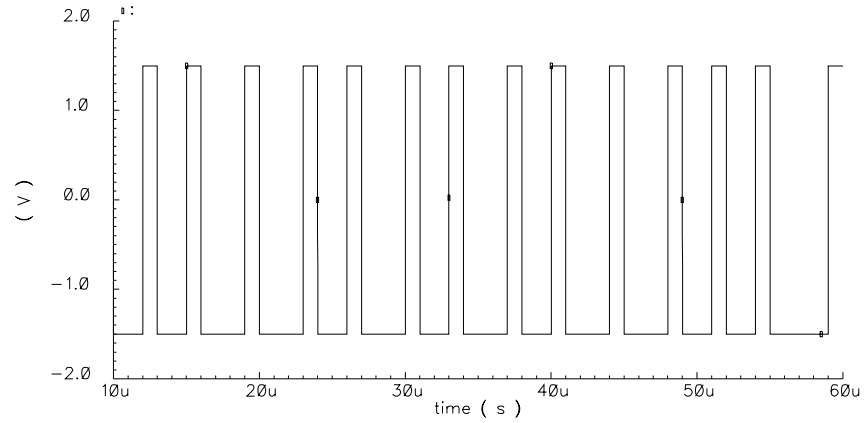
(c) Digital Sigma Delta Design

We reviewed the basic sigma-delta design in chapter 4 and now let us illustrate its time domain behavior using circuit level simulation. The output y[n] takes on values of 1.5 and -1.5 encoded in a signal bit that controls the digital divider.

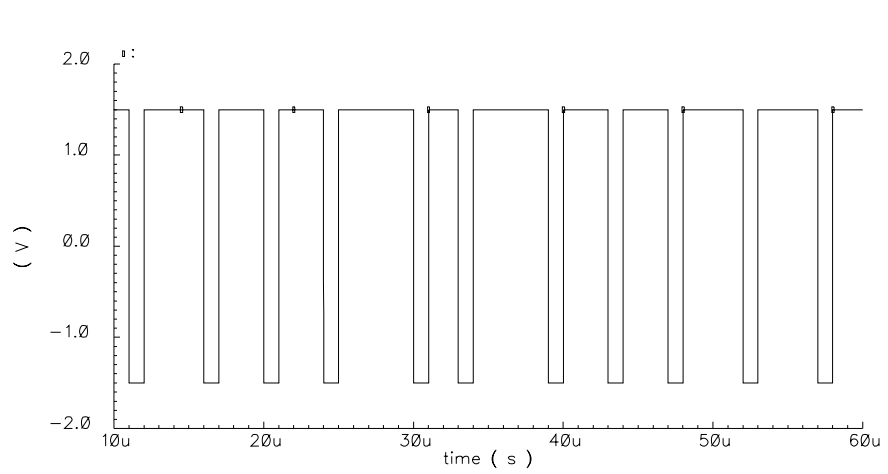
For a DC input x[n] = 1.5 (high level), all the modulator output values will be 1.5. For a DC input of -1.5 (low level), all the values will be -1.5. For a zero DC input, half of the modulator output values will be 1.5, and half -1.5. By averaging the modulator output over a period of time, we can approximate the input [27]. In other words, over a period of time, the proportion of high and low values will be directly related to the DC input value. The larger the input, the more high will be present in the output, and vice versa, for smaller inputs as shown in Figure 50.

6.4 Simulation Results

Figure 51 shows the circuit level simulation results for the whole loop with a modified 90 phase shift lock with PNE (dot line) and without PNE (solid line). As can be seen, the PNE block improves the phase noise level by decreasing loop gain after the loop goes into the locked zone.



(a) DC input = 0.28



(b) DC input = 0.78

Figure 50. Sigma-delta output

This schematic simulation supports the new concept to moving up the layout design for implementation.

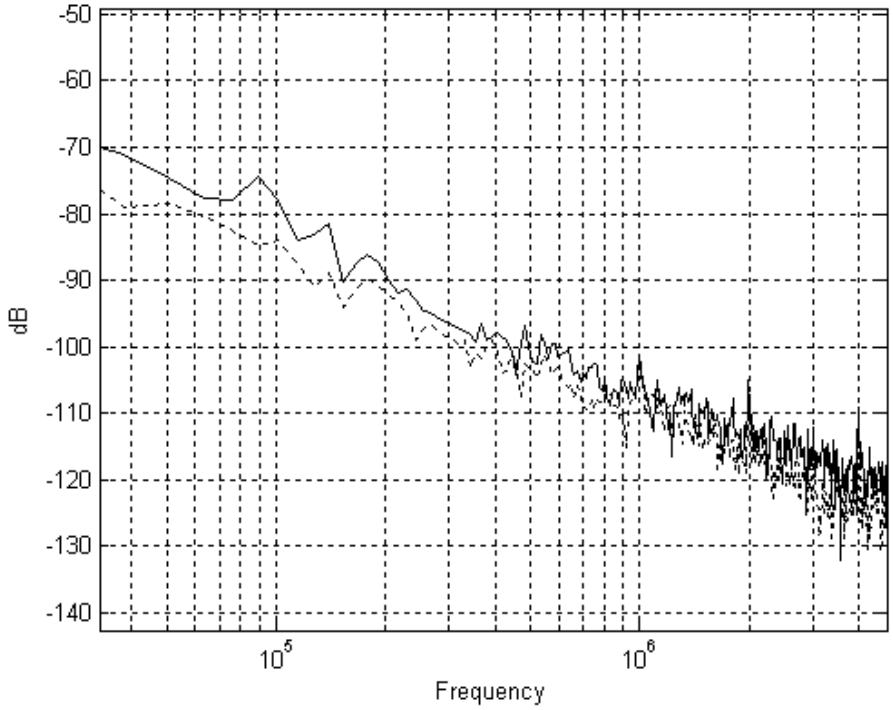


Figure 51. Simulation output. (phase noise without PNL (solid line), phase noise with PNL (dot line))

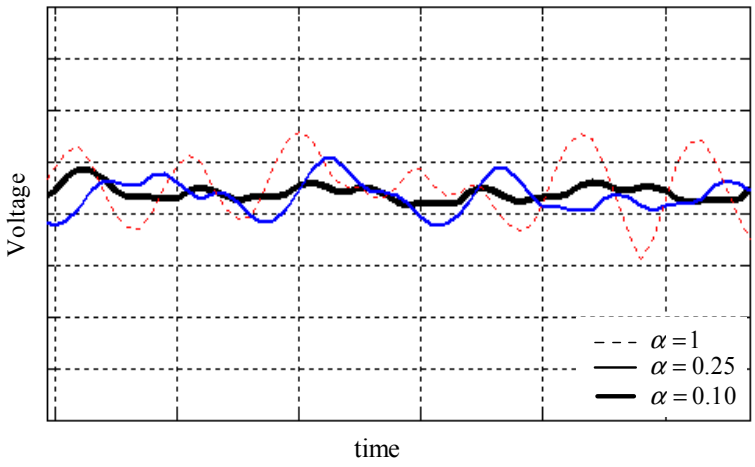


Figure 52. Control voltage variation according to the variable gain

Figure 52 illustrates the variation of control voltage to tune the VCO frequency. As expected from Equation (13), the control voltage variation becomes smaller, when variable gains are lower.

The value of variable gain should be considered carefully, because the loop should meet frequency hopping and noise recovery.

CHAPTER VII

EXPERIMENTAL RESULTS

The fully differential PLL discussed in previous chapters has been fabricated in a 0.25-μm CMOS technology with 2.8 mm^2 of active area. Because the LPF size is drastically decreased, the switch capacitor PLL becomes suitable for a full integration. The loop filter contains two capacitors of size around 40pF. The capacitors, VCO and digital sigma-delta modulator are integrated in the chip.

The circuit, excluding the output buffer, dissipates 30mW, of which 13.8mW is consumed by the VCO, 4.5mW by the digital sigma-delta and 5.4mW by the amplifier.

Successful testing of the PLL loop requires a detailed measurement to be performed. In order to satisfy this measurement requirement, the data process program, required for expeditiously analyzing the acquired data, was developed. Most of the data is accumulated at the digital sampling oscilloscope.

With proper shielding, the noise coupling is blocked from the digital block to the analog and the VCO. In addition, large on-chip PMOS capacitors are used to maintain a small bounce in the supply. Also, guard rings can be employed to isolate the analog block from the noise from the noisy digital block. The guard rings provide a low impedance path to ground for the charge carriers produced in the substrate.

The measured non-overlapping clocks, ϕ_1 and ϕ_2, are shown in Figure 53. These clocks will control the CMOS switches of the switched capacitor network.

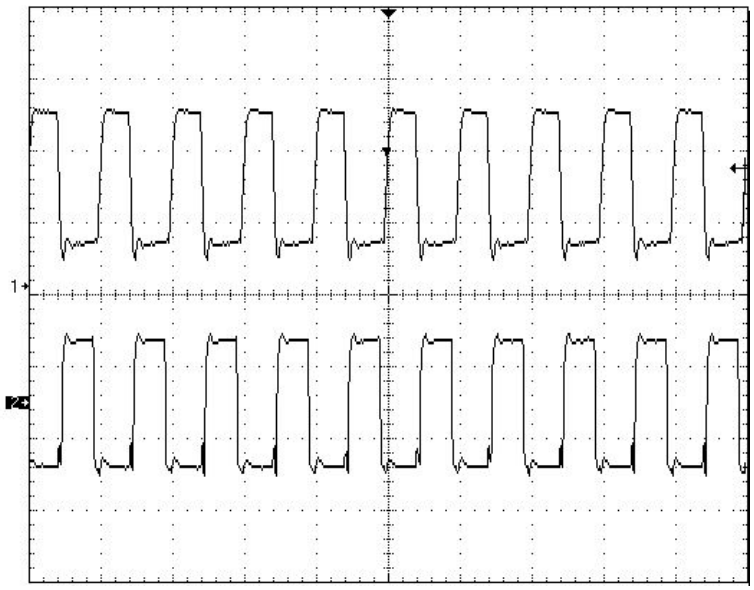


Figure 53. Non-overlapping clock

As the control voltage goes to the locked region of the loop, the sampling capacitor has an equivalent charging and discharging intervals in ϕ_1 and then accumulated current is transferred to LPF in ϕ_2. Thus, the control voltage results in oscillator output at the desired frequency. Figure 54 shows a sampling capacitor operation in the locked region [13]. The signal has the expected triangular shape in the charging and discharging phases. The trigger of the scope synchronizes itself during the first and second intervals of the reference period.

One of the main ideas in this research is the 90^o phase shift lock. Figure 55 illustrates its the operation. As can be seen, the reference clock and feedback signal show the 90^o phase shift. The output waveform of the VCO, which operates around 128.3 MHz, is shown in Figure 56. The divider has two moduli, 128 and 129, and provides an average modulus equal to 128+α.

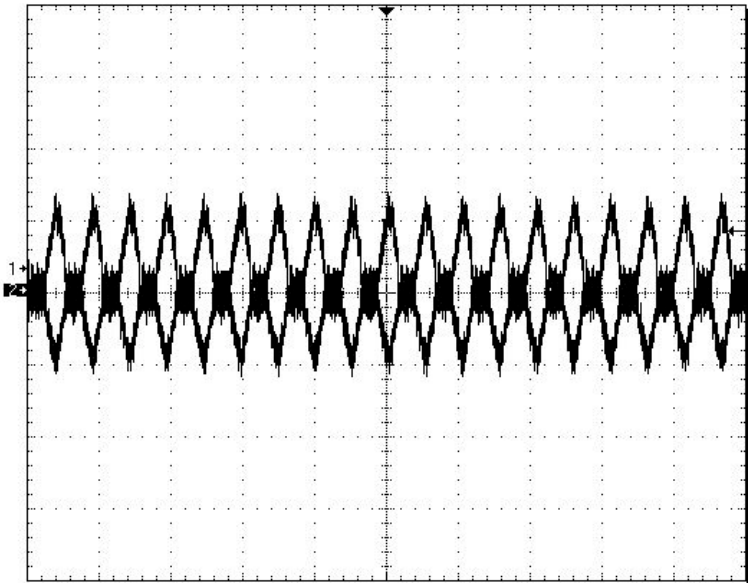


Figure 54. Sampling capacitor operation in locked zone

J. Park and F. Maloberti, "Fractional-N PLL with 90^o phase shift lock and active switched-capacitor loop filter," in *Proc. CICC,* ©[2005] IEEE.

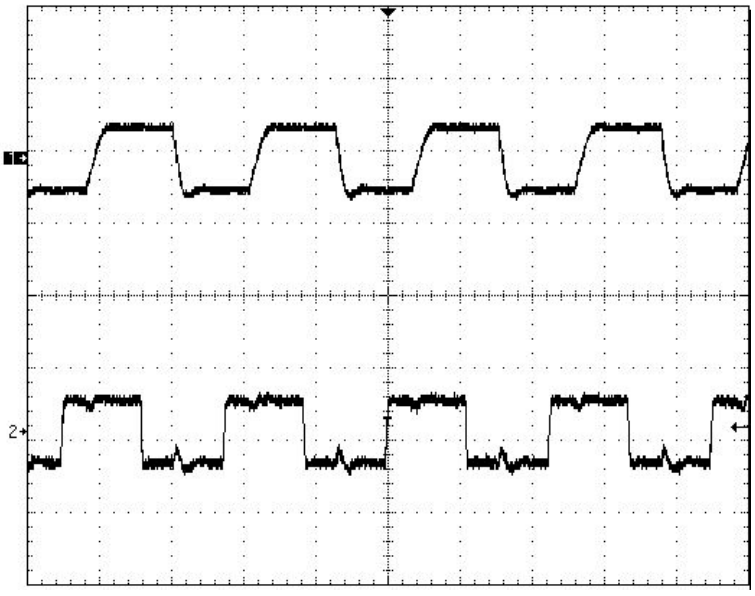


Figure 55. 90^o phase shift lock

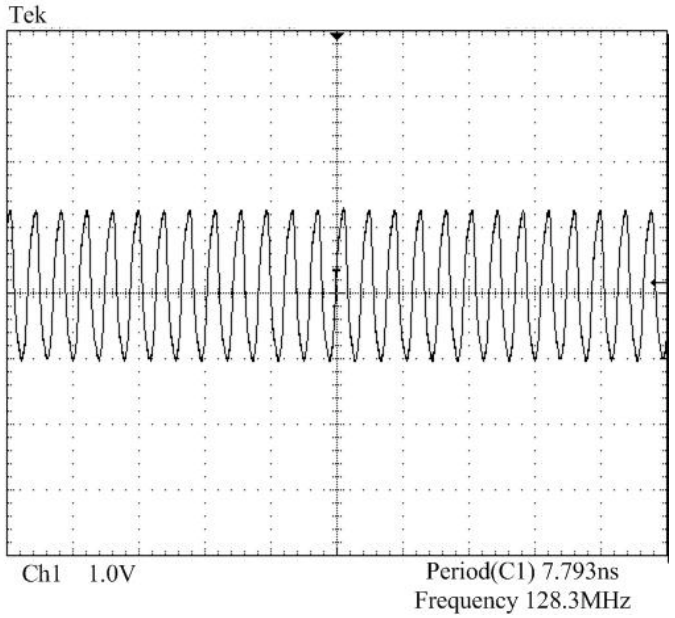


Figure 56. PLL output waveform

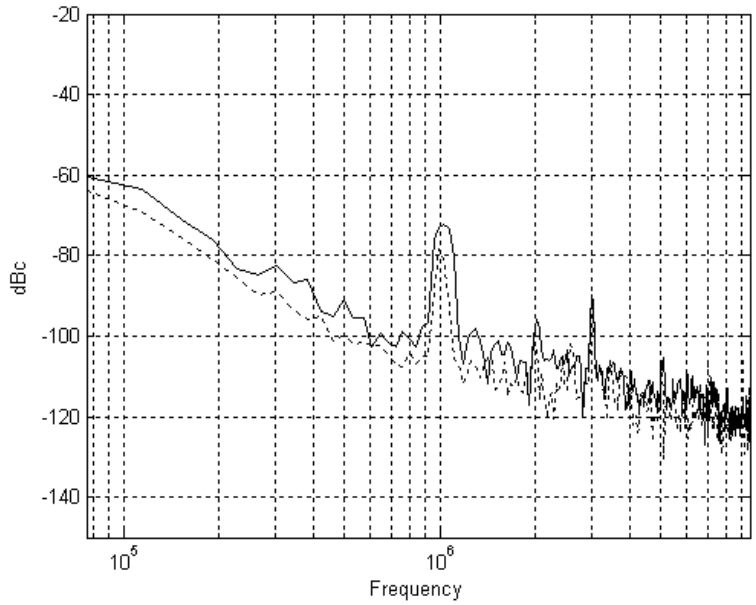


Figure 57. Phase noise measurement. (solid line(without error correction circuit) dashed line(with error correction circuit))

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As verified in the macro model and the subsequent schematic simulation, the PLL which has an phase noise enhancement block shows better phase noise performance. Figure 57 shows the measured phase noise with and without the PNE function. Results show that the PNE reduces the spur level below -80 dBc [13]. Moreover, the phase noise at 600 kHz is as low as -102 dBc; 5 dB better than without the enhancement circuit. Multiple gain values and a smart digital control might possibly permit 15dB of phase noise improvement. However, the spur level is not completely satisfactory. Continuous-time solutions obtain better results. Nevertheless, the result is still comparable with other published figures as shown in Table 8 [36].

Table 8. Previous work of PLL

	JSSC 98 [34]	JSSC 01 [35]	IEEE 04 [36]	This work
Architecture	Integer N	Frac N	Dual Loop	Frac N
Spurious Level	-83dBc	-55dBc	-55dBc	-80dBc
Chip Area	1.6mm^2	2.8mm^2	3.7mm^2	2.9mm^2
Phase Noise	-115dBc/Hz @600kHz	-100dBc/Hz @1MHz	-97dBc/Hz @1MHz	-102dBc/Hz @600kHz
Supply (V)	3V	3V	3.3V	3V
Consumption	90mW	60mW	49.5mW	30mW

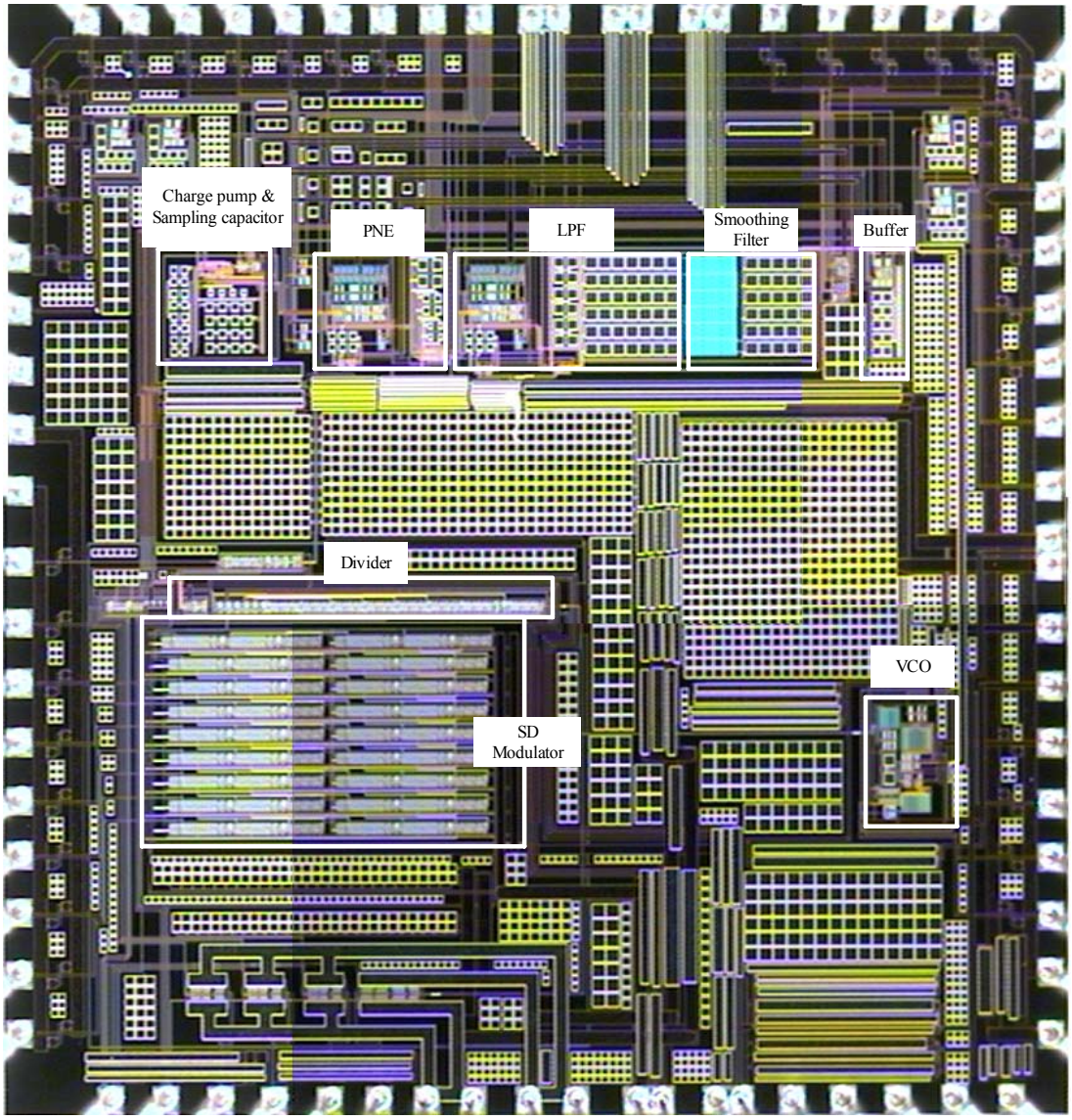

Figure 58. PLL die photograph

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Figure 58 shows the microphotograph of the fabricated chip and the entire die size is 2.9mm^2. As we can see in the die photograph, the mixed signal circuit employed different power supplies and ground, so as to avoid noise coupling by the large transient

noise by the digital section. The bonding wire connection of power supply to the package should be considered well because the bonding inductances will result ground bounce. In the fabrication, double bonding is used for power supply to decrease the inductance effect.

CHAPTER VIII

CONCLUSION

In recent years, the growing market of the mobile communication continues to drive for high performance to meet the system requirements. The present work has discussed the following design techniques to enhance the performance of the one of the most important block in communication system, the PLL:

- A switched capacitor filter can be effectively used to produce precise clock signals in a PLL. The 90^{o} phase shift lock and the SC filter have been introduced and subsequent improvement in the system performance has been verified.
- The phase noise enhancement is another idea that has been discussed in this work. Discrete time operation enables it to precisely change loop gain and thus avoid longer settling time.
- The opamp and oscillator with high supply noise immunity can be designed using differential architecture. The control voltage and loop filter of the PLL must be carefully isolated from supply noise. The present work uses an active filter based on the fully differential architecture due to its superior supply noise rejection properties.
- On-chip decoupling capacitors between the separated power supplies of the VCO have been used and they reduce supply variation and guarantee better signal output. Other noise parameters, namely the flick noise and the thermal noise, have also

been considered in the oscillator design as all the aforementioned sources determine the overall oscillator phase noise.

- The present work has presented theoretical and experimental results which indicate that the phase noise enhancement technique enables an increase in PLL bandwidth while satisfying the phase noise constraint.
- The SC based synthesizer using fractional PLL architecture has been fabricated in a 0.25μm CMOS technology.
- It can be verified that the PNE reduces the spur level below -80 dBc. Moreover, the phase noise at 600 kHz is as low as -102 dBc; 5 dB better than without the enhancement circuit.
- A switched capacitor LPF enables on-chip implementation with only 50pF used for the fully differential LPF and the entire chip area is at 1.7 x 1.7 mm^2. The capacitance usage is at least ten times smaller than a continuous-time counterpart.
- The noise performance meets or exceeds the results achieved in previous work [34]-[36] without the use of an extra processing step, an external loop filter.

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