DESIGN OF A 125 MHZ TUNABLE CONTINUOUS-TIME BANDPASS ΣΔ MODULATOR FOR WIRELESS IF APPLICATIONS

A Thesis

by

XUEMEI LIU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2004

Major Subject: Electrical Engineering

DESIGN OF A 125 MHZ TUNABLE CONTINUOUS-TIME BANDPASS ΣΔ MODULATOR FOR WIRELESS IF APPLICATIONS

A Thesis

by

XUEMEI LIU

Submitted to Texas A&M University
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE

Approved as to style and content by:

Jose Silva-Martinez (Chair of Committee)	Edgar Sanchez-Sinencio (Member)
Fred Strieter (Member)	Duncan M. (Hank) Walker (Member)
Chanan Singh (Head of Department)	

December 2004

Major Subject: Electrical Engineering

ABSTRACT

Design of a 125 MHz Tunable Continuous-time Bandpass Modulator
for Wireless IF Applications. (December 2004)
Xuemei Liu, B.S., Xi'dian University;
M.S., Xi'dian University, Xi'an, PR China
Chair of Advisory Committee: Dr. Jose Silva-Martinez

Bandpass sigma-delta modulators combine oversampling and noise shaping to get very high resolution in a limited bandwidth. They are widely used in applications that require narrowband high-resolution conversion at high frequencies. In recent years interests have been seen in wireless system and software radio using sigma-delta modulators to digitize signals near the front end of radio receivers. Such applications necessitate clocking the modulators at a high frequency (MHz or above). Therefore a loop filter is required in continuous-time circuits (e.g., using transconductors and integrators) rather than discrete-time circuits (e.g., using switched capacitors) where the maximum clocking rate is limited by the bandwidth of Opamp, switch's speed and settling-time of the circuitry.

In this work, the design of a CMOS fourth-order bandpass sigma-delta modulator clocking at 500 MHz for direct conversion of narrowband signals at 125 MHz is presented. A new calibration scheme is proposed for the best signal-to-noise-distortion-ratio (SNDR) of the modulator. The continuous-time loop filter is based on Gm-C resonators. A novel transconductance amplifier has been developed with high linearity at high frequency. Q-factor of filter is enhanced by tunable negative impedance which cancels the finite output impendence of OTA. The fourth-order modulator is implemented using 0.35 μm triple-metal standard analog CMOS technology. Postlayout simulation in CADENCE demonstrates that the modulator achieves a SNDR of 50 dB (~8 bit) performance over a 1 MHz bandwidth. The modulator's power consumption is 302 mW from supply power of ± 1.65V.

To my parents, brother

ACKNOWLEDGMENTS

I would like to take this opportunity to express my appreciation to many people who have made my research and this master's thesis possible.

First and foremost, I am deeply indebted to my advisor, Professor Jose Silva-Martinez, who has given me timely encouragement, guidance and patience as well as financial assistance throughout the entire research work. I have benefited tremendously from his knowledge, keen insight and enthusiasm.

I would also like to pay special thanks to Professor Edgar Sanchez-Sinencio for his invaluable advice on many issues related to the course projects and my research. I enjoyed the two advanced graduate-level courses in analog IC design he taught.

I want to thank Prof. Fred Strieter and Prof. Duncan M. (Hank) Walker for taking time to be my committee members and kindly sharing their academic experience.

It would be much different and difficult scenario without my project partner, Bharath Kumar Thandri. Illuminating technical discussion with him made my research cycle very productive. I would especially like to thank Xiaohua Fan, without his resourceful assistance this project would not have been completed easily. I am particular thankful to Haitao Tong for extensive discussion and valuable suggestions.

A great deal of gratitude goes out to my friends and office-mates, their constant feedback created an environment that fosters learning, collaboration and encouragement. I can not name them all but special thanks to Wenchang Huang, Jianhong Xiao, Shanfeng Cheng, Jinghua. Li, Jianlong Chen, Guang Zhang, Dr. Chunyu Xin, Dr. Mengdeng Cheng, Dr. Pedro Estrada, Alberto Valero-lopez, Johnny Lee, Lin Chen.

My study at AMSC is very memorable thanks to Ms. Ella M. Gallagher. Her kindness touched all sides of my life here and made it much easier for me.

I am very blessed with the unyielding love and encouragement of my parents and my brother. Last but not the least, I thank my husband for his unconditional love.

TABLE OF CONTENTS

CHAPTER Page

LIST OF FIGURES

FIGURE Page

FIGURE Page

LIST OF TABLES

CHAPTER I

INTRODUCTION

1. Conventional Receiver Architectures

With growing demand for wireless communication, the integrated circuit design for radio-frequency (RF) communication receivers has focused on high level of integration with small size, low power and low cost. To achieve these goals, the incoming radio frequency signals must be digitized. There are two RF receiver architectures where the on-chip solutions are practical: direct conversion and superheterodyne conversion.

Fig. 1. depicts the direct-conversion architecture. After the RF signal is selected by the external RF filter and amplified by LNA, the signal is mixed directly to DC by a quadrature mixer. The analog baseband filter performs the channel selection before A/D conversion. Direct conversion architectures consume less power than superheterodyne receivers do. However, it has several problems that affect the circuit performance such as DC offset, local oscillator leakage and flicker noise.

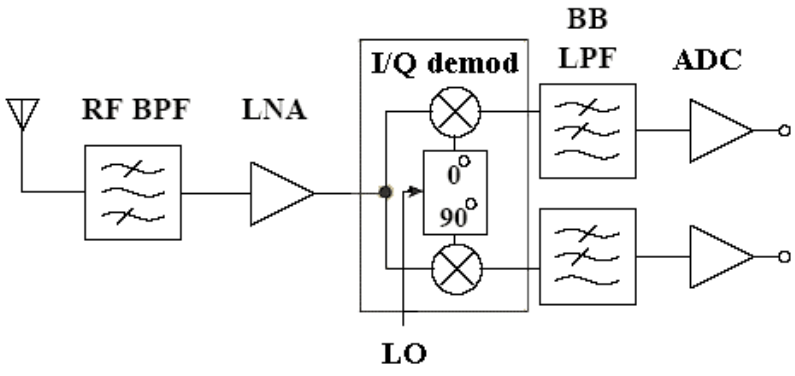


Fig. 1. Direct conversion architecture.

This thesis follows the format of *IEEE Journal of Solid State Circuits.*

Superheterodyne receiver architecture is shown in Fig. 2. First, the RF band signal is selected and amplified, as in direct conversion architecture. Then the signal is mixed to the first intermediate frequency (IF) before a quadrature down-converter. Compared to the direct conversion receiver, superheterodyne receiver includes two stages of down conversion and filters and hence increases the power consumption. Also, the I/Q demodulation is carried out in the analog domain.

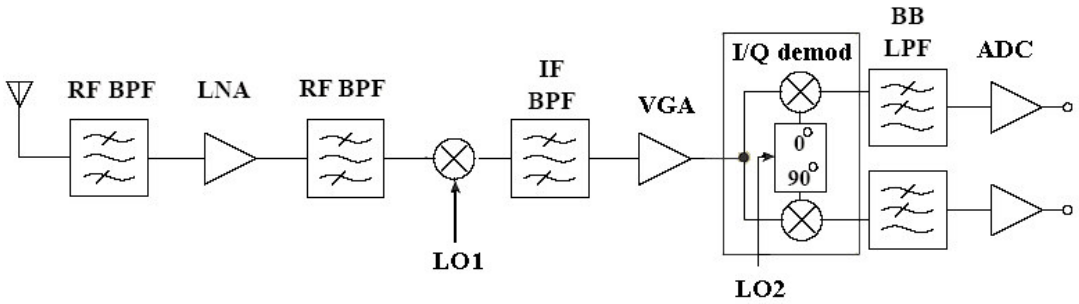


Fig. 2. Superheterodyne receiver architecture.

As Fig. 3. shows, digital IF receiver [1] is similar to the superheterodyne receiver except that the signal after the first IF is completely digital. It makes the low frequency operations, such as the second mixing and channel filtering in superheterodyne receiver, more efficient in the digital domain. The digital demodulation not only eliminates the I/Q mismatch problem inherent in analog demodulators but also provides more flexibility for the implementation of multi-mode functionality [2]. With the current technology developments, the size and power consumption will be scaled down. The digital IF architecture requires A/D conversion operating at high frequency, which is limited by linearity and dynamic range requirements due to the possible large adjacent interferes. In this thesis, a continuous-time ΣΔ modulator used in the digital IF receiver architecture is presented**.**

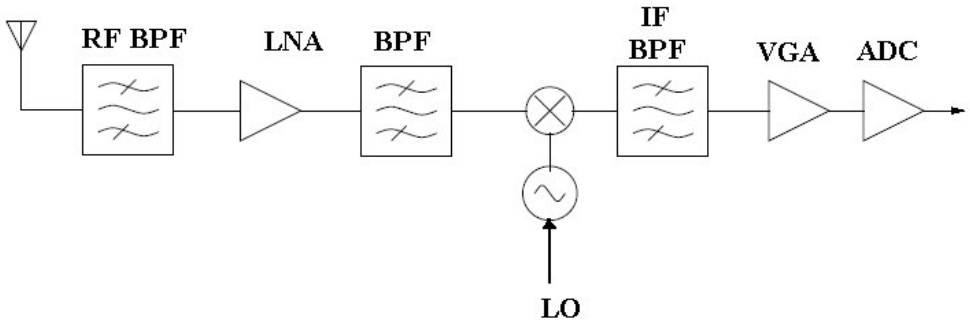


Fig. 3. Digital IF receiver architecture.

2. Analog-to-Digital (A/D) Conversion

The real world signals are inherently analog. However, digital signals can be processed in a more robust and cost-effective way. Therefore high performance data converters become critical for the full exploitation of digital signal processing techniques.

Data converters have traditionally been related to high resolution and low frequency application. It is always a tradeoff between speed and resolution. As Fig. 4. shows, flash A/D converters are the fastest A/D topology but suitable for a low resolution application.

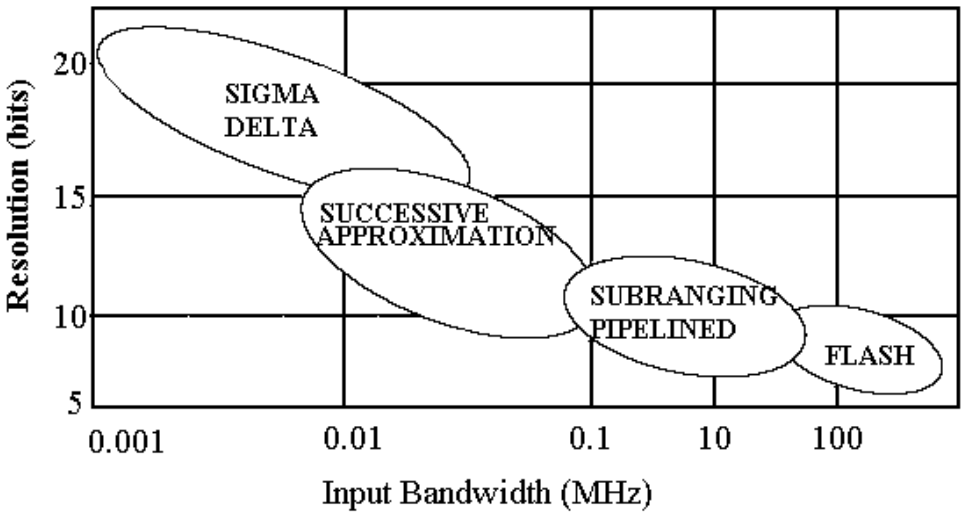


Fig. 4. Different A/D converters architectures.

The resolution is traded against conversion time in both of pipeline and successive approximation structures. In sigma-delta topology, the resolution is traded against the oversampling ratio which eventually limits its speed.

Fig. 5. shows the system difference between conventional A/D converter (also called Nyquist rate A/D converter) and sigma-delta (ΣΔ) A/D converter. The conventional A/D converter requires a high-performance analog lowpass filter before the sampling. However, in a ΣΔ A/D converter, the requirement for the filter is relaxed because of the high oversampling rate. The circuitry for the ΣΔ A/D converters is simple, compared to conventional A/D converters. ΣΔ A/D converters are not suitable for the high-resolution application for wide band signals because of the high OSR required.

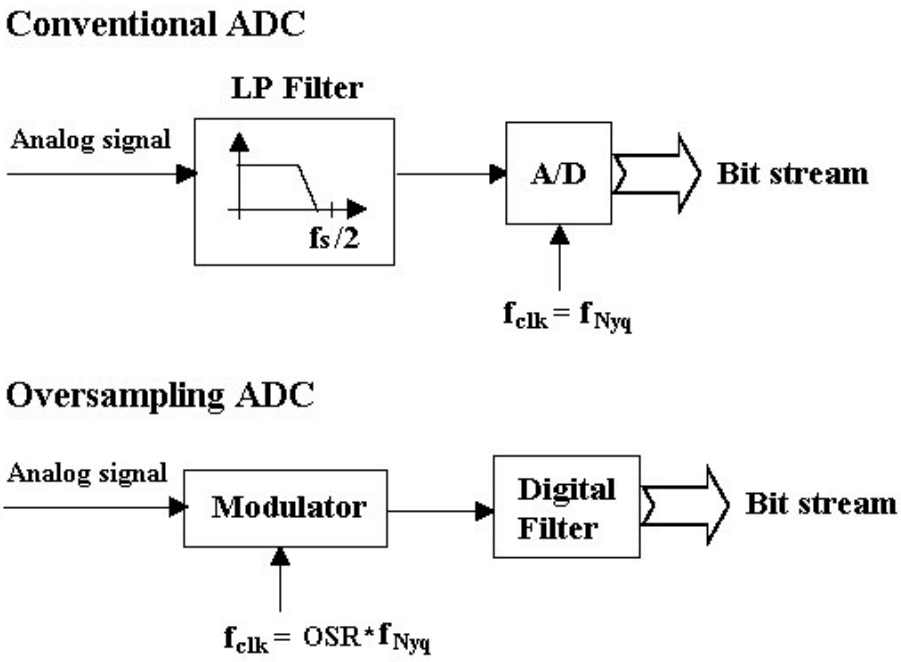


Fig. 5. A/D converters by Nyquist rate and oversampling rate.

3. Sigma-Delta (ΣΔ) A/D Converters

There are two basic principles involved in the operation of ΣΔ A/D converters: oversamping and noise shaping. The oversamping spreads the quantization noise over a bandwidth, which is equal to the sampling frequency and therefore reduces the quantization noise in the signal bandwidth. Also the ΣΔ A/D converters "shape" the quantization noise out of the signal bandwidth.

The advantages of ΣΔ A/D converter are outlined as follows,

- The cost of implementation is low and will continue to decrease because most circuits in sigma-delta converters are inherently digital. It also means that the performance will not drift drastically with time and temperature. Integrated with other circuitry becomes feasible.
- They minimize the requirements for analog anti-aliasing filters due to the high oversampling ratio.
- They achieve high solution due to the noise shaping characteristics of the modulator noise transfer function.
- They are inherently self-sampling and tracking and do not need any external sample and hold circuit.
- The background noise level is independent of the input analog signal level.

Also bandpass ΣΔ A/D converters can convert RF or IF narrow band signals directly to digital signals. The above advantages make bandpass ΣΔ A/D converters very attractive for digital IF receivers or other radio HF applications.

4. Organization of the Thesis

There are five chapters in the thesis. Chapter I gives an introduction to the research, including a short summary of three receiver architectures and the most important advantages of ΣΔ modulators.

Chapter II introduces the theoretical basis of the ΣΔ modulators. The fundamentals of the discrete-time lowpass ΣΔ modulator, discrete-time bandpass ΣΔ modulator and the continuous-time bandpass ΣΔ are covered in this section. A method to transform transfer function of the loop filter in the discrete-time domain to one in the continuous-time domain is described. Furthermore, a proposed structure of the fourth-order bandpass continuous-time ΣΔ modulator is presented. Then some implementation considerations about bandpass ΣΔ modulators are listed.

Chapter III focuses on the design of the 4^{th} order bandpass ΣΔ modulator. A proposed linear OTA used in the loop filter is discussed . Then the design and simulation for each block, which includes loop filter, feedback DACs, comparator and CMFB, are analyzed and described.

In chapter IV, circuit level simulations and postlayout simulation results are presented. The performance of the continuous-time bandpass ΣΔ modulator is summarized as well. The system was realized in a standard 0.35 μm CMOS process and the chip is under fabrication thanks to MOSIS educational service.

In chapter V, the conclusions of this research work are drawn .

CHAPTER II

SIGMA-DELTA MODULATOR

1. Introduction

Digital signal processing enables complex modulation and filtering of IF signals in the digital domain. Appropriate A/D converters are required for the function. In recent years, some publications [3] – [7] investigated the use of bandpass ΣΔ modulator for this application. Most reported bandpass ΣΔ modulators were realized with discrete-time circuits such as switched capacitor [7]-[8] or switched-current circuits [9]. However, they have a rather low upper-limit in operating frequency due to both switch resistance and limited speed of closed-loop amplifiers. It is possible to replace discrete-time loop filter by continuous-time counterpart. The modulator is called continuous-time modulator. It contains inherently anti-alias filtering and it is much faster because they relax the requirements of high speed Opamps and the settling time of the circuitry. Some continuous-time modulators that use Gm-C techniques [10] or LC filters [11] have also been reported.

In the chapter, firstly the fundamentals of the ΣΔ modulator are discussed to have a good understanding of its operation. Secondly, the proposed architecture of a fourth-order continuous-time bandpass ΣΔ modulator is depicted. Some practical design issues are then discussed.

2. Fundamentals of Sigma-Delta Modulator

2.1 Quantization Noise

All digital modulators include two functions: sampling in time and quantization in amplitude. If the quantization level is Δ and the quantization error e is uniform in the range $\pm \Delta/2$, the mean square value (quantization noise power) is given by,

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.1}$$

If the quantized signal is sampled at frequency f_s, the quantization noise folds into the frequency band [0, $f_s/2$]. Assuming the quantization noise is white, we may get the spectral density of the sampled noise as

$$E(f) = \sqrt{\frac{e_{rms}^2}{f_s/2}} = e_{rms}\sqrt{\frac{2}{f_s}} \tag{2.2}$$

The oversampling ratio (OSR) is the ratio of the actual sampling rate f_s to the Nyquist rate for the signal band $2f_B$:

$$OSR = \frac{f_s}{2f_B} \tag{2.3}$$

Hence, the noise power falling into the signal band is given by,

$$n_o^2 = \int_0^{f_B} E^2(f)df = e_{rms}^2 \frac{2f_B}{f_s} = \frac{e_{rms}^2}{OSR} \tag{2.4}$$

The above expression shows that the in-band quantization noise can be reduced by 3dB if the sampling frequency f_s is doubled.

Fig. 6. depicts the noise power spectral density with two different signal-sampling rates. As we noticed, only a small part of noise power falls into the signal band $[-f_B, f_B]$ if the oversampled conversion is used.

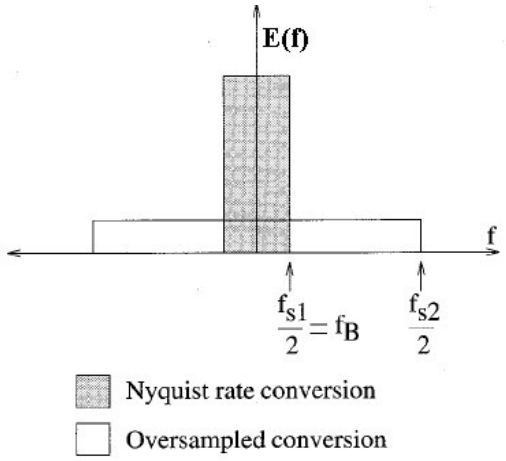


Fig. 6. Quantization noise power spectral densities for Nyquist rate and oversampled rate [12].

2.2 Discrete-Time Lowpass ΣΔ Modulator and Noise Shaping

A ΣΔ modulator includes three important components: a loop filter, a clocked quantizer and a feedback digital-to-analog converter (DAC), as shown in Fig. 7,

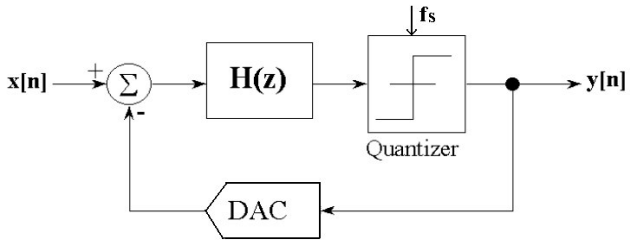


Fig. 7. Block diagram of a ΣΔ modulator.

If the quantization noise is white noise and independent of the input, we can use a linear model of the quantizer, shown in Fig. 8. We replaced the quantizer by an adder and a noise source *e*. Now the output *y* in frequency domain can be obtained as follows,

$$\begin{aligned} Y(z) &= \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) \\ &= STF(z) \cdot X(z) + NRF(z) \cdot E(z) \end{aligned} \tag{2.5}$$

Where *STF* and *NRF* mean signal transfer function and noise transfer function, respectively. If $H(z) >> 1$, then $Y(z) = X(z)$.

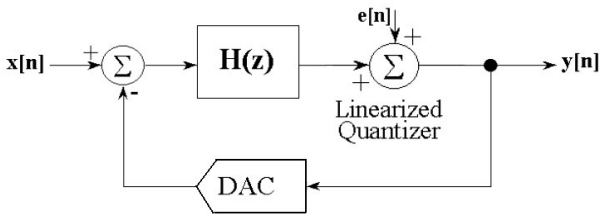


Fig. 8. ΣΔ modulator with a linearized quantizer.

We assume that the loop filter is a discrete-time first-order lowpass filter, and then its first-order transfer function is,

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.6}$$

If the DAC is ideal and it has a unity gain, the modulator output could be written by using the linear quantizer model,

$$Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z) \tag{2.7}$$

We notice that the output delays the input by one clock period. Since the *NTF* has a zero at DC frequency, the quantization noise is shaped by a highpass transfer function.

2.3 Discrete-Time Bandpass ΣΔ Modulator and Noise Shaping

Lowpass modulators realize zeros of *NTF* at DC or low frequencies on the unit circle of the Z plane. The upper-frequency is $f_c + f_B / 2$ for a bandpass signal that is located at a medium frequency f_c with a narrow bandwidth f_B. In this case it is not practical for a lowpass modulator to operate at medium or high frequency because the sampling frequency is required to be greater than the Nyquist frequency.

If the integrator in lowpass ΣΔ modulator is replaced by a resonator, which is equivalent to the transformation $z^{-1} \to -z^{-2}$, it leads to a bandpass ΣΔ modulator, and the zeros of *NTF* are located at non-zero frequency. It means that bandpass ΣΔ modulator makes the high-resolution conversion of bandpass signal possible if the sampling frequency f_s is greater than f_B instead of $f_c + f_B/2$. No matter where the signal is centered, the quantization noise is attenuated over the signal band for a large OSR or $f_s/(2f_B)$.

Using the aforementioned transformation to the first-order lowpass filter in 2.2, we get the transfer function of a resonator as,

$$H(z) = \frac{z^{-2}}{1+z^{-2}} \tag{2.8}$$

If the DAC is ideal and has a unity gain, the modulator output can be expressed as,

$$Y(z) = z^{-2} \cdot X(z) + (1+z^{-2}) \cdot E(z) \tag{2.9}$$

The *STF* is z^{-2} and it causes clock period delay between input and output. The *NTF*, which is $1+z^{-2}$, has zeros at the frequencies $\pm nf_s/4$ (n=1,3…). The transformation $z^{-1} \to -z^{-2}$ maps the zeros of *NTF* from DC to $\pm f_s/4$ (or $\pm\frac{\pi}{2}$), $\pm 3f_s/4$, etc. For a center frequency f_c, the sampling frequency has the relation $f_C = f_S/4$ if $n=1$. Therefore the quantization noise can be shaped away from f_c. The bandpass modulator has the same stability and properties of the lowpass prototype. The difference between the lowpass and bandpass modulator is shown in Fig. 9. [2],

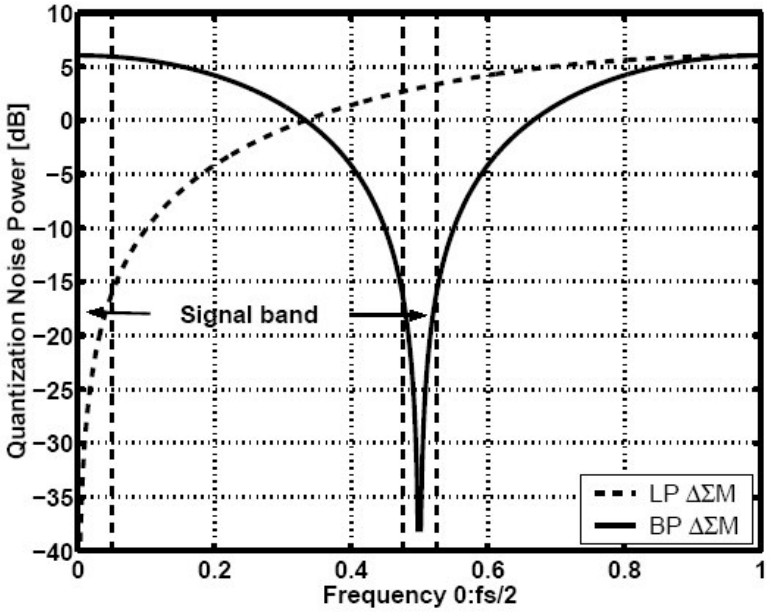


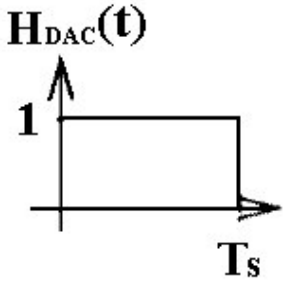
Fig. 9. The noise shaping of lowpass and bandpass ΣΔ modulators.

2.4 Continuous-Time ΣΔ Modulator

The discrete-time bandpass modulator enables the conversion of a bandpass signal with narrow band at the center frequency and makes the circuit implementation easy. However, these modulators cannot operate at higher frequency because the maximum clock is limited by the Opamp bandwidth and the settling time of the circuitry. In a discrete-time modulator, the analog input is converted to a digital signal by a S/H stage, which may limit the linearity and noise floor of the whole system. Also the discrete-time modulator requires an anti-alias filter. By contrast, a continuous-time modulator relaxes the requirements of high-speed Opamp because the signals vary continuously. The sampling occurs after integrator rather than at input as in a discrete-time modulator and therefore the anti-alias filter may be eliminated. Also a continuous-time modulator has less power consumption than the discrete-time counterpart and thus it is suitable for high-speed and low-power applications.

Intuitively, a continuous-time modulator can be obtained by replacing the discrete-time loop filter by a continuous-time one. The question is how to choose loop filter parameter. The key to designing a continuous-time filter is to make the two modulators behave exactly same. If we apply the same input signal to the two modulators and simulate them in time domain, they should generate the same output bits. It means that the input voltages of quantizer at sampling time are equal. The simplest approach is to perform an impulse-invariant transformation. It maps the frequencies linearly from $-\pi/(2T_S)$ to $\pi/(2T_S)$ while other frequencies will be aliased to the transformed band.

A DAC should be defined to do the transformation. A 1-bit DAC with a pulsed output that remains constant over a full period is used in the design. We term it the non-return-zero (*NRZ*) DAC. It's depicted in Fig. 10.



$$h_{DAC}(t) = \begin{cases} 1, 0 \le t < T_s \\ 0, \text{otherwise} \end{cases}$$

$$H_{DAC}(s) = \frac{1-e^{-sT_S/2}}{s}$$

Fig. 10. NRZ DAC pulse.

The impulse-invariant transformation leads to the following condition,

$$Z^{-1}[H(z)] = L^{-1}[H_{DAC}(s) \cdot H(s)]\Big|_{t=nT_s} \tag{2.10}$$

Where $H(z)$ is the transfer function of loop filter in discrete-time modulator, $H(s)$ is the transfer function of loop filter in continuous-time modulator. The condition is expressed in the time domain,

$$\begin{aligned} h(n) &= [h_{DAC}(t) * h(t)]\Big|_{t=nT_S} \\ &= \int_{-\infty}^{\infty} h_{DAC}(\tau)h(t-\tau)d\tau\Big|_{t=nT_S} \end{aligned} \tag{2.11}$$

For a continuous-time loop filter, the transfer function has the form of

$$H(s) = \sum_{k=1}^{N} \frac{a_k}{s - s_k} \tag{2.12}$$

Its impulse response is

$$h(t) = \sum_{k=1}^{N} a_k e^{s_k T_s} \cdot U(t) \tag{2.13}$$

Substituting (2.12) and (2.13) into (2.11) yields

$$\begin{aligned} &\int_{-\infty}^{\infty} h_{DAC}(\tau)h(t-\tau)d\tau \\ &= \begin{cases} 0 & t < 0 \\ \int_0^t h(t-\tau)d\tau & 0 \le t < T_s \\ \int_0^{T_s} h(t-\tau)d\tau & t \ge T_s \end{cases} \\ &= \begin{cases} 0 & t < 0 \\ \sum_{k=1}^{N} \frac{a_k}{s_k} e^{s_k t}(1 - e^{-s_k t}) & 0 \le t < T_s \\ \sum_{k=1}^{N} \frac{a_k}{s_k} e^{s_k t}(1 - e^{-s_k T_s}) & t \ge T_s \end{cases} \end{aligned} \tag{2.14}$$

Hence, the impulse response at the sampling time $t = nT_S$ can be obtained as follows,

$$h(nT_s) = \begin{cases} 0 & t < T_s \\ \sum_{k=1}^{N} \frac{a_k}{s_k} e^{s_k nT_s}(1 - e^{-s_k T_s}) & T_s \le t \end{cases} \tag{2.15}$$

Using the Z-transform, we can derive the equivalent transfer function of the continuous-time loop filter,

$$\begin{aligned} H(z) &= \sum_{n=-\infty}^{\infty} h(n) z^{-n} \\ &= \sum_{n=-\infty}^{\infty} [\sum_{k=1}^{N} \frac{a_k}{s_k} e^{s_k n T_s} (1 - e^{-s_k T_s})] \cdot z^{-n} \\ &= \sum_{k=1}^{N} \frac{a_k}{s_k} (1 - e^{-s_k T_s}) [\sum_{n=-\infty}^{\infty} (e^{s_k T_s} z^{-1})^n] \\ &= \sum_{k=1}^{N} \frac{a_k}{s_k} (1 - e^{-s_k T_s}) \cdot \frac{e^{s_k T_s} z^{-1}}{1 - e^{s_k T_s} z^{-1}} \\ &= \sum_{k=1}^{N} \frac{a_k}{s_k} (e^{s_k T_s} - 1) \cdot \frac{z^{-1}}{1 - e^{s_k T_s} z^{-1}} \end{aligned} \tag{2.16}$$

A continuous-time ΣΔ modulator can be designed by applying the impulse-invariant transformation given in equation (2.16). If we have a discrete-time modulator with a loop filter $H(z)$ that has a particular noise-shaping performance, first we choose a DAC, and use (2.11) to find the transfer function of continuous-time loop filter. In this way, we can build a continuous-time modulator with the same behavior as the discrete-time modulator.

2.5 Some Basic Performance Parameters

The most significant specifications of ΣΔ modulators include dynamic range, signal-to-noise-and-distortion-ratio (*SNDR*) and power consumption.

Signal to noise ratio (*SNR*)

SNR is the ratio of the maximum signal power to noise power in a specified band. In an ideal modulator, the noise power is determined only by quantization noise. However, there are some other noise sources in circuit-level implementation, such as thermal noise and flicker noise of a transistor. For bandpass ΣΔ modulators, flicker noise (low frequency noise) is not a major issue. Also non-linearity is another major noise source. So the signal-to-noise-and-distortion-ration (*SNDR*) is a performance parameter that

designers often keep a close eye on in ΣΔ modulator. It includes any harmonic power caused by distortion. The *SNDR* is usually reported in the same way as the *SNR*.

Dynamic Range (*DR*)

The dynamic range is defined as the ratio of the maximum input signal to the minimum input signal. It is often specified as the resolution of the modulator as an ADC. There is a conversion formula between the *DR* in bit and *DR* in dB.

$$DR(bit) = \frac{DR(dB) - 1.76}{6.02} \tag{2.17}$$

In order to find the *DR* of a modulator, *SNR* is plotted vs. the input amplitude and the input amplitude range that covers $SNR \geq 0$ is the *DR*.

3. Architecture of Continuous-Time Bandpass ΣΔ Modulator

Some continuous-time ΣΔ bandpass modulators that use Gm-C techniques [11] or LC filters [13] have been reported in recent years. Most continuous-time modulators were realized using expensive technologies such as GaAs or Inp technologies to achieve high-speed data conversion. However, it is hard to integrate these modulators on the same chip with digital signal processors (*DSP*), which are realized in standard CMOS technology. To the author's knowledge, attempts in CMOS bandpass ΣΔ modulators using Gm-C techniques are limited to tens of megahertz [14].

In this project, a continuous-time 4^{th}-order bandpass ΣΔ modulator using Gm-C topology is designed and implemented in 0.35 μm CMOS technology. It is clocked at 500 MHz for the direct conversion of narrowband signals (BW=1MHz) at 125 MHz.

3.1 System-Level of Continuous-Time Bandpass ΣΔ Modulator

The block diagram of the proposed continuous-time bandpass ΣΔ modulator with tuning loop is depicted in Fig. 11. The data acquisition card and the *DSP* are the only external

components in the design. A tuning algorithm is implemented in *DSP* and drives the tuning circuits against component tolerances and temperature variations.

Two identical resonators $As/(s^2+\omega_o{}^2)$ are used in the continuous-time modulator. Full controllability is achieved through the use of four *NRZ* DACs, which feed the information back to each node of the resonators. Fig. 12. shows an open loop path from the output of DACs to resonator with the assumption that each integrator is ideal.

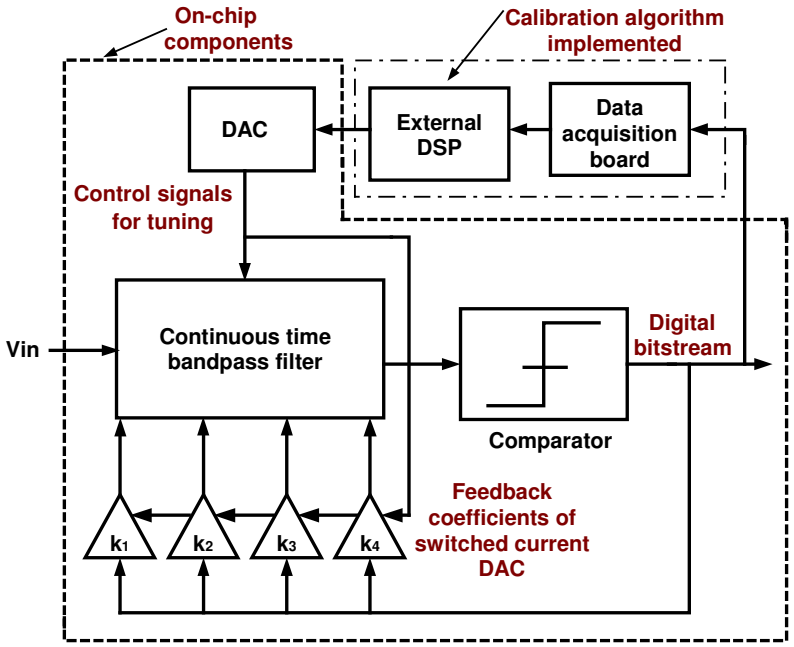


Fig. 11. Block diagram of ΣΔ modulator with the tuning loop.

Using Mason's rule, we can therefore write the open loop transfer function,

$$\frac{V_o}{V_i}(s)=\frac{K_3s^3+(K_1-AK_4)s^2+A(K_3-K_2)s-A^2K_4}{s^4+2As^2+1} \tag{2.18}$$

The above expression shows that four numerator coefficients can be independently controlled by four tunable parameters $K_1 \sim K_4$.

Using the design method discussed in [11], the nominal values of K (DAC's coefficients) are given as follows after high-level simulations on Matlab,

$$\{K_1, K_2, K_3, K_4\} = \{0.3183, 0.3183, 0.8408, 0.75\} \tag{2.19}$$

These coefficients need to be scaled such that the signals at internal nodes do not overload the operational amplifier.

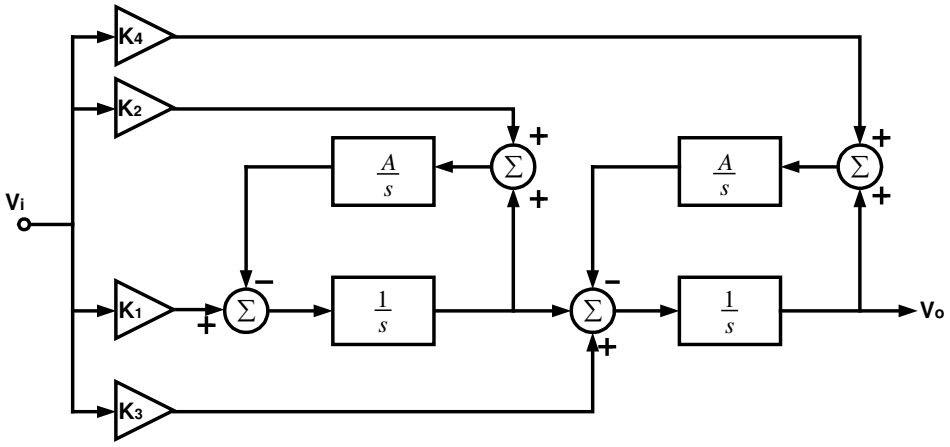


Fig. 12. Block diagram of resonator with feedback coefficients.

Although it is much more complex, a fully differential structure is chosen for the modulator because it reduces the common mode noise and even harmonic distortions, and increases the signal swing. In Fig. 13. the structure of the fully differential continuous-time bandpass ΣΔ modulator is shown. Here OTAs are used to select current as the state variables and get large dynamic range for the modulator. The input voltage is first converted to current by an OTA. Then the current is subtracted from current output of DAC and integrated through a capacitor. The next chapter will describe the design of each building block at the transistor level.

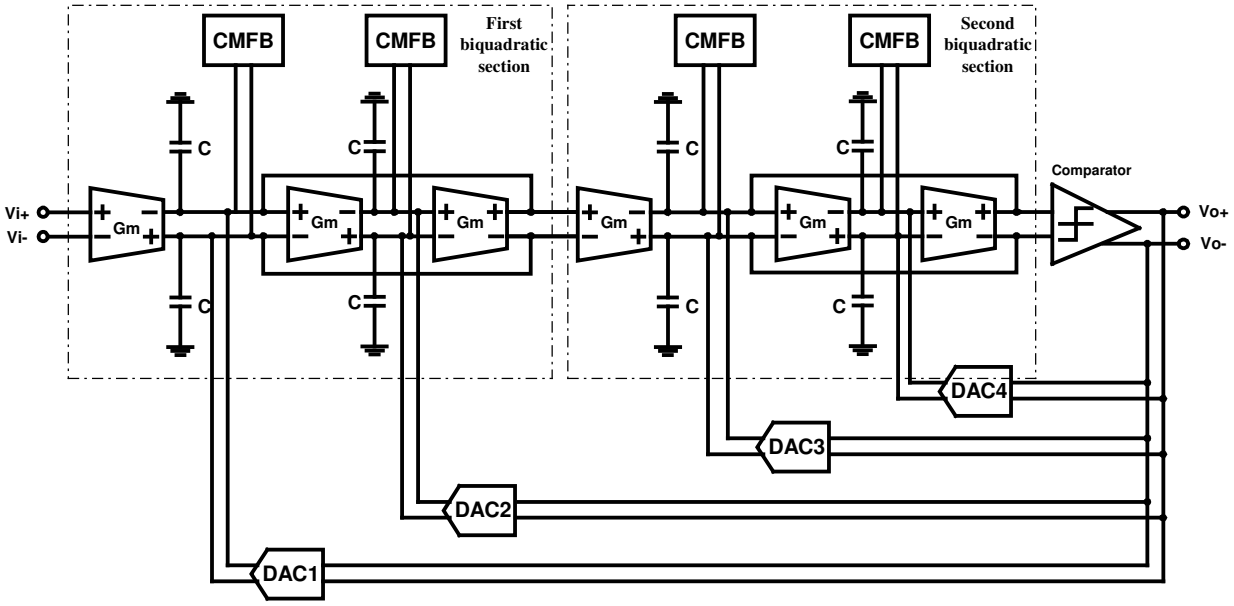


Fig. 13. Proposed 4th -order continuous-time bandpass ΣΔ modulator structure.

3.2 Filter

There are four different structures to realize the filter at the transistor-level: LC, Opamp-RC, OTA-RC and Gm-C. The LC filter implementation at 125 MHz usually requires large values of inductance or capacitance ($125\times10^6 = 1/\sqrt{LC}$), and hence the approach is not suitable for monolithic integration. Even though the Opamp-RC filter has the advantage of high linearity, they cannot be sufficiently fast to meet system requirements; the slew-rate and bandwidth of Opamp make this approach unsuitable for intermediate and high frequency applications. OTA-RC is a combination that uses an Opamp-RC filter at the input stage and Gm-C filter internally. However, its drawbacks are high noise and power consumption. Gm-C filter is a better choice for the high frequency applications compared to the other three structures.

3.3 CMFB

There are two reasons to implement a common-mode feedback circuit: (1) there are high impedance nodes inherently in the Gm-C filter, and the DC voltages at these nodes need to be fixed; (2) The common-mode signals must be suppressed in order to let the differential circuitry work properly. A modified CMFB [15] is used for this high frequency application.

3.4 DAC

Four 1-bit *NRZ* DACs are used in the design and implemented by steering current sources. The addition at each node of resonators is done by using current addition techniques. The DAC should be linear and fast.

3.5 Quantizer

The quantizer is implemented by a clocked-latch-type comparator. In ΣΔ modulators, the comparator is required to work at a high oversampling frequency but the resolution can be as small as 1-bit. The design should be focused on the high-speed operation instead of accuracy for this application.

4. ΣΔ Modulator Implementation Considerations

The above theory describes the functionality of ideal ΣΔ modulators. There are certain considerations for the circuit realization regarding to the non-idealities. Here we will discuss some of them in continuous-time bandpass ΣΔ modulators.

4.1 Circuit Noise

In an ideal modulator, the quantization noise mainly determines the in-band noise floor of the modulator. However in practical circuit implementations, noise is also introduced

by the active elements. As we know, noise due to the input, first integrator and first DAC are not shaped. These noise sources contribute to the noise levels of the modulator. The input OTA's noise density is inversely proportional to the transconductance Gm of the input differential pair. Increasing Gm will reduce the thermal noise, and the penalty is size or/and power consumption. Other noise may come from clock jitter and power supply noise.

To achieve the best performance of modulator, it is common to make the contribution of circuit noise and distortion less than that of the quantization noise, which will preserve the performance of the modulator model mentioned in 2.2 and 2.3.

4.2 Transconductance Nonlinearity

Transconductance nonlinearity introduces harmonic distortions, especially the third harmonic distortion. The harmonics will generate inband noise and degenerate the *SNDR* and *DR*. Since the major contribution of distortion comes from the transistors, transconductances need to be highly linear to have a good performance.

Source degenerated differential pairs are mostly used in the transconductor's input to improve the integrator linearity. Increasing the saturation voltage of the input transistors reduces the distortion. However it will only help to some extent and is only valid for transistors in strong inversion. The suppression of distortion will inevitably come at the cost of power consumption.

4.3 Q-Factor

The ideal modulator has an infinite Q-factor, which means that the gain and output impedance of transconductance amplifier are infinite too. However, it's not practical. A finite Q-factor makes the noise transfer function be flat in the center of signal band instead of sharp dip. For a modulator with high OSR, the effect is more obvious. There is always a minimum Q-factor to have a certain performance. The requirement of Q-factor

is much relaxed as OSR is reduced. Also the Q-factor is related to the signal swing at the internal nodes of the system, which may cause saturation of transistors or instability.

4.4 Component Mismatch and Tolerance

Device mismatch makes the frequency response different from what is designed. For a continuous-time modulator, it is important to know how much relative frequency mismatch can be tolerated. It is known that the transconductor is sensitive to component and temperature variations. A tuning circuitry and calibration scheme are used to get high resolution.

A one-bit quantizer is frequently employed in ΣΔ modulators. It is very simple to build, and a DAC driven by only two levels is inherently linear. In practice, multi-bit quantizers are very attractive and often used to reduce clock jitter sensitivity, improve the modulator resolution and make high-order modulators more stable. In a multi-bit DAC the errors between DAC levels will be directly input-referred and the performance of modulator depends on the DAC matching and is degraded by mismatch.

4.5 Excess Loop Delay

In a continuous-time sigma-delta modulator, the output of quantizer drives feedback DACs, and the outputs of DACs add up internal node voltage/current of filter. Ideally, the outputs of DACs respond immediately to the quantizer clock edge, however, the transistor in DACs and comparator cannot switch instantaneously. The excess loop delay is caused by the fact that the time is not zero from the sampling clock edge to the output changes at the feedback point. With the excess loop delay, the loop transfer function moves away from the desired loop transfer function because the modulator pulse response at the sampling instants is changed. It is imperative to consider the excess loop delay in design, especially in the high-speed application.

The easy way to understand the effect of excess loop delay is to model it by an additional pole and look at the stability of the loop transfer function, which is shown in

Fig. 14. With the pole existing and moving, the phase delay in loop may increase and it implies worse modulator stability, especially if the equivalent pole ω_p is not located at very high frequencies. Also the quantizer gain is not always a constant because it is input signal dependent, and the loop becomes unstable as the quantizer gain increases.

Fig. 14. Model of excess loop delay.

Choosing a right DAC and tunable feedback coefficients can partially solve the problem and improve the performance of modulator. A multi-bit quantizer is somewhat helpful, but a feedback multi-bit DAC is required and a circuitry to reduce the DAC mismatch is not suitable for high-speed design.

4.6 Clock Jitter

The ideal output of the feedback DAC is rectangular current or voltage pulses, and most of the charge transfer occurs at a constant value over a clock period for a continuous-time modulator. Therefore, clock jitter causes a random variation in the pulse widths of DAC and adds a random phase noise to the output bit stream because the feedback signal is added to the CT analog signal. Moreover, the timing uncertainty in the sampling clock causes an amplitude error in the continuous-time signal, as shown in Fig. 15. A sampling of a sinusoidal signal occurs at the point A without clock jitter, however, the time variation due to clock jitter makes the sampling occur at point B, resulting in a magnitude error. Hence a continuous-time ΣΔ modulator is sensitive to clock jitter.

In an *NRZ* modulator, jitter only affects when the sign of output changes. However, in a *RZ* modulator, the pulse has both rising and falling edges during every clock cycle, so jitter problem worsens. *NRZ* feedback DACs are employed in the design instead of RZ to ease the impact of clock jitter.

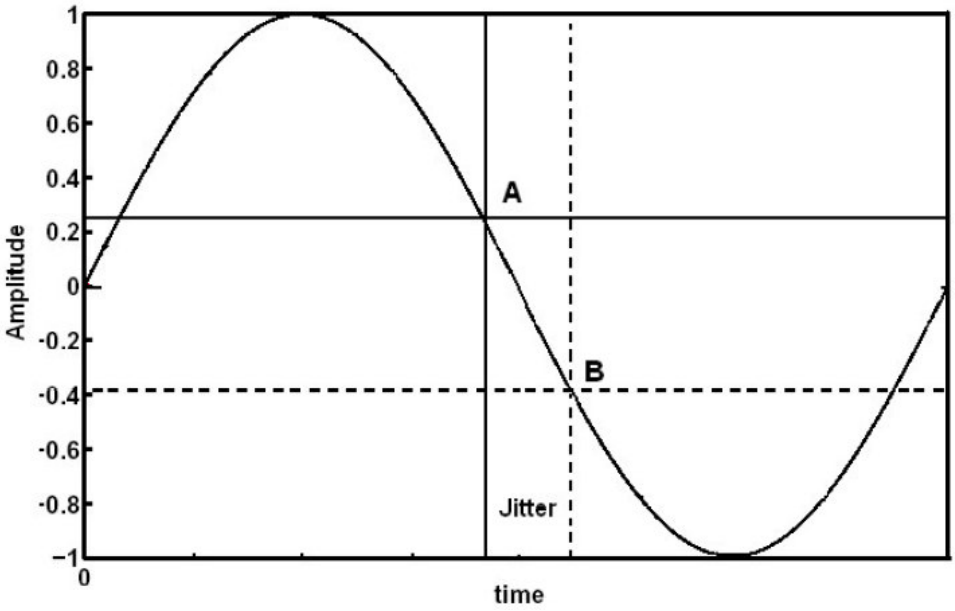


Fig. 15. Amplitude error in the signal sampling due to the clock jitter.

CHAPTER III

CIRCUIT DESIGN AND IMPLEMENTATION

1. Introduction

In previous chapter, the fundamentals of ΣΔ modulators have been discussed. Also the system-level design and architecture of the 4^{th}-order continuous-time bandpass ΣΔ modulator are presented. This chapter will focus on the design of each building block, which includes operational transconductance amplifier (OTA), loop filter, CMFB, DAC and comparator.

2. OTA for Loop Filter

Since the loop filter is implemented by using the Gm-C topology, the OTA is the most critical building block for the performance of the ΣΔ modulator. The main specifications are very high linearity, high tuneablility and high DC-gain.

An input OTA is required to make the signal operate in current mode and to be out of the loop's system. The minimum input of this modulator is determined by the input referred noise seen at the input transconductor, and the maximum input is limited by its linearity because transistors have nonlinear behaviors and introduce harmonic distortions. To a large extent, the *DR* of overall modulator is determined by the input transconductor. The distortion of the other transconductors in the design flow will generate inband noise and also degrade the *SNDR* and *DR* of modulator; nevertheless noise due to the next stages is usually shaped by loop gain. Therefore transconductors need to be highly linear, especially the input transconductor.

To make the notch frequency to a high accuracy (~1%) against the process and temperature variations, it is necessary to have a tunable transconductor in the resonator (we term the transconductor high DC-gain OTA in the thesis to distinguish from the input OTA). Since a tunable transconductor is less linear than a fixed one, a capacitors

bank is used for the coarse tuning and the transconductor is only tunable in a small range to maintain the linearity and accuracy.

A finite Q-factor makes the noise transfer function be flat in the center of signal band instead of sharp dip. The effect is more obvious for a modulator with high OSR. Also the Q-factor is related to the signal swing at the internal nodes of the system, and large signal swing may cause instability. A negative impedance to cancel the positive output impedance of transconductor is implemented in the design, and the Q-factor is tunable as well.

2.1 Specifications of OTAs

The linearity and transconductance are two critical specifications for the input OTA as we mentioned before. High linearity is required for the best *SNDR* of the system. After system simulations on Matlab and by using macromodels, the specifications for the input OTA can be obtained, and listed in table 3.1.

TABLE 3.1
Input OTA specifications

OTA parameters	**Values**
DC-gain	~ 30 dB
$G_{m,eff}$	~2 mA/V
Excess Phase @ 125 MHz	< 2°
IM3 @ 125 MHz, 0.5 Vpp input	-65 dB
Integrated noise (1 MHz BW)	< 100 μV
Power consumption	Minimized

For the high DC-gain OTA, tuneablility and gain are important specifications besides linearity. Tuneablility is required against the process and temperature variations. Large gain is for the high Q requirement and should be tunable as well. Since the OTA operates at high frequency, large transistors are needed. Thus we need to take account of the parasitic capacitance that will be accumulated on the load capacitance. A CMFB is required at each node of resonators, and introduces additional parasitic capacitance. In

the beginning of design, we assume that there is a 2~3pF capacitance at each node of resonators including the parasitic capacitance. The required effective transconductance of high DC-gain OTA can be obtained because the resonator frequency is determined by $G_{m,eff}/C$. Then the system simulations can determine the other parameters. The specifications for high DC-gain OTA are listed in table 3.2.

TABLE 3.2
High DC-gain OTA specifications

OTA parameters	**Values**
$G_{m,eff}$	~2 mA/V
DC-gain	>30 dB
Excess Phase @ 125 MHz	< 2°
IM3 @ 125 MHz, 0.5 Vpp input	-65 dB
Integrated noise (1 MHz BW)	100 μV
Power consumption	Minimized

2.2 Design and Simulation Results of Input OTA

Structure of input OTA

The simplicity and linearity are the essential features of the input OTA intended for the application. Large transconductances are needed for the bandpass resonator operating at 125 MHz, and their implementation usually employs large-dimension transistors and tail-current. However, transistors with large size introduce parasitic poles at lower frequencies. The use of large tail current will also increase the power consumption and further reduce the DC gain of transistors. A general differential pair has a good frequency response due to the absence of low-frequency parasitic poles. The problem of this topology is that the DC gain is very limited. Cascode output stages can boost the gain but introduce parasitic poles at the cascode node. An efficient OTA based on the complementary differential pairs was reported in [16], and is shown Fig. 16.

The OTA uses two differential pairs M1 and M2 as the driving stage, and both differential pairs draw from the same tail current. The effective transconductance increases but the power consumption is not increased. One part of the differential output current comes from N-type pairs M1, and the other from P-type pairs M2. With the help of small-signal transistor model, the effective OTA transconductance is given by,

$$G_m = g_{m1} + g_{m2} \tag{3.1}$$

where g_{m1} and g_{m2} are small-signal transconductances of M1 and M2, respectively.

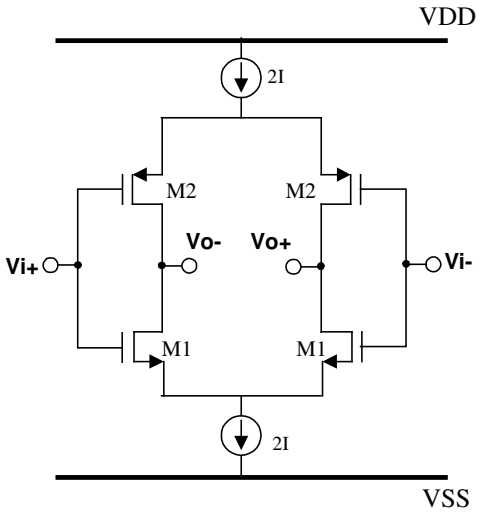


Fig. 16. Complementary differential pairs.

There are several circuit techniques reported with improved linearity of MOS transconductors. Most commonly used linearization methods are nonlinear term cancellation, attenuation and source degeneration [17]. Nonlinear term cancellation is realized by means of optimal algebraic sum of nonlinear term. However the linear range is very restricted and a good cancellation is hard to achieve. In the attenuation technique, the input voltage is reduced or attenuated by several factors in magnitude to improve the linearity. The drawback is that a higher gain is required to compensate the input attenuation, resulting in large area and more power consumption. Compared to the two

techniques, source degeneration is a technique mostly employed. Fig. 17. depicts two possible implementations.

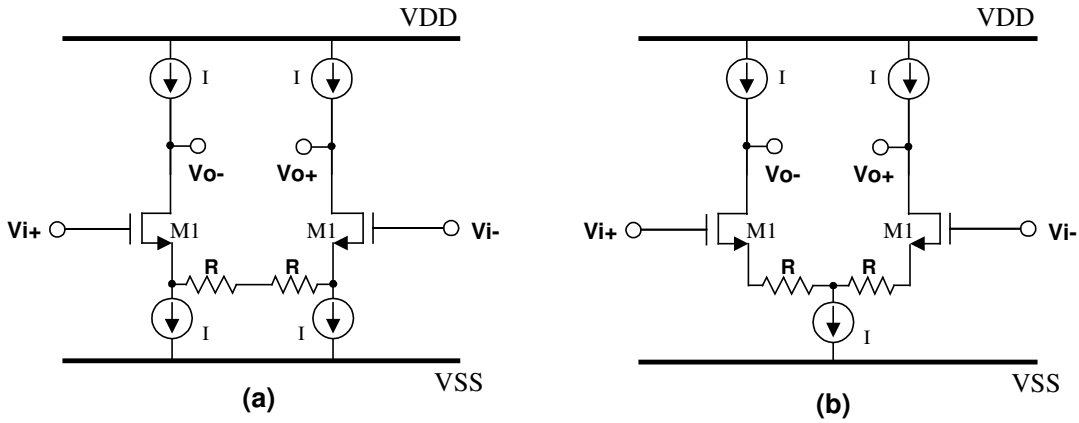


Fig. 17. Linearization techniques using source degeneration.

The difference between the two structures is how the current source is connected. Structure (a) has higher common-mode voltage swing at input. Also the noise contributed by current source is injected to a single output and appears like differential noise at the output node. In structure (b), the noise goes through the two branches evenly, and looks like common-mode noise.

Both of the two structures have the same effective transconductance $g_m/(1+g_mR)$, where g_m is the transconductance of transistor M1. When g_mR is much greater than 1, the effective transconductance is approximated to $1/R$, which means it is linear and does not change with the input signal. It is not practical to implement very large *R* monolithically. A transistor working in triode region is commonly used to implement R.

A structure of linearized complementary differential pairs is proposed in [16], which operates at 200 MHz with HD3 below –44 dB. In [18], a combination of source degeneration and cancellation techniques yields IM3 below –70 dB up to 50 MHz.

The proposed linear OTA combines both techniques reported in [16] and [18], as depicted in Fig. 18. It is based on the complementary differential pairs, which result in

increased effective transonductance and higher power efficiency. Then, source degeneration and cross-couple cancellation are employed to achieve a high linearity. The

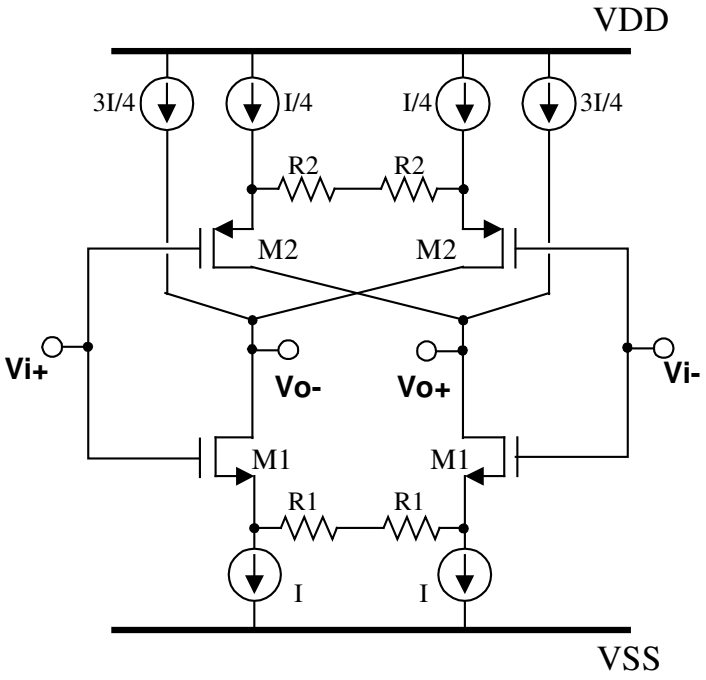


Fig. 18. Linearized input OTA structure.

bias current for M2 is first split, and only a small part of the DC current is used to bias M2, resulting in smaller small-signal transconductance of M2. Then the drains of M2 are crossed to drains of M1 in order to perform the nonlinear term cancellation of two transconductances. One fourth of the DC current is chosen to bias M2 because we do not want to reduce the saturation voltage of M2 too much and thus degrade the linearity. In doing so, the non-linearity cancellation is implemented without any power consumption increase. Also the cancellation technique performs phase compensation. The structure provides a good solution for this high frequency application with high linearity.

Using the first-order transistor small-signal model and neglecting the mobility degradation on the output impedance, the effective transconductance $G_{m,eff}$ of this OTA is given by

$$G_{m,eff} = \frac{g_{m1}}{1+N_n} - \frac{g_{m2}}{1+N_p} \tag{3.2}$$

Where g_{m1} and g_{m2} are small-signal transconductances of transistors M1 and M2, respectively. N_n and N_p are termed as the source degeneration factors, and they are defined as follows,

$$\begin{aligned} N_n &\cong g_{m1}R1 \\ N_p &\cong g_{m2}R2 \end{aligned} \tag{3.3}$$

The output current of OTA is

$$i_o = \frac{g_{m1}}{1+g_{m1}R1} v_i \sqrt{1-[\frac{v_i}{2(1+N_n)v_{dsat,M1}}]^2} - \frac{g_{m2}}{1+g_{m2}R2} v_i \sqrt{1-[\frac{v_i}{2(1+N_p)v_{dsat,M2}}]^2} \tag{3.4}$$

where v_i is the input differential voltage and v_{dsat} is the saturation voltage of transistor.

Using Taylor series, (3.4) can be expanded as follows,

$$i_o = (\frac{g_{m1}}{1+g_{m1}R1} - \frac{g_{m2}}{1+g_{m2}R2})v_i - \frac{1}{8}[\frac{g_{m1}}{(1+g_{m1}R1)^3 v_{dsat,M1}^2} - \frac{g_{m2}}{(1+g_{m2}R2)^3 v_{dsat,M2}^2}]v_i^3 + \cdots \tag{3.5}$$

Note that the even order harmonic distortions are ideally zero due to the symmetry of the fully differential OTA. The total harmonic distortion is mainly determined by the third harmonic distortion (HD3). We may have a complete HD3 cancellation as long as the following condition is met,

$$\frac{g_{m1}}{(1+g_{m1}R1)^3 v_{dsat,M1}^2} = \frac{g_{m2}}{(1+g_{m2}R2)^3 v_{dsat,M2}^2} \tag{3.6}$$

The above equations give us an insight into how to design the OTA meeting the specification of linearity.

The complete input OTA is shown in Fig. 19. Current sources are implemented by transistor M3, M4 and M5. The dimensions of M5 (M6) are three times the size of M4 (M2) to provide M2 the proper bias current and reduce the mismatch. A power supply of ± 1.65 V is used so there is some headroom for the structure.

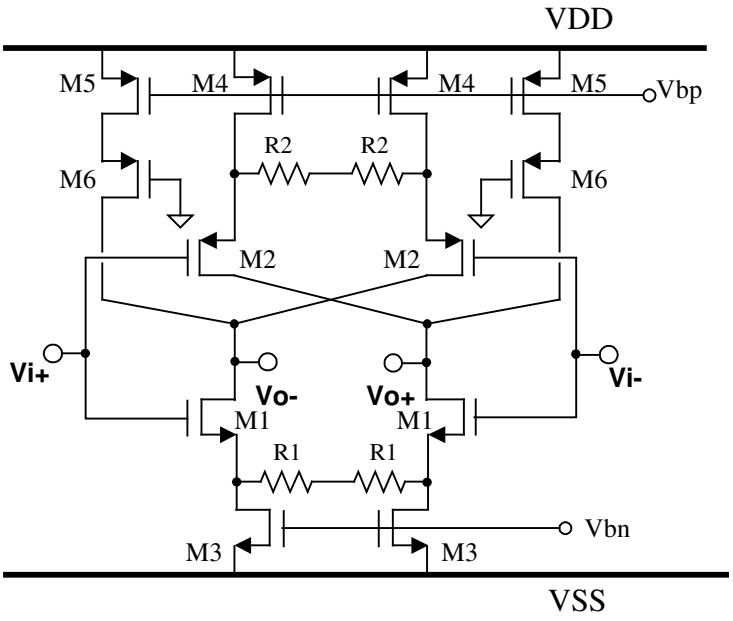


Fig. 19. Complete input OTA structure.

According to Eq. (3.5) the nonlinearity can be reduced by increasing saturation voltages. On the other hand, large saturation voltage limits the input signal swing. The saturation voltages of M1 and M2 are usually kept around 200~300 mV in the design of input OTA [16]. It's also mentioned that the product $N \cdot v_{dsat}$ must be greater than 3 $v_{i,peak}$, and g_{m1} is typically around 3~4 times greater than the effective transconductance to have a harmonic distortion below –50 dB. The main contribution of OTA transconductance comes from transistor M1. Following the analysis above, we choose *N* between 3~4 and the same g_{m1} & g_{m2} as those used in high DC-gain OTA to make the parasitic condition seen at each node similar.

Poly-poly resistors, instead of transistors, are used to implement source degeneration resistors because of small resistance and the nonlinearity of active elements.

Table 3.3 shows that the transistor dimensions, resistor values and bias current of the input OTA.

TABLE 3.3
Transistor dimensions (/Resistor values) and bias conditions

Transistor /Resistor	W/L (μm/μm) /Values (Ω)	Ibias (mA)
M1	76.8/0.4	1.5
M2	60.8/0.4	0.375
M3	100/0.6	1.5
M4	90/0.6	0.375
M5	270/0.6	1.125
M6	182.4/0.4	1.125
R1	245	0
R2	1100	0

Simulation results of the input OTA

The simulation to check effective transconductance and excess phase is performed by the small signal AC analysis. A voltage source is connected to the output of OTA. Fig. 20. shows that the effective transconductance is around 1.75 mA/V at 125 MHz. The excess phase is less than 1 ° at 125 MHz (Fig. 21.).

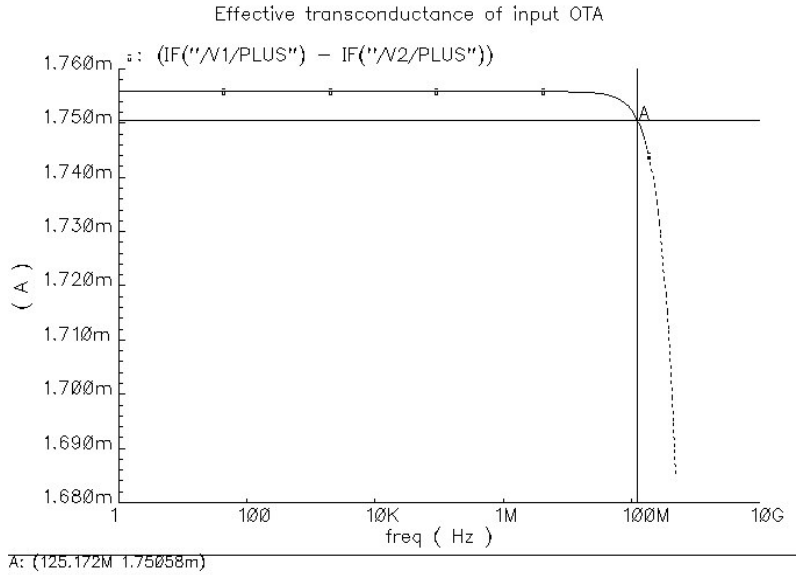


Fig. 20. Effective transconductance of the input OTA.

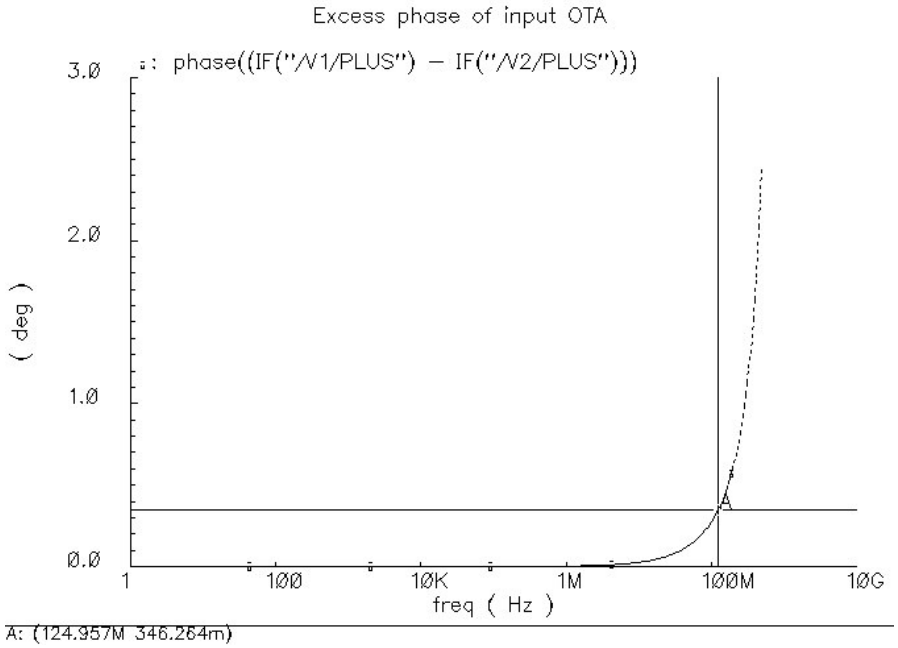


Fig. 21. Excess phase of the input OTA.

The output of the OTA is shunted to ground, and the input is swept from –2 V to 2V. The sweep analysis shows that the transconductance is very much constant for the input range between -1 V to 1V, as shown in Fig. 22.

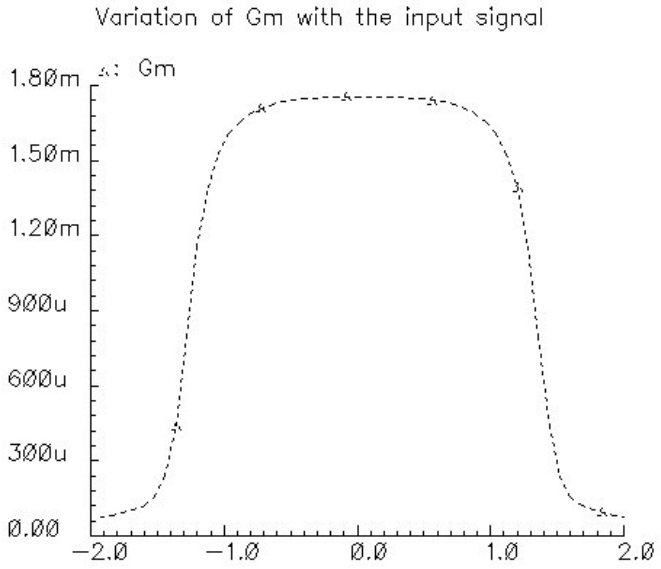


Fig. 22. Variation of Gm with the input signal.

The linearity of the input OTA is characterized by IM3. The output is loaded with a capacitance of 2 pF to make the unity gain frequency at 125 MHz. Two tones with 0.25 V (amplitude) at 125 MHz and 125.5 MHz are applied to the input, and IM3 distortion is obtained by performing PSS analysis on Cadence. As Fig. 23. shows, the IM3 is below –74 dB.

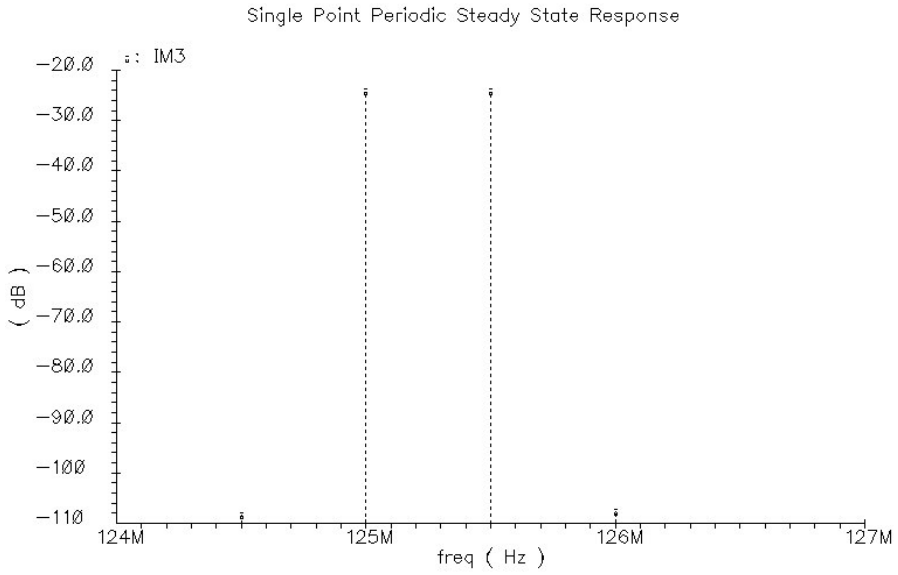


Fig. 23. IM3 distortion of the input OTA.

The simulation results for the input OTA is listed in the Table 3.4.

TABLE 3.4
Summary of input OTA simulation results

OTA parameters	**Simulation results**
Effective transconductance $G_{m,eff}$	1.75 mA/V
Excess Phase @ 125 MHz	0.4 °
IM3 @ 125 MHz, 0.5 Vpp input	-74 dB
Integrated noise (1 MHz BW)	10 μV
Power consumption	9.96 mW

2.3 Structure of the High DC-Gain OTA

Structure of the high DC-gain OTA

Fig. 24. depicts the proposed structure for the high DC-gain OTA.

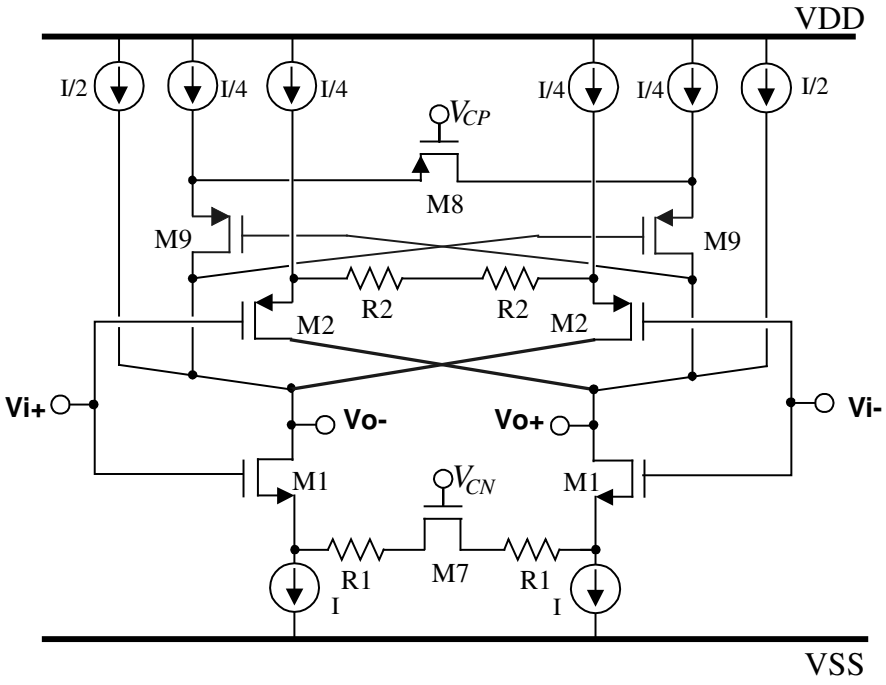


Fig. 24. Proposed high DC-gain OTA.

The structure of high DC-gain OTA is based on the input OTA because it is compliant with both linearity and frequency. The high DC-gain OTA is different from the input OTA where Gm and Q of the high DC-gain OTA are required to be tunable. As we know, the resonator frequency is determined by Gm and capacitance, so a capacitors bank controlled by three digital bits is employed to have a coarse tuning (± 30%) against the process and temperature variation, and the fine tuning is performed by the tunable Gm to maintain a precision of 1%. High Q is required to have a better noise attenuation.

To implement a tunable Gm, a triode-region transistor M7 is inserted between two source-degeneration resistors. By controlling the gate voltage V_{CN} of M7, the effective transconductance of the OTA can be tuned up to ±5 % without linearity degradation. Negative impedance compensation technique is used in this OTA to increase its output impedance and gain. In the input OTA (Fig. 16.), both M5 and M6 just work as DC current bias and do not process any AC signal. To make use of that current, we split M5 and M6. One part consists of M9, which is connected in a positive feedback to implement the negative impedance, and the other part provides DC current as M5 and M6 do. In this way, the negative impedance is implemented without increasing power consumption nor additional active elements that increase the OTA's noise. M8 works in triode region, and operates as a source degeneration resistor to make the negative resistance tunable and keep a good linearity.

The effective small signal transconductance of this high DC-gain OTA is approximately given by,

$$G_{m,eff} = \frac{g_{m1}}{1+N_n} - \frac{g_{m2}}{1+N_p} \tag{3.7}$$

The source degeneration factors N_n and N_p are defined as follows,

$$\begin{aligned} N_n &\cong g_{m1}[R1 + \frac{1}{2\mu_n C_{ox}(\frac{W}{L})_{M7}(V_{GS\_M7} - V_{TN})}] \\ N_p &\cong g_{m2}R2 \end{aligned} \tag{3.8}$$

where μ_n and C_{ox} are the mobility of the carriers in the channel and the gate-source capacitance per square, respectively. V_{TN} is the threshold voltage for N-type transistor.

The negative impedance is,

$$R_{neg} = \frac{1}{g_{m9}}[1 + \frac{1}{2\mu_p C_{ox}(\frac{W}{L})_{M8}(V_{GS\_M8} - V_{TP})}] \tag{3.9}$$

where V_{TP} is the threshold voltage for P-type transistor.

The complete high DC-gain OTA is depicted in Fig. 25.

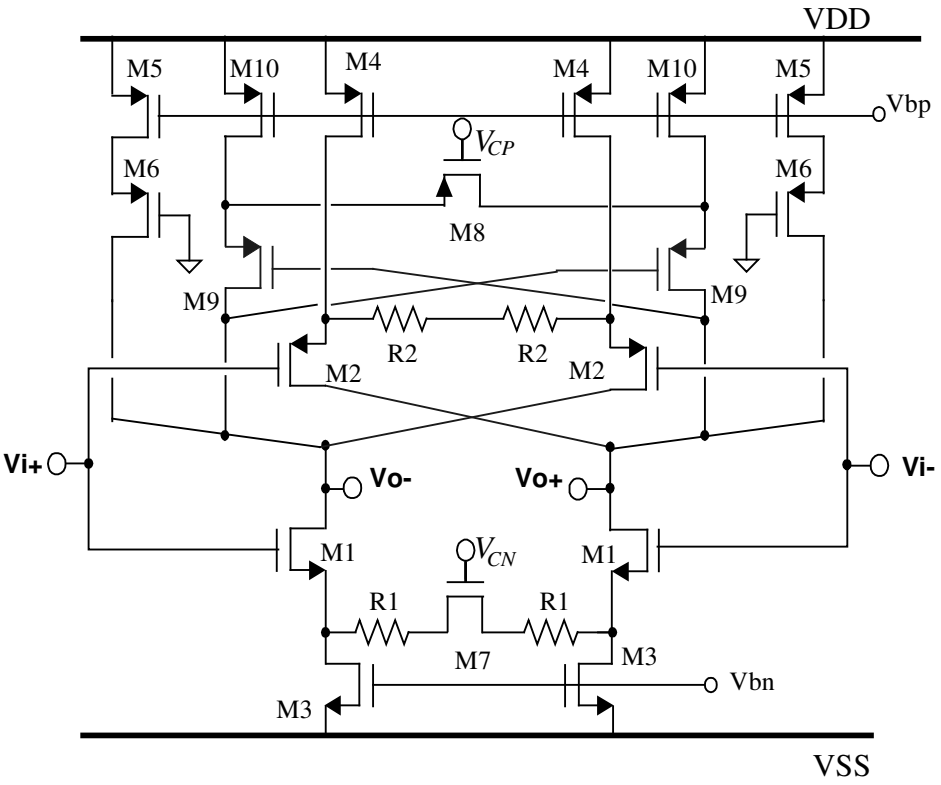


Fig. 25. Complete high DC-gain OTA.

The output impedance is given by,

$$R_o = 1/(\frac{1}{R_{pos}} - \frac{1}{R_{neg}}) \tag{3.10}$$

where R_{pos} is approximated as,

$$R_{pos} = [g_{m2} r_{o2} (R2 // r_{o4})] // g_{m6} r_{o6} r_{o5} // [g_{m1} r_{o1} (R1 + \frac{1}{2\mu_p C_{ox} (W/L)_{M7} (V_{GS\_M7} - V_{TP})}) // r_{o3}] \quad (3.11)$$

and the DC-gain of the OTA is,

$$A = G_{m,eff} R_o \quad (3.12)$$

The ratio of current through M4, M10 and M5 is 1:1:2, therefore we keep the dimension ratio of these transistors is also 1:1:2. Table 3.5 shows that the transistor dimensions, resistor values and bias current of high DC-gain OTA.

TABLE 3.5
Transistor dimensions (/Resistor values) and bias conditions
of high DC-gain OTA

Transistor /Resistor	W/L (μm/μm) /Values (Ω)	Ibias (mA)
M1	76.8/0.4	1.5
M2	60.8/0.4	0.375
M3	100/0.6	1.5
M4	90/0.6	0.375
M5	180/0.6	0.75
M6	121.6/0.4	0.75
M7	86.4/0.4	0
M8	1.5/0.4	0
M9	60.8/0.4	0.375
M10	90/0.6	0.375
R1	425	0
R2	140	0

Simulation results of the high DC-gain OTA

The simulation results of AC analysis are shown in Fig. 26. and 27. with the output of the OTA shunted to ground. The small signal transconductance of the OTA is 1.97 mA/V and the excess phase is less than 0.5 ° at 125 MHz.

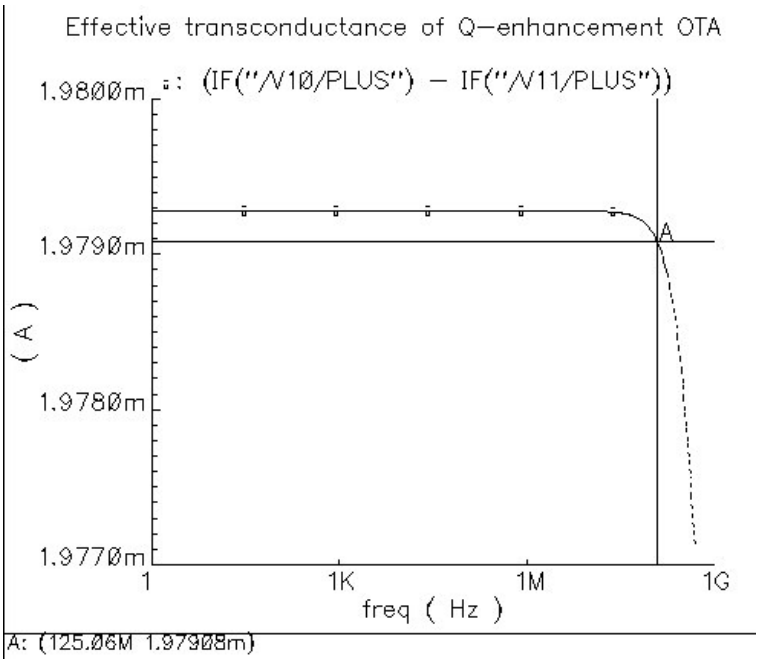


Fig. 26. Effective transconductance of the high DC-gain OTA.

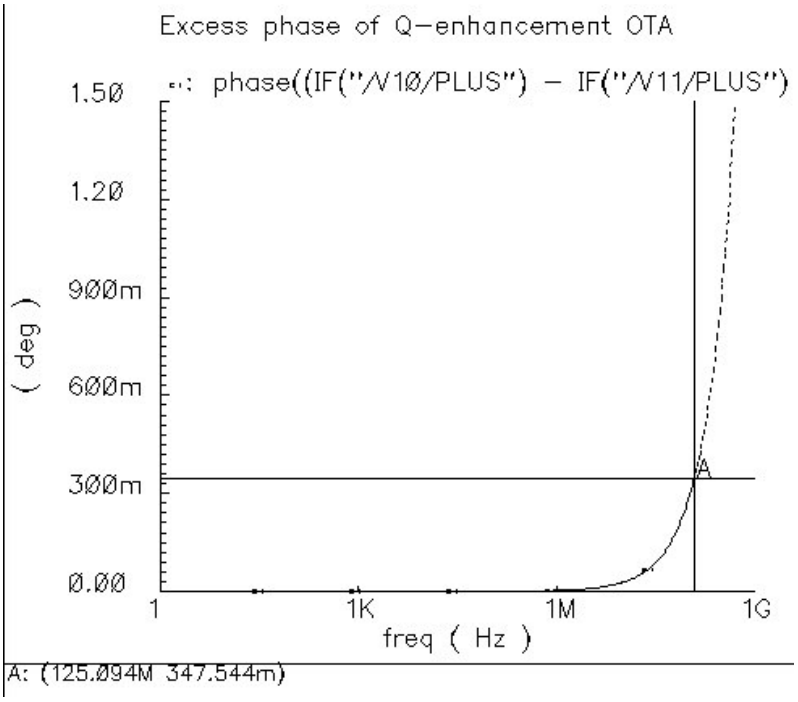


Fig. 27. Excess phase of the high DC-gain OTA.

The output of this OTA is shunted to ground, and the input is swept from –1.2 V to 1.2 V. The sweep analysis shows that the transconductance of the high DC-gain OTA is stable for the input variation up to ±0.5 V, as shown in Fig. 28.

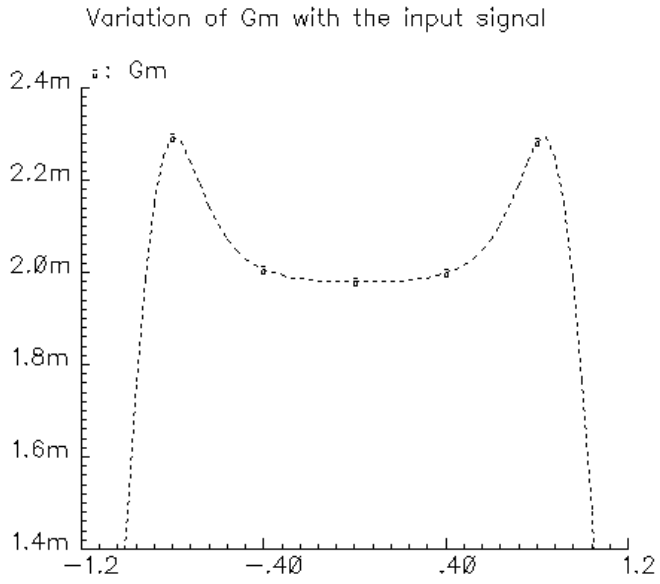


Fig. 28. Variation of Gm with differential input signal.

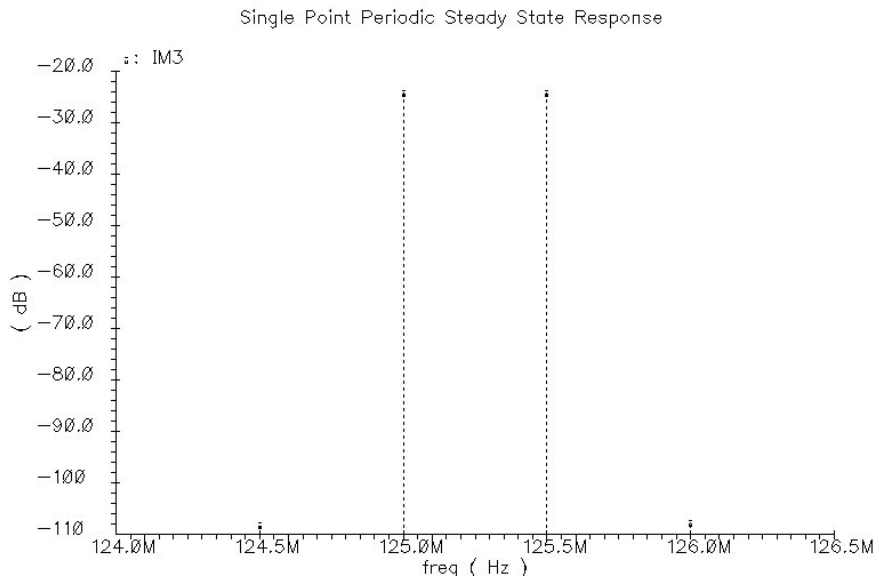


Fig. 29. IM3 distortion of the high DC-gain OTA.

The output is loaded with a capacitance of 2.45 pF to make the unity gain frequency at 125 MHz. Two tones with 0.25 V (amplitude) at 125 MHz and 125.5 MHz are applied to the input, and the IM3 distortion is obtained by performing PPS analysis on Cadence. As Fig. 29. shows, the IM3 is below –84 dB.

Table 3.6 summarizes the simulation results of high DC-gain OTA.

TABLE 3.6
Summary of high DC-gain OTA simulation results

OTA parameters	**Simulation results**
DC-gain	>30 dB
Effective transconductance $G_{m,eff}$	1.98 mA/V
Excess Phase @ 125 MHz	0.35 °
IM3 @ 125 MHz, 0.5 Vpp input	-84 dB
Integrated noise (1 MHz BW)	10.5 μV
Power consumption	9.96 mW

3. Loop Filter

A Gm-C bandpass filter is designed and discussed in this section. It is implemented using the OTA cells aforementioned.

3.1 Basic Gm-C Integrator and Biquadratic Cell

A Gm-C integrator is a basic unite circuit, which is obtained by loading a capacitance at the transconductor output. Fig. 30. depicts an integrator.

The circuit realizes the transfer function,

$$\frac{V_o}{V_{in+} - V_{in-}} = \frac{g_m}{SC} \tag{3.13}$$

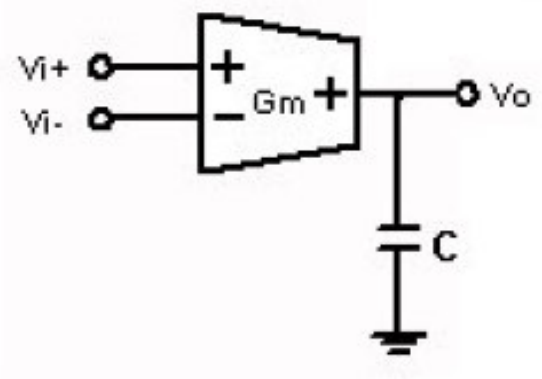


Fig. 30. Integrator using Gm-C topology.

If both the finite output impedance and parasitic capacitance of a transconductor are considered, Eq. (3.13) becomes,

$$\frac{V_o}{V_{in+}-V_{in-}} = \frac{g_m}{S(C+C_o)+g_o} \tag{3.14}$$

where g_o and C_o are the output conductance and parasitic capacitance of the transconductor, respectively. As we see, the integrator realized by Gm-C is lossy.

A lossless biquadratic section, which is a resonator, is depicted in Fig. 31. G_{m1} converts the input voltage into current; G_{m2} and G_{m3} together with a capacitor C_2 form a gyrator that emulate the effect of an inductor. The value of the equivalent inductor is,

$$L = \frac{C_2}{g_{m2}g_{m3}} \tag{3.15}$$

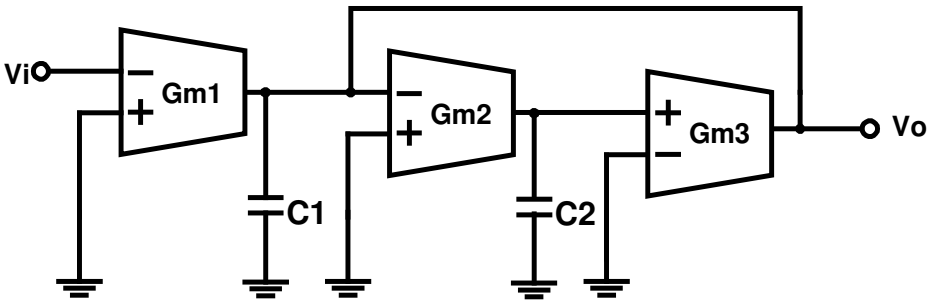


Fig. 31. Single-ended Gm-C realization of a lossless resonator.

The transfer function of the ideal resonator can be written as,

$$\frac{V_o}{V_i} = -\frac{g_{m1}}{sC_1 + \frac{g_{m2}g_{m3}}{sC_2}} = -\frac{sg_{m1}/C_1}{s^2 + g_{m2}g_{m3}/(C_1C_2)} \tag{3.16}$$

Considering the parasitic capacitors at each node and assuming that each transconductor has same input and output impedance and parasitic capacitance, we can obtain the capacitive impedances in Eq. (3.16) as follows,

$$\begin{aligned} C_1 &\rightarrow (C_1 + 2C_o + C_i) + 2g_o = C_{eff1} + 2g_o \\ C_2 &\rightarrow (C_2 + C_o + C_i) + g_o = C_{eff2} + g_o \end{aligned} \tag{3.17}$$

Substituting Eq. (3.16) with Eq. (3.17), then we have,

$$\frac{V_o}{V_i} = -\frac{g_{m1}}{sC_{eff1} + 2g_o + \frac{g_{m2}g_{m3}}{sC_{eff2} + g_o}} = -\frac{g_{m1}(sC_{eff2} + g_o)}{s^2C_{eff1}C_{eff2} + s(C_{eff1} + 2C_{eff2})g_o + (2g_o^2 + g_{m2}g_{m3})} \tag{3.18}$$

As the Eq. (3.18) shows, if the parasitic capacitances and finite output impedance are accounted, the transfer function changes. The quality factor is not infinite any more. The center frequency of resonator is not determined only by the transconductance and load capacitance, but also affected by OTA's output impedance.

3.2 Structure of Fourth-Order Resonator

Fully differential structure is used to implement the bandpass loop filter because of its good common-mode noise rejection, distortion performance and double output swing. Fig. 32. shows the typical structure of the fourth-order resonator by using Gm-C topology.

In ideal case, the transfer function of the resonator is given by,

$$\frac{V_o}{V_i} = \frac{(sg_{m1}/C)^2}{[s^2 + (\frac{g_{m2}}{C})^2]^2} \tag{3.19}$$

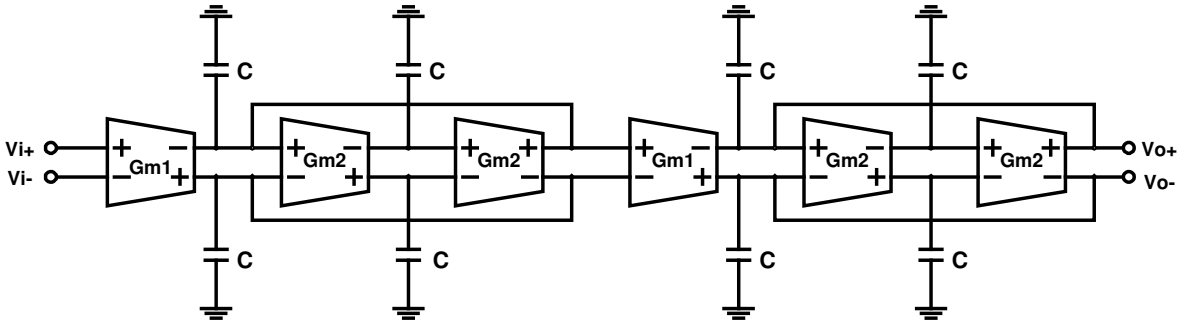


Fig. 32. 4th-order resonator.

The center frequency of this resonator is determined by g_{m2} / C.

Capacitor banks controlled by 3-bit digital signal are implemented in this resonator to have a coarse tuning (± 30%) on the resonator's center frequency. G_{m1} is implemented by the input OTA, and G_{m2} will be replaced by the high DC-gain OTA.

3.3 Simulation Results of Resonator

The frequency response simulation result of this resonator is shown in Fig. 33. The center frequency is 125 MHz, and the peak gain is 68 dB. The –3 dB bandwidth is 300 KHz and hence Q-factor is about 400. The total current of the filter is 42 mA at 3.3 V power supply. The input equivalent noise density is $45.7nV/\sqrt{Hz}$ or the equivalent input noise of this resonator is $45.7\mu V$ for a bandwidth of 1MHz.

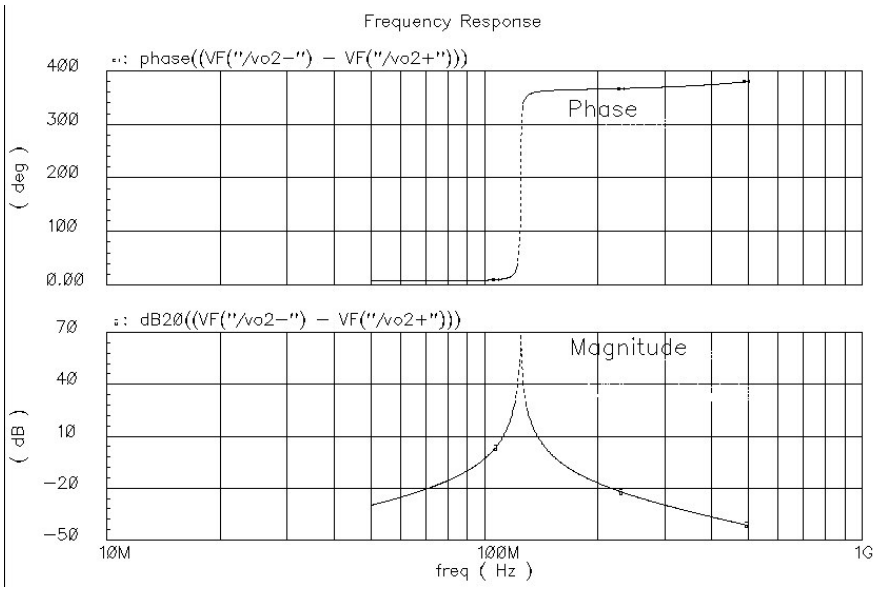


Fig. 33. Frequency response of the resonator.

The PSS simulation is performed with a unit-gain resonator, which is realized by connecting a linear resistor to the output of each G_{m1}. Fig. 34. shows that IM3 at the output of the first biquadratic section is below –70 dB for two-tone up to 0.25 Vpp at 125 MHz and 125.5 MHz, respectively, and IM3 at the output of the resonator is below –66 dB with the same input.

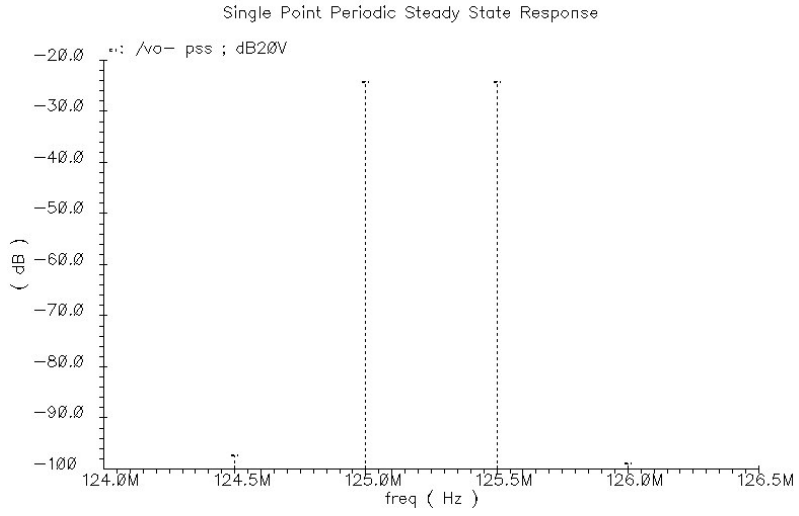


Fig. 34.a. IM3 at the output of the first biquadratic section.

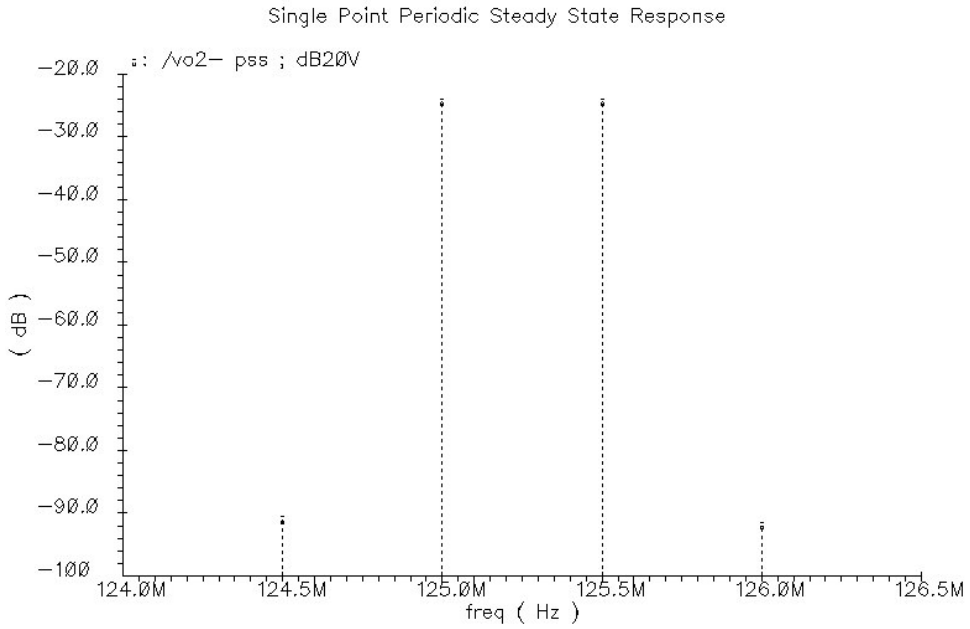


Fig. 34.b. IM3 at the output of the resonator.

Table 3.7 summarizes the simulation results of this resonator. The power consumption includes the CMFB loop.

TABLE 3.7
Summary of 4th-order filter simulation results

Resonator parameters		**Simulation results**
Center frequency		125 MHz
Gain at center frequency		68 dB
-3 dB bandwidth		300 KHz
IM3 @ 125 MHz, 0.5 Vpp input	The first biquadatic section	-70 dB
	The resonator	-66 dB
Integrated noise		45.7 μV
Power consumption		140 mW

4. Common-Mode Feedback (CMFB) Circuit

4.1 Structure of CMFB

A CMFB circuit is necessary if the fully differential circuits are used. A conceptual topology of the CMFB circuit is depicted in Fig. 35. The common-mode signal of differential circuitry is sensed by the common-mode detector, and then compared to a reference voltage V_{ref} . After the error is generated and amplified, a control signal forces the CM level of differential circuitry to a predetermined value.

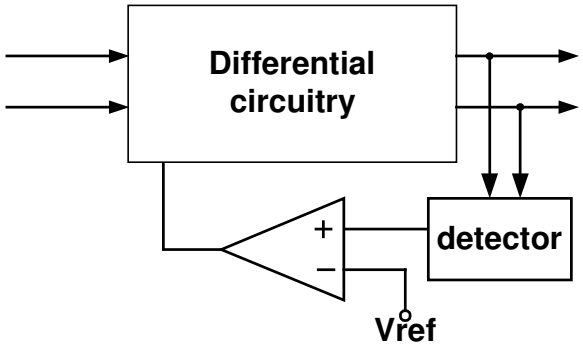


Fig. 35. Conceptual topology of CMFB circuit.

A CMFB circuit should meet the flowing requirements,

1. The DC gain of a CMFB loop should be large enough to control the CM signal.
2. The Gain Bandwidth product (GBW) of a CMFB should be at least equal to GBW of differential loop. Otherwise, the system may not operate in a fully balanced system and the common-mode signals at the filter's center frequency may not be attenuated.
3. A CMFB should only act on the CM signals and not affect the differential signals.

For high-frequency applications where the parasitic capacitors are comparable to load capacitors, it is hard to determine the tradeoff between large GBW and good phase margin. Large GBW is required to reject the high-frequency common-mode noise, but may cause potential stability issues.

A modified CMFB [16] is employed in the design, and depicted in Fig. 36.

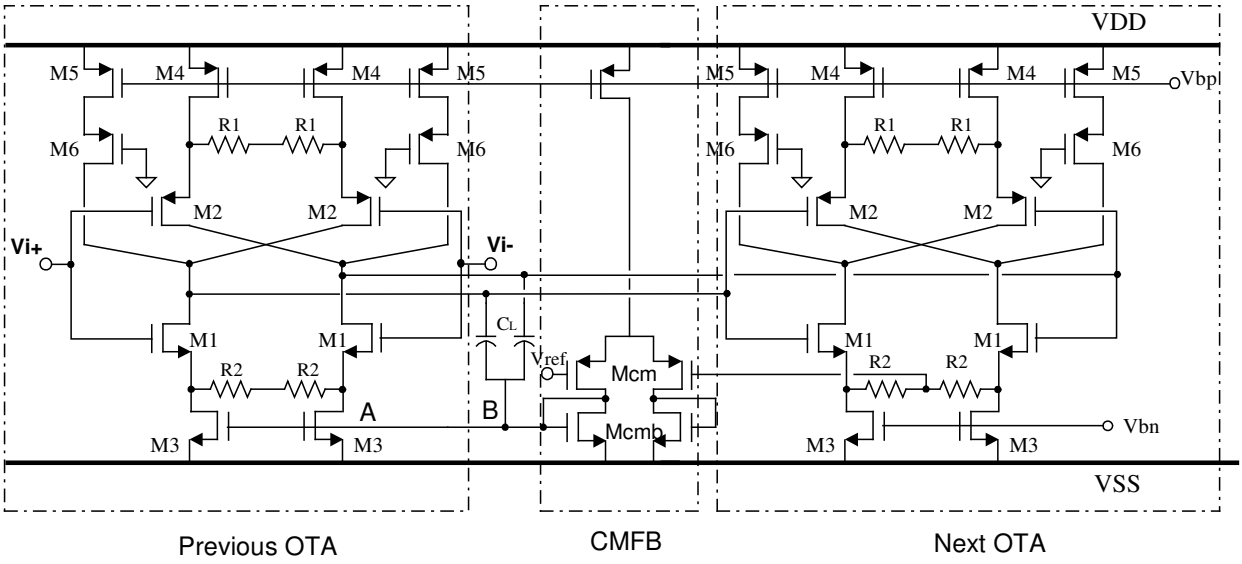


Fig. 36. CMFB loop structure.

The Common-mode voltage of output signals is sensed at the node between two resistors R2. Load capacitors C_L are connected to the diode-connected transistor Mcmb (point B) instead of ground so that the high-frequency signals can be shorted. A high-frequency left hand plain zero due to C_L and Mcmb improves the phase margin and stability.

As Fig. 37. shows, CMFB circuit is implemented at every node of the 4th order resonator.

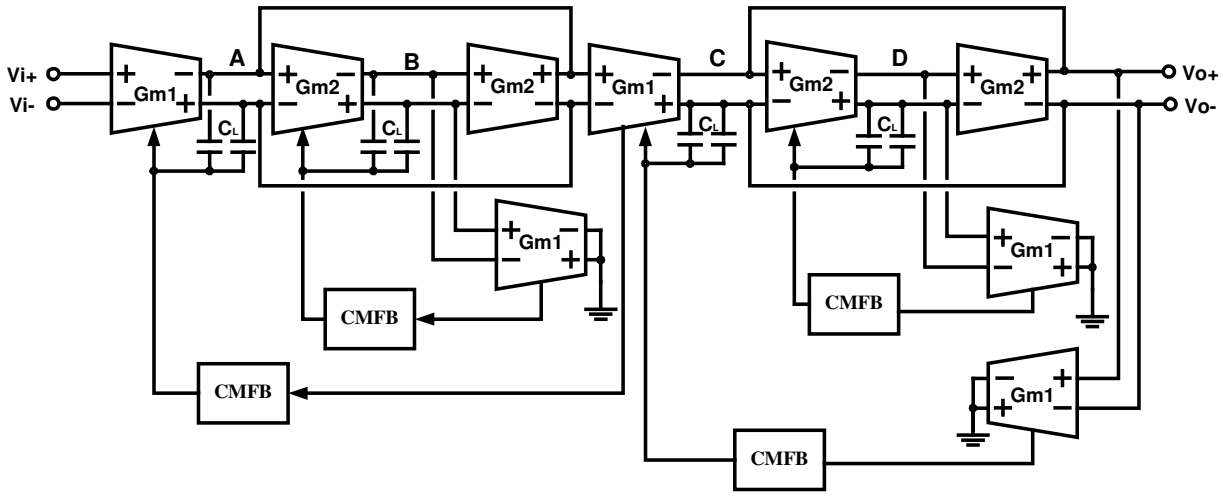


Fig. 37. Resonator with CMFB circuit.

To perform the control on the capacitor bank by three digital bits, it's necessary to make the parasitic capacitors seen at A, B, C and D node as similar as possible, G_{m1}, which is connected to node B, C and D accordingly, is functioned as dummy transconductor and also common-mode signal detector for the output at node B, C and D.

4.2 Simulation Results of CMFB

The phase margin and step-response of the common-mode loop are verified by AC and transient simulations. The frequency response is performed to a standalone OTA with a CMFB loop. A large inductor is placed between node A and B and an input is applied at node A, as shown in Fig. 38. Fig. 39. depicts that the gain bandwidth product (GBW) of CMFB circuit is 160 MHz, and the phase margin is 58 °. The DC-gain of the CMFB loop is 29 dB.

In order to test the step response of CMFB loop within a biquadratic cell and check the stability, a common-mode current pulse of 100 μA is injected to the output of the resonator and the input of filter is shorted to ground, as shown in Fig. 40.

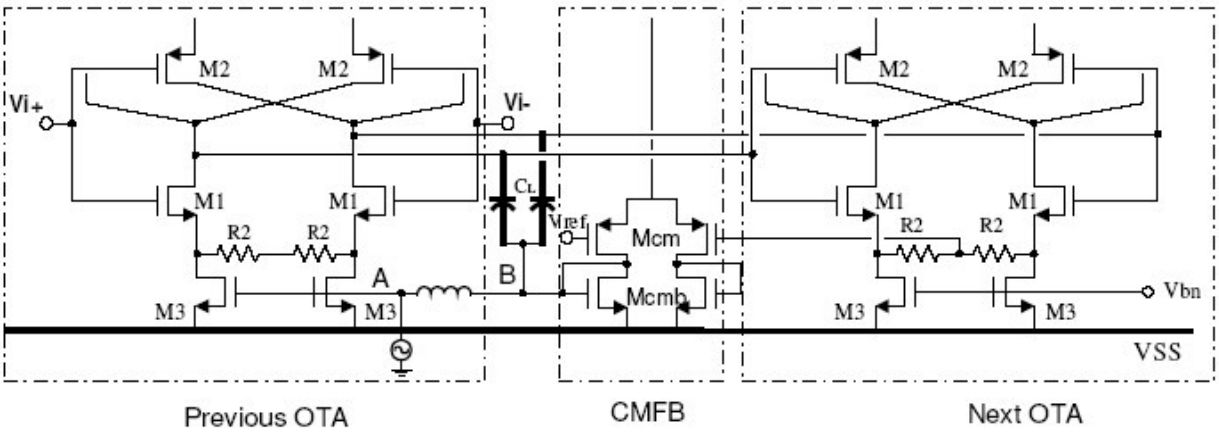


Fig. 38. CMFB AC testing circuit.

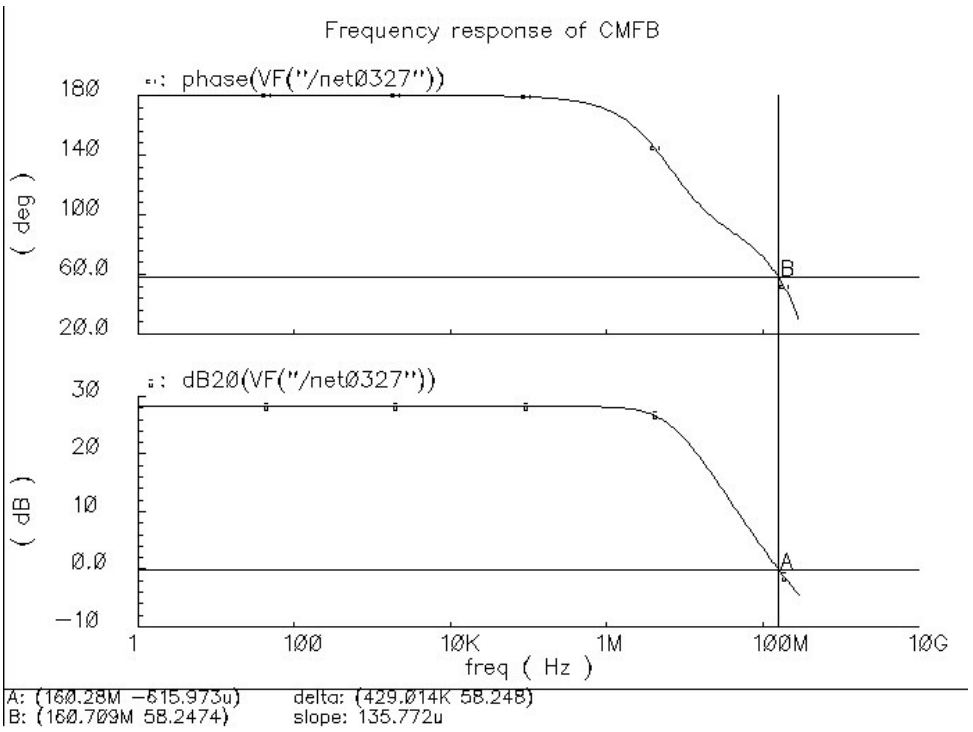


Fig. 39. Frequency response of CMFB circuit.

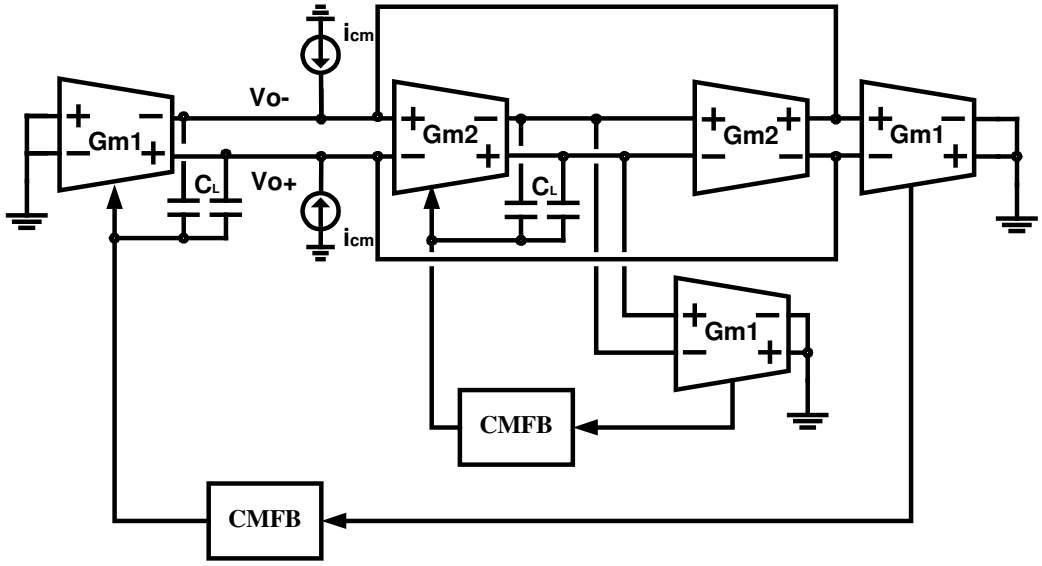


Fig. 40. CMFB step-response testing.

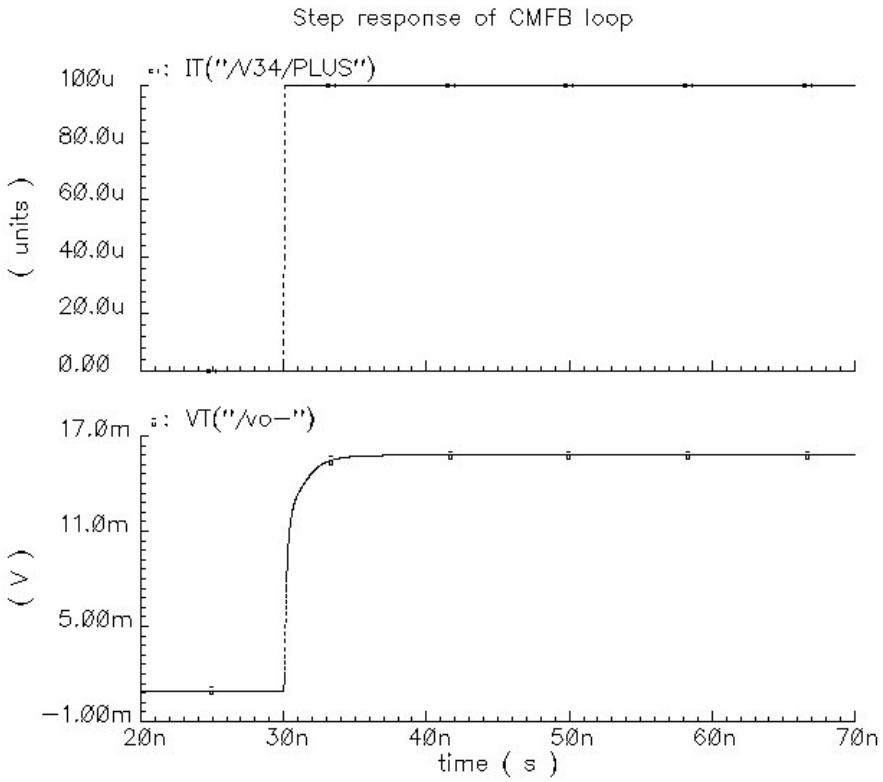


Fig. 41. Step response of CMFB loop.

Fig. 41. shows that the 1% settling-time of the CMFB loop is around 7 nsecs. The common-mode current applied is 100 µA, and a common-mode voltage around 15mV is generated. Hence we can conclude that the transconductance of CMFB loop is about 6 mA/V.

Table 3.8 lists the simulated results of CMFB loop as follows,

TABLE 3.8
Summary of CMFB loop simulation results

Resonator parameters		**Simulation results**
OTA	DC-gain	29 dB
	GBW	160 MHz
	Phase Margin	58 °
Biquads	1% Settling time	7 nsecs

5. Feedback DAC

5.1 Structure of DAC

In the bandpass ΣΔ modulator, four 1-bit *NRZ* DACs are used to feed the output bit-stream of the modulator back to the resonator.

The structure of DAC is an ordinary differential pair, shown in Fig. 42. The input is digital and therefore the differential pair operates as switches. Transistor M3 serves as a current source that provides a right feedback current to the resonator. Both transistor M1 and M2 operate as switches. The current from M3 goes completely through M1 or M2 according to the digital input.

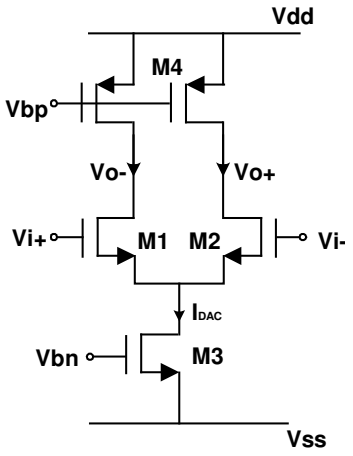


Fig. 42. Schematic of 1-bit DAC.

N-type transistor is used as the driver to make the switch fast enough. Also M1 and M2 operate in the deep-saturation region. The saturation voltage of M1 and M2 is chosen according to the following condition,

$$\sqrt{2}V_{dsat} > \frac{I}{C}T_{CLK} \tag{3.20}$$

The current provided by every DAC must be selected so as to give the right noise-shaping characteristic and node voltage in the resonator. It can be determined by

nominal feedback coefficients K (see Ⅱ.3.1). The DACs contribute to the current through capacitors that are connected to bandpass and lowpass nodes of resonators. Therefore it is required to use the proper bias current to avoid large currents that could overload the resonator.

The transistor dimension and bias current of the four DACs can be found in table 3.9.

TABLE 3.9
Transistor dimension and bias current of DACs

	DAC1 & DAC2	DAC3	DAC4
I_{DAC} (μA)	200	210	187.5
$V_{dsat,M1}$ (V)	0.115	0.116	0.118
M1,M2	35.2/0.4	36/0.4	32/0.4
M3	32/0.8	32/0.8	30.4/0.8
M4	33.6/0.4	33.6/0.4	30/0.4

5.2 CMFB of DAC

The output of DAC is directly connected to the resonator, and is a high-impedance node. A CMFB circuit, as shown in Fig. 43., is required to control the common-mode voltage

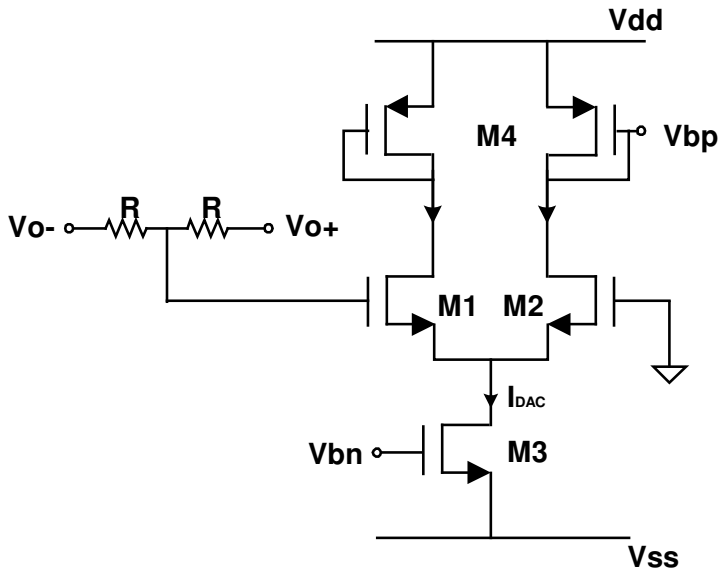


Fig. 43. CMFB circuit for DAC.

at the output of DAC and to keep it around 0 V, even though there are CMFB circuits for the resonator. The two resistors R average and detect the common-mode signal of the DAC output. The differential pairs M1 M2 compare the common-mode voltage with reference voltage (0V here), and transistors M4, which are diode-connected, mirror the error current to bias current of DAC and adjust DAC to have a common-mode signal at 0V.

The common-mode detector resistors with small value will decrease the gain and Q-factor of resonator. However, large resistors occupy more area and introduce more parasitic capacitance. Resistors of 20 KΩ are used in this CMFB circuit, compared with the output impedance of OTA around 10 KΩ.

6. Comparator

6.1 Structure of Comparator

The comparator is one of the most critical blocks for the high-speed operation. It compares two signals and outputs a high or low level. A latched-type comparator is implemented in the design. The high-speed comparator has one stage of preamplification and three track and latch stages, as shown in Fig. 44. The track and latch stages provide the one clock delay, which is required for the ΣΔ modulator.

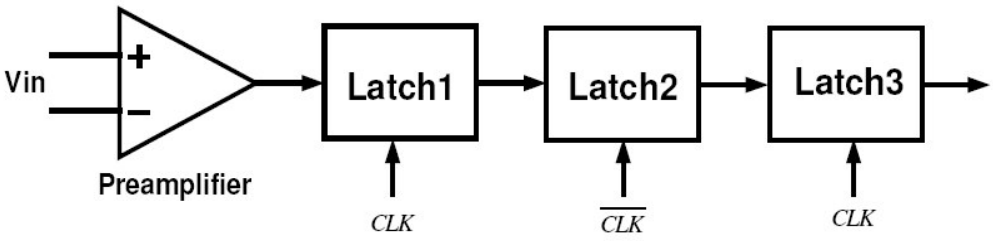


Fig. 44. The latched-type comparator

The preamplifier is used to increase the resolution and to eliminate charge transfer from the track and latch stage into filter's output. Fig. 45. depicts the circuit. It is a simple differential amplifier based on the complementary differential pairs. Resistors at the output of the amplifier are used to fix the common-mode signal at the high impedance nodes.

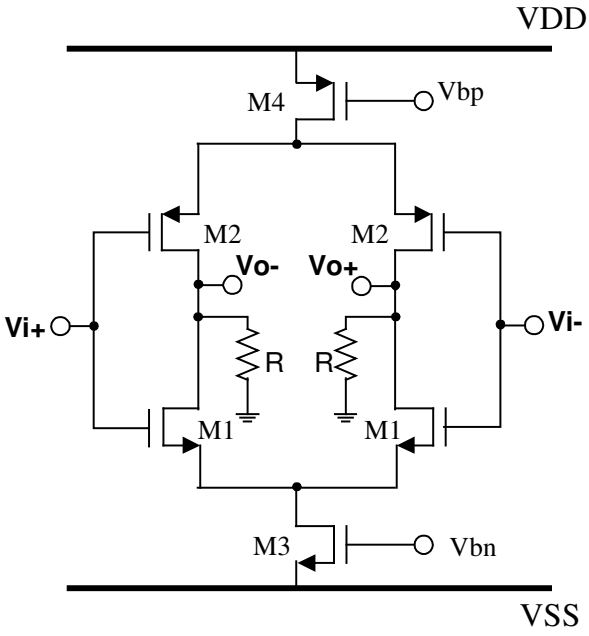


Fig. 45. Preamplifier circuit of the comparator.

Table 3.10 gives the transistor dimension and bias current of the amplifier.

TABLE 3.10
Transistor dimension and bias current of pre-amplifier

Transistor /Resistor	W/L (μm/μm) / (Ω)	Ibias (mA)
M1	30/0.4	0.775
M2	90/0.4	0.807
M3	200/0.8	1.55
M4	350/0.8	1.614
R	2.5K	0.032

A track and hold stage of comparator is shown in Fig. 46. The input is connected to the output of preamplifier. Differential pair M2 results in a positive feedback because the input is connected to the output in a cross-coupled manner. During track phase (when *CLK* is enabled), differential pair M1 is enabled and operates as a differential amplifier, which amplifies the signal further. During hold phase (when $\overline{CLK}$ is enabled), the positive feedback takes the input signal and amplifiers it quickly until a digital level.

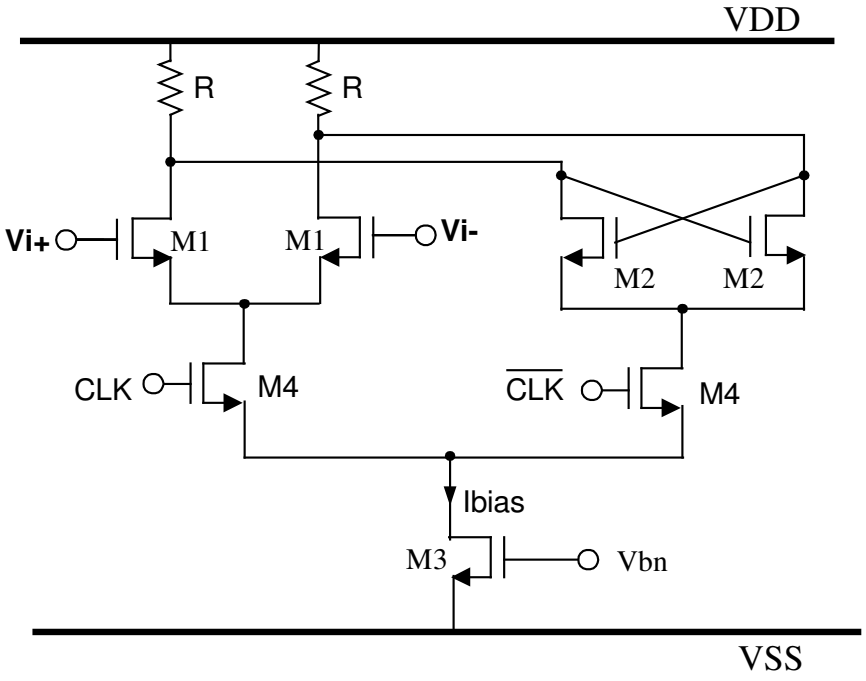


Fig. 46. Tack and hold stage of the comparator.

The transistor dimension and bias current of track and hold stages are given in table 3.11.

6.2 Simulation Results of Comparator

Fig. 45. shows the transient simulation results of the comparator. A 0.5 pF capacitor is loaded at the output of comparator. The input is a 100 MHz sinusoidal wave with amplitude of 5 mV. The comparator is clocked at 500 MHz. Note that when the second

clock detects the input greater than 0, an output transition (from low to high level) happens at the third clock. In the same way, the comparator outputs a low level at the fifth clock because the input at the fourth clock is less than 0.

The total current supply of the comparator is 12 mA at the operation frequency of 500 MHz and ±1.65 V power supply.

TABLE 3.11
Transistor dimension and bias current of track and hold stage

Stage	Transistor /Resistor	W/L (μm/μm) / (Ω)	Ibias (mA)
First stage	M1	20/0.4	0.775
	M2	40/0.4	
	M3	125/1	
	M4	25/0.4	
	R	800	
Second stage	M1	20/0.4	0.775
	M2	40/0.4	
	M3	125/1	
	M4	25/0.4	
	R	800	
Third stage	M1	40/0.4	1.55
	M2	50/0.4	
	M3	250/1	
	M4	50/0.4	
	R	300	

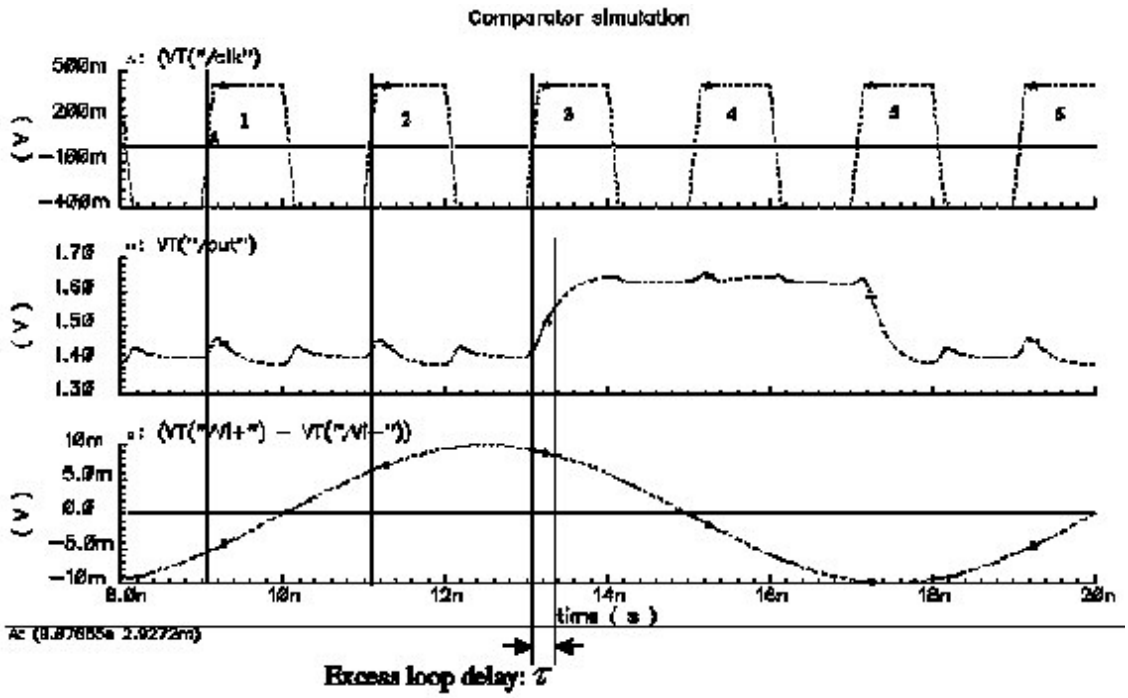


Fig. 47. Simulation results of the comparator.

As we mentioned before, the quantizer is a latched-type comparator whose output drives four differential pair DACs and the current output of DACs sum with the output of OTA at internal nodes of the resonator. Ideally, the currents of DACs respond immediately to the quantizer clock edge, however, in practical, the transistor in DACs and comparator cannot switch instantaneously. Fig. 47. shows that there is a delay (about 0.3 nsec) between the clock and the transition at the output of comparator. It is the delay we call excess loop delay. Since the latched-type comparator has a finite regeneration gain, it means that the excess loop delay depends on the input signal and a small quantizer input leads to a longer delay. Four the input with amplitude of 5 mV, the excess phase delay is 15% of clock period.

CHAPTER IV

SYSTEM SIMULATIONS

1. Introduction

In this chapter the complete system is simulated at the schematic level and postlayout level, and the results will be presented. The performance of the 4^{th}-order continuous-time bandpass modulator will be demonstrated.

2. Circuit Simulation of ΣΔ Modulator

The continuous-time bandpass ΣΔ modulator, shown in Fig. 13, has been implemented in a CMOS 0.35 μm process. We used two identical resonators and achieved full controllability by four feedback DACs with appropriate currents. A small signal AC analysis is first performed for the loop filter with DACs loaded. The filter can be tuned by a capacitors bank and the source degeneration resistors in Gm cell. Fig. 48. shows the frequency response of the filter. The gain at center frequency (125 MHz) is 45 dB and the -3 dB bandwidth is 1.6 MHz.

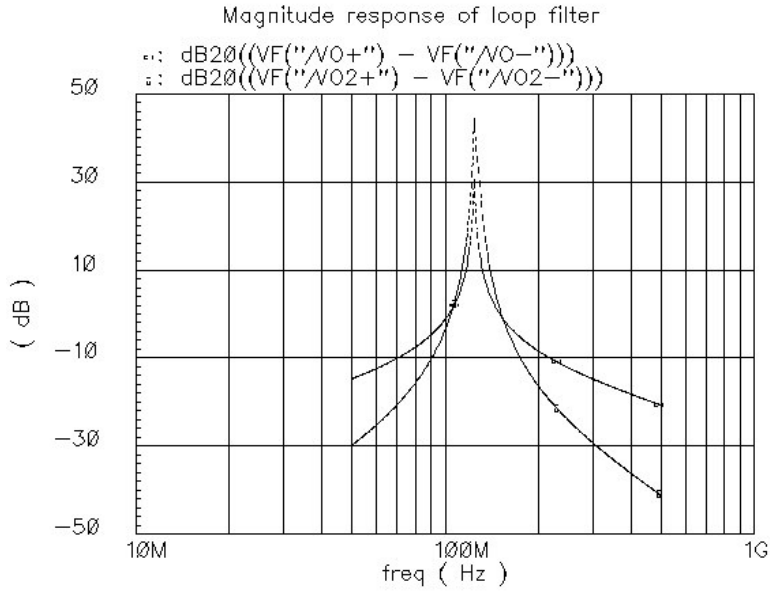


Fig. 48. Magnitude response of the loop filter in whole system.

Fig. 49. shows that the resonator frequency varies with the capacitors bank controlled by three digital bits. The tuning range of resonator frequency is from 82 MHz to 148 MHz. It demonstrates that the capacitors bank covers effectively the variation of ±30 %.

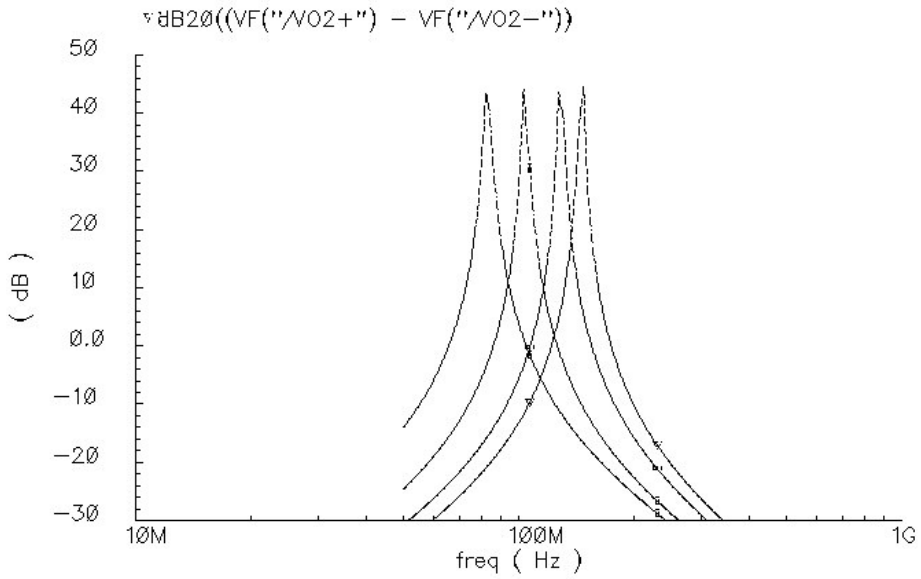


Fig. 49. Resonator frequency variation range.

It is commonly used time-domain simulation of the modulator to characterize the performance of the continuous-time bandpass ΣΔ modulator. A sinusoidal wave of 100 mV (amplitude) at 125 MHz is applied at the input. The transient simulation is performed on the whole modulator.

In Fig. 50, we see that the time domain output voltage of the first biquadratic cell has a swing of 800 mV peak-to-peak, or 400 mV peak for a input peak signal of 100 mV. As Fig. 51. shows, the voltage swing at the resonator output is less than 1 V peak-to-peak

Fig. 52. illustrates the input and output of the quantizer. The output swing is around 920 mV peak-to-peak. As mentioned before, there is a full clock delay prior to each DAC. The corresponding output occurs one clock after triggering input.

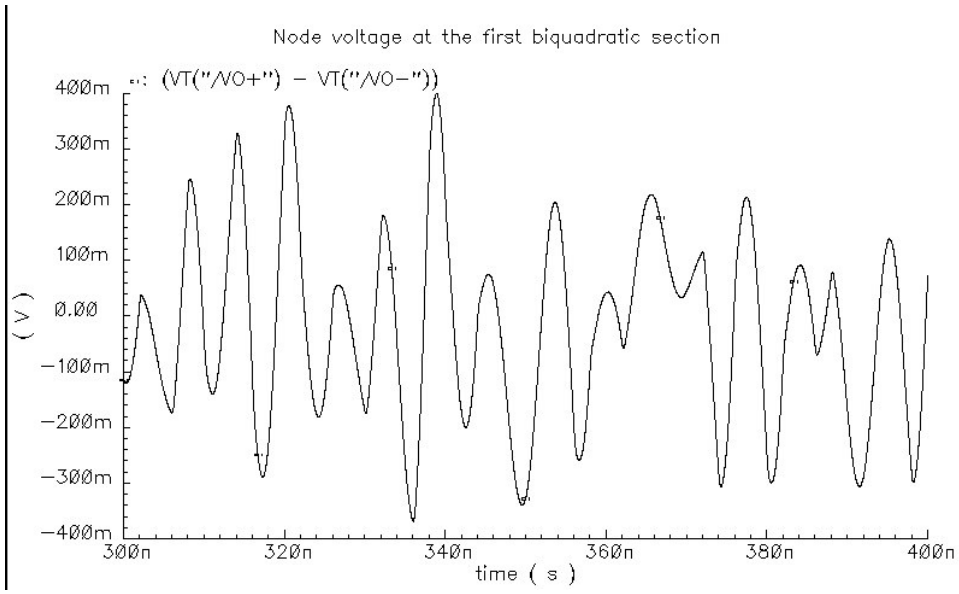


Fig. 50. Differential voltages at the output of the first biquadratic cell.

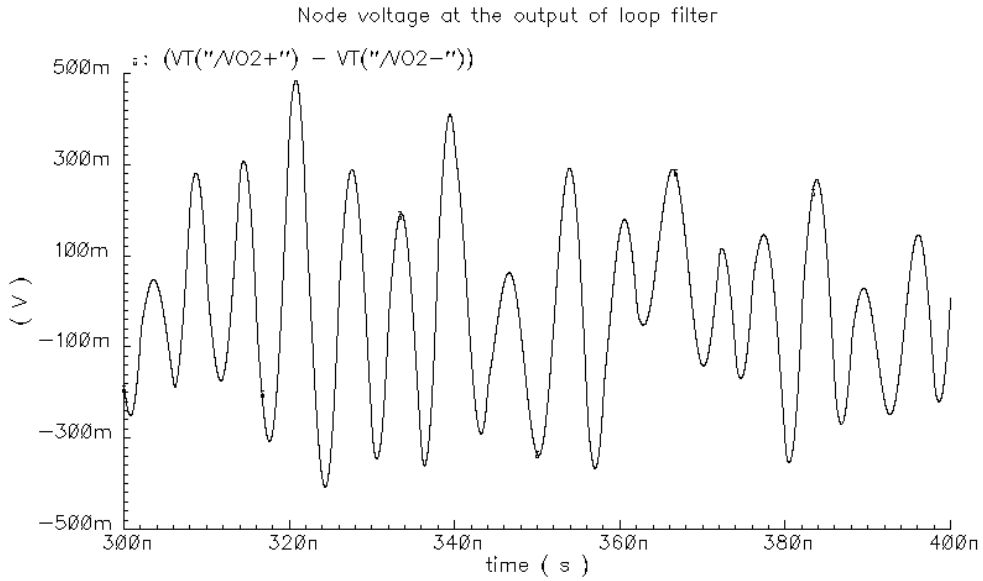


Fig. 51. Differential voltages at the output of the loop filter.

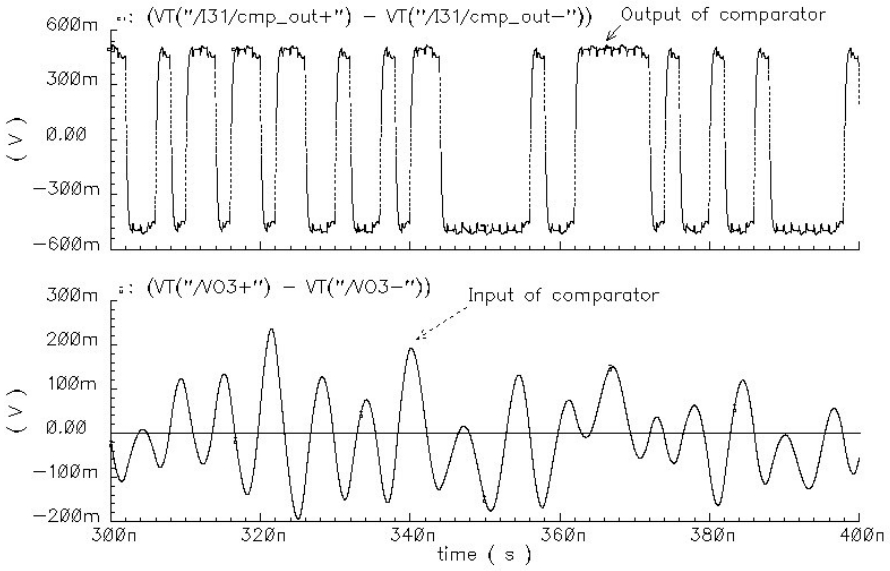


Fig. 52. Input and output signal of the comparator.

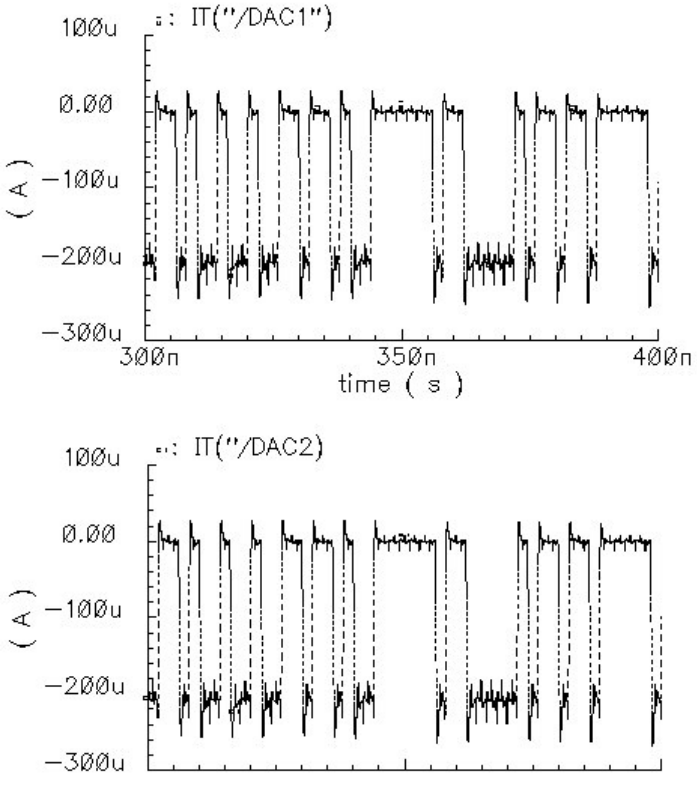


Fig. 53. Currents injected to each node of the resonator.

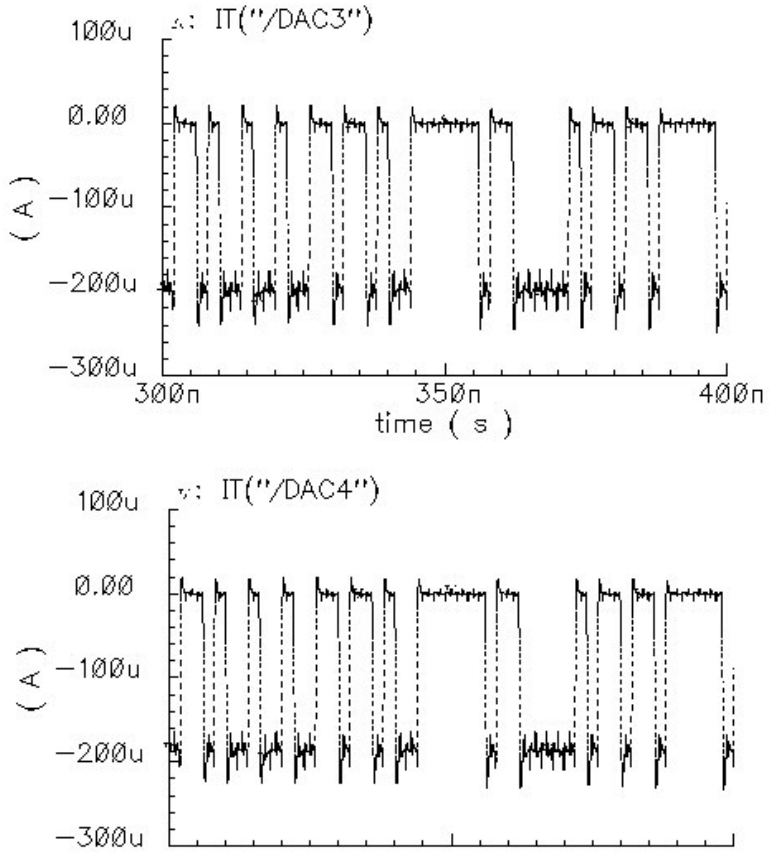


Fig. 53. Continued.

There are four DACs in the modulator. Each DAC is connected to the internal node of the resonator. The DACs are simple current-steering circuits, and the currents are relatively small (around 200 μA), as shown in Fig. 53. The feedback coefficients of the modulator are implemented by the pulse area of DACs. The current affects the loop filter zero-locations and determines the noise shaping. The glitches present in DAC outputs are mainly caused by parasitic capacitance and clock transitions.

Fig. 54. is the output of this ΣΔ modulator.

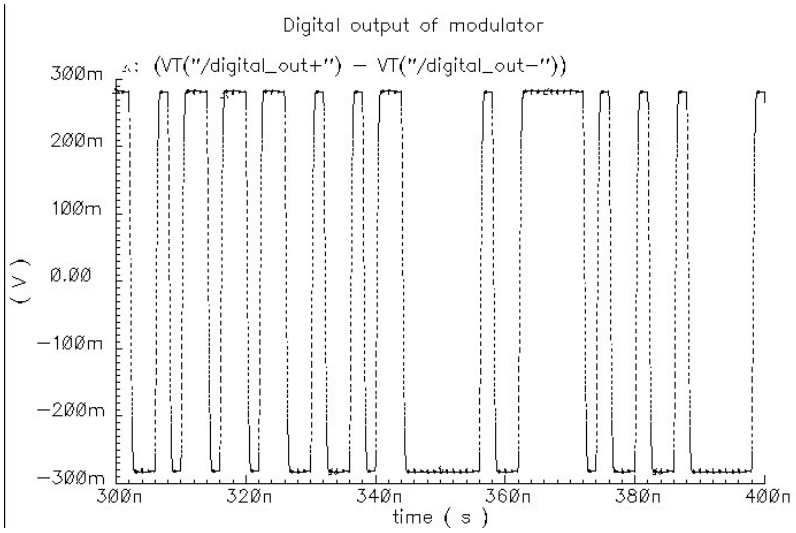


Fig. 54. Digital output of the ΣΔ modulator.

After the modulator digital output is captured, it is processed in Matlab to assess the power spectrum and compute SNDR by a 4096-point Hanning windowed Fast Fourier Transform (FFT). The SNDR is 62 dB over 1 MHz bandwidth for a sinusoidal input signal of $V_p = 0.1V$. Fig. 55. shows the noise shaping and Fig. 56. shows the noise power of the modulator.

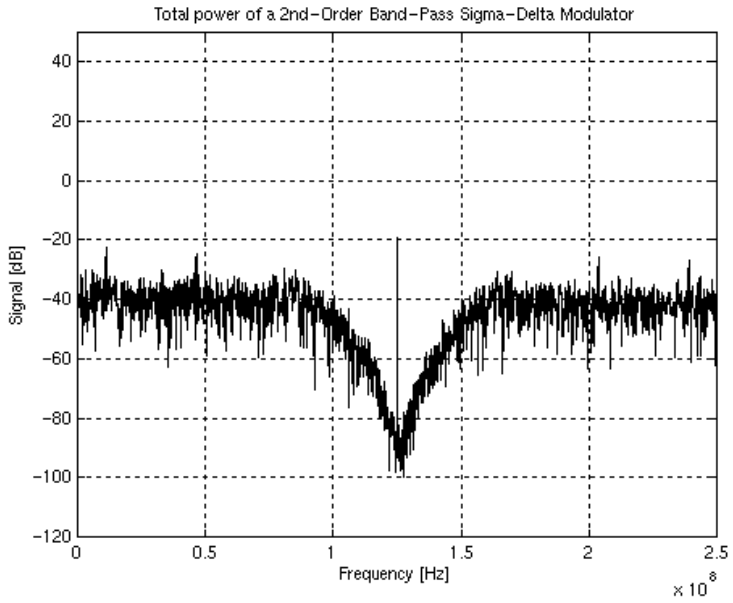


Fig. 55. Noise shaping of the ΣΔ modulator.

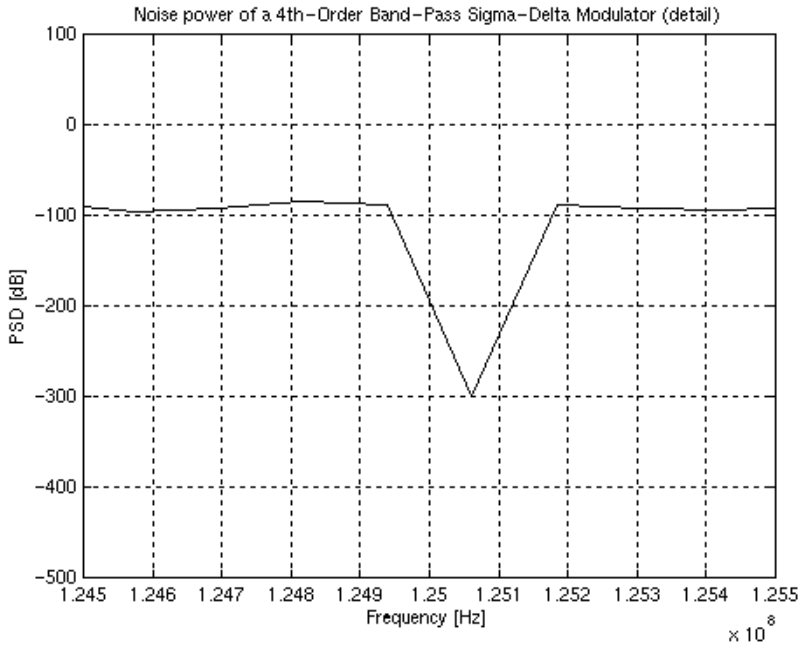


Fig. 56. Noise power of the ΣΔ modulator.

3. Layout of ΣΔ Modulator

The layout of loop filter with four feedback DACs is shown in Fig. 57. The source degeneration resistors are split into smaller elements for matching purpose. DACs are placed close to the loop filter to reduce the delay. Fig. 58. shows the layout of capacitors bank with switches. A good matching is required and the technique of splitting capacitance is also used. The layout of the comparator is depicted in Fig. 59.

The layout of the bandpass ΣΔ modulator is shown in Fig. 60, including analog and digital circuitry. Since the system contains digital circuits, such as comparator and demultiplexer, a guard ring is used to isolate the analog circuit from digital part to reduce the noise. The area of the entire ΣΔ modulator is 2041 μm × 2041 μm including the digital circuitry.

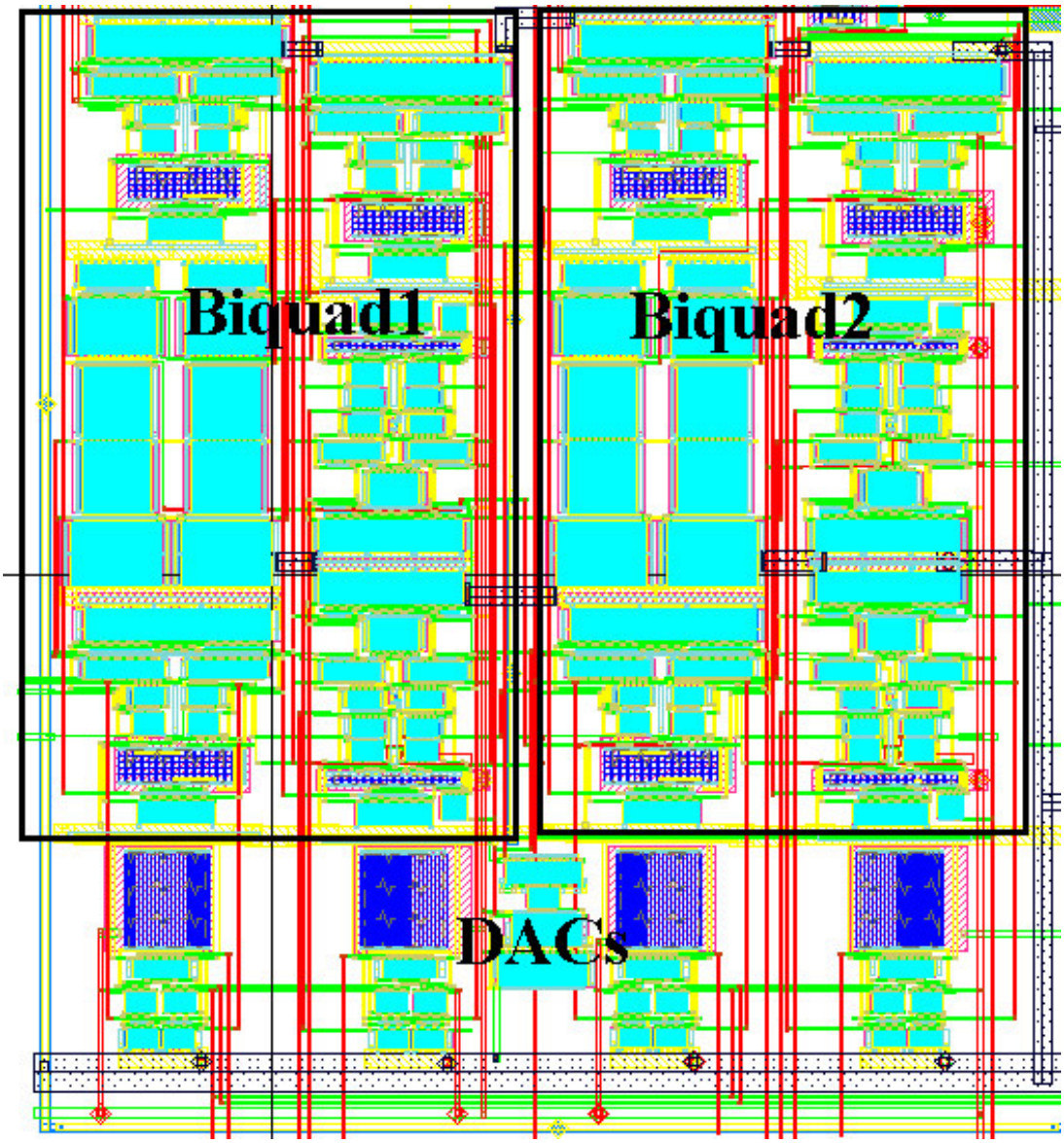


Fig. 57. Layout of loop filter with four DACs.

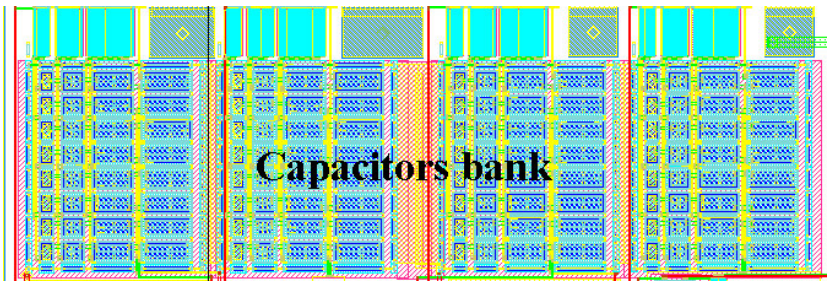


Fig. 58. Layout of the capacitors bank.

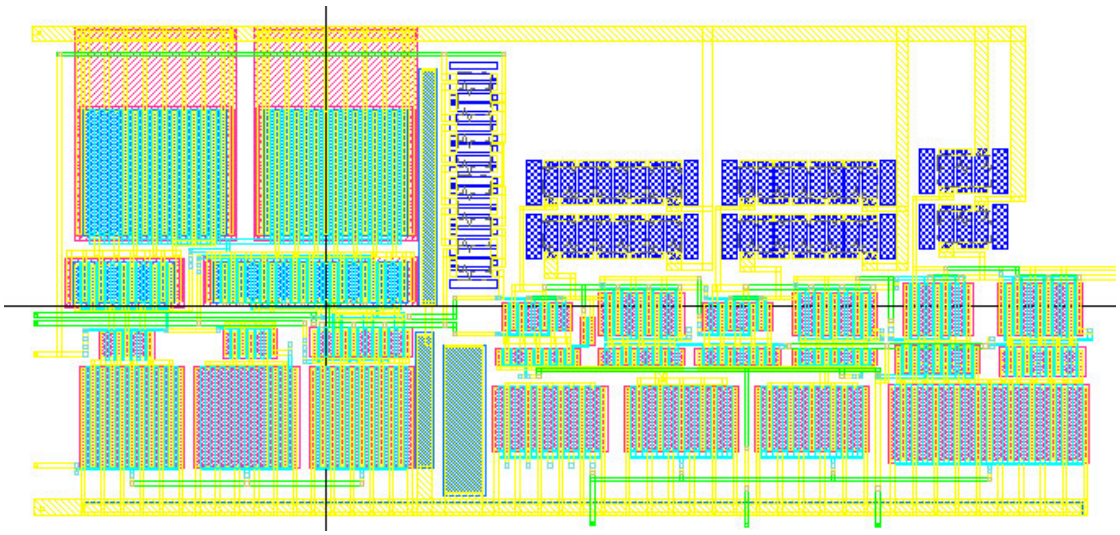


Fig. 59. Layout of comparator.

The area of each block and the modulator is given in Table 4.1,

TABLE 4.1
Summary of the area of layout for the ΣΔ modulator

Block	**Area**
Filter with CMFB and capacitors bank	500 µm × 580 µm
Four DACs	450 µm × 100 µm
Comparator	100 µm × 250 µm
Clock, DeMUX, Buffers	780 µm × 590 µm
Total Area	2041 µm × 2041 µm

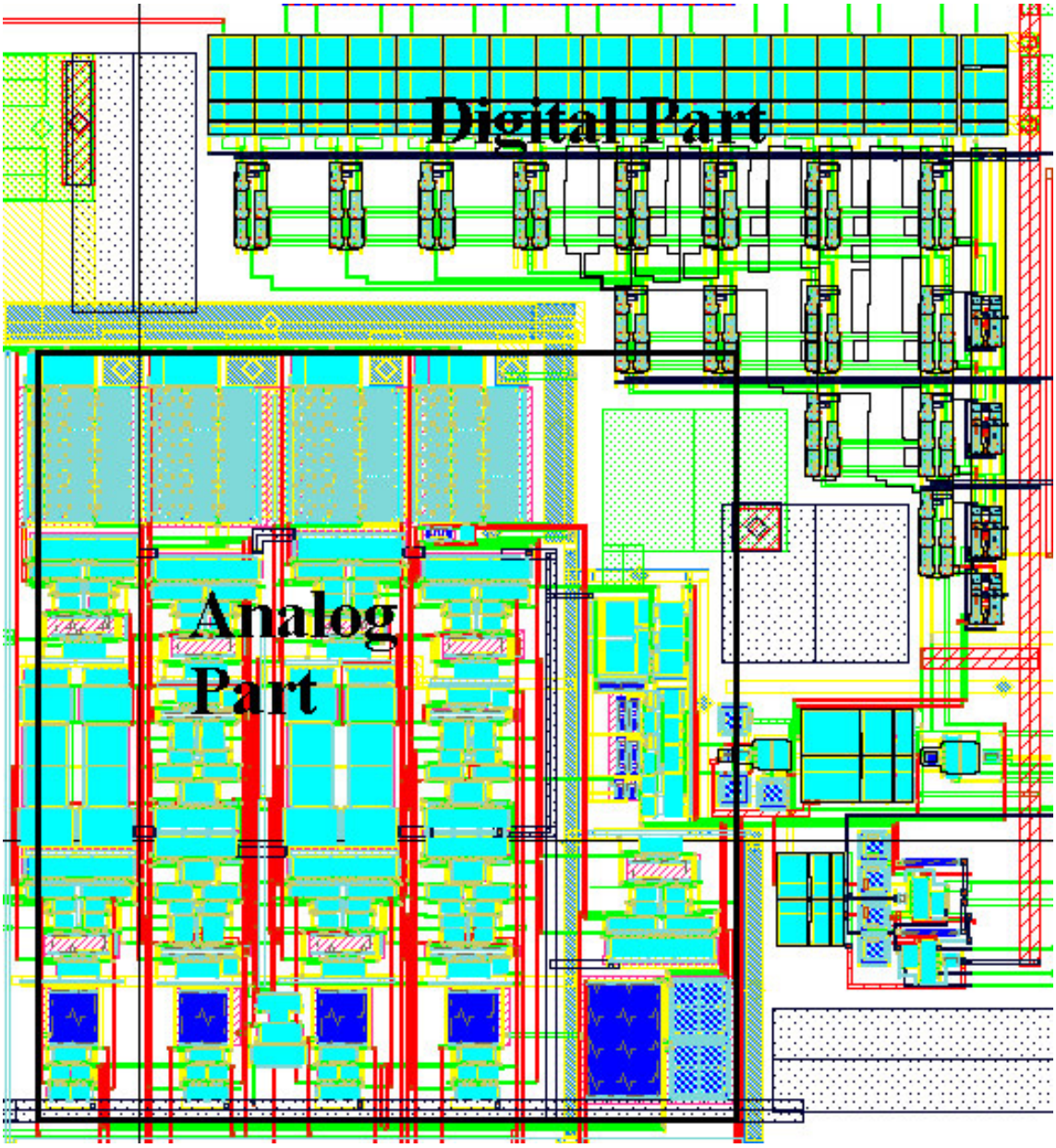


Fig. 60. Layout of ΣΔ modulator.

4. Postlayout Simulation

4.1 Postlayout Simulation of Resonator

Postlayout simulations have been carried out to check the performance of the resonator. The frequency response of resonator is shown in Fig. 61. The gain at the center frequency is 64 dB, and the 3-dB bandwidth is 0.9 MHz. The input equivalent noise density of the entire resonator is $44.7nV/\sqrt{Hz}$, or the equivalent input noise of the resonator is $44.7\ \mu V$ for a bandwidth of 1MHz.

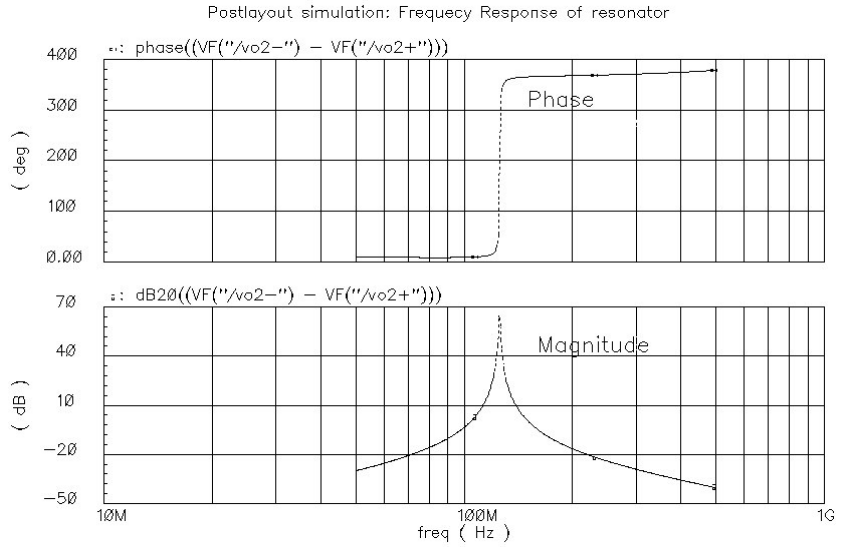


Fig. 61. Frequency response of a single resonator (Postlayout simulation).

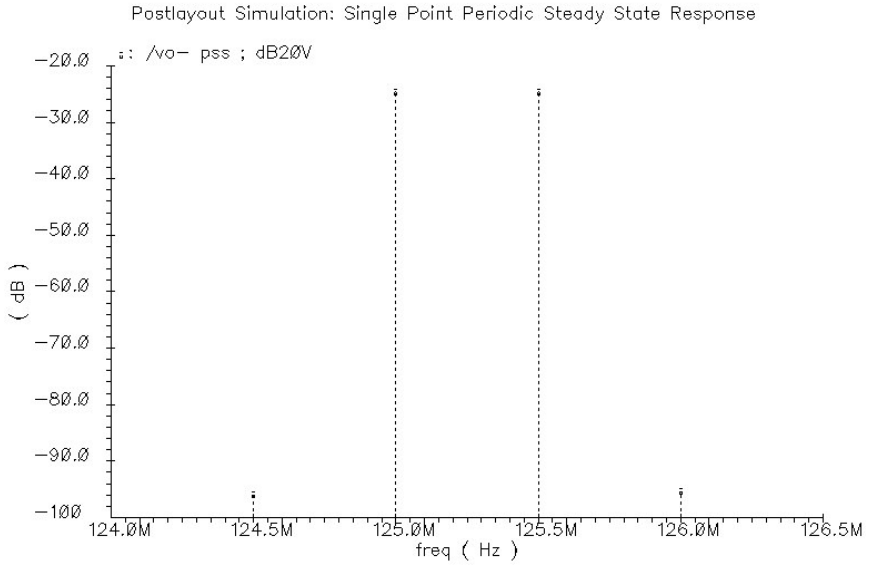


Fig. 62. IM3 distortion at the output of resonator (Postlayout simulation).

The linearity of resonator is characterized by its IM3 and the simulation is performed in the same way as for the schematic. Two tones at 125 MHz and 125.5 MHz are applied to the input of resonator, and the amplitude of each tone is 0.125 V (overall input amplitude of 0.25V). The IM3 distortion at the output of first biquadratic section is around –71 dB, as shown in Fig. 62.

Table 4.2 lists the postlayout simulation results of the resonator.

TABLE 4.2
Summary of resonator simulation results

Resonator parameters	**Simulation results**
Center frequency	125 MHz
Gain at center frequency	64 dB
-3 dB Bandwidth	0.9 MHz
IM3 @ 125 MHz, 0.5 Vpp input for the first biquadratic section	-71 dB
Integrated noise (1 MHz)	45.8 μV
Power consumption	140 mW

4.2 Postlayout Simulation of Modulator

To check the frequency response of the modulator on the layout level, a small signal AC analysis is performed. By adjusting capacitor banks and varying the source degeneration resistors, the filter is tuned to make the center frequency at 125 MHz. Fig. 63. shows the simulation results. The gain at the center frequency is 44 dB and the -3 dB bandwidth is 2 MHz.

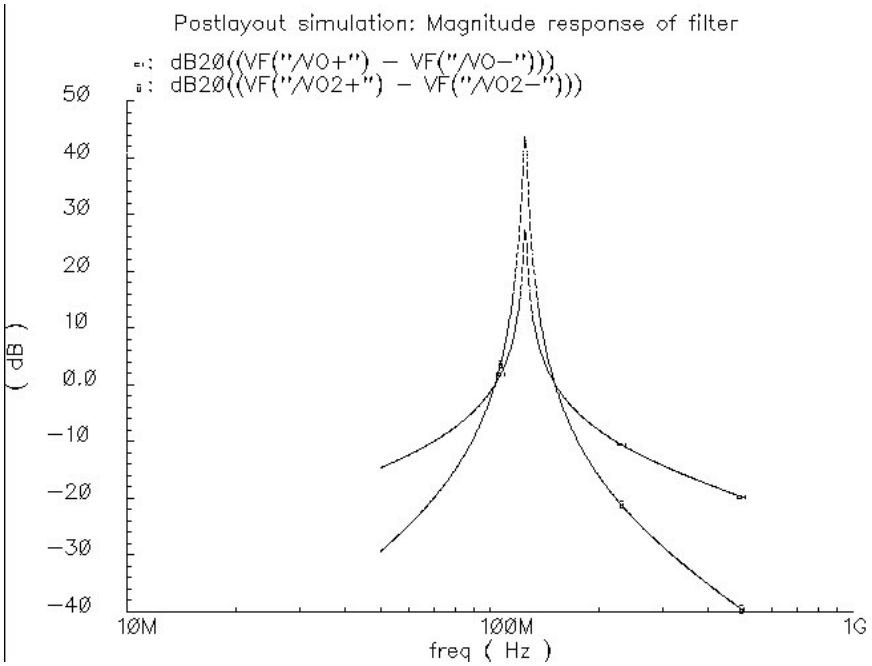


Fig. 63. Frequency response of filter with DACs loading (Postlayout simulation).

Similarly to the characterization of the schematic-level modulator, the time-domain simulation of the modulator is performed and the spectrum of output bit stream is taken. A sinusoidal signal of 100 mV (amplitude) at 125 MHz is applied to the input. Then the transient simulation for the whole modulator is performed.

Fig. 64. shows that the output voltage at the first biquadratic cell has a swing of 700 mV peak-to-peak for a input signal of 100 mV. The voltage swing at the output of the resonator is less than 800 mV, as shown in Fig. 65.

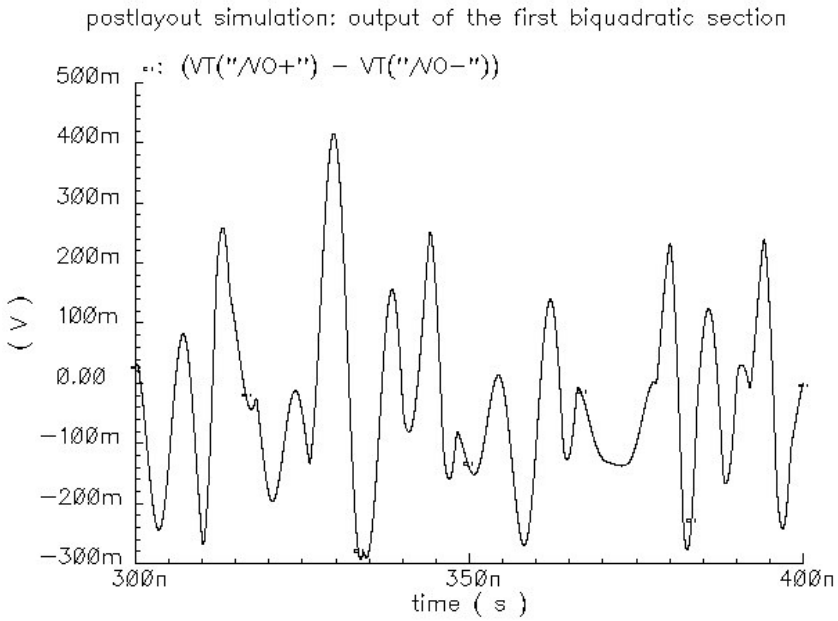


Fig. 64. Differential output of the first biquadratic cell (Postlayout simulation).

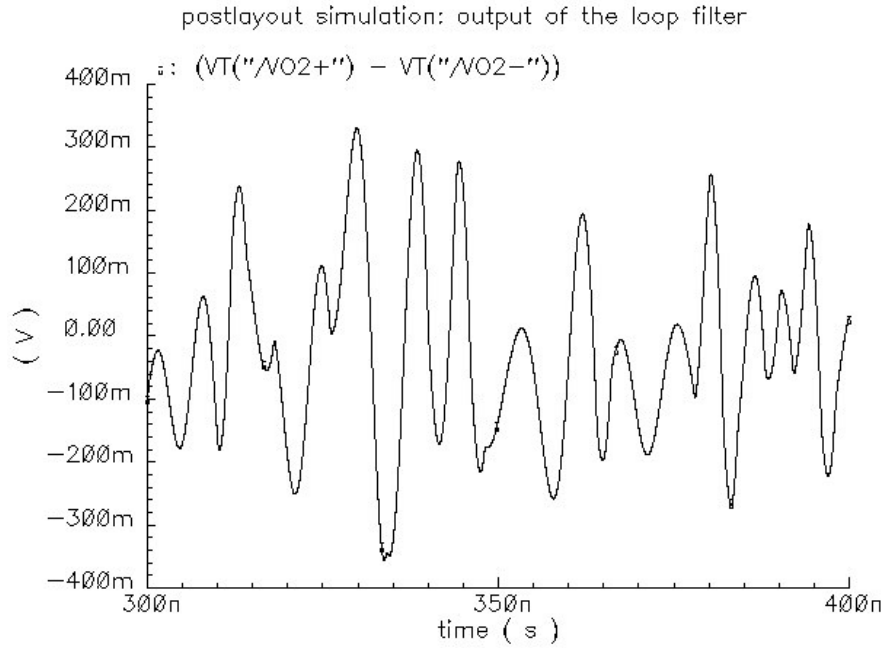


Fig. 65. Differential output of the loop filter (Postlayout simulation).

Fig. 66. illustrates the input and output voltage of the quantizer. The output swing is around 1040 mV peak-to-peak.

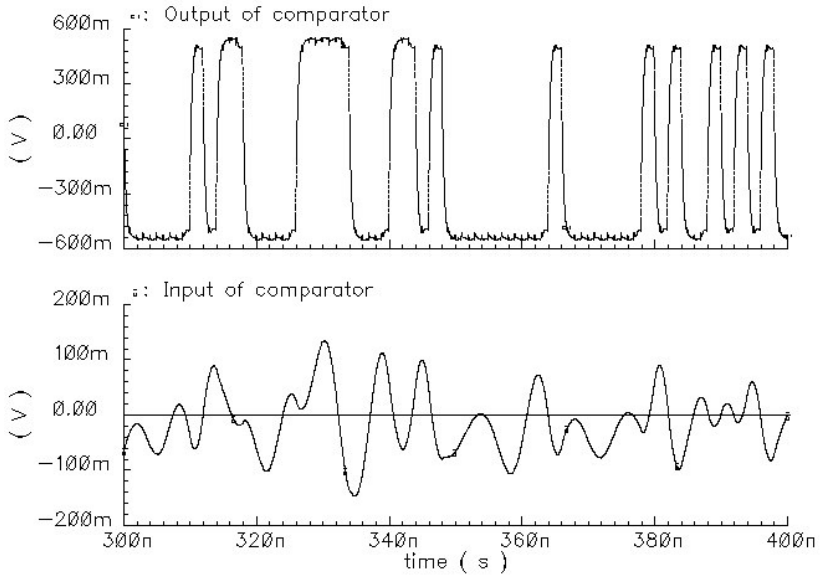


Fig. 66. Comparator characterization: input and output signals (Postlayout simulation).

Fig. 67. illustrates that the postlayout performance of DACs is very similar to that obtained for the schematic, even with fewer glitches. The main reason is that the common-centroid and interdigitized techniques are employed in the layout of DACs that reduce the parasitic capacitance, and improve component's matching.

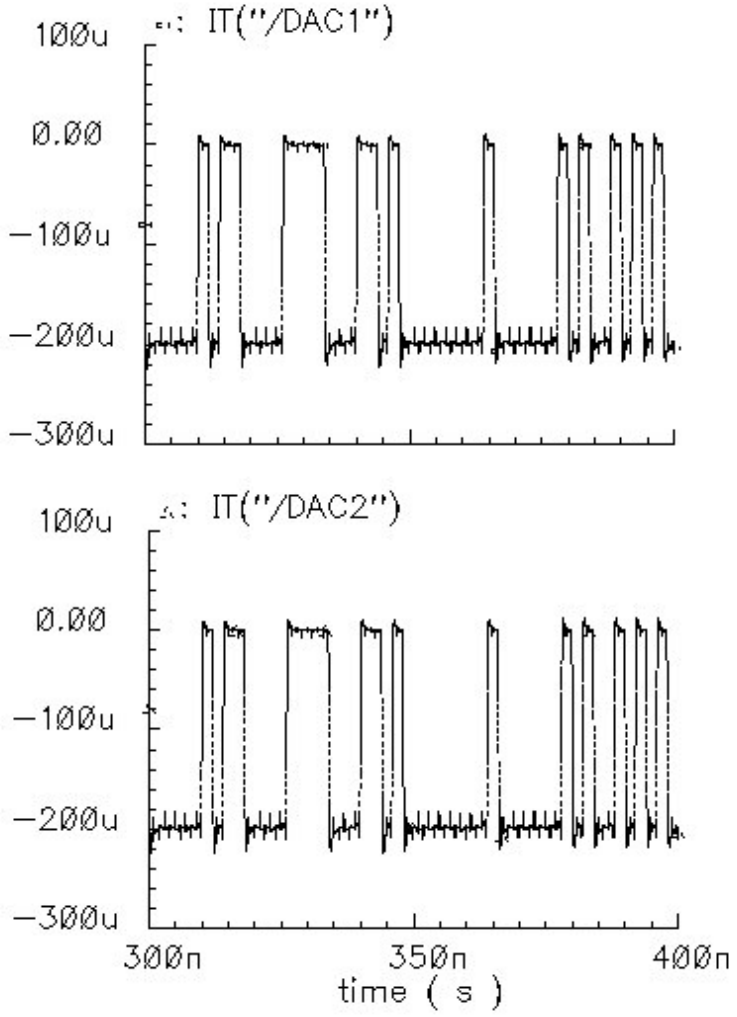


Fig. 67. Currents injected to the resonator (Postlayout simulation).

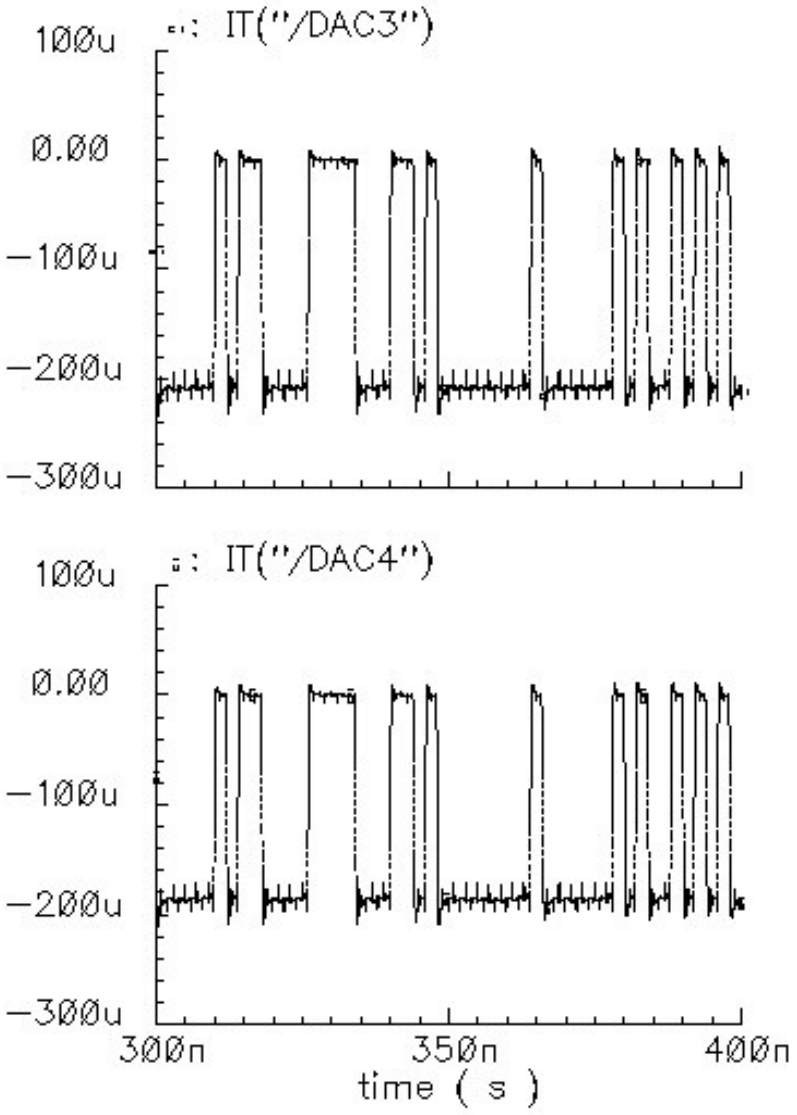


Fig. 67. Continued.

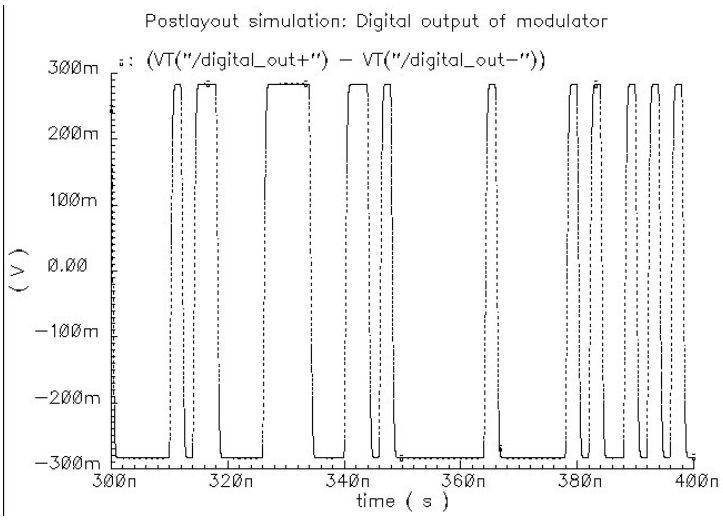


Fig. 68. Digital output of the ΣΔ modulator (Postlayout simulation).

The noise-shaping spectrum is obtained by taking an FFT (using Hanning window) of the modulator output bit stream, which is shown in Fig. 68. We can see in Fig. 69 that the SNDR is 50 dB within 1 MHz bandwidth for the input signal of $V_p = 0.1V$. Fig. 70. shows the noise power spectrum of the modulator.

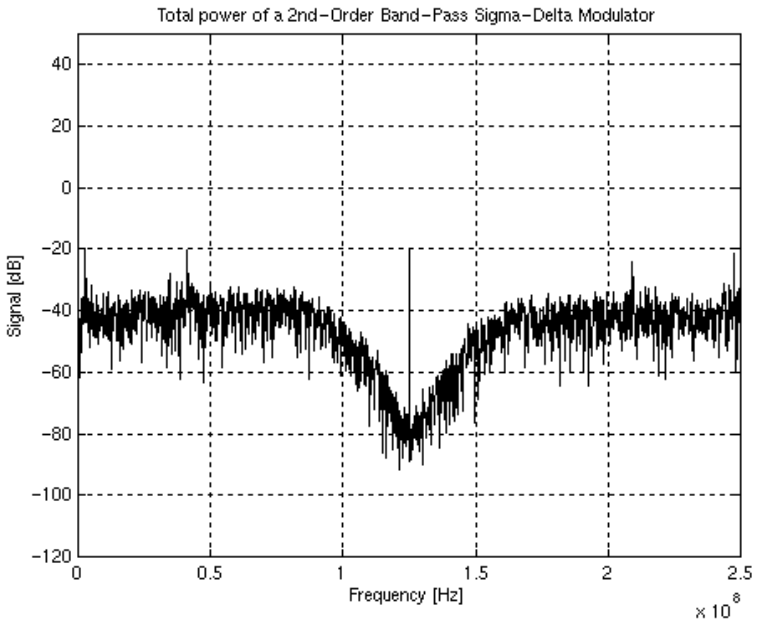


Fig. 69. Noise shaping of the ΣΔ modulator (Postlayout simulation).

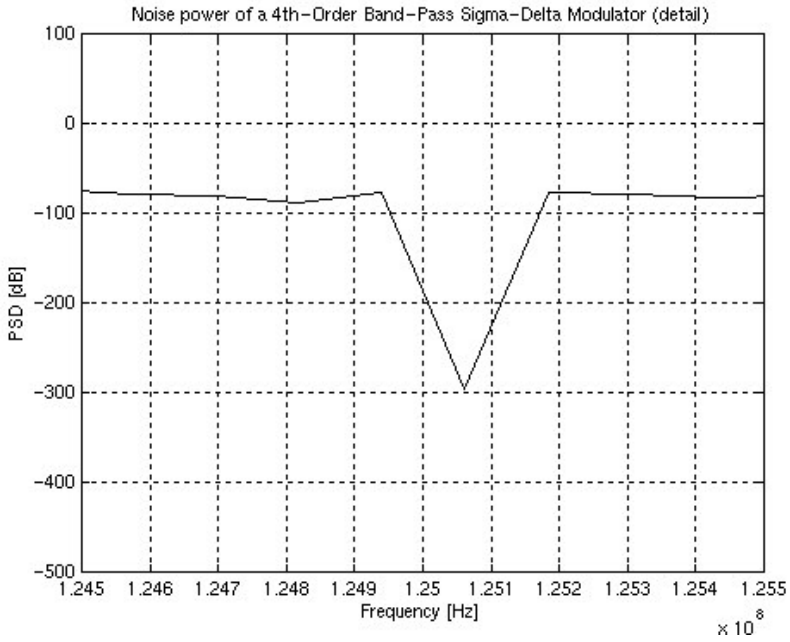


Fig. 70. Noise power of the ΣΔ modulator (Postlayout simulation).

Fig. 69. shows that the noise floor increases by 10 dB and the SNDR degrades compared to the noise floor at the notch frequency the filter achieved in schematic-level simulation, and the main reason is that we did not tune the modulator when the postlayout simulations were performed. A full circuit simulation of the modulator is painfully slow, especially when each block is described down to the layout level. We have to wait for days or even weeks while enough output bits for an FFT is being generated. Based on the experience, we expect that the fabricated device would have better performance (70 dB of SNDR) since the tuning and data-capture can be finished in short time.

5. Summary of performances

The performances of ΣΔ modulator is summarized in table 4.3,

TABLE 4.3
Summary of performance of ΣΔ modulator

Specifications		Schematic	Extracted
Filter	Center Frequency	125 MHz	125 MHz
	Gain at center frequency	68 dB	64 dB
	-3 dB bandwidth	0.3 MHz	0.9 MHz
	IM3 @ 0.5 Vpp, 125MHz	-70 dB	-71 dB
	Integrated noise (1 MHz)	45.8 μV	44.7 μV
ΣΔ Modulator	SNDR	62 dB	50 dB
	Power consumption	302 mW	302 mW

Table 4.4 shows a performance comparison between different designs and this work. A direct comparison may not be accurate because there are no other works at this frequency. However, it still demonstrates superior performance over previously reported modulators.

This design operates at 3.3 V power supply with 300 mW power consumption. The power consumption of the work is very small compared to Raghavan's design that was fabricated in an advanced technology. Also we expect that the work can achieve more than 70 dB of SNDR, which is comparable to other continuous-time modulators.

TABLE 4.4
ΣΔ modulators performance comparison

Author (Reference)	Tech.	Type	Power & Supply	Band-width	Center Freq.	Order	Performance
Shoaei(TCAS 97)	0.8 μm BiCMOS	CT (Gm-C)	-	0.2 MHz	50 MHz	2	SNDR 46 dB
Issac (M.S. Thesis)	0.5 μm CMOS	CT (Gm-C)	47 mW 3V	0.2 MHz	70 MHz	2	SNDR 42 dB
Tao (ISSCC 99)	0.35 μm CMOS	CT (RLC)	330 mW 3.3/2.7V	0.2 MHz	100 MHz	4	SNDR 45 dB
Raghavan (JSSC01)	AlInAs/ GaInAs HBT	CT (Gm-C)	3.2 W/ 10V	1 MHz	180 MHz	4	SNDR 75.8 dB
This work (postlayout)	0.35 μm CMOS	CT (Gm-C)	302mW 3.3V	1 MHz	125 MHz	4	SNDR 50dB

CHAPTER V

CONCLUSION AND FUTURE WORK

A fourth-order continuous-time bandpass sigma-delta modulator clocking at 500 MHz has been designed and fabricated using 0.35 μm CMOS technology. A single-stage OTA based on complementary differential pairs is used to achieve large transconductance for this high frequency application. Both source degeneration and cross-coupled cancellation techniques are employed to meet the high linearity requirement for the OTA operating at high frequency. Tunable negative impedance has been implemented to get a high Q-factor. The continuous-time loop filter is based on Gm-C topology. Capacitor bank and tunable Gm are used to compensate the topology against process and temperature variations.

Postlayout simulation in CADENCE demonstrates that the sigma-delta modulator achieves a SNDR of 50 dB over 1 MHz bandwidth. The power consumption is 302 mW from the 3.3 V power supply.

The chip is currently in the process of fabrication at MOSIS. Next, a Printed Circuit Board (PCB) will be made to confirm the performance obtained from hand calculations and postlayout simulations.

REFERENCES

[1] R. Schreier, M. Snelgrove, "Bandpass sigma-delta modulation", *IEE Electronics Letters*, vol. 25, November 1989, pp.1560-1561.

[2] T. Salo, "Bandpass delta-sigma modulators for radio receivers", Ph.D. dissertation, Helsinki University of Technology, April 2003.

[3] J. A. E. P van Engelen, R. J. van de Plassche, E. Stikvoort and A. G. Venes, "A sixth-order continuous-time bandpass sigma-delta modulator for digital radio IF", *IEEE J. Solid-State Circuits*, vol. 34, No. 12, December 1999, pp 1573-1764.

[4] C. I. Lao, H. L. Leong, K. F. Au, K. H. M and S. P. U, "A 10.7-MHz bandpass sigma-delta modulator using double-delay single-opamp SC Resonator with double-sampling", *IEEE Circuit and System*, vol. 1, May 2003, pp 1061-1064.

[5] V. Comino and A. C. Lu, " A bandpass sigma-delta modulator IC with digital branch-mismatch correction", *in IEEE Proceedings on Custom Integrated Circuits*, May 1999, pp 129-132.

[6] F. Henkel, U. Langmann, A. Hanke, S. Heinen and E. Wagner, " A 1-MHz-bandwidth second-order continuous-time quadrature bandpass sigma-delta modulator for low-IF radio receivers", *IEEE J. Solid-State Circuit*, vol. 37, No. 12, December 2002, pp 1628-1635.

[7] P. Cusinato, D. Tonietto, F. Stefani and A. Baschirotto, "A 3.3-V CMOS 10.7-MHz sixth-order bandpass ΣΔ modulator with 74-dB dynamic range", *IEEE J. Solid-State Circuits*, vol. 36, No. 4, April 2001, pp 629-638.

[8] P. C. Maulik, M. S. Chadha, W. L. Lee and P. J. Crawley, " A 16-bit 250-KHz delta-sigma modulator and decimation filter", *IEEE J. Solid-State Circuits*, vol. 35, No. April 2000, pp 458-467.

[9] T. Georgantas, S. Bouras, Y. Panananos and D. Dervenis, " Switched-current sigma-delta modulator for baseband channel application", *IEEE International Symposium on Circuits and Systems*, Geneva, vol. 4, May 2000, pp 413-416.

[10] O. Shoaei and W. M. Snelgrove, " Optimal (Bandpass) continuous-time ΣΔ modulator", *IEEE International Symposium on Circuits and Systems*, vol. 5, 1994, pp. 489-492.

[11] Y. F. Liang and Y. Lian, "A 250MHz CMOS bandpass delta sigma modulator using continuous-time resonator structure", *IEE CAS Workshop on Wireless Communications and Networking*, 2002.

[12] P. M. Aziz, H. V. Sorensen and J. V. Spiegel, "An overview of sigma-delta converters", *IEEE Signal Processing Magazine*, January 1996, pp 61-84.

[13] J. A. Cherry, W. M. Snelgrove and W. Gao, " On the design of a fourth-order continuous-time LC delta-sigma modulator for UHF A/D conversion", *IEEE Trans. Circuits and Systems II*, vol. 47, No. 6, June 2000, pp. 518-530.

[14] H. K. C. Issac, "A 70 MHz CMOS band-pass sigma-delta angalog-to-digital converter for wireless receivers", M.S. thesis, Hong Kong University of Science and Technology, August 1999.

[15] J. Silva-Martinez, J. Adut, J. M. Rocha-Perez, M. Robinson and S. Rokhsaz, "A 60-mW 200-MHz continuous-time seventh-order linear phase filter with on-chip automatic tuning system", *IEEE J. Solid-State Circuits*, vol. 38, No. 2, February 2003, pp. 216-225.

[16] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies", *IEEE J. Solid-State Circuits*, vol. 27, Feb. 1992, pp. 142-153.

[17] E. Sanchez-Sinencio and J. Silva-Martinez, " CMOS transconductance amplifiers, architectures and active filters: a tutorial", *in IEEE Proceedings on Circuits, Devices and Systems*, vol.147, Feb. 2000, pp. 3-12

[18] Lewinski and J. Silva-Martinez, "OTA linearity enhancement technique for high frequency application with IM3 below –65dB", *CICC 2003*, September, 2003, pp. 9-12.

VITA

Xuemei Liu received the B. S. and M. S. degrees in Electrical Engineering from Xi'dian University, P. R. China, in 1997 and 2000, respectively. From 2002 to the present, she has been a graduate student in the Department of Electrical Engineering, Analog and Mixed-Signal Center, Texas A&M University, College Station, working towards the Master's degree. Her research interests are in analog circuit design, including high frequency filter and continuous time sigma-delta modulator. E-mail: sherry95035@yahoo.com. Her home address is 231 Dixon Landing RD., Apt 257, Milpitas, CA 95035.