RETRODIRECTIVE PHASE-LOCK LOOP CONTROLLED PHASED ARRAY ANTENNA FOR A SOLAR POWER SATELLITE SYSTEM

A Thesis

by

SAMUEL JOHN KOKEL

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2004

Major Subject: Electrical Engineering

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Approved as to style and content by:

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(Head of Department)

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ABSTRACT

Retrodirective Phase-Lock Loop Controlled Phased Array Antenna for a Solar Power Satellite System. (December 2004)

Samuel John Kokel, B.S., Texas A&M University

Chair of Advisory Committee: Dr. Kai Chang

This thesis proposes a novel technique using a phase-lock loop (PLL) style phase control loop to achieve retrodirective phased array antenna steering. This novel approach introduces the concept of phase scaling and frequency translation. It releases the retrodirective transmit-receive frequency ratio from integer constraints and avoids steering approximation errors.

The concept was developed to achieve automatic and precise beam steering for the solar power satellite (SPS). The testing was performed using a transceiver converting a pair of received 2.9 GHz signals down to 10 MHz, and up converting two 10 MHz signals to 5.8 GHz. Phase scaling and conjugation was performed at the 10 MHz IF using linear XOR phase detectors and a PLL loop to synthesize a 10 MHz signal with conjugate phase.

A phase control loop design is presented using PLL design theory achieving a full 2π steering range. The concept of retrodirective beam steering is also presented in detail. Operational theory and techniques of the proposed method are presented. The prototype circuit is built and the fabrication details are presented. Measured performance is presented along with measurement techniques. Pilot phase detectors and PCL achieve good linearity as required. The achieved performance is benchmarked with standards derived from likely performance requirements of the SPS and beam steering of small versus large arrays are considered.

Dedicated to my parents Milton & Sylvia Kokel.

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CHAPTER I
INTRODUCTION

This thesis is divided into seven main chapters. The topics covered in the chapters include: 1) a review of wireless power transmission, solar power satellite, and retrodirective antennas; 2) an explanation of retrodirective operation and theory; 3) phase control system analysis; 4) system operation, design, and fabrication; 5) measured results; 6) array steering analysis; and 7) conclusions with ideas for further research and improvements.

A. Microwave Wireless Power Transmission

Wireless power transmission (WPT) is characterized by the following 3 step process: (1) converting DC electrical power to high frequency RF power, (2) transmitting the RF power through space to a distant point, and (3) receiving the RF power and reconverting it back to DC electrical power [1]. Having the capability to link power wirelessly offers consuming devices the freedom of complete physical decoupling from their power source. Removing the need for electrical wire connections between power sources and users provides a new dimension of flexibility necessary for a broad range of applications.

The existence of microwave WPT dates back to experiments of Heinrich Hertz (1857-1894) and Nicola Tesla (1856-1943) [1]. Interestingly, Tesla's first envisioned applications of electromagnetic wave propagation which he pioneered, was not centered in communication but power transmission applications [2]. At that time however, numerous devices that would be necessary to realize focused WPT at microwave frequencies did not exist.

The journal model for this thesis is *IEEE Transactions on Microwave Theory and Techniques*.

During World War II and soon after, a number of discoveries were made which enabled microwave WPT applications to be developed. Two noteworthy developments are the magnetron and amplitron, which serve as DC-to-RF converters capable of high efficiency and high power. Others include solid-state devices used to rectify the RF AC transmitted power to DC and capable of handling adequate power at microwave frequencies.

These developments spurred a surge of WPT research and feasibility investigation. William C. Brown is recognized as the father of modern microwave WPT. In 1959 he headed and was a chief innovator of the Raytheon Airborne Microwave Platform (RAMP) helicopter concept [3]. RAMP was proposed by Raytheon to the Department of Defense as a platform which would hover in a transmitted power beam, collect the beam's power to sustain its flight and activities, and provide a mobile and wireless platform suspended above the ground for communications and surveillance. The first rectennas (rectifying antennas) were conceived and built during this development along with initial methods of measuring rectenna efficiency. Rectennas are the portion of a WPT system that receive microwave power and convert it to DC power. In November of 1964 a small helicopter hovering device weighing 5 lbs. was wirelessly powered and sustained flight for 10 hours at a height of 60 ft. above a transmitting antenna. The rectenna aperture used was 4 $ft.^2$ and capable of receiving some 270 watts. Despite the demonstration, the funding for RAMP would later be cut before a complete surveillance and communications system could be implemented.

Besides RAMP, a number of other applications and demonstrations for WPT have been conceived and driven research endeavors resulting in considerable system demonstrations [4]. These endeavors span a period of many decades. In 1975, long distance WPT was demonstrated in the Mojave Desert at JPL's Goldstone Facility [5]. The power was transmitted 0.95 miles to the rectenna where it was converted to over 30

kW of output power illuminating a light bank. This system was in use for several years and demonstrated a robust WPT system.

Similar to the hovering RAMP application, in 1987 a fuel less light plane powered by wirelessly coupled microwave power was developed to serve as a communications platform. This was the result of the Canadian Stationary High Altitude Relay Program (SHARP). The plane had a wingspan of 14.8 ft., weighed 9 lbs., and circled above a target station at an altitude of 492 feet inside a 50° cone. The plane received 150 watts from a terrestrial transmitter via rectennas placed on the underside of the craft's wing structures. This power was enough to fuel the flight as well as power the electronic control systems on board used for steering and other functions.

Japan took a leading role in WPT research in the 1980's and 1990's. Japanese scientists succeeded in transmitting 830 W of power in flight from one rocket to another in the MINIX (Microwave Ionosphere Nonlinear Interaction eXperiment) demonstration [6]. In 1992 MILAX (MIcrowave Lifted Airplane eXperiment) was conducted [7]. Similar to SHARP, in this experiment a small electric airplane with a wingspan of 8.2 ft. flew roughly 49.2 ft. above a moving car over a distance of 1312 ft. powered solely by wirelessly transmitted microwave energy. This experiment was developed jointly between Kyoto University, Kobe University, Communications Research Laboratory, Nissan Motor Co. Ltd., Fuji Heavy Industries Ltd., and Toshiba Co. Japanese scientists also achieved the first WPT in space during the ISY-METS (International Space Year – Microwave PowEr Transmission in Space) experiment [7]. In this experiment a satellite was deployed into space equipped with a rectenna designed at Texas A&M University. A rocket was then launched transmitting 800 watts of microwave energy.

A considerable body of research has been done relating to WPT focusing primarily on improving rectenna performance. Such published rectenna topics include: high voltage and power output [8], large bandwidth [9], and dual frequency operation

[10]. In 2002, a rectenna design incorporating circular polarization, high RF-to-DC conversion efficiency (82%), and a low incident power density (2 mW/cm^2) was developed by B. Strassner and K. Chang at Texas A&M University [11]. A small scale WPT was presented at the 2002 World Space Congress [12]. The low level of power density at the rectenna is accepted as safe to plants and animals for extended exposure. For this demonstration, an array of 4 x 16 rectenna elements was fabricated and configured into a contiguous rectenna aperture. The aperture dimension was 3 ft. by 2 ft. and 4 in. tall and output 7.6 watts of power used to illuminate an array of light emitting diodes. This array demonstrated rectenna scalability to achieve desired power output.

B. Solar Power Satellite

Undoubtedly the largest envisioned application and driver of WPT research has been the concept of the Solar Power Satellite (SPS). The SPS concept originates in 1968 with Peter Glaser [13]. Such a system would entail launching huge solar panel structures into orbit. Outside the earth's atmosphere there would be virtually uninterrupted direct sunlight and uninhibited by the absorption and reflection of the earth's atmosphere.

Studied SPS systems propose power outputs of several giga-watts. Such systems include solar panels stretching many kilometers in length and width as well as a power-transmitting circular antenna aperture roughly 1 km in diameter. The terrestrial rectenna site to collect the transmitted microwave power would be shaped in the form of an ellipse about 10 km wide by 13 km long [14]. Fig. 1-1 depicts such a system.

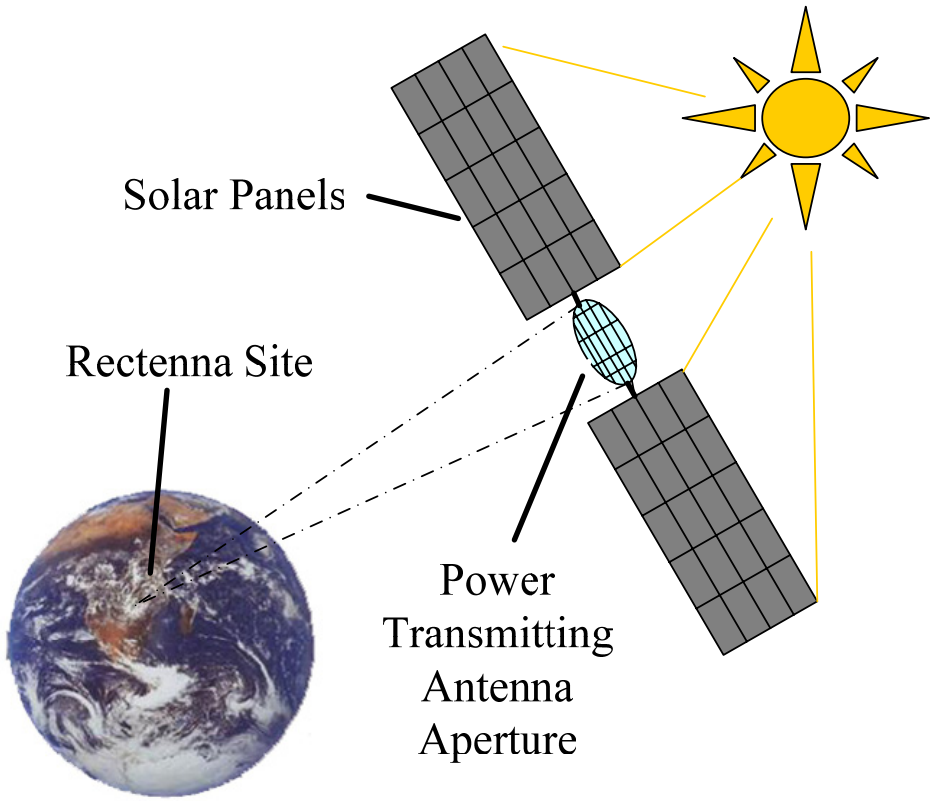

Fig. 1-1. SPS concept diagram.

These satellites will circle in geo-synchronous orbit approximately 35,000 km. above the earth and steer the microwave energy from the power transmitting antenna aperture toward the terrestrial rectenna site. Due to the large separation distance between the transmitter and receiver, steering accuracy is a very crucial part of system performance. Very small angular steering errors translate to huge swings of the focused microwave energy on earth away from the desired rectenna target. Fig. 1-2 illustrates the relationship between the steering error and its translation to displacement dimension. Where d is the separation distance, θ_e is the angular steering error, and r_u is the linear error distance from the zero error line.

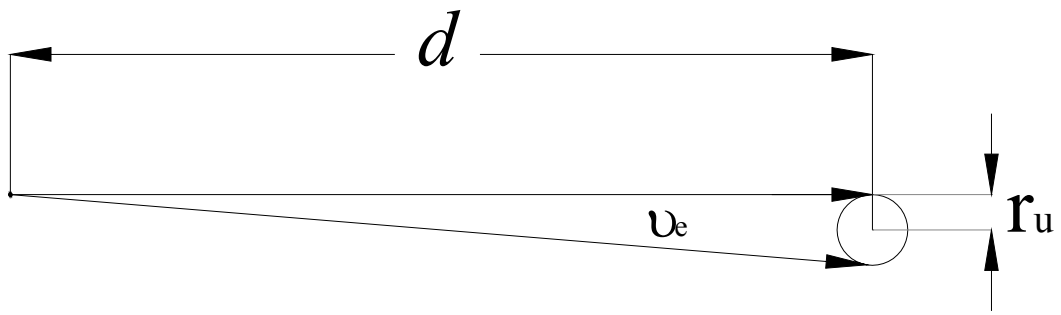

Fig. 1-2. Angular error to linear error translation.

The translation from angular error to linear error is given as: $r_u = d \cdot \tan(\theta_e)/2$. For application of the SPS the separation distance d will be around 35,000 km. This separation translates an angular steering error of $\theta_e = 0.0005$ degrees to a linear error of $r_u = 0.305$ km. This illustrates that even slight steering errors can cause a beam to stray from its intended targets drastically due to the large separation distance (d).

Other considerable factors contribute to the rigorous demands placed on the ability of the SPS to track its orientation changes relative to the terrestrial rectenna site. The SPS will be many kilometers in length and width, most likely in constant gyroscopic rotation. This rotation will create dynamic perturbations in the satellite attitude that must constantly be corrected for by the transmitting antenna. The transmitted power must also travel through the earth's atmosphere, which has electrical properties that are constantly changing and unpredictable. These properties can bend the direction of propagation as well as alter radiation polarization. Furthermore, the mechanical structure of the SPS will be constantly expanding and contracting due to temperature changes affecting the transmitting antenna array element spacing. All these effects pose challenges to the system's ability to accurately steer the highly directive power beam toward the receiving target.

C. Retrodirective Beam Steering

The concept of retrodirective beam steering has been employed in an attempt to overcome these steering obstacles and accurately direct the microwave power toward to the rectenna target.

Given the dynamic environment of an SPS, retrodirective beam steering has been identified as the most suitable choice to achieve WPT [14]. This is largely because the steering mechanism of the system is completely autonomous and needs no input or sensing of exterior variables. It needs only the target's pilot signal. Attempting to steer the beam without a pilot would require constant input from numerous sensing devices monitoring satellite attitude, satellite position, atmospheric conditions and other phenomena as well as processing the constant input in order to calculate the steering correction.

Another important characteristic of a retrodirective system besides its accuracy is its phase control bandwidth. This translates into the ability of a retrodirective system to make steering corrections at a sufficient rate to keep up with the changing attitude of incoming pilot signal. For the application of the SPS, the aforementioned phenomena of atmospheric redirection and thermal expansion/contraction occur at very low frequencies such as a few hertz. The higher frequency steering disturbances include the antenna rotation and mechanical vibrations. Though high relative to atmospheric and thermal variations their change rates will be with in the range of a few kilohertz maximum. Retrodirective systems involving moving targets and signal modulation must also account for these variation rates in the system design as well.

A number of retrodirective techniques have been explored and presented in literature. The very first retrodirective devices, filed for patent in 1955, were passive and commonly referred to as Van Atta reflectors [15]. Chuck Pon in 1964 was among the first to publish active retrodirective antennas capable of redirecting greater power in

the direction of the pilot beam than was received [16]. Since that time, there has been a considerable body of research conducted on the topic of retrodirective beam steering available in literature [17]. However, the largest body of retrodirective research has centered around its potential use for communications. Communication antennas usually have a large beam width and low transmitting power compared to that of the SPS. These systems are designed with the ultimate goal of achieving maximum information transfer and not maximum power capture. Retrodirective systems suited for efficient WPT remain largely unexplored.

The retrodirective system presented here has been configured specifically to investigate retrodirective antenna performance in an SPS system. The array element spacing for the power transmitting antenna is quite large at several wavelengths and is realistic for an SPS [14]. This large element spacing is possible due to the limited range of antenna steering that will be required. This retrodirective design utilizes linear phase detectors and a phase-locked loop (PLL) structure to achieve retrodirectivity. The incoming pilot signal is received by pilot elements embedded in the power transmitting aperture and down converted with reference signals containing coherent phase. The pilot phase is then measured to determine correct phasing for the retrodirective antenna.

A new and novel idea of phase scaling is used to transform the measured pilot phase to the corresponding transmit phase. In previous literature, transmit frequencies were determined to be harmonics of the pilot frequency unless microprocessors were used. The proposed method allows completely independent transmit and receive frequencies without the use of data converters and processors.

Though designed for SPS's, the proposed design contains functionality promising for other retrodirective applications as well such as communications and radar. Many retrodirective techniques performed exclusively at high frequencies never allow users access to the directional information from the pilot beam. Down-converting

the pilot signal and using linear phase detectors outputs target direction information as a measurable DC voltage. Such a system serves the dual purpose of autonomous beam steering as well as position sensing. The proposed design could be achievable on a single chip augmented with minimal low cost electronics.

CHAPTER II
RETRODIRECTIVE PRINCIPLES, THEORY AND IMPLEMENTATIONS

This chapter gives an extended introduction to the concept of retrodirectivity, its theory, a review of the implementations by which it has been achieved, and a new proposed method. It concludes by highlighting the proposed method's differences, advantages, and disadvantages.

A. Retrodirective Concept

For the purposes of this thesis, an entity may be referred to as retrodirective when it receives a transmitted signal from a previously unknown direction and reflects or transmits a return signal achieving maximum directivity in the direction of the incoming signal. This concept is effectively illustrated by contrasting the behavior of two elementary structures – one retrodirective and the other not.

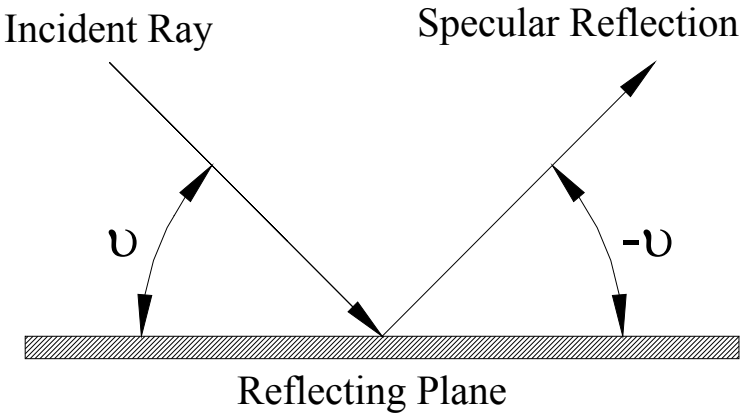

Fig. 2-1. Non-retrodirective reflection.

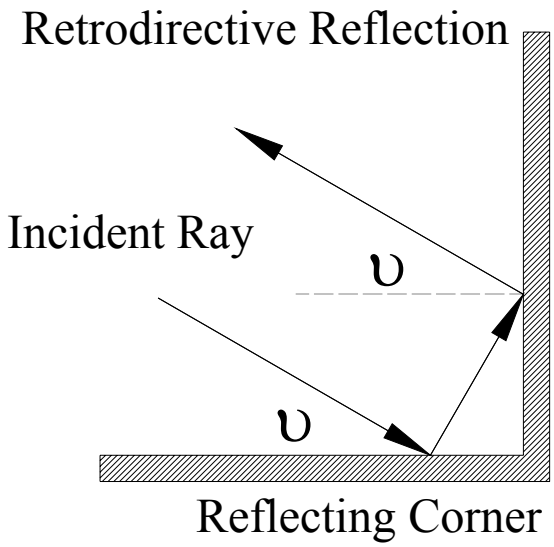

Fig. 2-2. Retrodirective structure.

Fig. 2-1 illustrates a non-retrodirective structure. An incident signal is reflected from the surface according to Snell's law and not back in the direction of the incident source. Fig. 2-2 illustrates the most basic retrodirective structure – a reflecting corner. After two reflections, the incident signal is redirected back to the direction from which it came. Regardless of the incident angle theta, this retrodirectivity will always be achieved.

Figs. 2-1 and 2-2 are reflective structures of a completely passive nature. Many retrodirective techniques have been developed employing active circuits, frequency conversion, and gain components. In many instances, the retrodirected signal can be consider a return transmitted signal rather than a reflection. The combination of active components has produced sophisticated retrodirective structures achieving high power return signals, transmit-receive frequency translation, and carrier modulation. Fig. 2-3 illustrates a generic retrodirective system as it may be understood for the purposes of the solar power satellite (SPS). Here, a mobile target antenna transmits a pilot signal. The pilot is received with a progressive phase shift across a retrodirective aperture. The

aperture in this illustration is an antenna array. The progressive phase shift contains the information required to determine the direction of the target's origin - the direction of arrival (DOA). Retrodirective Antennas (RA's) are specifically designed to preserve and operate upon the progressive inter-element phase shift.

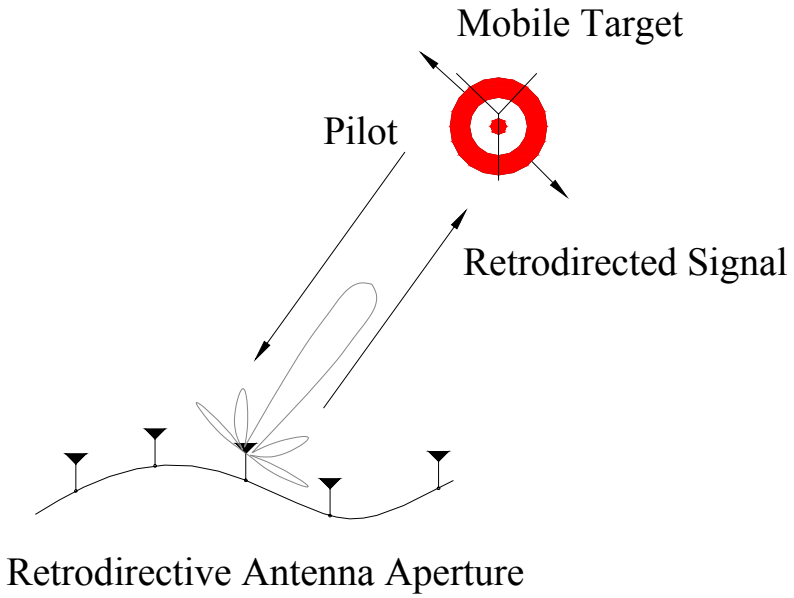

Fig. 2-3. Retrodirective antenna array.

B. Retrodirective Advantages and Applications

An RA is self-steering, dependant only upon the integrity of the pilot signal. It requires no other position or attitude sensors, nor information exchange between the target and RA. This allows compact and self-contained system implementation.

RA's in general are ideal for a broad range of applications: automatic pointing and tracking systems, microwave tracking beacons, radio frequency identification (RFID), cross-links for small satellite networks, and the SPS [18]. RA's excel in any

application where the relative position between two link points is not fixed. It is ideal for communication links between station to mobile users as well as mobile to mobile users. The highly directive pattern of RA's also lends itself to link and communication security. Since very little power is transmitted in directions other than in the intended direction, eavesdropping from any position other than in the main beam direction would be much more difficult [18]. The same spatially selective property could aid in achieving spatial diversity in large communications networks where unwanted interference due to spatial overlap is problematic.

Another advantage of retrodirective systems is their ability to conserve energy, one very important for many remote applications. Automatically steering antennas could likely replace omni directional antennas in many applications. RA's can be highly directive. Omni directional antennas transmit energy indiscriminately in all directions. Most of this energy will go unused. RA's are highly directive and transmit the majority of its energy in the direction of the target. This technique cuts out the wasted energy transmitted in other directions. Having a higher gain in the direction of the target allows for a decrease in the power transmitted and could extend battery life for remote users.

Due to the nature of their design and theory, RA's achieve virtual instantaneous steering control. There is no dependency of the system on positional communication system interrupts. Computing corrective beam steering based on other steering techniques can require a large network of sensory inputs and a large amount of arithmetic signal processing. These constraints will be the main factors limiting such systems ability to correct its steering rapidly and are often based on a large network and subsequently plagued with large liabilities for performance constraint or failure.

C. Retrodirective Disadvantages

Achieving retrodirectivity does of course involve tradeoffs in most cases. Compared to omni directional antennas retrodirective steering systems are much more

complex. They require a pilot source at the target, phase operation circuitry, and some form of antenna array. This complexity increases system cost of both design and fabrication. The pilot and phase operation circuitry would consume power as well. This power consumption might offset some or all of the power savings gained over the omni directional antenna. The signal to noise ratio might also suffer, depending on RA type. Many RA architectures involve conversion losses and attenuation to the signal. This can lower the system noise performance. To date, the operation frequency of most RA's has been very inflexible compared to other beam steering systems and hardware determined. Such characteristics have prevented frequency agile retrodirective systems. This is largely due to the method used to obtain retrodirectivity. However, the phase conjugation method proposed in this thesis will challenge that limitation.

As always, a good understanding of the trade offs between RA's and more conventional systems will be necessary to choose the most beneficial beam steering technique. A considerable body of research is being done concerning RA's. Further investigation into the performance characteristics and limitations of RA's will be necessary to empower system designers to choose the most appropriate solution.

D. Phased Array Review

The idea of phase shift across an antenna array aperture is central to the governing laws of RA's. Thus the theory of RAs must begin with a brief review of phased array antennas. A phased array antenna is used to electronically control the gain pattern and directivity of its aperture by inserting phase differences between its elements. This steering apparatus is desirable over mechanical steering because of its speed and independence of moving parts.

Consider a wave front with normal incidence relative to a flat array aperture with equal inter element spacing *d* as shown in Fig. 2-4. The array structure in Fig. 2-4 will

be referred to as a uniform linear phased array. Note the synchronized phase at the different antenna elements of the incident wave across the array.

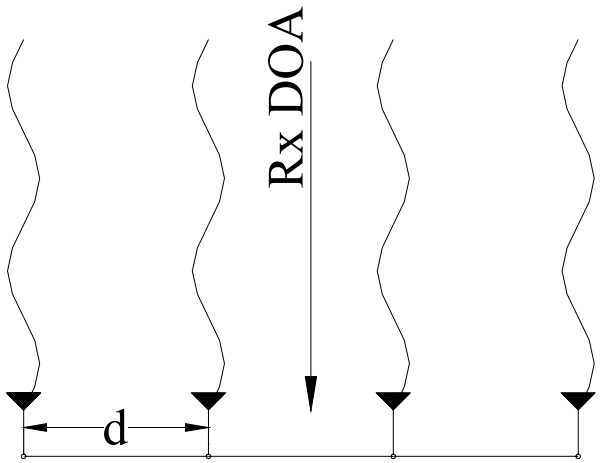

Fig. 2-4. Antenna array – normal incidence.

As the angle of incidence moves away from normal, the incident signal reaches different elements with different phase as shown in Fig. 2-5. Note the linear relationship between the phase lag and antenna position as it moves away from the arbitrary zero element. Assuming uniform inter element spacing of d and that the wave is propagating through free space, the geometry of the problem results in

$$\Delta\varphi = 2\pi fd\sin(\theta)/\mathrm{c}. \tag{2.1}$$

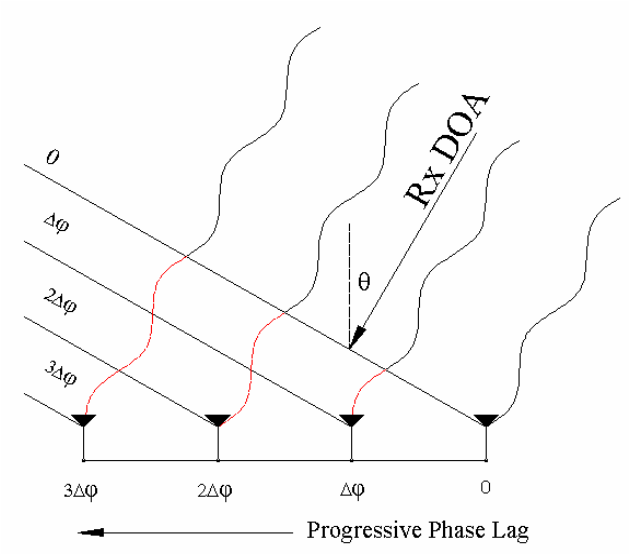

Fig. 2-5. Incident wave phase lag.

Δφ is the phase lag between two adjacent array elements; f is the frequency of the incoming wave; 'θ' is angle of incidence relative to the normal angle; and c is the speed of light in free space. Combining the progressive phase delay across all elements relative to the zero element gives

$$\Psi_N = 2\pi f d N \sin(\theta)/c. \tag{2.2}$$

Where Ψ_N is the combined phase lag of the Nth element away from the zero element and increases in Fig. 2-5 from right to left.

In order to fully utilize the large antenna aperture of the array, the received waves may be combined. However, as seen, if the incident angle moves away from normal incidence, the resulting multiple signals with various phase differences combine destructively and degrade the combined signal power. This problem may be overcome be placing the appropriate phase delay to counter destructive recombination as can be predicted by (2.2). The resulting phase adjustment places a phase delay element

increasing from right to left and incrementing by Δφ for the incident angle case shown in Fig. 2-5.

Conversely, reversing the direction of wave propagation from in to out produces a perfect complimentary case. Such as the previous inward propagation can be regarded as illustrating a receiving phased array antenna, the outward propagation case is analogous to a transmitting antenna as suggested by the illustration in Fig. 2-6. In this case the phase lag translates to phase lead. In order to achieve constructive recombination in the intended direction, the proper phase lead must be inserted into transmitting array just as the proper phase lag was inserted into the receiving array. Phase lag inserted in the opposite direction and of opposite sign in the place of phase lead achieves the correct element phasing for maximum directivity in the desired direction.

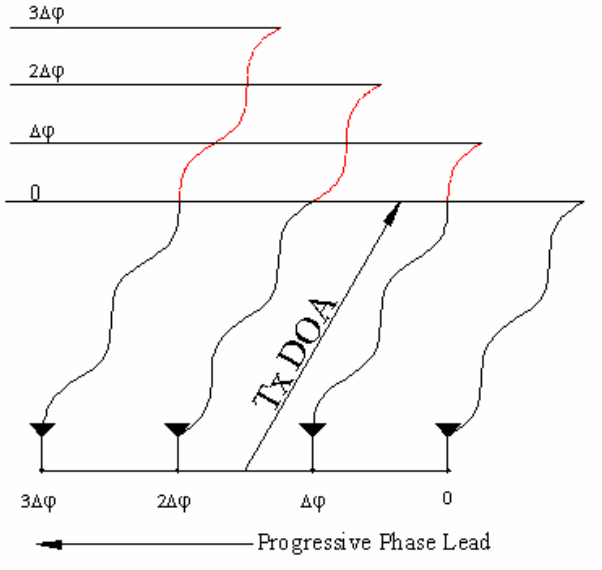

Fig. 2-6. Transmitting phased array.

E. Phase Conjugation

By now the necessary transmit-receive phase relation should be clear. In order to transmit in the same direction from which the array is receiving, the phase lead of the transmitting signal should be equal in magnitude to the phase lag of the incoming signal (assuming the transmit and receive frequencies are equal). Assigning a positive phase value to phase lag and negative to phase lead provides the basic retrodirective governing equation:

$$-\varphi_{Tx} = \varphi_{Rx}\,. \tag{2.3}$$

The operation of phase negation is commonly called phase conjugation. The classical conception of retrodirective beam steering simply transmits the outgoing in conjugate phase relation to the incoming wave. The term conjugation will be broadened for the context of this material to include the operation of phase scaling. This may include adding another cofactor X to the φ_{Rx} side of (2.3) The reason for this will become clear after the additional concept of frequency translation is presented.

Though the arguments will not be presented in this thesis, it is noteworthy that such an antenna configuration need not be planar or linear. The illustrations presented here have all been of the linear variety with uniform spacing to ease presentation of the concept. However, phase conjugating arrays may be conformed to fit any curved surface and contains the inherent ability to correct the phase irregularities of curvature.

It is also worthy to note that phase conjugation of two-dimensional arrays results in two-dimensional beam steering. Again, the presented illustrations have been of one dimension to simplify concept presentation and explanation. Expanding the one-dimensional arguments to two dimensions results in another axis of steering freedom.

F. Frequency Translation

Moving towards a frequency translating retrodirective system, consider a linear uniform phased array antenna tuned to receive an incoming signal from direction θ at frequency f_{Rx} while simultaneously transmitting a return signal in the same direction at a different frequency f_{Tx}. In this case, though the inter element delay versus position relation will remain linear, it will be scaled by a larger value for the higher frequency due to its shorter wavelength. Fig. 2-7 illustrates the same geometry as in previous examples but changes the metric of phase delay to that of time delay.

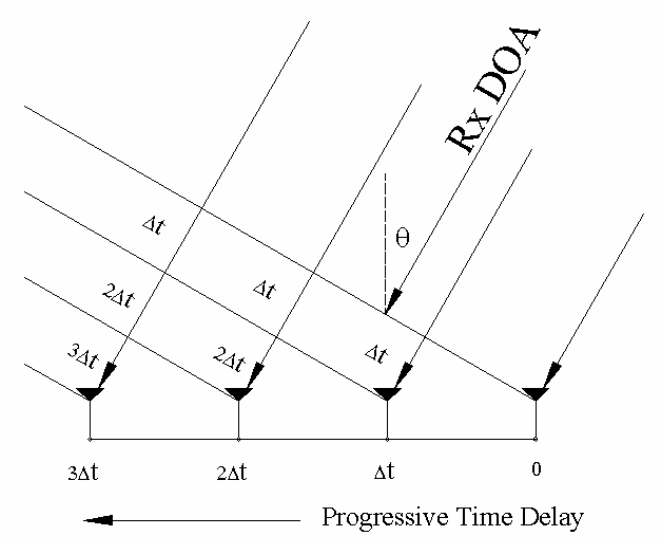

Fig. 2-7. Phased array time delay metric.

Similar to (2.1)

$$\Delta t = d\sin(\theta)/\mathrm{c}. \tag{2.4}$$

Relating Δφ to Δt for a given frequency gives

$$\Delta\varphi = 2\pi\Delta t f\,. \tag{2.5}$$

Given two different transmit and receive frequencies and using (2.5) the following relation is easily derived:

$$\Delta\varphi_{Tx} / \Delta\varphi_{Rx} = f_{Tx} / f_{Rx} \equiv X . \tag{2.6}$$

X is defined as the ratio between the transmit and receive frequency and will be referred to as the phase scaling factor. This name is given since for two given frequencies f_{Tx} and f_{Rx}

$$\Delta\varphi_{Tx} = X\Delta\varphi_{Rx} \tag{2.7}$$

and the receive phase is scaled by X. An illustration of a retrodirective phased array antenna receiving a signal at one frequency and transmitting at a different one is illustrated in Fig. 2-8 along with the scaling factor relations.

$$f_{Tx} = X f_{Rx} \rightarrow \varphi_{Tx} = X\,\varphi_{Rx}$$

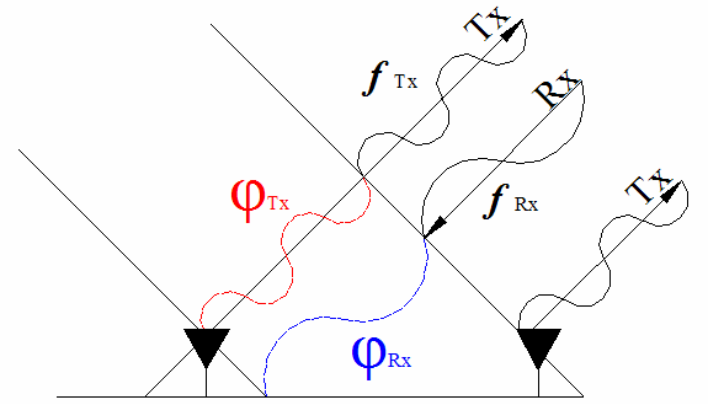

Fig. 2-8. Different f_{Rx} and f_{Tx} frequencies.

This illustrates that given the same array spacing and steering direction different wavelength dimensions translate to different phase lag and lead dimensions. In this case, the transmitting frequency is higher and has a shorter wavelength. Therefore to steer the transmitted beam in the direction of the incoming wave, the incoming waves phase lag must be translated to phase lead of the outgoing transmitted wave and scaled by a factor of X.

G. Previous Retrodirective Implementations

Previous retrodirective array architectures show the progression of technology and ideas of the retrodirective concept. They also aid in understanding the nuance of design performance and variation.

Van Atta Reflector

Besides the corner reflector the first modern retrodirective structure proposed suitable for microwave frequencies was the Van Atta reflector [15,19-20]. A diagram of the Van Atta reflector is shown below in Fig. 2-9. Similar to the corner reflector, the Van Atta reflector is a completely passive structure with no active components. Subsequently, there is no possibility for frequency translation or gain. The best performance achievable by Van Atta receivers is to retransmit the entire received back into the direction of the incoming source with no loss.

The Van Atta Array Reflector achieves retrodirectivity by transporting the phase lead of one side of the receiving aperture to the opposite side, and the phase lag of the opposite side to the side of received phase lead. All received phase lags are traded for transmit phase leads of equal amplitude, and all received phase leads are traded for transmit lags. This achieves phase conjugation and retrodirectivity.

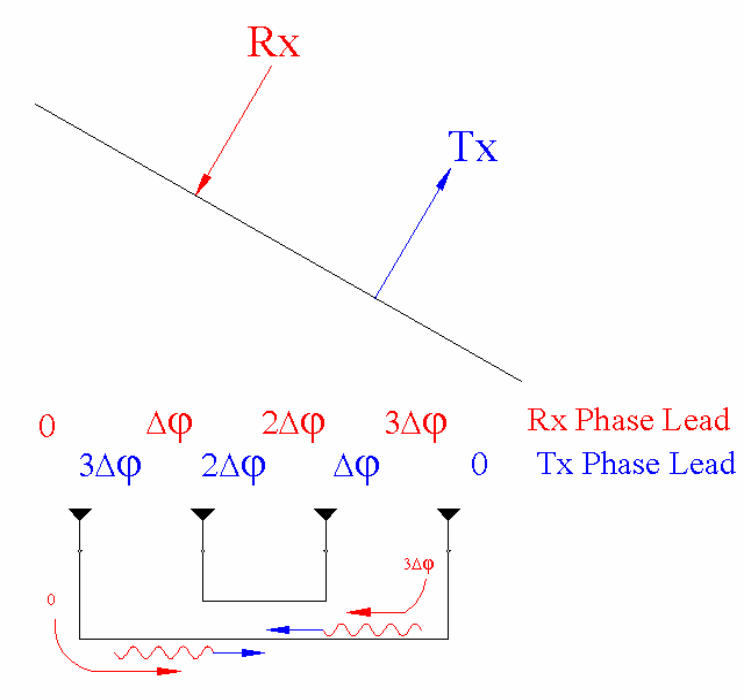

Fig. 2-9. Van Atta reflector.

Referring to Fig. 2-9, the right side of the leading aperture is impinged upon first by the incoming wave and so the output of its antenna element to the transmission line is phase leading. This phase lead is then carried to the correlating element on left side and transmitted. The analogous process occurs with the phase lag received on the left side. It is transported to the right and transmitted.

The Van Atta reflector is a good choice to maximize the radar cross section of an aperture with minimal demands on aperture geometry, fabrication, and cost. However, due to its passive and simple nature, it does not lend its self well to the application of modulation - not allowing any addition of power or information to the retransmitted signal.

Heterodyne Technique

Another method conceived by C. Pon is named the heterodyne technique [16]. This name was given due to its use of a lower sideband mixer. The phase conjugation is achieved by mixing the received signal of known frequency f_{Tx} with its double f_{Tx}. The received signal will be represented as $\sin(\omega_{TX} t + \Delta\varphi)$ where $\Delta\varphi$ represents the phase lag relative to the zero-element. The operation of mixing the incoming angular frequency and phase with its double can be mathematically represented as

$$\sin(\omega_{TX} t + \Delta\varphi) \cdot \sin(2\omega_{Tx} t) = \tag{2.8}$$

$$\frac{1}{2}\sin(2\omega_{Tx} t - \omega_{Tx} t - \Delta\varphi) + \quad \text{(lower sideband)}$$

$$\frac{1}{2}\sin(2\omega_{Tx} t + \omega_{Tx} t + \Delta\varphi) \quad \text{(upper sideband)}$$

Eliminating the upper sideband and simplifying the middle term gives

$$\frac{1}{2}\sin(\omega_{Tx} t - \Delta\varphi). \tag{2.9}$$

Though the amplitude of the output wave is scaled by ½, note that the phase has been conjugated and frequency has been returned to the receive frequency. This output can then be retransmitted through the same antenna element where it was received to achieve retrodirectivity. It is important to note that sine term in the first line of (2.8) representing the output from the local oscillator LO ($2\omega_{Tx}$) does not include a phase term. This is because the LO signal will be applied to all elements with identical phase.

Due to this consistency its phase term is arbitrary and is set to zero for the purpose of simplifying the presentation.

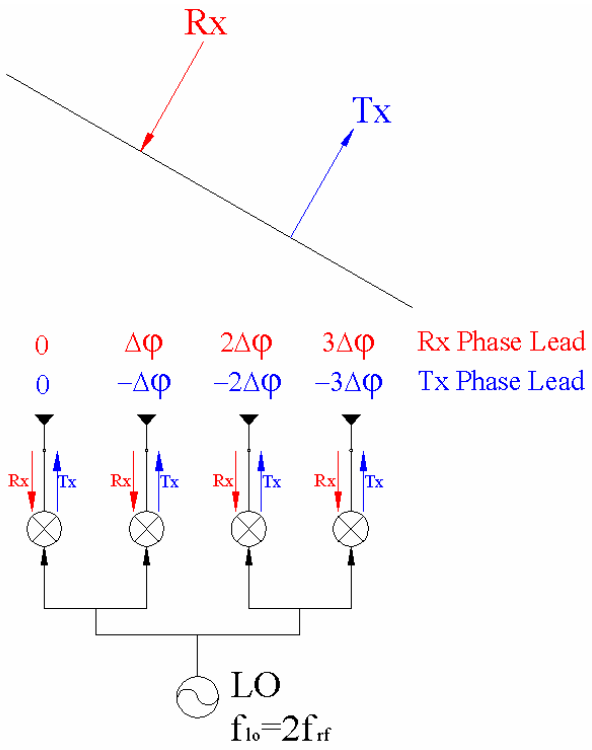

Fig. 2-10. Heterodyne technique.

Fig. 2-10 shows a simplified diagram of the heterodyne retrodirective process. Compared to the Van Atta the illustrated paradigm of phase conjugation is slightly different. Beam steering is most directly linked to phase gradient along the array, and not the phase magnitude of any single element. In the Van Atta array no sign change is used to represent the phase conjugation, instead the gradient of the positive phase value of the transmitted wave is shown to decrease from left to right. The representation of the heterodyne technique is best depicted by demonstrating no change of phase magnitude between transmit and receive but rather only a sign change. Note that in both cases the gradient is identical and the transmitted phase value decreases from left to right.

The heterodyne technique also uses active components. This enables it to provide signal amplification and gain. This is an important differentiating feature from the Van Atta reflector. It also provides the opportunity for modulation. Modulation can be achieved by modulating the amplitude, frequency, or phase of the LO input into the retrodirective system or gain elements in the transmitting chain.

Though opening the door to modulation, the heterodyne technique has some inherent limitations. Because the transmit and receive frequencies are the same, isolating the amplified and modulated output from the small input power is critical and difficult. A commonly proposed method to achieve isolation is to create a slight frequency offset between the output and input frequencies [17]. This offset allows the implementation of filters able to discriminate between the two different frequencies and to prevent output leakage into the input. Though aiding the problem of output/input isolation it creates a slight error in the steering phase delay. Relating the offset difference between the transmit and receive frequency as

$$f_{TX} = (1 + \gamma) f_{Rx} \tag{2.10}$$

introduces γ representing the offset factor. Using this relation and the definition of the phase scaling factor X in (2.7) necessary to achieve perfect retrodirectivity results in

$$X = (1 + \gamma) \tag{2.11}$$

The offset technique assumes γ gamma as negligible and approximates X=1. Published implementations demonstrate gammas as small as 0.01. The zero limit of γ is constrained by filter Q and fabrication accuracy. γ = -.01 translates to a 1% or 3.6° error in steering phase. Applications employing relatively broad beam array antennas may find such error acceptable. High gain, high efficiency, narrow-beam applications such as the SPS require much more accurate steering phase. The overall metric for acceptable

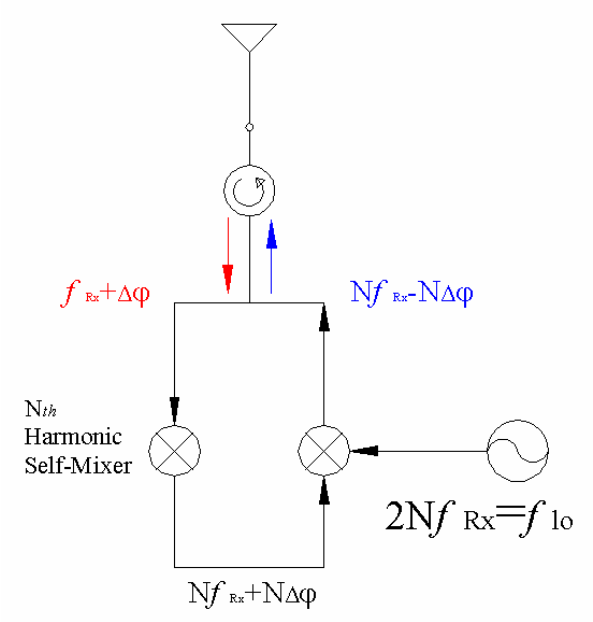

Fig. 2-11. Heterodyne with frequency translation element cell.

steering error would likely be chosen as a certain percentage of the array antenna's beam width. Steering error larger than the beam width would allow the error magnitude to steer the beam completely off target.

Channel bandwidth is another issue concerning the frequency offset heterodyne technique. Channels requiring an increased percent bandwidth would require an increase in γ necessary to achieve isolation. As γ increases, steering error does as well. After the steering error reaches the critical limit dictated by antenna beam width, increasing channel width would dictate a broader beam antenna array and decrease link efficiency.

Another method stemming from the heterodyne technique uses harmonic mixers to achieve integer multiplication of the incoming signal and is illustrated Fig. 2-11 [21]. This method multiplies the phase and frequency of the signal to be conjugated with itself using an Nth harmonic mixer. With this operation, the phase to be conjugated is scaled

by N. This scaled phase can then be negated and translated to the proper frequency by being multiplied with a local oscillator frequency of 2N. The lower difference product is selected using filters and retransmitted. The mathematic representation of the final step achieving phase conjugation is analogous to the operations demonstrated in (2.8) and (2.9).

PLL Antenna Array

Another method used to achieve retrodirectivity employs the use of a common device - a phase lock loop (PLL). The idea of controlling phased array antennas with PLL has been presented in [22]. Fig. 2.12 is taken from [23] and illustrates a recently developed retrodirective system. This system offers three operation modes. The control circuitry can be easily converted from retrodirective mode to both conventional phased array receive or transmit mode. It does not however offer the capability for phase scaling and frequency translation. It also uses the frequency offset technique with a $\gamma = 0.12$ limiting the retrodirective steering accuracy.

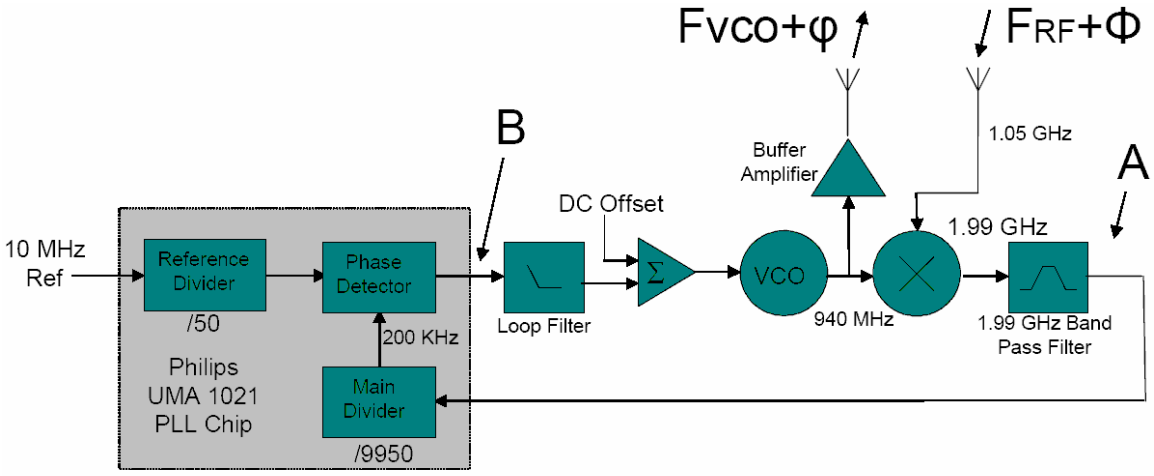

Fig. 2-12. PLL phase conjugation array cell [23] © 2004 IEEE.

Most of the blocks illustrated in Fig. 2-12 diagram are primarily related to PLL control. A PLL control system will be presented in detail in Chapter III. The circuit operations achieving retrodirectivity center around the upper sideband mixer and system

level PLL control concepts. The transmit and receive signals are mixed together passing the upper side band product. The upper sideband product term adds the frequency and phase components of the two mixer inputs. The mixer output at point A can be represented as

$$\sin(\ \omega_{Tx}\, t + \omega_{Rx}\, t + \varphi + \Phi\ ) \tag{2.12}$$

where f_{Rx} is 1.05 GHz, f_{Tx} is 940 MHz, φ is the phase of the transmitted VCO signal, and ϕ is the phase of the received signal.

The output signal of (2.11) is then divided into a frequency of 200 KHz and applied to a phase detector (PD). PD's measure the phase difference between two signals. The other signal applied to the PD is derived from a reference signal that will be fed to all conjugating elements. The phase of the reference signal is assigned φ_{REF}. The voltage output of the PD (at point B) will be linearly proportional to the input phase difference between (2.11) and the reference. It can be represented as

$$V_{PD}\ \propto \varphi_{REF}\ -(\varphi + \Phi). \tag{2.13}$$

The nature of PLL's in general is to control a VCO using feedback to maintain a fixed phase difference relation with the input reference signal such that

$$\varphi_{REF}\ -(\varphi + \Phi\ ) = \varphi(V_{DC}\ ) \tag{2.14}$$

where $\varphi(V_{DC})$ is the translation of the DC offset input in Fig. 2-12 into phase domain and is adjustable by the system user. Ideally all elements receive the reference 10 MHz signal with identical phase. Due to this commonality and mathematic relations of phase the reference may be arbitrarily assigned as zero phase, setting $\varphi_{REF} = 0$. The DC Offset voltage may also be adjusted to set $\varphi_{(VDC)}=0$. These two equivalences and (2.13) results in the familiar phase conjugate relation of

$$\varphi\ = -\Phi\,. \tag{2.15}$$

Reexamining Fig. 2-12 shows the incoming phase lag of $-\Phi$ is conjugated to outgoing phase lead φ thus achieving retrodirectivity.

H. Proposed System

A new retrodirective system has been designed employing a combination of previous methods. It is the first design that achieves arbitrary frequency translating retrodirective capability. Frequency translation has been demonstrated using the heterodyne technique but constrained by the discrete properties of scaling the phase using harmonic mixers. Up converting harmonic mixers constrain phase scaling factors to positive integers and subsequently the same constraint is placed on frequency translation. The proposed technique releases this constraint. It achieves this by scaling the gain of two linear PD's by different factors and incorporating them into a phase control loop. The ratio of the different PD gain factors determines the phase scaling. These gain factors are not discrete in nature and therefore release the phase scaling and frequency translation from any integer constraints

The concept of the proposed phase scaling technique is visually emphasized in the relationship between Figs. 2-13 and 2-14. Fig. 2-13 shows an ideal output from a linear phase detector. In the retrodirective system, the progressive phase shift between elements is represented by φ_o. The system measures the inter-element phase shift of the incoming pilot signal with a phase detector of gain K_{PD1} as seen in Fig. 2-14. The measured receive phase is translated to V_o according to the PD characteristic. This V_o is then referenced in the control phase loop of the transmitting circuitry which containing a phase detector of linear gain K_{PD2}. The mismatch of PD gains result in a phase scaling operation as desired.

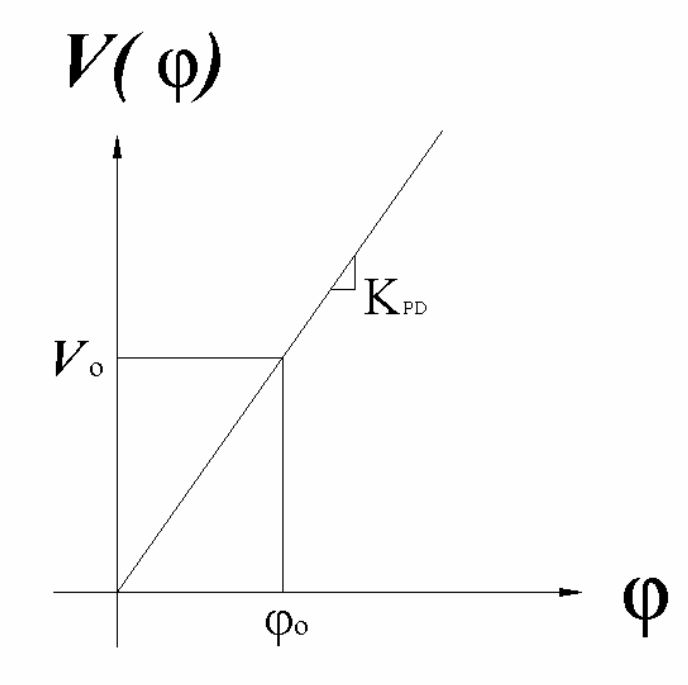

Fig. 2-13. Ideal linear phase detector output.

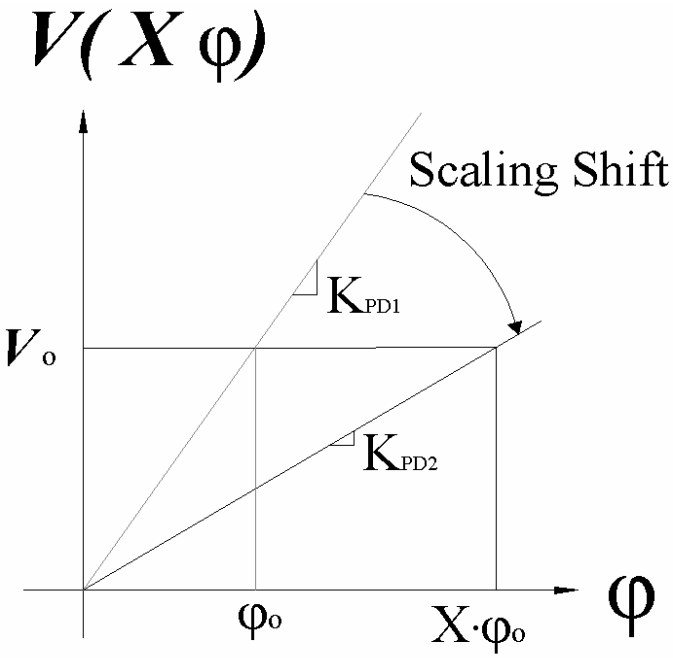

Fig. 2-14. Phase scaling operation on phase detector output.

The phase scaling factor X in Fig. 2-14 relates to the respective PD gains as

$$X = K_{PD1} / K_{PD2} \tag{2.16}$$

where K_{PD1} is the gain of the receive PD and K_{PD2} the gain of the PCL PD.

A system overview in Fig. 2-15 illustrates the basic principles and elements of the phase conjugating and scaling part of the array. In the top left, the incoming wave is incident upon the receiver's antenna. The antenna spacing and angle of the incident plane wave causes a phase difference φ_o between the two received waves. The two waves are then down converted by mixers to f_{IF1} by phase referenced LO signals. Any phase difference between the two LO signals applied to the mixers to down convert the received RF signals translates directly to phase conjugation uncertainty and error. Identical phase of LO inputs is critical. The mixer operation down converts the phase difference to a lower frequency within the operating range of common low cost electronics.

The two signals with the preserved phase relation are then applied to a linear phase detector outputting a voltage proportional to the phase difference. The phase detector translates the phase information from the angular domain to the voltage domain as depicted in Fig. 2-15 with the angular-voltage boundary. Using the presented method of PD gain mismatch, the phase is scaled and conjugated. This scaled and conjugate voltage reference is applied to a phase control loop and the DOA information once again crosses from the voltage to angular domain of frequency f_{IF2}. This rather low frequency f_{IF2} is then up converted to the transmit frequency f_{Tx} using an analogous mixing process to that of the down conversion. The LO mixer input phase coherency requirement is again rigorously maintained during the up conversion. Any phase incoherency is translated directly to phase steering error.

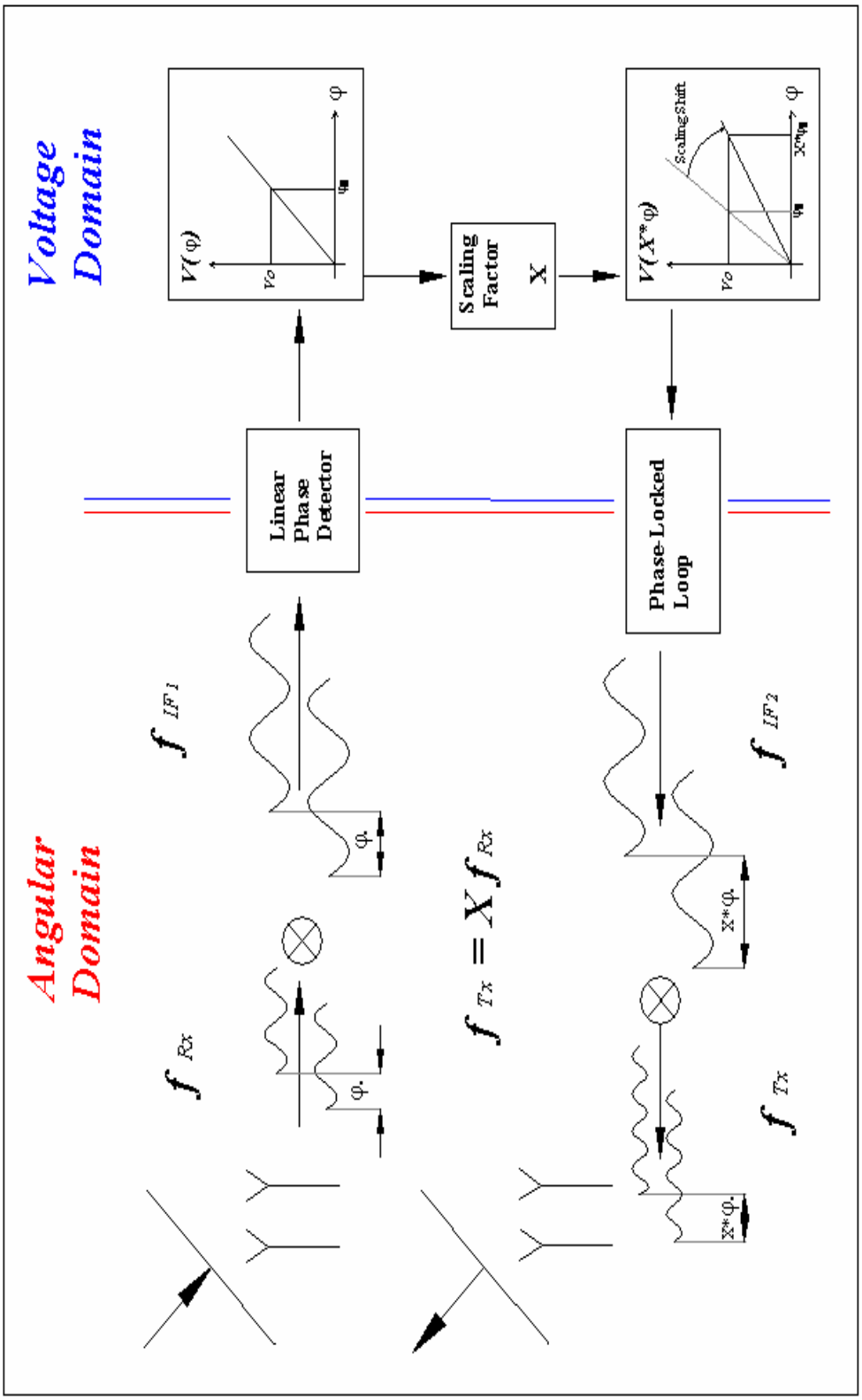

Fig. 2-15. Phase scaling PLL retrodirective concept diagram.

Fig. 2-16 shows the system with many similar blocks as Fig. 2-15, but takes a step toward the actual hardware system realization. The transmitting frequency of 5.8 GHz and receive frequency of 2.9 GHz is denoted, as well as the IF frequencies of both 10 MHz. It also asserts the presence of the down and up converting LO enforcing phase coherency between signal paths. It may be noticed that the transmit frequency is the first harmonic of the receive frequency and interpreted as an inherent system constraint of the type previously mentioned. The fundamental relation is purely incidental. The ratio of f_{Tx} to f_{Rx} could be any real positive number and is not constrained to integers.

The system also further depicts the phase control loop (PCL) and its subcomponents; the phase detector, summer, and VCO in the lower right of Fig. 2-16. These components work together achieving a negative feedback system stabilizing the phase relation between the 10 MHz LO reference and synthesized phase conjugated signal output from the VCO. The negative input from the loop PD into the loop summer indicates negative loop feedback and is necessary to achieve loop stability. In the loop, the boundaries between the voltage and angular domain are again noted in the figures.

I. Proposed Advantages and Disadvantages Comparison

The proposed method for retrodirectivity offers a number of advantages over other presented methods. As previously stated, it eliminates the integer constraint of frequency translating phase conjugation systems. It also poses no theoretical steering accuracy limit as do frequency offset methods with γ approximations. Compared to retrodirective methods performed entirely at RF frequencies, this technique is similar to the PLL Antenna Array.

It also gives users access to the pilot DOA information. This can be achieved by sensing the PD output from the receive elements measuring the inter element phase delay from the pilot signal. Also similar to the PLL Antenna Array method such an array could easily be changed to various modes of operation. Relieving the integer

constraint also lends itself to the capability of frequency hopping as security and diversity robustness tools. The proposed design system though more complex than others is still of the scale which could be fit onto a single monolithic chip and would be able to employ common silicon circuit design issues aiding in design and manufacturing cost minimization.

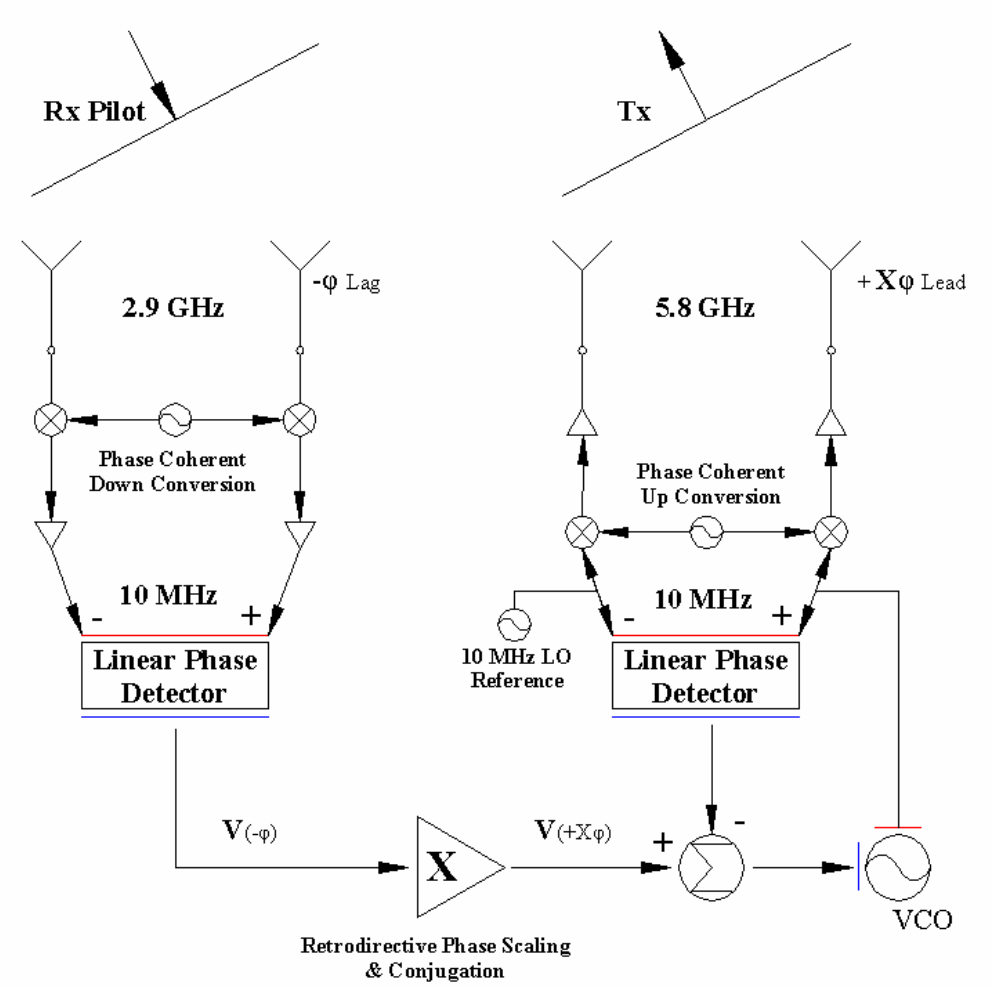

Fig. 2-16. Proposed retrodirective system.

Disadvantages include system complexity. The entirely RF designs such as published in [17] require comparatively few active components. The up and down

conversion of the proposed method require demanding design and performance of mixers and LO's. Currently the design involves a broad range of components and design considerations. Though a monolithic solution would greatly decrease power consumption, the design currently requires a significant amount of bias power.

CHAPTER III
PHASE CONTROL LOOP ANALYSIS

The phase locked loop (PLL) is a structure commonly employed in electrical systems [24]. In the proposed system, a modification of the classical PLL structure is used to achieve inter-element phase control of a retrodirective phased array antenna. This modification is applied to existing PLL theory and useful design equations are derived.

A. The Phase Control Loop

In its most common application, a PLL is used to obtain a fixed phase relation between what would otherwise be two uncorrelated oscillators by way of a feedback loop. Oscillators not phase locked will inevitably develop slight frequency perturbations and undeterminable phase relations over time. Most applications only require frequency or phase lock without the ability to control the phase relation of the two signals. For example, many mixer-based PLL structures acquiesce to a 90^o phase difference between the reference and controlled signal. This 90^o difference is fixed and not user adjustable.

A time-varying phase relation between the reference and controlled signal is required for real-time steering capability. A PLL structure including this modification and capability will be referred to more specifically as a phase control loop (PCL). A block diagram depicting PCL inputs and outputs as will be used in the proposed retrodirective system is depicted in Fig. 3-1. $V_{\Delta\varphi}$ is derived from a phase detector sensing the incoming pilot inter-element progressive phase shift. The output $\Delta\varphi$ vs. $V_{\Delta\varphi}$ is ideally linear with a slope K_{PD} as shown in Fig. 2-13. The proper $V_{\Delta\varphi}$ is required to achieve retrodirective steering. Recall that the phase scaling is achieved with a slope

mismatch between the PCL phase detector and incoming inter-element phase shift detector. The reference signal f_{Ref} is input into the PCL and serves as a phase reference between all array elements. The PCL produces the signal $f_{Ref} + \Delta\varphi$. This signal is frequency matched to f_{Ref} but has the inserted phase delay $\Delta\varphi$ necessary to achieve retrodirectivity. This phase delay $\Delta\varphi$ is linearly proportional to the input voltage $V_{\Delta\varphi}$ which is derived from the PD measuring the DOA inter element phase. In further illustrations $V_{\Delta\varphi}$ will be labeled as V_{CONJ}, but is here so labeled to emphasize its relation to the phase delay of the output signal.

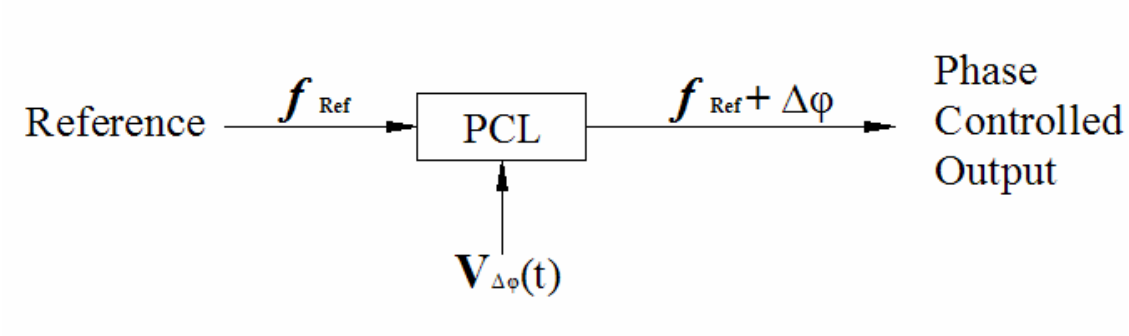

Fig. 3-1. Phase conrol loop input-output diagram.

Fig. 3-1 does not explicitly depict any feedback; it simply shows the inputs and output of the system. Fig. 3-2 illustrates the feedback structure of the loop. Recognizing the PLL component similarities and topology can be done somewhat intuitively. For example the loop blocks contributed by the phase detector operations may be easily discerned from those contributed by the VCO. In order to give full detail of the structure and process by which it is synthesized, a breakdown of the topology into individual modules will presented. The loop topology may be broken into three major components; the PD, Filter, and VCO.

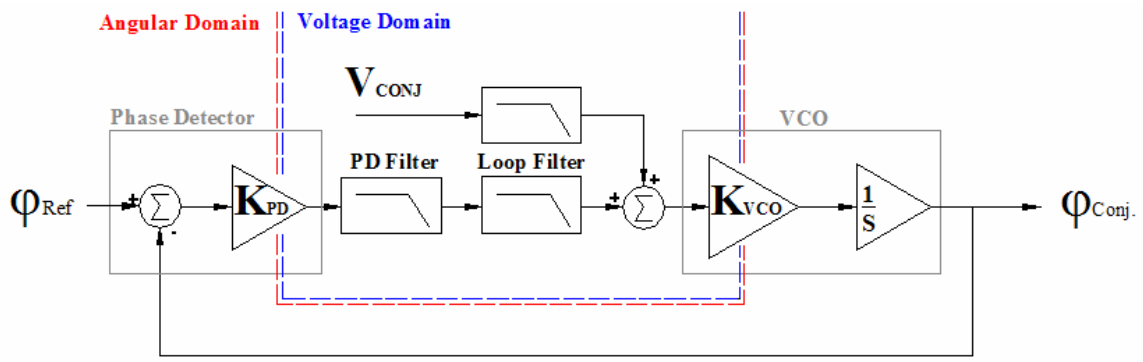

Fig. 3-2. Phase control feedback loop demarking the angular-voltage boundary.

B. Loop Components

Circling the blocks in Fig. 3-2 clockwise beginning from input of φ_{Ref} identifies the subcomponents of the loop. The phase detector embodies the first difference summer and the K_{PD} gain block of Fig. 3-2. The PD filter is represented by the low-pass block similarly named. The output from the PD filter and the conjugation voltage V_{CONJ} are input into the loop through the two Loop Filter blocks and summer. The VCO block include the VCO gain K_{VCO} and phase integrator $1/s$. $1/s$ is the La Place transform operator equal to integration in the time domain. The La Place transform is chosen to simplify the integration operation in the time domain to a simple scalar factor in the La Place domain. The VCO output is then fed back into the difference summer of the PD and achieves negative feedback and loop stability.

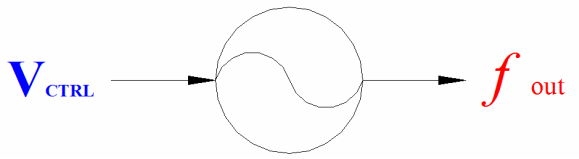

Fig. 3-3. VCO symbol.

VCO

An important concept related to the VCO is that of translating phase information between the voltage domain and the angular domain as depicted in Figs. 3-4 and 3-5. Since signal phase varies with a known relation due to target position, it may be considered information. Subsequently, the voltages that are derived from this phasing may be considered to contain information as well. The transition of this information from voltage to phase is demarked in Fig. 3-2 with the broken lines representing the angular-voltage boundary.

Fig. 3-4. VCO information translation.

The voltage controlled oscillator (VCO) translates a dc control voltage to a correlated oscillation frequency with the ideal characteristic of Fig. 3-5. When in phase lock, the reference frequency and VCO output frequency match. Subsequently, the VCO control voltage achieves steady state quiescence at the corresponding voltage V_q as may be noted in Fig. 3-5. In the case of the proposed system f_q = 10 MHz.

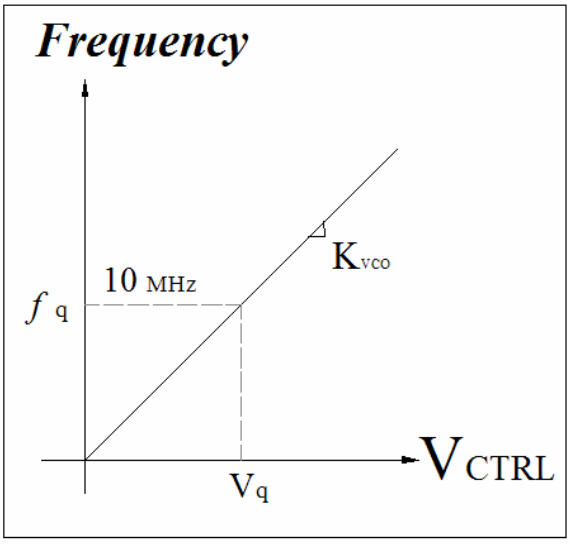

Fig. 3-5. Ideal VCO characteristic.

To implement the VCO model into loop design, the output frequency of the VCO block of Fig. 3-3 must be further simplified and translated to phase. This can be achieved by two main steps – 1) removing the acquiescence offset, and 2) utilizing the frequency phase relation.

Assuming phase lock, it is known that the steady state average control voltage of the VCO will be V_q. The feedback model presented in Fig. 3-2 only requires the variations of the control voltage and system perturbations about the quiescent point. To remove the added complexity of the steady state values and zero the VCO operation around its quiescent point, offsetting terms to the left and right of the VCO block are implemented. The VCO output frequency may be broken into quiescent steady state and transient components respectively using the representation of $f_q + f_\Delta$. The components of the control voltage may be similarly represented as $V_q + V_\Delta$. This achieves zero mean variables f_Δ, and V_Δ. The above is achieved with the block manipulation of Fig. 3-6.

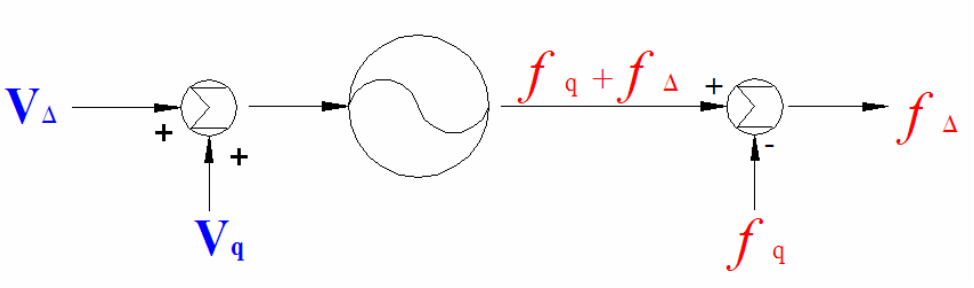

Fig. 3-6. Removing acquiescence offset from VCO model.

The phase-frequency relation is:

$$\varphi = \int f\,dt \tag{3.1}$$

as may be depicted as in Fig. 3-7.

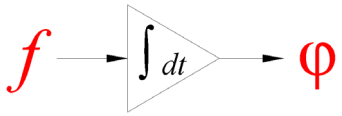

Fig. 3-7. Inputting frequency into an integrator outputs the signal phase.

Applying the La Place transform as defined in [25] to (3.1) gives

$$\varphi = \int f\,dt \xleftrightarrow{LaPlace} \varphi = \frac{f}{s}. \tag{3.2}$$

Using La Place representation of the integrating operation reduces its complexity from time integration to simple scalar multiplication by $1/s$. Here s represents the La Place operator analogous to the Fourier $j\omega$ term.

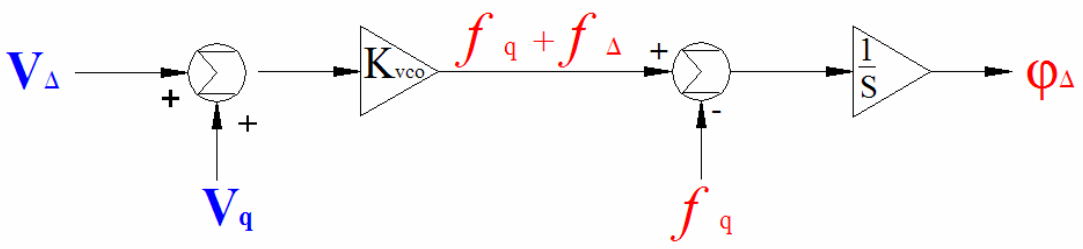

Fig. 3-8. Expanded VCO control block.

The VCO block may now be expanded to Fig. 3-8. The circular oscillator symbol has been altered to represent a simple scalar operation multiplying $V_q + V_\Delta$ by K_{vco} translating it to the frequency domain. K_{vco} is the gain of the VCO and has units of Hz/V. Noting the relation

$$V_q \cdot K_{vco} = f_q. \tag{3.3}$$

If one allows the $+V_q$ term left of the K_{vco} scalar block to be cancelled with the $-f_q$ term on the right. This reduces the VCO control block to its final form as is represented in the PCL loop of Fig. 3-2.

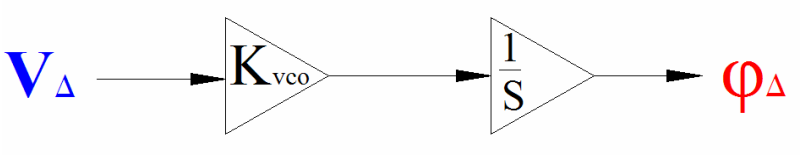

Fig. 3-9. Simplified VCO block.

Phase Detector

The loop representation of the PD is shown in Fig. 3-9. The operations it performs are comparatively simple to that of the VCO. The detector subtracts the phase difference between the reference and VCO feedback. The difference is scaled by the appropriate PD gain K_{PD}. For the proposed realization, the phase detector is an XOR

which mixes the two discrete inputs and outputs a pulse train. The output duty cycle varies linearly with phase difference and toggles between V_{Hi} and V_{Lo}. The frequency is also divided down by a factor of 8 before mixing. The frequency division multiplies the phase range of the XOR type mixer with undivided inputs by the same factor. The frequency division also achieves a perfect 50% duty cycle of the divided input to the XOR. 50% duty cycle is necessary to achieve the full linear range of the PD. The subsequent PD gain using the chosen detector type is

$$K_{PD} = G\frac{V_{hi} - V_{lo}}{8\pi} \tag{3.4}$$

having the units of (Volts/Radian). K_{PD} is adjusted by amplifying the pulse output or time averaged pulse output as is done in the proposed method and shown in Fig. 3-10. This variable amplification is symbolized by the *G* term in (3.4) and is the means by which the phase is scaled appropriately to achieve frequency translation.

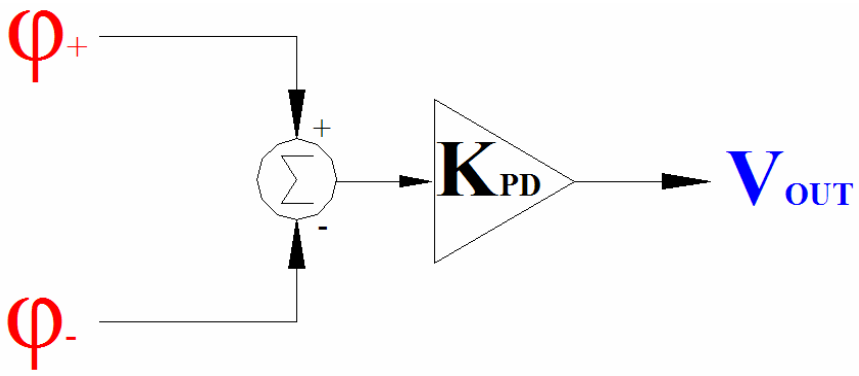

Fig. 3-10. Phase detector control representation.

The PD translates the phase information in the angular domain to the voltage domain as emphasized in Fig. 3-11. This performs the counter domain transition as compared to the VCO and allows the feedback loop to be closed. It is again worth noting that proposed implementation uses two PD's to achieve DOA detection, phase control, and frequency translation. Phase scaling is enabled by the ratio of two different

phase detector gains. Both the down conversion of the DOA information to baseband that is accessible to the user as well as retrodirective phase conjugation can not be achieved with out using two PD's. In the PLL Antenna Array [23] as presented in Chapter II, only one PD is used. The result is that it only achieves retrodirectivity and does not convert the DOA information to baseband accessible to the user, nor does it enable the phase and frequencies to be scaled.

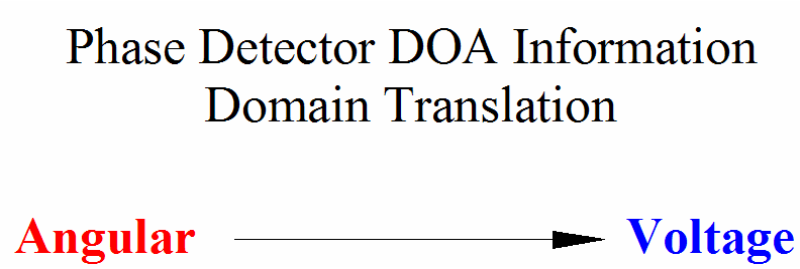

Fig. 3-11. Phase detector information domain translation directionality.

Loop Filter

The loop bandwidth is determined by the loop filter. The loop filter is needed to isolate the VCO control voltage from the high frequency content of the output pulses from the mixer. The phase noise of the locked signal will increase as the amount of high frequency content of the XOR output is allowed to pass to the VCO. In this case, loop bandwidth is traded to decrease the phase noise of the locked signal. The filter design requires selecting loop values such as bandwidth and damping coefficient of the system. These values in turn determine PCL phase noise, stability, and linearity. Several choices for loop type and design have been published presented in literature [23]. This implementation has proposed a new hybrid loop filter structure and design equations. The loop filter can be divided into two cascaded passive and active sub-filters. The passive component filters the pulse train output from the PD and will be referred to as

the PD Filter. The active element is the loop filter as proposed in [22] and will be referred to as the proper Loop Filter.

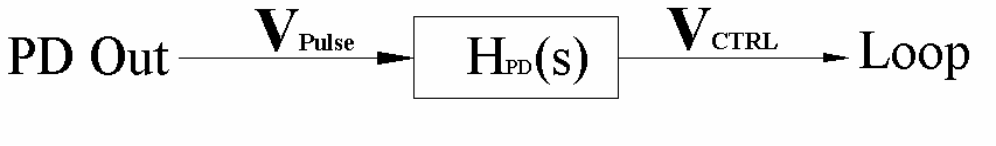

Fig. 3-12. PD Filter control block.

The PD filter averaging the PD output pulse train is a classic lag/lead network. The block and circuit realizations are illustrated in Figs. 3-12 and 3-13 respectively. It is cascaded directly behind the phase detector. The La Place transform of the network transfer function is

$$H_{PD}(s) = \frac{1 + s\tau_{PD2}}{1 + s\tau_{PD1}} \tag{3.5}$$

where

$$\begin{aligned} \tau_{PD1} &= C_{PD}(R_{PD1} + R_{PD2}) \\ \tau_{PD2} &= C_{PD}R_{PD2}. \end{aligned} \tag{3.6}$$

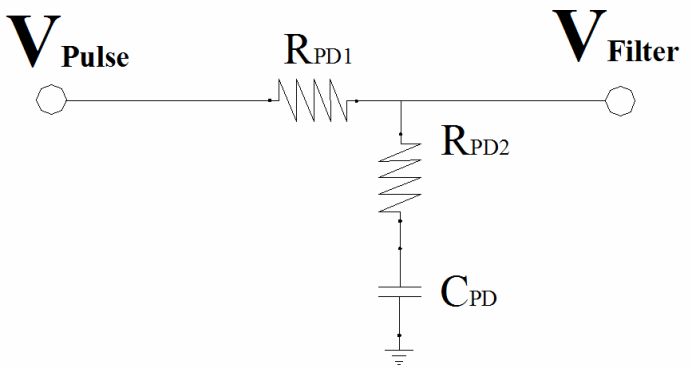

Fig. 3-13. PD Filter – filters the pulse train output from the phase detector.

The filter has a transfer function with one pole and one zero and has the constraint that $\tau_2 > \tau_1$. A more detailed presentation of the theory supporting both this and following active filter may be found in [26]. The active filter in Fig. 3-14 is a voltage integrator and employs the use of an op amp. It has two inputs; V_{PD} is the output from the loop PD Filter, V_{CONJ} is the filtered output from the receiver PD and contains the DOA information.

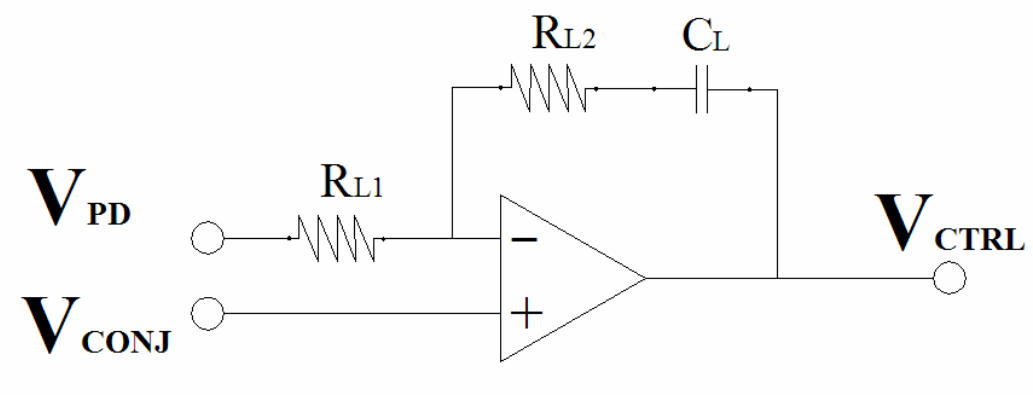

Fig. 3-14. Loop filter – voltage integrator with two inputs.

The two different inputs translate differently to the output. Therefore the block representation of the Loop Filter must discriminate between the two inputs using two different transfer functions as shown in Fig. 3-15. Using superposition, the two different inputs upon the block output are summed.

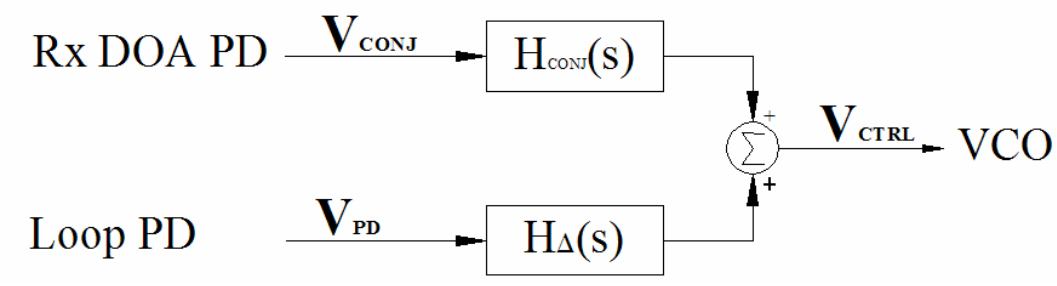

Fig. 3-15. Loop filter block representation, two transfer functions are required because there are two inputs with different gains.

$$H_{\Delta}(s) = \frac{-(1+s\tau_{L2})}{s\tau_{L1}} \tag{3.7}$$

$$H_{CONJ}(s) = \frac{1+s\tau_{L3}}{s\tau_{L1}} \tag{3.8}$$

$$\begin{aligned} \tau_{L1} &= C_L R_{L1} \\ \tau_{L2} &= C_L R_{L2} \\ \tau_{L3} &= C_L (R_{L1} + R_{L2}) \end{aligned} \tag{3.9}$$

C. Loop Transfer Function

The necessary relations have now been presented to derive the open and closed loop transfer functions and determine stability. There are two inputs into the loop and one output. To simplify the analysis and relate the output to the one input at a time, one input will be assumed zero as the other's transfer function is obtained. This technique is used in [23].

The output phase as a function of reference phase will be examined first. Assuming zero input from V_{CONJ} simplifies Fig. 3-2 to a unity feedback loop with and closed loop gain of

$$H_{\varphi}(s) = \frac{\varphi_{Conj.}(s)}{\varphi_{\mathrm{Re}f}(s)} = \frac{H_{\varphi o}(s)}{1+H_{\varphi o}(s)}. \tag{3.10}$$

$H_{\varphi o}(s)$ is the open loop gain and defined as

$$H_{\varphi o}(s) = K_{PD} H_{PD}(s) H_{\Delta}(s) K_{VCO} \frac{1}{s} \tag{3.11}$$

where K_{PD}, $H_{PD}(s)$, and $H_{\Delta}(s)$ are defined in (3.4), (3.5), (3.7) respectively and K_{VCO} is the VCO gain as shown in Fig. 3-4. Assuming zero input from φ_{Ref} and manipulating the loop blocks results in

$$H_C(s) = \frac{\varphi_{Conj.}(s)}{V_{CONJ}(s)} = \frac{H_{co}(s)}{1 - H_{co}(s)H_{cf}(s)}. \tag{3.12}$$

where

$$\begin{aligned} H_{co}(s) &= H_{CONJ}(s)\frac{K_{VCO}}{s} \\ H_{cf}(s) &= K_{PD}H_{PD}(s)H_{\Delta}(s)H_{CONJ}(s)^{-1} \end{aligned}. \tag{3.13}$$

$H_C(s)$ is the frequency response of the output phase versus the conjugation voltage $V_{CONJ}(s)$. This relation is important to consider if the target direction is expected to vary quickly and also if any modulation will be imposed upon the output through the means of modulating the conjugation voltage.

It is important to note that as $V_{CONJ}(s)$ and φ_{Ref} approach a virtual DC value of sufficiently low frequency, the relation

$$H_{\varphi}(s) \xrightarrow{s \to 0} 1 \tag{3.14a}$$

$$H_C(s) \xrightarrow{s \to 0} \frac{1}{K_{PD}} \tag{3.14b}$$

results. (3.14a) confirms that the output phase tracks the input phase. (3.14b) confirms that the output phase difference is linearly proportional to the conjugate voltage V_{CONJ} times the phase detector gain.

The transfer functions derived will be used to verify stability when designing the loop elements. They will also guide and determine the selection of component values and time constants. These functions are of third and fourth order and are subsequently difficult to solve for. A Matlab program using numerical techniques will be used to determine loop zeroes and poles as well as plot the individual loop frequency responses.

CHAPTER IV
PHASE CONJUGATION DESIGN

As has been shown, there are a number of steps and system components required to achieve the proposed method of phase conjugation. The system was presented in Chapter III from the control theory point of view necessary to design for stability. It was shown to be composed of numerous subcomponent blocks in Chapter III as well as Chapter II. The implementation of these blocks and components are here presented.

A. Transceiver Architecture

The transceivers used to achieve retrodirectivity as proposed must posses some qualities uncharacteristic of normal architectures. These qualities center around the need to synthesize each elements RF signal individually while protecting the phase relation between the transmit elements. Phased array architectures normally achieve phase shifting and subsequently beam steering by inserting an adjustable phase delay between the RF modulated signal and the radiating elements. This is commonly achieved by switched delay lines, varactor-tuned phase delay filters, or less commonly with piezo-electric transducers [27]. In all the above implementations the RF signal is synthesized and modulated in one location and then sent to the transmitting elements through the phase shifters. Though commonly amplified before being transmitted, it is rarely translated in frequency after the phase adjustment.

Since the proposed method converts the phase information to baseband, the transmitted and received signals must be down and up converted between the receiving and transmitting elements. As can be observed from (2.8), any arbitrary phase relation addition from the LO signals applied to the conversion mixers will add arbitrary and

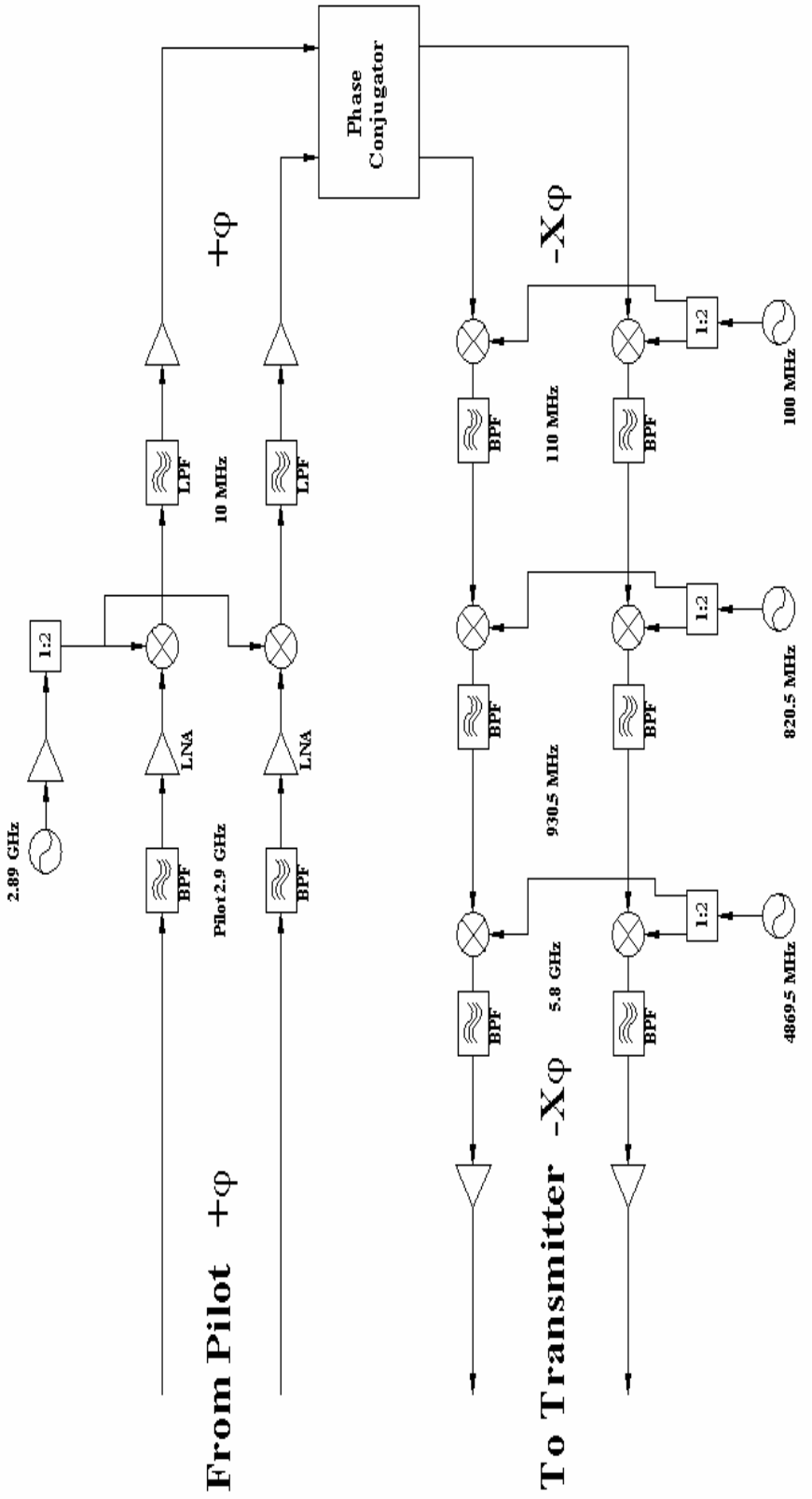

Fig. 4-1. Transceiver architecture for proposed phase conjugation method. Simultaneously synthesizes the RF signal while protecting phase relation by maintaining LO phase coherency.

corrupting phase relation between the phased array elements. The transceiver architecture in Fig. 4-1 uses phase coherent converting mixer LO's to achieve inter-element synthesis phase integrity. The pilot signal with the phase relation determined by the DOA is received at 2.9 GHz and then down-converted directly to 10 MHz with a lower-sideband mixer and 2.89 GHz LO. The phase conjugation is performed and two 10 MHz signals are output with proper phase relation to achieve retrodirectivity. The phase is scaled by the X factor as defined in (2.6). The phase conjugated waveforms are then up converted to 5.8 GHz in three stages using upper-sideband mixers and 100 MHz, 820 MHz, and 4.87 GHz respectively.

In both the down and up conversion to and from 10 MHz, the mixing is done at each stage in the parallel conversion process by splitting the output of a single LO in two. Each conversion path subsequently inserts identical phase delay into the signal. Recall that the phase detector senses only the difference between the two respective phases. This determines that the common phase differences inserted in the down and up conversion path cancel each other and are inconsequential to beam steering.

B. Phase Detector

Using a linear PD or at least a linear region of a PD is necessary to achieve phase conjugation with the proposed technique. An XOR type detector was chosen due to its entirely linear output characteristic. Another linear PD type investigated was the flip-flop based phase frequency detector (PFD) due to its similarly linear output. It is conceivable however to use a nonlinear PD to achieve phase conjugation in a linear region of the output. Mixer type PD's have a sinusoidal output characteristic which can be approximated linear in limited regions and achieve phase conjugation in the same method as is presented in this thesis. The design implemented presented in Fig. 4-2 will be discussed moving left to right along the transition from the angular to voltage domain.

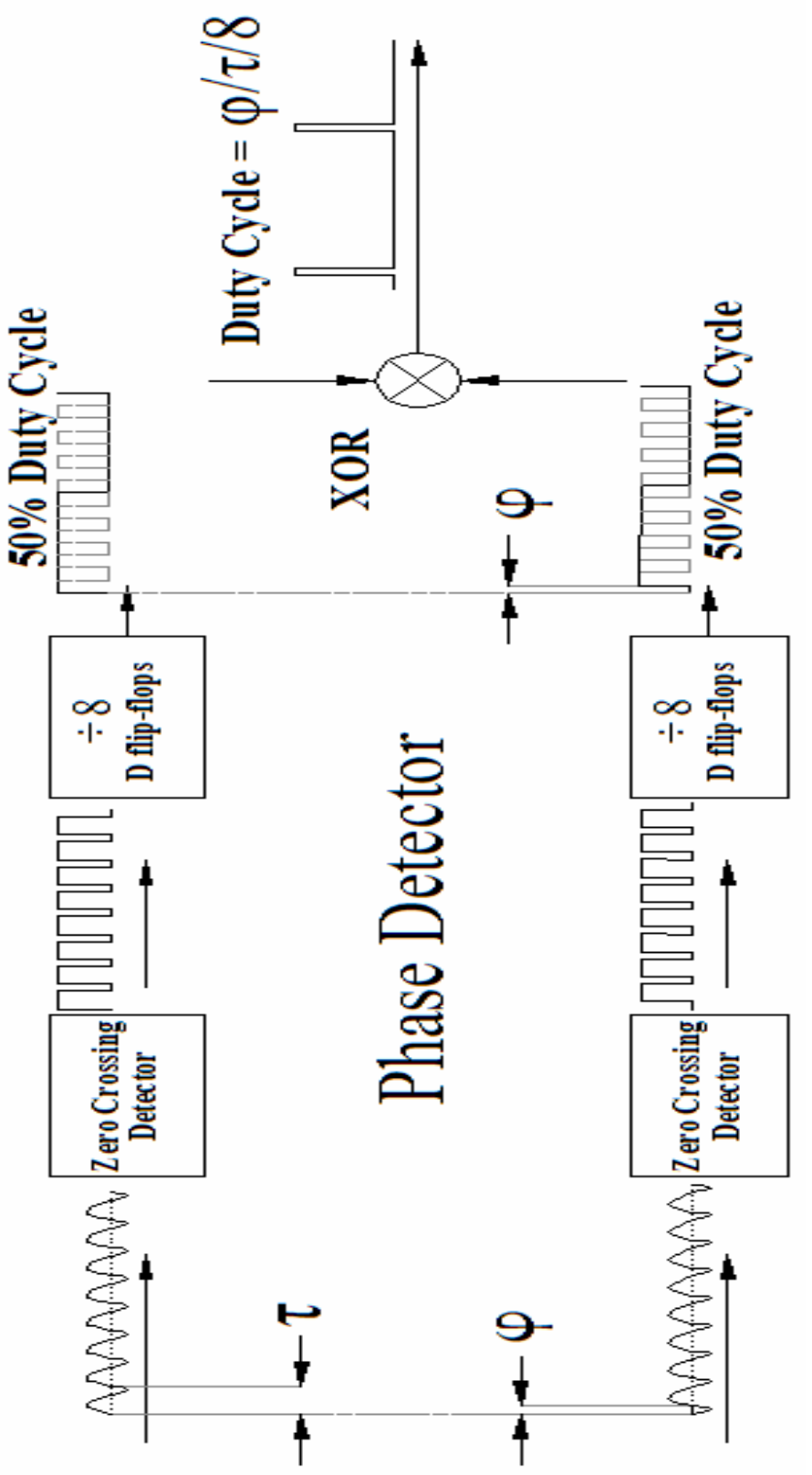

Fig. 4-2. Phase detector block diagram illustrating frequency division and duty cycle linearly proportional to φ.

Signal Shape

The first noteworthy element of Fig. 4-2 is the waveform shape coming into the PD from the left. After down-conversion and due to modulation, the shape of the waveform may not be perfectly sinusoidal. It is also clearly not in the digital form ready to be input into an XOR gate. As implemented in [22], it is possible to directly input the incoming waveform into a TTL logic device such as a D-type flip-flop. However the transition of the incoming waveform is comparatively slow to the rising edges of TTL devices. The states of the TTL devices are voltage driven. The range for transition voltage levels as specified by the device manufacturers varies greatly. This leaves the TTL trip point at a rather arbitrary and indeterminable position in the incoming waveform.

In addition to the possibility of the incoming wave being modulated, setting the transition point at the waveform zero-crossing was determined preferable. The zero crossing point can be described as the point in time when the waveform value passes the DC average of the incoming waveform. For a perfectly AC coupled waveform as is implemented, this average is always equal zero. Regardless of modulation scheme, this stays fixed relative to the waveform phase. It is also important because the incoming waveforms might have mismatched amplitudes. This mismatch would require special compensation should the trip points be chosen at a non-zero value.

Zero-crossing Detector

The zero crossing is detected with a comparator. The output of the comparator is required to be interface directly with TTL devices. The detector is supplied with the same power voltage as the TTL devices. The accuracy of the crossing detection is also important. Due to the possibly small amplitude of the incoming waveform, any comparator offset and detection error could translate into large phase mismatches between the two signals. The crossing accuracy of the chosen comparator was accurate

to only a few millivolts. Of secondary but considerable importance was the output bandwidth of the comparator.

Having an adequate output slew rate and minimal transition time is also important for detecting phase accuracy. It is noteworthy that in the PD section of the phase conjugation system, all time uncertainties translate to phase error using the metric of the 10 MHz period, 100 ns. Further details concerning this component as well as all the components used in the phase conjugation circuitry can be viewed in Appendix B including component values, component packages, and component manufacture numbers.

Flip-Flops and Frequency Division

Continuing the path in Fig. 4-2 from left to right, the frequency of the incoming signals have been converted to 10 MHz square-waves, these waveforms are divided by a factor of 8 before being input into the XOR. The division is done for three main reasons; 1) it achieves 50% waveform duty cycle, 3) increases the PD detection range and 3) it eases the bandwidth requirements of the circuitry following the PD. As can be visualized by closely examining the square-waveforms in Fig. 4-2, frequency division using flip-flops gives a waveform output with a perfect 50% duty cycle. This is required when using XOR type phase detectors since their states are voltage driven and not edge driven as are phase frequency detectors. Phase-voltage characteristics of XOR PD's driven by waveforms not having 50% duty cycle relinquish a large amount of the phase detection range at the characteristic edges.

Dividing the frequency by a factor of 8 increases the phase range of the PD by a factor of 8. An increased phase range helps improve the lock-time of the phase control loop as well as help maintain loop stability. Also, it is necessary to achieve a bipolar linear phase range of $\pm\pi$ about the zero phase point. The shape of the XOR PD with no preceding phase delay has the output characteristic of Fig. 4-3. The range of such a PD

would not be able to accommodate for a full ±π range needed for beam steering. Preceding the PD with frequency division expands the range as shown in Fig. 4-4 to accommodate for the necessary range. An operating point at 4π as depicted in Fig. 4-4 would achieve a virtual zero phase difference since 4π is a periodic multiple of zero phase. A 4π operating point would also have a linear range of ±4π in which to operate.

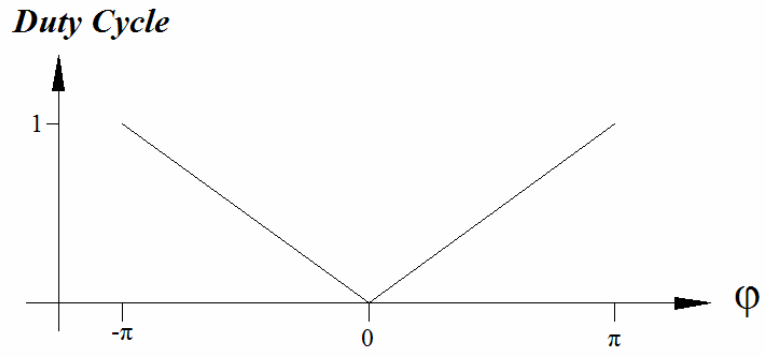

Fig. 4-3. XOR PD with no preceding frequency division output characteristic – does not possess sufficient linear operating range.

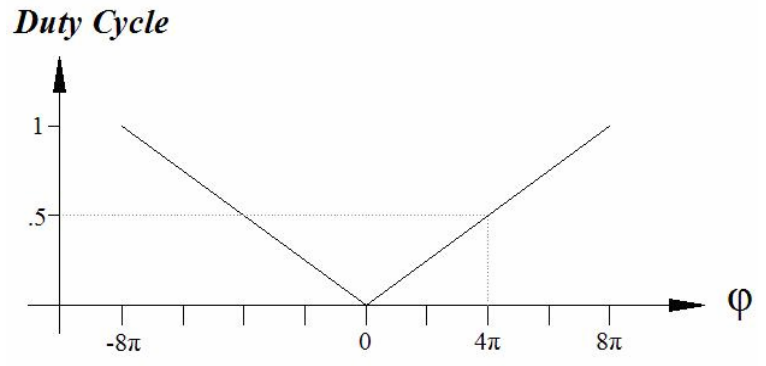

Fig. 4-4. XOR PD with preceding frequency division – possesses a ±4π linear operating range about φ=4π.

Dividing down the input waveform of the XOR PD has the effect of dividing down the frequency of the output pulse train. This pulse train will be a square wave with a duty cycle proportional to the phase difference. The higher the frequency of the output pulse train, the higher the bandwidth required of the active components that

follow the XOR in the PD. Asymmetry was observed between the following active PD components up currents and down currents due to the abrupt up and down voltage of the output pulses. This asymmetry was suspected to be a large contributor to the nonlinearity of the PD and PCL. By increasing the amount of time between the up and down pulse changes, the negative effects of the asymmetry on the PD and PCL linearity was decreased.

XOR

The XOR operation is achieved along with the third of the tree flip-flop stages (achieving division by a factor of 8) using the commercial component AD 9901 from Analog Devices. This device was chosen due to its final on-chip division stage and integration. An unanticipated disadvantage of this implementation is that the V_{hi} and V_{lo} output from the XOR function are very dependant upon the bias power voltage V_{cc}. Therefore, if there are slight drifts or voltage differences of the component's V_{cc}, there will be corresponding offset and gain errors in the filtered and amplified output. This can be overcome by creating an independent regulator using a voltage reference and feedback to control the power voltage of the 9901.

Pulse Filter

The pulses output from the XOR are filtered using a simple lag lead network as shown in Fig. 3-13. The network is realized using two discrete 0805 package resistors and a 6032 package tantalum capacitor. The values for these components were determined using a Matlab program employing the control theory equations of Chapter II. This program will be further presented later in this chapter. The Matlab program in its entirety is presented in Appendix C. It should be noted that the filter, as well as the frequency division performed by the flip flops help reduce the bandwidth requirement of the following buffer, gain, and offset stages. However, the filter as might be expected does not remove all high frequency components of the signal, it only attenuates them.

Gain and Offset Adjustment

After the filter, the pulse output goes through three stages employing the use of op amps to buffer and condition the pulse signal for the feedback loop. Fig. 4-5 shows the buffer stage, voltage offset adjustment stage, and gain adjustment stage. All the op amps achieve precision OP07 standard specifications - meaning there are extremely low offset voltages between the inverting and non-inverting nodes. The buffer stage serves simply to propagate the PD output the following stages without loading down the output from the PD filter. The value of the single resistor in this stage is matched to the input resistance seen when looking into the non-inverting node of the op amp. This helps to minimize the offset between the inverting and non-inverting nodes.

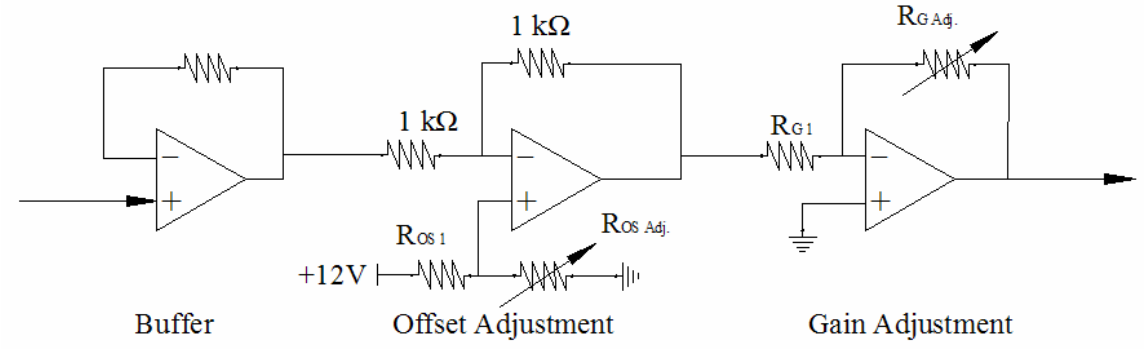

Fig. 4-5. Conditioning stages for pulses output from the PD.

The offset adjustment stage sums an offset correction voltage as determined by adjusting the offset adjustment variable resistor. Since the pulse train from the PD is uni-polar and a bipolar operating region around the zero phase point is desired, the offset voltage summed cancels exactly the zero phase voltage of XOR characteristic. This shifts the output from the PD as shown in Fig. 4-6.

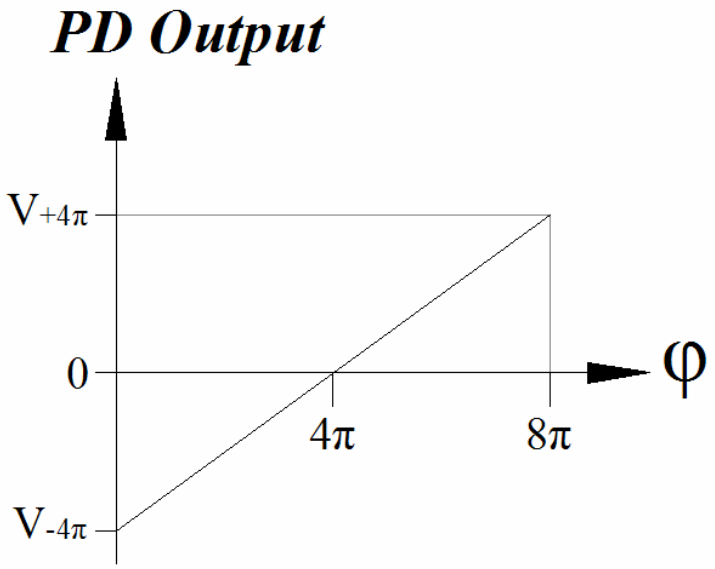

Fig. 4-6. Offset adjustment operation shifts the output voltage due to the PD pulses so that the chosen zero phase relation outputs zero volts.

The gain (slope of the linear function of Fig. 4-6) is then scaled appropriately by adjusting the variable resistor in the final gain stage. It is this stage alone that will determine the phase and frequency scaling of the phase conjugation. This gain can also compensate for slight mismatches in of V_{hi}-V_{lo} difference between the two XOR outputs used for phase conjugation. The gain of the PD in the PCL is set to half that of the PD sensing the received pilot phase difference.

C. VCO

A simple varactor tuned Colpitts voltage controlled oscillator was designed and fabricated. A schematic and image of the VCO can be found in Appendix A as well as the specification of its components in Appendix B. Due to the simple design used and the non-linearity of the varactor diode capacitance, output characteristic of the VCO presented in Fig. 4-7 is highly non-linear. It is known that the operating point will be 10 MHz. The assumption that when in lock the VCO output will not move far from the prescribed operating point allows the gain (slope of the characteristic curve of Fig. 4-7)

to be approximated and linearized to the slope about 10 MHz. The resulting VCO gain is 0.2 MHz/V. This gain may by observing the trend line equation in Fig. 4-7. Where the VCO gain equals the slope *m* of the slope-offset form *y*=*mx*+*b*. This trend line passes through the two measured points nearest the expected operating frequency. The VCO gain experimentally measured here will be used in the equations derived from control loop theory to design the PCL loop filter component values.

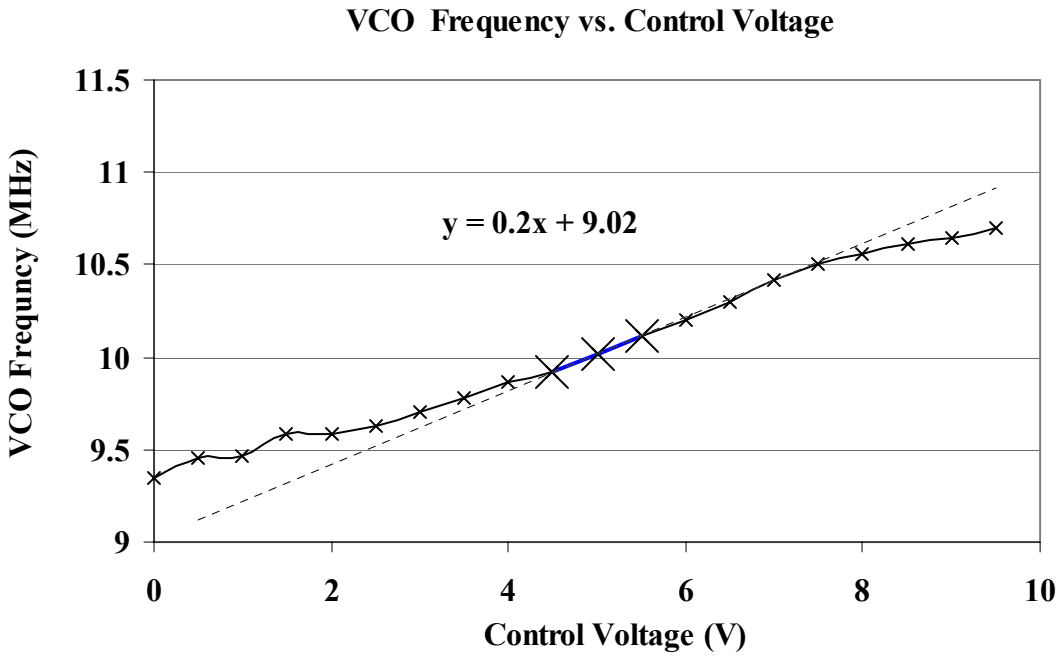

Fig. 4-7. Output characteristic of fabricated VCO - the VCO gain around the 10 MHz operating point is indicated with the dotted linear trend line.

In place of the fabricated VCO, an Agilent 33220A waveform generator was initially used in frequency modulation mode to act as the VCO. This gave the advantage of a highly linear frequency vs. control voltage characteristic as well as the ability to adjust the VCO gain in circuit to experimentally search for optimal VCO gain. It was subsequently determined that the VCO performance was not a major constraint on PCL

performance. Large variances in the waveform generator VCO gain produced no large performance enhancements as compared to the fabricated VCO.

D. Loop Filter Design

The loop filter topology is shown in Fig. 3-14. The same op amp was used as in the previous active pulse train conditioning stages. Determining the values of the resistors and capacitor of the loop are the main design task for this subcomponent of the system. The VCO gain and PD gain for the PCL loops have been previously determined and required to design the loop filter to achieve stability. The loop transfer function is third order as is presented in (3.10) and difficult to simultaneously solve for all the component values. A novel method of choosing $\tau_{L2}=\tau_{PD2}$ allows great simplification and reduces the loop to second order. Where $H_{\varphi}(s)$ in (3.10) reduces to

$$H_{\varphi}(s) = \frac{2\eta\omega_n s + {\omega_n}^2}{s^2 + 2\omega_n s + {\omega_n}^2} \tag{4.1}$$

where the loop bandwidth ω_n can be approximated as

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{\tau_{L1}}} \tag{4.2}$$

and the damping constant η equals

$$\eta = \frac{\tau_{PD1}\omega_n}{2}. \tag{4.3}$$

A Matlab program was written to determine the necessary component values for the loop filter design and is available in Appendix C. A loop bandwidth of $\omega_n = 2\pi\cdot 2000$ was chosen with $\eta=2$, $C_L= 400$ nF, $C_P=4.7\mu$F. Table 4.1 lists the components and values for the PD filter as well as the loop filter output from the Matlab program and were implemented in the system build.

E. Fabrication Method

The designs were first verified with spice simulations. They were then realized using Protel 2004 printed circuit board (PCB) software tools. The schematics were first entered into the Protel schematic editor. The manner in which the schematic was entered took advantage of the multi-channel design capabilities of the layout software. A singe channel is only entered once into the schematic and can then be called numerous times without the need to repeat the same design.

The schematic was then translated to layout. The multi-channel capabilities were again utilized to layout the repeated sections of the design only once. This layout was then mimicked for other like sections and saved the time of repeating the same layout. The design was laid out and machine milled on a double sided PCB board. The process specified a minimum copper clearance was 8 mils with a minimum trace width of 8 mils as well. Thru-hole copper-plated vias were drilled and plated for inter-layer connectivity. The bottom layer was reserved for ground only routing signals on it when absolutely necessary. The grounding of different regions of the modules were specially connected to achieve minimal noise coupling between different circuit regions. For example, the ground regions between the PD and the control loop circuitry are connected only be a sing strip underneath the PD pulse output trace that crosses the two regions' boundaries.

CHAPTER V
PHASE CONJUGATION PERFORMANCE

The fabricated components were integrated and phase conjugation performance was measured. Five performance measurements of the phase operations at 10 MHz were obtained; 1) PD linearity, 2) PCL linearity, 3) direct phase conjugation, 4) phase-lock jitter, and 5) PCL step response.

A. Measurement Setup

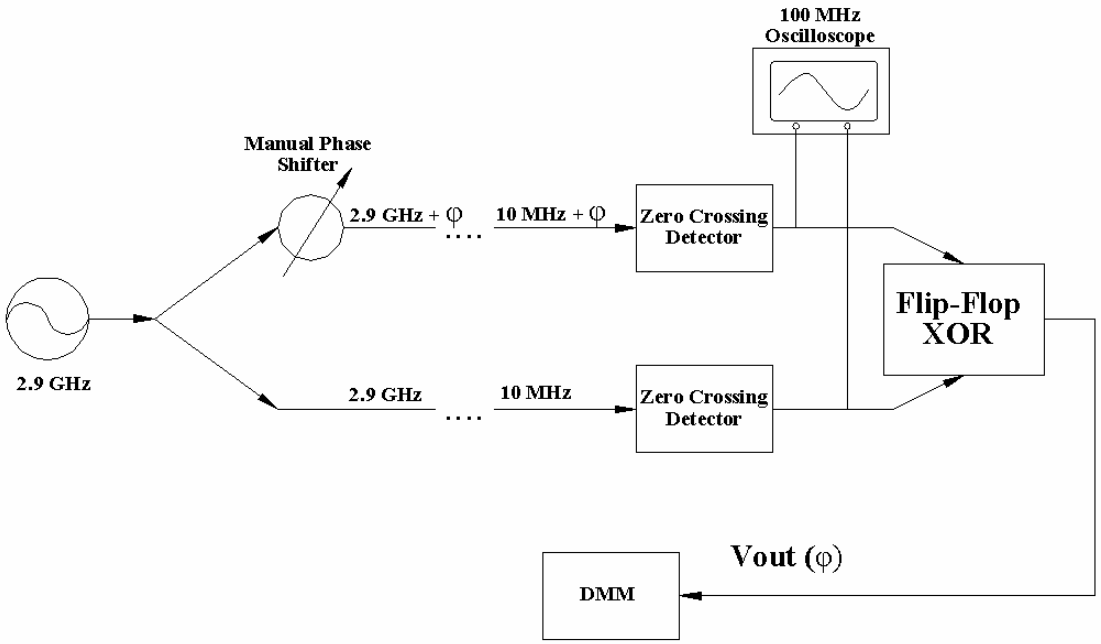

Fig. 5-1. Conjugation measurement setup with microwave source and line stretcher phase shift module to mimic pilot source.

The PD linearity measurement setup split the output of a microwave source at 2.9 GHz and used manually controlled line stretcher phase delay modules to insert and adjust the two split paths' relative phase relation. Using a single microwave source is

necessary to ensure constant phase coherency. This setup is illustrated in Fig. 5-1. This range of phase adjustment mimics the inter-element phase delay of a pilot signal being received from a range of various arrival angles.

B. PD Linearity

Measuring PD and PCL linearity determines optimal system performance and accuracy. As presented in Chapter II, linearity is assumed and necessary to achieve accurate phase steering. Offset error and gain error can be adjusted in their respective adjustment stages of the PD and PCL. However, there is no device implemented to compensate for non-linearities.

Gain and Offset Adjustment

First, a rough offset and gain adjustment was performed by adjusting the respective variable resistors of the PD. The offset was adjusted so that the PD output was zero volts when the two 10 MHz zero crossing detector outputs were perfectly in phase. The 10 MHz zero-crossing signals were aligned by adjusting the line stretcher phase delay modules manually and viewing the zero cross detector output on a 100 MHz oscilloscope. Since the PD has a linear range of 8π, a 2π ambiguity exists. Since the phase delay modules only added 2π of phase delay in the signal path, the ambiguity must be considered. Initially the PD randomly assigns the input into one of the 2π ranges. Therefore care was take to ensure the zeroed voltage output correlated to the 4π PD operating point within its range and not the 2π or 6π operating point.

The PD gain was set to 6.53 mV/deg. This was accomplished by using the ambiguous nature of the 8π PD range. The PD responds to a 10 MHz phase-zeroed input by randomly latching to one of the 2π-multiple points in its 8π range. The phase-zeroed 10 MHz was applied and reapplied until the PD randomly latched to a 2π or 6π state. It could then be discerned which of the 2π or 6π states the PD had latched to. The PD difference of 360° was then known and the PD gain could then be determined using

the simple relation $|K_{PD}|= |V_{out}|/360°$. The variable gain resistor could then be adjusted to achieve the desired gain.

After full system integration, these adjustments would be superseded by supplemental tuning to achieve maximum accuracy. They were here performed to adjust the gain and offset so that the system would be operating in the same region as its final integrated realization to achieve similar linearity performance.

Measurement Procedure and Results

Having adjusted the gain and offset, the delay line phase shifters were manually adjusted and a data was taken to produce the linearity graphs of Figs. 5-2 – 5-5. At each point, the PD output voltage was measured with a digital multimeter and the time difference between the two 10 MHz zero crossing detected input edges was measured using a 100 MHz oscilloscope. The measurement was taken with the following procedure: the scope trigger source was set to the PD reference input; the frequency of the reference input was measured; the time difference between the rising edges of the two PD inputs were measured by zooming in the scope time scale and marking the edges with respective markers; the markers' time separation was noted along with the PD voltage output. Given that frequency as was measured, the edge time separation is then translated to phase difference.

There were various sources of measurement error resulting in limited measurement accuracy. The largest component of these sources was due to the eyeball method of measuring pulse edges. It was estimated to be as much as ±1 ns of error for each measurement. At 10 MHz 0.7 ns translates to 3.6° error. Another source of error was due to drift in the frequency of the microwave source. Any frequency drift at 2.9 GHz translates directly down to 10 MHz. Though 0.5 MHz drift at 2.9 GHz is minimal, it has a large impact when down-converted to a 0.5 MHz drift at 10 MHz. The 10 MHz frequency was measured at the beginning of each linearity series. Unfortunately the

time necessary to complete each series often is several minutes. It was observed that over a period of just a few minutes, the measured frequency of the 10 MHz source can vary as much as ±0.5%. This variation contributes error as large as ±1.5 deg due to microwave source frequency drift. These measurement errors total to ±4 deg and set the limit for measurement accuracy. This ± accuracy limit is denoted on all the following linearity graphs of this section by the straight broken line going horizontally across the top and bottom of the charts.

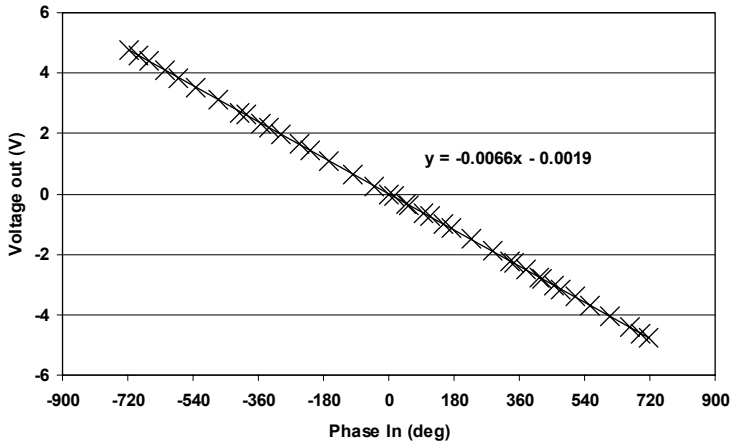

Fig. 5-2. PD linearity – full ±4π range from zeroed range center.

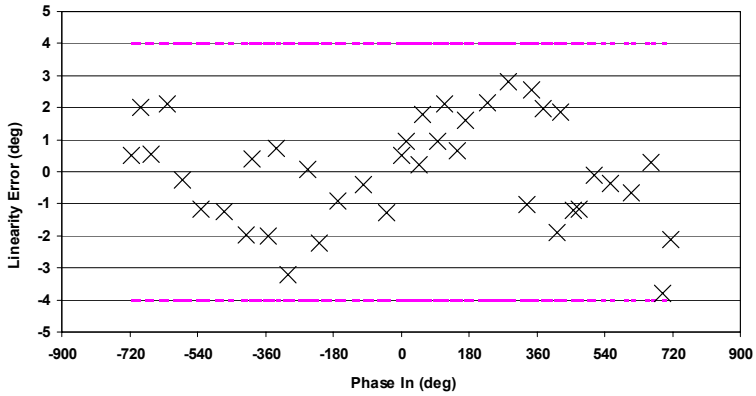

Fig. 5-3. PD linearity error – full ±4π range from zeroed range center. The broken line on top and bottom shows measurement accuracy limits.

The PD output was measured for the entire 8π range as seen in Fig. 5-2 showing good linearity. A best-fit trend line derived from the entire 8π range data was inserted to act as an optimal linearity baseline. Since the linearity is good, the trend line is almost indiscernible from the raw data spline. Linearity error is defined as the deviation of the measured data from the best fit linear trend line and shown in Fig. 5-3. Note that almost all points fall within the measurement error range.

Linearity was measured for the entire 8π range, but the PD operation will only be used in a single 2π region. The linearity of only the operation region is further investigated in Fig. 5-4. Similarly, a best fit linear baseline is inserted, but based only on the points in the 2π region. From this base line the linearity error of the 2π region is obtained and presented in Fig. 5-5, and again achieves measurements within the measurement error range. The extra consideration given by zooming into the operating range would allow the gain and offset to be fine tuned to accommodate specifically for non-linearities of the operating region and achieve absolute minimal error. The same zooming and tuning concept will be applied to the linearity of the PCL.

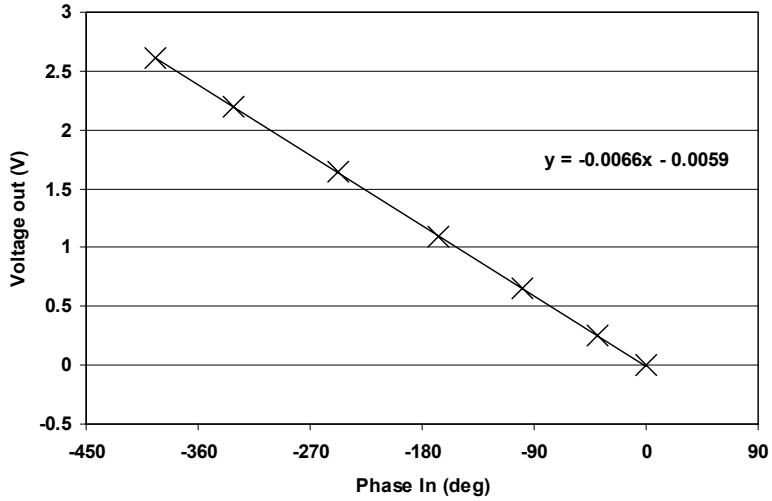

Fig. 5-4. PD linearity – a subset of the PD linearity data is further expanded. The PD will only need to operate in a 2π range.

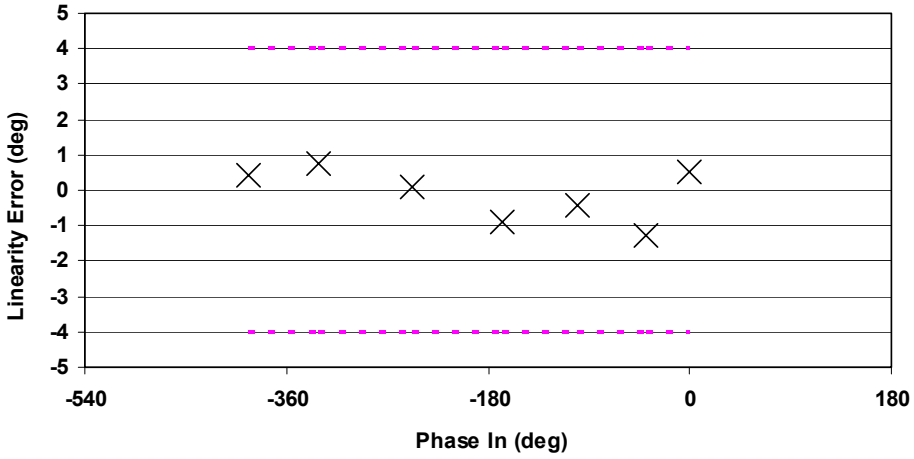

Fig. 5-5. PD linearity error – trend line equation has been optimized for specifically this region.

C. PCL Linearity

The linearity of the PCL was also measured in a similar fashion. The main difference between the operation of the PD and the PCL measurement methods is that for the PD, a phase difference is input, and a voltage is output. For a PCL a voltage is input and a phase difference is output. The largest difference between the measurements was the measurement error range. A significant amount of phase noise was present in the synthesized VCO and will be further investigated in the next section. As pertaining to the linearity measurement, it significantly affected the measurement uncertainty of the edge separation between the reference and VCO signals output from the PCL. This increased the estimated measurement uncertainty to ±7.2 deg. A picture of the phase locked PCL synthesized input and output sinusoids as shown Fig. 5-6. The PCL input reference is on top and the output below is steered to 180° as determined by the DC phase conjugation voltage input into the PCL.

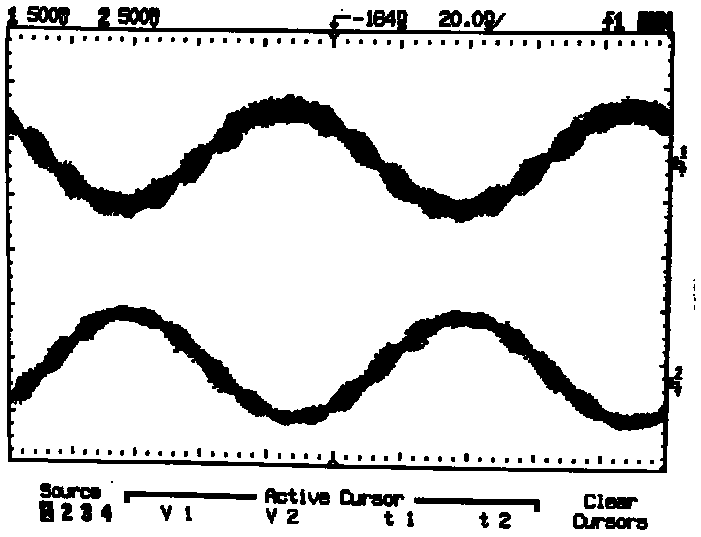

Fig. 5-6. Phase-locked PCL output showing reference-VCO coherency and with a set phase difference of 180°. The time scale is 20 ns/(major division) and the voltage scale is 500 mV/(major division).

PCL uncertainty for the entire region as well as the sub-region of operation was measured and is presented in Figs. 5-7 – 5-10 and show a highly linear correlation. The PCL shows considerably larger non-linearities than did the PD. This is due to the fact that the PCL filter placed between the XOR and the active conditioning stages did not filter out as much high frequency component from the pulse output waveform. As the duty cycle of the pulsed waveform tended towards zero and one, a larger percentage of the pulse output power was contained in the high frequency components. Disparity between the rise and fall times of up edges and down edges were observed in op amp performance. It is believed that this behavior plays a key role in PCL nonlinearity. Filtering out more high frequency content from the XOR pulse output was investigated to help improve linearity, but the necessity for loop stability opposed such filtering.

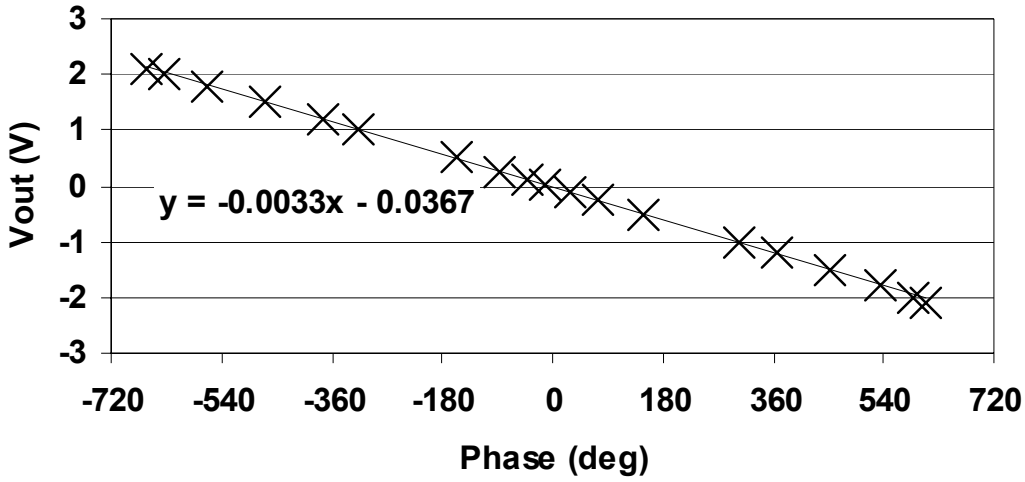

Fig. 5-7. PCL linearity over entire range – equation of the line best-fit to the data of 8π range in slope-intercept form, y=mx+b.

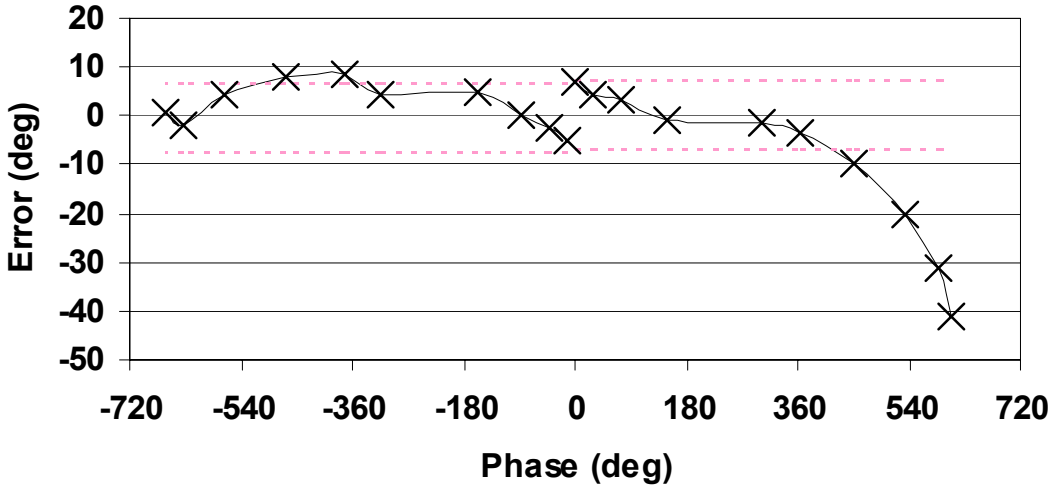

Fig. 5-8. PCL linearity error over entire range.

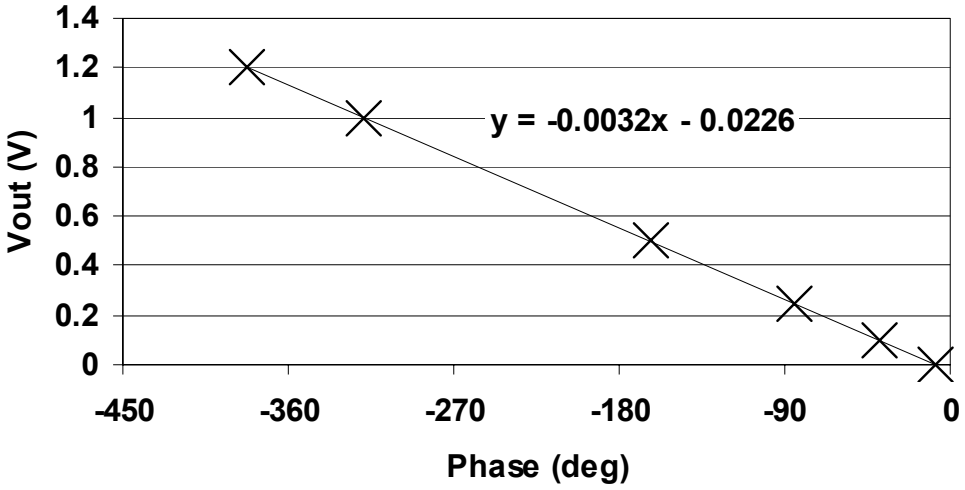

Fig. 5-9. PCL linearity of operating range – equation of line best-fit to data in the operating range in slope-intercept form, y=mx+b.

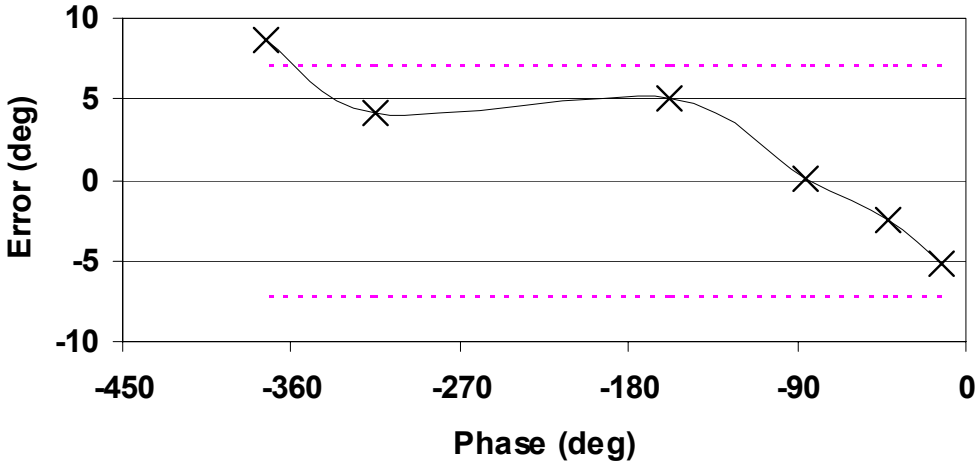

Fig. 5-10. PCL linearity error of operating range only – derived from best fit line of operating region points only. Smaller error is subsequently achieved.

D. Phase Conjugation Measurement

The PD and PCL were then integrated together and the phase conjugation and scaling performance was then directly measured. The phase difference applied to the PD was measured versus the conjugated and scaled phase difference output from the PCL. The scope display of such a measurement is illustrated in Fig. 5-11. Note in Fig. 5-11 that the waveform edge of the PCL output leads the edge of the phase shifted waveform by twice as much time and demonstrates a phase scaling factor of two.

Two graphs showing the direct phase scaling relation are shown in Figs. 5-12 and 5-13. A best-fit trend line is inserted in both and demonstrates the phase scaling factor of 2. This may be noted by the trend line equation slope. Fig. 5-12 shows the characteristic across the entire region of the PCL. Fig. 5-13 shows the operation region and again reveals increased linearity and accuracy over the short range.

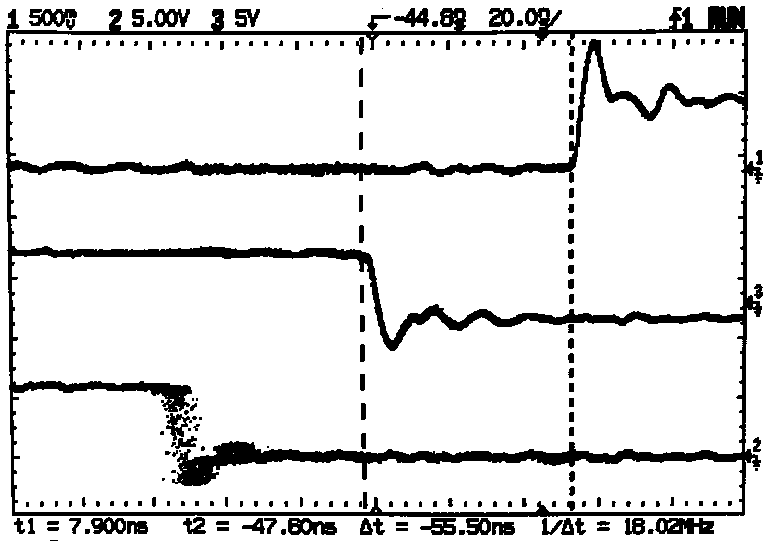

Fig. 5-11. Scope display of direct phase conjugation measurement. The reference of both PD and PCL is on top, the phase shifted PD waveform is in the middle, and the phase scaled and conjugated phase PCL output is on the bottom. The time scale is 20 ns/(major division) and the voltage scale is 5 V/(major division).

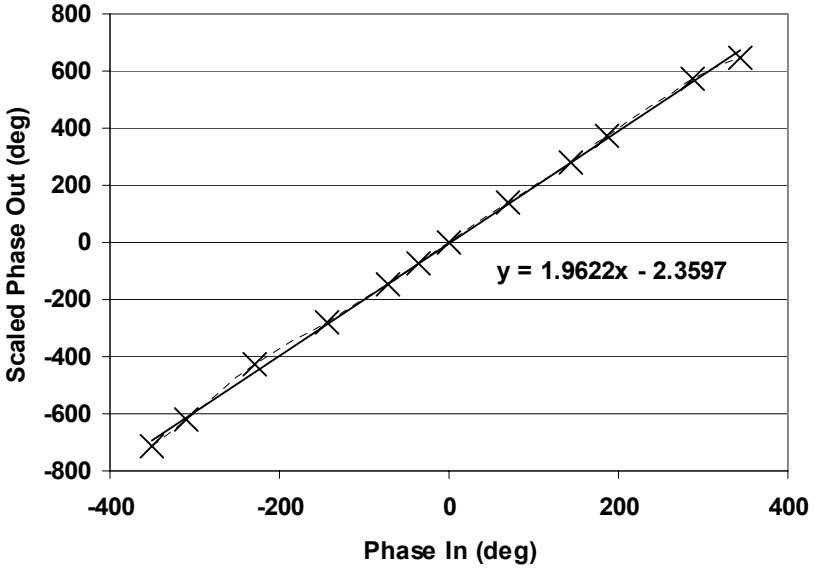

Fig. 5-12. Phase conjugation across entire PCL operation range. The slope of the inserted best-fit linear trend line equation demonstrates the phase scaling factor of nearly two.

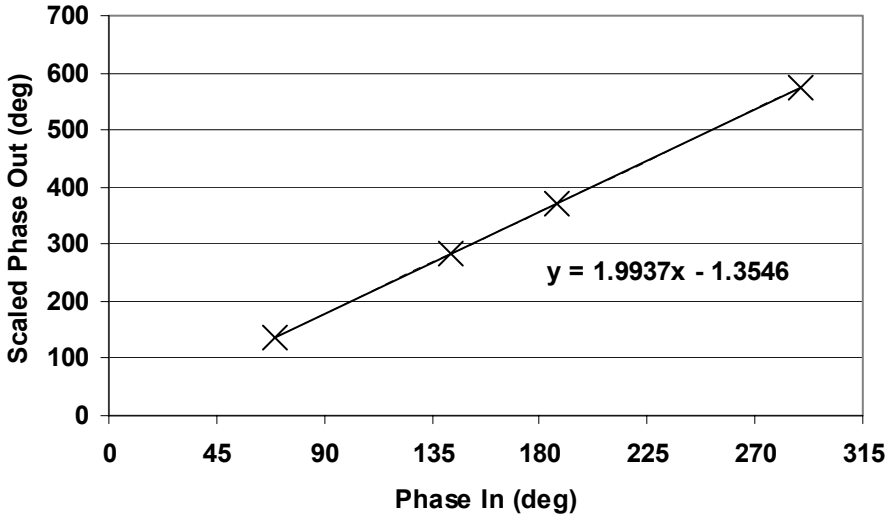

Fig. 5-13. Phase conjugation across limited range of operation. The slope of the inserted best-fit linear trend line equation demonstrates the phase scaling factor of nearly two. Gain accuracy improves due to fine tuning in the operation region.

E. PCL Phase Noise

Though phase locked to the reference, some amount of random phase difference will always be present between the reference and VCO output due to the inherent behavior of the feedback loops. This random difference will here be referred to as phase noise. A scope image illustrating the phase noise between the VCO and reference is shown in Fig. 5-14.

The phase noise is assumed to have a zero mean Gaussian distribution. The width of time uncertainty measured in Fig. 5-14 is 1.8 ns corresponding to 6.48 degrees. This value is probably a good estimate for the phase noise distribution function's standard deviation. Its primary detriment to retrodirectivity is to reduce the efficiency of the transmitting array by causing destructive recombination in the direction of the target. Also as previously mentioned, it increases the uncertainty of the time measurements by dispersing time values.

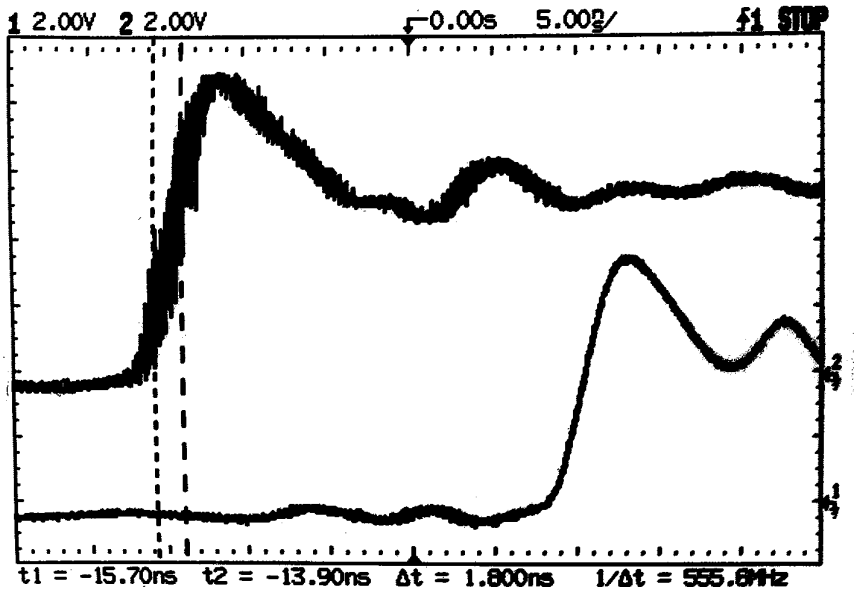

Fig. 5-14. Phase noise between locked PCL output and phase reference input. The time scale is 20 ns/(major division) and the voltage scale is 2 V/(major division).

F. PCL Modulation

The PCL response to a control voltage step function was observed. This was accomplished by inputting a square wave into the steering voltage of the PCL with an amplitude of 500 mV. The gain of the PCL PD determines this 500 mV step to be translated to a 76° phase step. The response of the VCO control voltage to a rising step is shown in Fig. 5-15 to have a settling time of 4.9 ms. Small oscillations in the VCO control voltage can be observed as it settles to the new state. Integration of the control voltage over time multiplied by the VCO gain would yield the phase transition characteristics.

As previously mentioned, disparity between the up and down edges of PCL op amps are suspected to play a role in the nonlinear characteristics of its output. This hypothesis is supported by comparing the loop response of the down edge step with that of the up edge step as may be seen in Fig. 5-16. The settling time of the down step is noticeably shorter than that of the up step's settling time.

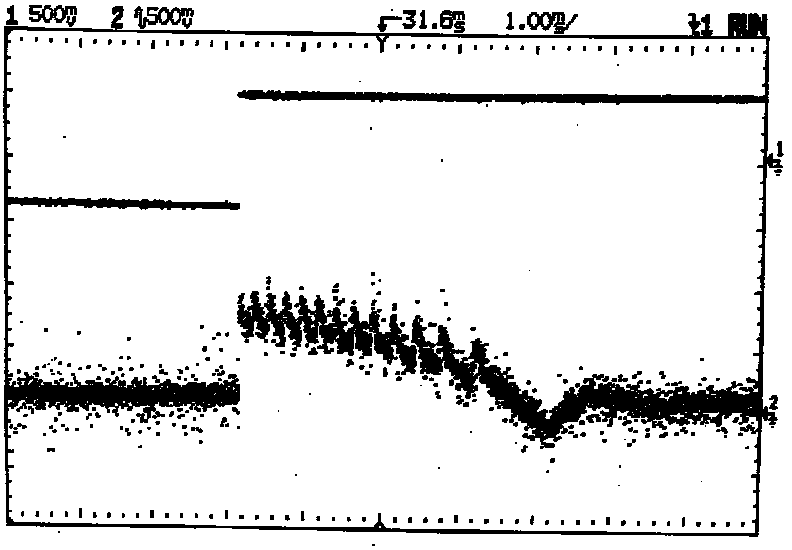

Fig. 5-15. The PCL VCO control voltage response to 500 mV step function is shown to have a settling time of 4.9 ms. The time scale is 1 ms/(major division) and the voltage scale is 500 mV/(major division).

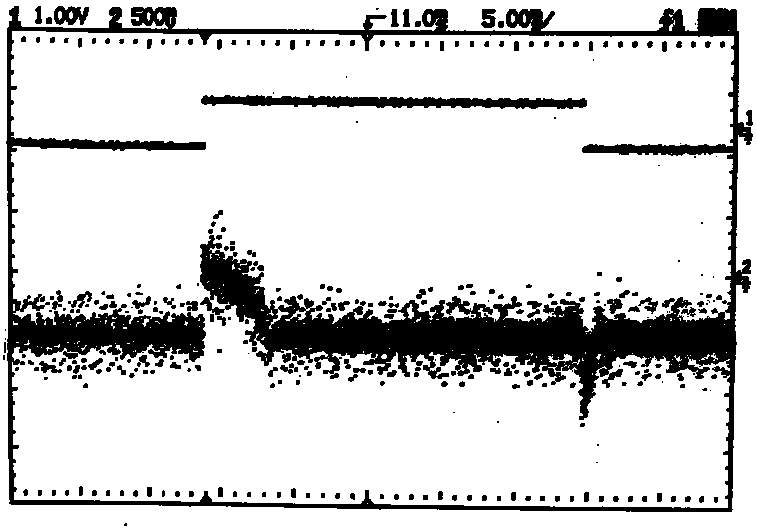

Fig. 5-16. Viewing the PCL VCO control voltage response of both the down and up steps shows loop asymmetry. The time scale is 5 ms/(major division) and the voltage scale is 500 mV/(major division) for the VCO control voltage on the bottom and 1 V/(major scale) for the modulation function on top.

The obtained data has thus shown the retrodirective phase scaling capability of the proposed design. Loop stability has been achieved showing the merit of the loop design equations and procedure. A baseline has been established from which to analyze the conjugation and beam steering performance as will be presented in the following chapter.

CHAPTER VI
ARRAY STEERING

As seen in the measured phase conjugation results, there is a considerable amount of conjugation error that is unavoidable. This error will limit beam steering accuracy. As relating to the application of SPS, steering accuracy has been mentioned as a cardinal performance metric. However, the large size and capital investment necessary to implement such an array became an impeder of such a venture. The measured phase conjugation data will be used to derive beam steering performance expectations. Consideration is here given to how different array sizes and elements would affect beam shape, steering accuracy, and measurement requirements. This is done to investigate likely antenna measurements that will be performed in future research.

A. Steering Performance

An estimate of steering accuracy can be constructed by building a table which sums the nonlinearity errors of the PD and the PCL at correlating phase angles. The actual steering angle θ_a can be broken into two parts where $\theta_a = \theta_e + \theta_o$.

$$\theta_e = \sin^{-1}\left(\frac{\varphi_o + \varphi_e}{kd}\right) - \sin^{-1}\left(\frac{\varphi_o}{kd}\right) \tag{6.1}$$

is defined as the steering error while

$$\theta_o = \sin^{-1}\left(\frac{\varphi_o}{kd}\right) \tag{6.2}$$

is the ideal steering value derived from the measured best-fit linear steering phase value φ_o. The phase error φ_e is obtained by summing the nonlinear phase error of a few closely correlating steering points, k is the propagation constant (rad/m) and d is the spacing between elements. It is noteworthy that the relation between steering error and

phase delay error changes as a sine function achieving maximum $d\theta_e/d\varphi_e$ when $\varphi_o = 0$. Table 6-1 lists the steering error estimate extrapolated from the measured data of φ_e.

TABLE 6-1
STEERING AND PHASE ERROR

Steering phase delay φ (deg)		Steering Angle θ (deg) $kd = \pi$		$kd = 4\pi$	
φo	φe	θo	θe	θo	θe
0	7.00	0.00	2.23	0.00	0.56
-85	2.00	-28.18	0.72	-6.78	0.16
-163	5.50	-64.90	3.85	-13.08	0.45
-319	5.20	13.17	1.71	3.26	0.41

It is important to note that for a large array of elements, element error will likely not be uniform. This indeterminable non-uniformity will affect the steering error unpredictably. A truly random error distribution over a large number of array elements would result in a more dispersive and less efficient radiator [28]. The above analysis however is still deemed useful to obtain a quantified estimate of phase steering performance for a two element array.

From the values in Table 6-1 a number of observations may be made. The steering accuracy required for the SPS array that was presented in Chapter I set a maximum angular steering error on the order of $\theta_e = 0.0005°$. The case of $kd = 4\pi$ has inter-element spacing most like that of the SPS and achieve a best case steering error of 0.16° and achieves 0.56° steering error at array broadside. An accuracy improvement of several orders of magnitude will likely be required for this approach to be implemented in the SPS application. For applications other than the SPS, these values are useful when considering beam width. The beam width should be larger than the steering error, this will ensure sufficient power will always be directed in the intended direction of propagation.

B. Two-element Array Patterns

A Matlab program was written to produce the array gain pattern for arrays composed of various element types. A two element array pattern of both an isotropic element array and a narrow beam two-element array of two 16x16 sub-array patch antennas are presented to demonstrate the logistics of measuring antenna retrodirectivity. The program multiplied the individual element patterns times the array factor AF taken from [29] as

$$AF = \sum_{n=1}^{N} e^{j(n-1)\psi} \tag{6-3a}$$

and

$$\psi = kd \sin\theta. \tag{6-3b}$$

For a two element array N = 2. The inter-element phasing ψ of (6-3b) equals the propagation constant *k* times the physical element spacing *d* times the sin(θ) where θ is defined as the steering angle from array broadside.

Two-element Isotropic Array

To serve as a reference, the array factor for a two element array of isotropic radiators is illustrated in Fig. 6-1. Since isotropic radiators are assigned an element gain factor of one, the array factor for isotropic radiator array equals the overall array gain. Having two elements, the array factor increases the array gain by only 3 dB. As is apparent in Fig. 6-1, the beam is quite broad with gradual and gently sloping gain transitions. The difference between the maximum and minimum gain is less than 0.2 dB. Though such a pattern is recognizable and capable of verifying the proposed concept, the low gain variation makes identifying the peak beam and directivity accurately very difficult. It should therefore be observed that since performance of beam steering is crucial in phased arrays that array factors of greater magnitude and directivity would allow greater steering measurement certainty and less error.

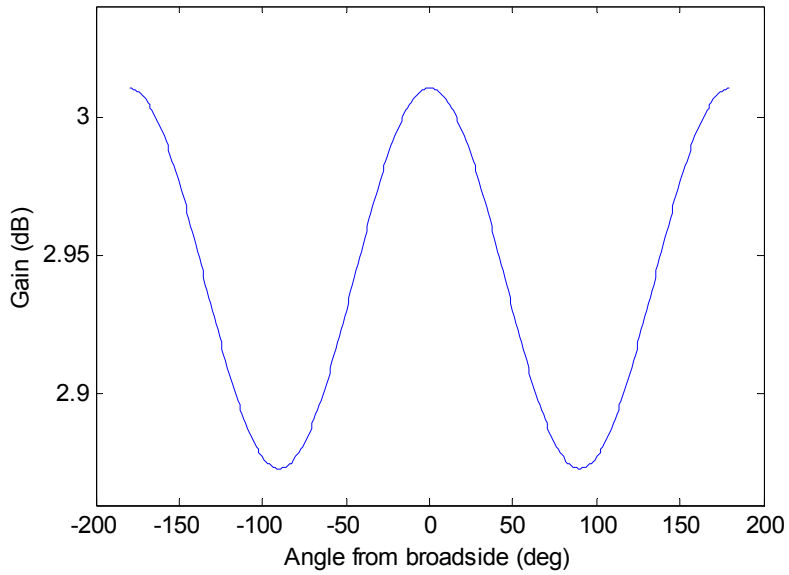

Fig. 6-1. Gain (dBi) of two-element isotropic radiator array steered to broadside.

Two-element SPS Transmitter

A 16x16 patch array was designed and presented in [30] achieving high directivity and gain of 20.2 dBi as shown in Fig. 6-2. The array is composed of truncated patch antennas achieving circular polarization at an operating frequency of 5.8 GHz. A profile if the 16x16 array is also shown inset into the gain chart in Fig. 6-2. This transmitter was designed to be a viable solution to the application of the SPS and is capable of sustaining high power transmission will low loss. This 16x16 array antenna would serve as sub-array elements of vary large SPS transmitter directing the captured energy from space to earth. The two element array factor and gain steered to broadside is shown in Fig. 6-3. The array factor and radiation pattern steered to $\theta=20°$ is shown in Fig. 6-4. It should be promptly noticed that the two radiation patterns look nearly indistinguishable and show no signs of beam steering as did the isotropic array. This is

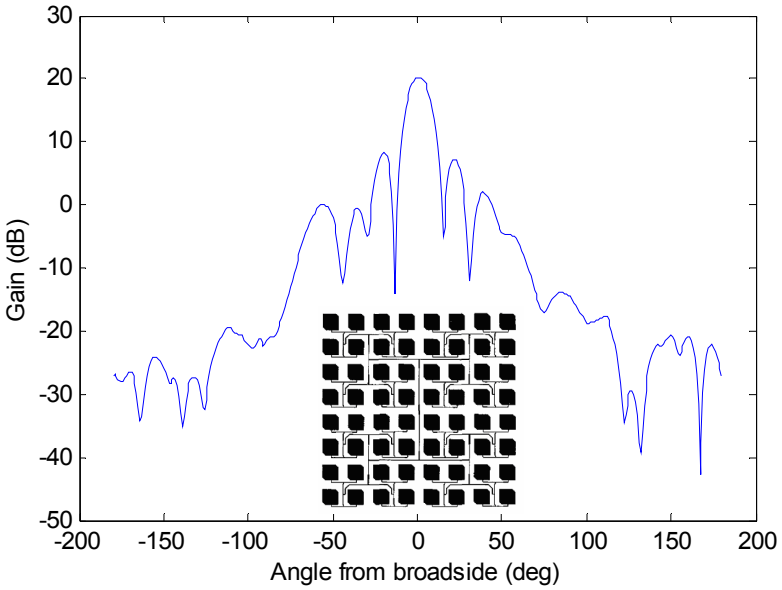

Fig. 6-2. The radiation pattern and antenna profile of a single subarray of 16x16 transmitting antennas designed for the SPS (5.8 GHz).

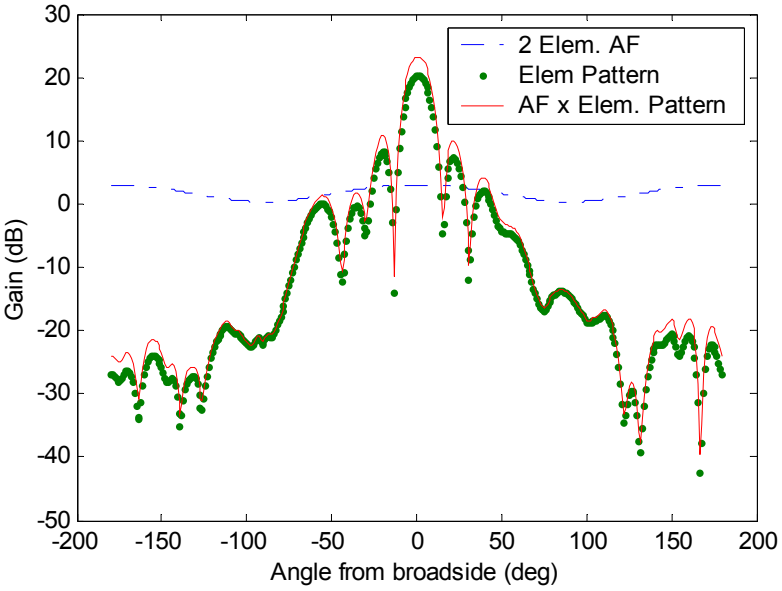

Fig. 6-3. The radiation pattern of a two-element array of two 16x16 subarrays steered to broadside with the two element array factor and single element gain shown to reference relative pattern multiplication factor amplitudes.

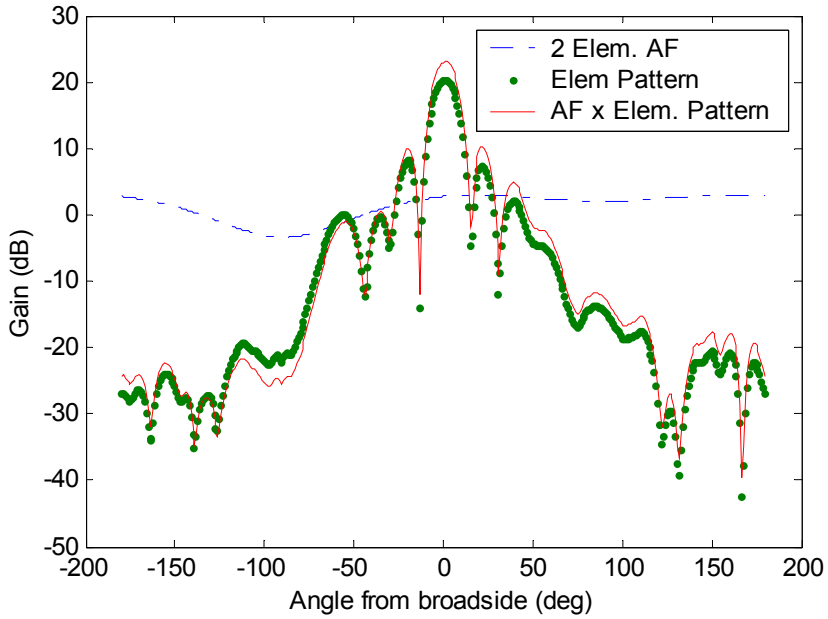

Fig. 6-4. The radiation pattern of a two-element array of two 16x16 subarrays steered to 20° with the two element array factor and single element gain shown to reference relative pattern multiplication factor amplitudes.

due to the relatively low directivity of the array factor compared to the sub-element directivity.

C. Large Array Beam Steering

Increasing the number of sub-elements to 100 shows considerably better steering results in Fig. 6-5. The high number of array elements is needed to increase the relative directivity of the array factor. It also demonstrates that due to the high directivity of the proposed SPS transmitting sub-array, a large transmitting array with many elements will need to be built to test the performance of the large SPS system as proposed in [14].

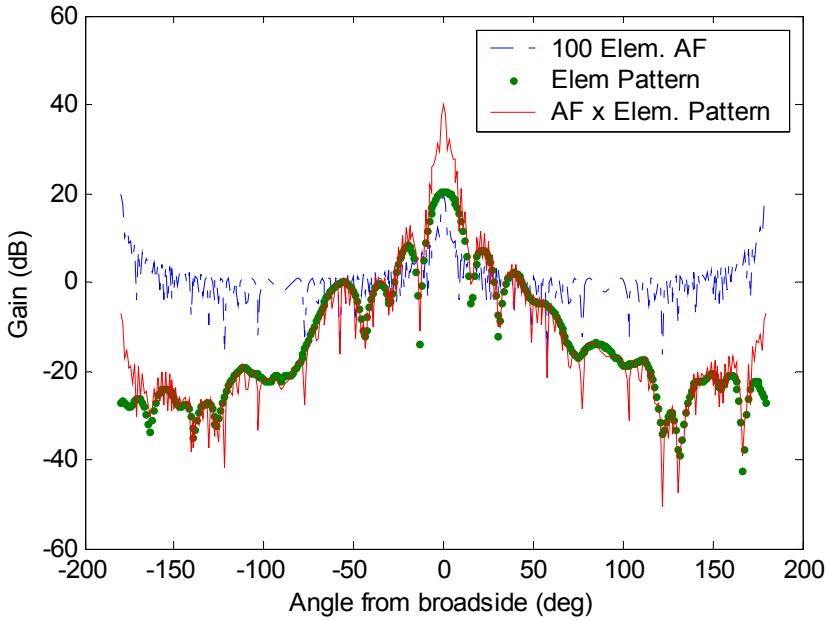

Fig. 6-5. 100 element SPS array transmitting pattern. This shows the array factor magnitude has increased dramatically with respect to the element pattern.

D. Steering Measurement Accuracy

The beam steering of the SPS application requires beam steering accuracy on the order of $\theta_e = 0.0005°$ where θ_e is the angular steering error. This is an unprecedented steering accuracy for space antenna arrays. Fig. 6-6 again illustrates the geometry of angular uncertainty relative to two positions with separation distance *d* and uniform radii of uncertainty r_u.

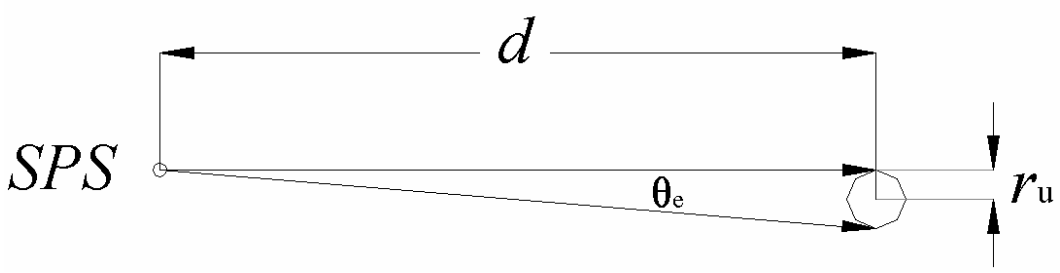

Fig. 6-6. Geometry positional error between two points.

Achieving measurement techniques capable of such accuracy will be a necessary step before SPS realization. Array design and performance will need to be verified before launch. Table 6-2 presents a list of uncertainty radii and separation distances correlating to various conceived practiced measurement techniques.

TABLE 6-2
ANGULAR MEASUREMENT ACCURACY DIMENSIONS

Measuring Apparatus & Environment	Uncertainty Radius r_u (mm)	Separation Distance d (m)	Steering Error θ_e (deg)	Steering Error θ_e (arc sec)
Anechoic Chamber	1	10	0.011459	41.25
Augmented GPS	10	68	0.016852	60.67
Augmented GPS	10	400	0.002865	10.31
Mount. Range/ GPS	10	5000	0.000229	0.83
Geosynch. Orbit	184.5685684	42300000	0.000500	1.80

Various separation distances and uncertainty radii along with correlating angular error. This illustrates the need for greater measurement accuracy and new technique development.

Various measurement apparatus provide different measurement accuracies. A recent development called augmented GPS allows location relative to a known source to be accurate up a 10 mm radius of uncertainty. Using the augmented GPS equipment in the environment of a mountain range with a separation distance of 5 km could achieve steering measurements with accuracy on the order that required for the SPS. It is also noted that while convenient, the accuracy of an anechoic chamber with a dimension of 10 m also provides only limited measurement performance.

In summary, the beam steering of two-element arrays has been shown to produce measurable but minimal steering effects. The phase conjugation error as defined by best-case measurements from Chapter V achieves steering accuracy far from that required of the SPS. It has also been shown that using a highly directive antenna such as that proposed for the SPS requires very large antenna arrays to achieve measurable beam

steering. This requires special attention must be paid to measurement techniques and accuracy.

CHAPTER VII
CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE STUDY

A. Conclusions

The idea of WPT has been introduced along with the concept of the SPS. The method of retrodirectivity has been proposed as a possibility to achieve SPS beam steering. The theory of retrodirective phased array beam steering has been reviewed. A new novel method for achieving retrodirectivity has been introduced. The concept of phase scaling and frequency translation has released retrodirective beam steering from integer constraints and approximation errors. The proposed method was realized and its governing design equations were presented. Existing PLL control theory was adapted to produce a successful phase control loop. Subcomponents such as the PD and PCL have been characterized to establish linearity. Performance of overall phase conjugation and scaling has been verified. The results achieved have matched well with expected values and validate the new retrodirective technique.

B. Recommendations for Future Study

Future research on this topic could include design loop refinement, transceiver miniaturization, and large array beam steering performance measurement. Loop refinement might entail further investigation to optimize loop performance increasing linearity, and reduce phase conjugation noise. The current transceiver used for up and down conversion is quite large, heavy, and expensive. Integrating the transceiver and retrodirective circuitry onto one circuit board is desirable. Efficient system integration would allow easier and more cost effective array element construction. This would allow large retrodirective arrays to be built and testing of antenna system level steering performance. Showing large array system performance is considered to be the next step to prove the proposed retrodirective technique's relevancy to future applications.

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APPENDIX A
PCL AND PD SCHEMATICS AND IMAGES

The following diagrams illustrate the various electrical components used to create the PD and PCL. These schematics were generated in Protel PCB layout software and used to layout the board components. Fig. A-1 shows the schematic of the PD circuitry. This design was used in both the receiving phase detector circuitry as well as the PD of the PCL. The design software contained a valuable tool allowing design sections to be marked for repetitive use and redundant design work was avoided. Fig. A-2 shows a schematic of the VCO Colpitts type design and Fig. A-3 shows the control loop circuitry. Fig. A-4 is a block diagram of the layout. Fig. A-5 shows a picture of the transceiver. Figs. A-6 – A-8 are images of the phase conjugation circuitry operating at 10 MHz.

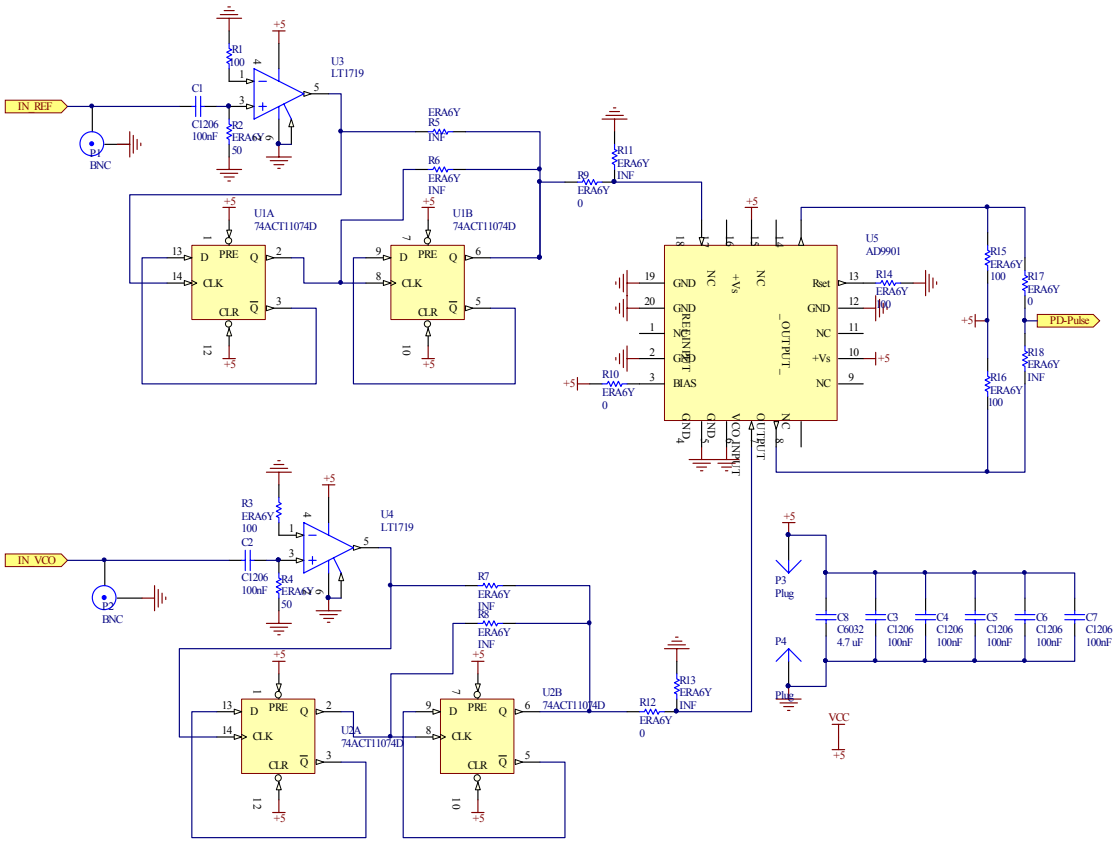

Fig. A-1. Zero-crossing and PD circuitry. The inputs on the left are the respective sinusoid waveforms. The output on the right would be the pulse train output from the XOR.

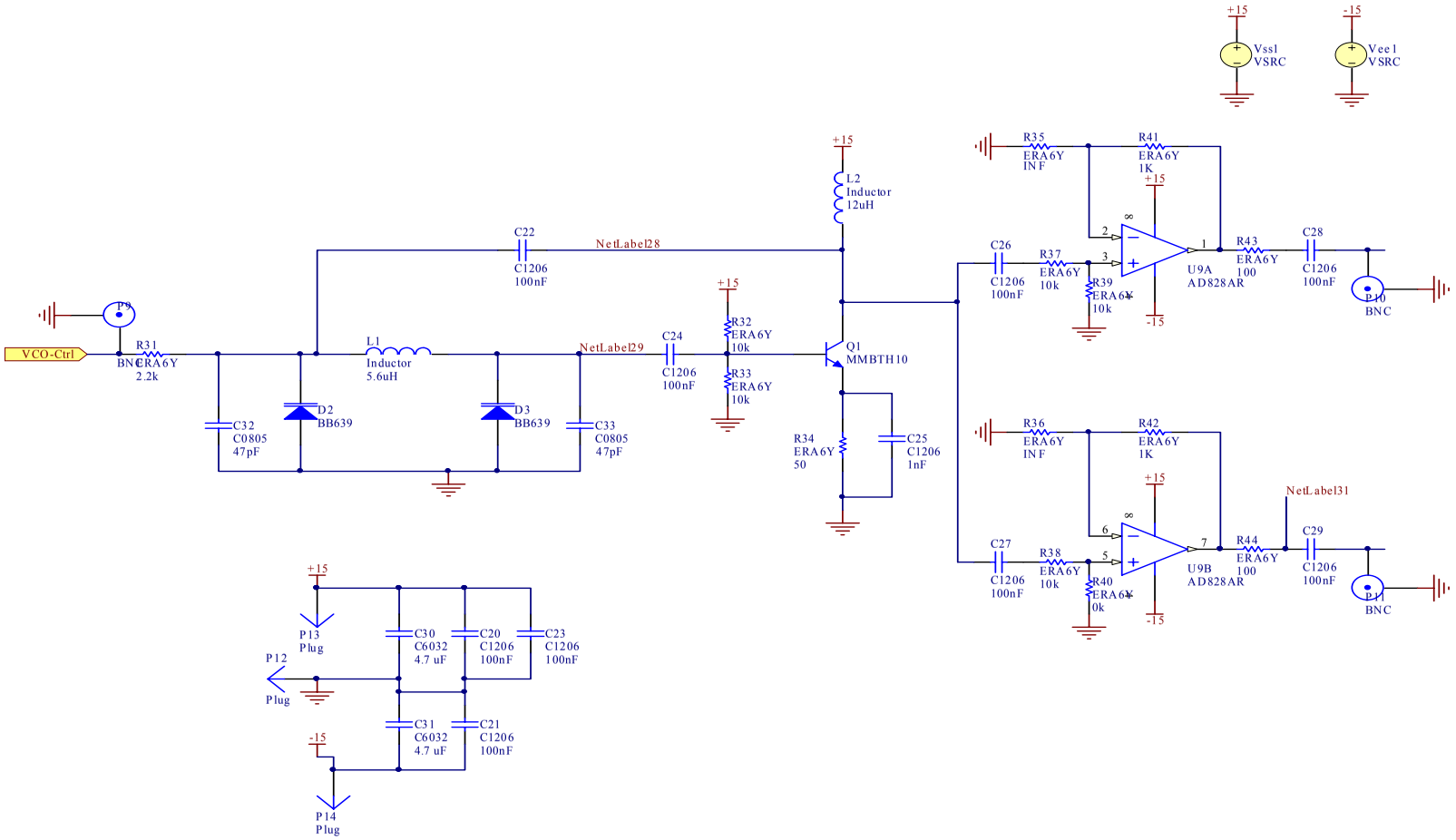

Fig. A-2. Colpitts VCO – the DC control voltage comes in from the left. The LC tank is composed of two capacitors, two varactors, and an inductor. The transistor Q1 amplifies the oscillations of the tank and provides positive feedback. The amplifiers on the right simply buffer the output from Q1 to prevent operating frequency shift from loading the output.

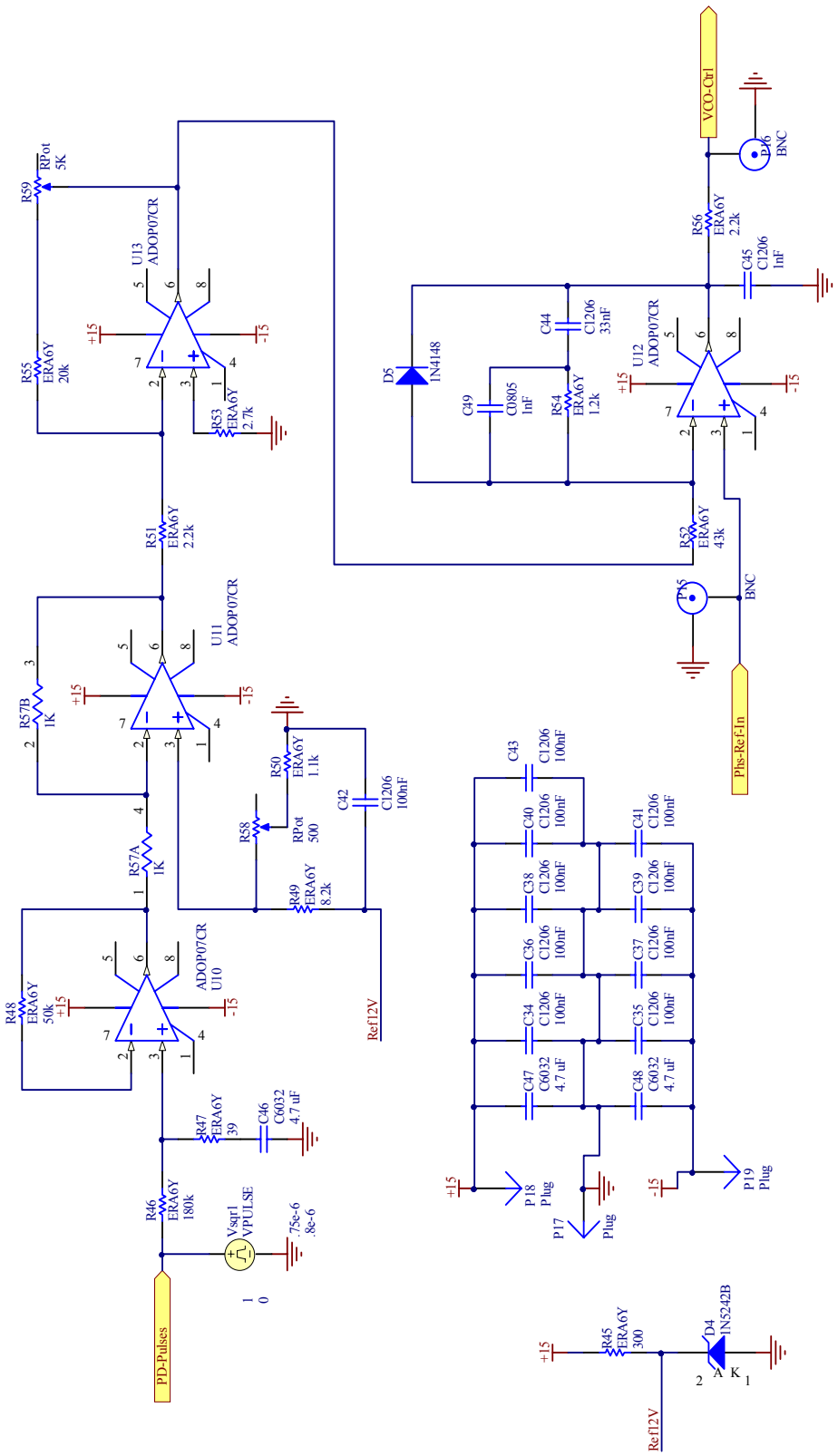

Fig. A-3. Control loop circuitry – the output pulses from the XOR is input from the left and immediately filtered. Offset and gain are then added to the filtered pulses. This averaged phase sample is compared with the reference phase voltage at amplifer U12 and a VCO control voltage is subsequently produced

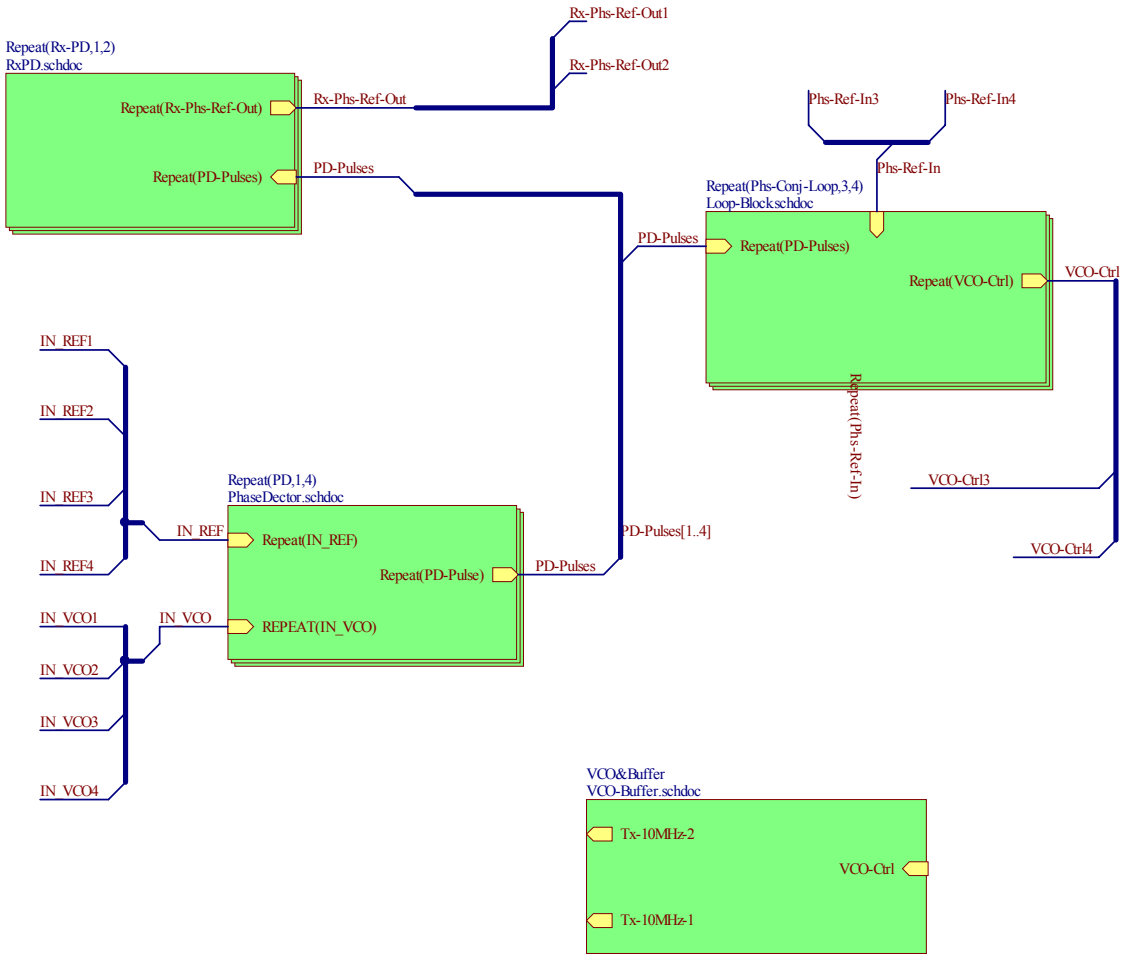

Fig. A-4. Block diagram of phase conjugating layout.

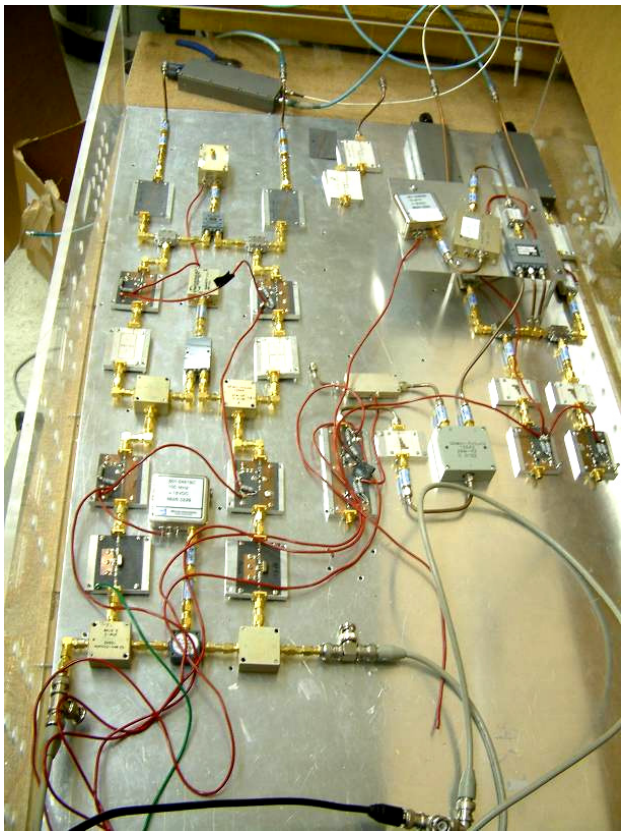

Fig. A-5. Transceiver – down-converting from 2.9 GHz to 10 MHz and up-converting from 10 MHz to 5.8 GHz while maintaining phase coherency between parallel channels.

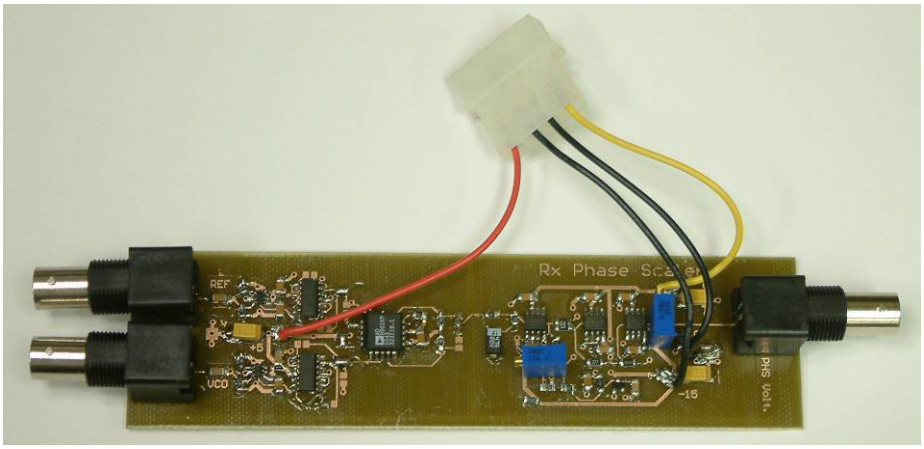

Fig. A-6. Phase Detector – two phase coherent sinusoidal inputs from the left and a DC output voltage linear to the phase difference output on the right.

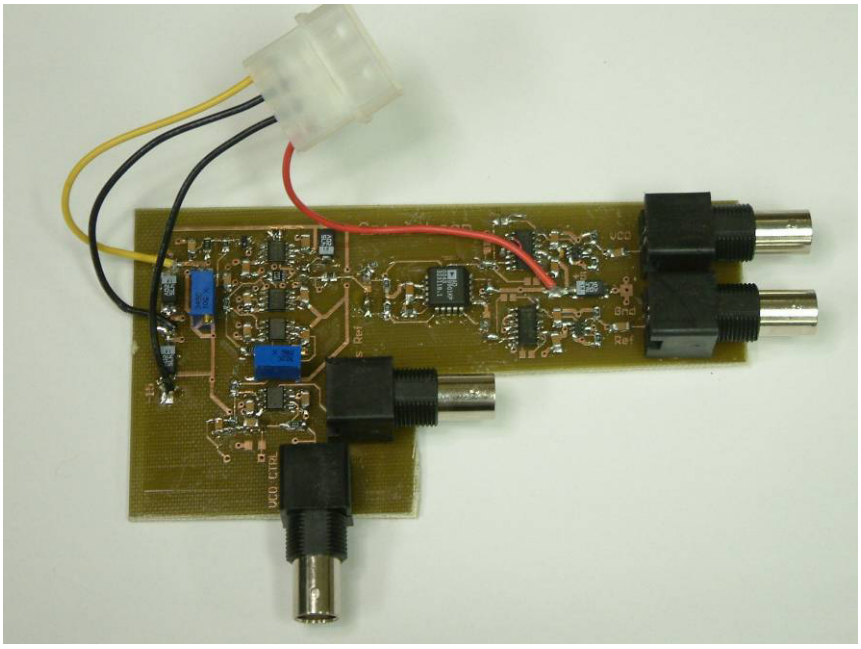

Fig. A-7. PCL – input are a phase reference voltage, a reference 10 MHz and the output from the VCO. Output is the VCO control voltage.

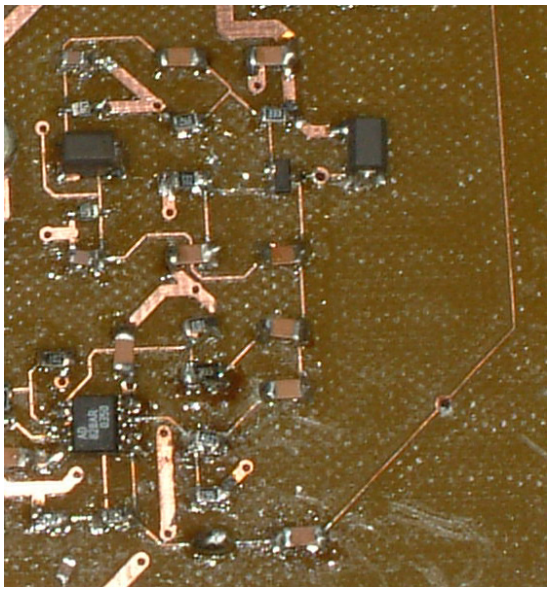

Fig. A-8. VCO image.

APPENDIX B
PD AND PCL SCHEMATIC COMPONENT INFORMATION

Further details of the components used in the schematic diagrams are presented in Appendix B. Information includes part description, component values, part numbers, and layout footprints.

TABLE B-1
COMPONENT VALUES, REFERENCE DESIGNATORS, AND FOOTPRINTS

Description	Designator	Footprint	Value
Ceramic Chip Capacitor - Standard	C1_PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C1_PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C1_PD3	1206	100nF
Ceramic Chip Capacitor - Standard	C1_PD4	1206	100nF
Ceramic Chip Capacitor - Standard	C2_PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C2_PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C2_PD3	1206	100nF
Ceramic Chip Capacitor - Standard	C2_PD4	1206	100nF
Ceramic Chip Capacitor - Standard	C3_PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C3_PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C3_PD3	1206	100nF
Ceramic Chip Capacitor - Standard	C3_PD4	1206	100nF
Ceramic Chip Capacitor - Standard	C4_PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C4_PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C4_PD3	1206	100nF
Ceramic Chip Capacitor - Standard	C4_PD4	1206	100nF
Ceramic Chip Capacitor - Standard	C5_PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C5_PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C5_PD3	1206	100nF
Ceramic Chip Capacitor - Standard	C5_PD4	1206	100nF
Ceramic Chip Capacitor - Standard	C6_PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C6_PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C6_PD3	1206	100nF
Ceramic Chip Capacitor - Standard	C6_PD4	1206	100nF
Ceramic Chip Capacitor - Standard	C7_PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C7_PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C7_PD3	1206	100nF
Ceramic Chip Capacitor - Standard	C7_PD4	1206	100nF

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Tantalum Chip Capacitor - Standard	C8_PD1	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C8_PD2	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C8_PD3	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C8_PD4	Cap6032	4.7 uF
Ceramic Chip Capacitor - Standard	C9_Rx-PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C9_Rx-PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C10_Rx-PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C10_Rx-PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C11_Rx-PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C11_Rx-PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C12_Rx-PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C12_Rx-PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C13_Rx-PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C13_Rx-PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C14_Rx-PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C14_Rx-PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C15_Rx-PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C15_Rx-PD2	1206	100nF
Ceramic Chip Capacitor - Standard	C16_Rx-PD1	1206	100nF
Ceramic Chip Capacitor - Standard	C16_Rx-PD2	1206	100nF
Tantalum Chip Capacitor - Standard	C17_Rx-PD1	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C17_Rx-PD2	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C18_Rx-PD1	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C18_Rx-PD2	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C19_Rx-PD1	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C19_Rx-PD2	Cap6032	4.7 uF
Ceramic Chip Capacitor - Standard	C20	1206	100nF
Ceramic Chip Capacitor - Standard	C21	1206	100nF
Ceramic Chip Capacitor - Standard	C22	1206	100nF
Ceramic Chip Capacitor - Standard	C23	1206	100nF
Ceramic Chip Capacitor - Standard	C24	1206	100nF
Ceramic Chip Capacitor - Standard	C25	1206	1nF
Ceramic Chip Capacitor - Standard	C26	1206	100nF
Ceramic Chip Capacitor - Standard	C27	1206	100nF
Ceramic Chip Capacitor - Standard	C28	1206	100nF
Ceramic Chip Capacitor - Standard	C29	1206	100nF
Tantalum Chip Capacitor - Standard	C30	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C31	Cap6032	4.7 uF
Ceramic Chip Capacitor - Standard	C32	CR2012-0805	47pF
Ceramic Chip Capacitor - Standard	C33	CR2012-0805	47pF
Ceramic Chip Capacitor - Standard	C34_Phs-Conj-Loop1	1206	100nF

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Ceramic Chip Capacitor - Standard	C34_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C35_Phs-Conj-Loop1	1206	100nF
Ceramic Chip Capacitor - Standard	C35_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C36_Phs-Conj-Loop1	1206	100nF
Ceramic Chip Capacitor - Standard	C36_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C37_Phs-Conj-Loop1	1206	100nF
Ceramic Chip Capacitor - Standard	C37_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C38_Phs-Conj-Loop1	1206	100nF
Ceramic Chip Capacitor - Standard	C38_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C39_Phs-Conj-Loop1	1206	100nF
Ceramic Chip Capacitor - Standard	C39_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C40_Phs-Conj-Loop1	1206	100nF
Ceramic Chip Capacitor - Standard	C40_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C41_Phs-Conj-Loop1	1206	100nF
Ceramic Chip Capacitor - Standard	C41_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C42_Phs-Conj-Loop1	1206	100nF
Ceramic Chip Capacitor - Standard	C42_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C43_Phs-Conj-Loop1	1206	100nF
Ceramic Chip Capacitor - Standard	C43_Phs-Conj-Loop2	1206	100nF
Ceramic Chip Capacitor - Standard	C44_Phs-Conj-Loop1	1206	33nF
Ceramic Chip Capacitor - Standard	C44_Phs-Conj-Loop2	1206	33nF
Ceramic Chip Capacitor - Standard	C45_Phs-Conj-Loop1	1206	1nF
Ceramic Chip Capacitor - Standard	C45_Phs-Conj-Loop2	1206	1nF
Tantalum Chip Capacitor - Standard	C46_Phs-Conj-Loop1	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C46_Phs-Conj-Loop2	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C47_Phs-Conj-Loop1	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C47_Phs-Conj-Loop2	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C48_Phs-Conj-Loop1	Cap6032	4.7 uF
Tantalum Chip Capacitor - Standard	C48_Phs-Conj-Loop2	Cap6032	4.7 uF
Ceramic Chip Capacitor - Standard	C49_Phs-Conj-Loop1	CC2012-0805	1nF
Ceramic Chip Capacitor - Standard	C49_Phs-Conj-Loop2	CC2012-0805	1nF
Half Watt Zener	D1_Rx-PD1	SO-G3/G1	
Half Watt Zener	D1_Rx-PD2	SO-G3/G1	
Silicon Variable-Capacitance Diode for Tuning of Extended Frequency Band in VHF TV/VTR Tuners	D2	SOD-323	
Silicon Variable-Capacitance Diode for Tuning of Extended Frequency Band in VHF TV/VTR Tuners	D3	SOD-323	
Half Watt Zener	D4_Phs-Conj-Loop1	SO-G3/G1	
Half Watt Zener	D4_Phs-Conj-Loop2	SO-G3/G1	
High Conductance Fast Diode	D5_Phs-Conj-Loop1	DO-35	
High Conductance Fast Diode	D5_Phs-Conj-Loop2	DO-35	
Inductor	L1	CC4532-1812	5.6uH

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Inductor	L2	CC4532-1812	5.6uH
BNC Elbow Connector	P1_PD1	BNC_RA CON	
BNC Elbow Connector	P1_PD2	BNC_RA CON	
BNC Elbow Connector	P1_PD3	BNC_RA CON	
BNC Elbow Connector	P1_PD4	BNC_RA CON	
BNC Elbow Connector	P2_PD1	BNC_RA CON	
BNC Elbow Connector	P2_PD2	BNC_RA CON	
BNC Elbow Connector	P2_PD3	BNC_RA CON	
BNC Elbow Connector	P2_PD4	BNC_RA CON	
Plug	P3_PD1	PIN1	
Plug	P3_PD2	PIN1	
Plug	P3_PD3	PIN1	
Plug	P3_PD4	PIN1	
Plug	P4_PD1	PIN1	
Plug	P4_PD2	PIN1	
Plug	P4_PD3	PIN1	
Plug	P4_PD4	PIN1	
BNC Elbow Connector	P5_Rx-PD1	BNC_RA CON	
BNC Elbow Connector	P5_Rx-PD2	BNC_RA CON	
Plug	P6_Rx-PD1	PIN1	
Plug	P6_Rx-PD2	PIN1	
Plug	P7_Rx-PD1	PIN1	
Plug	P7_Rx-PD2	PIN1	
Plug	P8_Rx-PD1	PIN1	
Plug	P8_Rx-PD2	PIN1	
BNC Elbow Connector	P9	BNC_RA CON	
BNC Elbow Connector	P10	BNC_RA CON	
BNC Elbow Connector	P11	BNC_RA CON	
Plug	P12	PIN1	
Plug	P13	PIN1	
Plug	P14	PIN1	
BNC Elbow Connector	P15_Phs-Conj-Loop1	BNC_RA CON	
BNC Elbow Connector	P15_Phs-Conj-Loop2	BNC_RA CON	
BNC Elbow Connector	P16_Phs-Conj-Loop1	BNC_RA CON	
BNC Elbow Connector	P16_Phs-Conj-Loop2	BNC_RA CON	
Plug	P17_Phs-Conj-Loop1	PIN1	
Plug	P17_Phs-Conj-Loop2	PIN1	
Plug	P18_Phs-Conj-Loop1	PIN1	
Plug	P18_Phs-Conj-Loop2	PIN1	
Plug	P19_Phs-Conj-Loop1	PIN1	
Plug	P19_Phs-Conj-Loop2	PIN1	
NPN RF Transistor	Q1	SO-G3	
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R1_PD1	ERA-0805	100

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R1_PD2	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R1_PD3	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R1_PD4	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R2_PD1	ERA-0805	50
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R2_PD2	ERA-0805	50
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R2_PD3	ERA-0805	50
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R2_PD4	ERA-0805	50
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R3_PD1	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R3_PD2	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R3_PD3	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R3_PD4	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R4_PD1	ERA-0805	50
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R4_PD2	ERA-0805	50
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R4_PD3	ERA-0805	50
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R4_PD4	ERA-0805	50
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R5_PD1	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R5_PD2	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R5_PD3	ERA-0805	INF

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R5_PD4	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R6_PD1	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R6_PD2	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R6_PD3	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R6_PD4	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R7_PD1	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R7_PD2	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R7_PD3	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R7_PD4	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R8_PD1	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R8_PD2	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R8_PD3	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R8_PD4	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R9_PD1	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R9_PD2	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R9_PD3	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R9_PD4	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R10_PD1	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R10_PD2	ERA-0805	0

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R10_PD3	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R10_PD4	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R11_PD1	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R11_PD2	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R11_PD3	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R11_PD4	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R12_PD1	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R12_PD2	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R12_PD3	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R12_PD4	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R13_PD1	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R13_PD2	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R13_PD3	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R13_PD4	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R14_PD1	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R14_PD2	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R14_PD3	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R14_PD4	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R15_PD1	ERA-0805	100

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R15_PD2	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R15_PD3	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R15_PD4	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R16_PD1	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R16_PD2	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R16_PD3	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R16_PD4	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R17_PD1	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R17_PD2	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R17_PD3	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R17_PD4	ERA-0805	0
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R18_PD1	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R18_PD2	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R18_PD3	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R18_PD4	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R19_Rx-PD1	ERA-0805	180k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R19_Rx-PD2	ERA-0805	180k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R20_Rx-PD1	ERA-0805	1K
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R20_Rx-PD2	ERA-0805	1K

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R21_Rx-PD1	ERA-0805	39
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R21_Rx-PD2	ERA-0805	39
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R22_Rx-PD1	ERA-0805	50k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R22_Rx-PD2	ERA-0805	50k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R23_Rx-PD1	ERA-0805	8.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R23_Rx-PD2	ERA-0805	8.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R24_Rx-PD1	ERA-0805	1.1k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R24_Rx-PD2	ERA-0805	1.1k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R25_Rx-PD1	ERA-0805	2.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R25_Rx-PD2	ERA-0805	2.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R26_Rx-PD1	ERA-0805	2.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R26_Rx-PD2	ERA-0805	2.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R27_Rx-PD1	ERA-0805	20k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R27_Rx-PD2	ERA-0805	20k
Resistor Array - Parts	R28_Rx-PD1	LCC4	1K
Resistor Array - Parts	R28_Rx-PD2	LCC4	1K
Potentiometer	R29_Rx-PD1	VR5	500
Potentiometer	R29_Rx-PD2	VR5	500
Potentiometer	R30_Rx-PD1	VR5	5K
Potentiometer	R30_Rx-PD2	VR5	5K
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R31	ERA-0805	2.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R32	ERA-0805	10k

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R33	ERA-0805	10k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R34	ERA-0805	50
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R35	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R36	ERA-0805	INF
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R37	ERA-0805	10k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R38	ERA-0805	10k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R39	ERA-0805	10k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R40	ERA-0805	0k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R41	ERA-0805	1K
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R42	ERA-0805	1K
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R43	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R44	ERA-0805	100
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R45_Phs-Conj-Loop1	ERA-0805	300
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R45_Phs-Conj-Loop2	ERA-0805	300
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R46_Phs-Conj-Loop1	ERA-0805	180k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R46_Phs-Conj-Loop2	ERA-0805	180k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R47_Phs-Conj-Loop1	ERA-0805	39
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R47_Phs-Conj-Loop2	ERA-0805	39
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R48_Phs-Conj-Loop1	ERA-0805	50k

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R48_Phs-Conj-Loop2	ERA-0805	50k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R49_Phs-Conj-Loop1	ERA-0805	8.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R49_Phs-Conj-Loop2	ERA-0805	8.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R50_Phs-Conj-Loop1	ERA-0805	1.1k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R50_Phs-Conj-Loop2	ERA-0805	1.1k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R51_Phs-Conj-Loop1	ERA-0805	2.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R51_Phs-Conj-Loop2	ERA-0805	2.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R52_Phs-Conj-Loop1	ERA-0805	43k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R52_Phs-Conj-Loop2	ERA-0805	43k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R53_Phs-Conj-Loop1	ERA-0805	2.7k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R53_Phs-Conj-Loop2	ERA-0805	2.7k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R54_Phs-Conj-Loop1	ERA-0805	1.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R54_Phs-Conj-Loop2	ERA-0805	1.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R55_Phs-Conj-Loop1	ERA-0805	20k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R55_Phs-Conj-Loop2	ERA-0805	20k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R56_Phs-Conj-Loop1	ERA-0805	2.2k
Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W	R56_Phs-Conj-Loop2	ERA-0805	2.2k
Resistor Array - Parts	R57_Phs-Conj-Loop1	LCC4	1K
Resistor Array - Parts	R57_Phs-Conj-Loop2	LCC4	1K
Potentiometer	R58_Phs-Conj-Loop1	VR5	500
Potentiometer	R58_Phs-Conj-Loop2	VR5	500

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Potentiometer	R59_Phs-Conj-Loop1	VR5	5K
Potentiometer	R59_Phs-Conj-Loop2	VR5	5K
Dual Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset	U1_PD1	D014	
Dual Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset	U1_PD2	D014	
Dual Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset	U1_PD3	D014	
Dual Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset	U1_PD4	D014	
Dual Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset	U2_PD1	D014	
Dual Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset	U2_PD2	D014	
Dual Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset	U2_PD3	D014	
Dual Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset	U2_PD4	D014	
Ultrafast Comparator	U3_PD1	SO-G6/P.95	
Ultrafast Comparator	U3_PD2	SO-G6/P.95	
Ultrafast Comparator	U3_PD3	SO-G6/P.95	
Ultrafast Comparator	U3_PD4	SO-G6/P.95	
Ultrafast Comparator	U4_PD1	SO-G6/P.95	
Ultrafast Comparator	U4_PD2	SO-G6/P.95	
Ultrafast Comparator	U4_PD3	SO-G6/P.95	
Ultrafast Comparator	U4_PD4	SO-G6/P.95	
Phs/Freq Discriminator	U5_PD1	P-20A	
Phs/Freq Discriminator	U5_PD2	P-20A	
Phs/Freq Discriminator	U5_PD3	P-20A	
Phs/Freq Discriminator	U5_PD4	P-20A	
Ultra-Low Offset Voltage Operational Amplifier	U6_Rx-PD1	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U6_Rx-PD2	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U7_Rx-PD1	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U7_Rx-PD2	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U8_Rx-PD1	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U8_Rx-PD2	R-8	
Dual, Low-Power Video Operational Amplifier	U9	R-8D	
Ultra-Low Offset Voltage Operational Amplifier	U10_Phs-Conj-Loop1	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U10_Phs-Conj-Loop2	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U11_Phs-Conj-Loop1	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U11_Phs-Conj-Loop2	R-8	

TABLE B-1 CONTINUED

Description	Designator	Footprint	Value
Ultra-Low Offset Voltage Operational Amplifier	U12_Phs-Conj-Loop1	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U12_Phs-Conj-Loop2	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U13_Phs-Conj-Loop1	R-8	
Ultra-Low Offset Voltage Operational Amplifier	U13_Phs-Conj-Loop2	R-8	

TABLE B-2
COMPONENT PART NUMBERS, DESCRIPTIONS, DESIGNATOR LIST, AND PACKAGE REFERENCES

Part Name	Pattern	Qnty.	Components	Description
1N4148	DO-35	2	D5_Phs-Conj-Loop1, D5_Phs-Conj-Loop2	High Conductance Fast Diode
1N5242B	SO-G3/G1	4	D1_Rx-PD1, D1_Rx-PD2, D4_Phs-Conj-Loop1, D4_Phs-Conj-Loop2	Half Watt Zener
74ACT11074D	D014	8	U1_PD1, U1_PD2, U1_PD3, U1_PD4, U2_PD1, U2_PD2, U2_PD3, U2_PD4	Dual Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset
AD828AR	R-8D	1	U9	Dual, Low-Power Video Operational Amplifier
AD9901	P-20A	4	U5_PD1, U5_PD2, U5_PD3, U5_PD4	Phs/Freq Discriminator
ADOP07CR	R-8	14	U6_Rx-PD1, U6_Rx-PD2, U7_Rx-PD1, U7_Rx-PD2, U8_Rx-PD1, U8_Rx-PD2, U10_Phs-Conj-Loop1, U10_Phs-Conj-Loop2, U11_Phs-Conj-Loop1, U11_Phs-Conj-Loop2, U12_Phs-Conj-Loop1, U12_Phs-Conj-Loop2, U13_Phs-Conj-Loop1, U13_Phs-Conj-Loop2	Ultra-Low Offset Voltage Operational Amplifier
BB639	SOD-323	2	D2, D3	Silicon Variable-Capacitance Diode for Tuning of Extended Frequency Band in VHF TV/VTR Tuners
BNC	BNC_RA CON	17	P1_PD1, P1_PD2, P1_PD3, P1_PD4, P2_PD1, P2_PD2, P2_PD3, P2_PD4, P5_Rx-PD1, P5_Rx-PD2, P9, P10, P11, P15_Phs-Conj-Loop1, P15_Phs-Conj-Loop2, P16_Phs-Conj-Loop1, P16_Phs-Conj-Loop2	BNC Elbow Connector
C0805	CC2012-0805	2	C49_Phs-Conj-Loop1, C49_Phs-Conj-Loop2	Ceramic Chip Capacitor - Standard
C0805	CR2012-0805	2	C32, C33	Ceramic Chip Capacitor - Standard

TABLE B-2 CONTINUED

Part Name	Pattern	Qnty.	Components	Description
C1206	1206	78	C1_PD1, C1_PD2, C1_PD3, C1_PD4, C2_PD1, C2_PD2, C2_PD3, C2_PD4, C3_PD1, C3_PD2, C3_PD3, C3_PD4, C4_PD1, C4_PD2, C4_PD3, C4_PD4, C5_PD1, C5_PD2, C5_PD3, C5_PD4, C6_PD1, C6_PD2, C6_PD3, C6_PD4, C7_PD1, C7_PD2, C7_PD3, C7_PD4, C9_Rx-PD1, C9_Rx-PD2, C10_Rx-PD1, C10_Rx-PD2, C11_Rx-PD1, C11_Rx-PD2, C12_Rx-PD1, C12_Rx-PD2, C13_Rx-PD1, C13_Rx-PD2, C14_Rx-PD1, C14_Rx-PD2, C15_Rx-PD1, C15_Rx-PD2, C16_Rx-PD1, C16_Rx-PD2, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C34_Phs-Conj-Loop1, C34_Phs-Conj-Loop2, C35_Phs-Conj-Loop1, C35_Phs-Conj-Loop2, C36_Phs-Conj-Loop1, C36_Phs-Conj-Loop2, C37_Phs-Conj-Loop1, C37_Phs-Conj-Loop2, C38_Phs-Conj-Loop1, C38_Phs-Conj-Loop2, C39_Phs-Conj-Loop1, C39_Phs-Conj-Loop2, C40_Phs-Conj-Loop1, C40_Phs-Conj-Loop2, C41_Phs-Conj-Loop1, C41_Phs-Conj-Loop2, C42_Phs-Conj-Loop1, C42_Phs-Conj-Loop2, C43_Phs-Conj-Loop1, C43_Phs-Conj-Loop2, C44_Phs-Conj-Loop1, C44_Phs-Conj-Loop2, C45_Phs-Conj-Loop1, C45_Phs-Conj-Loop2	Ceramic Chip Capacitor - Standard
C6032	Cap6032	18	C8_PD1, C8_PD2, C8_PD3, C8_PD4, C17_Rx-PD1, C17_Rx-PD2, C18_Rx-PD1, C18_Rx-PD2, C19_Rx-PD1, C19_Rx-PD2, C30, C31, C46_Phs-Conj-Loop1, C46_Phs-Conj-Loop2, C47_Phs-Conj-Loop1, C47_Phs-Conj-Loop2, C48_Phs-Conj-Loop1, C48_Phs-Conj-Loop2	Tantalum Chip Capacitor - Standard

TABLE B-2 CONTINUED

Part Name	Pattern	Qnty.	Components	Description
ERA6Y	ERA-0805	128	R1_PD1, R1_PD2, R1_PD3, R1_PD4, R2_PD1, R2_PD2, R2_PD3, R2_PD4, R3_PD1, R3_PD2, R3_PD3, R3_PD4, R4_PD1, R4_PD2, R4_PD3, R4_PD4, R5_PD1, R5_PD2, R5_PD3, R5_PD4, R6_PD1, R6_PD2, R6_PD3, R6_PD4, R7_PD1, R7_PD2, R7_PD3, R7_PD4, R8_PD1, R8_PD2, R8_PD3, R8_PD4, R9_PD1, R9_PD2, R9_PD3, R9_PD4, R10_PD1, R10_PD2, R10_PD3, R10_PD4, R11_PD1, R11_PD2, R11_PD3, R11_PD4, R12_PD1, R12_PD2, R12_PD3, R12_PD4, R13_PD1, R13_PD2, R13_PD3, R13_PD4, R14_PD1, R14_PD2, R14_PD3, R14_PD4, R15_PD1, R15_PD2, R15_PD3, R15_PD4, R16_PD1, R16_PD2, R16_PD3, R16_PD4, R17_PD1, R17_PD2, R17_PD3, R17_PD4, R18_PD1, R18_PD2, R18_PD3, R18_PD4, R19_Rx-PD1, R19_Rx-PD2, R20_Rx-PD1, R20_Rx-PD2, R21_Rx-PD1, R21_Rx-PD2, R22_Rx-PD1, R22_Rx-PD2, R23_Rx-PD1, R23_Rx-PD2, R24_Rx-PD1, R24_Rx-PD2, R25_Rx-PD1, R25_Rx-PD2, R26_Rx-PD1, R26_Rx-PD2, R27_Rx-PD1, R27_Rx-PD2, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45_Phs-Conj-Loop1, R45_Phs-Conj-Loop2, R46_Phs-Conj-Loop1, R46_Phs-Conj-Loop2, R47_Phs-Conj-Loop1, R47_Phs-Conj-Loop2, R48_Phs-Conj-Loop1, R48_Phs-Conj-Loop2, R49_Phs-Conj-Loop1, R49_Phs-Conj-Loop2, R50_Phs-Conj-Loop1, R50_Phs-Conj-Loop2, R51_Phs-Conj-Loop1, R51_Phs-Conj-Loop2, R52_Phs-Conj-Loop1, R52_Phs-Conj-Loop2, R53_Phs-Conj-Loop1, R53_Phs-Conj-Loop2, R54_Phs-Conj-Loop1, R54_Phs-Conj-Loop2, R55_Phs-Conj-Loop1, R55_Phs-Conj-Loop2, R56_Phs-Conj-Loop1, R56_Phs-Conj-Loop2	Rectangular Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 0.1% and 0.5% Tolerance, 0805 Size, 0.1 W
Inductor	CC4532-1812	2	L1, L2	Inductor
LT1719	SO-G6/P.95	8	U3_PD1, U3_PD2, U3_PD3, U3_PD4, U4_PD1, U4_PD2, U4_PD3, U4_PD4	Ultrafast Comparator
MMBTH10	SO-G3	1	Q1	NPN RF Transistor
Plug	PIN1	23	P3_PD1, P3_PD2, P3_PD3, P3_PD4, P4_PD1, P4_PD2, P4_PD3, P4_PD4, P6_Rx-PD1, P6_Rx-PD2, P7_Rx-PD1, P7_Rx-PD2, P8_Rx-PD1, P8_Rx-PD2, P12, P13, P14, P17_Phs-Conj-Loop1, P17_Phs-Conj-Loop2, P18_Phs-Conj-Loop1, P18_Phs-Conj-Loop2, P19_Phs-Conj-Loop1, P19_Phs-Conj-Loop2	Plug
Res Pack1	LCC4	4	R28_Rx-PD1, R28_Rx-PD2, R57_Phs-Conj-Loop1, R57_Phs-Conj-Loop2	Resistor Array - Parts
RPot	VR5	8	R29_Rx-PD1, R29_Rx-PD2, R30_Rx-PD1, R30_Rx-PD2, R58_Phs-Conj-Loop1, R58_Phs-Conj-Loop2, R59_Phs-Conj-Loop1, R59_Phs-Conj-Loop2	Potentiometer

APPENDIX C

PCL COMPONENT VALUES MATLAB PROGRAM

The program presented in Appendix C used the control equations derived in Chapter III to obtain values for control loop components to achieve a stable phase control loop.

```
% Samuel Kokel        7.10.2004
%
%
% This program helps obtain the values for a phase control loop.
% Loop bandwidth and dampening are obtained from the user.
% Capacitor values are set in the code.
% Ideal resistor values are determined and displayed to the user.
% The user then modifies the presented values to standard values to
% be implemented on a PCB.
% The modified values are used in place of the ideal ones.
% The transfer function of the loop is used to create bode plots of
% the various loop components inlcuding the entire closed loop.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%5

clear;
wo=10e9;        %Used for graph limits
pi=4*atan(1);

%Phase Detct & VCO Gain
PDgain=3.263;                   %(mV/deg)
Kpd = PDgain/1000/(2*pi/360);   %(V/rad)
VCOgain=1e6/5;                  %(Hz/V)
Kvco = VCOgain*2*pi;            %(Rad/s/V)

fn=input('Loop frequency  = ? ')
wn=fn*2*pi;
eta=input('Damping Constant  = ? ')
TL1=Kvco*Kpd/wn^2
TP1=2*eta/wn
TL1oTP1=TL1/TP1
CP=4.7e-6
```

```
CL=400e-9
RP2=TP1/CP
RP2=input('RP2 = ? ')
TP2 = TP1*(TL1oTP1)^.5*.7
RP1=TP2/CP-RP2
RP1=input('RP1 = ? ')
TL2=TP2
RL2=TL2/CL
RL2=input('RL2 = ? ')
RL1=TL1/CL
RL1=input('RL1 = ? ')
%eta = 1  %   % error on pole match

TL1=CL*RL1;
TL2=CL*RL2;
TL3=CL*(RL1+RL2);
TP1=CP*RP2;
TP2=CP*(RP1+RP2);

s = tf('s');
t   =   strcat('TL1=',num2str(TL1,4),'   TL2=',num2str(TL2,4),'   TL3=',num2str(TL3,4),'
TP1=',num2str(TP1,4),' TP2=',num2str(TP2,4))

%   Txfr Functs and poles  ----------------------------------------

Flp = -1*(1+TL2*s)/(s*TL1);
[p,z] = pzmap(Flp);


Flk = (TL3*s+1)/(TL1*s);
[p,z] = pzmap(Flk);


Fpd = (1+TP1*s)/(1+TP2*s);
[p,z] = pzmap(Fpd);
poles_of_Fpd = p


Hol=(-1)*Kpd*Kvco/s*Fpd*Flp
[p,z] = pzmap(Hol);
poles_of_Hol = p
```

```
Hp = (-1*Kpd*Kvco/s*Fpd*Flp)/(1+(-1)*Kpd*Kvco/s*Fpd*Flp)
[p,z] = pzmap(Hp);
poles_of_Hp = p
% zeros_of_Hp = z
[Gm_Hp,Pm_Hp,Wcg_Hp,Wcp_Hp] = margin(Hp)

Hv = (Flk*Kvco/s)/(1-Kvco/s*Flp*Fpd*Kpd)
[p,z] = pzmap(Hv);
poles_of_Hv = p
% zeros_of_Hv = z
[Gm_Hv,Pm_Hv,Wcg_Hv,Wcp_Hv] = margin(Hv)

figure(1)
set(1,'Name',strcat('Open loop Control  Hp',t))

subplot(3,2,1);
bode(Fpd, {.1,wo});
title(strcat('Fpd = (1+TP1*s)/(1+TP2*s)   ', t));

subplot(3,2,2);
bode(Flk, {.1,wo});
title(strcat('Flk = (TL3*s+1)/(TL1*s)   ', t));

subplot(3,2,3);
bode(Flp, {.1,wo});
title(strcat('Flp = -1*(1+TL2*s)/(s*TL1)   ', t));

subplot(3,2,5);
bode(Hol, {.1,wo});
title(strcat('Hol=(-1)*Kpd*Kvco/s*Fpd*Flp   ', t));

subplot(3,2,6);
pzmap(Hol);
title(strcat('Hol  P-Z Map   ', t));


figure(2);
set(2,'Name',strcat('Closed Loop Conrol Hp', t));

subplot(2,2,1);
margin(Hp)%, {.1,wo});
title(strcat('Hp Bode   ', t));
```

```
subplot(2,2,2);
pzmap(Hp);
title(strcat('Hp  P-Z Map   ', t));

subplot(2,2,3);
margin(Hv)%, {.1,wo});
title(strcat('Hv Bode   ', t));

subplot(2,2,4);
pzmap(Hv);
title(strcat('Hv  P-Z Map   ', t));
```

VITA

Samuel John Kokel was born in Austin, Texas on January 22, 1979. In May of 2002 he received a Bachelor of Science degree in electrical engineering cum laude from Texas A&M University in College Station, Texas. As an undergraduate he participated in the co-operative education program and spent three alternating semesters as a worker for National Instruments in Austin, Texas where he helped design and test data acquisition products. After receiving his B.S. he worked from May 2002 to October 2004 as a research assistant in the Electromagnetics and Microwave Laboratory at Texas A&M while pursuing his master's degree. He spent the summer of 2003 as an invited researcher at Kobe University in Kobe, Japan investigating phased array beam steering as related to the topic of microwave wireless power transmission. He will receive his Master of Science in electrical engineering from Texas A&M in December 2004. He was awarded a government scholarship from the Monbusho of Japan and will pursue a Doctor of Engineering degree at Kobe University. His current research includes microwave circuits, antennas, and retrodirecitive beam steering. He can currently be contacted by email at samuel-kokel@ieee.org or through the Department of Electrical Engineering at Texas A&M University at the address of 214 Zachry Engineering Center, College Station, TX 77843.