DESIGN AND IMPLEMENTATION OF LOW POWER MULTISTAGE AMPLIFIERS AND HIGH FREQUENCY DISTRIBUTED AMPLIFIERS

A Thesis

by

CHINMAYA MISHRA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2004

Major Subject: Electrical Engineering

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Approved as to style and content by:

Edgar Sánchez-Sinencio (Chair of Committee)	Jose Silva-Martinez (Member)
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Major Subject: Electrical Engineering

ABSTRACT

Design and Implementation of Low Power Multistage Amplifiers and High Frequency Distributed Amplifiers.

(August 2004)

Chinmaya Mishra, B.E. (Hons.), Birla Institute of Technology and Science, Pilani, India

Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

The advancement in integrated circuit (IC) technology has resulted in scaling down of device sizes and supply voltages without proportionally scaling down the threshold voltage of the MOS transistor. This, coupled with the increasing demand for low power, portable, battery-operated electronic devices, like mobile phones, and laptops provides the impetus for further research towards achieving higher integration on chip and low power consumption. High gain, wide bandwidth amplifiers driving large capacitive loads serve as error amplifiers in low-voltage low drop out regulators in portable devices. This demands low power, low area, and frequency-compensated multistage amplifiers capable of driving large capacitive loads. The first part of the research proposes two power and area efficient frequency compensation schemes: Single Miller Capacitor Compensation (SMC) and Single Miller Capacitor Feedforward Compensation (SMFFC), for multistage amplifiers driving large capacitive loads. The designs have been implemented in a 0.5µm CMOS process. Experimental results show

that the SMC and SMFFC amplifiers achieve gain-bandwidth products of 4.6MHz and 9MHz, respectively, when driving a load of 25KΩ/120pF. Each amplifier operates from a ±1V supply, dissipates less than 0.42mW of power and occupies less than 0.02mm^2 of silicon area.

The inception of the latest IEEE standard like IEEE 802.16 wireless metropolitan area network (WMAN) for 10 - 66 GHz range demands wide band amplifiers operating at high frequencies to serve as front-end circuits (e.g. low noise amplifier) in such receiver architectures. Devices used in cascade (multistage amplifiers) can be used to increase the gain but it is achieved at an expense of bandwidth. Distributing the capacitance associated with the input and the output of the device over a ladder structure (which is periodic), rather than considering it to be lumped can achieve an extension of bandwidth without sacrificing gain. This concept which is also known as distributed amplification has been explored in the second part of the research. This work proposes certain guidelines for the design of distributed low noise amplifiers operating at very high frequencies. Noise analysis of the distributed amplifier with real transmission lines is introduced. The analysis for gain and noise figure is verified with simulation results from a 5-stage distributed amplifier implemented in a 0.18µm CMOS process.

DEDICATION

To my Parents and Brother.

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I would like to thank several people, who have made my graduate life at Texas A&M University a pleasant and enriching experience.

First, I would like to express my sincere gratitude to my advisor Dr. Edgar Sánchez-Sinencio for his constant support and guidance. He has always been a source of encouragement and inspiration. I am deeply indebted to him for providing me financial assistance during my entire course of study. I am very thankful to him for allowing me to work on different challenging research areas under his supervision.

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the project on multistage amplifiers as well as on distributed circuits. Thanks to Chunyu Xin for his guidance and help on the project on distributed amplifiers. I have learned a lot from these people during the course of the projects. Their diligence and perseverance was very motivating.

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CHAPTER I

INTRODUCTION

The design of high gain and wide bandwidth amplifiers using single stage cascode or telescopic amplifiers becomes increasingly difficult with the scaling of device sizes due to less voltage swings and output impedance degradation in sub-micron technologies, forcing designers to take recourse to multistage topologies. Multistage amplifiers are based on cascading of gain stages horizontally to improve the gain while operating in low voltage conditions [1]. But because of their multiple-pole nature, these amplifiers suffer from closed loop stability problems. Hence phase compensation techniques become very essential to stabilize these amplifiers. Towards this end there has been quite a number of compensation schemes [2-11] reported to improve stability, frequency and transient responses of the multistage amplifiers.

High gain, wide bandwidth amplifiers driving large capacitive loads and requiring low power serve as the error amplifier in a linear regulator [6] where large capacitors in the order of nano or micro Farads form the load. The main bottleneck of such amplifiers is that the pole at the output is pulled inside (very close to the dominant pole) which greatly limits the bandwidth and makes the compensation of the amplifier difficult under low power and low area constraint. Compensation using capacitors or using feedforward paths are the two most commonly used frequency compensation

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This thesis follows the style and format of *IEEE Journal of Solid-State Circuits*.

techniques in multistage amplifiers. Most of the techniques reported for multistage amplifiers driving large capacitive loads invariably use two capacitors for compensation, which greatly contributes, to the circuit area. Especially when loads are large these compensation capacitors also increase in size further increasing the area. Some of the implementations use active capacitors to reduce the size of the physical capacitor thereby reducing the silicon area [10-11]. The gain bandwidth product (GBW) of these amplifiers is still limited and hence demands robust frequency compensation schemes, which can improve the GBW without sacrificing in power or area.

Two low power, efficient three stage amplifier topologies are presented in this work: Single Miller Capacitor Compensation (SMC) and Single Miller Capacitor Feedforward Compensation (SMFFC). The use of a single Miller capacitor for compensation in three stage amplifiers is explored. Experimental results show that the SMC and SMFFC amplifiers achieve gain-bandwidth products of 4.6MHz and 9MHz, respectively, when driving a load of 25KΩ/120pF. Each amplifier operates from a ±1V supply, dissipates less than 0.42mW of power and occupies less than 0.02mm^2 of silicon area [12].

At very high frequencies i.e. GHz range, multistage amplifiers are not suitable because of the difficulty involved in controlling too many poles and zeroes of the amplifiers. Devices used in cascade can be used to increase the gain but it is achieved at an expense of bandwidth, because the bandwidth of a multi stage amplifier is less than that of a single stage amplifier. The GBW of an amplifier is very much dependent on g_m and C of the active device both of which are intrinsic parameters of the device, and are

not easily alterable once the device is fabricated [13]. Although the f_t (unity gain frequency) of the transistors are comparatively higher in submicron technologies, the circuits built with these transistors do not operate at such high frequencies, the reason being the parasitics associated at high frequencies. Using the concept of distributed amplification helps alleviate this problem by distributing the capacitance associated with the active device over a periodic ladder structure consisting of inductors and capacitors (which emulates a transmission line) and at the same time summing the signal outputs of various stages to maintain the gain. This type of circuit is called distributed because it uses multiple parallel signal paths and devices working in harmony to perform a desired task [14].

Distributed circuits are very common in microwave implementations. Since distributed circuits aid in overcoming the frequency and power limitations of conventional circuits these circuits are currently being explored in CMOS technologies. Distributed amplifiers (DA) can serve as low noise front-ends in broadband wireless receivers operating at very high frequencies. There are very few implementations of DAs using real transmission lines in CMOS. CMOS being cost effective, the implementation of distributed amplifiers with transmission lines is explored and design considerations for the design of distributed amplifiers serving as low noise amplifiers are proposed in this work.

CHAPTER II

FREQUENCY COMPENSATION IN MULTISTAGE AMPLIFIERS

2.1. Background and Motivation

Many phase compensation techniques for multistage amplifiers have been proposed in recent years. Table 2.1 summarizes the results of some of the techniques.

Table 2.1. Summary of multistage amplifier topologies

Parameter	C_L (pF)	Gain (dB)	GBW (MHz)	SR^+ (V/μS)	Power (mw@Vdd)	FOM_S (MHz.pF/mW)	FOM_L (V/μS.pF/mW)	Technology
NMC [2]	100	100	60	20	76 @ 8	79	26	3 GHz f_t BJT
MNMC [2]	100	100	100	35	76 @ 8	132	46	3 GHz f_t BJT
NGCC [3]	20	100	0.61	2.5	0.68 @ 2	18	74	2 μm CMOS
NMCFNR [4]	100	>100	1.8	0.79	0.406 @ 2	443	195	0.8 μm CMOS
ETC [5]	40	102	47	69	6.9 @ 3	272	400	0.6 μm CMOS
DFCFC [6], [7]	100	>100	2.6	1.32	0.42 @ 2	619	314	0.8 μm CMOS
NCFF [8]	12	90	250	*	14 @ 2.5	214	*	0.5 μm CMOS
PFC [9]	130	>100	2.7	1	0.275 @ 1.5	1276	473	0.35 μm CMOS
AFFC [10]	120	>100	4.5	1.49	0.4 @ 2	1350	447	0.8 μm CMOS
DLPC [11]	120	>100	7	3.3	0.33 @ 1.5	2545	1200	0.6 μm CMOS

$^+$ Average value used * Slew rate values were not reported

Next, a brief overview of the different phase compensation schemes so far reported in the literature is given. Nested Miller compensation (NMC) [2] is a well-established pole splitting technique for phase compensation. But it has been shown [2] that it has a major drawback, i.e. bandwidth reduction when using large number of stages. Again the creation of a RHP zero by the Miller capacitor requires a large output conductance in the last stage, to ensure stability, making it unsuitable for low power applications. These drawbacks led to the multipath nested Miller compensation (MNMC) [2] which used a feedforward path to create a LHP zero for canceling the non dominant poles within the pass-band of the amplifier and thereby improving the bandwidth of the overall amplifier. To improve stability by removing the RHP zero in the NMC, phase compensation schemes like nested Gm-C compensation (NGCC) [3] and NMC with feedforward transconductance stage and nulling resistor (NMCFNR) [4] were reported. But the bandwidth improvement of these structures was not that significant while driving large capacitive loads. Hence to improve the bandwidth significantly the embedded tracking compensation (ETC) [5] and damping factor control frequency compensation (DFCFC) [6], [7] were developed with the idea of reducing the capacitive load at the output for higher bandwidth operation.

All the above compensation techniques use Miller capacitor whose size depends on the size of the load capacitor and hence for higher loads the sizes of the Miller capacitors results in more area. Besides this, the above techniques use passive capacitive feedback networks, which limit the bandwidth of the amplifier for high frequency applications under low power operation.

The above topologies were followed by new approaches such as, the no capacitor feedforward technique (NCFF) [8] and the active feedback frequency compensation (AFFC) [10] technique. NCFF is based on pole zero cancellation technique at high frequencies resulting in higher bandwidth and higher settling time. But the pole zero cancellation is done by the high-speed feed forward paths, and hence more power consumption. Besides, NCFF also uses small load capacitors. The AFFC technique is a low power topology, which uses an active capacitor in place of a passive one, and hence a smaller capacitor size. Again, it uses a high-speed block with a feedforward path to enhance the bandwidth and the transient response of the amplifier.

Another compensation technique known as positive feedback compensation technique (PFC) [9], removes the inner compensation capacitor reducing the loading of the output, to enhance the bandwidth. A modification to the AFFC topology results in what is known as dual loop parallel compensation technique (DLPC) [11]. It uses a damping factor control block instead of a Miller capacitor between the second and third stage thereby reducing the loading at the output. The comparison of bandwidth using different pole splitting techniques [11] shows that this topology has the largest bandwidth while driving a 120pF load and using very low power and area.

2.2. Overview of Existing Multistage Amplifiers

Before proposing the new topologies we briefly discuss some of the existing topologies which are considered to be viable candidates for large load applications. The discussion includes NMC, DFCFC, AFFC, PFC and DLPC amplifiers. The following

assumptions are made: (a) the gains of all the stages are much greater than 1 (i.e. $\left(\frac{g_{mi}}{g_{oi}}\right)_{i=1,2} >> 1$ and $\left(\frac{g_{mL}}{g_L}\right) >> 1$), where g_m is the transconductance and g_o is the output conductance and g_L is the loading conductance, (b) the loading and compensation capacitors are much greater than the lumped output parasitic capacitance of each stage (i.e. C_L and $C_m >> C_p$) and, (c) interstage coupling capacitances are negligible.

2.2.1. Nested Miller Compensation

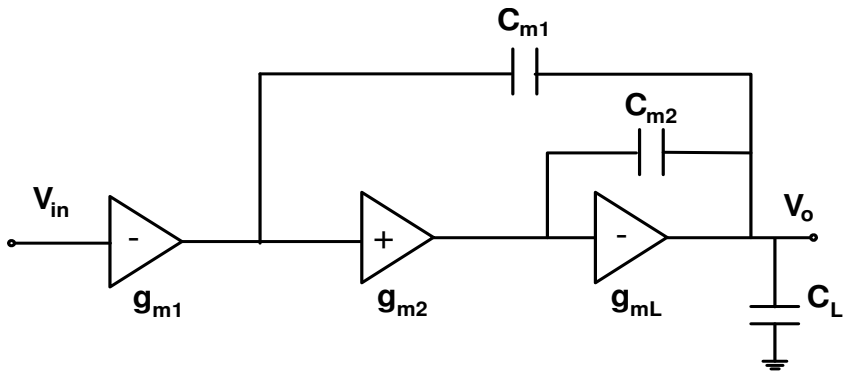


Fig. 2.1. Three stage NMC amplifier

Fig. 2.1 shows the block diagram of a NMC amplifier. The transfer function [7] is given by

$$A_{v(NMC)} \approx \frac{1}{\left(\frac{sC_{m1}}{g_{m1}}\right)\left(1 + s\frac{C_{m2}}{g_{m2}} + s^2\frac{C_L C_{m2}}{g_{m2} g_{mL}}\right)} \tag{2.1}$$

The dc gain and GBW [7] are given by

$$A_v = \frac{g_{m1} g_{m2} g_{mL}}{g_{o1} g_{o2} g_L} \tag{2.2}$$

$$GBW = \frac{g_{m1}}{C_{m1}} \tag{2.3}$$

Assuming that $g_{mL} >> g_{m1}$ and g_{m2} and the zeroes locate at higher frequencies, for a Butterworth unity feedback response the dimension conditions for the compensation capacitors are

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right) C_L \tag{2.4}$$

$$C_{m2} = 2\left(\frac{g_{m2}}{g_{mL}}\right) C_L \tag{2.5}$$

which result in large values for large load capacitors.

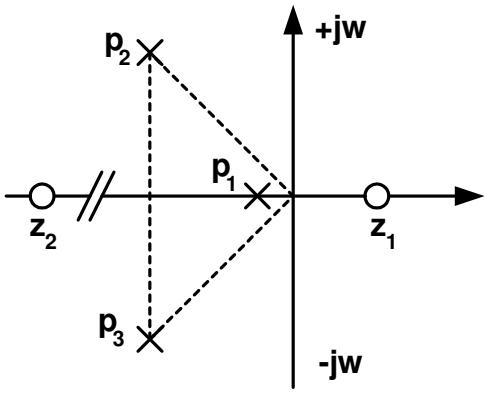


Fig. 2.2. Pole-zero diagram for the NMC amplifier

Fig 2.2 shows the pole-zero diagram after compensation. After compensation there is a dominant pole p_1 and two non-dominant complex poles p_2 and p_3 with a damping factor

equal to $\frac{1}{\sqrt{2}}$. Large load capacitors limit the GBW to a great extent as C_{m1} also increases. The transconductance of the last stage g_{mL} in NMC needs to be very high as compared to g_{m1} and g_{m2} in order to ensure stability by avoiding the right half plane (RHP) zero due to the Miller capacitor at lower frequency. This implies higher power consumption.

2.2.2. Damping-Factor-Control Frequency Compensation

Fig. 2.3 shows the block diagram of the three stage DFCFC amplifier. The transfer function [6] is given by

$$A_{v(DFCFC)} \approx \frac{1+s\frac{C_{p2}g_{mf2}-C_{m1}g_{m4}}{g_{m2}g_{mL}+g_{mf2}g_{m4}}-s^2\frac{C_{p2}C_{m1}}{g_{m2}g_{mL}+g_{mf2}g_{m4}}}{\left(\frac{sC_{m1}}{g_{m1}}\right)\left(1+s\frac{C_Lg_{m4}}{g_{m2}g_{mL}+g_{mf2}g_{m4}}+s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}+g_{mf2}g_{m4}}\right)} \tag{2.6}$$

The dc gain and GBW are given by [7]

$$A_v = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L} \tag{2.7}$$

$$GBW = \frac{\beta}{4}\left(\frac{g_{mL}}{C_L}\right) \tag{2.8}$$

and the stability conditions [7] can be outlined as follows:

$$g_{mf2} = g_{mL} \tag{2.9}$$

$$g_{m4} = \beta\left(\frac{C_{p2}}{C_L}\right)g_{mL} \tag{2.10}$$

$$C_{m1} = \frac{4}{\beta}\left(\frac{g_{m1}}{g_{mL}}\right)C_L \tag{2.11}$$

$$C_{m1} >> C_{m2} > C_{p2} \tag{2.12}$$

where $\beta = 1 + \sqrt{1 + 2\left(\frac{C_L}{C_{p2}}\right)\frac{g_{m2}}{g_{mL}}}$.

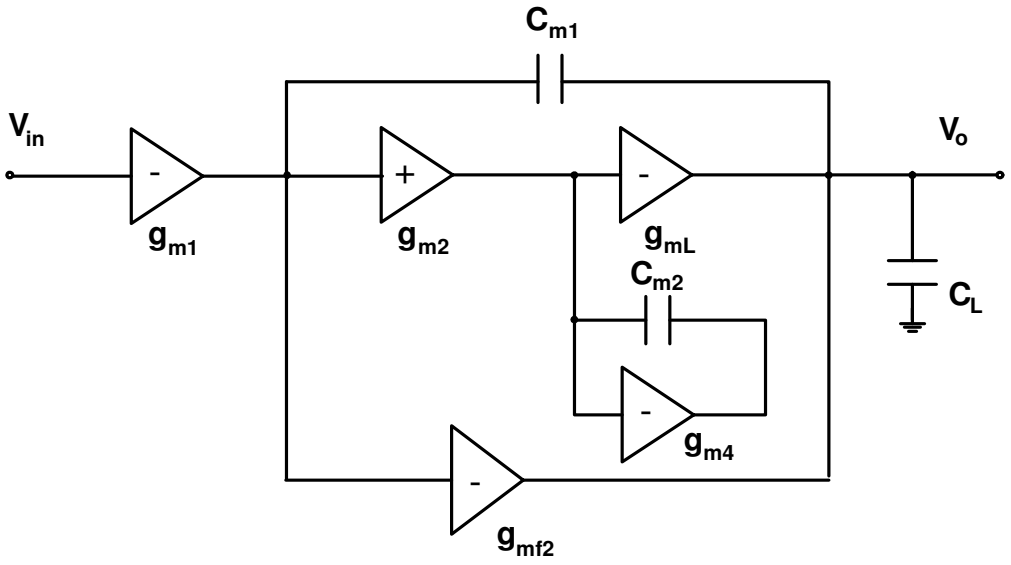


Fig. 2.3. Three stage DFCFC amplifier

The pole-zero diagram is shown in Fig. 2.4. The structure results in a pair of complex non-dominant poles. This topology helps in substantially increasing the bandwidth of the amplifier especially when driving large capacitive loads, along with improved transient response and power supply rejection ratio [6]. The compensation capacitors are also small in size, greatly reducing the area of the circuit, but there is a slight increase in power consumption and circuit complexity.

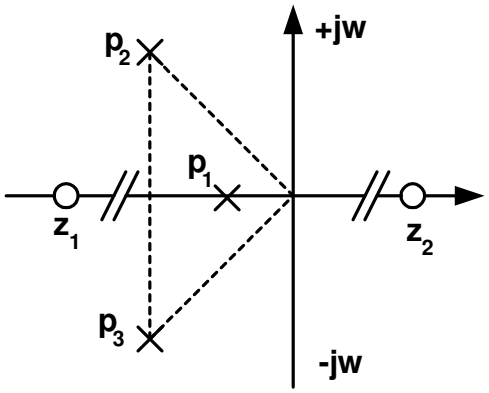


Fig. 2.4. Pole-zero diagram for the DFCFC amplifier.

2.2.3. Positive Feedback Compensation

Fig. 2.5 shows a three stage positive feedback compensated amplifier. The structure avoids an inner Miller capacitor between the second and last stage there by reducing the loading at the output.

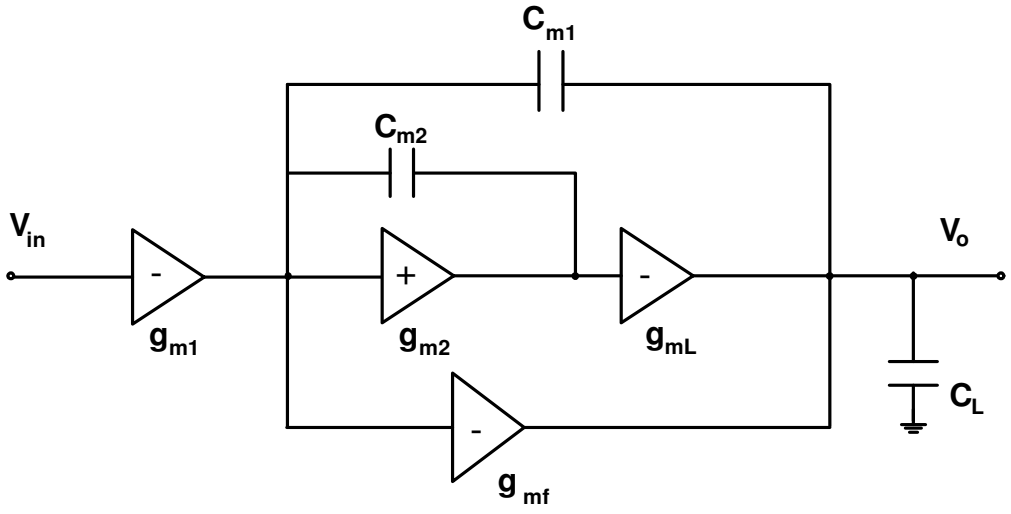


Fig. 2.5. Three stage PFC amplifier

The dc gain and GBW are given by [9]

$$A_v = \frac{g_{m1} g_{m2} g_{mL}}{g_{o1} g_{o2} g_L} \tag{2.13}$$

$$GBW = \frac{\beta}{4}\left(\frac{g_{mL}}{C_L}\right) \tag{2.14}$$

where $\beta = \frac{7}{2}\sqrt{\left(\frac{C_L}{C_{m2} + C_{p2}}\right)\frac{g_{m2}}{g_{mL}}}$.

The stability conditions [9] can be outlined as follows:

$$g_{mf} = g_{mL} \tag{2.15}$$

The pole-zero diagram for the amplifier is shown in Fig. 2.6. The amplifier has two complex non-dominant poles, the damping factor of which is controlled by C_{m2}. The left-half plane zero helps in improving the phase margin.

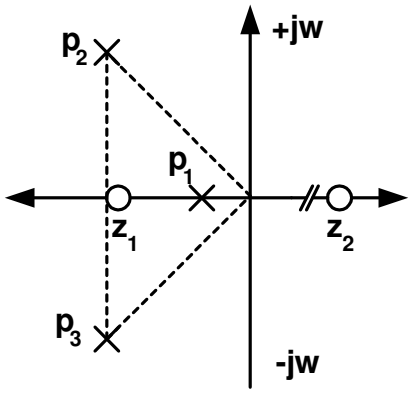


Fig. 2.6. Pole-zero diagram for the PFC amplifier

2.2.4. Active Feedback Frequency Compensation

Fig. 2.7 shows the block diagram of the three stage AFFC amplifier. The transfer function of the amplifier is given by

$$A_{v(AFFC)} \approx \frac{\left(1+s\frac{C_a}{g_{ma}}\right)}{\left(\frac{sC_a}{g_{m1}}\right)\left(1+s\frac{C_{p1}C_L}{C_a\left(g_{mf}-g_{m2}\right)}+s^2\frac{C_{p1}C_L}{g_{ma}\left(g_{mf}-g_{m2}\right)}\right)} \tag{2.16}$$

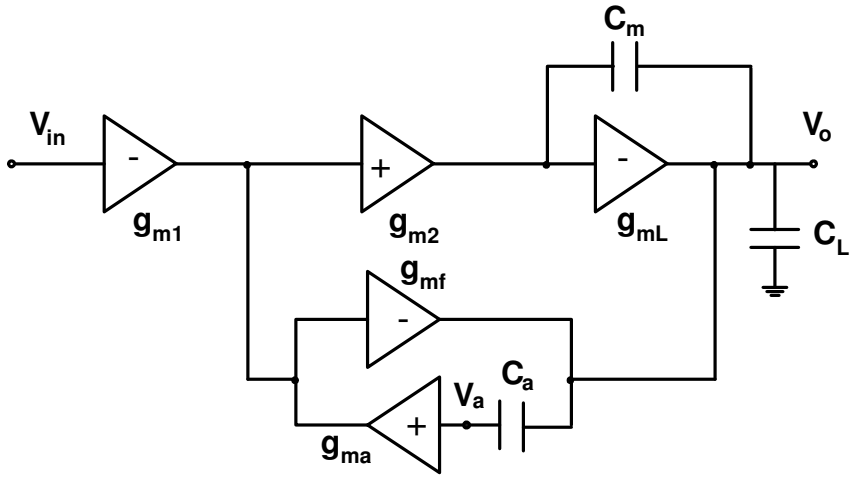


Fig. 2.7. Three stage AFFC amplifier

The dc gain and GBW are given by [10]

$$A_v = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L} \tag{2.17}$$

$$GBW = \frac{g_{m1}}{C_a} \tag{2.18}$$

The stability conditions [10] can be outlined as follows:

$$g_{mf} > g_{m2} \tag{2.19}$$

$$g_{ma} = 4g_{m1} \tag{2.20}$$

resulting in $C_a = C_m = \frac{4}{N}\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ where $N = \sqrt{8\left(\frac{C_L}{C_{p1}}\right)\left[\frac{g_{m1}\left(g_{mf} - g_{m2}\right)}{g_{mL}^2}\right]}$.

This topology replaces the C_{m1} of NMC with an active-capacitive-feedback network, in which an active positive gain stage is added in series with the dominant compensation capacitor so that the required compensation capacitor is very small. This greatly reduces the amplifier area and both the bandwidth and transient response are improved. But this circuit still uses two capacitors. Fig. 2.8 shows the pole-zero diagram of the AFFC amplifier based on the transfer function (2.16). The LHP zero helps in boosting the phase margin of the amplifier.

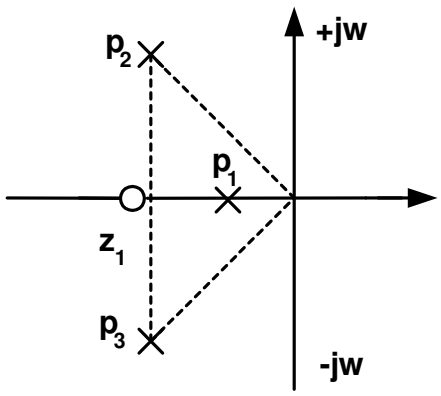


Fig. 2.8. Pole-zero diagram of the AFFC amplifier

2.2.5. Dual-Loop Parallel Compensation

Fig. 2.9 shows the dual path amplifier topology with dual loop parallel compensation scheme. The scheme is the same as AFFC technique without the Miller capacitor around the third stage, thereby reducing the loading at the output. Hence this technique achieves a higher bandwidth as compared to other reported topologies. Besides, avoiding a Miller capacitor around the last stage provides another high speed path as the node at the output of the second stage is no more loaded by the amplified Miller capacitance. The dc gain and GBW are given by [11]

$$A_v = \frac{g_{m1} g_{m2} g_{mL}}{g_{o1} g_{o2} g_L} \tag{2.21}$$

$$GBW = \frac{g_{m1}}{C_a} \tag{2.22}$$

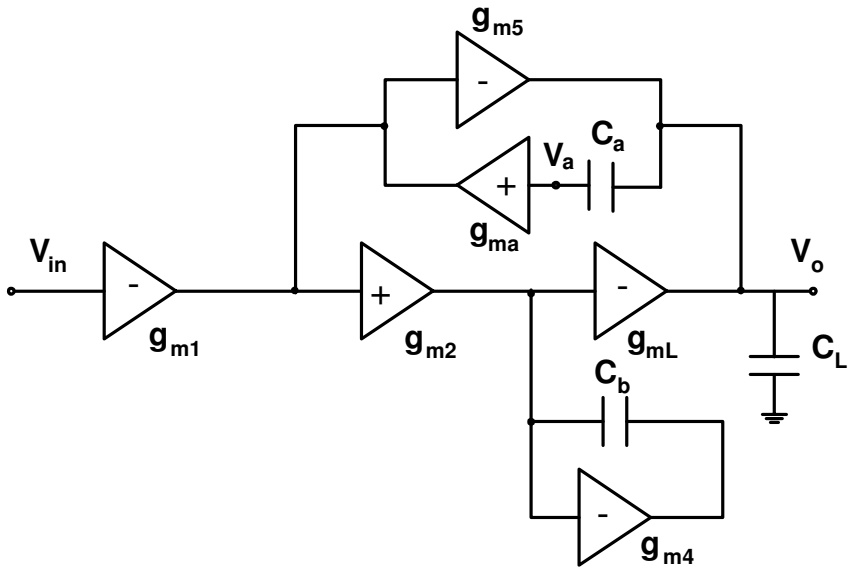


Fig. 2.9. Three stage DLPC amplifier

The pole-zero diagram for the DLPC amplifier is similar to that of the AFFC amplifier. This amplifier has a higher bandwidth because of the reduced loading at the output due to the removal of the second Miller capacitor for compensation. Hence this path is a high speed path. The stability conditions are derived using butterworth approximation of the transfer function in unity gain feedback configuration [11] which result in

$$C_a = C_b = \sqrt{2\left(\frac{g_{m1}g_{m4}}{g_{m2}g_{mL} + g_{m4}g_{m5}}\right)C_{p1}C_L} \tag{2.23}$$

$$g_{ma} = 4g_{m1} \tag{2.24}$$

Table 2.2. summarizes the various existing compensation schemes for large capacitive loads. The table includes the expressions for dc gain, GBW and the conditions for stability for the different compensation schemes. The expressions for different topologies involve same variables for easier comparison. This helps in assessing the different techniques in terms of their performance and ease of implementation.

Table 2.2. Summary of compensation techniques for large capacitive loads

Topology	DC Gain	Stability Conditions	GBW
NMC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$	$g_{mL} >> g_{m1}, g_{m2}$ $C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $C_{m2} = 2\left(\frac{g_{m2}}{g_{mL}}\right)C_L$	$\frac{1}{4}\left(\frac{g_{mL}}{C_L}\right)$
DFCFC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$	$g_{mf2} = g_{mL}$ $g_{m4} = \beta\left(\frac{C_{p2}}{C_L}\right)g_{mL}$ $C_{m1} = \frac{4}{\beta}\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $C_{m1} >> C_{m2} > C_{p2}$ $\beta = 1 + \sqrt{1 + 2\left(\frac{C_L}{C_{p2}}\right)\frac{g_{m2}}{g_{mL}}}$	$\frac{\beta}{4}\left(\frac{g_{mL}}{C_L}\right)$
PFC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$	$g_{mf} = g_{mL}$ $\beta = \frac{7}{2}\sqrt{\left(\frac{C_L}{C_{m2}+C_{p2}}\right)\frac{g_{m2}}{g_{mL}}}$	$\frac{\beta}{4}\left(\frac{g_{mL}}{C_L}\right)$
AFFC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$	$g_{mf} > g_{m2}$ $g_{ma} = 4g_{m1}$ $C_a = C_m = \frac{4}{N}\left(\frac{g_{m1}}{g_{mL}}\right)C_L$ $N = \sqrt{8\left(\frac{C_L}{C_{p1}}\right)\left[\frac{g_{m1}\left(g_{mf}-g_{m2}\right)}{g_{mL}^2}\right]}$	$\frac{g_{m1}}{C_a}$
DLPC	$\frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$	$C_a = C_b = \sqrt{2\left(\frac{g_{m1}g_{m4}}{g_{m2}g_{mL}+g_{m4}g_{m5}}\right)C_{p1}C_L}$ $g_{ma} = 4g_{m1}$	$\frac{g_{m1}}{C_a}$

CHAPTER III

MULTISTAGE AMPLIFIERS WITH A SINGLE COMPENSATION CAPACITOR

3.1. Introduction

From the existing topologies it is clear that almost all three-stage amplifiers that have been reported for large capacitive loads invariably have two capacitors. The main problem of an uncompensated three-stage amplifier with a large capacitive load lies in the fact that the load being large, the pole at the output is very close to the dominant pole (pole at the output of the first stage) as shown in Fig. 3.1.

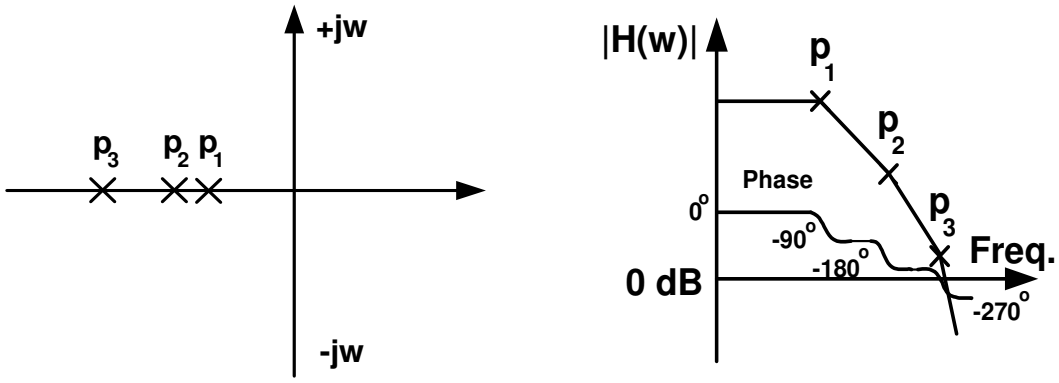


Fig. 3.1. Pole-zero diagram of an uncompensated three stage amplifier.

In order to push all the non dominant poles beyond the GBW of the amplifier, it is very essential to do away with the output pole. Pole splitting and pole-zero cancellation seem to be the two obvious ways of doing it. But, it is known that imperfect

pole-zero cancellation at low frequencies deteriorates the settling time of the amplifier because of the creation of a pole-zero doublet [15]. Another major drawback of this technique is that the system becomes very sensitive to load – a slight change in load leads to pole-zero doublets at lower frequencies – hence instability. This leaves us with only one alternative i.e. pole splitting (splitting the output pole and the dominant pole using a Miller capacitor). This technique has been used in the proposed topologies and their performance has been verified.

3.2. Single Miller Capacitor (SMC) Compensation Technique

3.2.1. Structure

The proposed structure, which is shown in Fig. 3.2, is introduced and analyzed in this section. A larger bandwidth compared to the NMC can be obtained by using only one capacitor for compensation instead of two. The structure has three gain stages with only one compensation capacitor. It has an additional transconductance stage, g_{mf} from the output of the first stage to the final output, forming a push-pull stage at the output that helps in improving the transient response of the amplifier [6]. A single Miller compensation capacitor (C_m) is used to split the first pole (pole at the output of the first stage) and the third pole (pole at the output of third stage). After compensation, the position of the second non-dominant pole is dictated by the gain of the second stage, which decides the stability of the amplifier. In fact, as will be shown later, a judicious distribution of the total gain among the three stages can stabilize the amplifier with the use of a single compensation capacitor.

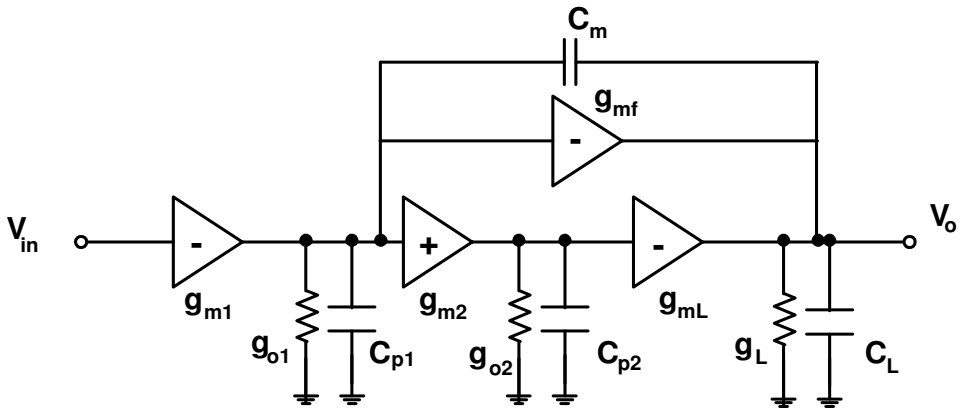


Fig. 3.2. Structure of single Miller capacitor amplifier (SMC)

3.2.2. Small Signal Analysis

The small signal model is shown in Fig. 3.3. Using the small signal model with the following assumptions: 1) the gains of all the stages are much greater than 1; 2) the parasitic capacitances C_{p1} and C_{p2} are much smaller than the Miller capacitor C_m and loading capacitor C_L; 3) the transconductance of the feedforward stage, g_{mf}, is equal to that of the third gain stage, g_{mL}, the transfer function is given by (3.1)

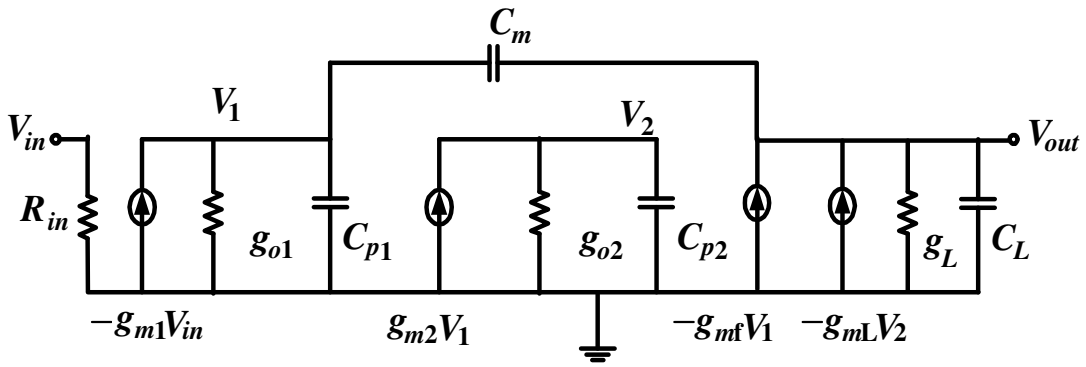


Fig. 3.3. Equivalent small-signal circuit of single Miller capacitor amplifier (SMC)

$$A_{v(SMC)}(s) = \frac{A_{dc}\left(1 + s\frac{C_{p2}g_{mf} - C_m g_{o2}}{g_{m2}g_{mL}} - s^2\frac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{3.1}$$

$$A_{v(SMC)}(s) \approx \frac{\left(1 + s\frac{C_{p2}g_{mf} - C_m g_{o2}}{g_{m2}g_{mL}} - s^2\frac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{s\frac{C_m}{g_{m1}}\left(1 + s\frac{C_L}{G_{meff}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{3.2}$$

where $A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$ is the dc gain of the amplifier, $p_{3-dB} = \frac{g_{o1}g_{o2}g_L}{g_{m2}g_{mL}C_m}$ is the dominant pole of the amplifier and $G_{meff} = \frac{g_{m2}g_{mL}}{g_{o2}} = A_{v2}g_{mL}$, A_{v2} being the gain of the second stage. Hence the gain-bandwidth product is given by $GBW = A_{dc} \cdot p_{3-dB} = \frac{g_{m1}}{C_m}$.

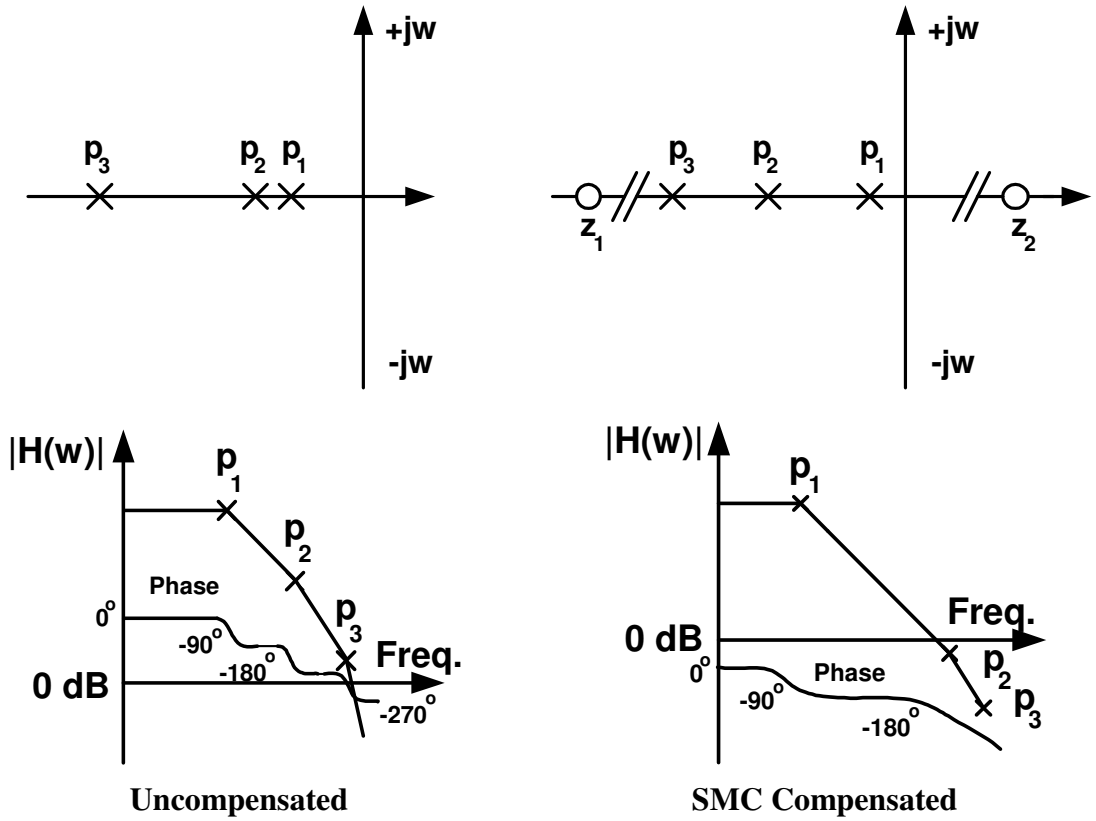
From the transfer function, the amplifier has two non-dominant poles and two zeros. The position of the non-dominant poles depends on the parasitic capacitance of the second stage, C_{p2} that could be very small if the last stage transistor is not huge.

3.2.3. Stability Analysis, Gain-Bandwidth Product, Phase Margin and Dimension Conditions

Assuming that the zeros of the amplifier are located at higher frequencies and hence can be neglected, the non-dominant poles of the amplifier are calculated as follows.

As seen from the transfer function, the non-dominant poles are located on the left-hand plane. The complex poles is avoided and hence frequency peaking

if $\left(\frac{g_{o2}}{C_{p2}}\right)^2 >> 4\frac{g_{m2}g_{mL}}{C_{p2}C_L}$, which is the case for large loads, resulting in a condition $A_{v2} < \frac{1}{2}\sqrt{\frac{g_{m2}C_L}{g_{mL}C_{p2}}}$, where $A_{v2}=\frac{g_{m2}}{g_{o2}}$, is the gain of second stage. The non-dominant poles are hence given by $p_2 = \frac{G_{meff}}{C_L}$ and $p_3 = \frac{g_{o2}}{C_{p2}} - \frac{G_{meff}}{C_L}$ where $G_{meff} = \frac{g_{m2}g_{mL}}{g_{o2}}$. The approximate locations of the zeroes are given by $z_2 = \frac{G_{meff}}{C_m}$(RHP Zero) and $z_1 = \frac{g_{o2}}{C_{p2}} + \frac{G_{meff}}{C_m}$ (LHP Zero).



Uncompensated **SMC Compensated**

Fig. 3.4. Pole-zero diagram of the uncompensated and SMC compensated amplifier

The pole-zero diagrams for the uncompensated and the SMC compensated amplifier is shown in Fig. 3.4. In the figure p_1 denotes p_{3-dB} of the amplifier. For stability of the circuit, the second and third pole should satisfy the condition, $GBW \le \frac{1}{2} p_2 \le \frac{1}{4} p_3$. This implies $\frac{g_{m1}}{C_m} \le \frac{1}{2}\frac{G_{meff}}{C_L} \le \frac{1}{4}\left(\frac{g_{o2}}{C_{p2}} - \frac{G_{meff}}{C_L}\right)$. Hence, $C_m = \frac{2g_{m1}C_L}{G_{meff}}$ or $C_m = \frac{2g_{m1}g_{o2}C_L}{g_{m2}g_{mL}}$.

The value of the compensation capacitor is given by (3.3)

$$C_m = \frac{1}{2A_{v2}}\left(4\frac{g_{m1}}{g_{mL}}C_L\right) \tag{3.3}$$

resulting in a very small compensation capacitor C_m. Thus, it can be seen that by suitable choice of the second stage gain the value of the compensation capacitor can be reduced. Hence the requirement of $g_{mL} >> g_{m1}$ no longer needs to be satisfied which helps reducing the power consumption of the amplifier. The zeroes of the amplifier depend on the second order equation in the numerator which depends on C_m. Since the value of C_m is very small, all the zeroes are located at high frequencies, and hence can be ignored in the stability analysis.

A more rigorous stability analysis can be done using Routh-Hurwitz stability criterion. Neglecting the zeroes, the closed loop transfer function of the SMC amplifier is given by

$$A_{v(SMC)closedloop}(s) \approx \frac{1}{1 + s\frac{C_m}{g_{m1}}\left(1 + s\frac{C_L}{G_{meff}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{3.4}$$

Since the order of the numerator is less than that of the denominator, the stability is

determined by the denominator. The characteristic equation is formed by equating the denominator to zero. Comparing the characteristic equation to that of a general characteristic equation of the form $a_o s^3 + a_1 s^2 + a_2 s + a_3 = 0$, we have

$$a_o = \frac{C_{p2} C_L C_m}{g_{m1} g_{m2} g_{mL}} \tag{3.5}$$

$$a_1 = \frac{g_{o2} C_L C_m}{g_{m1} g_{m2} g_{mL}} \tag{3.6}$$

$$a_2 = \frac{C_m}{g_{m1}} \tag{3.7}$$

$$a_3 = 1 \tag{3.8}$$

Applying the Routh-Hurwitz stability criterion on the characteristic equation we have,

$$a_1 a_2 - a_0 a_3 > 0 \tag{3.9}$$

$$\Rightarrow \frac{g_{o2}}{C_{p2}} > \frac{g_{m1}}{C_m} = GBW \tag{3.10}$$

While Routh-Hurwitz stability criterion gives the general condition, separate pole approach is more suitable for large capacitive loads. The phase margin (PM) is calculated according to equation (3.11) as

$$PM = 180^o - \tan^{-1}(\frac{GBW}{p_1}) - \tan^{-1}(\frac{GBW}{p_2}) - \tan^{-1}(\frac{GBW}{p_3}) \tag{3.11}$$

$$\Rightarrow PM = 180^0 - 90^0 - \tan^{-1}(\frac{1}{2}) - \tan^{-1}(\frac{1}{4}) \approx 50^0$$

3.2.4. Slew Rate and Settling Time

The transient response of the amplifier comprises of the slewing and settling

behavior of the amplifier in closed loop condition [15]. The slew rate of the amplifier depends on the amount of the charging current and the size of the capacitors to be charged. With a push-pull output stage in the SMC amplifier, the slew rate is not limited by the output stage instead it depends on the size of the compensation capacitor if the available charging current is fixed by the low power constraint. The slew rate is given by

$$SR = \frac{I_{charge}}{C_m} \tag{3.12}$$

The significant increase in the slew rate of SMC as compared to that of NMC under same power constraint is due to the reduction in the size of the compensation capacitor by a factor of $2A_{v2}$. An improved settling response is obtained by maximizing the phase margin and avoiding pole-zero doublets in the pass-band of the amplifier [15]. In the proposed amplifier there is no presence of pole-zero doublets in the pass-band and the calculated phase margin is close to 50^{o}. For an amplifier with an almost single pole response i.e. no pole-zero doublet in the pass-band, the settling time is dictated by its GBW. Every additional pole close to the pass-band slows the settling response. In order to increase the phase margin considerably a LHP zero is introduced with the help of a feedforward stage as shown in the following proposed amplifier structure.

3.3. Single Miller Capacitor Feedforward Compensation (SMFFC) Technique

3.3.1. Structure

The proposed single Miller capacitor feedforward frequency compensation approach (SMFFC) (shown in Fig. 3.5) uses a feedforward path to provide a LHP zero to

compensate the second pole (first non-dominant pole). The feedforward path adds current at the second stage output pushing the second non-dominant pole to higher frequencies. The LHP zero is placed near the second pole which provides a positive phase shift and compensates for the negative phase shift due to the non-dominant poles.

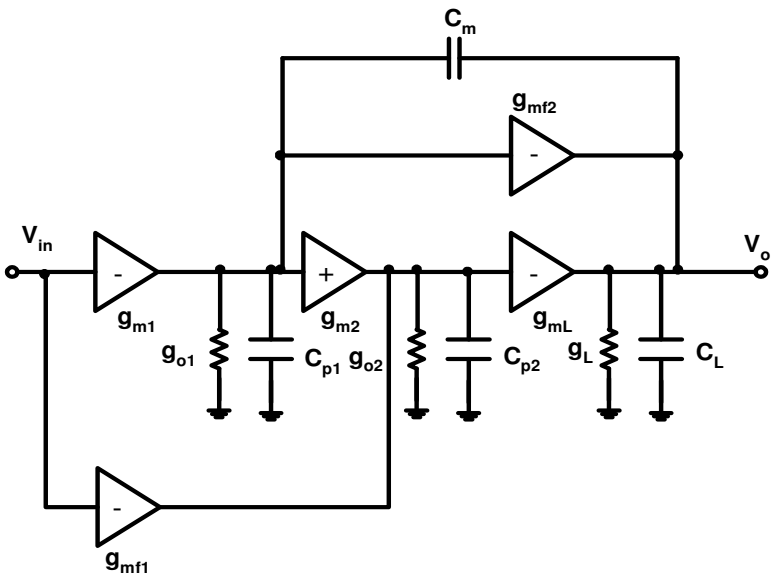


Fig. 3.5. Structure of single Miller capacitor feedforward frequency compensation amplifier (SMFFC)

3.3.2. Small Signal Analysis

The small signal model is shown in Fig. 3.6. On solving the small signal circuit model with the same assumptions as that of SMC, the transfer function is given by (3.13)

$$A_{v(SMFFC)}(s) = \frac{A_{dc}\left(1 + s\frac{C_m g_{mf1}}{g_{m1}g_{m2}} - s^2\frac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{3.13}$$

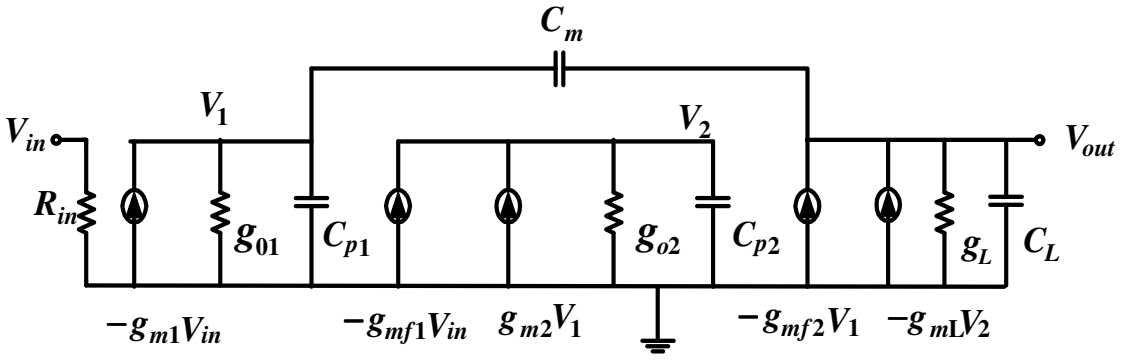


Fig. 3.6. Equivalent small-signal circuit of SMFFC amplifier

$$A_{v(SMFFC)}(s) \approx \frac{\left(1 + s\frac{C_m g_{mf1}}{g_{m1}g_{m2}} - s^2\frac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{s\frac{C_m}{g_{m1}}\left(1 + s\frac{C_L}{G_{meff}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{3.14}$$

where $A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$, is the dc gain of the amplifier and $p_{3-dB} = \frac{g_{o1}g_{o2}g_L}{g_{m2}g_{mL}C_m}$, is the dominant pole of the amplifier. Hence the gain-bandwidth product is given by $GBW = A_{dc} \cdot p_{3-dB} = \frac{g_{m1}}{C_m}$. From the transfer function shown in (3.14), the amplifier has two non-dominant poles and two zeros. The locations of the non-dominant poles are the same as those of the SMC amplifier.

3.3.3. Stability Analysis, Gain-Bandwidth Product, Phase Margin and Dimension Conditions

The stability analysis of the amplifier is done using the separate pole approach. Since the s^2 term is negative and the s term is positive, this implies that there is a LHP zero and a

RHP zero and the LHP zero occurs at a lower frequency than the RHP zero, which does not pose any threat to the stability of the amplifier, instead it helps improving the frequency response. From the transfer function the zeroes of the amplifier are obtained as $z_1 = \frac{g_{m1}g_{m2}}{g_{mf1}C_m}$ (LHP Zero) and $z_2 = \left(\frac{g_{mf1}g_{mL}}{g_{m1}C_{p2}} + \frac{g_{m1}g_{m2}}{g_{mf1}C_m}\right) \approx \frac{g_{mf1}g_{mL}}{g_{m1}C_{p2}}$ ($C_m >> C_{p2}$) (RHP zero). The pole-zero diagrams for the uncompensated and the SMFFC compensated amplifier is shown in Fig. 3.7.

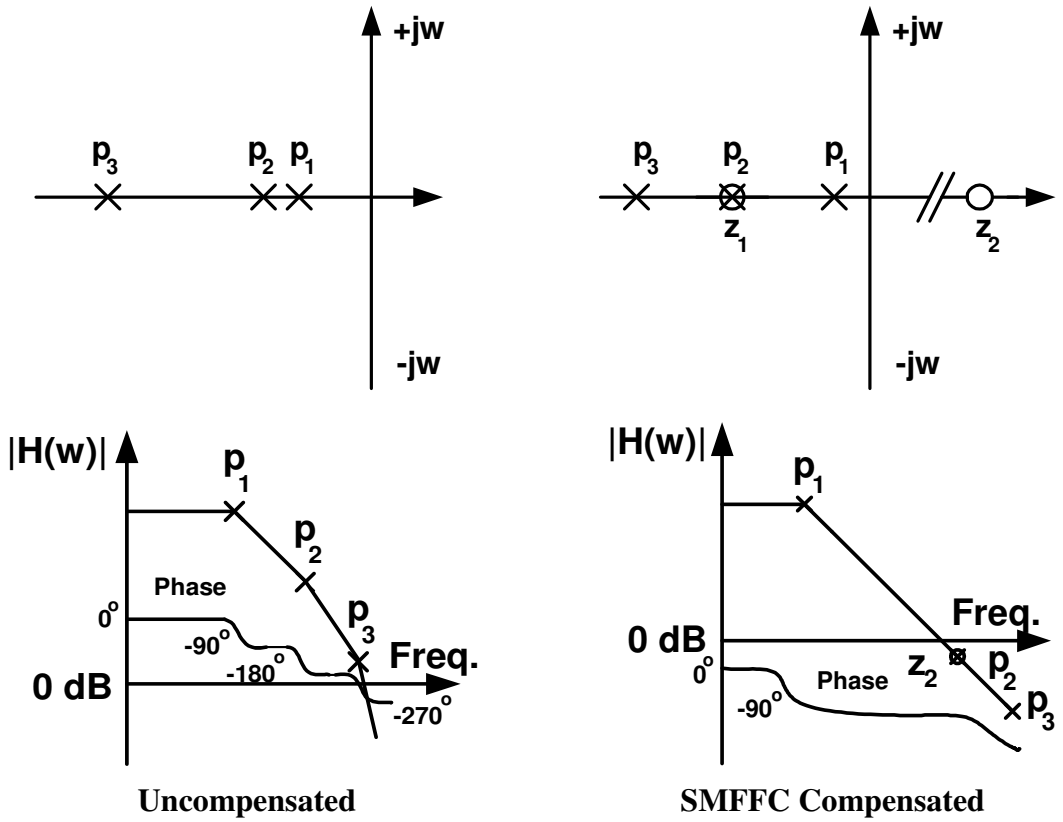


Fig. 3.7. Pole-zero diagram of the uncompensated and SMFFC compensated amplifier

In the figure p_1 denotes p_{3-dB} of the amplifier. The RHP zero is at very high

frequency and hence does not cause stability problems. The non-dominant poles and stability conditions are exactly the same as that of SMC. GBW and dimension conditions remain exactly the same. Neglecting the RHP zero, the closed loop transfer function of the SMFFC amplifier is given by

$$A_{v(SMFFC)closedloop}(s) \approx \frac{1+s\frac{g_{mf1}C_m}{g_{m1}g_{m2}}}{1+s\frac{g_{mf1}C_m}{g_{m1}g_{m2}}+s\frac{C_m}{g_{m1}}\left(1+s\frac{C_L}{G_{meff}}+s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{3.15}$$

Since the order of the numerator is less than that of the denominator the stability is determined by the denominator. The characteristic equation is formed by equating the denominator to zero. Comparing the characteristic equation to that of a general characteristic equation of the form $a_o s^3 + a_1 s^2 + a_2 s + a_3 = 0$, we have

$$a_o = \frac{C_{p2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \tag{3.16}$$

$$a_1 = \frac{g_{o2}C_L C_m}{g_{m1}g_{m2}g_{mL}} \tag{3.17}$$

$$a_2 = \frac{g_{mf1}C_m}{g_{m1}g_{m2}} + \frac{C_m}{g_{m1}} \tag{3.18}$$

$$a_3 = 1 \tag{3.19}$$

Applying the Routh-Hurwitz stability criterion on the characteristic equation we have,

$$a_1 a_2 - a_0 a_3 > 0 \tag{3.20}$$

$$\Rightarrow \frac{g_{o2}}{C_{p2}} > \frac{g_{m1}}{C_m}\frac{1}{\left(1+g_{mf1}/g_{m2}\right)} \tag{3.21}$$

The phase margin (PM) is calculated as per equation (3.22)

$$PM = 180^{o} - \tan^{-1}(\frac{GBW}{p_1}) - \tan^{-1}(\frac{GBW}{p_2}) - \tan^{-1}(\frac{GBW}{p_3}) + \tan^{-1}(\frac{GBW}{z_1}) \quad (3.22)$$

$$PM = 180^{0} - 90^{0} - \tan^{-1}(\frac{1}{2}) - \tan^{-1}(\frac{1}{4}) + \tan^{-1}(\frac{1}{2}) \approx 76^{0}$$

The above calculation of phase margin assumes exact pole-zero cancellation, which implies

$$p_2 = z_1 \Rightarrow g_{mf1} = \frac{1}{A_{V2}} \frac{g_{m1} g_{m2} C_L}{g_{mL} C_m} \quad (3.23)$$

where $p_2 = \frac{g_{m2} g_{mL}}{g_{o2} C_L}$ and $z_1 = \frac{g_{m1} g_{m2}}{g_{mf1} C_m}$.

3.3.4. Slew Rate and Settling Time

In the case of SMFFC the theoretical phase margin obtainable is close to 76^0. Hence the compensation capacitor C_m can be further reduced to achieve a still higher bandwidth without sacrificing the stability of the amplifier. This helps in improving the slew rate of the amplifier because with a push-pull output stage, the slew rate is not limited by the output stage instead it depends on the size of the compensation capacitor if the available charging current is fixed by the low power constraint. In the proposed topology there is no presence of pole-zero doublets in the pass-band, because the pole and the zero both are at higher frequencies and could be placed outside the pass-band of the amplifier although close to the unity gain bandwidth. It is well known that high frequency pole-zero doublet does not degrade the settling time [15] as much as low

frequency doublets and hence the settling time is not affected much by the introduction of the LHP zero.

3.4. Design Considerations and Circuit Implementations

A judicious distribution of gain among the three stages is the most important consideration in the design of these amplifiers. For high gain amplifiers (>100 dB) the gain is distributed such that $A_{v1} >> A_{v2} > A_{v3}$. The gain of the first stage is maximized, with the second stage having moderate gain and the final stage having a very small gain. This results in the second and third pole of the amplifier to be located at higher frequencies due to the high output conductance of the second and third stages and thereby resulting in a single pole system. In order to achieve this, the first stage uses a folded cascode topology to enhance the output impedance. A moderate gain at the second stage helps in reducing the required compensation capacitor to a great extent. For example a 100dB gain from three stages can be distributed as 60dB, 30 dB and 10 dB for first, second and third stage respectively. Thus, A_{v2} = 30dB ≈ 30V/V resulting in the reduction of the required C_m by a factor of 30 as compared to that of NMC while ensuring stability.

The circuit implementations of the SMC and SMFFC amplifiers are shown in Fig. 3.8 and Fig. 3.9 respectively. Transistors M_1-M_8 form the first gain stage. Transistors M_{f1} and M_{f2} form the feedforward transconductance stage, g_{mf1} in the SMFFC amplifier. The second gain stage of the amplifiers comprises of transistors M_9–

M_{12}. The output stage comprises of a feedforward stage (g_{mf} in SMC and g_{mf2} in SMFFC) and the third gain stage g_{mL} forming a push-pull stage.

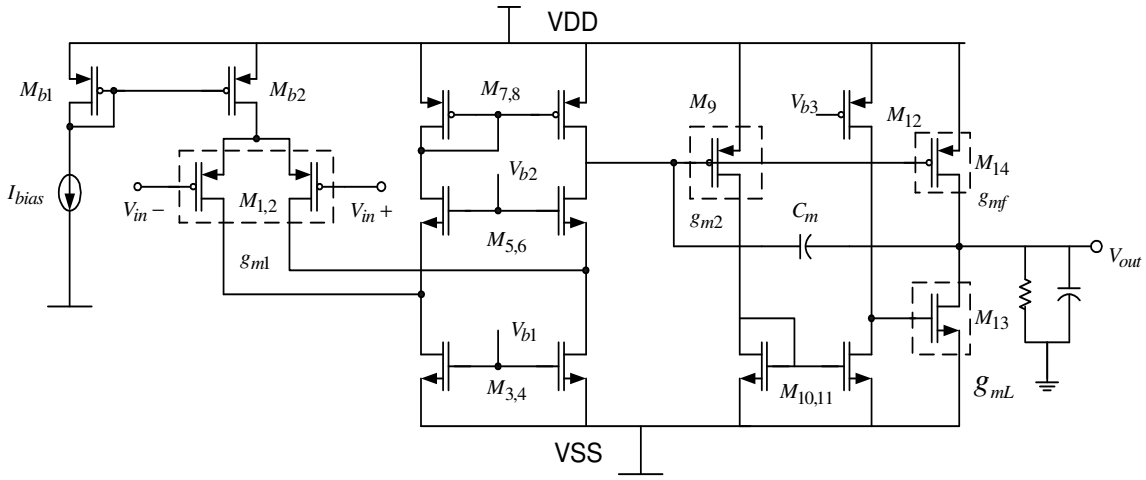


Fig. 3.8. Circuit schematic of SMC

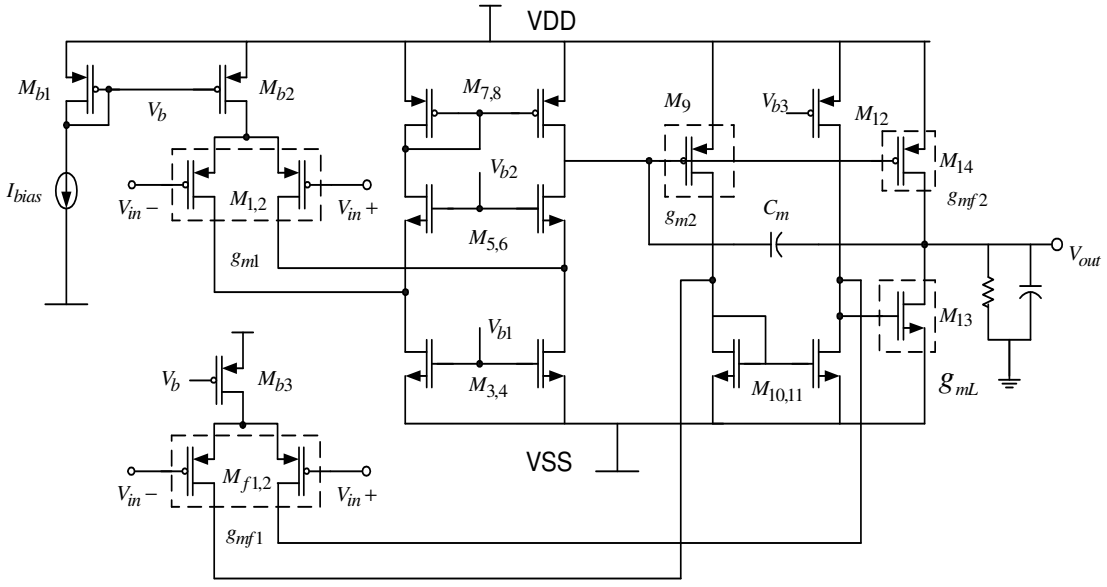


Fig. 3.9. Circuit schematic of SMFFC

The third gain stage is realized by transistor M_{13} whereas the feedforward stage is realized by transistor M_{14}. Transistors $M_{b1} - M_{b3}$ are used for biasing. The bias voltages Vb1 and Vb2 were realized using a cascode current mirror using a single current source. Each of the other bias voltage sources was realized using a simple current mirror (i.e. a current source with a diode-connected transistor).

The design procedure for the SMC and SMFFC amplifiers is almost the same except that the SMC amplifier does not have the additional feedforward stage. The general design procedure is shown in Fig. 3.10. The design procedure starts with the distribution of gain among the three stages. It is very important to have a very high gain in the first stage as compared to the other stages in order to have a dominant pole and this results in a slower first stage and faster second and third stages. This is very common in every multistage amplifier. Next, with an assumption of the value of the Miller compensation capacitor the transconductance of the first stage can be determined followed by the transconductance of the other stages with the knowledge of the desired GBW and the load capacitor. An estimation of the parasitic capacitance at the output of the second stage is required for determining g_{m2} . The transconductance of the feedforward stages can then be easily determined. The sizes of the transistors are determined using the equations (one equation all region model) shown in the design procedure. The inversion level i_f is typically large (typical values could be 48 or 80) for current mirrors to ensure strong inversion. The power consumption increases with i_f and it increases rapidly for large i_f , whereas the silicon area decreases with i_f and hence

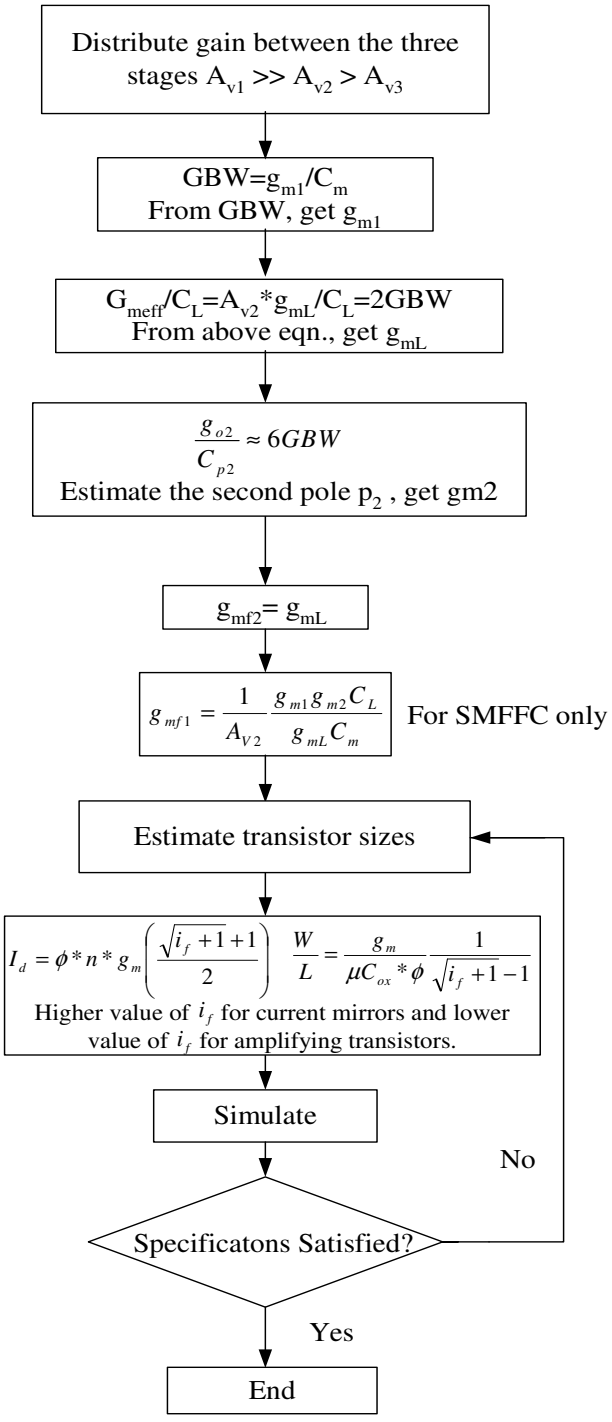


Fig. 3.10. Design procedure for the SMC and SMFFC amplifiers

under low power constraint a value of i_f close to 10 is used which is comparatively lower. Power consumption of the amplifiers can be given by

$$P = (V_{DD} - V_{SS})(I_1 + I_2 + I_3) \tag{3.24}$$

where I_1, I_2 and I_3 are the dc currents of the first second and third stages respectively. For the SMFFC amplifier an additional stage (feedforward stage, g_{mf1}) needs to be considered.

Table 3.1. Component sizes

Transistor	SMC	SMFFC
Mb1	2*(5.55/1.05)	2*(5.55/1.05)
Mb2	8*(5.55/1.05)	8*(5.55/1.05)
M1,2	8*(6.15/0.6)	8*(6.15/0.6)
M3,4	6*(10.05/1.05)	6*(10.05/1.05)
M5,6	2*(10.05/1.05)	2*(10.05/1.05)
M7,8	6*(6.15/1.95)	6*(6.15/1.95)
M9	6*(6.3/0.6)	6*(6.3/0.6)
M10,11	2*(9/0.75)	2*(9/0.75)
M12	6*(5.55/0.6)	6*(5.55/0.6)
M13	2*(9.3/0.6)	2*(9.3/0.6)
M14	10*(10.05/0.6)	10*(10.05/0.6)
Mf1,2	-	6*(5.55/0.75)
Mb3	-	6*(5.55/1.05)
Cm	15*(0.46pF)	10*(0.4pF)

Since the transconductance of a transistor is proportional to its dc current, the total dc current in a stage is proportional to the product of the number of branches and the

transconductance of each branch approximately. This provides an additional degree of freedom in the design especially for low power. Since the estimation of the parasitics and the pole locations is generally not accurate, the designer after simulating the calculated values needs to perform several iterations to obtain the final transistor sizes. Table 3.1 gives the sizes of the transistors (along with multiplicity) and compensation capacitors for both the amplifiers as obtained after tuning. It can be seen that the compensation capacitor value for SMFFC is less as compared to that of SMC as explained previously.

3.5. Experimental Results

The proposed SMC and SMFFC amplifiers were implemented with AMI 0.5µm CMOS technology through MOSIS. Fig. 3.11a and Fig. 3.11b show the chip micrograph of the SMC and SMFFC amplifiers respectively.

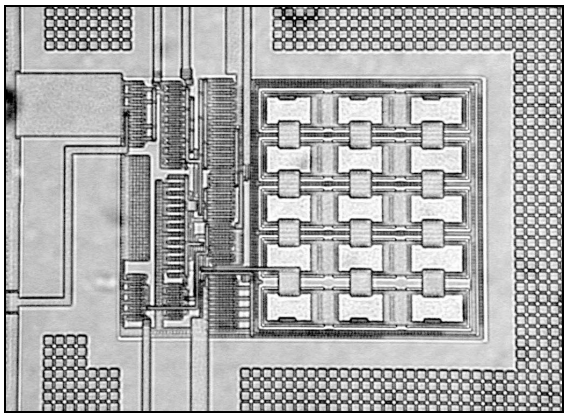


Fig. 3.11a. Chip micrograph of the SMC amplifier ($0.02mm^2$)

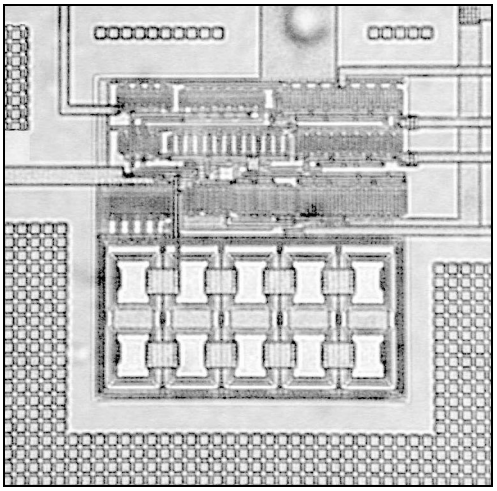


Fig. 3.11b. Chip micrograph of the SMFFC amplifier (0.015mm^2)

The area of the SMC amplifier is 0.02mm^2 whereas that of SMFFC amplifier is 0.015mm^2. This reduction is area for the SMFFC amplifier is primarily due to the reduction in the size of the compensation capacitor.

Fig. 3.12 shows the experimental setup for the testing of the amplifiers. For the frequency response characterization a large value for both R and C are used. At low frequency the capacitor behaves as open and the dc operating conditions are established. For high frequency, the capacitor behaves as a short to ground and the amplifier's frequency response is captured. The value of the resistor is 1MΩ and the value of the capacitor is 10μF. Since this connection is a high pass network the pole due to the RC product should be at very low frequencies (lower than the open-loop dominant pole of the amplifier) in order to obtain the accurate frequency response of the amplifier. Using a potentiometer instead of a fixed resistance is a better idea. This helps in controlling the feedback resistance value so as to be able to control the pole position. For the transient

response the amplifiers are connected in closed-loop unity gain configuration and an input step of 0.5Vpp with a time-period of 20µsec was applied.

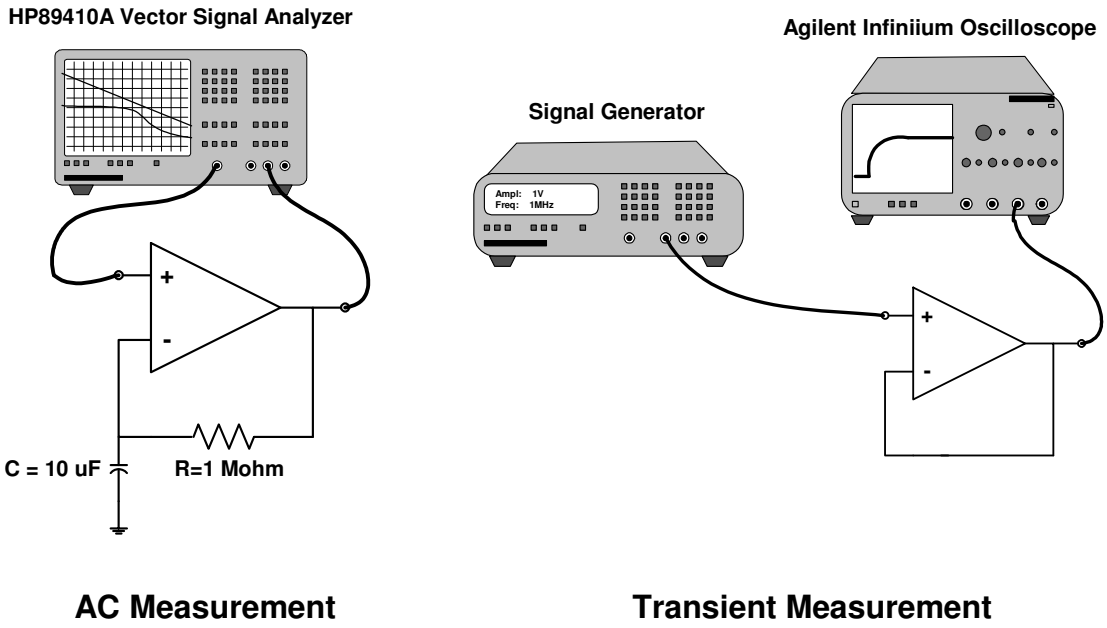


Fig. 3.12. Experimental setup.

The AC responses of the SMC and SMFFC amplifiers are shown in Fig. 3.13a and Fig. 3.13b respectively. Fig. 3.14 shows the transient response for both amplifiers. A comparison table (Table 3.2) is provided to show the advantage and drawback of the proposed and previous topologies. Four figures of merit FOM_S, FOM_L [5], [6], FOM_S^* and FOM_L^* are used to evaluate the small signal (GBW) and large signal (Slew rate) performances of the proposed amplifiers. Chip area (which is mainly dominated by capacitor size) is taken into consideration in FOM_S^* and FOM_L^*.

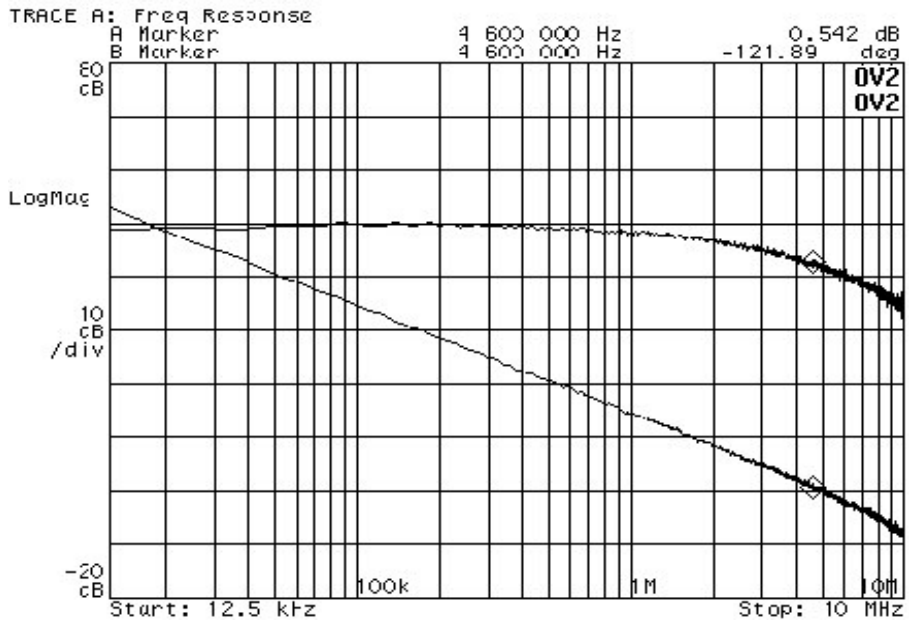


Fig. 3.13a. Frequency response of the SMC amplifier, GBW=4.6MHz and PM=57^{o}

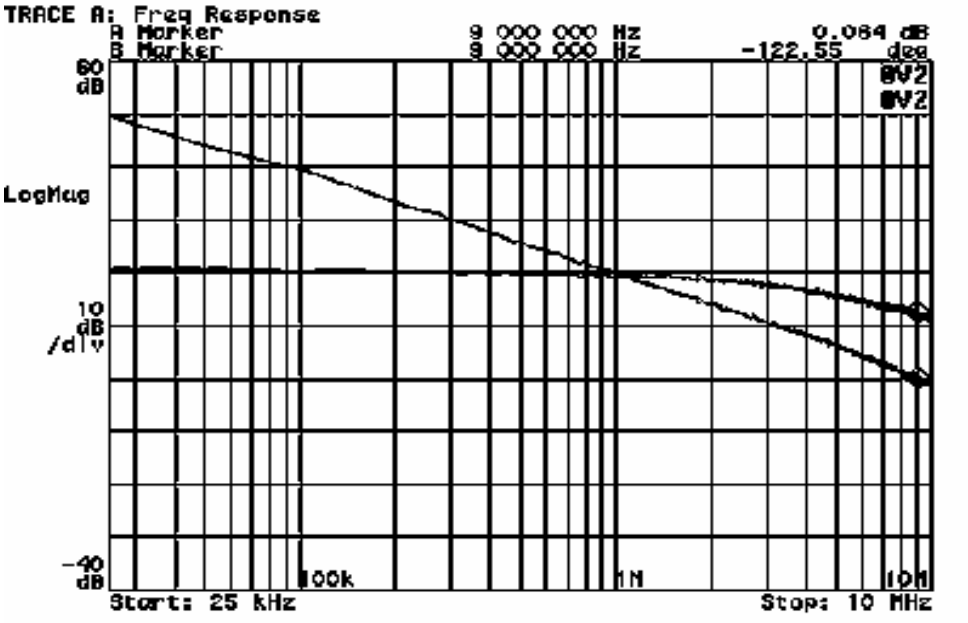


Fig. 3.13b. Frequency response of the SMFFC amplifier, GBW=9MHz and PM=57^{o}

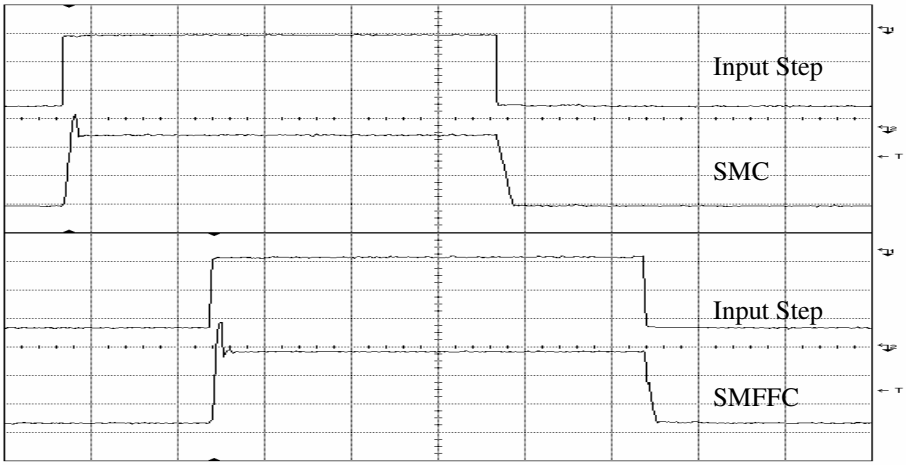


Fig. 3.14. Transient response of the amplifiers

(The horizontal and vertical scales are 2μS/div and 0.2V/div respectively)

Table 3.2. Comparison of different multistage amplifiers with large capacitive loads

Parameter	NMC [10]	DFCFC [6],[7]	PFC [9]	AFFC [10]	DLPC [11]	SMC [12]	SMFFC [12]
Load pF/KΩ	120/25	100/25	130/24	120/25	120/25	120/25	120/25
DC gain(dB)	>100	>100	>100	>100	>100	>100	>100
GBW(MHz)	0.4	2.6	2.7	4.5	7	4.6	9
Phase margin	61°	43°	52°	65°	46°	57°	57°
Power(mW@Vdd)	0.38 @2	0.42 @2	0.275 @1.5	0.4 @2	0.33@1.5	0.38@2	0.41@2
Capacitor Value (pF)	C_{m1}=88 C_{m2}=11	C_{m1}=18 C_{m2}=3	-	C_m=3 C_a=7	C_a=4.8 C_b=2.5	C_m=7 (one)	C_m=4 (one)
SR+(V/μS)	0.15	1.32	1	0.78	2.2	3.28	4.8
SR-(V/μS)	0.13	1.27	1	2.20	4.4	1.31	2
+1% TS (μs)	4.9	0.96	-	0.42	0.315	0.53	0.58
-1% TS (μs)	4.7	1.37	-	0.85	0.68	0.4	0.43
FOM_S(MHz.pF/mW)	127	619	1276	1350	2545	1453	2634
FOM_L(V/μs.pF/mW)	45	308.3	473	447	1200	726	996
FOM_S^*(MHz.pF/mW.pF)	1.28	29.5	-	135	348.6	207.6	658
FOM_L^*(V/μs.pF/mW.pF)	0.45	14.7	-	44.7	164.4	103.7	249
Area(mm^2)	0.14	0.11	0.03	0.06	0.05	0.02	0.015
Technology	0.8μm CMOS	0.8μm CMOS	0.35μm CMOS	0.8μm CMOS	0.6μm CMOS	0.5μm CMOS	0.5μm CMOS

$$FOM_S = \frac{GBW * C_L}{Power} \tag{3.25}$$

$$FOM_L = \frac{SR * C_L}{Power} \tag{3.26}$$

$$FOM_S^* = \frac{GBW * C_L}{Power * C_{Total}} \tag{3.27}$$

$$FOM_L^* = \frac{SR * C_L}{Power * C_{Total}} \tag{3.28}$$

where C_{Total} is the total value of compensation capacitor used and SR is the average slew rate. Fig. 3.15 shows a graphical comparison of the various multistage amplifiers.

The GBW of the SMC and SMFFC amplifiers is 22.5 and 11.5 times that of the NMC [10] (designed in 0.8µm CMOS) respectively. The average slew rates are 24 and 16.4 times that of the NMC amplifier respectively. As compared to NMC the SMC and SMFFC amplifiers occupy almost 7 and 9.3 times less silicon area respectively without much power consumption. NMC of [10] was chosen for fair comparison in terms of loading conditions and technology used.

3.6. Discussion

From the previous sections it is clear that for very large capacitive loads the amplifier has real poles. Now, as the load reduces the non-dominant poles form a complex pole pair. If this complex pole pair is close to the GBW of the amplifier, it influences the settling time of the overall amplifier. As far as stability is concerned, the stability of an amplifier can be verified from the Nyquist plot of the open-loop transfer

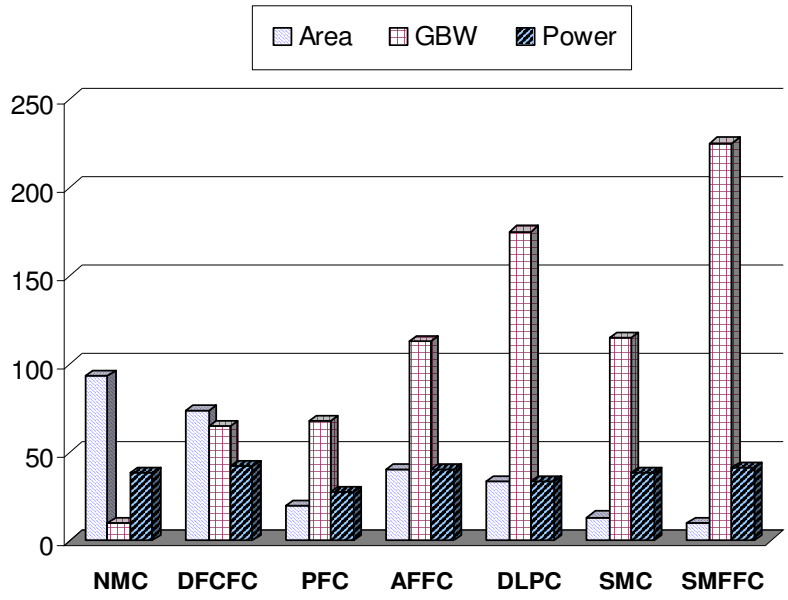


Fig. 3.15. Comparison of various multistage amplifiers

function. If the Nyquist plot does not encircle the point (-1+0i) in the complex plane then the closed loop system is unconditionally stable. Fig. 3.16 shows the Nyquist plot of the open-loop transfer function of the SMFFC amplifier generated using MATLAB.

After the initial slewing period, the settling time of the amplifier is determined by the GBW, in the absence of any non-dominant poles or pole-zero doublets close to the GBW. In the presence of complex poles close to the GBW the settling time is affected by the damping factor of the non-dominant complex poles. A small damping factor of the complex poles results in magnitude peaking in the frequency response and can result in oscillations or ringing in the settling response. This behavior is more prominent in a pure second order system. Besides, there is significant influence of the pole-zero doublets on the settling time. A low frequency pole-zero doublet implies less peaking

but more decay time (or higher settling time) whereas a high frequency doublet although has a faster decay time, shows more peaking in the transient response.

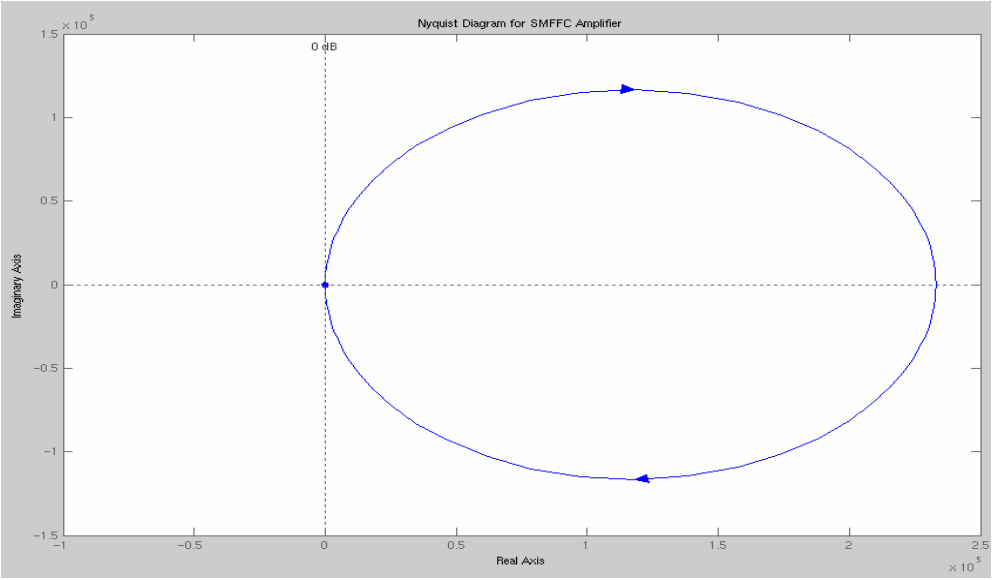


Fig. 3.16. Nyquist plot for the SMFFC amplifier.

With so many factors influencing at the same time, the prediction of the settling time of a third order system (the transfer function of the amplifiers in closed loop) becomes difficult. Having the non-dominant poles as far as possible from the GBW and performing pole-zero cancellation at high frequencies can lead to better settling time. From the transient response of the amplifiers we observe non-uniform positive and negative slew rates. One of the reasons could be the difference in the value of available charging current during the positive and negative slopes.

The trade-off with power and position of non-dominant poles is very evident as more power is required to push the non-dominant poles to high frequencies to have a

higher phase margin. Besides, a large Miller compensation capacitor is required for better pole-splitting as the load capacitor increases. This implies more circuit area.

3.7. Conclusions

Two low-power, efficient, three stage amplifier topologies for large capacitive loads were introduced. A small compensation capacitor used in the amplifiers helps in reducing the area and improving the bandwidth without sacrificing stability. Based on a comprehensive comparison of the proposed amplifiers with the previously reported structures with large capacitive loads, the proposed compensation schemes demonstrate superior performance. Fig. 3.17a and Fig. 3.17b show the performance of various multistage amplifiers for different loads. The ratio of GBW and average slew rate each with respect to power consumption is shown. The values for GBW, power and average slew rates for the various amplifier topologies are taken from Table 2.1 and Table 3.2.

These figures can serve as guidelines for the choice of a particular topology for a particular capacitive load. The choice of topology would also be dictated by the power consumption and the performance (both small and large signal).

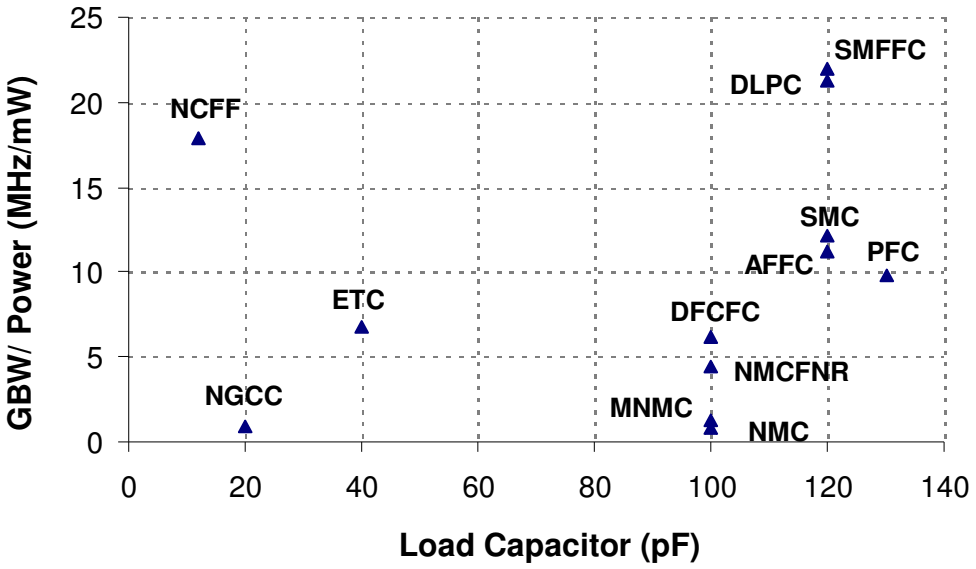


Fig. 3.17a. Small signal performance comparison of multistage amplifiers with different frequency compensation schemes

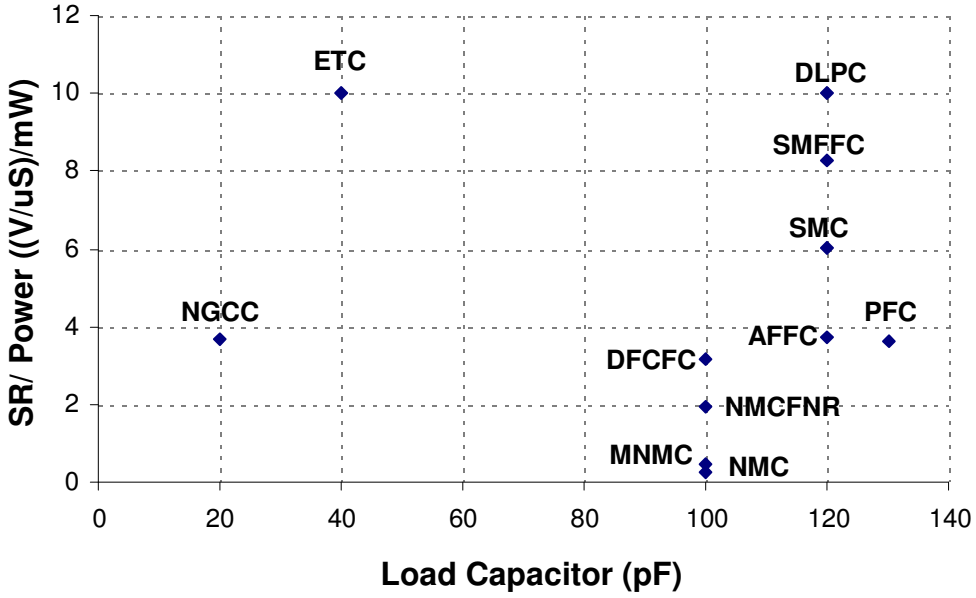


Fig. 3.17b. Large signal performance comparison of multistage amplifiers with different frequency compensation schemes

CHAPTER IV

DISTRIBUTED CIRCUITS

4.1. Background and Motivation

The insatiable thirst for sending large volume of data, to very long distances, at very high speed while providing good quality of service to a large number of users all at the same time serves as the driving force for the ever growing RF and wireless industry. The latest IEEE standards like IEEE 802.15.3a for very high data rate wireless personal area networks (WPAN) also known as Ultra Wideband (UWB) in the 3.1 to 10.6GHz range and IEEE 802.16 wireless metropolitan area network (WMAN) standard for 10 - 66 GHz range are a move towards alleviating the current bandwidth crunch. Design and integration of high-speed analog circuits for such applications need to comply with contradictory specifications such as frequency of operation, gain, dynamic range, power and cost.

Higher data rates in communication systems demands large bandwidth which in turn demands higher frequency of operation of the circuits. The unity-gain frequency f_T of a transistor is defined as the frequency at which the current gain of the transistor drops to unity. Although the f_T of the transistors are generally higher in modern IC technologies, but the circuits built using these transistors rarely operate at those frequencies. One of the reasons is that in order to have a gain greater than one, which is generally the case for better noise and power efficiency the transistor must operate at a frequency less than f_T and secondly, the parasitics associated with the circuit which are

not intrinsic to the transistor itself greatly inhibit the frequency of operation [14]. These bottlenecks in high frequency operation of conventional circuit building blocks provide the motivation to pursue alternative approaches to alleviate the bandwidth limitations. Distributed circuit design can be used to overcome the power and frequency limitations of conventional circuits.

4.2. Distributed Circuit Design

A circuit is considered lumped as long as the device dimensions are very small compared to the wavelength of the signal under concern and it can be modeled using Kirchhoff's voltage and current laws. At higher frequencies these device dimensions are comparable to the wavelengths of the signal and hence we cannot assume the circuit to be lumped. Then the circuit may be considered to be distributed. But the term distributed can be used for any system that uses multiple parallel signal paths and devices working in harmony to perform a desired task [14]. The actual physical dimensions may or may not be comparable to the signal wavelengths.

This definition of distributed circuit design is contrary to the conventional cascaded structure such a multistage amplifier. Devices used in cascade can be used to increase the gain but it is achieved at an expense of bandwidth, because the bandwidth of a multistage amplifier is less than that of a single stage amplifier. In a multistage amplifier as discussed in the previous chapters, it is the parasitic poles (RC time constants associated with each internal node) which degrade the frequency of operation of the amplifier. The gain of a system can be increased by superimposing the outputs of

the various stages in a constructive fashion while maintaining the bandwidth of a single section [13]. But this in turn will require additional components while lowering the output impedance of the amplifier. The use of a non-distributed impedance matching network mostly results in a reduction in bandwidth and a non-uniform group delay degrading high frequency performance and transient response [13]. The underlying principle of distributed circuit design is to distribute the capacitance associated with the input and the output of the device over a ladder structure (which is periodic), rather than considering it to be lumped to achieve an extension of bandwidth. This structure acts as a signal-summing element so that the above desired phenomenon can be achieved without degrading bandwidth.

4.3. Existing Distributed Circuits

Distributed circuits are very common in the microwave regime. There are circuits like distributed amplifiers, oscillators and mixers realized as MMICs (millimeter wave monolithic microwave ICs) on compound semiconductor technology such as GaAs or InP. CMOS implementation of distributed circuits has recently gained more interest due its low cost. Following are some of the existing CMOS distributed circuits.

4.3.1. Distributed Amplifiers

The concept of distributed amplification has been around for over half a century. Although the term *distributed amplifier* was coined in a paper by Ginzton *et al.* in 1948 [16] which used vacuum tubes, the underlying concept can be traced to the patent

specification entitled “Improvements in and relating to thermionic valve circuits” filed by Percival in 1935 [17]. Distributed amplifiers employ a topology in which the gain stages are connected such that their capacitances are not lumped at their respective input and output nodes, yet the output currents still combine in an additive fashion. The capacitances can be distributed either by including series inductive elements resulting in a lumped LC ladder network which emulates a transmission line, or by using transmission lines.

Table 4.1 shows a summary of the reported distributed amplifiers on silicon. [18] presents a distributed amplifier (DA) using bondwire and packaging inductance to achieve 5±1.2 dB gain from 300 kHz to 3 GHz. A fully integrated DA in a 0.6µm CMOS process using on-chip spiral inductors [19] achieves a pass-band gain of 6.5±1.2dB with a unity gain bandwidth of 5.5 GHz whereas its fully differential version [20] achieves a gain of 5.5±1.5 dB with a unity gain bandwidth of 8.5GHz. [21] demonstrates a DA in 0.5µm SOS (Silicon-on-Sapphire) NMOS process achieving 5 dB pass-band gain and 10GHz bandwidth.

A five-stage DA in a 0.18µm CMOS process using coplanar strip lines [22] achieves 5dB of low frequency gain which drops to 1dB at around 15 GHz. DAs using high impedance coplanar waveguides in a 0.18µm CMOS [23] demonstrate more than 8 dB of gain till 10GHz. [24] uses cascade gain cells with m-derived matching sections to achieve a gain of 7.3±0.8 dB with a bandwidth of 22GHz.

Table 4.1. Distributed amplifiers on silicon

Process	BW (GHz)	Gain (dB)	NF (dB)	UGF (GHz)	S11 (dB)	V_{DD} (V)	P_{DC} (mW)	Area (mm^2)	Chip Feature
0.8µm [18]	0.3 – 3	5 ± 1.2	5.1-7	4.7	< -6	3	54	0.72*0.32	Bondwire
0.6µm [19]	0.5 – 4	6.5±1.2	5.3-8	5.5	< -7	3	83.4	1.4*0.8	Spiral
0.6µm [20]	0.5 -7.5	5.5±1.5	8.7-13	8.5	< -6	3	216	1.3*2.2	Fully Diff. Spiral
0.5µm [21]	2 – 10	5 ± 1	-	-	< -5	-	-	-	CPW, SOS
0.18µm [22]	-	5	-	23	< -14	-	-	0.3*1.5	CPS
0.18µm [23]	1 – 10	8 ± 1	-	-	-	-	-	1.8*1.3	Darlington CC., CPW
0.18µm [24]	0.6 – 22	7.3±0.8	4.3-6.1	24	< -8	1.3	52	0.9*1.5	CC., Spiral

SOS: Silicon-on-Sapphire, CPS: Coplanar strip lines, CC: Cascode topology

CPW: Coplanar Waveguide

4.3.2. Distributed Oscillators

A distributed oscillator is derived from a distributed amplifier by connecting its output node to the input. The frequency of oscillation depends on the total delay time for the signal traveling from the input to the output. Since the extension of bandwidth in a distributed amplifier comes at a price of larger time delay between its input and output due to the transmission lines or LC ladder network, this delay can be used to design a distributed amplifier based oscillator. There are some distributed oscillators that have been realized in CMOS. Kleveland *et al.* use the forward gain operation mode of the distributed amplifier to realize a 17 GHz 0.18µm CMOS distributed oscillator with off-chip termination and without any tuning capability [22]. Wu *et al.* propose two tuning schemes for distributed voltage controlled oscillators (DVCO) namely inherent-varactor

tuning and delay-balanced current steering tuning. They implement a 10 GHz CMOS DVCO and a 12 GHz bipolar DVCO in a 0.35µm BICMOS process [25].

4.3.3. Distributed Active Transformer (DAT) Power Amplifier

The DAT power amplifier is another example of a distributed circuit which uses a distributed method to perform impedance transformation and power combining simultaneously to achieve large output power while maintaining acceptable power efficiency. It overcomes the low breakdown voltage of short-channel MOS transistors and alleviates the substrate loss problems by providing power gain through multiple similar stages and signal paths [26]. This helps in realizing watt-level fully integrated CMOS power amplifiers.

CHAPTER V

DISTRIBUTED AMPLIFIERS AND TRANSMISSION LINES

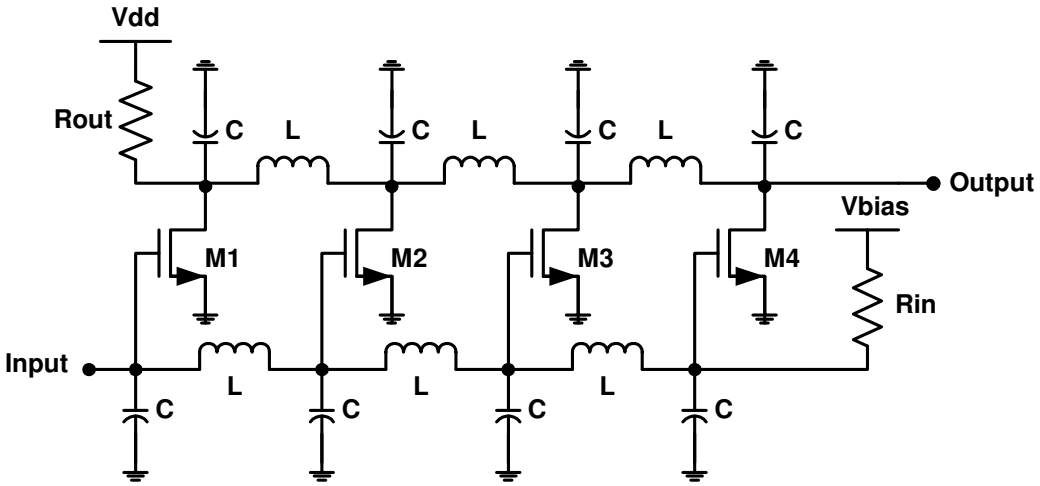
In this chapter, the underlying theory and operation of distributed amplifiers is presented. The chapter also discusses the issues and the procedure to design transmission lines on silicon substrate.

5.1. Distributed Amplifier – Principle of Operation

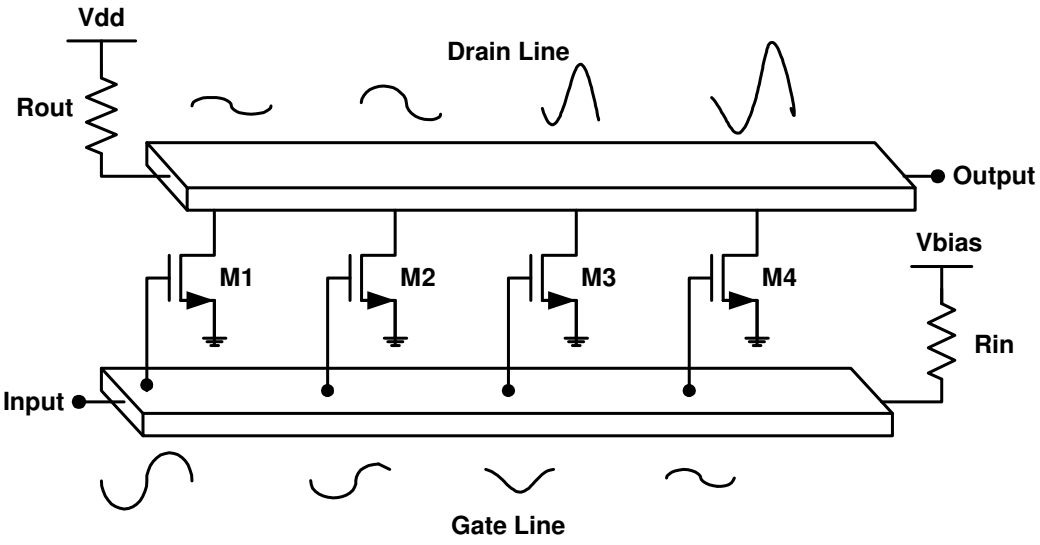
For a single stage lumped amplifier, the gain-bandwidth product is limited by $\frac{g_m}{C}$ [13], where g_m is the transconductance of the device, and $C = \lim_{\omega \to \infty} \frac{1}{j\omega Z}$ (Z is the load impedance) (also known as Bode-Fano limit), which is determined by the parasitic capacitance. This limit is solely dictated by the intrinsic parameters of the device. A distributed amplifier absorbs the parasitic capacitances of the devices into transmission like structures which form a high order LC ladder filter, while combining gain in an additive fashion.

Fig. 5.1 shows a basic distributed amplifier. A distributed amplifier consists of a gate line and a drain line implemented either by artificial transmission lines (comprising of cascade of LC filter sections to form a ladder type structure) or by uniform transmission lines. These two lines are coupled via active devices (transistors). The operation of a distributed amplifier is based on the fact that the signal from the input travels forward (towards the right in Fig. 5.1 (a) or (b)) along the gate line and gets

amplified by each transistor. The drain line carries these amplified signals both in the forward and reverse direction. The forward traveling-waves on the drain line are in



(a)



(b)

Fig. 5.1. Distributed amplifier with (a) LC ladder sections (b) transmission lines

phase synchronization with the forward traveling wave of the gate line and with each other, implying that each device adds power in phase to the output signal at each tap point on the drain line. The forward traveling-wave on the gate line and the reverse traveling-wave on the drain line are absorbed by terminations which are generally matched to the loaded gate and drain lines.

Next a brief overview of transmission line theory will be presented and then we shall focus on implementation of transmission lines on silicon.

5.2. Transmission Line Theory

As shown in Fig. 5.2 [27] a transmission line is often schematically represented as a two-wire line, since transmission lines (for TEM wave propagation) always have at least two conductors. An infinitesimal piece of the transmission line of length Δz can be modeled as a lumped-element circuit, as shown in Fig. 5.2, where R, L, G, C are per unit length quantities defined as follows:

R = series resistance per unit length, for both conductors, in Ω/m.

L = series inductance per unit length, for both conductors, in H/m.

G = shunt conductance per unit length, in S/m.

C = shunt capacitance per unit length, in F/m.

The series inductance L represents the total self-inductance of the two conductors and the shunt capacitance C is the capacitance between the conductors. The series resistance R represents the finite conductivity of the conductors and the shunt conductance G

represents the dielectric loss of the material between the conductors. Both *R* and *G* quantify loss.

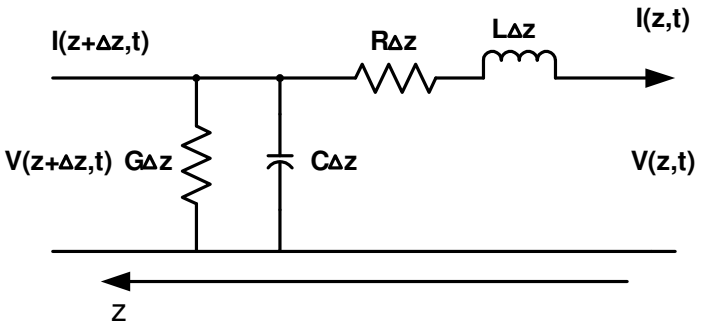


Fig. 5.2. Transmission line model

Assuming steady-state condition, and representing the current and voltage as phasors we have

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{5.1}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{5.2}$$

Solving the above two equation simultaneously we have

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{5.3}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{5.4}$$

where $\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$ is the complex propagation constant (a function of frequency), α is the attenuation constant and $\beta = \frac{2\pi}{\lambda}$ is the wave number.

The solutions of the above equations can be found as

$$V(z) = V_o^+ e^{-\gamma z} + V_o^- e^{\gamma z} \tag{5.5}$$

$$I(z) = I_o^+ e^{-\gamma z} + I_o^- e^{\gamma z} \tag{5.6}$$

where $e^{-\gamma z}$ and $e^{+\gamma z}$ terms represent wave propagation in the $+z$ and $-z$ directions respectively. The current can be expressed as

$$I(z) = \frac{V_o^+ e^{-\gamma z} - V_o^- e^{\gamma z}}{Z_C} \tag{5.7}$$

where $Z_C = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$ is defined as the characteristic impedance of the transmission line. The phase velocity is given by

$$v_p = \frac{\omega}{\beta} = \lambda f \tag{5.8}$$

The transmission line parameters (Z_C and γ) are complex as can be seen from the expressions. For most practical microwave transmission lines the loss is small and hence the low loss approximation can be used to express the transmission line parameters. Rearranging the expression for γ as

$$\begin{aligned} \gamma &= (j\omega L)(j\omega C)\sqrt{\left(1 + \frac{R}{j\omega L}\right)\left(1 + \frac{G}{j\omega C}\right)} \\ &= j\omega\sqrt{LC}\sqrt{1 - j\left(\frac{R}{\omega L} + \frac{G}{\omega C}\right) - \frac{RG}{\omega^2 LC}} \end{aligned} \tag{5.9}$$

For low-loss case assuming $R << \omega L$ and $G << \omega C$, then $RG << \omega^2 LC$ and hence (5.9) can be expressed as

$$\gamma = j\omega\sqrt{LC}\sqrt{1-j\left(\frac{R}{\omega L}+\frac{G}{\omega C}\right)} \tag{5.10}$$

Applying Taylor's series expansion for the square-root term and taking the first higher order real term we have

$$\gamma \approx j\omega\sqrt{LC}\left(1-\frac{j}{2}\left(\frac{R}{\omega L}+\frac{G}{\omega C}\right)\right) \tag{5.11}$$

so that

$$\alpha \approx \frac{1}{2}\left(R\sqrt{\frac{C}{L}}+G\sqrt{\frac{L}{C}}\right)=\frac{1}{2}\left(\frac{R}{Z_C}+GZ_C\right) \tag{5.12}$$

$$\beta \approx \omega\sqrt{LC} \tag{5.13}$$

where $Z_C = \sqrt{L/C}$ is the characteristic impedance of the line in the absence of loss. With the same approximations the characteristic impedance can be approximated as

$$Z_C = \sqrt{\frac{(R+j\omega L)}{(G+j\omega C)}} \approx \sqrt{L/C} \tag{5.14}$$

For a lossless line $R = G = 0$, implying

$$\gamma = \alpha + j\beta = j\omega\sqrt{LC} \tag{5.15}$$

$$\alpha = 0 \tag{5.16}$$

$$\beta = \omega\sqrt{LC} \tag{5.17}$$

and the characteristic impedance reduces to

$$Z_C = \sqrt{L/C} \tag{5.18}$$

The phase velocity for low-loss case and no loss case is almost the same and is given by

$$v_p = \frac{1}{\sqrt{LC}} \tag{5.19}$$

5.3. Transmission Line Design on Silicon Substrate

Although there has been several implementations using artificial transmission lines that is inductors and capacitors to form a ladder network, but because of the lossy silicon substrate, the quality of these passives is not good. Transmission lines which are an alternative to inductors also suffer from similar issues, but according to [28], compared to spiral inductors, transmission lines have lower loss and less parasitic capacitance for the same value of inductance. Lower capacitance implies higher cut-off frequency and hence higher frequency of operation. Besides, at very high frequencies, the spiral inductors can no longer be considered as lumped, in fact they would have a distributed behavior and inductor modeling becomes very complex. Considering all these facts it is better to go for design using transmission lines.

The low-resistivity bulk silicon which causes significant high frequency loss is the main bottleneck towards realizing circuits operating at very high frequencies in CMOS. With the advancement in IC technology it is predicted [22] that the top metal layers become thicker and so is the dielectric between the metal layers. This results in a great amount of isolation from the substrate and hence the top metals are conducive for realizing low loss passive elements. Using line widths comparable to that of the dielectric thickness helps in confining the field lines and since a large surface area of the

conductor is now used for current conduction, this helps reducing the skin effect [22].

5.3.1. Transmission Line Types

Different types of transmission lines can be realized on silicon. Next we evaluate these types of transmission lines in terms of their loss and characteristic impedance. Fig. 5.3 shows different types of transmission lines. The simplest is a microstrip line which has a single signal line with the silicon substrate underneath as shown in Fig. 5.3(a). This structure has a very high loss because all the field lines terminate in the substrate and besides, since the capacitance to the substrate is high this structure has poor characteristic impedance. Fig. 5.3(b) shows an improved version that is a microstrip line with a metal ground plane (one of the lower metal layers forming the ground plane). In this case since all the field lines terminate in the ground plane they rarely penetrate the silicon substrate and hence the loss is drastically reduced and again due to the proximity of the metal layer to the top metal layer as compared to the substrate, this structure provides very low characteristic impedance compared to the previous structure. This substrate shielding effect provided by the ground plane results in the lowest loss amongst various transmission lines. A coplanar waveguide has three lines (ground, signal and ground) above the silicon substrate and is shown by Fig. 5.3(c). Most of the field lines terminate in these ground lines and hence there is low loss due to the substrate. The characteristic impedance of these structures is decent due to the fact that most of the field is confined between the lines and hence the inductance per unit length of the line, L is high.

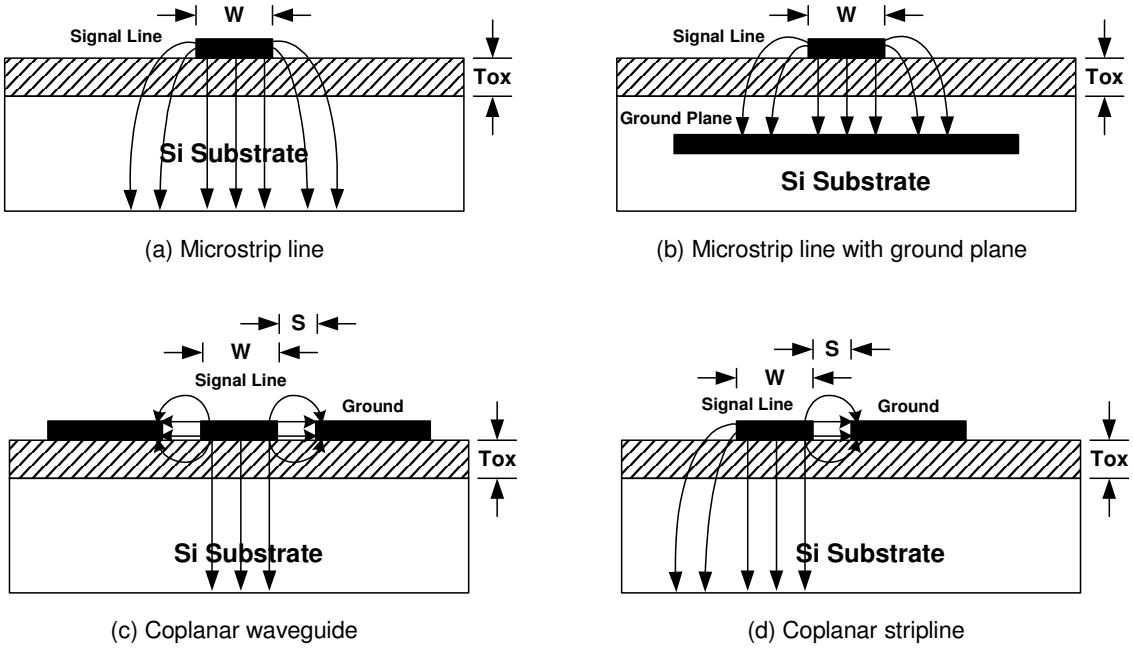


Fig. 5.3. Types of transmission lines on silicon

Finally Fig. 5.3(d) shows what is called as a coplanar stripline comprising of a signal and a ground line with the silicon substrate underneath. This structure has been proven to be the best compromise between loss and characteristic impedance. The loss is low due to the same reason as that of the coplanar waveguide and the impedance is the highest because of reduced capacitance per unit length. Above all the coplanar stripline occupies less area as compared to that of a coplanar waveguide and hence is preferred.

From the above knowledge of the variation of transmission line parameters it can be concluded that for a low loss transmission line the fields have to be confined between the lines and the lines must be far from the substrate, which implies a larger inductance and lower capacitance both per unit length of the lines. This defines a clear trade-off

between loss and characteristic impedance. From the discussion in the previous paragraph it can be concluded that coplanar stripline provides the best trade-off.

5.3.2. Simulation of Transmission Lines

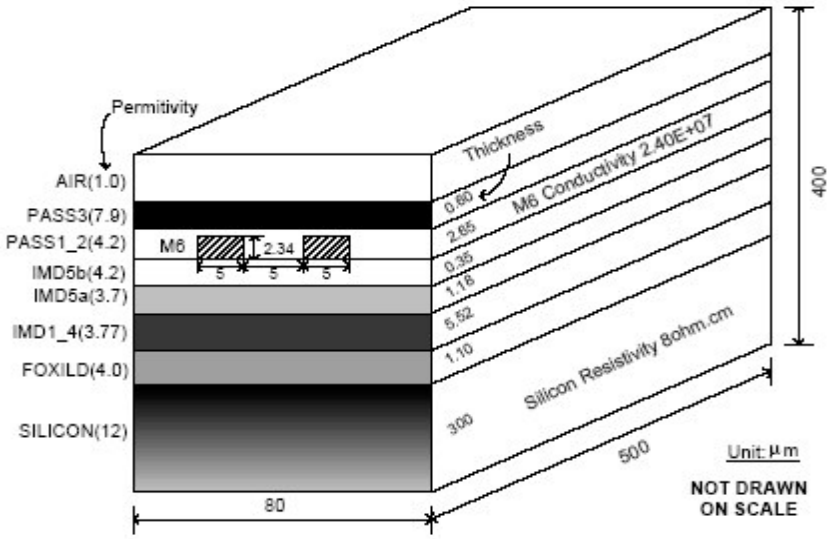


Fig. 5.4. Structure of the silicon substrate in a 0.18µm CMOS process

Fig. 5.4 shows the structure of the silicon substrate for a 0.18µm CMOS process. After having decided the type of transmission line to be used the method of simulation needs to be defined. Different available electromagnetic (EM) simulators target on different problems and use different methods of solving as shown in Table 5.1 [29].

HFSS which is a 3D simulator uses finite element method or FEM to accurately simulate very complex 3D structures, which is at the expense of large simulation time and memory. 2.5D simulators are basically 2D simulators with additional capability of

Table 5.1. EM simulators

Simulator	Dimension	Method	Computing Load	Targeting Problem
HFSS	3D	FEM	Large	Antenna, board
Sonnet	2.5D	Moment	Medium	IC, board
IE3D	2.5D	Moment	Low-Medium	IC, board
Momentum	2D	Moment	Medium	IC, board
Asitic	2D	Green's Functions	Low	On-chip inductors

taking into account the dielectric or metal thickness. These simulators such as Sonnet and IE3D use the method of moment and are very suitable for IC design because of the planar structure [29]. Asitic is a program to simulate on-chip inductors and it uses Green's functions. For this design IE3D has been used to simulate coplanar strip lines of various widths and spacing.

Fig. 5.5 shows the simulated characteristic impedance of coplanar strip lines with W = 4, 10 and 20µm. The coplanar strip lines have both their signal and ground lines to be of same width. Each line is 900µm long. The spacing between the signal and ground lines varies as 4, 6, 8 and 10µm for each value of width. It can be concluded from the figure that the characteristic impedance of the line is higher for smaller line widths and for a particular width, the characteristic impedance increases with increase in spacing between the signal and ground line. The reasons for the above mentioned characteristic can be outlined as follows. The line inductance decreases logarithmically with line width [30] whereas the line capacitance increases linearly with line width because of a linear increase in the area component. Hence the characteristic impedance decreases

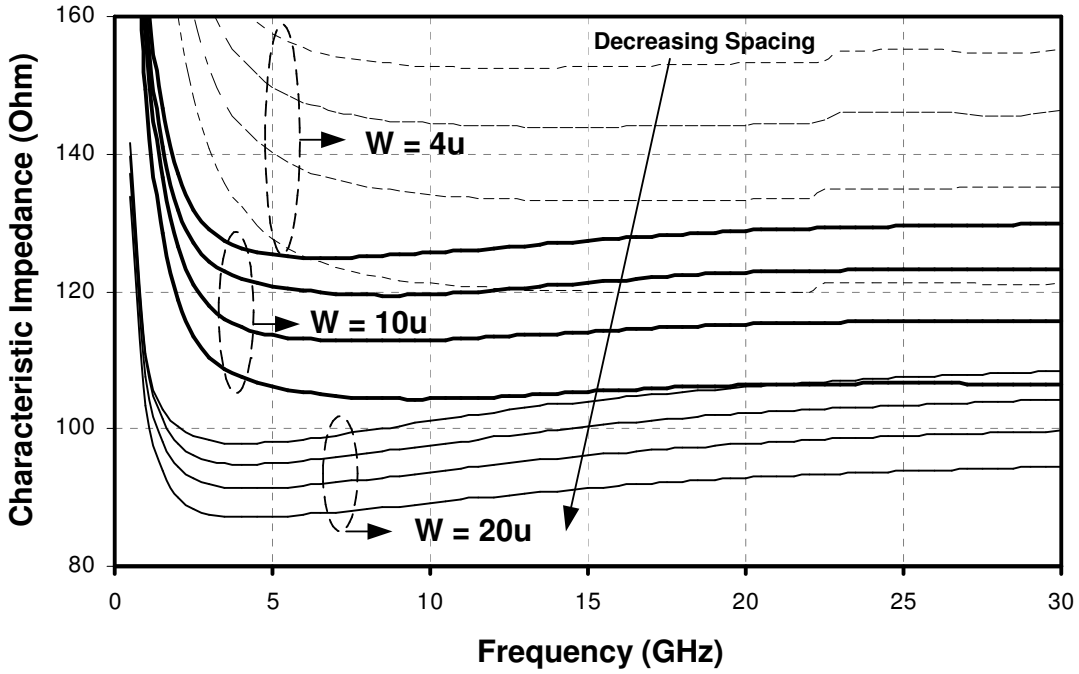


Fig. 5.5. Simulated characteristic impedance of coplanar strip lines with width W = 4, 10, 20µm and each with spacing S = 4, 6, 8, 10µm.

with line width. For a constant width when the spacing increases between the lines the fringe capacitance decreases and the line inductance increases because now more flux is contained between the signal and ground line. This results in an increase in the characteristic impedance of the line.

The following equations [30] can justify the above reasons cited

$$L = 0.6 + 0.03.\ln(S) - 0.15.\ln(W) + 0.13.\ln\left(\frac{7}{f}\right) \qquad 5.20)$$

The inductance (L in nH/mm) is mainly a function of line width (W in µm) and frequency (f in GHz for 100MHz< f <7GHz). The spacing dependence to the adjacent

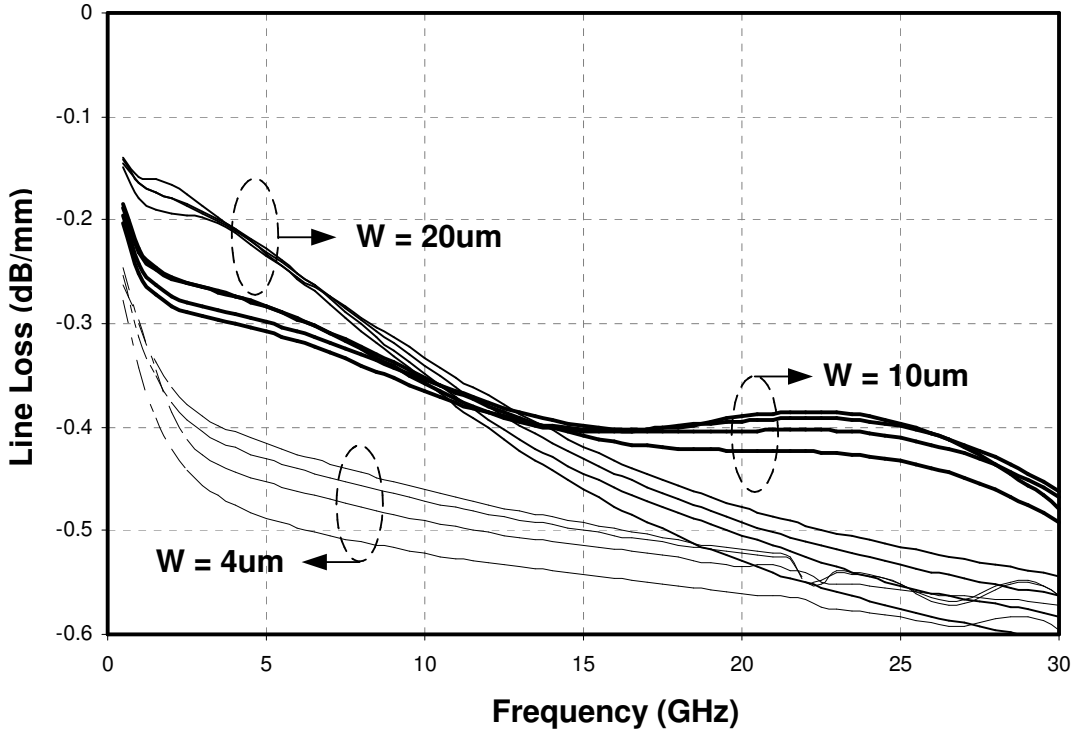


Fig. 5.6. Simulated line loss for different coplanar strip lines

ground line is so small that it can almost be ignored (S in μm). At frequencies between 7GHz and 20GHz, the frequency dependence is even weaker and the above equation reduces to

$$L = 0.6 + 0.03.\ln(S) - 0.15.\ln(W) \tag{5.21}$$

Fig. 5.6 shows the line loss, α in dB/mm for coplanar strip lines of different widths and spacing. A narrow width line with narrow spacing has higher series resistance and hence higher loss as compared to a wider line. From Fig. 5.6 it is seen that at higher frequencies the above reasoning does not hold good. A wide line has more loss than a narrow line; this can be attributed to the high frequency shunt loss through the

substrate because of more field lines coupling into the substrate [30]. In the case of lines whose widths and spacing are comparable to the oxide thickness the field lines can easily couple to the substrate and mostly contribute to loss at high frequencies. The coplanar strip line with W=4µm and S=10µm was chosen for the design of the distributed LNA because of its high characteristic impedance.

CHAPTER VI

DISTRIBUTED AMPLIFIER AS A BROADBAND LOW NOISE AMPLIFIER

6.1. Distributed Low Noise Amplifier Characteristics

The possibility of using a distributed amplifier for the design of a broadband LNA has been explored. A typical LNA has the following characteristics:

(a) High gain

(b) Low noise

(c) Good input impedance matching

(d) Good Linearity

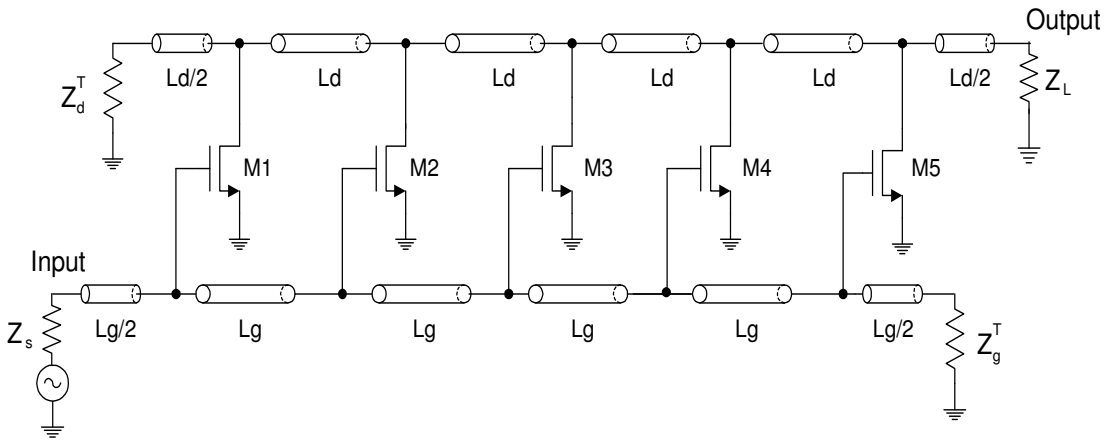


Fig. 6.1. A five stage distributed amplifier

Besides the above, it should be broadband in nature and operate at higher frequencies. Fig. 6.1 shows a 5-stage (section) distributed amplifier with nmos

transistors. Assuming the transmission lines to be lossless, the MOS transistors are modeled as a gate source capacitance, drain source capacitance and a transconductance. Since the transmission lines are periodically loaded with the MOS devices, these capacitances can be assumed to be uniformly distributed across the length of a unit cell transmission line i.e. C_{gs} of each transistor across a gate line length of l_g, from $-\frac{l_g}{2}$ to $+\frac{l_g}{2}$ and C_{ds} of each transistor across a drain line length of l_d, from $-\frac{l_d}{2}$ to $+\frac{l_d}{2}$, for each section. If the intrinsic gate and drain lines have their distributed parameters given by L_d, C_d, L_g and C_g then the propagation constant and the characteristic impedance of the loaded lines is given by [13]:

$$\gamma_g \approx j\beta_g = j\omega\sqrt{L_g\left(C_g + \frac{C_{gs}}{l_g}\right)} \tag{6.1}$$

$$Z_g^C \approx \sqrt{\frac{L_g}{\left(C_g + \frac{C_{gs}}{l_g}\right)}} \tag{6.2}$$

for the gate line and

$$\gamma_d \approx j\beta_d = j\omega\sqrt{L_d\left(C_d + \frac{C_{ds}}{l_d}\right)} \tag{6.3}$$

$$Z_d^C \approx \sqrt{\frac{L_d}{\left(C_d + \frac{C_{ds}}{l_d}\right)}} \tag{6.4}$$

for the drain line respectively.

6.1.1. Gain of the Distributed Amplifier

The current generated due to the transconductance can be assumed to be spread across each segment of the line. Under perfect matching conditions both the lines are terminated by their characteristic impedances i.e.

$$Z_S = Z_g^C = Z_g^T \tag{6.5}$$

and

$$Z_L = Z_d^C = Z_d^T \tag{6.6}$$

Assuming phase synchronization on each of the lines we have

$$\beta_g l_g = \beta_d l_d = \beta l = \theta \tag{6.7}$$

Again from [13] the voltage gain is given by

$$A_v = -\frac{N g_m Z_d^C}{2} e^{-jN\theta} \tag{6.8}$$

where N is the number of stages or sections in the amplifier. With the increase in the number of sections in a distributed amplifier the gain increases linearly but so long as the conditions of uniform loading is valid. The power gain of the distributed amplifier (assuming lossless transmission lines) can be written as

$$G = \frac{N^2 g_m^2 Z_d^C Z_g^C}{4} \tag{6.9}$$

In practical implementation in silicon the transmission lines cannot be devoid of losses. In fact, the loaded gate and drain lines will have α_g and α_d as the real part of

their propagation constants respectively. Although imaginary components do appear in the propagation constants, their contribution is negligible in the useful frequency range. Under phase synchronization condition of (6.7), the power gain of the amplifier is [13]

$$G \approx \frac{g_m^2 Z_d^C Z_g^C}{4} \left| \frac{e^{-N\alpha_g l_g} - e^{-N\alpha_d l_d}}{\alpha_g l_g - \alpha_d l_d} \right|^2 \tag{6.10}$$

Thus the gain does not increase monotonically with N and at a particular frequency the optimum value of N is given by [13].

$$N_{opt} = \frac{\ln(\alpha_d l_d) - \ln(\alpha_g l_g)}{\alpha_d l_d - \alpha_g l_g} \tag{6.11}$$

Fig. 6.2 shows the variation in gain with number of stages of the distributed amplifier. It is seen that gain increases with N at low frequencies. For N=5 we obtain a higher and flatter gain performance over a large bandwidth and less peaking as compared to N=4 and 6. A higher gain could be obtained by a higher transconductance of the transistors, which under low-power constraint would imply large transistor sizes. A high characteristic impedance of the transmission lines can also boost the gain. Such high impedance could be achieved by increasing the inductance per unit-length implying larger spacing between signal and ground lines. However, this would introduce higher loss. Therefore there are trade-offs between power dissipation, gain, transmission line characteristic impedance and loss.

A higher characteristic impedance transmission line with low capacitance per unit length could be used while obtaining the impedance matching by compensating for the capacitance through a larger transistor size. This seems to be a way to increase the

gain without sacrificing matching. But this comes with a price of lower bandwidth of operation. The frequency of operation of the transmission line depends on the product of

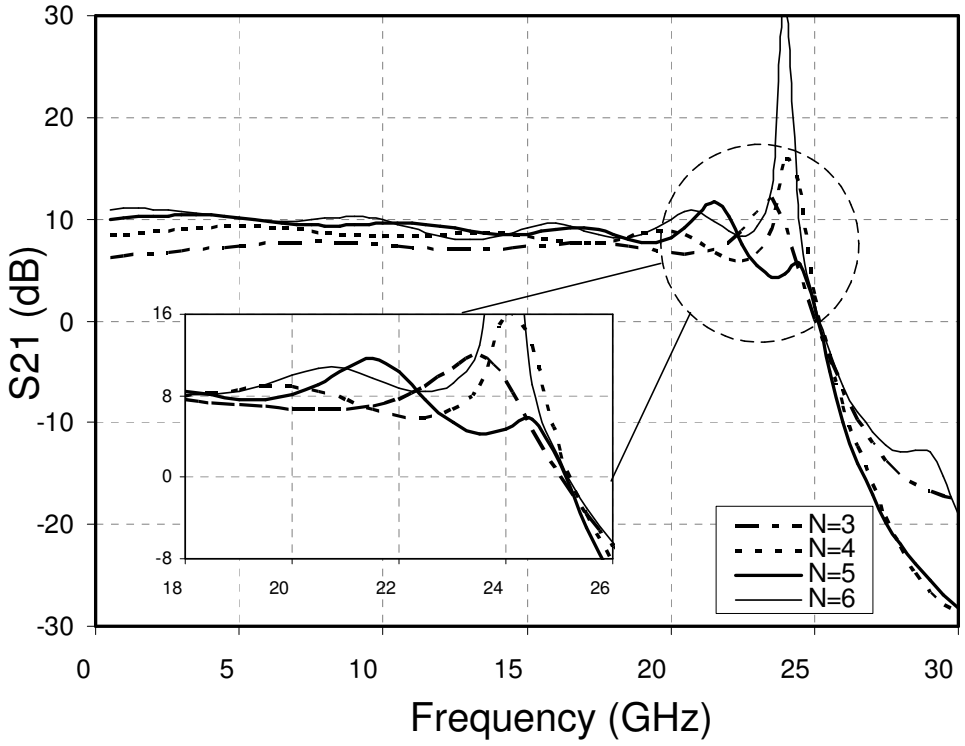


Fig. 6.2. Variation of power gain with number of stages

the inductance and capacitance. Since, from the above discussion a higher inductance and capacitance would be required; the loaded transmission line would be limited in the frequency of operation.

6.1.2. Noise Figure of the Distributed Amplifier

In order to design an amplifier with low noise characteristics one needs to identify the important noise sources in the amplifier and the key controllable

contributors to the overall noise figure of the amplifier. Fig. 6.3 shows the approximate noise model of a mos transistor. The intrinsic noise sources of the transistor shown in the figure are [31]:

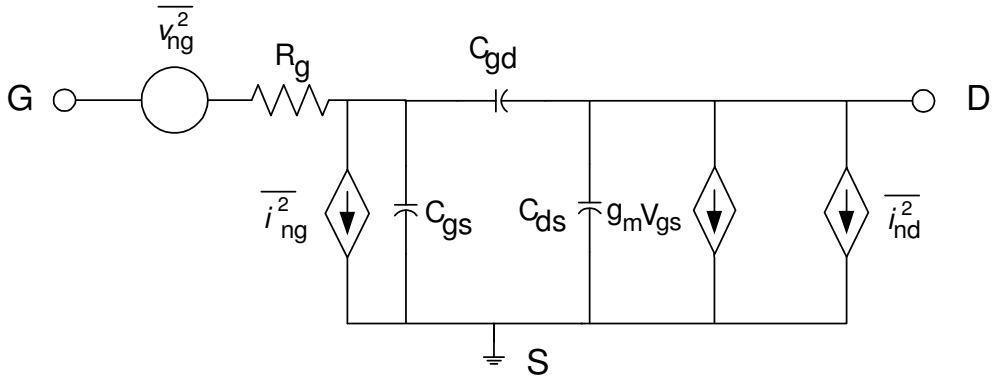


Fig. 6.3. Approximate noise model of a MOSFET.

(i) Drain channel noise ($\overline{i_{nd}^2}$): This is the thermal noise due to the carriers in the channel region. This is given by $\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f$ where γ is a bias dependent parameter, g_{do} is the zero drain voltage conductance of the device (generally taken to be the transconductance of the device, g_m), k is the Boltzmann's constant, T is the temperature of the carriers in the channel and Δf is the noise bandwidth.

(ii) Gate resistance noise ($\overline{V_{ng}^2}$): This is the thermal noise generated by the gate resistance and is given by $\overline{V_{ng}^2} = 4kT\frac{R_{g,sq}}{3}\frac{W}{L}\Delta f$, where $R_{g,sq}$ is the sheet resistance of the gate material, W is the width of the device and L is the

length of the channel region. The factor of three accounts for the distributed nature of the intrinsic gate region. The gate resistance of a MOS transistor affects the RF performance in three ways. First, if the gate resistance is not accounted for at the simulation stage of a circuit, errors would result in power matching the device to off-chip source impedance (e.g., 50). Second, the value of the gate resistance strongly influences the minimum noise figure of the transistor. Third, the power gain of the MOS transistor is strongly governed by the gate resistance. It is commonly assumed that if one uses a fingered structure for the gate then this noise can be fairly ignored.

(iii) *Induced gate noise* ($\overline{i_{ng}^2}$)*:* This noise is due to the thermal noise generated by the carriers in the channel, which capacitively couples itself onto the gate node as a gate current and is given by $\overline{i_{ng}^2} = 4kT\delta\frac{\omega^2 C_{gs}^2}{5g_{do}}\Delta f$ where δ is the gate noise coefficient.

Since the channel drain noise and the induced gate noise have the same physical origin, they are correlated with a correlation coefficient defined as $c \equiv \frac{\overline{i_{ng}.i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}.\overline{i_{nd}^2}}}$. The long-channel value of c is theoretically j0.4 and approaches j0.3 as the frequency of operation increases.

Assuming that the losses due to the transmission lines can be ignored for simplicity, the only other contributors of noise are the termination resistors and the source. Again, the noise due to each of the transistors can be considered uncorrelated.

Now, assuming that the drain current source is distributed across each segment (see Fig. 6.4 which shows the noise model for a unit section of the distributed LNA) of the transmission line that is the drain line is periodically driven by a noise current given by $\frac{i_{nd}}{l_d}$. The noise voltage at the load due to the noise current source of the kth section is

$$v_{nd,k} = \int_{(k-1)l_d}^{kl_d} \frac{i_{nd}}{l_d} \frac{Z_d^C}{2} e^{-j\beta_d (Nl_d - x_d)} dx_d = \frac{1}{2} i_{nd} Z_d^C \left(\frac{\sin\frac{\theta}{2}}{\frac{\theta}{2}} \right) e^{-j\theta\left(N-k+\frac{1}{2}\right)} \tag{6.12}$$

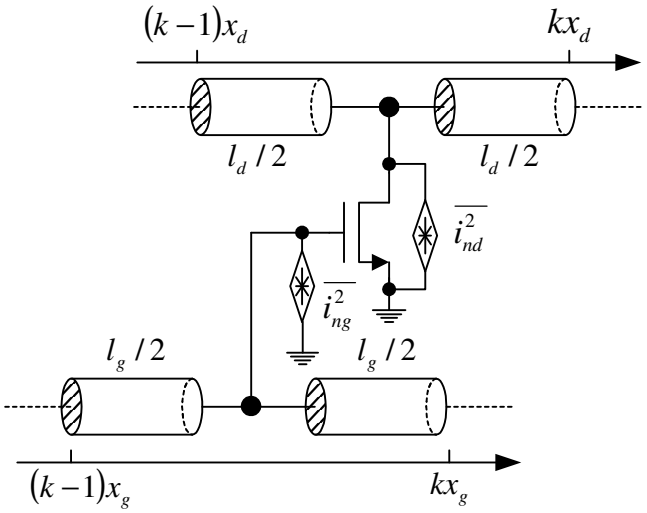


Fig. 6.4. Noise model of a unit-section of the distributed LNA

When the gate noise is injected into the kth section gate line at $(k-1)l_g$ then the noise voltage due to gate noise at the load has two components [32]:

$$v_{ng,k}^{+} = \frac{1}{4} g_m Z_g^C Z_d^C i_{ng} \left(N - k + \frac{1}{2} \right) e^{-j\left(N-k+\frac{1}{2}\right)\theta} \tag{6.13}$$

due to the forward propagation and

$$v_{ng,k}^{-} = \frac{1}{4} g_m Z_g^C Z_d^C i_{ng} \frac{\sin\left(k-\frac{1}{2}\right)\theta}{\theta} e^{-j\left(k-\frac{1}{2}\right)\theta} e^{-j\left(N-k+\frac{1}{2}\right)\theta} \tag{6.14}$$

due to the reverse propagation respectively.

Combining (6.12), (6.13) and (6.14) together results in the total output noise voltage due to the transistors in the k-th section and is given by

$$v_{no,k} = \left[\left(\frac{\sin\frac{\theta}{2}}{\theta} \right) i_{nd} + \frac{1}{4} M(k) g_m Z_g^C i_{ng} \right] Z_d^C e^{-j\theta\left(N-k+\frac{1}{2}\right)} \tag{6.15}$$

where $M(k) = \left(N-k+\frac{1}{2}\right) + \frac{\sin\left(k-\frac{1}{2}\right)\theta}{\theta} e^{-j\left(k-\frac{1}{2}\right)\theta}$. From the discussion above we know that i_{ng} and i_{nd} are correlated with a correlation coefficient c. Hence i_{ng} can be decomposed into a part which is correlated with i_{nd} that is i_{ngc} and another completely uncorrelated that is i_{ngu}. Hence,

$$i_{ng} = i_{ngu} + i_{ngc} \tag{6.16}$$

where

$$\overline{i_{ngu}^2} = 4kTG_u\Delta f \tag{6.17}$$

$$i_{ngc} = F_c i_{nd} \tag{6.18}$$

and

$$G_u = \delta \frac{\omega^2 C_{gs}^2}{5 g_{do}} \left(1 - |c|^2\right) \tag{6.19}$$

$$F_c = j\,|\,c\,|\sqrt{\frac{\delta}{5\gamma}}\frac{\omega C_{gs}}{g_{do}} \tag{6.20}$$

Substituting the above in (6.15) the total noise power at the load due to the transistors ignoring the gate resistance noise is given by (6.21) as

$$P_{no} = 4kTg_m Z_d^C \frac{\gamma}{\alpha}\Delta f \sum_{k=1}^{N}\left|\frac{\sin\frac{\theta}{2}}{\theta} + \frac{1}{4}g_m Z_g^C F_c M(k)\right|^2 + \frac{1}{4}kTg_m^2 G_u (Z_g^C)^2 Z_d^C \Delta f \sum_{k=1}^{N}|\,M(k)\,|^2 \tag{6.21}$$

where $\alpha = \frac{g_m}{g_{do}}$.

The output noise power due to the drain line termination impedance Z_d^T is given by

$$P_{ndT} = kT\Delta f \tag{6.22}$$

due to the gate line termination impedance is given by

$$P_{ngT} = kT\Delta f G\left|\frac{\sin N\theta}{N\theta}\right|^2 \tag{6.23}$$

and that due to the source resistance is given by

$$P_{nS} = kT\Delta f \tag{6.24}$$

Hence from the definition of noise figure we have the noise figure of an N stage distributed amplifier given by

$$F = 1 + \frac{P_{ngT} + P_{ndT} + P_{no}}{P_{nS} G} \tag{6.25}$$

where G is given by (6.9).

$$\Rightarrow F = 1 + \left|\frac{\sin N\theta}{N\theta}\right|^2 + \frac{4}{N^2 g_m^2 Z_d^C Z_g^C} + \frac{16}{N^2 g_m Z_g^C}\frac{\gamma}{\alpha}\sum_{k=1}^{N}\left|\frac{\sin\frac{\theta}{2}}{\theta} + \frac{1}{4} g_m Z_g^C F_c M(k)\right|^2$$

$$+ \frac{1}{N^2} G_u Z_g^C \sum_{k=1}^{N} |M(k)|^2 \tag{6.26}$$

Equation (6.26) can be further simplified by assuming large values of N. In that case

$$\sum_{k=1}^{N}\left|M(k)\right|^2 \approx \sum_{k=1}^{N}\left|(N-k+\frac{1}{2})\right|^2 = \frac{N^3}{3} \tag{6.27}$$

and hence

$$\sum_{k=1}^{N}\left|\frac{\sin\frac{\theta}{2}}{\theta} + \frac{1}{4} g_m Z_g^C F_c M(k)\right|^2 \approx N\left(\frac{\sin\frac{\theta}{2}}{\theta}\right)^2 + \frac{1}{16} g_m^2 \left(Z_g^C\right)^2 \left|F_c\right|^2 \frac{N^3}{3} \tag{6.28}$$

Ignoring the second and third term in (6.26) for large N the noise figure expression for the distributed amplifier with real transmission lines is given by

$$F = 1 + \frac{1}{NZ_g^C}\frac{4\gamma}{\alpha}\frac{1}{g_m}\left(\frac{\sin\frac{\theta}{2}}{\frac{\theta}{2}}\right)^2 + NZ_g^C \frac{\alpha\delta}{3}\frac{\omega^2 C_{gs}^2}{5g_m} \tag{6.29}$$

The second term in (6.28) is not included in (6.29) because this term after substitution in (6.26) results in a term which is $|c|^2$ times the second term in (6.29). Since the value of $|c|$ is small and less than 1, $|c|^2$ is even smaller than 1 and hence the term can be ignored as compared to the second term in (6.29). This essentially removes the correlation between the gate and drain noise current sources. There exists an optimum value of NZ_g^C for minimum noise figure at a particular frequency and is given by

$$\left(NZ_g^C\right)_{opt} = \frac{2}{\alpha}\sqrt{\frac{15\gamma}{\delta}}\left(\frac{\sin\frac{\theta}{2}}{\frac{\theta}{2}}\right)\frac{1}{\omega C_{gs}} \tag{6.30}$$

and the minimum noise figure is given by

$$F_{\min} = 1 + 4\sqrt{\frac{\delta\gamma}{15}}\frac{\omega C_{gs}}{g_m}\left(\frac{\sin\frac{\theta}{2}}{\frac{\theta}{2}}\right) \tag{6.31}$$

Since Z_g^C is close to 50 ohms for input matching the only variable to optimize noise figure is N i.e. the number of stages or sections. It is shown next as to how noise figure varies with N. Fig. 6.5 shows this variation.

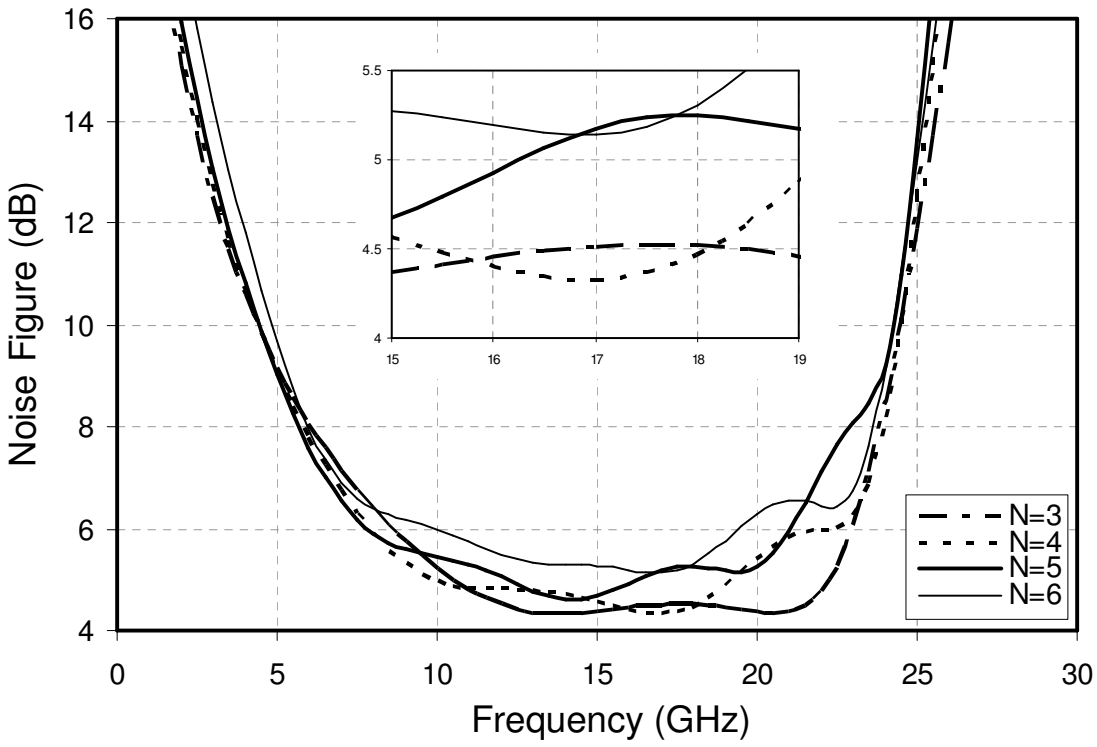


Fig. 6.5. Variation of noise figure with number of stages.

The noise figure is high at both low and high frequencies while remaining flat in between. This is because of the sinc function in (6.29), which dominates at low frequencies between dc and the first null. With increase in frequency the third term in (6.29) increases proportionally to ω^2 . The noise figure further degrades at high frequencies due to gain reduction. From the figure it is evident that at a particular frequency e.g. 17 GHz the minimum noise figure is obtained for a particular N i.e. 4.Noise figure for N=4 decreases at around 22GHz due to the gain peaking as seen in Fig. 6.2.

6.1.3. Input Impedance Matching

A good input matching is provided by having the impedance of the loaded transmission line (gate and drain) equal to the terminating impedance of the line which is generally 50 ohms. It implies that condition (6.5) and (6.6) are to be satisfied. This demands proper modeling of the transmission lines with EM simulators like HFSS, IE3D or Sonnet. In this case the transmission lines were simulated with IE3D. On loading the impedance will change and hence the transmission lines are over designed for their characteristic impedances so that they can compensate the loading in order to match a termination of 50 ohms.

6.1.4. Linearity

Intercept and 1-dB compression point are two common measure of linearity, but they are by no means the only ones. Many others exist and, in fact, more could be

defined. Two other measure of linearity that are common in wide-band systems handling many signals simultaneously are called *composite triple-order beat* (CTB) and *composite second order beat* (CSO) [33]. In these tests of linearity, N signals of voltage v_i are applied to the circuit equally spaced in frequency. Taking three of these signals, the third order non-linearity is given by (6.32)

$$\begin{aligned}\left(x_1+x_2+x_3\right)^3 &= x_1^3+x_2^3+x_3^3 \text{ (HD3)}\\ &+3x_1^2x_2+3x_1^2x_3+3x_2^2x_1+3x_3^2x_1+3x_2^2x_3+3x_3^2x_2 \text{ (IM3)}\\ &+6x_1x_2x_3 \text{ (TB)}\end{aligned} \tag{6.32}$$

The cubic terms constitute the HD3, the last term causes what is called the CTB, in that it creates terms at frequencies $\omega_1 \pm \omega_2 \pm \omega_3$ where $\omega_1 < \omega_2 < \omega_3$. Note that except for the case where all three are added ($\omega_1+\omega_2+\omega_3$) these tones can fall into any of the channels being used and many will fall into the same channel. In fact the *triple-beat* (TB) products are more critical than IM3 products in a wideband system. It can be shown that the maximum number of terms will fall on the tone at the middle of the band. With N tones, it can be shown that the number of tones falling there will be equal to $\frac{3}{8}N^2$. The voltage of these tones is twice that of the IP3 tones. From [33] the TB, CTB and CSO are given by

$$TB(dBm) = P_{IP3} - 3\left(P_{IP3} - P_s\right) + 6 \tag{6.33}$$

$$CTB(dB) = P_s - \left[P_{IP3} - 3\left(P_{IP3} - P_s\right) + 6 + 10\log\left(\frac{3}{8}\right)N^2 \right] \tag{6.34}$$

$$CSO(dB) = P_s - \left[P_{IP2} - 2\left(P_{IP2} - P_s\right) + 10\log\left(N_B\right)\right] \tag{6.35}$$

where P_s is the power level of each fundamental tone, P_{IP3} is the IP3 power level of the given circuit, P_{IP2} is the IP2 power level of the given circuit and N_B is the number of second order beats above any given carrier.

6.1.5. Stability

A microwave amplifier is unconditionally stable [34] for passive source and load termination if

$$|S_{11}| < 1 \tag{6.36}$$

$$|S_{22}| < 1 \tag{6.37}$$

$$K > 1 \tag{6.38}$$

The stability factor K is an important measure of stability and is given by

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|}{2|S_{12}S_{21}|} \tag{6.39}$$

The above conditions are necessary and sufficient conditions for unconditional stability. If any of the above conditions are not satisfied the circuit can be unstable. The peaking in Fig. 6.2 can be attributed to one of these reasons. Fig 6.6 shows the stability factor simulation for the 5-stage distributed LNA. The simulation method is explained in the next section. The stability factor is less than 1 between 19GHz and 25GHz. The LNA is potentially unstable in this region of frequencies.

6.2. Layout and Simulation Results

Fig. 6.7 shows the layout of the 5-stage distributed amplifier. For the design of this circuit the coplanar strip line of width W=4µm and S=10µm was used. This has characteristic impedance close to 155Ω. For a gain of 10dB (3.163V/V) with a 5 stage distributed LNA the transconductance required can be calculated from equation (6.8)

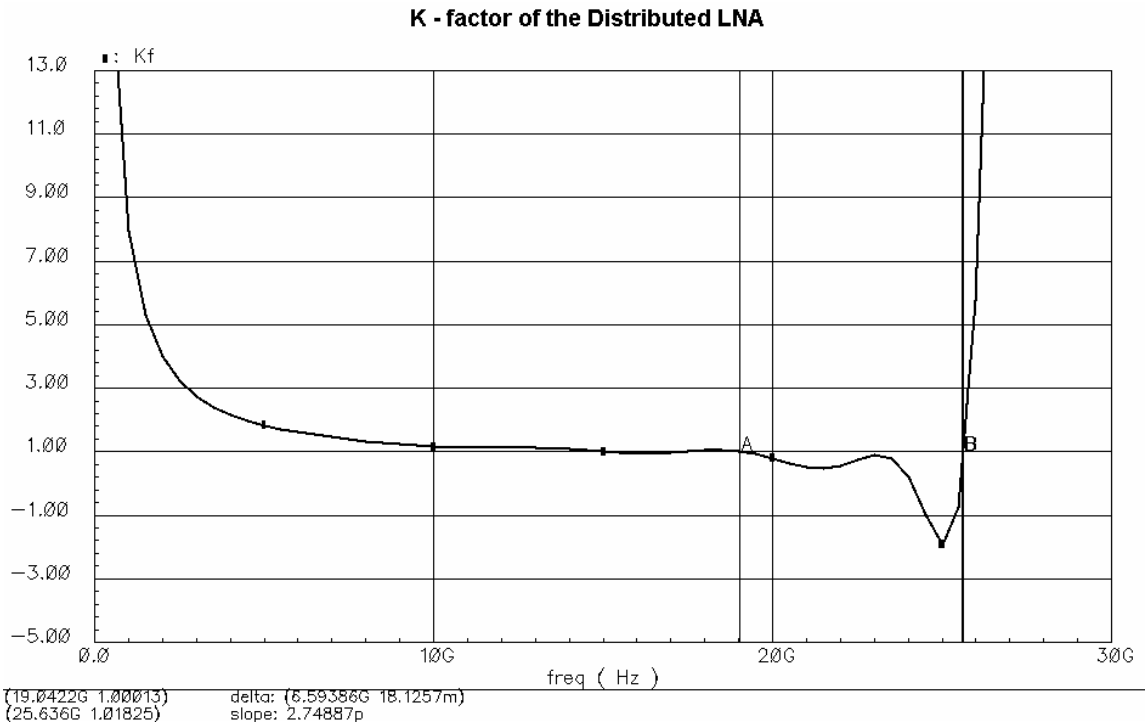


Fig. 6.6. Stability factor (K–factor) of the 5-stage distributed LNA

resulting in $g_m = \frac{3.163}{5 \times (50/2)} = 25.3mA/V$. It is to be remembered that the characteristic impedance of the loaded lines (here it is assumed to be 50Ω under condition of perfect termination) is used in calculations as this is the impedance that the drain current of each

transistor would see. The circuit includes 5 NMOS transistors (W = 65 µm and L = 0.18 µm) each comprising of 26 fingers. A large number of fingers were used to minimize the effect of distributed gate resistance. The value of the distributed gate resistance for a 26 fingered transistor is 4.16Ω. The transmission lines used are coplanar strip-lines with a total length of 4.5mm. The drain and gate lines were terminated with 50Ω. The drain line was biased at 1.2V whereas the gate line was biased at 900mV. Layout considerations include sufficient spacing (>50µm) between the gate and drain lines to avoid coupling

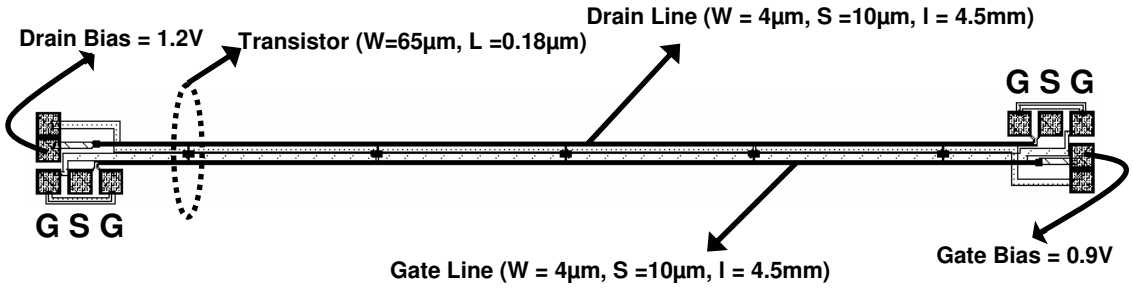


Fig. 6.7. Layout of the 5-stage distributed amplifier

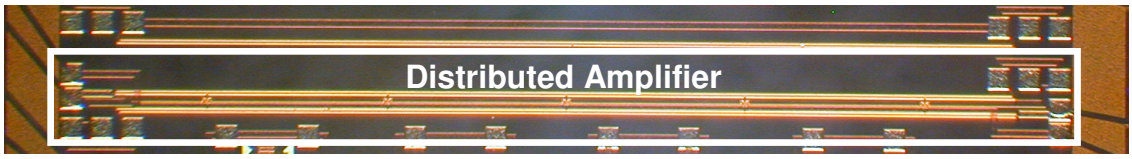


Fig. 6.8. Chip micrograph of the 5-stage distributed amplifier

between each other. The pads are each 100µm by 100µm in dimension. The center to center distance between the ground-signal-ground pads is 150µm. Fig. 6.8 shows the chip micrograph of the 5-stage distributed amplifier in 0.18µm CMOS process.

The simulations were performed using the Spectre circuit simulator in Cadence. The s-parameter files for the transmission lines generated by IE3D (electromagnetic simulator) were used in the N-port component of Spectre for the transmission lines. N-port can incorporate models described by a file of s-parameters. But since s-parameters data are in frequency domain, transient simulations could not be performed.

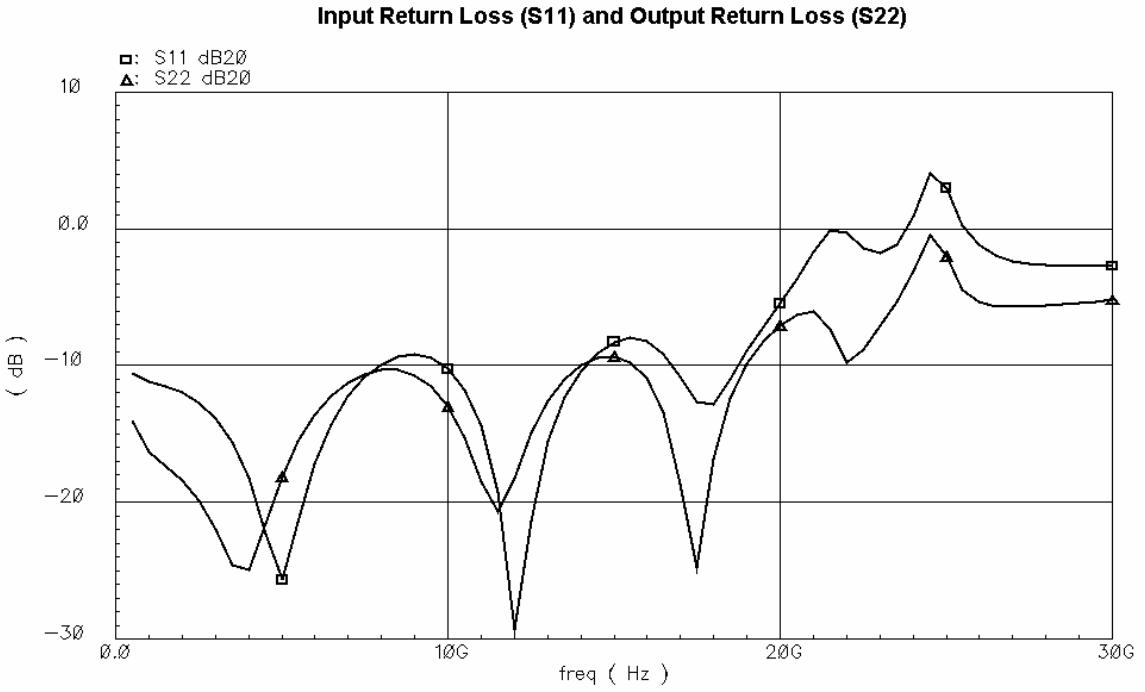


Fig. 6.9. S11 and S22 simulation results

Fig. 6.9 shows the simulation results for S11 and S22 of the distributed amplifier. The input return loss (S11) and the output return loss (S22) are within acceptable range till 18GHz.

Table 6.1 summarizes the simulations result of the distributed amplifier. From

the above simulation results it can be seen that a distributed amplifier has the potential of being used as a low noise amplifier with moderate gain at high frequencies over a large bandwidth.

Table 6.1. Performance summary of the distributed amplifier

Parameter	Value
Power Gain (S21)	9.5 dB ± 1 dB (0.5GHz - 22 GHz)
Unity Gain Bandwidth	25 GHz
Input Return Loss (S11)	< -8 dB (0.5GHz – 19GHz)
Output Return Loss (S22)	< -8 dB (0.5GHz – 19GHz)
Noise Figure	<6.5 dB (6 GHz – 22 GHz)
Power Dissipation	54 mW

6.3. Conclusions

The design of transmission lines on a lossy silicon substrate has been explored. Design considerations for the design of a distributed amplifier as a low-noise front-end were outlined and discussed. Noise analysis of the distributed amplifier with real transmission lines was introduced. The analysis for gain and noise figure was verified with simulation results from a 5-stage distributed amplifier in a 0.18µm CMOS process.

REFERENCES

[1] E. Sánchez-Sinencio and A. G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems: Low-Voltage Mixed-Signal Circuits*. Piscataway, New Jersey: IEEE Press, 1999.

[2] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure," *IEEE Journal of Solid-State Circuits*, vol. 27, pp. 1709-1717, Dec. 1992.

[3] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested Gm-C compensation," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 2000-2011, Dec. 1997.

[4] K. N. Leung and P. K. T. Mok, "Nested Miller compensation in low-power CMOS design," *IEEE Transactions on Circuits and Systems–II*, vol. 48, pp. 388-394, Apr. 2001.

[5] H. T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 339-347, Mar. 1999.

[6] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 221-230, Feb. 2000.

[7] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 48, pp. 1041-1056, Sep. 2001.

[8] B. K. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 237-243, Feb. 2003.

[9] J. Ramos and M. Steyaert, "Three-stage amplifier with positive feedback compensation scheme," in *Proc. IEEE Custom Integrated Circuits Conference*, Orlando, FL, May 2002, pp. 333-336.

[10] H. Lee and P. K. T. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers, *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 511-520, Mar. 2003.

[11] H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation", *IEEE Journal of Solid State Circuits*, vol. 38, pp. 1739-1744, Oct. 2003.

[12] X. Fan, C. Mishra, and E. Sánchez-Sinencio, "Single Miller capacitor compensated multistage amplifiers for large capacitive load applications", in *Proc. IEEE International Symposium on Circuits and Systems*, Vancouver, Canada, May 2004, pp. 493-496.

[13] T. T. Y. Wong, *Fundamentals of Distributed Amplification*. Boston: Artech House, 1993.

[14] A. Hajimiri, "Distributed integrated circuits: an alternative approach to high-frequency design", *IEEE Communications Magazine*, vol. 40, pp. 168-173, Feb. 2002.

[15] B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 9, pp. 347-352, Dec. 1974.

[16] E. L. Ginzton, W. R. Hewlett, J. H. Jasberg, and J. D. Noe, "Distributed amplification," *Proc. IRE*, vol. 36, Aug. 1948, pp. 956–969.

[17] W. S. Percival, "Improvements in and relating to thermionic valve circuits," British Patent Specification No. 460,562, 1936.

[18] P. J. Sullivan, B. A. Xavier, and W. H. Ku, "An integrated CMOS distributed amplifier utilizing packaging inductance," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, pp. 1969-1976, Oct. 1997.

[19] B. M. Ballweber, R. Gupta, and D. J. Allstot, "A fully integrated 0.5-5.5 GHz CMOS distributed amplifier", *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 231-239, Feb. 2000.

[20] H. Ahn and D. J. Allstot, "A 0.5-8.5 GHz fully differential CMOS distributed amplifier", *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 985-993, Aug. 2002.

[21] P. F. Chen, R. A. Johnson, M. Wetzel, P. R. de la Houssaye, G. A. Garcia, P. M. Asbeck, and I. Lagnado, "Silicon-on- sapphire MOSFET distributed amplifier with coplanar waveguide matching," 1998 *IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 1998, pp. 161-164.

[22] B. Kleveland, C. H. Diaz, D. Vook, L. Madden, T. H. Lee, and S. S. Wong, "Exploiting CMOS reverse interconnect scaling in multigigahertz amplifier and oscillator design," *IEEE Journal of Solid-State circuits*, vol. 36, pp. 1480-1488, Oct. 2001.

[23] B. M. Frank, A. P. Freundorfer, and Y. M. M. Antar, "Performance of 1-10-GHz traveling wave amplifiers in 0.18-µm CMOS", *IEEE Microwave and Wireless Components Letters*, vol. 12, pp. 327-329, Sep. 2002.

[24] R. Liu, K. Deng, and H. Wang, "A 0.6-22-GHz broadband CMOS distributed amplifier," *2003 IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2003, pp.103-106.

[25] H. Wu and A. Hajimiri, "Silicon-based distributed voltage-controlled oscillators", *IEEE Journal of Solid State Circuits*, vol. 36, pp. 493-502, Mar. 2001.

[26] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully integrated CMOS power amplifier design using the distributed active-transformer architecture", *IEEE Journal of Solid State Circuits*, vol. 37, pp. 371-383, Mar. 2002.

[27] D. M. Pozar, *Microwave Engineering*. 2nd Edition, New York: John Wiley & Sons Inc., 2003.

[28] I. Aoki, "Distributed active transformer for integrated power amplification", Ph.D. dissertation, California Institute of Technology, Pasadena, CA, 2002.

[29] H. Wu, "Signal generation and processing in high-frequency / high-speed silicon-based integrated circuits", Ph.D. dissertation, California Institute of Technology, Pasadena, CA, 2003.

[30] B. Kleveland, “CMOS interconnects beyond 10GHz”, Ph.D. dissertation, Stanford University, Stanford, CA, 2000.

[31] T. Manku, “Microwave CMOS-device physics and design,” *IEEE Journal of Solid State Circuits*, vol. 34, pp. 277-285, Mar. 1999.

[32] C. S. Aitchison, “The intrinsic noise figure of the MESFET distributed amplifier,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, pp. 460-466, Jun. 1985.

[33] J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*. Boston: Artech House, 2003.

[34] G. Gonzalez, *Microwave Transistor Amplifiers-Analysis and Design.* Paramus, New Jersey: Prentice Hall, 1997.

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