MULTI-PHYSICS INVESTIGATION ON THE FAILURE MECHANISM AND SHORT-TIME SCALE WAVE MOTION IN FLIP-CHIP CONFIGURATION

A Dissertation

by

YOONCHAN OH

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2004

Major Subject: Mechanical Engineering

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ABSTRACT

Multi-Physics Investigation on the Failure Mechanism and Short-Time Scale
Wave Motion in Flip-Chip Configuration. (August 2004)
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The demands for higher clock speeds and larger current magnitude in high-performance flip-chip electronic packaging configurations of small footprint have inevitably raised the concern over rapid thermal transients and large thermal spatial gradients that could severely compromise package performance. Coupled electrical-thermal-mechanical multi-physics were explored to evaluate the concern and to establish the knowledge base necessary for improving flip-chip reliability. It was found that within the first few hundred nanoseconds upon power-on, there were fast attenuating, dispersive shock waves of extremely high frequency propagating in the package. The notions of high cycle fatigue, power density and joint time-frequency analysis were employed to characterize the waves and the various failure modes associated with the moving of these short-lived dynamical disturbances in bulk materials and along interfaces. A qualitative measure for failure was also developed which enables the extent of damages inflicted by short-time wave propagation to be calculated in the probability sense. Failure modes identified in this study are all in agreement with what have been observed in industry. This suggests that micron cracks or interfacial flaws initiated at the short-time scale would be further propagated by the CTE-induced thermal stresses at the long-time scale and result in eventual electrical disruptions.

Although epoxy-based underfills with fillers were shown to be effective in alleviating thermal stresses and improving solder joint fatigue performance in thermal cycling tests of long-time scale, underfill material viscoelasticity was found to be insignificant in attenuating short-time scale wave propagation. On the other hand, the inclusion of Cu interconnecting layers in flip-chips was shown to perform significantly better than Al layers in suppressing short-time scale effects. These results imply that, if improved flip-chip reliability is to be achieved, all packaging constituent materials need to be formulated to have well-defined short-time scale and long-time scale properties. In addition, the results also suggest that the composition and layout of all packaging components be optimized to achieve discouraging or suppressing short-time scale dynamic effects. In summary, results reported herein and numerical procedures developed for the research would not just render higher packaging manufacturing yield, but also bring out significant impact on packaging development, packaging material formulation and micro-circuit layout design.

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Lots of thanks go to all those friends who cared for me and helped me out when I needed them. Pleasant memories with those good friends will last for a long time.

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TABLE OF CONTENTS

CHAPTER Page

LIST OF FIGURES

FIGURE Page

FIGURE Page

FIGURE Page

FIGURE Page

LIST OF TABLES

CHAPTER I

INTRODUCTION

1.1 Overviews

We are in a revolutionizing era in which fast developing semiconductor technology is dramatically changing the way we live. Microelectronic products that are indispensable to our daily lives are enabled by the electronic packaging technology keeping face with semiconductor integration. Microelectronic packaging, which is defined as the "technology of packaging electronic equipment" [1], mainly deals with efficient ways of interconnecting electronic components and the substrates. There are three basic types of microelectronic package according to their connecting type. They are: (1) Wire Bonding, (2) Tape Automated Bonding (TAB) and (3) Flip-Chip. Flip-Chip has rapidly seen wide applications due to its advantages over increased density and better electrical performance. Microelectronic packaging technology is a cross-discipline field integrating physics, chemistry, electrical engineering, computer engineering, chemical engineering, material science and mechanical engineering. The demanding trend for higher level integration, higher clock speed and, at the same time, smaller die size, has created drastic increase in power consumption and heat dissipation in packages. Thus the role of mechanical engineering in heat transfer, thermal management, thermo-mechanical analysis, mechanical integrity and manufacturing is seeing growing significance. Total semiconductor sales were up to $155.35 billion in 2002. The research reported herein is aimed to establish the governing physics essential for improving electronic packaging reliability, so that better quality and higher yield can be achieved. In the following sections, flip-chip

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This dissertation follows the style and format of the Journal of Electronic Packaging.

packages will be briefly described along with the testing procedures for evaluating flip-chip reliability. This is followed by a literature review of relevancy and interest to this research. A description of the research objectives will then conclude this chapter.

1.2 Flip-Chip Technology and Reliability Tests

In the past, the interconnection between silicon (SI) chips and printed circuit boards (PCBs) was through the peripheral wire bonding [2,3] and TAB [4]. A configuration originally invented by IBM in the 1960's incorporating the C-4 (Controlled Collapse Chip Connection) technology [5], flip-chip packaging has been a successful solution to meeting the ever-demanding need for high I/Os, high packaging density, better electrical performance and low cost manufacturability [6-8]. Flip-chip is a configuration where a silicon chip is mounted with its active surface facing the substrate via solder joints [9]. Like many new technologies, flip-chip also has some critical issues, such as a large mismatch in the coefficient of thermal expansion (CTE) between the silicon chip and PCB [10]. Due to this CTE difference, when a package assembly is heated or cooled, solder joints are subjected to large strains and stresses. To ease this problem and improve its performance, applying underfill materials into the gap between the silicon chip and PCB has been a solution practical for reducing CTE mismatch-induced deformations and mechanical straining of the solder joints [10]. In the development and other stages, Finite Element Analysis (FEA) is often employed for estimating thermally induced stresses and strains in electronic packages of complex geometry and various dissimilar materials. FEA helps in understanding and identifying the underlying mechanisms and physics inside a package. There are two procedures frequently performed for testing the reliability of electronic packages: (1) thermal cycling tests and (2) power cycling tests.

1.2.1 Thermal Cycling Tests

In thermal cycling tests, packages are subjected to a temperature cycle defined by a given upper-lower bound and times of ascending/descending and dwelling. The behavior of solder joints undergoing low fatigue cycle, especially plastic and creep deformations, has been the main focus of research [11-14]. Since underfills provide mechanical coupling to reduce the CTE mismatch between silicon chips and substrates, they play an essential role in ensuring overall packaging performance. Thus, the thermal and mechanical properties of underfills have a direct impact on the reliability of flip-chips [6]. An in-depth understanding of underfill materials is therefore essential for optimal design of parameters. The general requirements for underfill materials are high elastic modulus, low CTE, high T_g and high adhesion strength [15-17]. Most underfills are two-phase composites of epoxy-based polymer matrix and filler particles.

Much research has been done for the thermal cycling test, but little has been done on the optimal material parameter design, especially for the underfill. The few available studies [7,8,18,19] were mostly on the uncoupled variations of Young's modulus (assumed linearly elastic) and CTE of the underfill, both out of the need for more realistic prediction for package performances.

1.2.2 Power Cycling Tests

A silicon chip is the brain of a microelectronic package. Modern microelectronic processors can accommodate dozens of millions of transistors in their integrated circuits (ICs). But as the number of transistors embedded in a processor increases, proper heat management has emerged as an urgent issue. Unlike the thermal cycling tests mentioned above which is of long-time scale, power cycling tests mainly deal with short-time scale response of a package. Upon power-on, a semiconductor device dissipates heat and induces a temperature rise. As a result, the silicon chip starts expanding ahead of the solders, underfills and PCB, resulting in considerable stresses in the assembly and possible failures [20]. In power cycling tests, a given power consumption in a silicon chip is usually assumed and a transient heat transfer analysis is implemented, followed by a coupled thermal-mechanical analysis. The response of the package upon power-on is of main focus of the research [13,21-24]. Power cycling tests are conducted for silicon dies that dissipate significant amount of heat upon power-on in real-world applications.

Until now, not much attention has been paid to power cycling tests as has been paid to thermal cycling tests. However, recent developments demanding drastic increase in package power consumption and heat dissipation have rendered large transient thermal gradients upon each power-on inevitable. This rapid thermal transient at short-time scale suggests that dynamic thermal-mechanical phenomena in packages need to be fully understood and the associated failure mechanisms be identified for improved microelectronic reliability. Unlike the long-time thermal cycling tests, power cycling tests deal with short-time scale response. Considering ICs being made of 0.13μm feature line width or less, current power cycling tests need to be re-evaluated and redefined to realize the thermally induced dynamic response of a package that is of the sub-microsecond scale. A more realistic method capable of appreciating the response of each microelectronic component in a very short-time scale is urgent for evaluating the reliability of high performance packages. To address the need, this dissertation presents an approach incorporating simultaneous electrical-thermo-mechanical studies to the understanding of short-time scale dynamic effects on packaging reliability.

1.3 Transient Analysis of Electronic Packages

Other than the thermal cycling and power cycling tests, the response of an electronic package subject to rapid power consumption needs to be investigated. This would impact not only the long-time scale response, but also the short-time scale response. As manufacturing, assembly or duty cycles can lead to temperature variations having a negative effect on package structure and functionality, the transient thermal response of a package is a critical issue. Large temperature gradients pose serious limitations on manufacturing and assembly processes. Understanding of package thermal behavior is critical for accurate prediction of the general mechanical performance of a package under certain constraints and conditions. The assembly and manufacturing conditions should be such that the temperature gradient inside the package and its evolution in time are not detrimentally high. Electronic packages experience large temperature excursions during their fabrication and under operational conditions. Inherent to electronic packages is the presence of geometric and material discontinuities. Discontinuities are critical locations for failure initiation due to heat flux singularities and large thermo-mechanical stresses. Thus determination of heat fluxes and temperature fields is essential in transient thermo-mechanical stress analysis.

Transient thermal behaviors of an electronic package under different operational conditions were observed by Y.J. Min et al [25]. Transient response of a 2-layer semi-infinite structure subject to an embedded heat source was investigated. By applying rectangular heat source of various sizes on the top surface of a Si chip, it was found that the temperature had a singularity at the center of the heat source. While the slope of thermal response at the heat source approaches infinity regardless of the heat source size, they concluded that a single parallel RC circuit charged by a step current source could not represent the transient thermal response. Instead, it should be represented by parallel RC circuits connected in series. This transient thermal study is particularly valuable for the analysis and design of devices that are to operate under pulses of high peak power.

Sherif et al. [26] derived a 1-D analytical model using thermal resistance and applied asymptotic solutions to predict how thermal gradients across solder interconnections evolve during power-on. The transient strain is predominantly due to thermal gradients between the chip and the substrate, and the fatigue life of solders is affected by not only steady-state strains, but also transient strains. This provides a better understanding of how thermal gradients evolve. They also concluded that the magnitude of the thermal strains during power-on transient could be several times higher than the steady-state strains.

Liu et al. [27] used resistor-capacitor (RC) network to model the thermal response of IC packages for accurate measurement and simulation of the thermal performance of IC packages. This electrical analysis of thermal network was then used to predict junction temperatures. As numerical solutions of thermal fields are computationally intensive, they employed a circuit simulation concept of asymptotic waveform evaluation (AWE) for the efficient transient analysis of lumped and distributed networks, which has high CPU efficiency in handling large size networks. By extending AWE to the solution of thermal equations at the PCB level, they determined the time-dependent temperature profiles. Using AWE and conventional thermal network method incorporating a forward finite-difference scheme, they compared the simulation of a given electronic packaging with two three-layer chips mounted on the top a two-layer circuit board. Some transient temperature profiles inside the package were obtained.

Ben Chambers et al. [28] studied the steady state and transient maximum allowable power consumption in chip scale packages (CSP). Using variables including die size, addition of thermal vias and thermal bumps, free and natural convection boundary condition, PCB thermal conductivity, PCB heat loading and addition of a heat sink, the maximum power consumption of a fixed junction was investigated. For transient analysis, their investigation showed that when a chip scale package of 2 Watts steady state power is subjected to 1000 Watts for about 1 ms, junction temperature was seen to rise 50°C.

Mercado et al. [29] did an integrated transient thermal and mechanical analysis for a molded plastic ball grid array (PBGA) package subject to thermal shock. They used computational fluid dynamics (CFD) to obtain the thermal boundary conditions surrounding the package during thermal shock. Heat transfer coefficients thus obtained were incorporated into the coupled heat transfer and thermal stress analysis. They verified that high stresses occur in the die in the transient thermal shock period and that they cannot be captured by isothermal assumption. Dominant stresses within the die at the initial stage shifted from tensile to compressive as time increased. Large temperature gradients existed within the package before steady state was reached. This is why an accurate time-dependent temperature distribution has to be determined in the package.

Chiriac and Lee [30] performed transient thermal simulations to analyze thermal responses of a package undergoing assembly procedure. Anisotropic conductive films (ACFs) were employed to provide insight of the package's thermal behavior. Using CFD, they found that during the initial ramping stage, the die first experienced a small temperature drop of less than 5°C due to cooling effect of the ACF and relatively large heat capacity of the substrate. Afterwards the die began to heat up in less than 20 ms. The manufacturing process induced large temperature gradients inside the substrate, while it induced small temperature changes in the anisotropic film.

D. Fedasyuk [31] developed a new mathematical method for the description of transient thermal conduction in flip-chip configurations. The thermal model was based on the formalization and analytical solution of a conjugate transient heat exchange problem for the die and substrate. Since one of the key issues in flip-chip design is to provide temperature field analysis and heat removal in three-dimensional structures, developing mathematical methods for the description of transient thermal conduction in these structures is of great importance.

R. Mandal [32] performed experimental and numerical transient thermal studies on an IC package to predict real time thermal responses. Power input into the IC package varied with time depending on the type of function it performed during each instance. The ability to successfully simulate a transient thermal event has been helpful in understanding the thermal response of an IC package. This real time response is particularly useful in determining a proper thermal management scheme for electrical testing and operational life. In the study, the applied heat source on the die was modeled as a planer source uniformly dissipating heat and located at the center (mid plane) of the die assuming that thermal resistor is uniformly distributed within the test die -- a scenario not true with dies in real operational situation.

Guven et al. [33] proposed a novel hybrid boundary element-finite element algorithm for the investigation of transient thermal response of electronic packages consisting of dissimilar materials. The boundary conditions along the interfaces between BEM and FEM regions were matched by satisfying temperature continuity and energy balance. They simulated the cooling stage from a fabrication temperature to an ambient temperature of a typical die, die-attach, and substrate system, and found that the temperature profile along the substrate/die-attach interface exhibited oscillatory behavior in the vicinity of the edge of the die-attach. In addition, to satisfy the convective heat loss condition along with a very low die-attach thermal conductivity, a high temperature gradient was required.

To capture main transient phenomena in electro-thermal simulation of power electronic circuits subject to short power pulse excitation, Ammous et al. [34] proposed a dynamic thermal model of discrete semiconductor packages using experimentally measured transient thermal impedance responses. An equivalent thermal model was built using a step transient thermal impedance curve. The proposed thermal model gave accurate thermal responses when the dissipated power duration was in the range of a few microseconds. (Thermal impedance is a function of the peak value, the duration and the duty cycle of the dissipated heat.) When the duration of the power impulse was short, the evolution of the thermal impedance curves was very sensitive to duty cycle variation and the temperature gradient inside the package became large, especially in the silicon die. When the magnitude of the dissipated heat was very high, such as in the case of a large power surge of short durations, the peak temperature increased rapidly and a high temperature gradient was generated inside the die. Since the purpose was to model the electro-thermal couplings inside a power semiconductor device, a one-dimensional heat flow model for the die and other layers was assumed in their modeling. This leaves an opportunity for improvement since mapping of temperatures inside the package was not realized.

In summary, there exists a large transient thermal gradient inside an electronic package within a very short time window while undergoing manufacturing, assembly stage, or operation. When this is combined with drastic power increase in packages of small sizes, the impact on the reliability and integrity of the package can be detrimental.

1.4 Research Objectives

The primary objective of the research is to establish the underlying physics governing the short-time responses of a flip-chip package subject to rapid thermal gradients induced electrical heating. Realization of the objective will help identify failure mechanisms that render low packaging reliability. In addition, suggestions feasible for optimal packaging materials having desired long-time and short-time characteristics will be provided. Considering the ever-increasing market demand for improved technology and shorter product development cycle, knowledge gained for optimal material parameter design would be valuable for both product development and post-failure evaluation.

Since it has been identified that there are large transient thermal gradients from high heat dissipation, the two-fold focus of the research is to develop an improved power cycling test method using a coupled electrical-thermal-mechanical analysis to capture the rapid thermal transient response and to investigate how heat is generated and propagates within a package. As thermally induced dynamic events are expected to rise up shortly after power-on, the time window of the analysis will be of sub-microsecond scale. Thus, heat-generated propagating stress waves of short-time scale will be the focus of the research. The corresponding failure mechanisms attributable to thermal-mechanical transients will also be investigated. The investigation will provide a better understanding of the underlying physics governing the responses of a high-performance flip-chip configuration subject to rapid thermal-mechanical transients. Knowledge base established in the research can be the guideline for developing new types of packaging materials that would aid in attaining higher packaging reliability.

1.5 Dissertation Outline

It has been identified why there is an urgent need for improved electronic packaging reliability and what objectives are to be achieved to address this need. The organization of the remaining chapters is as follows. In Chapter II, a detailed analysis procedure will be presented for the optimal packaging material properties for the long-time scale thermal cycling tests. An improved, transient power cycling analysis will be fully described in Chapter III, in which the modeling procedure, presence of large transient thermal gradients and the resulting propagating stress waves are addressed in detail. In Chapter IV, the interpretation of the generated stress waves will be investigated employing the notions of high cycle fatigue analysis and power density. The failure mechanisms associated with this short-time scale effect will also be identified. In Chapter V, underfill material optimization will be treated for various elastic, viscoelastic material properties and the effect of different filler contents on the performance of the underfill materials will be discussed. With the trend of Al material being replaced by Cu material in electronic packaging, a comparison of short-time scale effect between Al layer and Cu layer will be covered in Chapter VI. Lastly, Chapter VII will summarize this dissertation with conclusions and suggestions for future work.

CHAPTER II

OPTIMAL MATERIAL PROPERTIES AT LONG-TIME SCALE

2.1 Accelerated Thermal Cycling Test for Flip-Chip

As previously mentioned, much research has been done for the thermal cycling tests, but little has been done on the optimal material parameter design, especially for the underfills. The few studies documented were mostly on the uncoupled variations of Young's modulus (assumed linearly elastic) and the CTE of underfills. Underfill materials are often combinations of epoxy and fillers. Usually fillers have a higher thermal conductivity and stiffness (E), and a comparatively lower CTE than that of the epoxy. If the effective material properties of a filler particle-added epoxy composite material are available, FEA on the epoxy resin of a given filler content can then be conducted. It is known that the CTE of underfills need to be closely matched to that of the solder joints (21 ppm/^{o}C). As both the E and CTE are essential in the performance of the underfill, the way stresses are redistributed subjected to various E's and CTE's and under thermal-cycling influence can be investigated using FEA. The optimal material parameter design is performed with available epoxy matrix and filler particles combinations, where various material properties including E, CTE, Poisson's ratio, thermal conductivity and density all vary with the specific filler contents in the epoxy matrix.

To appreciate the effect of various underfill materials with different thermal, mechanical material properties, a flip-chip model is constructed for a thermal cycling simulation. This allows the fatigue life of solder joints as a direct measurement of electronic package's performance. The 2-D flip-chip configuration is shown in Fig. 2.1 [35] and the corresponding FEA model is in Fig. 2.2. Only half of the configuration is modeled due to its geometrical symmetry and eight-node plane strain elements are used.

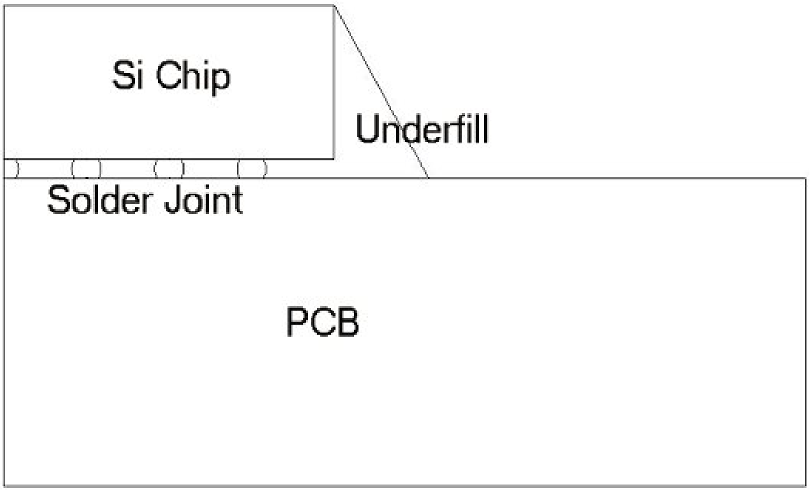


Fig. 2.1 Flip-Chip configuration

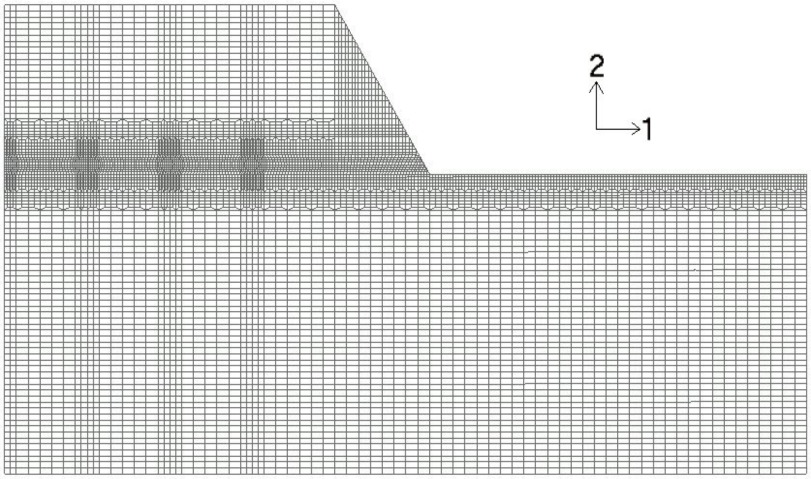


Fig. 2.2 FEA model of flip-chip

The symmetric line is restrained in the 1-direction, while the bottom is constrained in the 2-direction. The dimensions for the configuration can be found in Table 2.1, while the associated material properties are given in Table 2.2 [35]. The solder is 63Sn/37Pb eutectic having a temperature-dependent yield strength of Y(MPa) = 22.71-0.097*T(°C) [36]. To realize the creep behavior of 63Sn/37Pb, the following hyperbolic sine law was adopted from [37]:

$$\dot{\varepsilon}_{cr} = A(\sinh B\sigma)^n \exp(-\frac{\Delta H}{RT}) \tag{2-1}$$

where A=12423(1/sec), B=1.26E-7(1/Pa), n=1.89, activation energy ΔH=61417(J/mol) and gas constant R = 8.314(J/mol·K).

To investigate the effect of underfill material properties on the performance of the flip-chip, a parametric study for different underfill material properties is performed. Since E and CTE are dominating factors, E is varied from 3 to 12 GPa with a 3 GPa difference; while CTE is varied from 10 to 40 ppm/°C with a 5 ppm/°C difference. (See Table 2.2) For this configuration and varying underfill material properties, a thermal cycling load is applied as in Fig. 2.3. By conducting coupled thermo-mechanical analysis, the behavior of each component, especially the solder joints, is carefully observed. For the 63Sn/37Pb eutectic solder joints, the saturated total inelastic strain range is taken as the sum of the saturated plastic and creep strain range. This total inelastic strain range can be used as an input to predict the mean (50%) fatigue life of the solder joints using the method developed by Mukai et al [38]:

$$N_f = 0.146(\Delta\varepsilon_{in})^{-1.94} \tag{2-2}$$

where $\Delta\varepsilon_{in} = \Delta\varepsilon_{pl} + \Delta\varepsilon_{cr}$ per each thermal cycle.

Table 2.1 Description of flip-chip components

Material	Size
Si Chip	1.2 mm x 0.5 mm
Solder (63Sn/37Pb)	64μm standoff height, 0.3mm pitch
PCB	2.913 mm x 1.0 mm

Table 2.2 Material properties of flip-chip components

Component	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/^{o}C)
Si Chip	131	0.3	2.8
Solder (63Sn/37Pb)	32-0.088*T(^{o}C)	0.4	21
Underfill	3/6/9/12	0.35	10~40
PCB	22	0.28	18

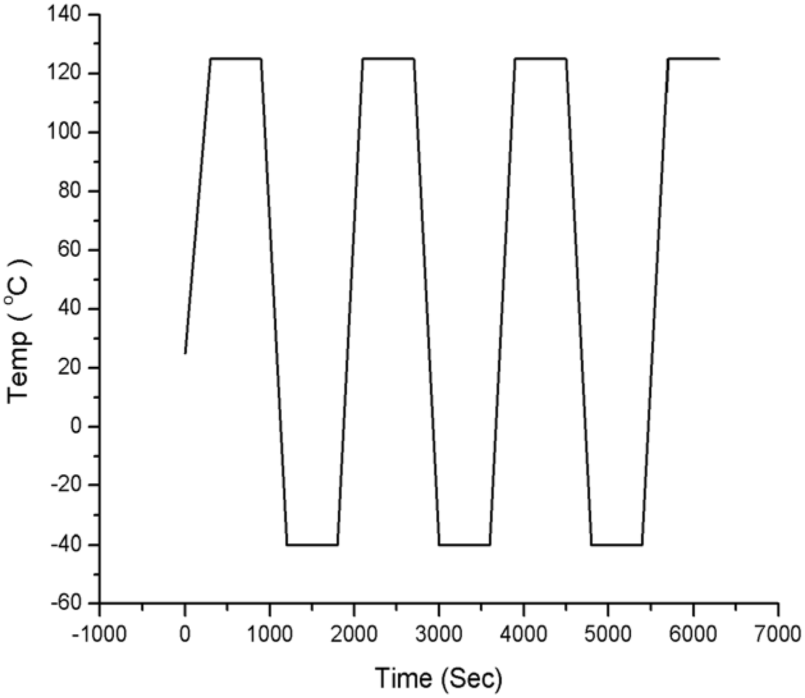


Fig. 2.3 Thermal cycling temperature profile

The calculated saturated inelastic strain range and the corresponding predicted fatigue lives are plotted in Figs. 2.4 to 2.5 as functions of E and CTE. As distinctly noticed in Fig. 2.5, CTE shifts to a lower value as E increases and there exists an optimal CTE value for a given E. Various techniques have been developed to modify the material properties of underfills. By having this insight of optimized property combination, material characterization for high performance electronic packaging can be realized.

2.2 Flip-Chip Fatigue Life Subject to Underfills with Filler-Included Epoxy

As shown, the solder fatigue life of a flip-chip can be expressed as a function of E and CTE of underfill materials. Since an underfill is a combination of epoxy and fillers, and fillers usually have a higher E and comparatively lower CTE values, as the content of fillers increases, the effective CTE tends to decrease while the effective E increases. Many formulations have been suggested for the effective material properties of a particle-included composite material with the following best fitting published experimental data [39,40]:

$$K_n = \frac{E_n}{3(1-2\nu_n)} \ , \quad n = 0, 1 \tag{2-3}$$

$$\mu_n = \frac{2E_n}{2(1+\nu_n)} \ , \quad n = 0, 1 \tag{2-4}$$

$$\gamma_0 = \frac{1+V_0}{9(1-V_0)} \tag{2-5}$$

$$\delta_0 = \frac{4-5V_0}{15(1-V_0)} \tag{2-6}$$

$$\overline{K} = K_0 \left\{ 1 + \frac{\phi(K_1 - K_0)}{K_0 + 3\gamma_0(1-\phi)(K_1 - K_0)} \right\} \tag{2-7}$$

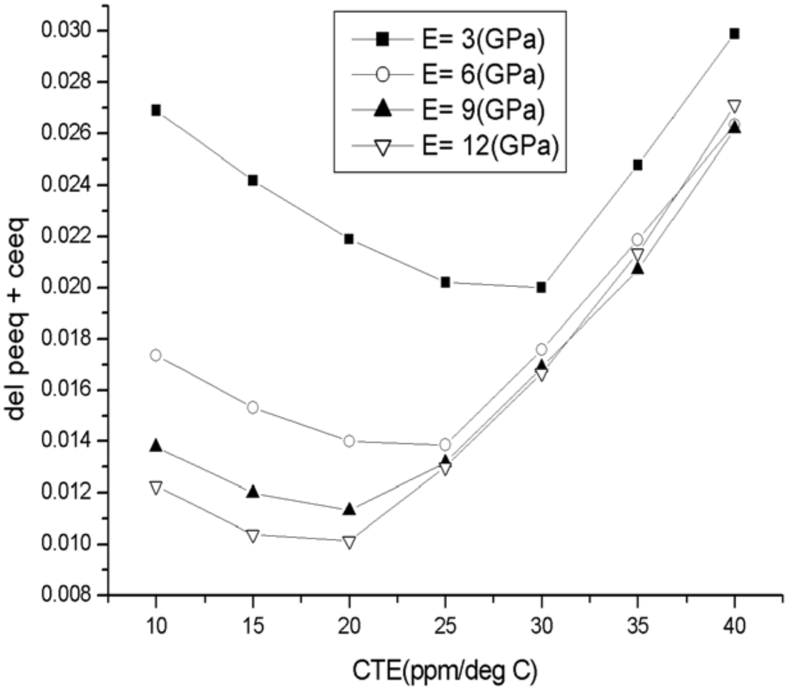


Fig. 2.4 Saturated inelastic strain range as a function of E and CTE

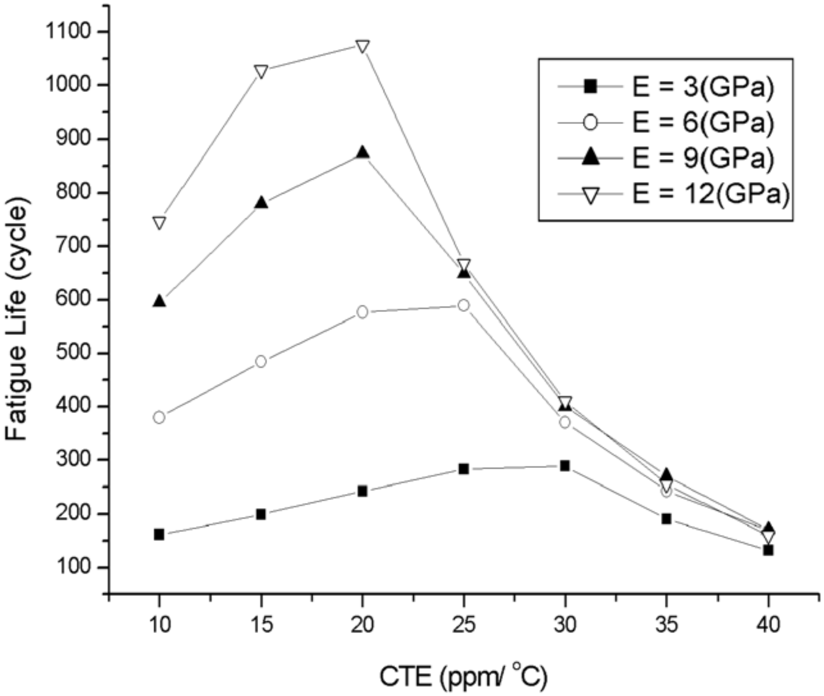


Fig. 2.5 Predicted fatigue life as a function of E and CTE

$$\overline{\mu} = \mu_0 \left\{ 1 + \frac{\phi(\mu_1 - \mu_0)}{\mu_0 + 2\delta_0(1-\phi)(\mu_1 - \mu_0)} \right\} \tag{2-8}$$

$$\overline{E} = 2\overline{\mu} \left\{ 1 + \frac{3\overline{K} - 2\overline{\mu}}{2(3\overline{K} + \overline{\mu})} \right\} \tag{2-9}$$

$$\overline{k} = k_0 \frac{k_1 + 2k_0 + 2\phi(k_1 - k_0)}{k_1 + 2k_0 - \phi(k_1 - k_0)} \tag{2-10}$$

$$\overline{K}' = K_0 + \frac{\phi}{\frac{1}{K_1 - K_0} + \frac{3(1-\phi)}{3K_0 + 4\mu_0}} \tag{2-11}$$

$$\overline{\alpha} = \alpha_0 + \frac{K_1}{\overline{K}'} \frac{(K_0 - \overline{K}')(\alpha_1 - \alpha_0)}{K_0 - K_1} \tag{2-12}$$

where E_0, ν_0, K_0, μ_0, k_0, α_0 are, respectively, Young's modulus, Poison's ratio, bulk modulus, shear modulus, thermal conductivity and CTE of epoxy matrix, while E_1, ν_1, K_1, μ_1, k_1, α_1 are those of the filler particle, ϕ is the volume fraction of the filler, V_0 is the particle size (15 μm), and $\overline{K}$, $\overline{\mu}$, $\overline{E}$, $\overline{k}$, $\overline{\alpha}$ are the corresponding effective moduli and properties of the composite underfill material.

Three different kinds of fillers, silica, SCAN (Silica-Coated Aluminum Nitride) and alumina are incorporated in the study that follows. Material properties along with those of the epoxy are listed in Table 2.3 [39]. The average filler particle size is about 15μm. Using Eqs. 2.3 to 2.12 and the material properties in Table 2.3, the weight percent of the fillers within the epoxy resin is increased from 0% to 90%. The corresponding variations of the thermal conductivity, CTE, and Young's modulus as functions of filler weight percent are given in Figs. 2.6 - 2.8. Using the datum material properties of the underfill system A(silica), B(SCAN), C(alumina) as functions of their individual filler contents, thermal cycling FEA is performed. It should be noted that the applied thermal cycling loads and the material properties, except for the underfills, are the same as the previous sections. Effects of underfill systems with different filler contents are studied in the following.

The obtained saturated inelastic strains are plotted in Fig. 2.9 and the corresponding fatigue lives are given in Fig. 2.10. As can be seen from Fig 2.10, different filler contents of the underfill play a very important role in the performance of the flip-chip. For silica fillers, there exists an optimal 85 weight %. If this content is maintained for this silica filler system, the fatigue life of the flip-chip will be maximized. For SCAN fillers and alumina fillers, the predicted lives increase as the filler contents increase. When the filler contents are relatively low (below 85%), SCAN fillers underfill system performs better than the underfill system with alumina fillers. However, with high filler content around 90%, the reverse is true. Likewise, in the development or other processing and post-failure evaluation stages, to analyze an electronic packaging with complex geometry and various different materials, one would reply on FEA for estimating thermally induced stresses and strains. FEA helps in understanding and identifying the underlying physics in a package.

Manipulating the material properties of all the components involved would lead to a better understanding of the performance of the package configuration. Using FEA, the effects of underfill material properties on the performance of electronic packages can be modeled and studied effectively. Investigated results and conclusions can also be provided to material scientists for further material and processing optimizations.

Table 2.3 Material properties of epoxy and 3 different fillers

Material	Epoxy	Silica	SCAN	Alumina
Thermal Conductivity (W/m-K)	0.195	1.5	220	36
CTE (ppm/^{O}C)	88	0.5	4.4	6.6
Young’s Modulus (GPa)	2.25	73	330	385
Poisson’s Ratio	0.19	0.19	0.25	0.24
Shear Modulus (GPa)	0.8	31	132	155
Bulk Modulus (GPa)	3.75	39	220	247
Density (kg/m^3)	1.1	2.2	3.26	3.98

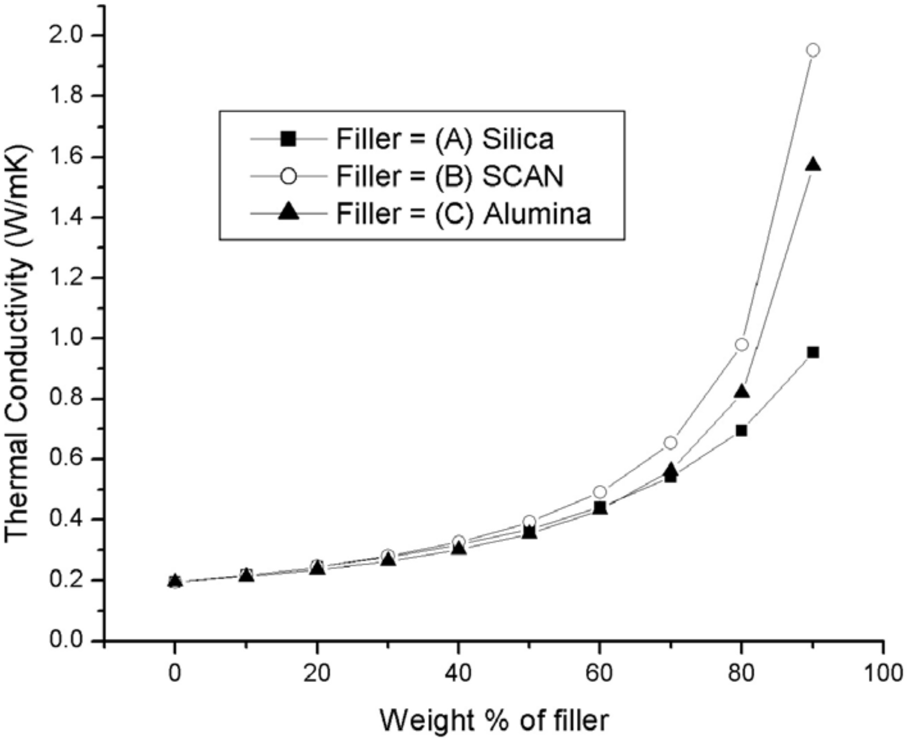


Fig. 2.6 Thermal conductivity of underfill A, B, C
as a function of weight % of filler

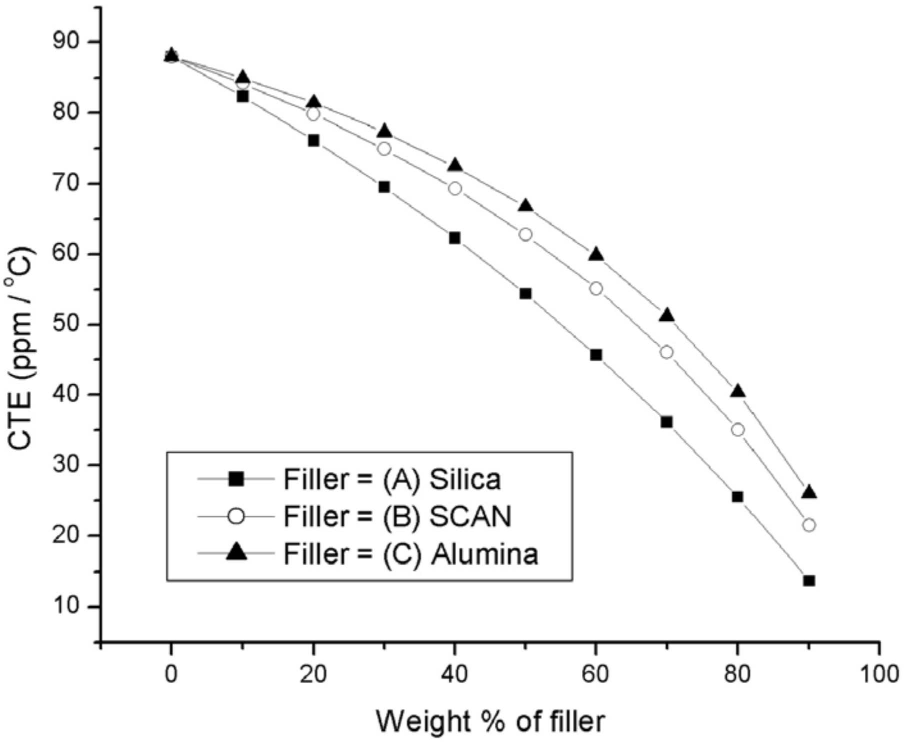


Fig. 2.7 CTE of underfill A, B, C
as a function of weight % of filler

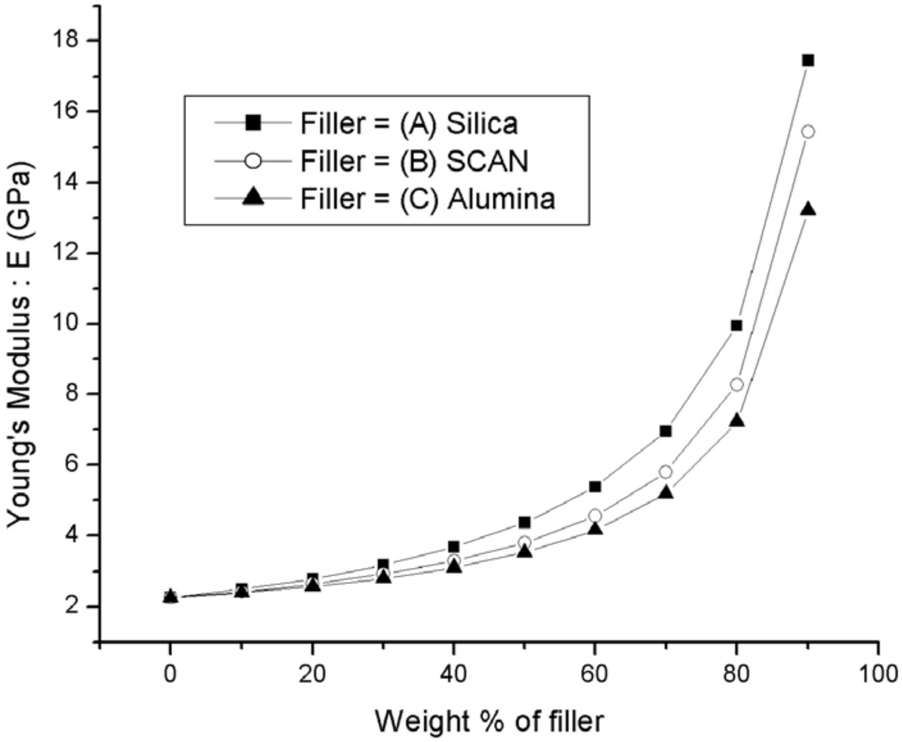


Fig. 2.8 Young's modulus of underfill A, B, C
as a function of weight % of filler

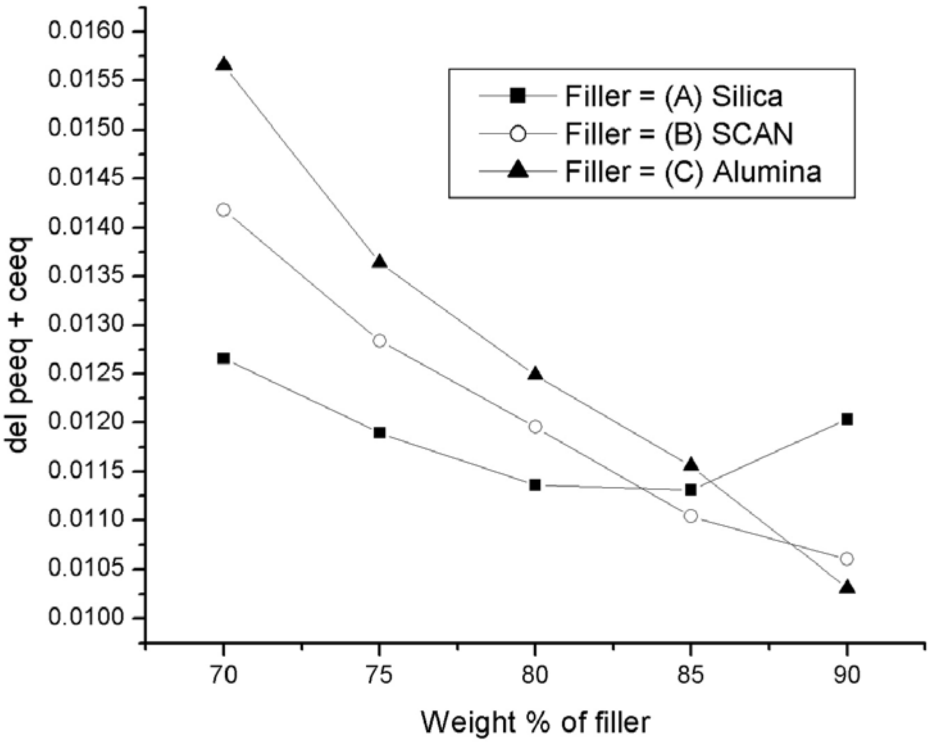


Fig. 2.9 Saturated inelastic strain within solder joint with underfill A, B, C of different filler contents

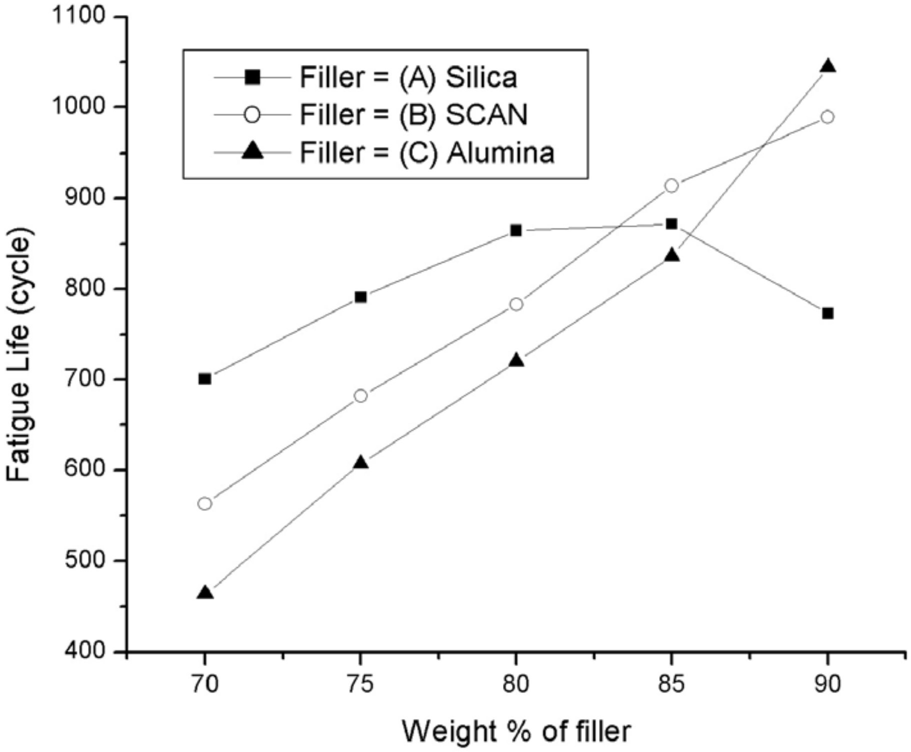


Fig. 2.10 Predicted fatigue life of solder joint
with underfill A, B, C of different filler contents

CHAPTER III

SHORT-TIME SCALE DYNAMIC EFFECT IN FLIP-CHIP CONFIGURATION

3.1 Governing Equations for Electrical, Thermal and Mechanical Fields

The behavior of electronic package in response to electrical current needs to be investigated by considering the coupling of electrical, thermal and mechanical fields simultaneously. In the sections that follow, the governing field equations, which was summarized by Nied and Schlansker [41], are briefly reviewed.

3.1.1 Governing Equation for Electrical Field

Electrical currents flowing through a solid conductor can be expressed in terms of the applied electric potential. Current density, *I*, is a vector and is proportional to the gradient of the electrical potential, *V* as follows

$$I_i = -\frac{V_{,i}}{R} \tag{3-1}$$

where subscript *i* is understood as the spatial index. Eq. (3-1) is the Ohm’s law and R is the specific resistance of the solid through which the current flows. When magnetic effects are neglected, electrical current flow in a solid can be determined from the following equation using the divergence theorem

$$I_{i,\,i} + \dot{\phi} = 0 \tag{3-2}$$

where ϕ is the charge density. Eq. (3-2) can be further simplified, when the time rate of change of this charge density is negligible, as

$$I_{i,\,i} = 0 \tag{3-3}$$

Then Eq. (3-3) can be expressed to have the form

$$(\frac{1}{R}V_{,\,i})_{,\,i}=0 \tag{3-4}$$

When electrical current flows through a conductor of non-zero resistivity, energy is dissipated in the form of heat as governed by the Joule's law

$$\dot{Q}=I_i(I_iR) \tag{3-5}$$

where $\dot{Q}$ is the heat source term due to joule heating.

3.1.2 Governing Equation for Heat Conduction

By the well-known Fourier conduction law, heat flux, q, can be expressed in terms of the temperature gradient as

$$q_i=-kT_{,\,i} \tag{3-6}$$

with k being the thermal conductivity and T the temperature. The heat flow in a conducting solid can be determined from the divergence theorem using

$$-q_{i,\,i}+\dot{Q}=\rho\, C_v\,\dot{T} \tag{3-7}$$

where $\dot{Q}$ is the heat source, ρ is the density and C_v is the specific heat. Note that the heat source $\dot{Q}$ defined in Eq. (3-5) is to be employed in Eq. (3-7) to realize heat conduction induced by joule heating.

3.1.3 Governing Equation for Thermoelasticity

The stress-strain relationship for a solid where thermal expansion exists is governed by

$$\sigma_{ij} = \lambda\varepsilon_{kk}\delta_{ij} + 2\mu\varepsilon_{ij} - \beta\ (T - T_o)\delta_{ij} \tag{3-8}$$

where $\beta = (3\lambda + 2\mu)\alpha$, λ and μ are Lame's constants, α is the coefficient of thermal expansion and T_o is the reference temperature. The strain field is defined in terms of displacement vectors as

$$\varepsilon_{ij} = \frac{1}{2}(u_{i,j} + u_{j,i}) \tag{3-9}$$

The equilibrium equation of motion can be expressed using the spatial gradients of stresses

$$\sigma_{ij,j} + \rho\ f_i = \rho\ddot{u}_i \tag{3-10}$$

When Eqs. (3-8)-(3-10) are considered together, the governing equation for dynamic thermoelasticity [42] can be obtained as follows

$$(\mu\ u_{i,j})_{,j} + ((\lambda + \mu)\ u_{k,k})_{,i} - (\beta\ (T - T_o))_{,i} + \rho\ f_i = \rho\ \ddot{u}_i \tag{3-11}$$

When material properties are independent of temperature, Eq. (3-11) becomes the Navier's equation which can be expressed in terms of displacement components as

$$\mu\ u_{i,jj} + (\lambda + \mu)(u_{k,k})_{,i} - \beta\ (T - T_o)_{,i} + \rho\ f_i = \rho\ \ddot{u}_i \tag{3-12}$$

When the displacement fields are determined, the strain fields can be obtained using Eq. (3-9) and the stress fields using Eq. (3-8).

3.2 Finite Element Formulations for Coupled Electrical, Thermal and Mechanical Fields

The coupled governing equations for the three field variables were briefly reviewed in the previous section. In this section, the corresponding finite element formulations [43] derived from the coupled governing equations, which was summarized by Nied and Schlansker [41], are briefly reviewed.

3.2.1 Electro-Thermal Element

Using the voltage potential V as the primary variable, Eq. (3-1) can be recast into the form with R_{ii} as the resistivity in the i-direction.

$$\frac{1}{R_{xx}}\frac{\partial^2 V}{\partial x^2}+\frac{1}{R_{yy}}\frac{\partial^2 V}{\partial y^2}=0 \tag{3-13}$$

Considering two-dimensional heat conduction only, Eqs. (3-6) and (3-7) can expressed as

$$K_{xx}\frac{\partial^2 T}{\partial x^2}+K_{yy}\frac{\partial^2 T}{\partial y^2}+\dot{Q}=\rho\ C_v\frac{\partial T}{\partial t} \tag{3-14}$$

where K_{ii} is the thermal conductivity in the i-direction and $\dot{Q}$ is the heat source due to joule heating, which is defined using

$$\dot{Q}=\frac{1}{R_{xx}}(\frac{\partial V}{\partial x})^2+\frac{1}{R_{yy}}(\frac{\partial V}{\partial y})^2 \tag{3-15}$$

The thermal and electrical effects can be applied to a single finite element and the nodal temperature and potential of each element therefore can be obtained. Upon applying the finite element method, a set of simultaneous equations can be obtained in the following matrix form

$$\begin{bmatrix} C^t & 0 \\ 0 & 0 \end{bmatrix}\begin{Bmatrix} \dot{T} \\ 0 \end{Bmatrix}+\begin{bmatrix} K^t & 0 \\ 0 & K^v \end{bmatrix}\begin{Bmatrix} T \\ V \end{Bmatrix}=\begin{Bmatrix} \dot{Q} \\ 0 \end{Bmatrix} \tag{3-16}$$

where $\left[C^t\right]$ = specific heat matrix

$\left[K^t\right]$ = thermal conductivity matrix

$\left[K^v\right]$ = electrical conductivity matrix (reciprocal of resistivity)

$\{T\}$ = nodal temperature

$\left\{\dot{T}\right\}$ = nodal temperature change with time

$\{V\}$= nodal potential (voltage)

$\left\{\dot{Q}\right\}$= heat flow into the node due to joule heating

3.2.2 Mechanical Element

The displacement due to a non-homogeneous temperature distribution can be obtained using Eq. (3-11). For a two-dimensional problem, the displacement components u and v, in the x- and y-direction, respectively, are as follows

$$\mu(\frac{\partial^2 u}{\partial x^2}+\frac{\partial^2 u}{\partial y^2})+(\lambda+\mu)\frac{\partial}{\partial x}(\frac{\partial u}{\partial x}+\frac{\partial v}{\partial y})-\beta\frac{\partial T}{\partial x}+\rho\ f_x=\rho\ \ddot{u} \tag{3-17}$$

$$\mu(\frac{\partial^2 v}{\partial x^2}+\frac{\partial^2 v}{\partial y^2})+(\lambda+\mu)\frac{\partial}{\partial y}(\frac{\partial u}{\partial x}+\frac{\partial v}{\partial y})-\beta\frac{\partial T}{\partial y}+\rho\ f_y=\rho\ \ddot{v} \tag{3-18}$$

By applying the finite element theory, Eqs. (3-17) and (3-18) are reduced to a set of simultaneous equations with the nodal displacements, U, as the primary variable.

$$[M]\left\{\ddot{U}\right\}+[K]\ \{U\}=R^t \tag{3-19}$$

where $[M]$= element mass matrix

$\left\{\ddot{U}\right\}$= nodal acceleration vector

$[K]$= element stiffness matrix

$\{U\}$= nodal displacement vector

$\{R^t\}$= element thermal load vector

3.3 Need for Multi-Physics Simulation in Flip-Chip Configuration

The common practice these days for investigating the transient response of an electronic package is to first assume a power input into the Si chip and then follow with conducting a coupled thermo-mechanical analysis to evaluate the induced stresses and strains at a given time. Because knowing the exact locations of large transient thermal gradients is essential to the success of any such analysis, this assumption for a prescribed amount of ‘power input’ into the Si chip falls short of resolving these locations and therefore needs to be re-evaluated. To fully capture the dynamic response of an electronic package subject to rapid thermal transients in the first brief moment after power-on, better realistic methods capable of resolving the response of each component involved in a very short time scale are needed. One solution feasible for addressing this need is to incorporate electrical modeling into thermo-mechanical study. This would allow the dynamic transient thermal field to be generated from transient electrical field, thus rendering the final stress and strain evaluation more exact and close to the real-world situation.

The dynamic thermo-mechanical phenomenon in a package can be investigated by considering transient thermoelastic responses due to local joule heating. Employing the approach of multi-physics involving electrical, thermal and mechanical elements, the associated mechanisms responsible for packaging failure can be identified, thus leading to improved electronic packaging reliability. This is the primary objective of the dissertation. To meet the objective, commercial Finite Element Analysis (FEA) package ABAQUS was chosen to conduct coupled electrical-thermal-mechanical analyses. The nature of multi-physical analysis involving current flows and rapid joule heating requires that a large number of finite elements and very small integration time steps be used. With its highly optimized capacity for handling problems of large DOFs and small time step, ABAQUS would be ideal for these analyses. In sections that follow, a flip-chip finite element model for coupled electrical-thermal-mechanical analysis is described.

3.4 Model Description and Electro–Thermal Analysis

Unlike the formerly mentioned power cycling tests in which an assumed power input was incorporated into the Si chip, a different approach including an electrical model is employed to study the response of a flip-chip subject to power-on. In essence, the notion of coupled electrical-thermal-mechanical excitation is used, thus allowing the localized heat generation to be realized as a result of current flow in the package. This marks the major difference between the proposed approach and the common one using an assumed power input to approximate heat generation.

The main interest is to understand how and where exactly the local heat is generated due to the flow of electrical current. As rapid joule heating is capable of initiating high frequency stress waves, much focus will also be on the generation and propagation of electrical-thermally induced mechanical disturbances in a package. The 2-D model used for the research is a flip-chip configuration as shown in Fig. 3.1 and in Fig. 3.2 [35] as a half model. The dimensions for each component in the configuration are the same as in Table 2.1, except for the addition of a 2μm Al layer and a 10μm Cu layer, whose electrical and thermal material properties are listed in Table 3.1. The current is assumed to flow from the Cu layer through the 2nd solder joint and then the Al layer into the 3rd solder joint and then back to the Cu layer at a different location. In all studies that follow, the underfill and PCB are considered as non-conductors. The current used in the studies is of 0.5A in magnitude with no rise time. The time window within which dynamic responses are observed is from t = 0.0 sec to t = 0. 5 μsec with a constant time step of $\Delta t = 0.5$ nsec.

First, the electrical current density magnitude (ECDM) in response to the 0.5A current flow is shown in Fig. 3.3. Since the Al layer is very thin (2μm in thickness), the current density is seen to be very high in that layer and in a localized corner of the solder joint adjacent to the Al layer. As joule heating is realized as temperature rise subject to the electrical current passing through the Al layer and solder joint, electrostatic analysis would allow resistivity-induced heat dissipation to be modeled as the source of excitation for thermo-mechanical disturbances in the package.

Because temperature increase over the considered time window is extremely small and given the fact that ABAQUS for some unknown reasons could only show two decimal digits for temperature output, temperature increase could not be checked numerically. However, the existence of large transient thermal gradients can be confirmed by heat fluxes of non-negligible magnitudes as seen in Fig. 3.4. The heat fluxes were extracted at the Si-Al-underfill interface right next to the corner of the 3rd solder joint as shown in Fig. 3.3. Besides large magnitude heat fluxes, it was found more heat is conducted from the Al layer to underfill than from the Al layer to Si in the first 75 nsec. Beyond that, most heat is transferred from Al layer to Si.

The amount of increase in temperature is very small with the time span considered. However, since the transient (time taken for this heat-up) is so rapid, the induced response is highly dynamical. Thus the response assumes very different aspects unlike the thermal cycling test. Temperature profiles thus generated within the package are then incorporated to run thermo-mechanical analyses. The resulted mechanical stress variations subject to the action of the coupled electro-thermal field are presented in the following section.

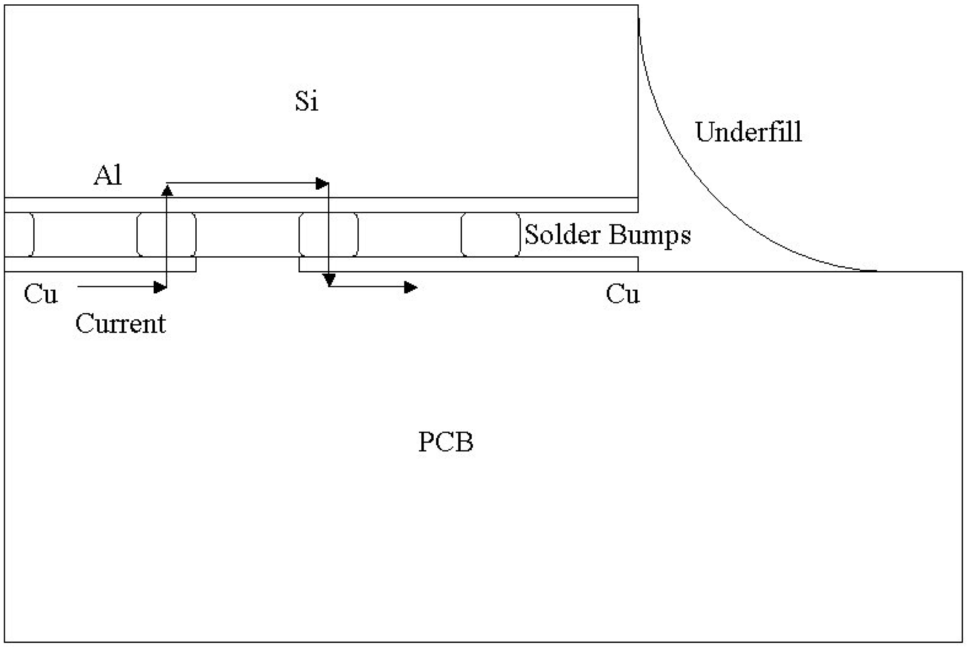


Fig. 3.1 Flip-Chip configuration (not to scale)

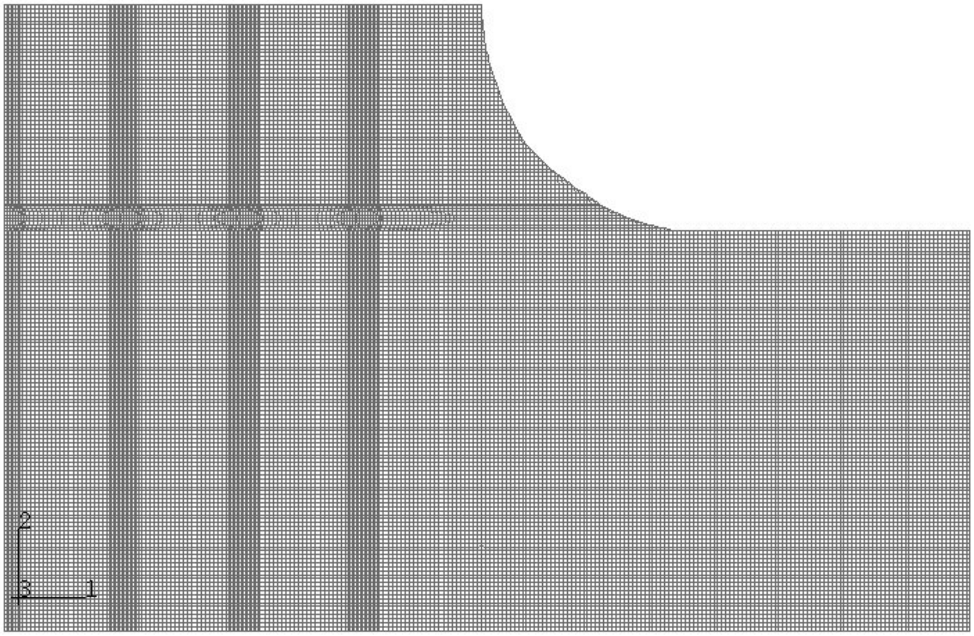


Fig. 3.2 FEA mesh of flip-chip configuration

Table 3.1 Thermal and electrical properties of flip-chip components

Material	Thermal Conductivity (W/m-K)	Electrical Conductivity (mho/m)	Specific Heat (cal/Kg)	Density (kg/m^3)
Si	148	4.348E-4	712	2330
Solder	51	7E+6	151	8470
Al	237	3.745E+7	900	2700
Cu	401	5.977E+7	380	8940
Underfill	1.6	-	674	6080
PCB	13	-	879	1938

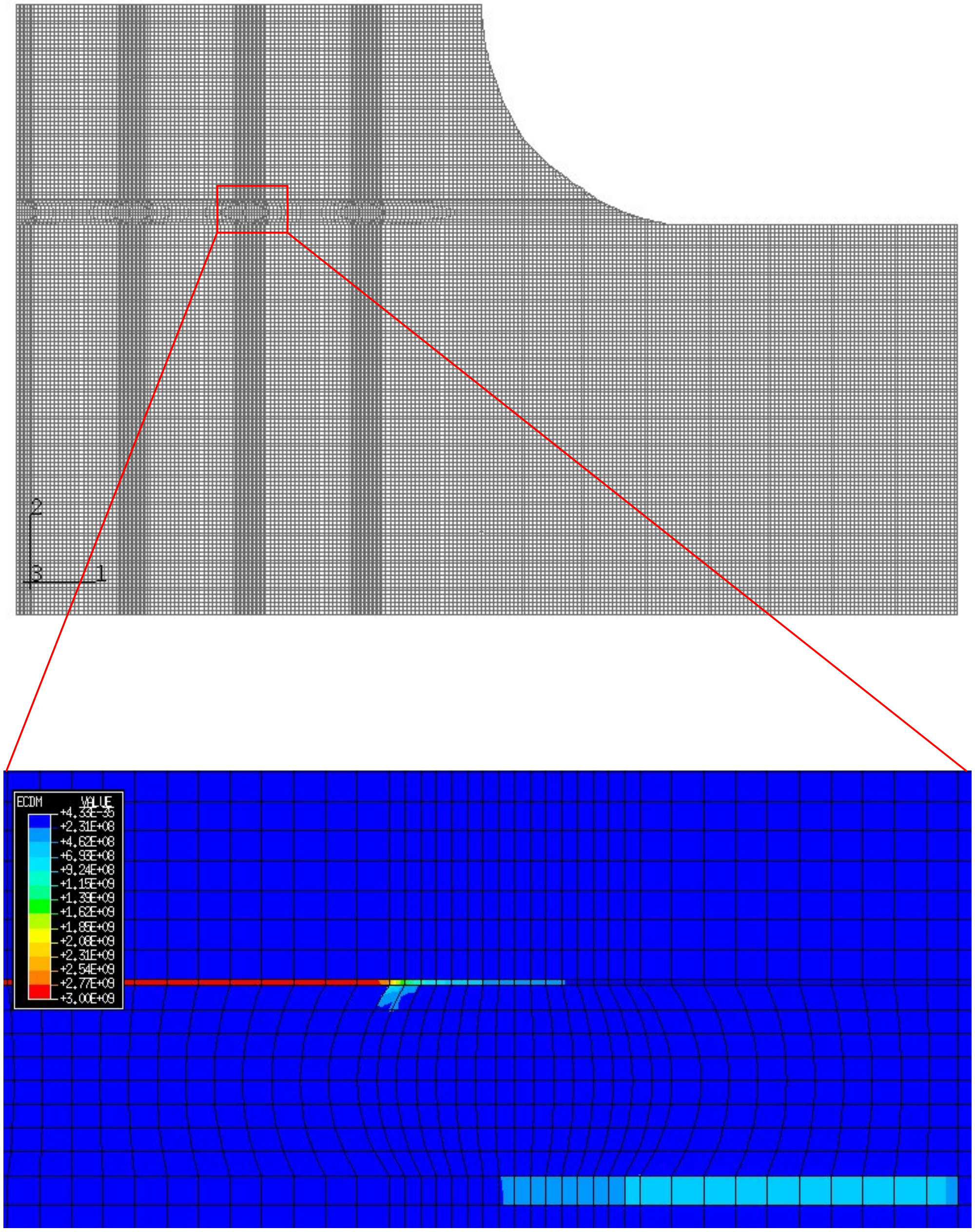


Fig. 3.3 ECDM contour inside flip-chip

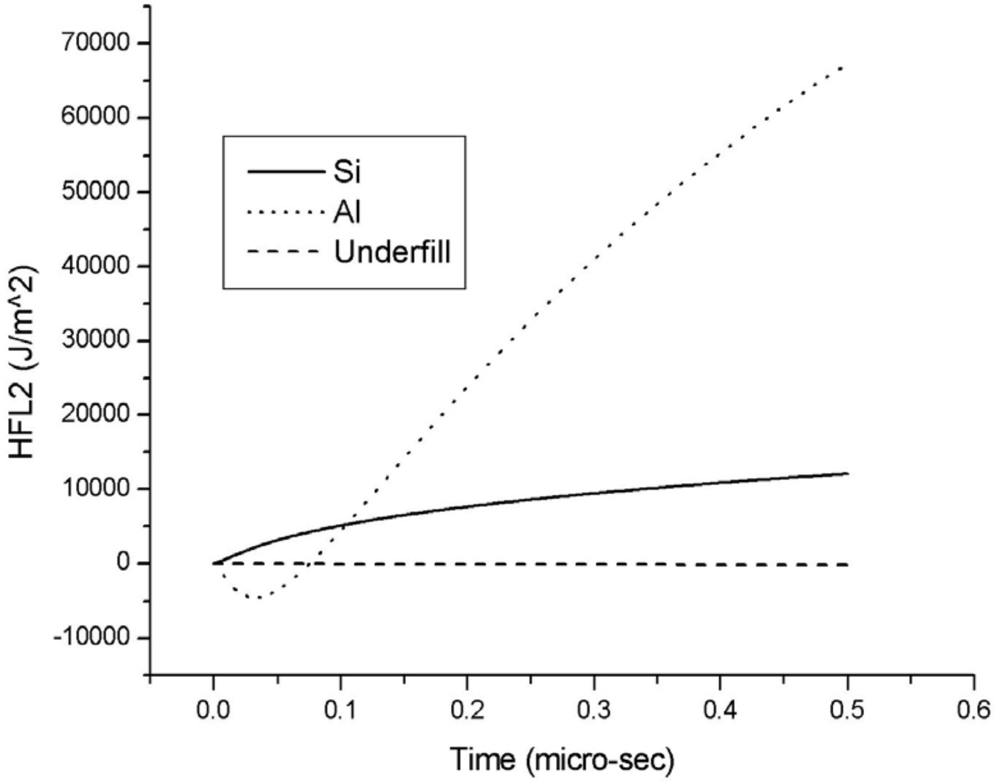


Fig. 3.4 Heat flux in 2-direction at the Si-Al-underfill interface next to the corner of the 3rd solder joint

3.5 Mechanism of Stress Wave Propagation and Model Verification

Thermo-mechanical analysis was performed by incorporating the thermal field output generated through the electrostatic analysis. The boundary conditions for the mechanical analysis are the center of the whole package is constrained in the 1-direction and the bottom of the PCB is constrained in the 2-direction in Fig. 3.2 where a half model is considered due to its innate symmetry. The mechanical properties of the Al and Cu layers are listed in Table 3.2 and all other component properties of the flip-chip are the same as in Table. 2.2.

First, understanding why there are wave propagation phenomena in electronic packages was attempted. The results of the coupled electro-thermal analysis, which are temperature profiles, are the input for the coupled thermo-mechanical stress analysis. Since it has been showed that high ECDM is distributed mainly in the Al layer and the corners of the solder joints under the current path, heat is expected to build up locally around these areas of high ECDM. While other areas remain intact, these regions would undergo relatively large sudden expansion in a very short time, thus acting as the origins of stress waves that propagate in all directions.

Before engaging in full analysis, it is imperative to verify the constructed model. The flip-chip consists of various materials and has complex geometry; nonetheless, by doing a simple calculation, validations can be done as follows. The longitudinal wave propagation speed in a semi-infinite isotropic elastic material can be estimated using $C = \sqrt{E/\rho}$, where E is elastic modulus and ρ is material density. The wave speeds, C, for three different composition materials of the flip-chip package are given in Table 3.3. As the Al and Cu layers are both very thin (2μm and 10μm respectively), they are excluded from the calculation.

Two selected points in the model are examined to determine the arrival times of propagating stress waves. In Fig. 3.5, path 1 is from the origin to the top of the Si and path 2 is from the origin to the bottom of PCB.

Table 3.2 Mechanical properties of Al and Cu layer

Material	Elastic Modulus (GPa)	CTE (ppm/^{o}C)	Poisson's Ratio
Al	70	22.4	0.33
Cu	117	16.8	0.35

Table 3.3 Longitudinal wave propagation speeds in three different materials

Material	Elastic Modulus (GPa)	Density (kg/m^3)	Wave Speed (m/s)
Si	131	2330	7498.2
Underfill	8	6080	1147.1
PCB	22	1938	3369.3

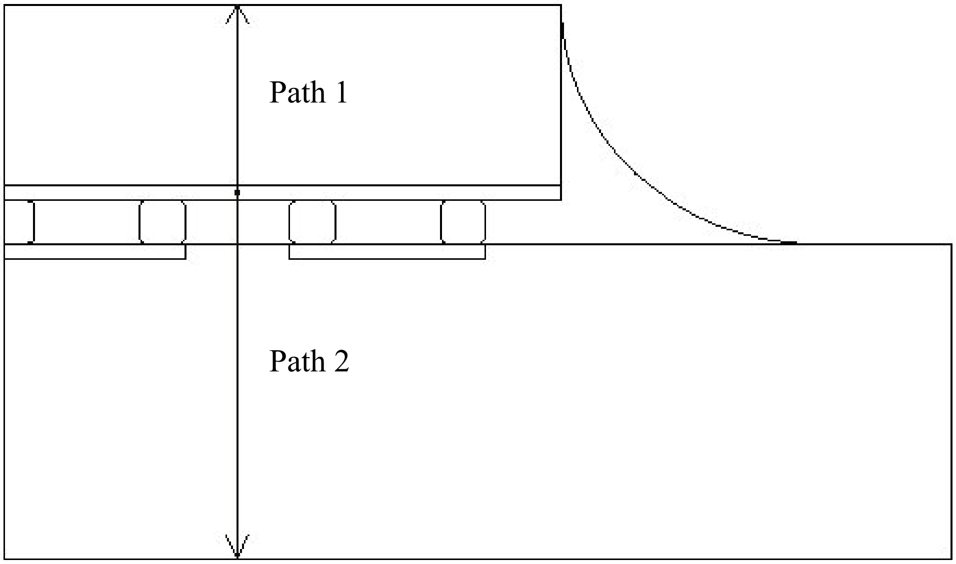


Fig. 3.5 Selected paths of wave propagation (not to scale)

For these two paths, the expected times of arrival for the stress wave propagating along the 2-direction are listed in Table 3.4 and the waveforms from FEA are in Fig 3.6. Numbers found in Table 3.4 are for longitudinal waves propagating in semi-infinite media. Thus discrepancies between the numbers calculated using C = $\sqrt{E/\rho}$ and those from simulations are expected. This is indeed the case for the stress wave acquired along path 2 (S22 wave) where the underfill is not even close to being semi-infinite in dimension. However, the two sets of numbers are in good agreement with each other, thus laying valid foundation for subsequent investigation. It is easily noticed that the magnitudes of these waves are all relatively small. The accumulated plastic strains in solder joints from this short-time scale effect are therefore of zero magnitude. Such is where the power cycling tests differ from the thermal cycling tests. The formerly mentioned power cycling tests (assuming power dissipation into Si chip and including no electrical model) cannot predict the realistic behavior of flip-chip package since it does not appreciate the localized heat build-up and dissipation around the Al layer and the corners of the solder joints. As it is usually the interface that is most affected by wave propagation, stress waveforms at several selected locations (see Fig. 3.7) are also extracted.

The acquired normal and shear stress waveforms, namely S11, S22 and S12 for the whole duration, are shown in Figs. 3.8 to 3.12 (To observe the transient period more closely, the time window is limited to 0.25 μsec). Because ECDM distribution is symmetric about location 1 in Fig. 3.7, the resulting stress waves will assume similar forms (location 1 and 2 are set as where waves are first initiated), thus only the right half is considered in the investigation. These figures show each stress waveform and the time interval for the wave to arrive. Again, the magnitudes of those waves are small, with the observed maximum to be around 400Pa.

Table 3.4 Expected arrival time of wave for 2 paths

Path	L (mm)	C (m/s)	t (nsec)
1 (Si)	0.5	7498.2	66.7
2 (Underfill + PCB)	0.064 / 1	1147.1 / 3369.3	330.9

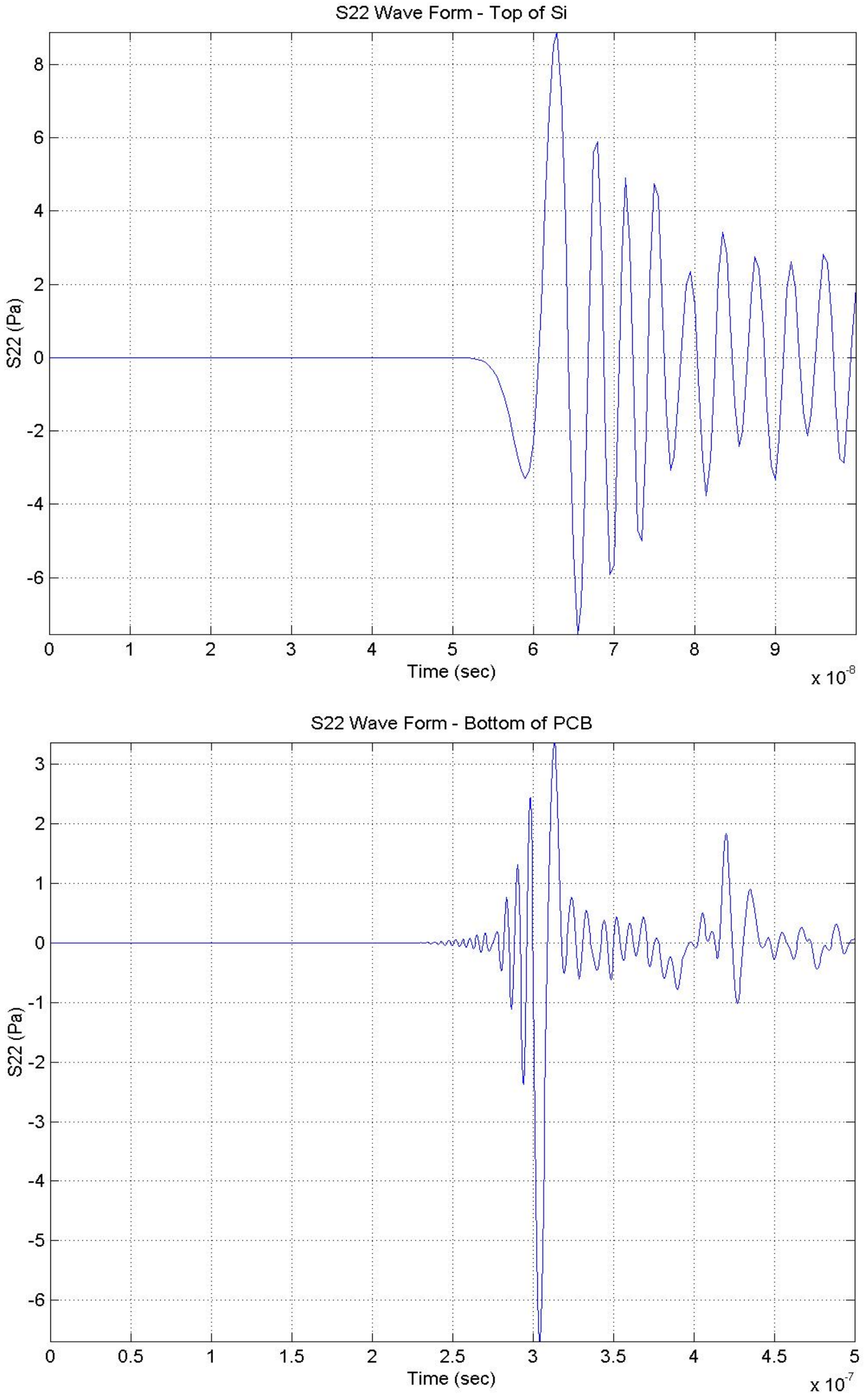


Fig. 3.6 Stress waves acquired at selected locations

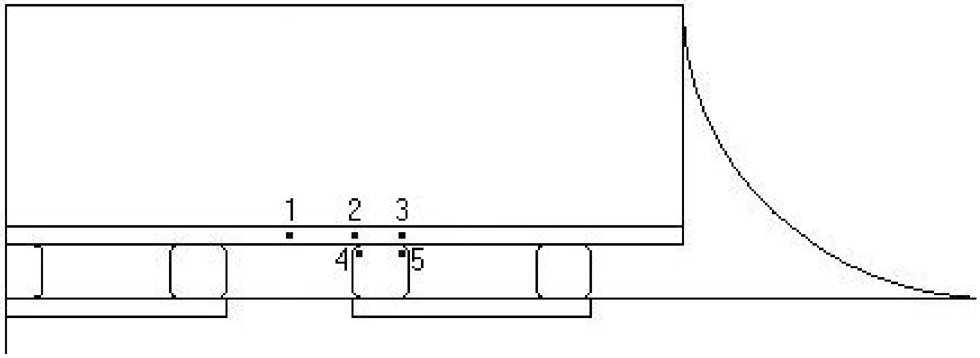


Fig. 3.7 Selected locations in flip-chip for waveform acquisition
(not to scale)

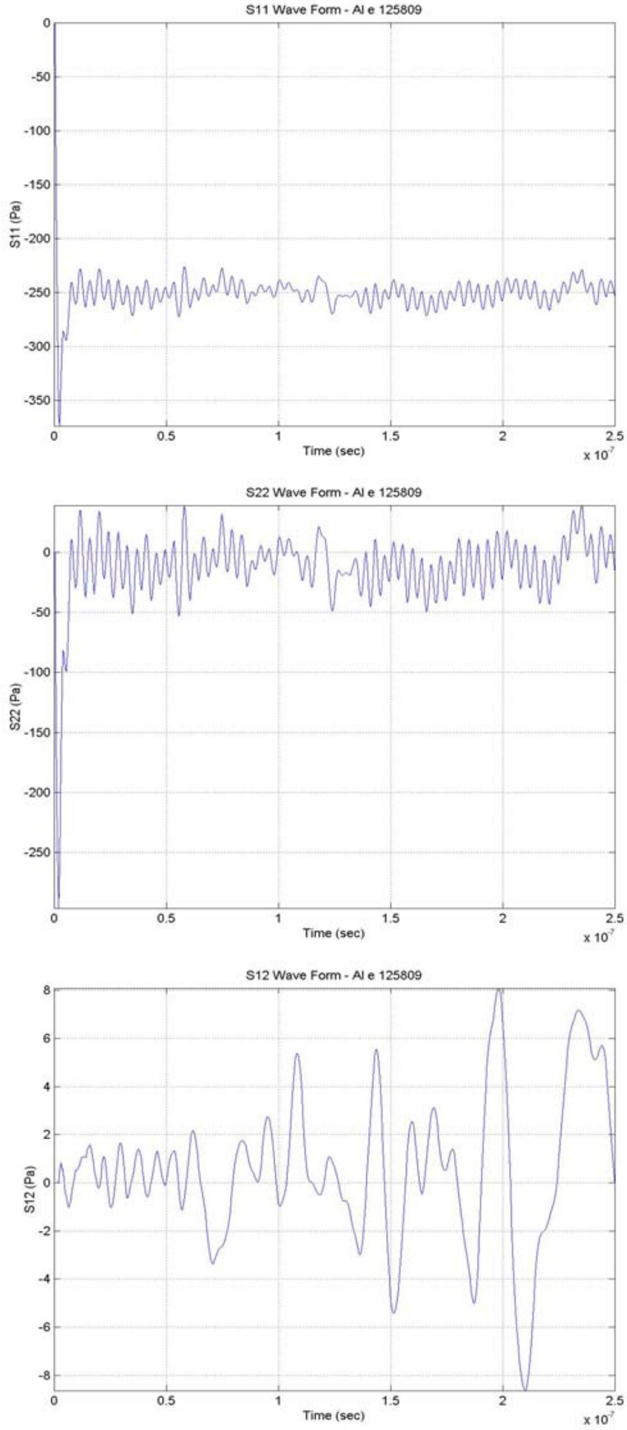


Fig. 3.8 Stress waveforms at Al e 125809 (location 1)

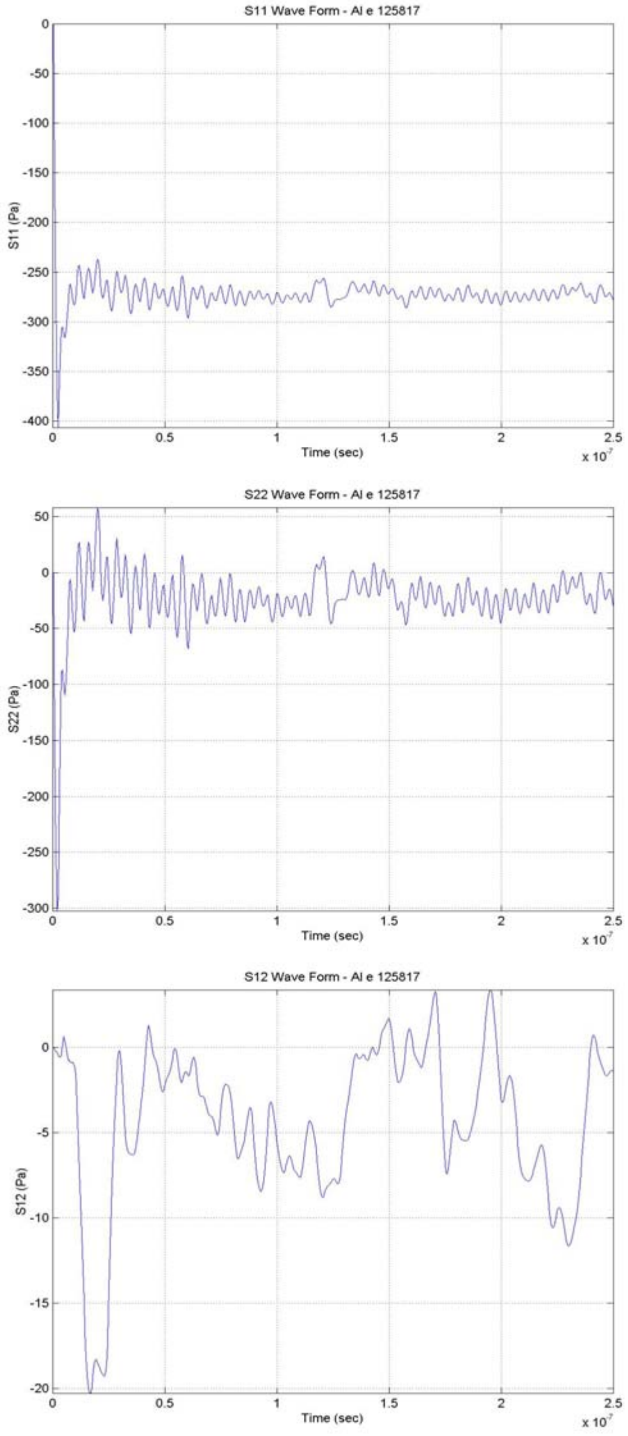


Fig. 3.9 Stress waveforms at Al e 125817 (location 2)

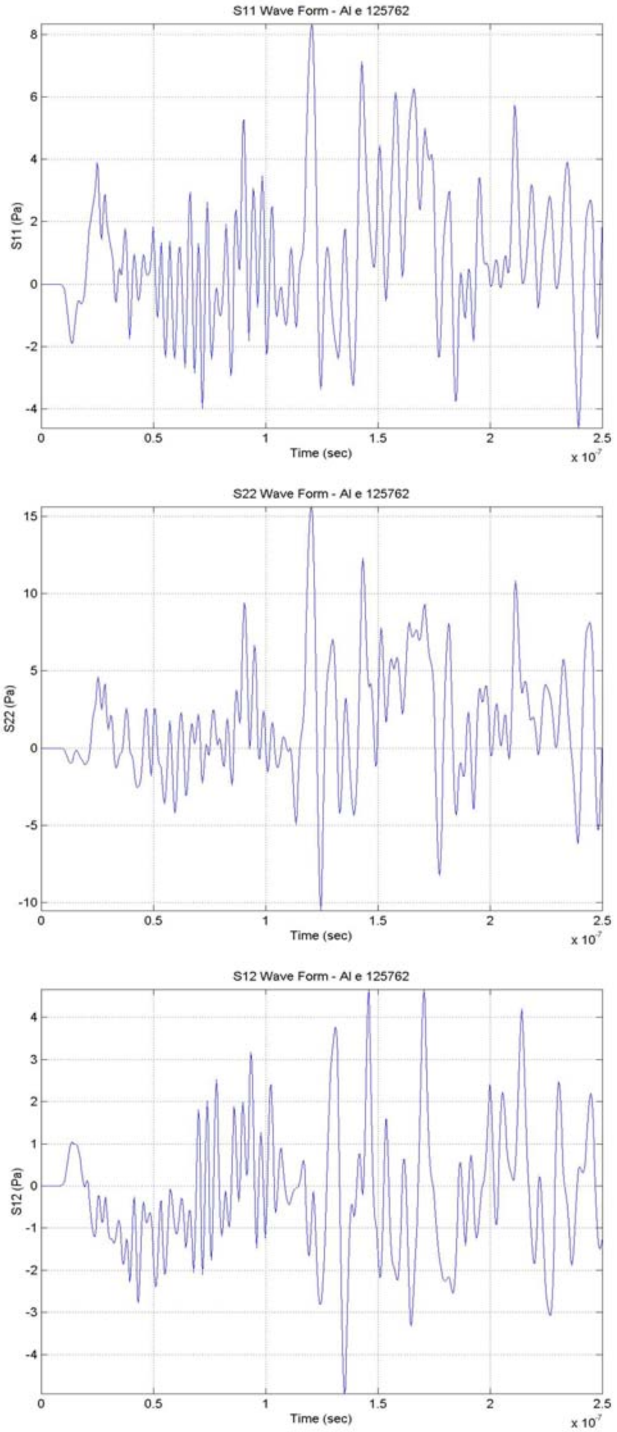


Fig. 3.10 Stress waveforms at Al e 125762 (location 3)

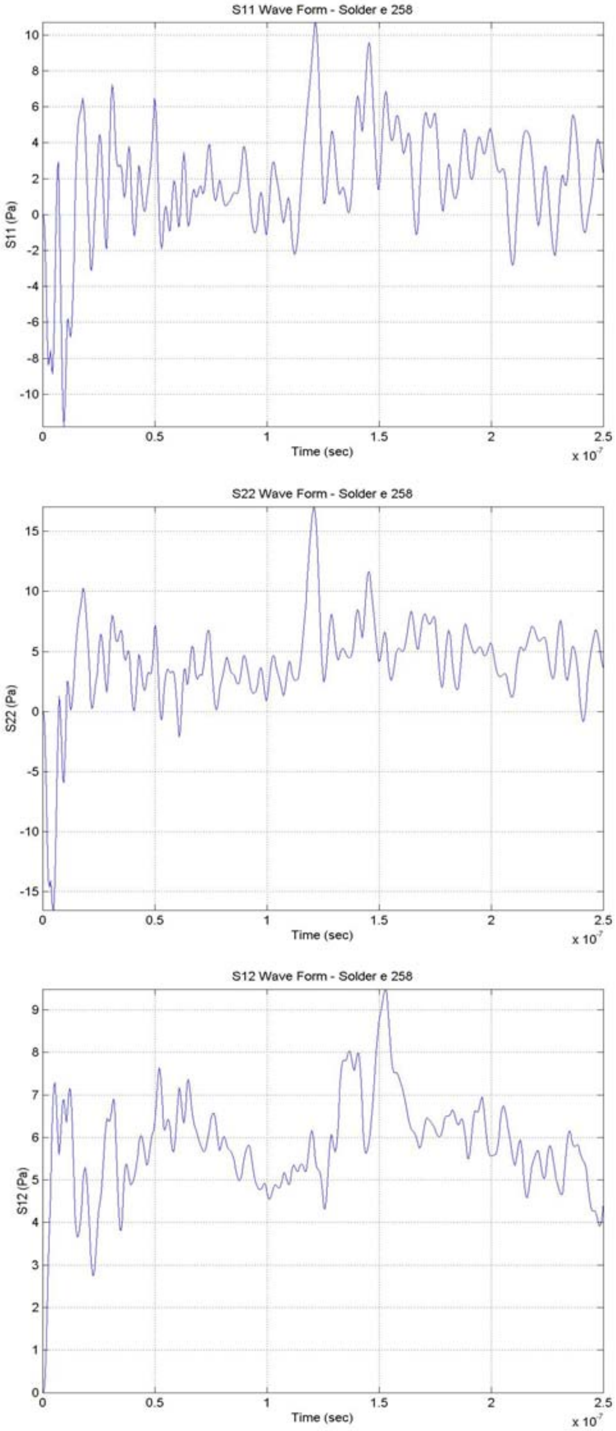


Fig. 3.11 Stress waveforms at solder e 258 (location 4)

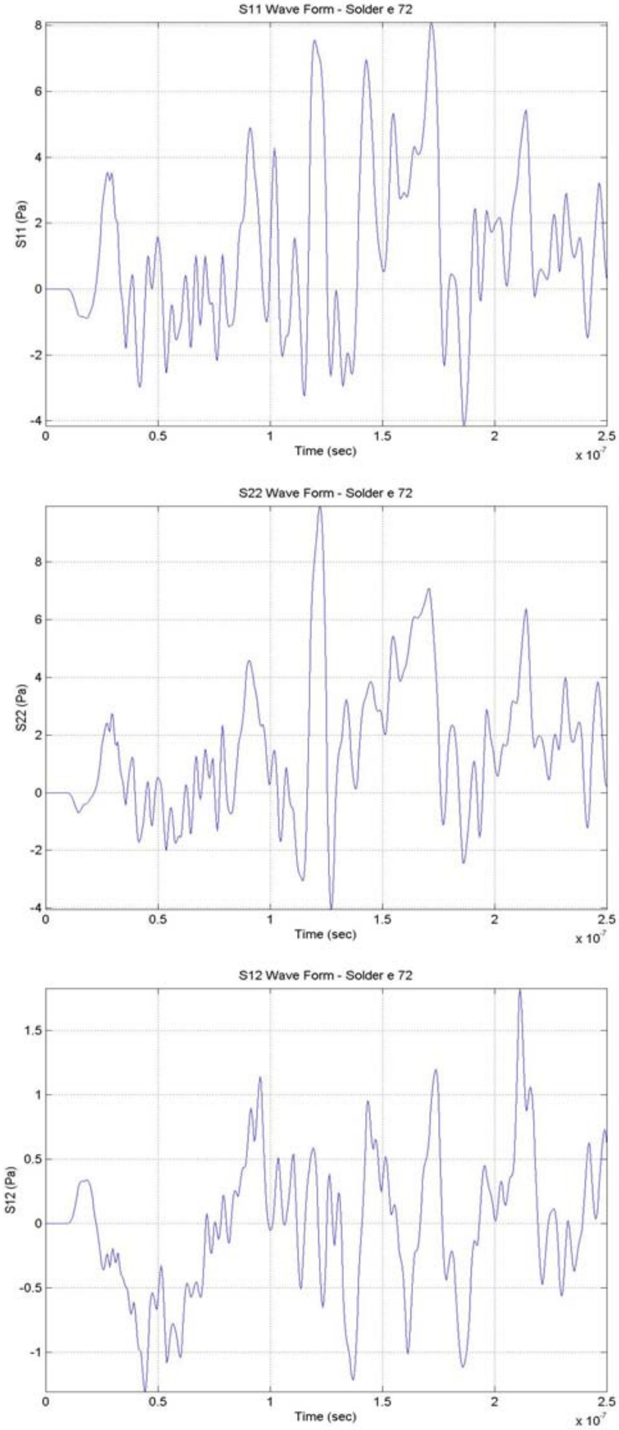


Fig. 3.12 Stress waveforms at solder e 72 (location 5)

In what ways do these low-magnitude stress waves affect the reliability of the flip-chip assembly? Even though the magnitudes are not that high, it should be noted that there is much oscillation along time, especially considering the very short time spent to capture the waveforms. Thus significant insight can be obtained by examining the spectral characteristics of the waves propagating along these locations. Figs. 3.13 - 3.17 give the Discrete Fourier Transform (DFT) results of selected stress waveforms acquired from the same locations as in Figs. 3.8 - 3.12. It is readily seen that the wave spectra are all characteristically broadband and that dominant spectral components are in the high 400MHz range.

It is established that the stress waves due to the rapid electro-thermal transient are of small magnitudes, but with extremely high frequencies as demonstrated above. More information can be obtained when the temporal notion is also considered in the frequency analysis, thus implying time-frequency analysis. The Short-Time Fourier Transform (STFT) is employed to extract joint time-frequency information. To ensure simultaneous good temporal and spectral resolution, a Gaussian window is used in the STFT. Detailed description will follow in Chapter IV, leading eventually to the identification of failure mechanisms prominent in the short-time window that is of a few hundred nanoseconds.

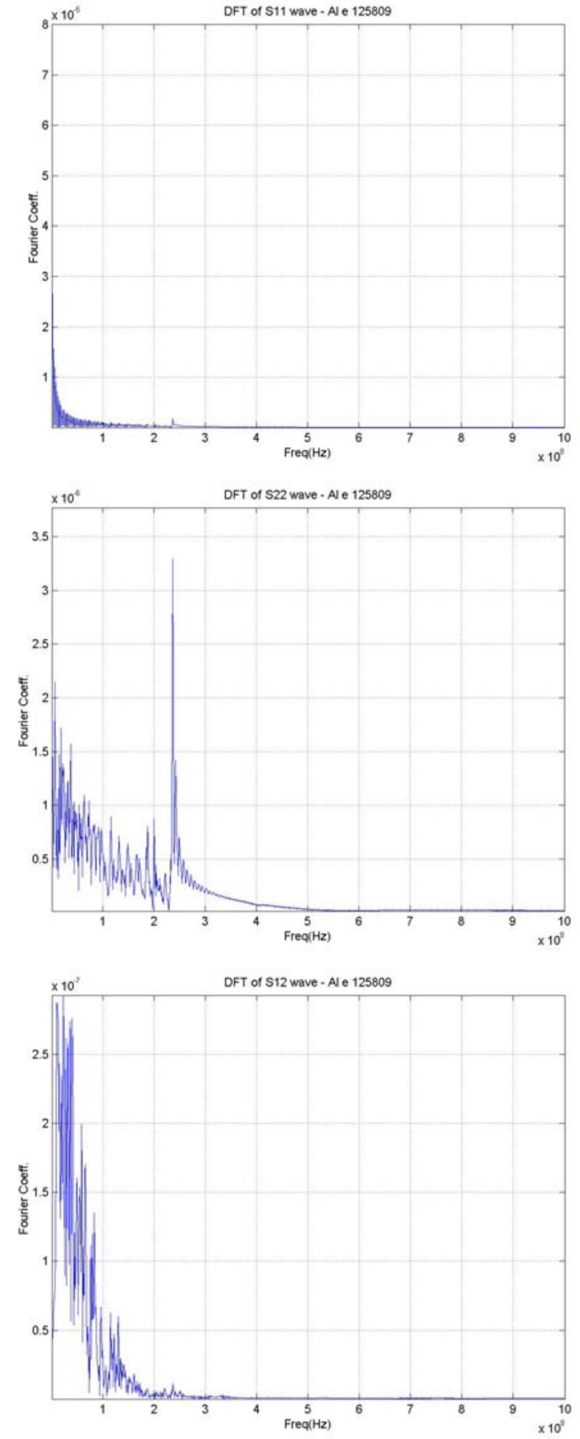


Fig. 3.13 Frequency response at Al e 125809 (location 1)

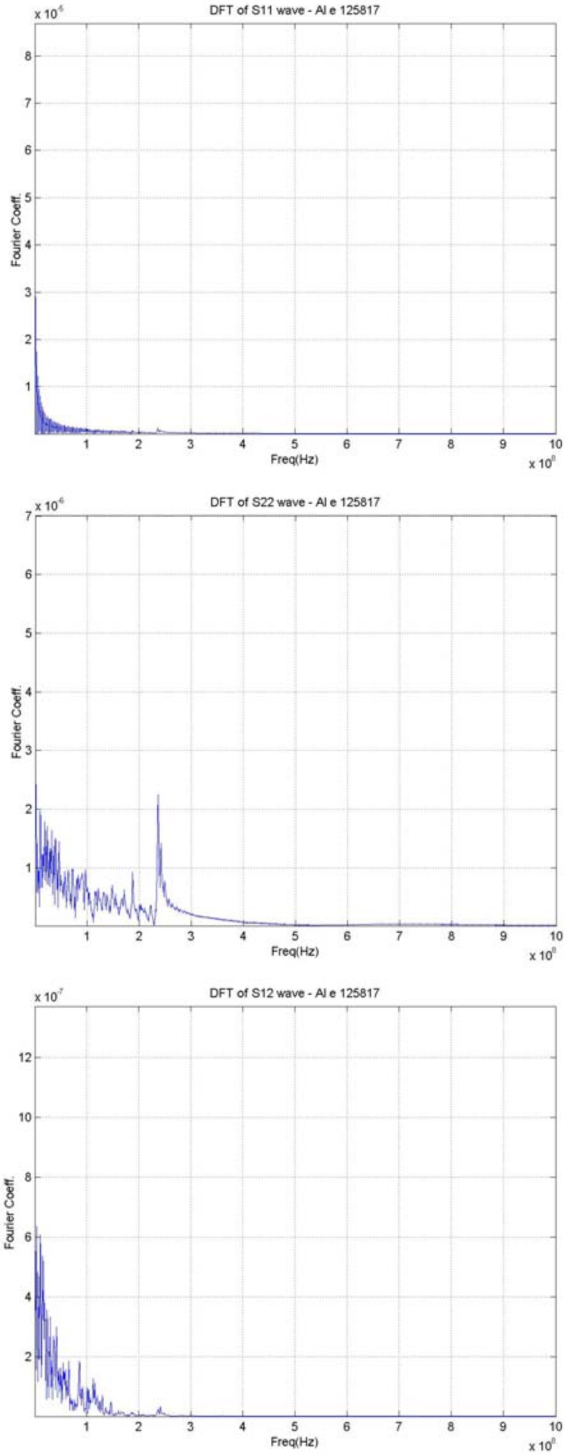


Fig. 3.14 Frequency response at Al e 125817 (location 2)

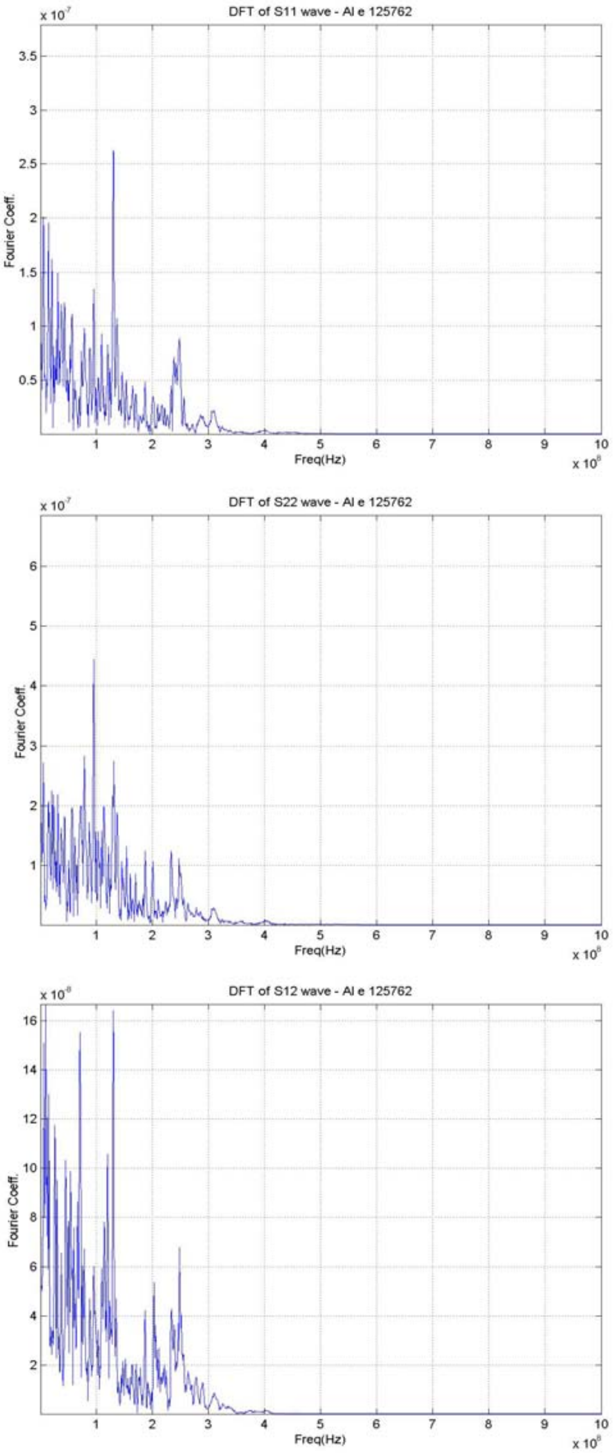


Fig. 3.15 Frequency response at Al e 125762 (location 3)

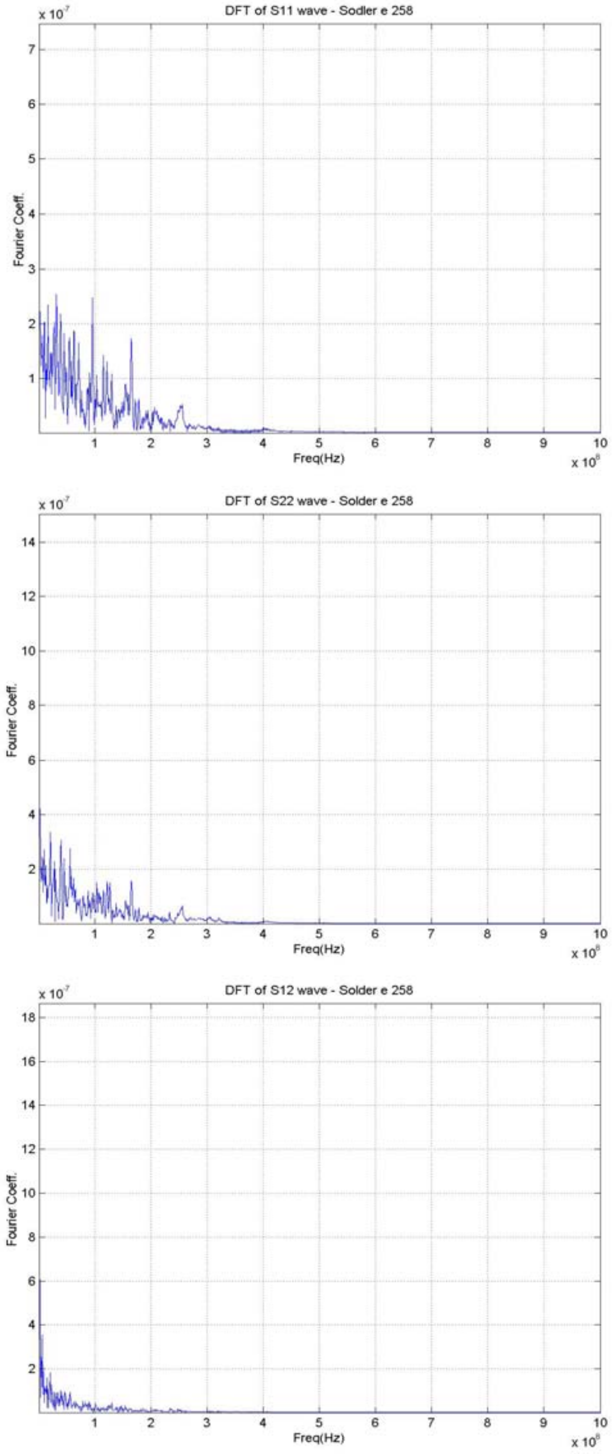


Fig. 3.16 Frequency response at solder e 258 (location 4)

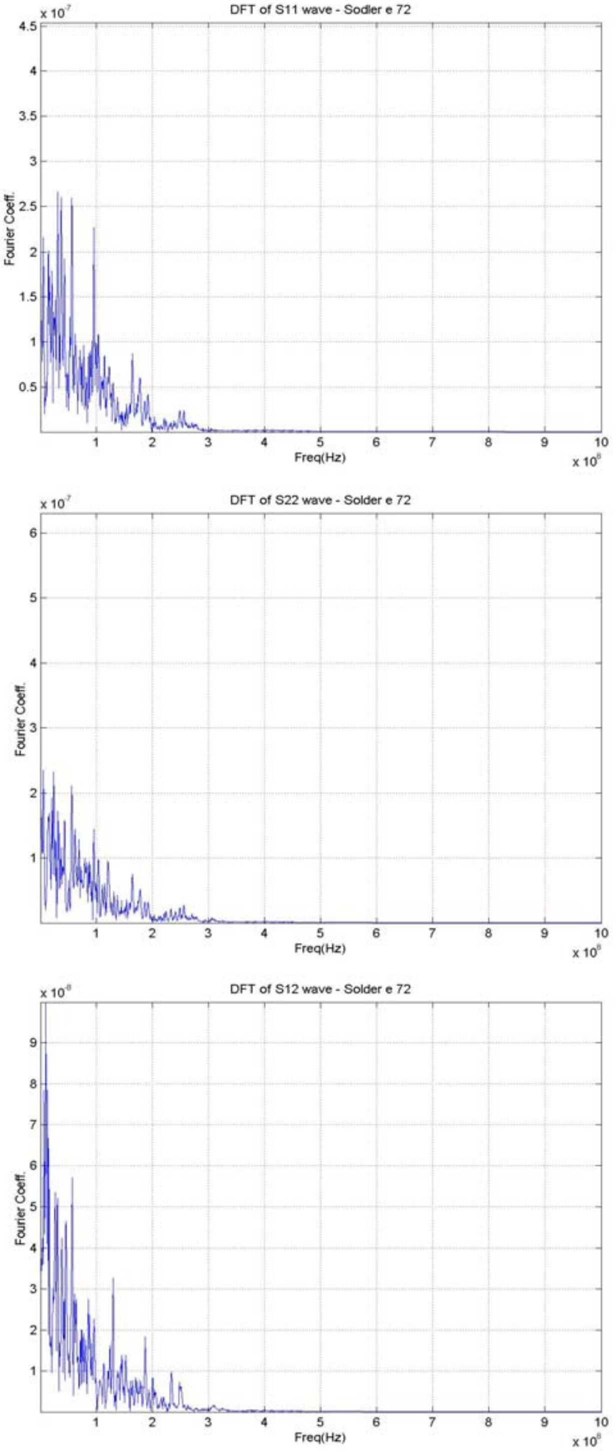


Fig. 3.17 Frequency response at solder e 72 (location 5)

CHAPTER IV

SHORT-TIME SCALE FAILURE MECHANISM IN FLIP-CHIP CONFIGURATION

4.1 New Finding and Tasks to be Accomplished

It has been shown that there are dispersive thermal-mechanical stress waves of small magnitude, high frequency and rapid attenuation propagating in electronic packages within a very short time window upon power-on. Small stress amplitude is expected with these propagating shock waves, however, that they also carry high frequency components is not. As mentioned in Chapter I, packages that are of high clock speed, high power consumption and small footprint impose great concerns over wave motions, so it is imperative that attention be paid to short-time scale effects to improve the overall packaging reliability. The present chapter investigates the initiation and propagation of high frequency stress wave in the flip-chip configuration. Tasks are defined to address the following two questions of relevancy: “How to interpret these high frequency waves?” and “What would be the failure modes associated with this dynamic effect of short-time scale?” In sections that follow investigation details are presented.

4.2 Short-Time Fourier Transform (STFT) Analysis

The time waveforms shown in Figs. 3.8 - 3.12 are clearly non-periodic. Their frequency responses resolved using the Discrete Fourier Transform (DFT) provide no simultaneous time information. It was determined necessary to appeal to joint time-frequency analysis for time information extraction. The Short-Time Fourier Transform (STFT) was employed for its inherent good temporal and spectral resolution. A brief introduction to the STFT [44] is given below.

Short-Time Fourier transform allows the spectral information of a function, $f(t)$, at a specific time $t = b$ to be obtained through first windowing the function using a proper window function, $\phi(t)$, to produce the windowed function, $f(t)\phi(t-b)$, and then taking the Fourier transform of $f(t)\phi(t-b)$. The STFT of function $f(t)$ using a Gaussian window function, $\phi(t)$, is defined in the time-frequency plane as

$$G(\omega_n, b_m) = \int_{-\infty}^{+\infty} f(t)\phi(t-b_m)e^{-i\omega_n t}dt \cong \sum_{n=0}^{m} f(n\Delta t)\phi(n\Delta t - b_m)e^{-i\omega_n(n\Delta t)}\Delta t \qquad (4\text{-}1)$$

where $\phi(t) = \frac{1}{\sqrt{2\pi}\sigma}e^{-(t^2/2\sigma^2)}$ and σ is the width of the window function, $\phi(t)$, in both time and frequency domains. Note that by definition $\phi(t)$ must satisfy $\int_{-\infty}^{+\infty}\phi(t)dt \neq 0$ as the necessary condition.

4.3 High Cycle Fatigue Analysis

In analyzing the stress waves in Chapter III, stress wave oscillations can be readily related to fatigue cycling in which stresses alternate between a maximum-minimum bound. Conventionally, S-N curves provide the most important information for studying the fatigue behaviors of materials, with S being the alternating stress amplitude and N the number of cycles to fatigue failure under S. The S-N curves of ferrous and titanium alloys show a limiting stress level, oftentimes called the endurance limit, below which fatigue failure will not occur regardless of the number of applied cycles. For most nonferrous alloys, however, the endurance limit does not exist and the S-N curve continues its downward trend as the number of cycle increases.

In general, materials could be loaded to fail from either low cycle fatigue or high cycle fatigue. In low cycle fatigue, the applied loading is so high that not only elastic strains, but plastic strains are also produced, resulting in relatively small number of cycles to failure ($N<10^5$). However, when the alternating stress level is not that high, only elastic deformations are induced, resulting in a larger number of cycles before failure. This is called high cycle fatigue and the number of cycles to failure is usually larger than 10^5 cycles [45].

Usually, fatigue failure can be recognized in two distinct stages: (1) crack initiation and (2) crack propagation. Stage (1) is where a small crack is formed and stage (2) is the process of incremental crack advance with each cycle untill sudden failure when the propagating crack reaches a critical size. For high cycle fatigue with low stress level, a large fraction of the whole fatigue life is utilized in stage (1). As stress level increases, crack forms more rapidly, making stage (2) more dominant. Oscillating fatigue loading can produce microscopic surface discontinuities resulting from dislocation slip steps from which cracks can be initiated [45].

4.4 Interpretation of the Power Density Waves

Since the magnitudes of short-time scale stress waves are very small, they cannot be directly related to fatigue test data where stresses are usually over MPa in magnitude. An alternative measurement is needed so that the generated stress waves inside a package can be compared with the experimental fatigue test data. One of the important materials directly related to fatigue in flip-chips is eutectic solder. Many studies have been directed to low cycle fatigue of eutectic solders (see Chapter II). However, no high cycle fatigue phenomenon in flip-chips has ever been investigated.

The load of triangular profile applied to produce the S-N curve of eutectic solder as shown in Fig. 4.1 is 1Hz in frequency [46]. Using the experimental data, the S-N curve for eutectic solder can be expressed as

$$S = (349.1 - 68.6 \log N) * 10^{6} (Pa) \tag{4-2}$$

Since the triangular loading is of 1Hz, variation of S in time can be approximated as

$$dS / dt = 4 * 10^{6} * (349.1 - 68.6 \log N)(Pa) \tag{4-3}$$

When Eq. (4-3) is expressed as a function of dS / dt with 99.9 % reliability (Fig. 4.2),

$$N = 10^{[5.089 - 2.423 * 10^{-9} * (dS / dt)]} \tag{4-4}$$

Here dS / dt is the temporal gradient of the stress having a unit of Watt/m^3, thus being defined as the 'Power Density' associated with the stress level, *S*. From the unit itself, dS / dt tells how much power is transmitted per cubic meter volume. As examples, the power densities of the stress waves from Chapter III that propagate along location 1 and 2 (Fig. 3.7) in Figs. 3.8 – 3.9 are presented in Figs. 4.3 and 4.4. It is seen that the dS / dt within the direct impact region of the large transient thermal gradient of the order of 11 in initial period attenuates considerably over time. The STFT of the dS / dt waves corresponding to those presented in Chapter III from Figs. 3.9 to 3.12 are shown in Figs. 4.5 to 4.16. These show the dominant frequencies of the power density waves at particular time instances. In Figs. 4.5 to 4.7 the frequency responses of power densities, *dS11/dt, dS22/dt* and *dS12/dt*, along location 2 are all 1GHz in bandwidth. These spectra demonstrate characteristics of high dispersion as they rapidly disperse over the observation window with reduced bandwidth to below 300MHz. For location 3 that is outside the direct impact region, peak frequencies arrive late and the initial spectra ranging up to 500MHz are also seen to quickly disperse to below 300MHz.

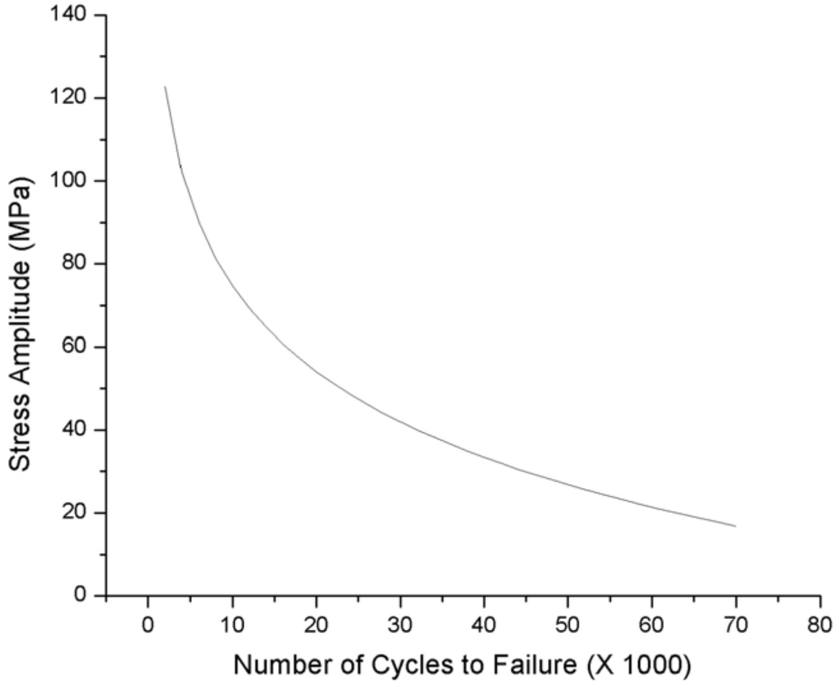


Fig. 4.1 S-N curve of eutectic solder

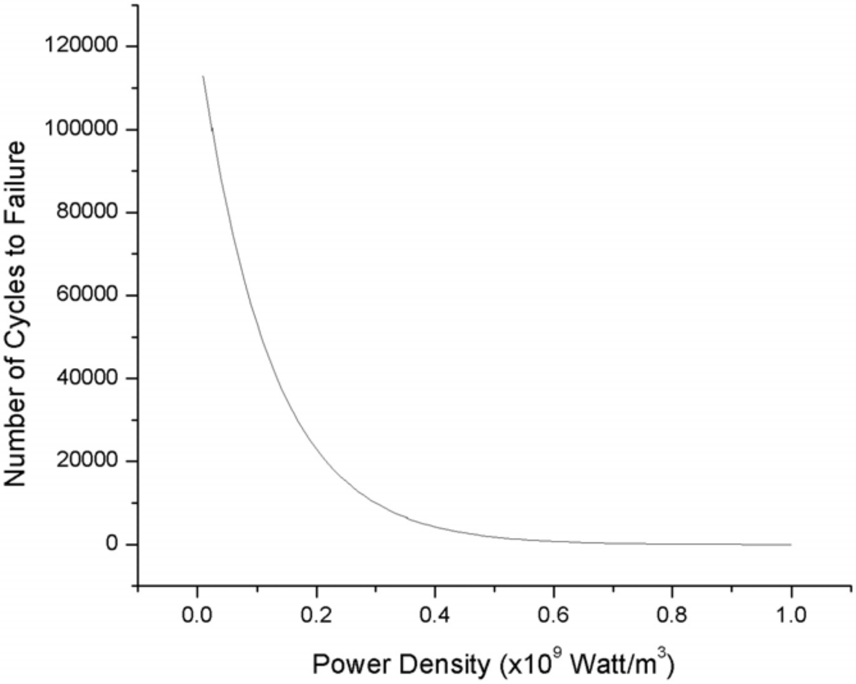


Fig. 4.2 N-Power Density curve of eutectic solder

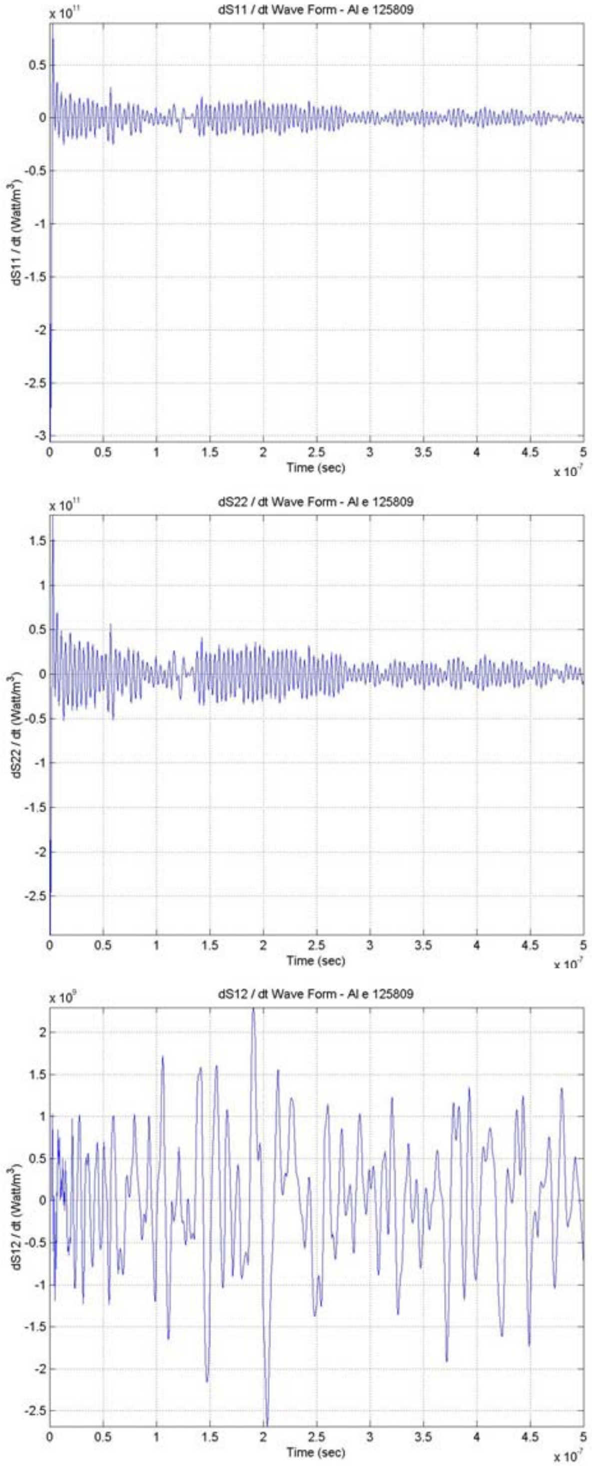


Fig. 4.3 Power density wave at location 1 (Al e 125809)

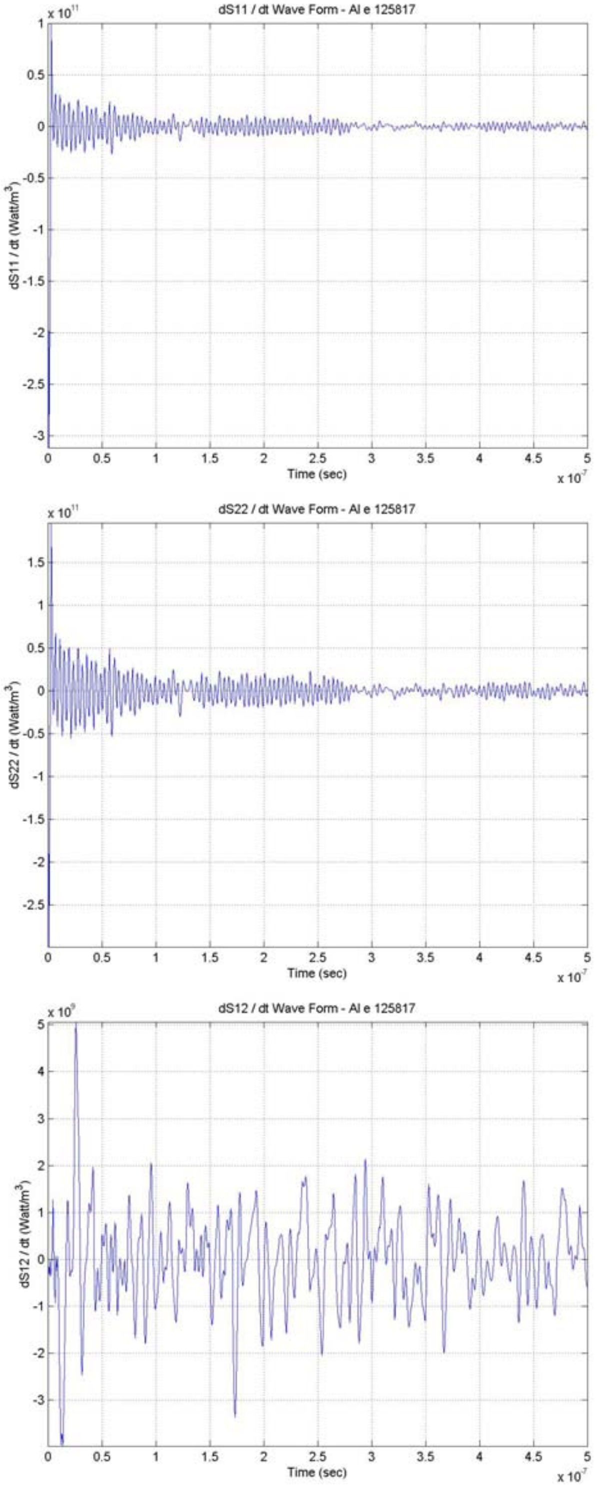


Fig. 4.4 Power density wave at location 2 (Al e 125817)

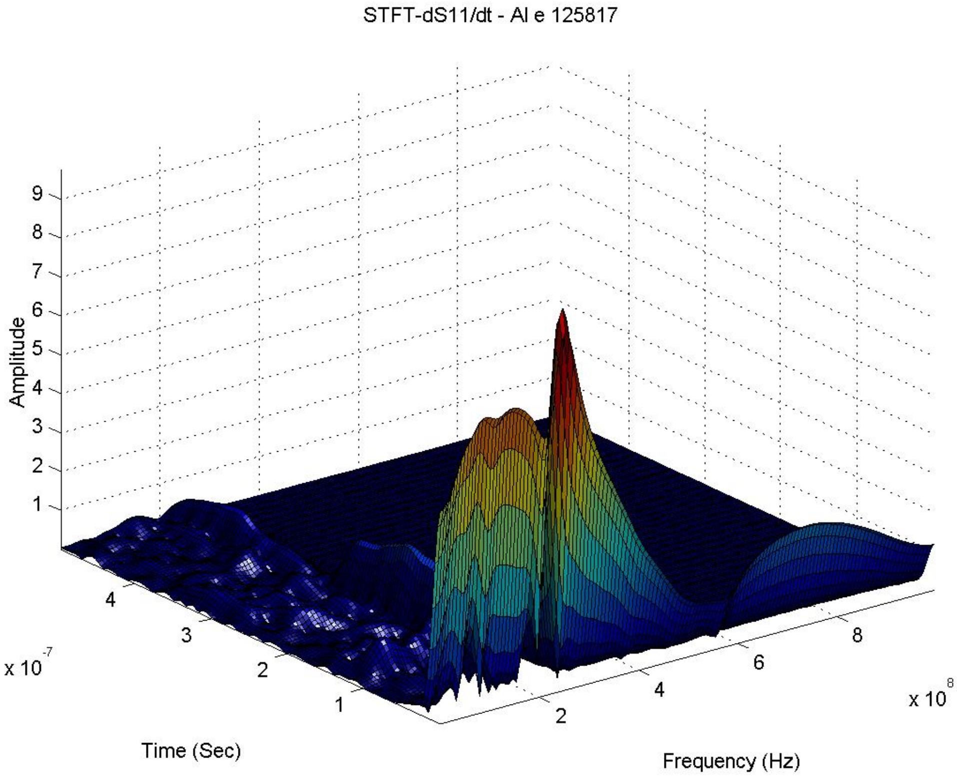


Fig. 4.5 STFT analysis of dS11/dt wave at location 2 (Al e 125817)

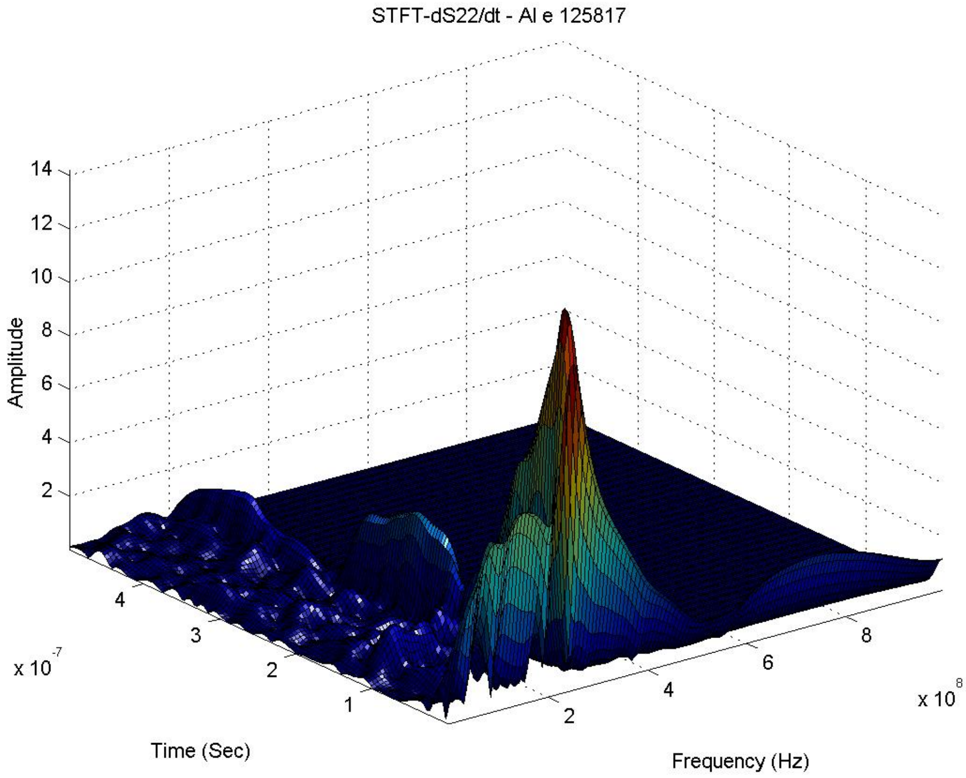


Fig. 4.6 STFT analysis of dS22/dt wave at location 2 (Al e 125817)

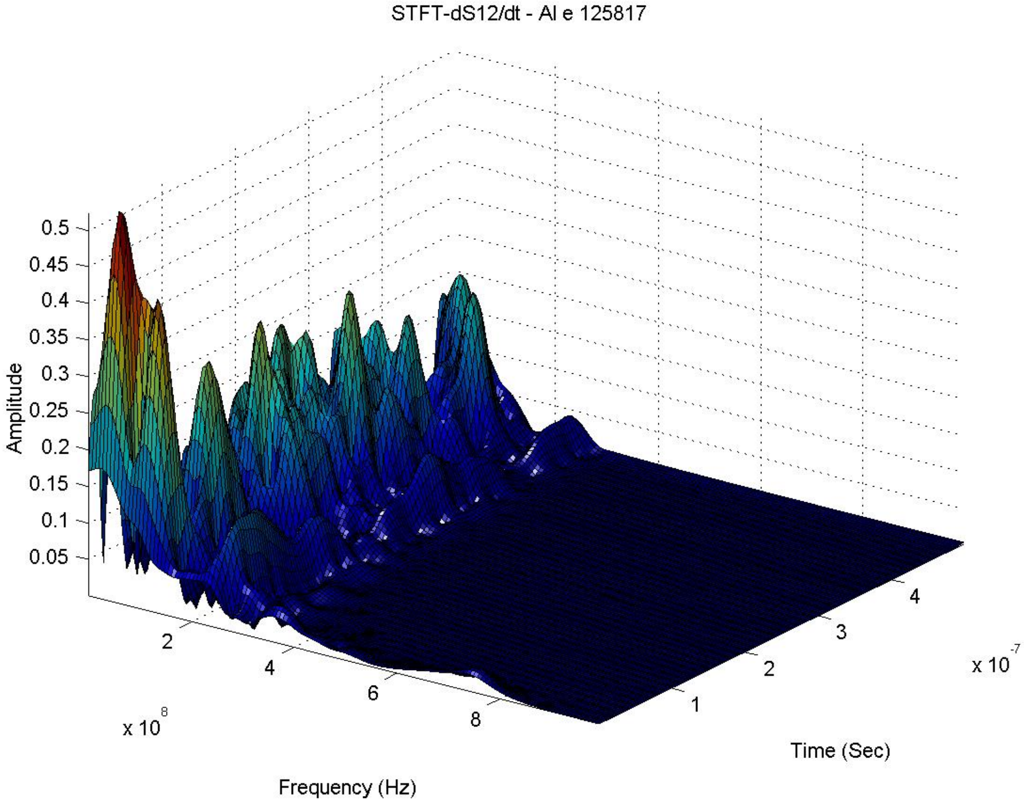


Fig. 4.7 STFT analysis of dS12/dt wave at location 2 (Al e 125817)

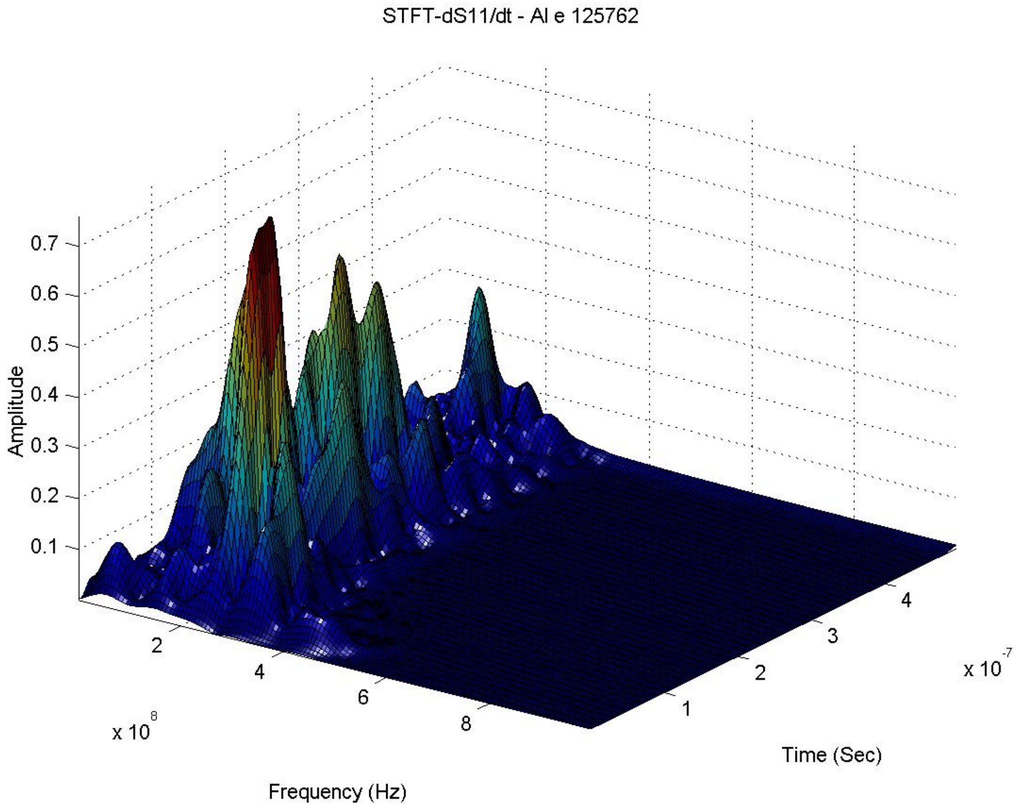


Fig. 4.8 STFT analysis of dS11/dt wave at location 3 (Al e 125762)

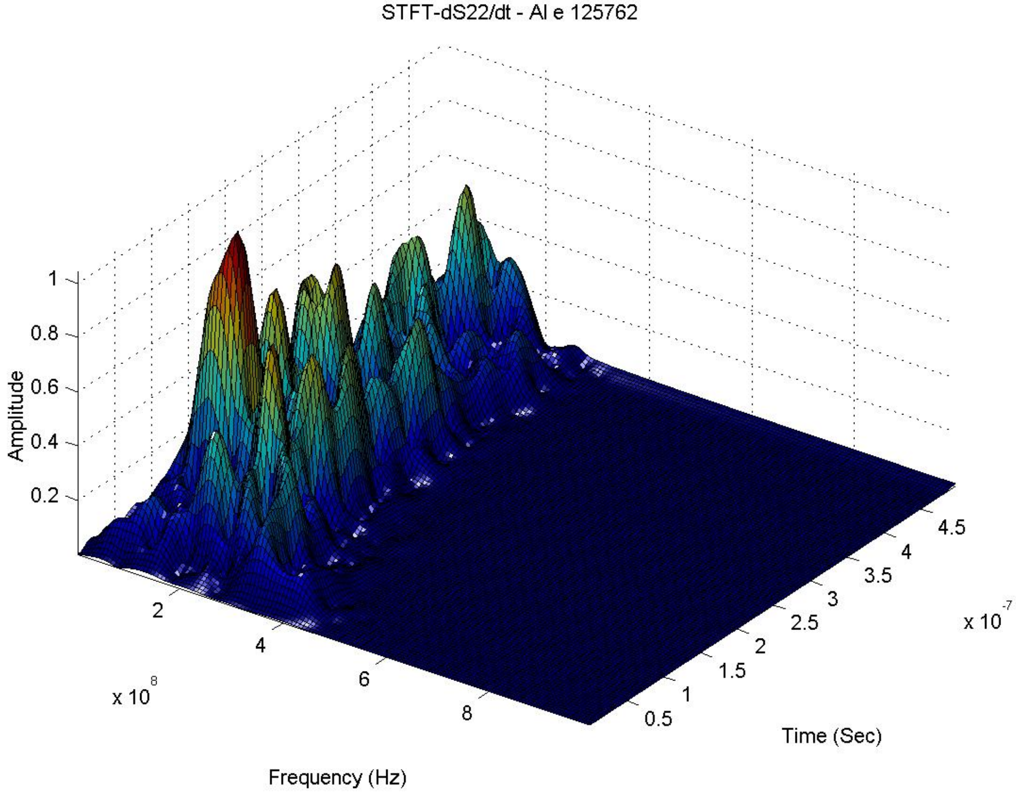


Fig. 4.9 STFT analysis of dS22/dt wave at location 3 (Al e 125762)

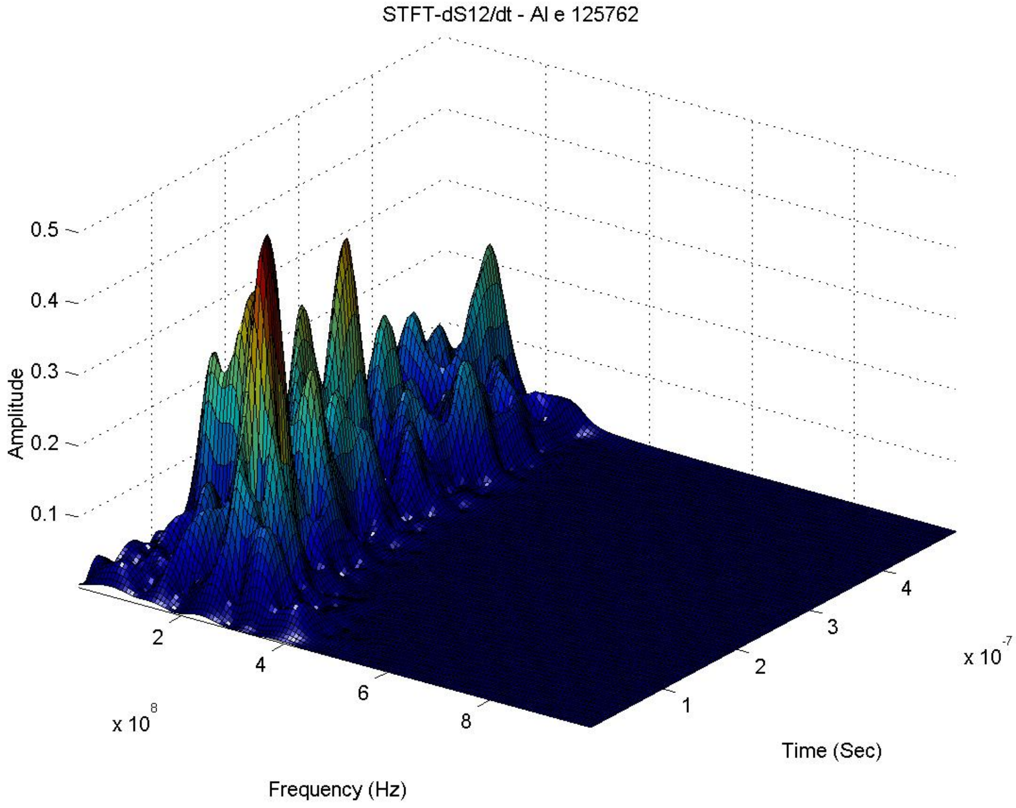


Fig. 4.10 STFT analysis of dS12/dt wave at location 3 (Al e 125762)

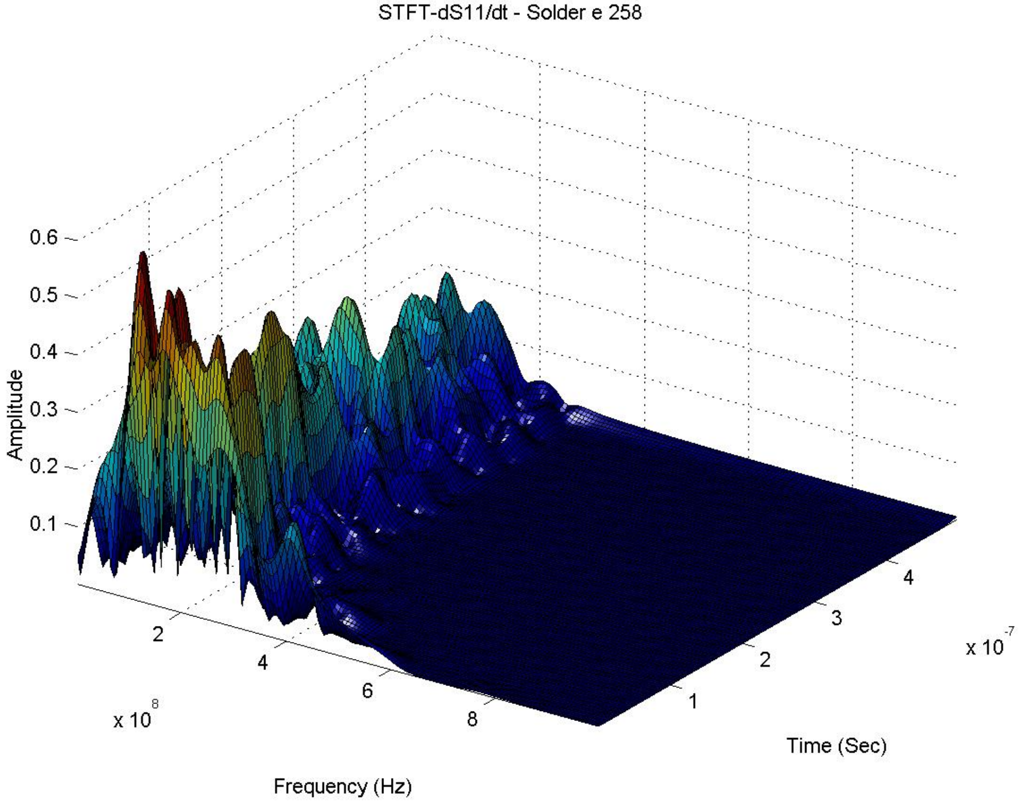


Fig. 4.11 STFT analysis of dS11/dt wave at location 4 (Solder e 258)

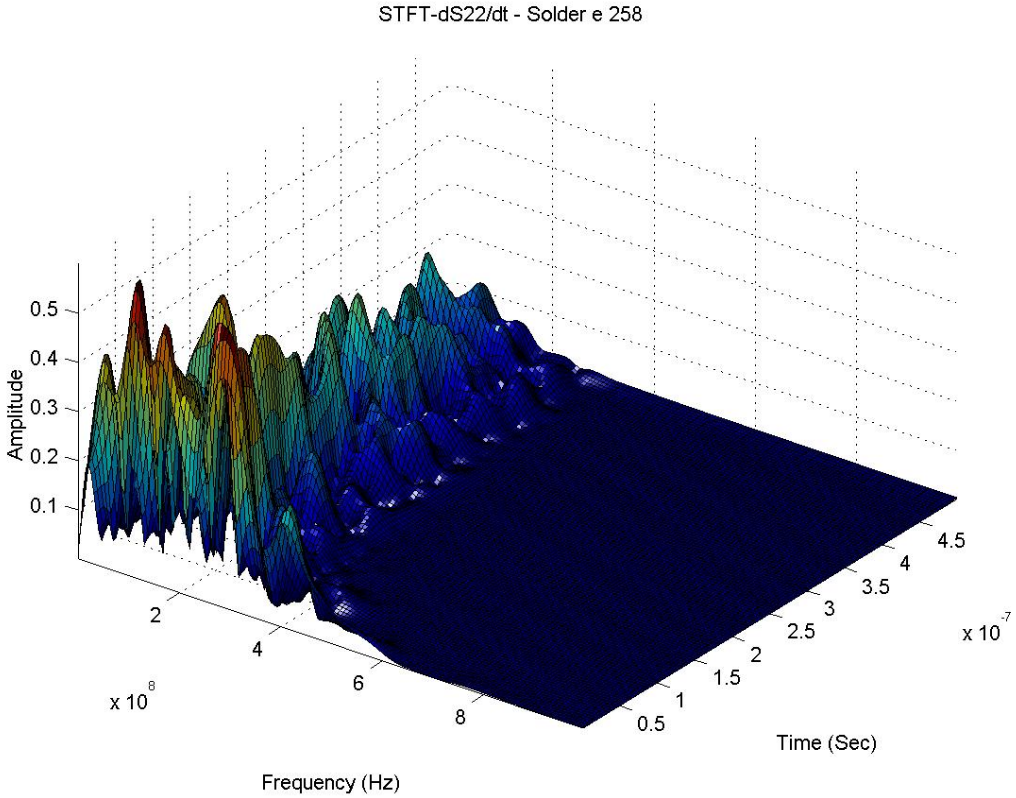


Fig. 4.12 STFT analysis of dS22/dt wave at location 4 (Solder e 258)

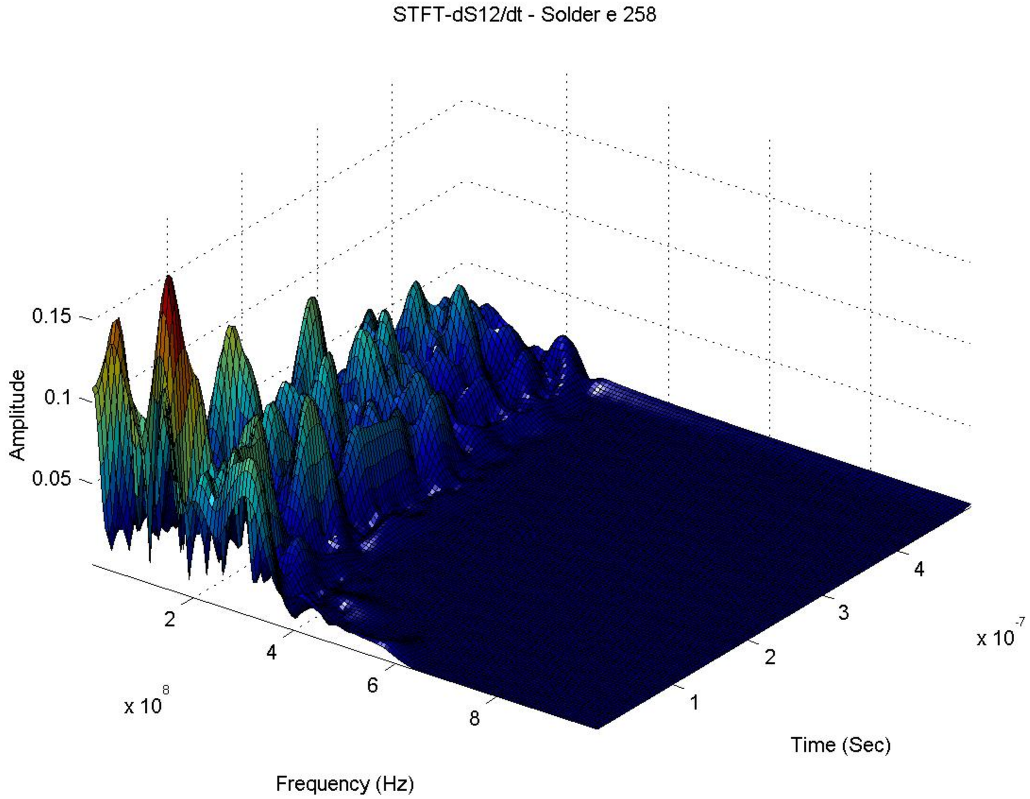


Fig. 4.13 STFT analysis of dS12/dt wave at location 4 (Solder e 258)

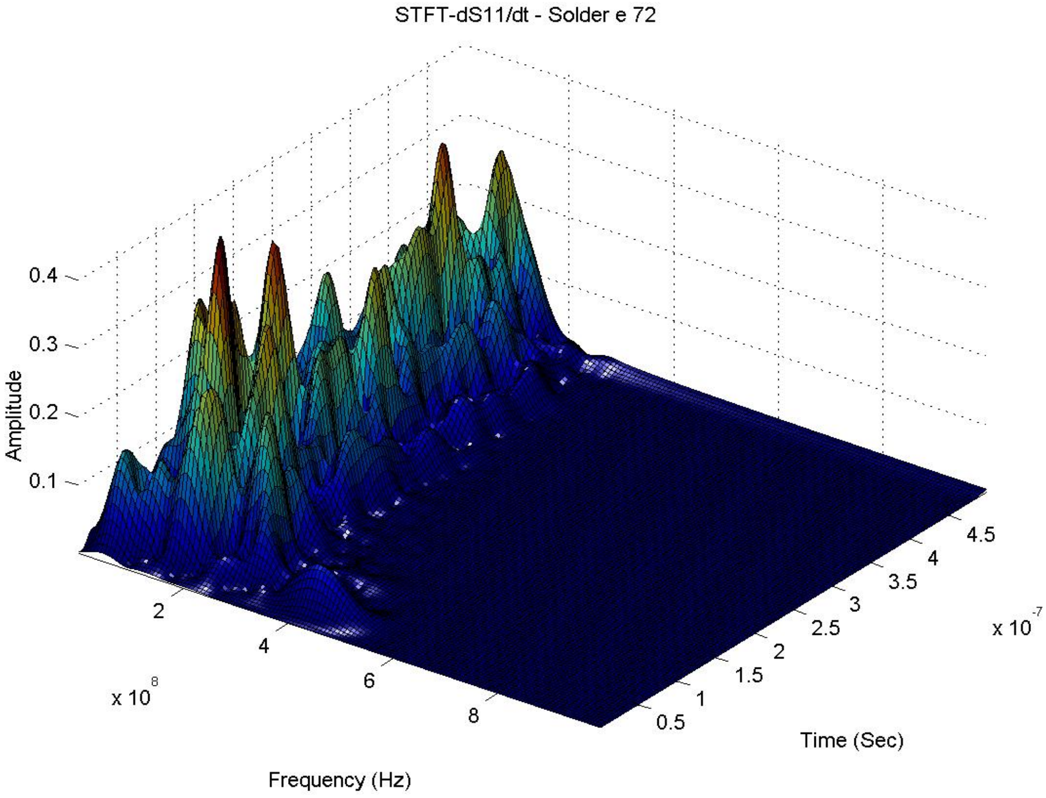


Fig. 4.14 STFT analysis of dS11/dt wave at location 5 (Solder e 72)

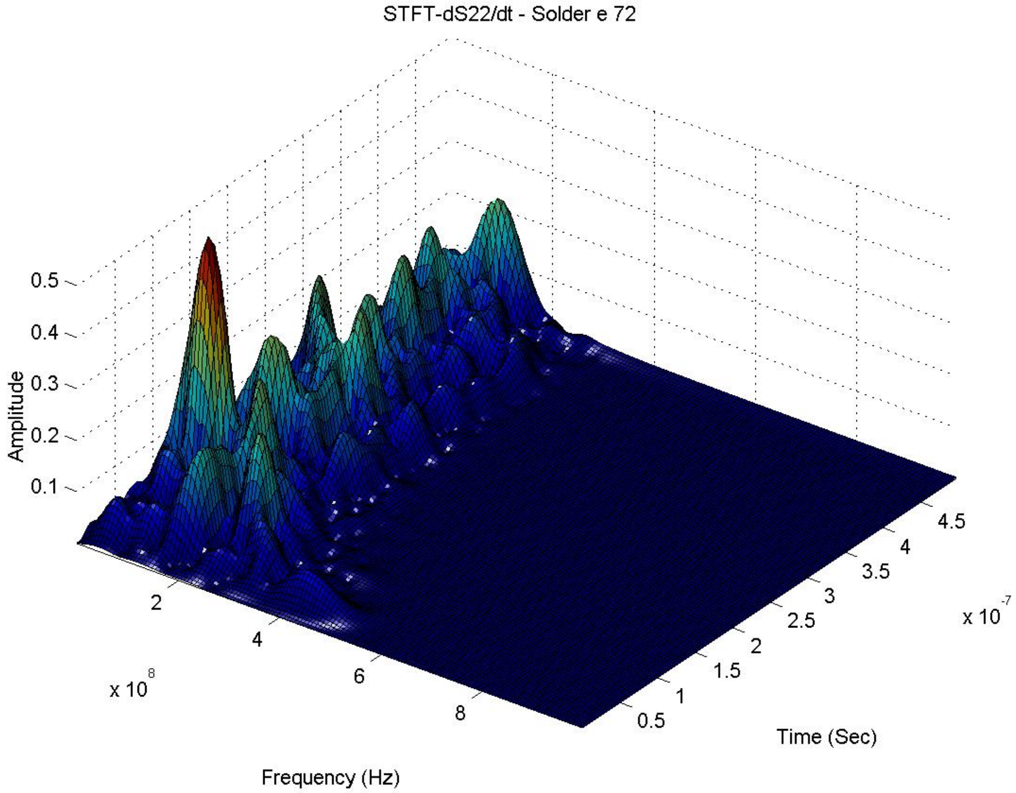


Fig. 4.15 STFT analysis of dS22/dt wave at location 5 (Solder e 72)

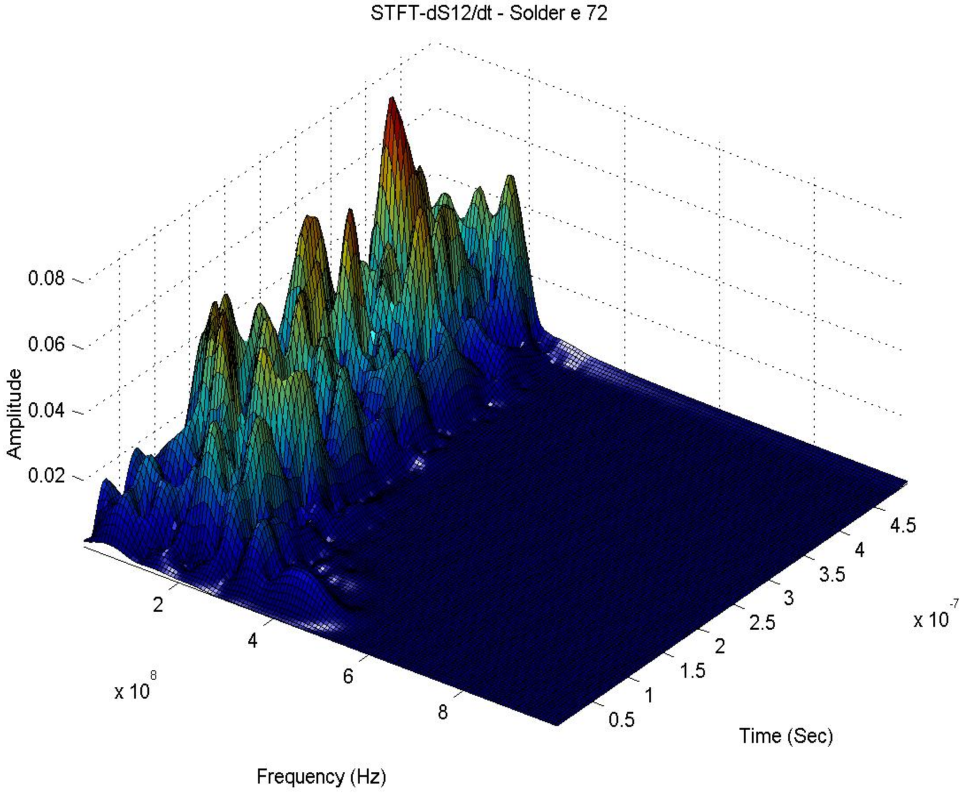


Fig. 4.16 STFT analysis of dS12/dt wave at location 5 (Solder e 72)

The same is observed with solder joints where the initial high frequencies ranging up to 600MHz are seen dispersed to below 300MHz, thus showing the characteristics of being broadband and dispersive.

Assume that the loading frequency for the eutectic solder fatigue test data is F Hz. (Note that F = 1Hz for standard low cycle fatigue tests.) Both S and F play an important role in determining whether a failure by fatigue would occur for a given time period. Because S determines N (the number of cycles at which an eventual fatigue failure would occur) and the corresponding number of applied cycles can be determined from F for a given time period, thus if fatigue failure is to be studied, all information about the applied stress level, loading frequency and time period need to be available.

Power density waves found in Figs. 4.5 to 4.16 are all dispersive and the dominant frequencies constantly vary with time. Since the dominant frequencies continuously shift as time elapses, the number of applied cycles corresponding to these dominant frequencies also varies. Therefore, there is a need for estimating how many cycles it goes through relative to the corresponding total fatigue life within a given time. By this comparison, it is possible to predict how much damage has been accumulated at a particular location for a given time by the cyclic stress wave amplitude. The procedure for determining accumulated damage by fatigue cycle loading is illustrated in Fig. 4.17.

Basically the number of cycles until fatigue failure for a given stress level can be estimated from the S-N curve. The same strategy can be applied when estimating the number of cycles until failure for a given level of power density from the Power Density–N curve. Therefore, given the power density and the corresponding loading frequencies at a specific time, it can be estimated as to how much damage has been accumulated for a given time. This would be the key point in interpreting the high cycle fatigue associated with power density waves.

Scheme of Accumulated Damage Evaluation

For a given material,

dS/dt = function1(N_f)

0.665 * dS/dt = function1(N_f) (99.9% reliability)

N_f= function2(dS/dt) : For a given dS/dt, N_f is known.

(Assumption)

At any given time t_o, the power density, $(dS/dt)_{t=t_o}$ can be decomposed into multiple cosine signals with frequency of F_i and amplitude $A_i = (dS/dt)_i$

$$(dS/dt)_{t=t_0} = \sum_i A_i Cos(F_i \Delta t)$$

N_i is the number of cycles associated with F_i, at a given time t_o with time interval Δt

$(N_f)_i$ is the number of fatigue cycles until failure associated with A_i

(1) At $t = t_o$ w/ time interval of Δt,

Accumulated damage (A.D.) = $\sum_i N_i / (N_f)_i$

(2) For given number of time steps = j

Total Accumulated damage (T.A.D.) = $\sum_j \sum_i N_i / (N_f)_i$

(3) Failure Criteria for fatigue cracking:

Failure by fatigue will occur when T.A.D. = $\sum_j \sum_i N_i / (N_f)_i \geq 1$

Fig. 4.17 Accumulated damage evaluation approach

To determine the corresponding amplitude, $A_i = (dS/dt)_i$, for each individual frequency, F_i, at a given time $t = t_o$, values of F_i can be obtained from the STFT of dS/dt waves at $t = t_o$ and A_i can be determined by comparing the summation of individual signals of A_i and F_i with the dS/dt amplitude at $t = t_o$. Take the power density wave of location 5 as an example. STFT coefficients need to be extracted along frequency at a particular time to estimate the power density levels at dominant frequencies. From Fig. 4.18, it can be checked that the dominant frequencies are 85MHz, 175MHz, 260MHz, 305MHz and 385MHz, and their corresponding STFT coefficients are 0.449, 0.239, 0.0504, 0.0221 and 0.0033. These STFT coefficients give information about the relative magnitude of the different power density levels associated with various dominant frequencies. So the power density of the normal stress wave along the 2-direction at t = 1.3E-7 sec can be expressed as

$$\begin{aligned}(\frac{dS22}{dt}) = A*[\ & 0.449*Cos(8.5E+7*\Delta t) + 0.239*Cos(1.75E+8*\Delta t) \\ & + 0.0504*Cos(2.60E+8*\Delta t) + 0.0221*Cos(3.05E+8*\Delta t) \\ & + 0.0033*Cos(3.85E+8*\Delta t)\ ] \qquad (4\text{-}5)\end{aligned}$$

where A is a variable to be determined and Δt = 5.E-10 sec

The real power density value at this particular time can be obtained from the power density wave

$$(\frac{dS22}{dt})_{t=1.3E-7\sec} = 1.546*10^9 \text{ (Watt/m}^3\text{)} \qquad (4\text{-}6)$$

If Eq. (4-5) is set to be equal to Eq. (4-6), then A = 2.258E+09.

So finally Eq. (4-5) becomes

$$(\frac{dS22}{dt}) = 1.013E+9*Cos(8.5E+7*\Delta t) + 5.396E+8*Cos(1.75E+8*\Delta t)$$
$$+1.138E+8*Cos(2.60E+8*\Delta t) + 5.000E+7*Cos(3.05E+8*\Delta t)$$
$$+7.526E+6*Cos(3.85E+8*\Delta t) \qquad \text{(4-7)}$$

Eq. (4-7) is composed of 5 different waves of varying loading frequency and alternating power density magnitude. Since the frequencies are known, the number of cycles undergone can be calculated from Δt. Also, from the magnitudes of the alternating power densities, total number of cycles until fatigue failure can be estimated using Eq. (4-4). The ratio of number of cycles undergone during Δt to total number of cycles until fatigue failure is the accumulated damage during that Δt. The calculated accumulated damage between t = 1.2975E-7 sec and t = 1.3025E-7 sec at location 5 (solder e72) amounts to 1.183E-4 (0.01183%). The entire procedure is summarized in Table 4.1. While accumulated damage is estimated, it is assumed that positive and negative alternating power density levels have the same effect on accumulated damage due to fatigue.

Until now, it has been shown how the power density waves can be analyzed and how they can be related to fatigue failure. By the notion of ‘accumulated damage by fatigue cycle’, one can estimate how much damage has been accumulated (or established) at a particular location inside a package over a specific time period. As time elapses, the damage at each step is stored up to total accumulated damage and the final failure would occur when the total accumulated damage equals to or is larger than 1 (i.e., 100%). This approach provides a qualitative measure in the probability sense for possible and potential locations for submicron cracking.

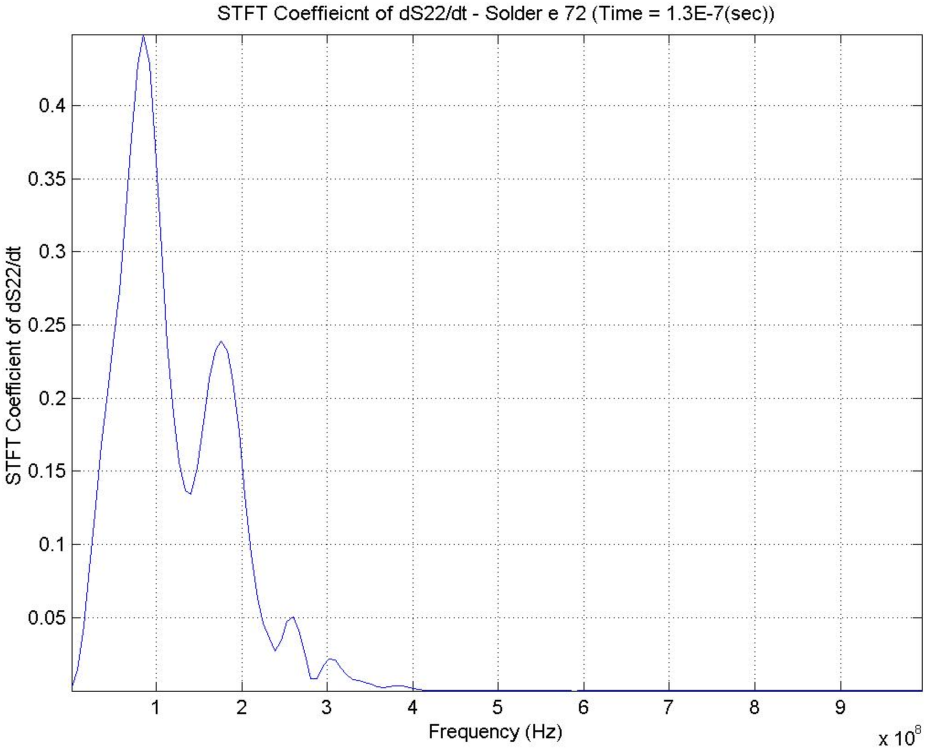


Fig. 4.18 STFT coefficient of dS22/dt wave along frequency
at location 5 (Solder e 72) at t = 1.3E-7 sec

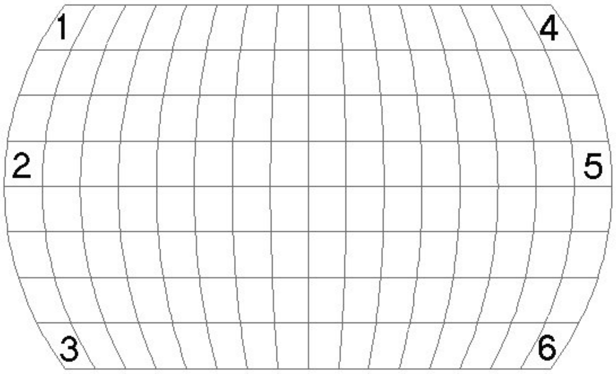
Table 4.1 Accumulated damage at location 5 (solder e 72)
between t = 1.2975E-7 sec and t = 1.3025E-7 sec

Frequency (Hz)	Power density (watt/m^3)	Accumulated damage by each power density	Accumulated damage during Δt
8.50E+7	1.103E+9	9.855E-5	1.183E-4
1.75E+8	5.396E+8	1.447E-5	
2.60E+8	1.138E+8	1.998E-6	
3.05E+8	5.000E+7	1.642E-6	
3.85E+8	7.526E+6	1.636E-6	

Between the two stages of fatigue life mentioned before, crack initiation stage is assumed to be dominant in this analysis. This is a valid assumption since the oscillating loading under investigation is related to high cycle fatigue. It should be noted that this damage estimation is presented in a probability sense. The S-N curve itself is representing average values, best fitting scattered experimental data. There is always a variation in each measured N value for different tests at the same stress level. The scatter in test data in part can be attributed to the fatigue sensitivity of uncontrollable material parameters such as metallurgical variables. So it should be understood that the larger number of total accumulated damage implies the higher probability for sub-micron crack nucleation to exist.

Time taken for crack formation by the *dS22/dt* power density waves at various locations within the 3rd and 4th solder joint from the center (Fig. 4.19) has been summarized in Table 4.2. As expected, location 1 of the 3rd solder joint, which lies under direct impact of the rapid thermal gradient in response to current flow, is predicted to fail first. Location 2, which is very close to location 1, would then fail, followed by location 4 and location 6. It should be noted that locations 3 and 5 did not fail until t = 5.E-7 sec. One of the reasons can be that the current flows askew from location 1 (adjacent to the Al layer) to location 6 (adjacent to the Cu layer), putting location 3 and 5 out of its path and making them rather unaffected by the dynamic transient phenomenon. For the 4th solder joint, no location would fail until t = 5.E-7 (sec), which is not surprising, considering that this 4th solder joint is not on the current flow path. To evaluate how much fatigue damage by the *dS22/dt* power density evolving along time, the accumulated damages by the dS22/dt wave along time at various locations within the 3rd and 4th solder joints are plotted in Figs. 4.20 and 4.21. It seems that there are sudden increases in amplitude especially for locations 1, 2, 4 and 6. These sudden hikes correspond to the moment when any of those decomposed signals has a large power density.

3rd solder joint



4th solder joint

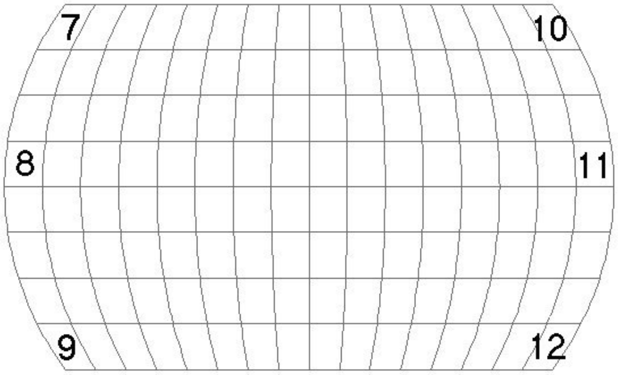


Fig. 4.19 Locations for accumulated damage estimation

Table 4.2 Location and time for accumulated damage estimation by dS22/dt within the 3rd and 4th solder joint

Location	Time for T.A.D $\geq$ 1 (sec)
1	2.00E-9
2	2.25E-8
3	Not Failed
4	1.25E-7
5	Not Failed
6	1.45E-7
7	Not Failed
8	Not Failed
9	Not Failed
10	Not Failed
11	Not Failed
12	Not Failed

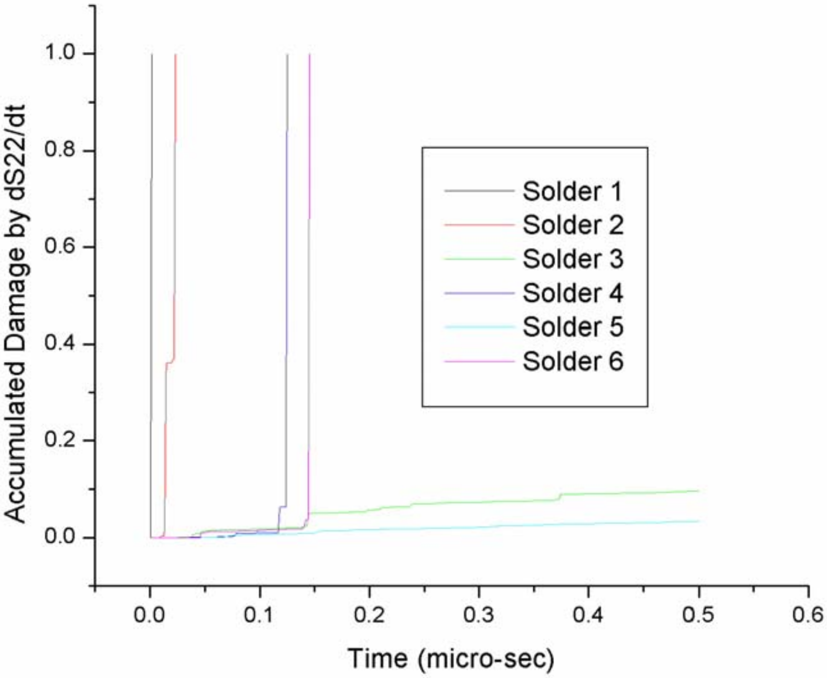


Fig. 4.20 Accumulated damage by dS22/dt along time
at various locations within the 3rd solder joint

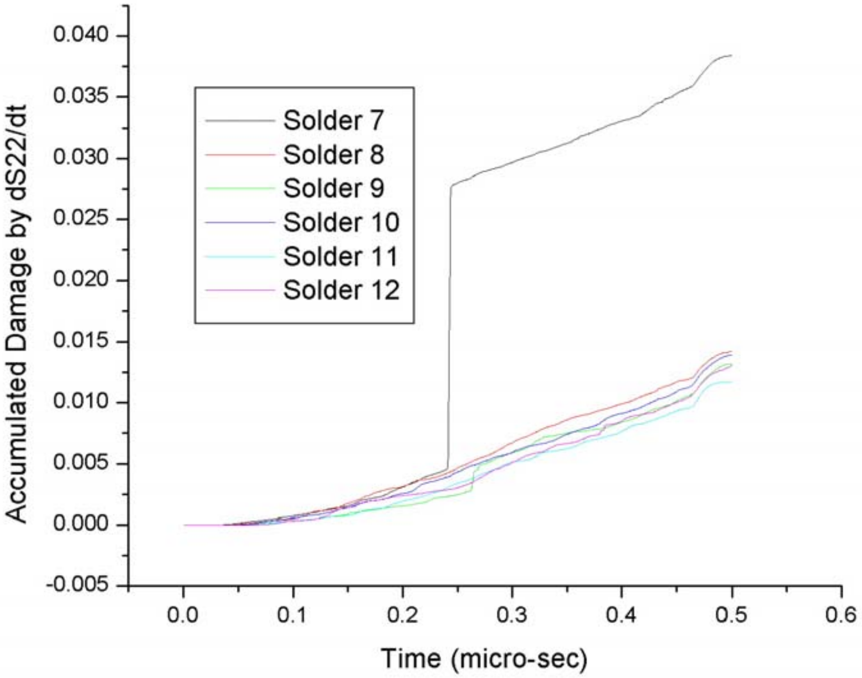
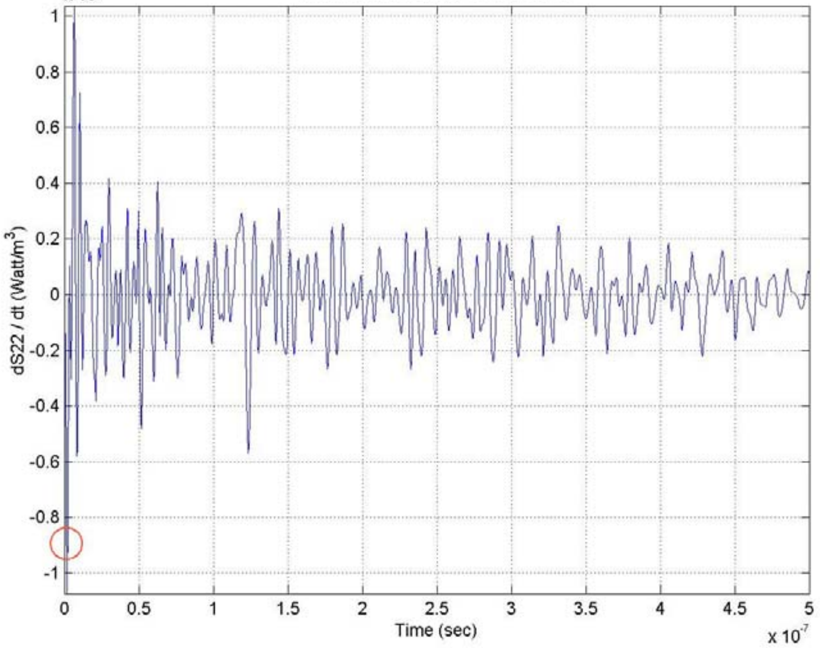


Fig. 4.21 Accumulated damage by dS22/dt along time
at various locations within the 4th solder joint

The corresponding time moments are highlighted in Fig. 4.22. Location 1 and 2 fails at the initial stage upon power-on, followed by location 4 and 6. However, it can be checked that not much fatigue damage by dS22/dt wave is accumulated at location 3 and 5. All locations within the 4th solder joint show little sign of fatigue damage by the dS22/dt power density waves. The same procedure can be applied for the estimation of damage by the dS11/dt power density waves. In Table 4.3, the estimated times until fatigue failure at various locations within the 3rd and 4th solders (same as in Fig. 4.19) are listed. Only location 1 within the 3rd solder joint fails at t = 5.5E-9 sec. Again, to see how these damages evolve along time, the accumulated damages by the dS11/dt wave at various locations within the 3rd and 4th solder joints are plotted in Figs. 4.23 and 4.24. Location 1 fails almost immediately and location 2 and 3 show 68% and 28.2% fatigue damage accumulation each by the dS11/dt wave. All other locations, especially the 4th solder joint, show almost no sign of fatigue damage.

The dS12/dt power density waves are also analyzed at the same locations and the results are presented in Table 4.4. The corresponding accumulated damage along time is shown in Figs. 4.25 and 4.26. The probability for failure by the dS12/dt wave to occur within the 3rd and 4th solder joints is relatively low compared to those associated with the normal power density waves presented before.

Location 1 of the 3rd solder joint



Location 2 of the 3rd solder joint

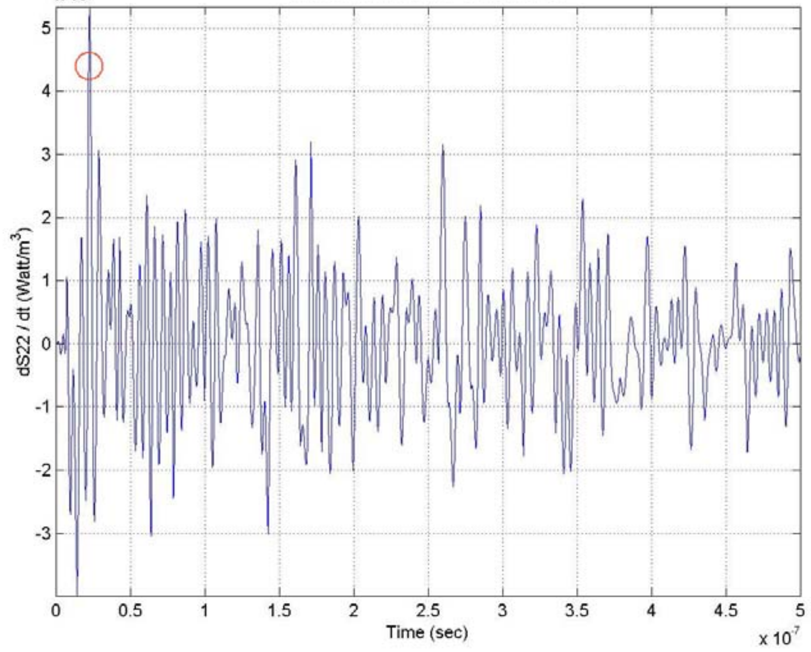
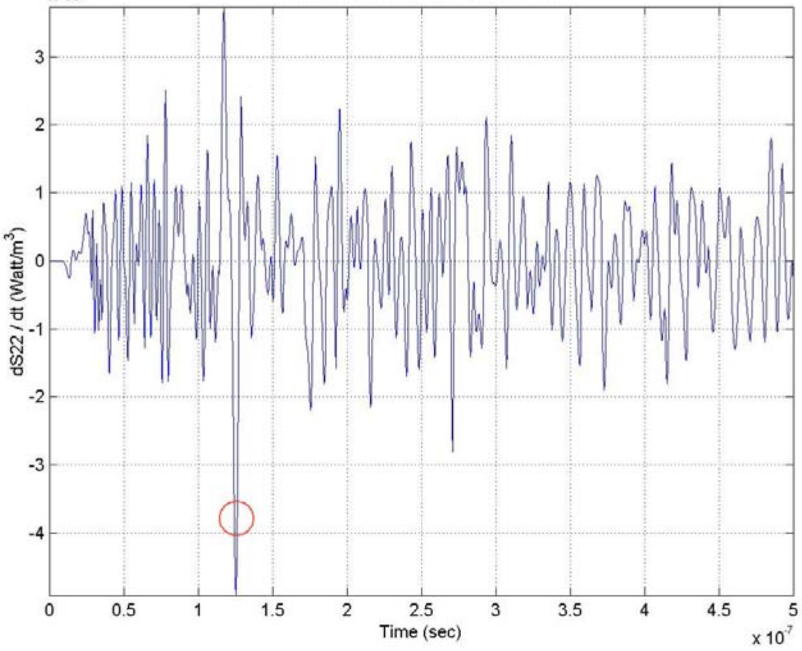
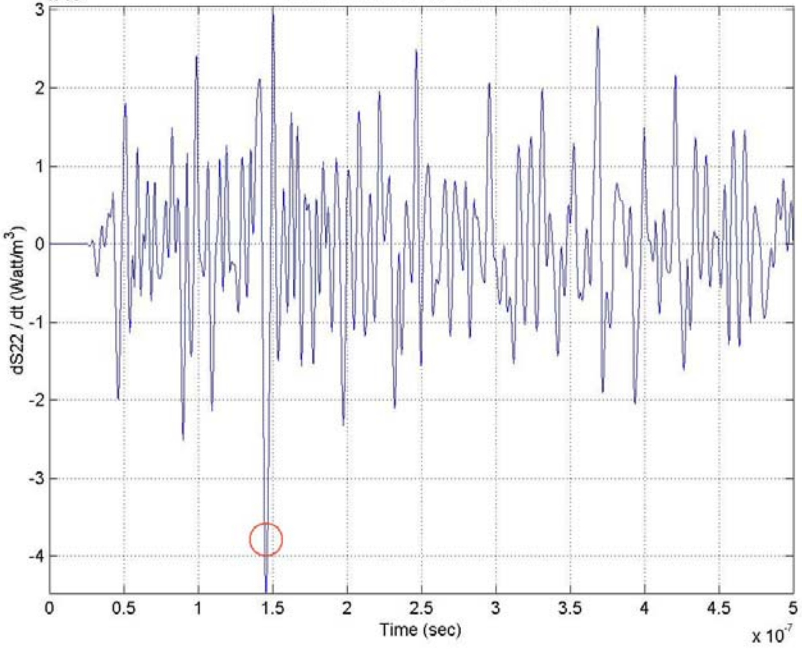


Fig. 4.22 dS22/dt power density wave at various locations within the solder joints



Location 4 of the 3rd solder joint



Location 6 of the 3rd solder joint

Fig. 4.22 Continued

Location 7 of the 4th solder joint

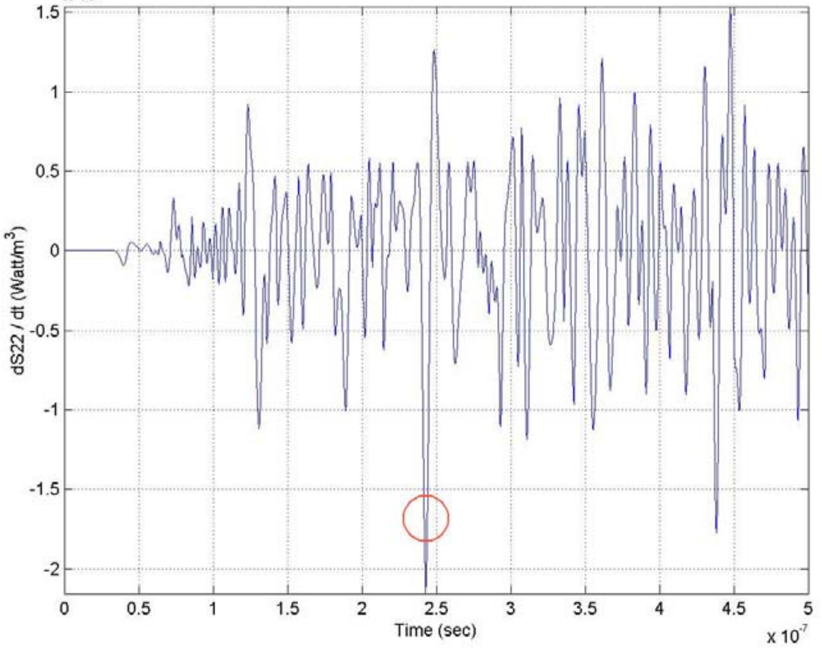


Fig. 4.22 Continued

Table 4.3 Location and time for accumulated damage estimation by dS11/dt within the 3rd and 4th solder joint

Location	Time for T.A.D $\geq$ 1 (sec)
1	5.5E-9
2	Not Failed
3	Not Failed
4	Not Failed
5	Not Failed
6	Not Failed
7	Not Failed
8	Not Failed
9	Not Failed
10	Not Failed
11	Not Failed
12	Not Failed

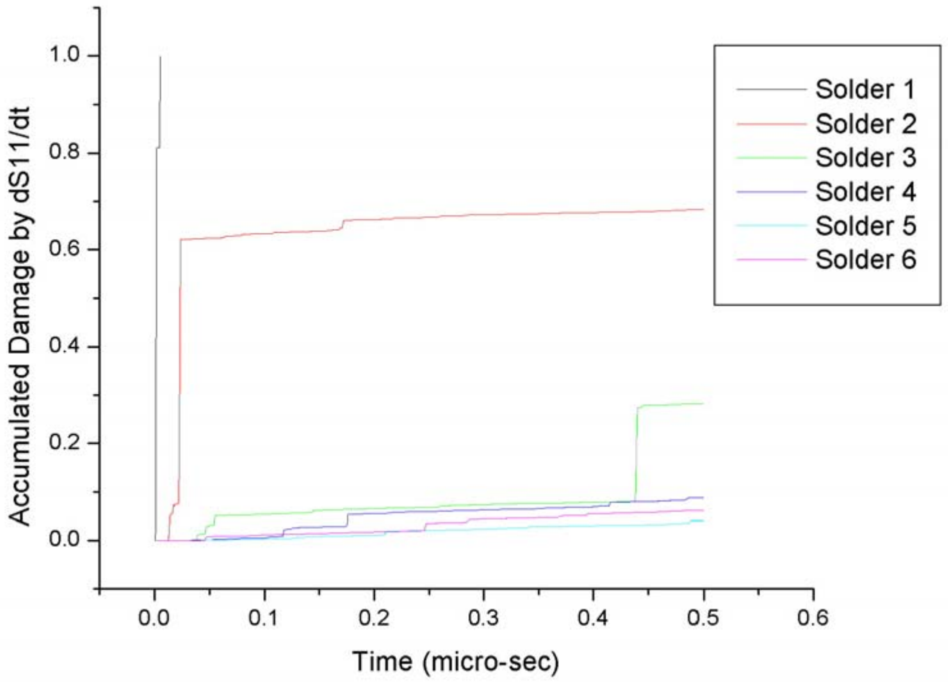


Fig. 4.23 Accumulated damage by dS11/dt along time at various locations within the 3rd solder joint

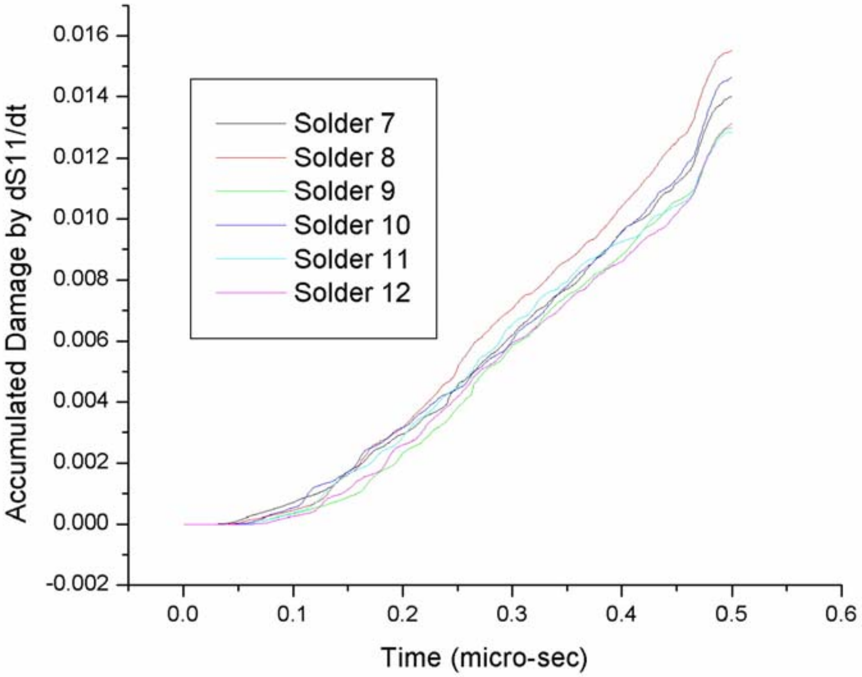


Fig. 4.24 Accumulated damage by dS11/dt along time
at various locations within the 4th solder joint

Table 4.4 Location and time for accumulated damage estimation by dS12/dt within the 3rd and 4th solder joint

Location	Time for T.A.D $\geq$ 1 (sec)
1	Not Failed
2	Not Failed
3	Not Failed
4	Not Failed
5	Not Failed
6	Not Failed
7	Not Failed
8	Not Failed
9	Not Failed
10	Not Failed
11	Not Failed
12	Not Failed

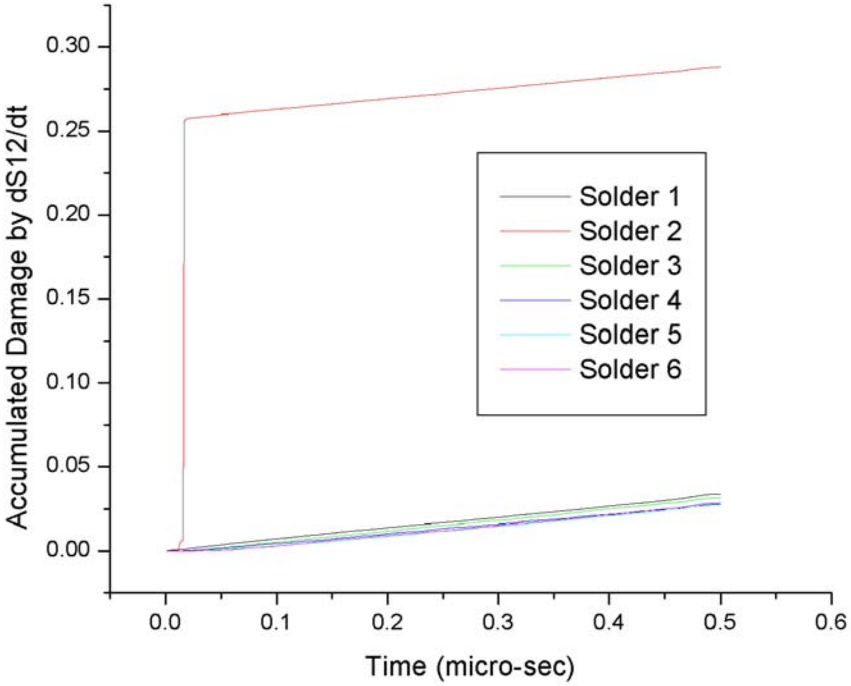


Fig. 4.25 Accumulated damage by dS12/dt along time
at various locations within the 3rd solder joint

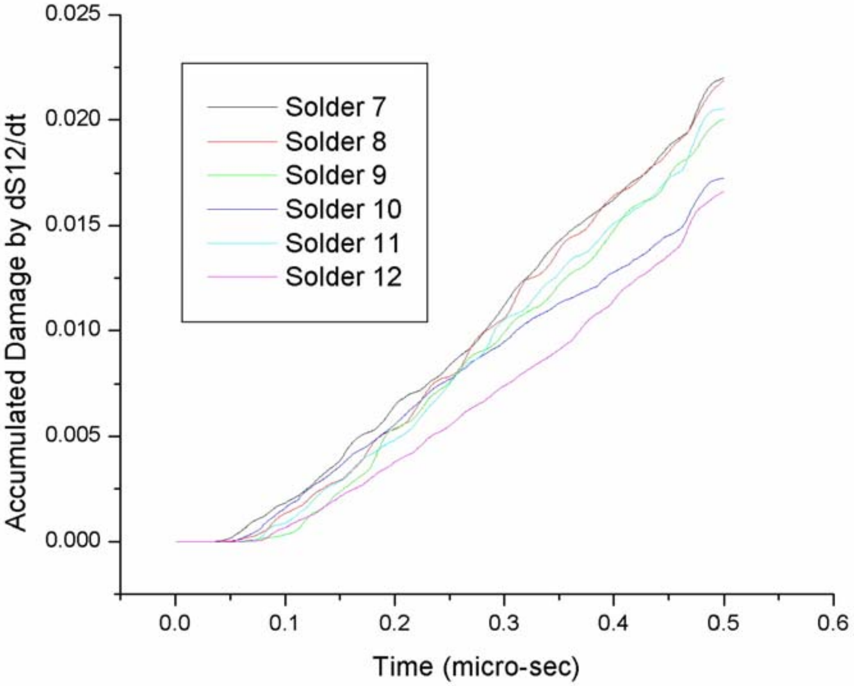


Fig. 4.26 Accumulated damage by dS12/dt along time
at various locations within the 4th solder joint

So far, power density waves within homogeneous materials were studied. The same procedure can be applied to the prediction of interfacial delamination between dissimilar materials, based on the assumption that interfacial delamination could occur by accumulated damage established by the dS12/dt power density waves. Since there is no available data on this dynamic failure at interfaces between dissimilar materials, a shearing power density–N function needs to be assumed for the prediction of accumulated damage evaluation. The assumed shearing power density–N curve for interfacial delamination is

$$N = 10\hat{}[5.089 - 2.423 * 10^{-9} * (dS/dt) + 1] \tag{4-8}$$

which is 10 times of the power density–N curve employed previously for the eutectic solder. To more accurately predict the accumulated damage behavior at interfaces, new experimental approach to quantify this dynamic shearing failure would be needed in the future.

Fig. 4.27 shows several locations between Al and other materials (Si, underfill and solders) from which shear power density waves are extracted. Again, STFT was applied to resolve dominant frequency components. By applying the above power density–N formula in Eq. (4-8), the accumulated damage by dS12/dt power density waves are evaluated at selected time instances. The total accumulated damages by dS12/dt waves for interfacial delamination at various locations in the Al layer are given in Fig. 4.28. Since this evaluation is based on the assumed shearing power density-N function, the results presented in Fig. 4.28 should be appreciated in a probability sense. These estimated time until failure and accumulated damage by power density waves are not absolute values, but rather should be compared to each other for estimating which interfacial location is more likely to fail than others. Interfacial delamination would mostly likely to occur at interfaces 2 and 10, followed by interfaces 1 and 9. Thus locations around the corner of the solder joint engaging in electrical current flow (interfaces 2 and 10) are the most critical from the viewpoint of interfacial delamination.

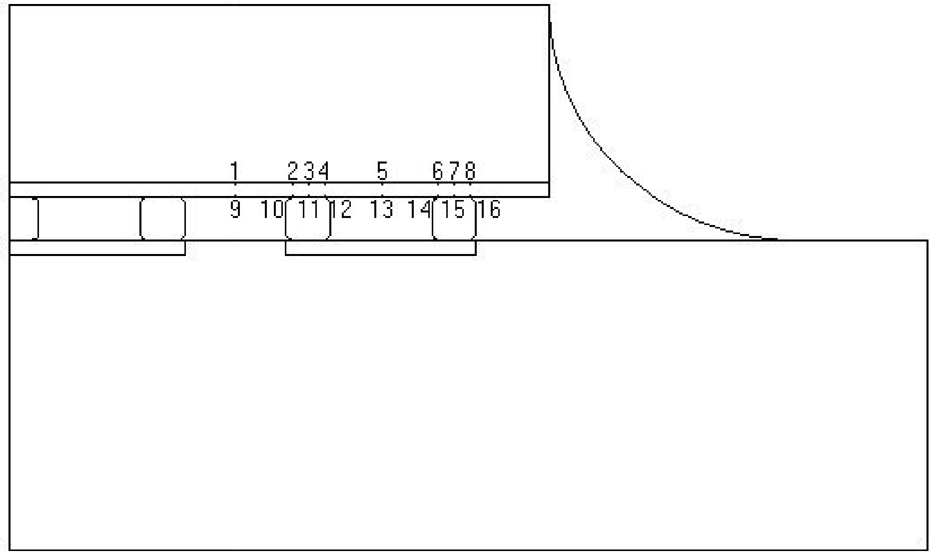
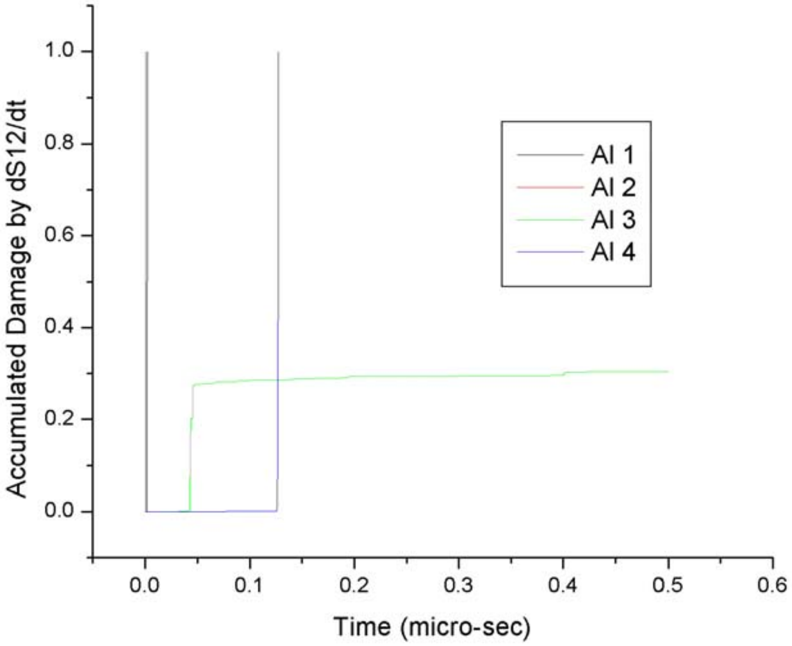


Fig. 4.27 Selected locations in flip-chip for waveform acquisition
for interfacial delamination damage evaluation

Interface 1 to 4



Interface 5 to 8

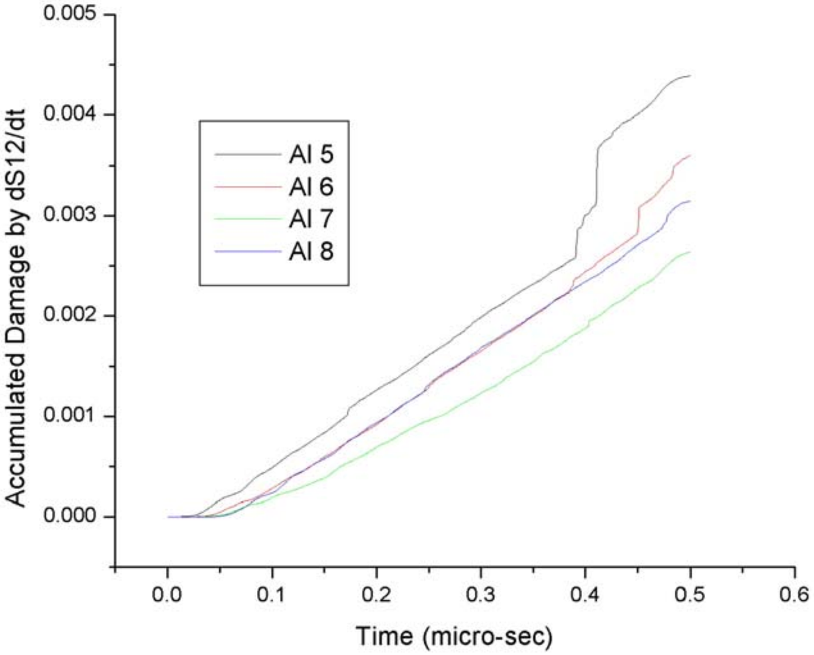
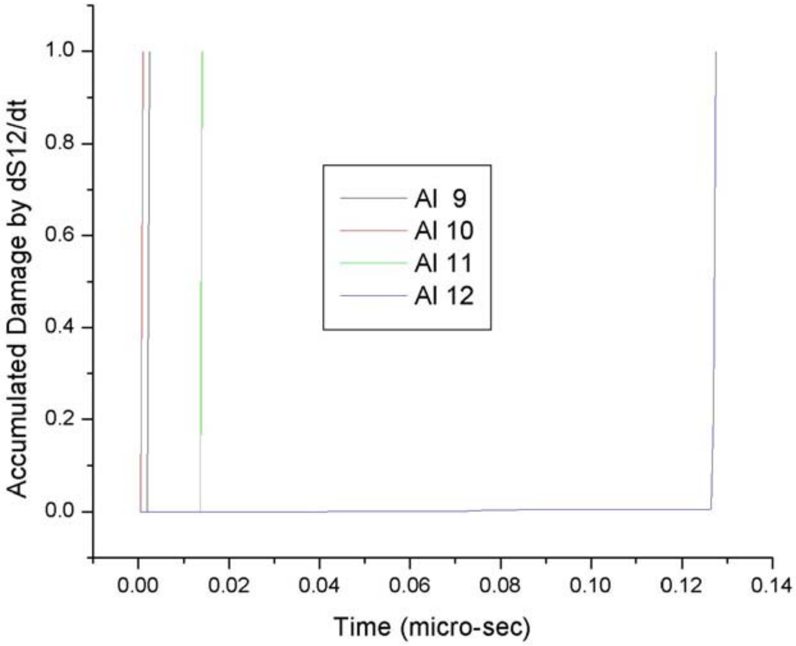


Fig. 4.28 Accumulated damage by dS12/dt along time
at various interface locations between Al and other materials

Interface 9 to 12



Interface 13 to 16

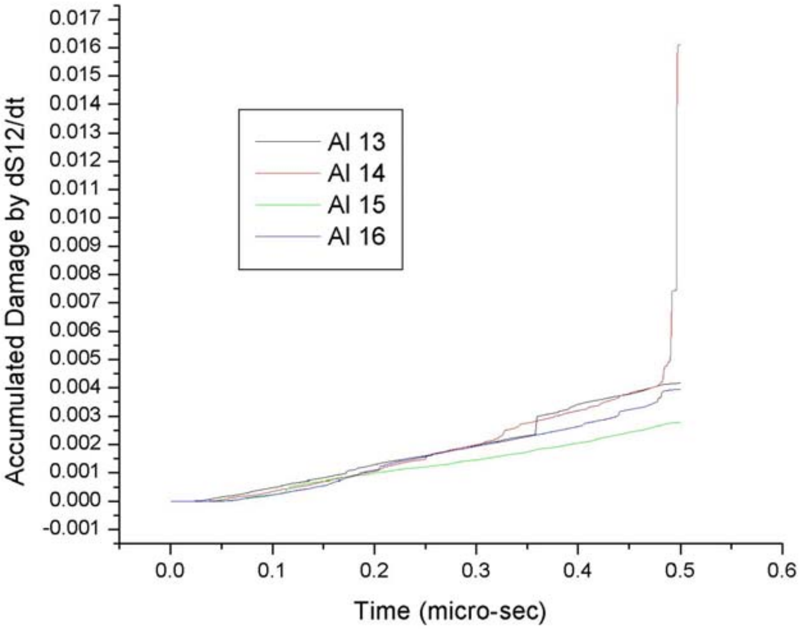


Fig. 4.28 Continued

Interfaces 1 and 9 also demonstrate high probability to fail, followed by interfaces 11, 4 and 12. It should be noted that interface 3 has relatively low possibility for interfacial delmanination failure than all the others around the 3rd solder joint. Lastly, other locations show no sign of interfacial delamination using this accumulated damage approach.

4.5 Conclusions

In summary, at location 1 within the 3rd solder joint, which is directly hit by large transient thermal gradient, the probability for microcrack formation is extremely high in both the 1- and 2-direction. When long-time scale loading initiates, these cracks would open and further propagate subject to the induced thermal stress. High probability for microcracking in the 1-direction also exists at locations 2, 4 and 6. Locations 4 and 6 in the corners would show higher possibilities than location 2 for further crack propagation in the 1-direction since these areas are where high thermal stresses are produced in the long-time scale. The effects of shearing power densities in solder joints were relatively low compared to the normal power densities, and the locations most likely to fail from interfacial delamination are those around the corner of the solder joints experiencing high current densities.

It has been shown how power density waves generated by transient thermal gradient induced by current flows inside an electronic package can be interpreted and further correlated to microcrack nucleation and interfacial delaminations at various locations. Even though the generated stress magnitudes are very small, however, the high frequencies that propagating stress waves carry render sub-micron cracking possible by their highly dynamical features. Considering today's trends mentioned in Chapter I, having this notion of short-time scale failure would be extremely helpful in achieving the goal of reliability improvement in advanced electronic packages.

CHAPTER V

INVESTIGATION OF OPTIMAL UNDERFILL MATERIALS FOR SHORT-TIME SCALE EFFECT

5.1 Effects of Underfill Material Properties: Elastic vs. Viscoelastic

In Chapter IV, failure mechanisms associated with the short-time wave propagation were investigated. As material attenuation can have a significant impact on stress wave generation and propagation, the fact that the underfill material was assumed to be elastic, not viscoelastic, had raised the concern for obscuring the true characteristics of the short-time scale waves. In this chapter, viscoelastic underfill materials are considered to investigate the effect of viscoelasticity on wave motion and the induced failure mechanisms.

5.1.1 Viscoelastic Modeling of Underfill Material

The viscoelastic model considered herein is based on the Maxwell model, which is composed of a series of spring and dashpot elements defined using the Prony series expansion

$$G(t) = G_e + \sum_i G_i \exp(-\frac{t}{\tau_i}) \tag{5-1}$$

where $G(t)$ is the shear relaxation modulus, G_e is the equilibrium shear modulus as time $t \to \infty$, and G_i and τ_i are shear modulus and relaxation time, respectively, for each element. The instantaneous shear modulus G_o can be defined as

$$G_o = G_e + \sum_i G_i \tag{5-2}$$

By letting $g_e = \frac{G_e}{G_o}$ and defining relative modulus, $g_i = \frac{G_i}{G_o}$, Eq. (5-2) becomes

$$g_e + \sum_i g_i = 1 \tag{5-3}$$

Eq. (5-1) can then be expressed as the following,

$$G(t) = G_o g_e + \sum_i G_o g_i \exp(-\frac{t}{\tau_i})$$

$$= G_o[(1 - \sum_i g_i) + \sum_i g_i \exp(-\frac{t}{\tau_i})]$$

or alternatively as

$$G(t)/G_o = 1 - \sum_i g_i (1 - \exp(-\frac{t}{\tau_i})) \tag{5-4}$$

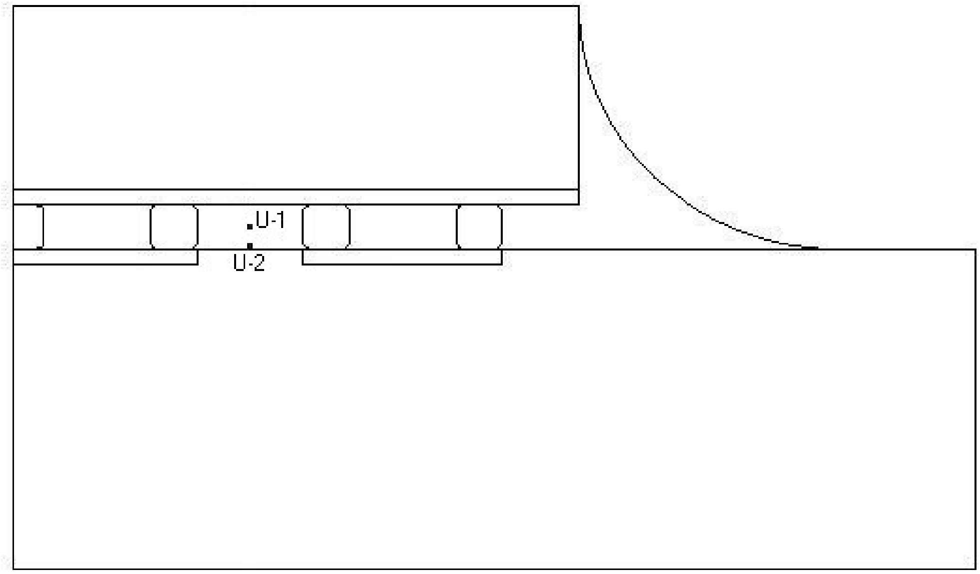
Eq. (5-4) is of the format that can be incorporated into ABAQUS analysis. Simulation results obtained by using this viscoelastic property for the underfill are discussed in the next section.

5.1.2 Wave Propagation with Viscoelastic Underfill Material

In this section, results corresponding to multi-physics study of the flip-chip package incorporating viscoelastic underfill materials are compared to the results with elastic underfills. Based on the aforementioned Maxwell model, the viscoelastic underfill material is modeled as in Table 5.1 (with G_e = 252.881 MPa) [47]. While viscoelastic material is expected to attenuate propagating waves, the extent of attenuation is of main interest. First, wave propagation within the underfill material is considered. In Fig. 5.1, two locations were chosen for waveform extraction, with one in the center of underfill and the other at the bottom of the underfill in contact with the PCB.

Table 5.1 Viscoelastic material parameters of underfill for each element

Relaxation Time (sec)	G_i (MPa)	g_i
1.0145E-9	59.45	0.01262
1.0145E-8	120.19	0.02552
1.0145E-7	294.43	0.06252
1.0145E-6	361.99	0.07686
1.0145E-5	605.57	0.12858
1.0145E-4	693.13	0.14178
1.0145E-3	855.40	0.18163
1.0145E-2	807.59	0.17148
1.0145E-1	392.61	0.08336
1.0145	164.28	0.03488
10.145	56.69	0.01204
101.45	45.42	0.00964



3rd solder joint

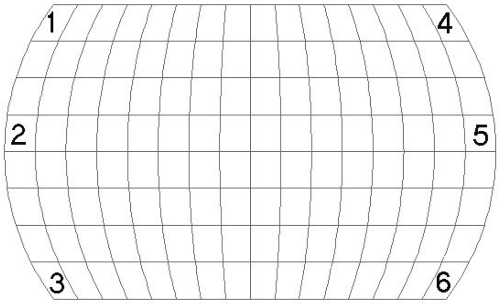
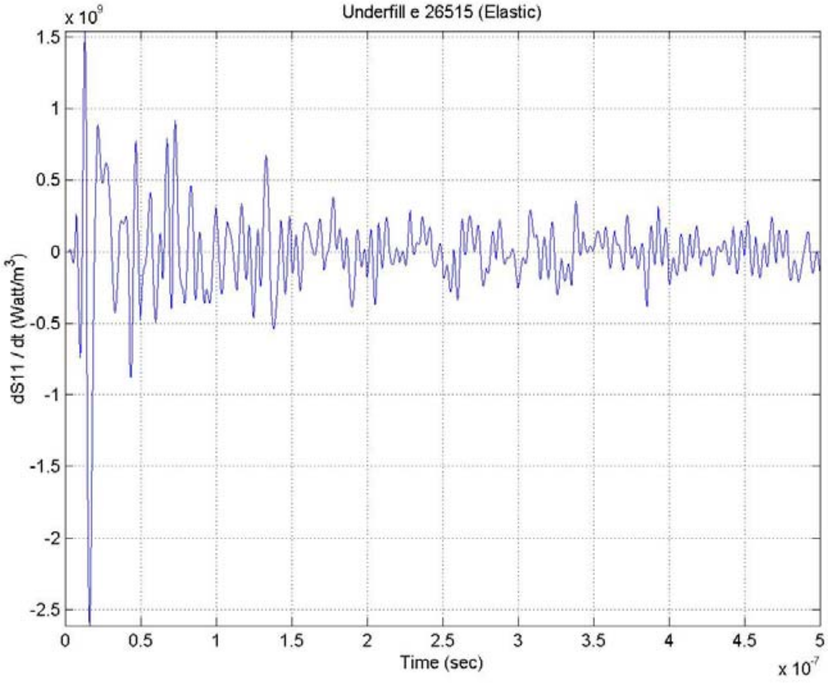


Fig. 5.1 Selected locations within underfill and the 3rd solder joint for waveform acquisition

Fig. 5.2 shows the two normal power density waveforms along the 1-direction corresponding to the elastic (Top) and viscoelastic (Bottom) underfill materials. The $dS22/dt$ and $dS12/dt$ waveforms are given in Figs. 5.3 and 5.4, respectively. They are all extracted from location U-1 as in Fig. 5.1. The attenuation in all power density amplitudes seems insignificant, although there is slight decrease in magnitude. The accumulated damages determined by analyzing both the frequency and amplitude following the procedures detailed in Chapter IV are evaluated in Figs. 5.5 to 5.7 (It should be noted that since S-N data for underfill was not available, that of eutectic solder was used. So its accumulated damage analysis results should be compared only between underfill materials in a qualitative way). It is shown that when underfill material is viscoelastic, waves attenuate more in the case of elastic underfills resulting in a slight decrease in the accumulated damage by the corresponding power density. However, as fatigue damage is more critical in solder joints than in underfills, how viscoelastic underfills would affect the accumulated damage in solder joints is also investigated. In Figs. 5.8 and 5.9, the accumulated damages within 3rd solder joint counting from the left are compared for the elastic and viscoelastic underfill materials. Six locations within the solder joint as found in Fig. 4.19 are referenced. Even though the viscoelastic underfill attenuates the propagating waves within the material itself (thus decreasing the accumulated damage slightly), this is not the case with the accumulated damage within the solder joints. As is seen in Fig. 5.8, location 1 fails almost at the same time by the dS11/dt power density wave, and the accumulated damage decreases from 68.3% to 55.5% for location 2, and from 28.2% to 8.08% for location 3. However, when S22/dt power density waves are considered as in Fig. 5.9, locations 1, 2, 4 and 6 all fail almost at the same time, with the accumulated damage for location 3 within the 3rd solder joint increasing from 9.6% to 41.5%. These results suggest that there is no guarantee for wave attenuation that would help alleviate accumulated damages employing viscoelastic underfill materials.



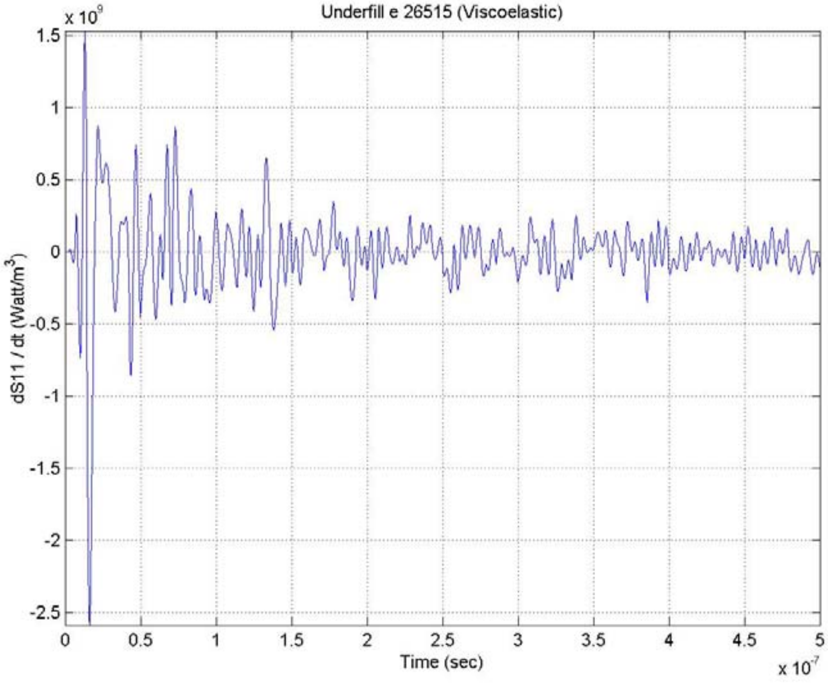
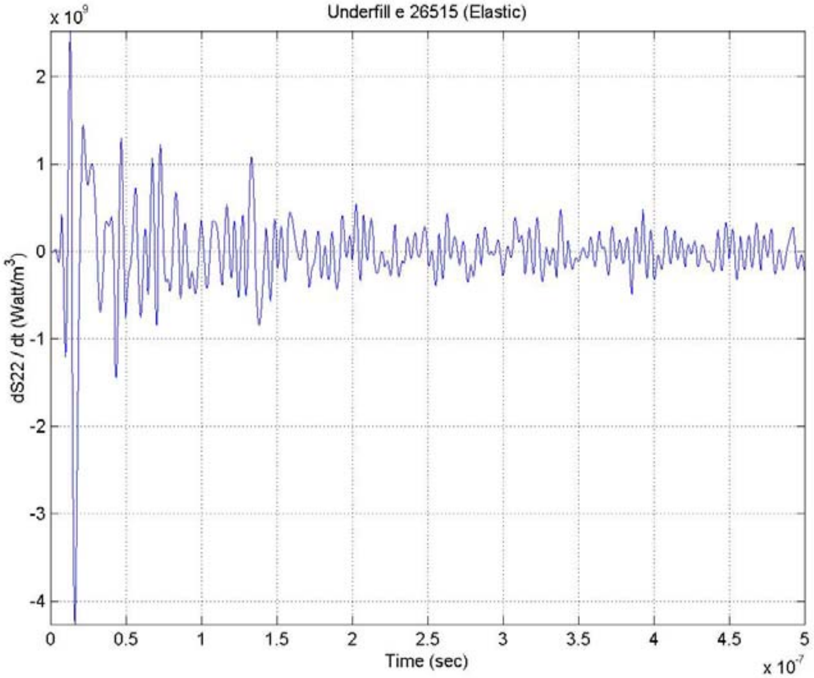


Fig. 5.2 dS11/dt power density waveforms at location U-1
(Elastic vs. Viscoelastic)



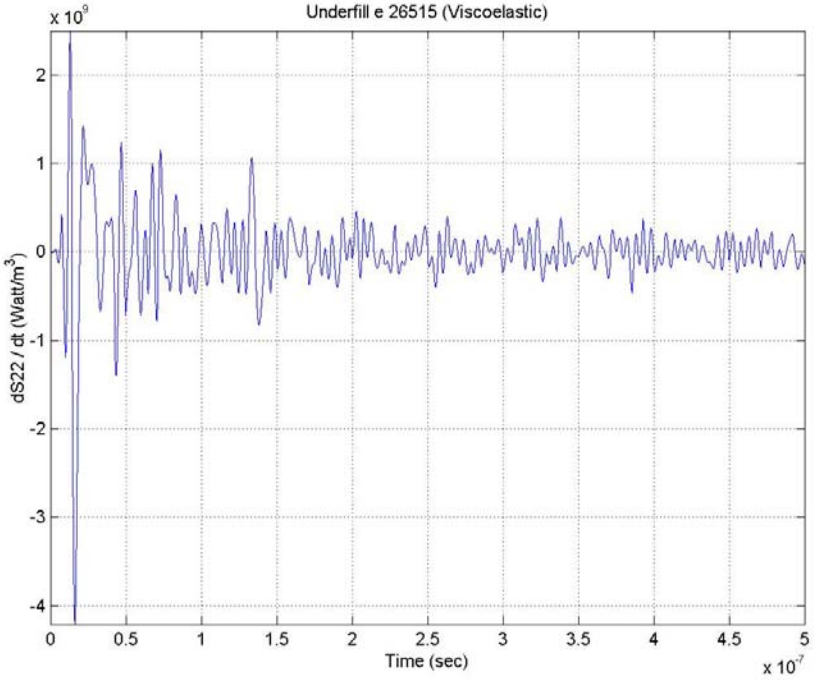
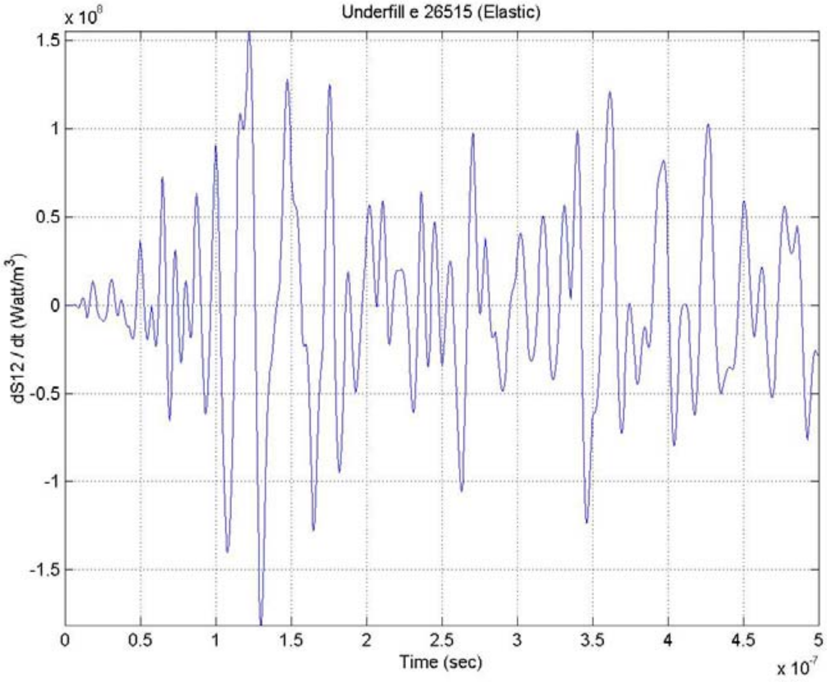


Fig. 5.3 dS22/dt power density waveforms at location U-1
(Elastic vs. Viscoelastic)



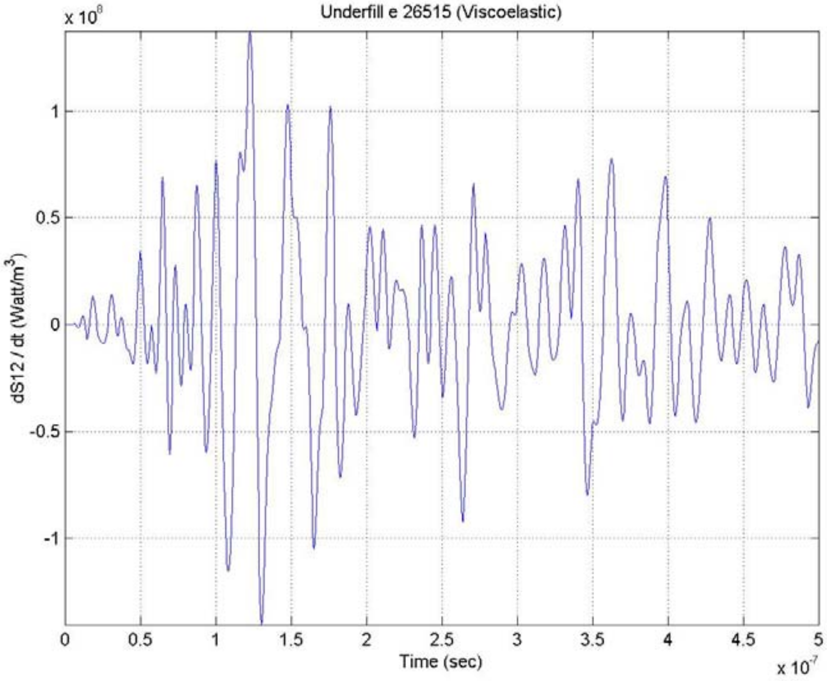


Fig. 5.4 dS12/dt power density waveforms at location U-1
(Elastic vs. Viscoelastic)

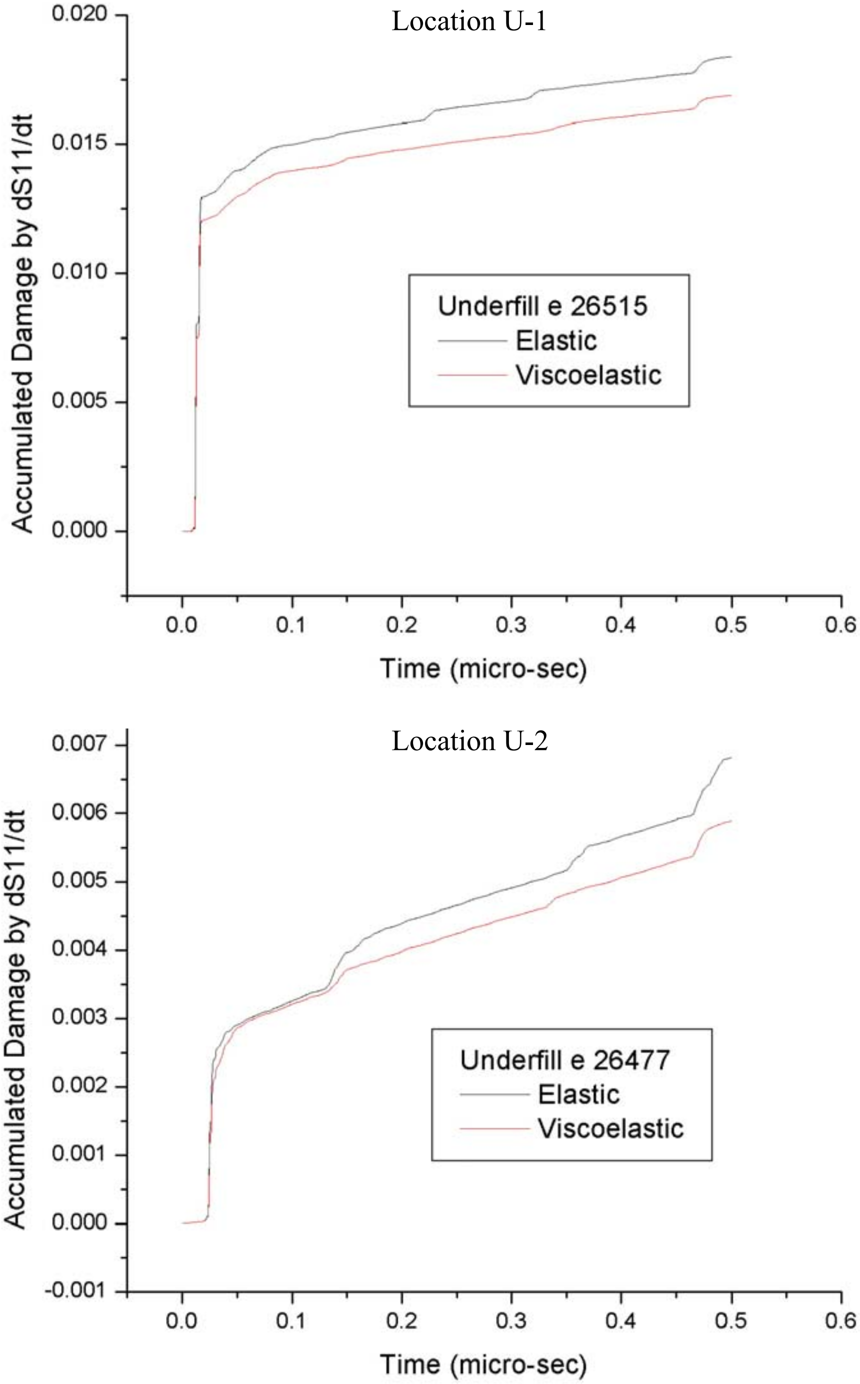
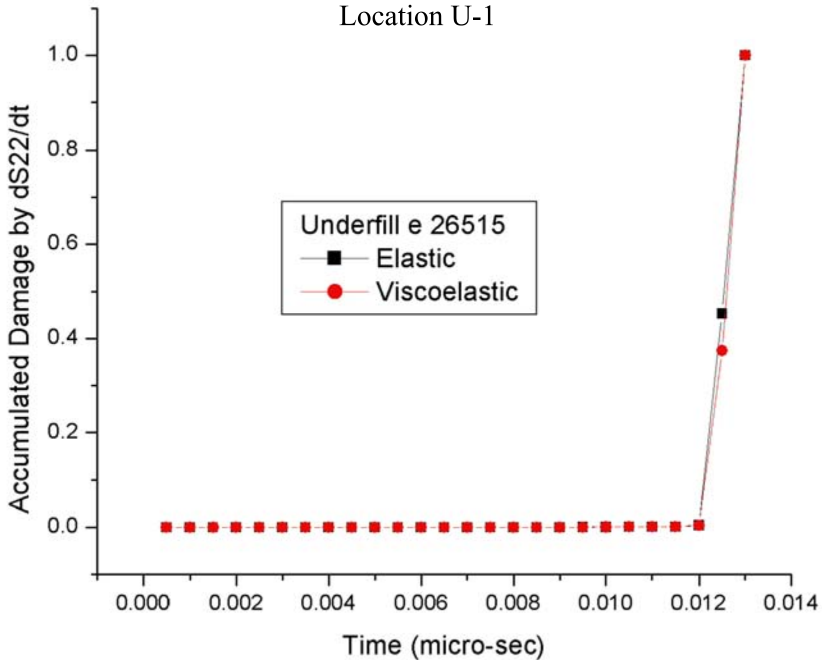


Fig. 5.5 Accumulated damage by dS11/dt
at locations within underfill
(Elastic vs. Viscoelastic)



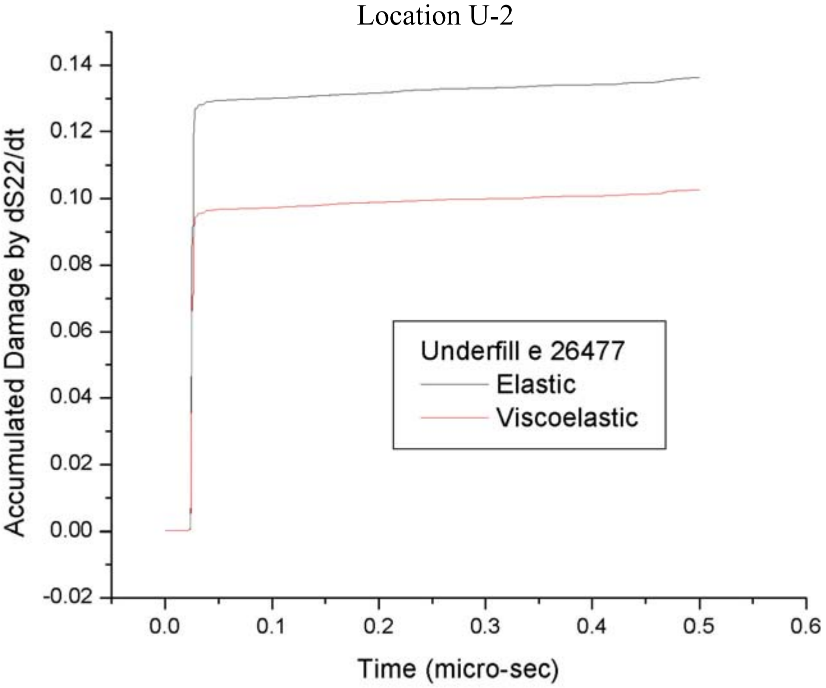


Fig. 5.6 Accumulated damage by dS22/dt
at locations within underfill
(Elastic vs. Viscoelastic)

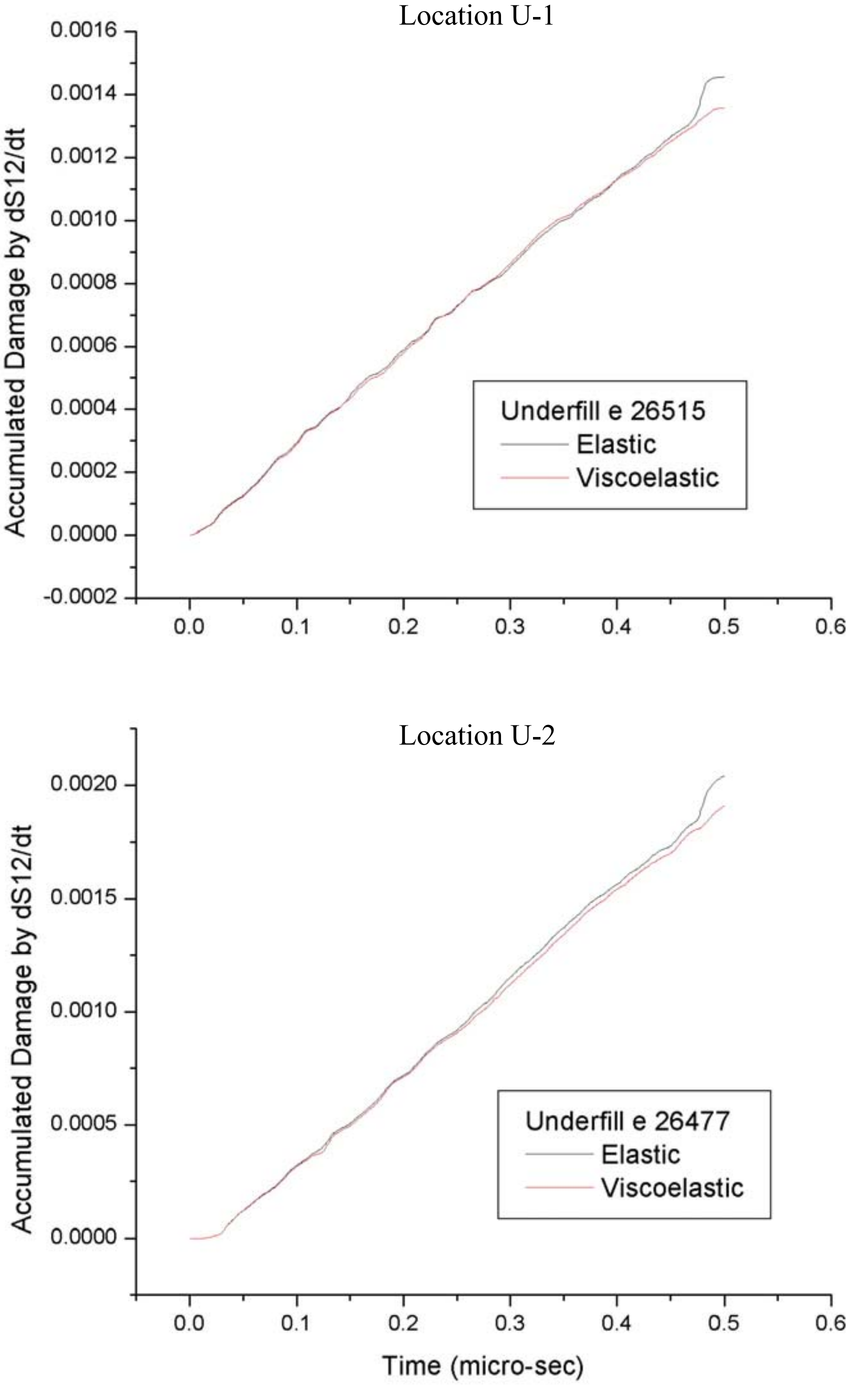
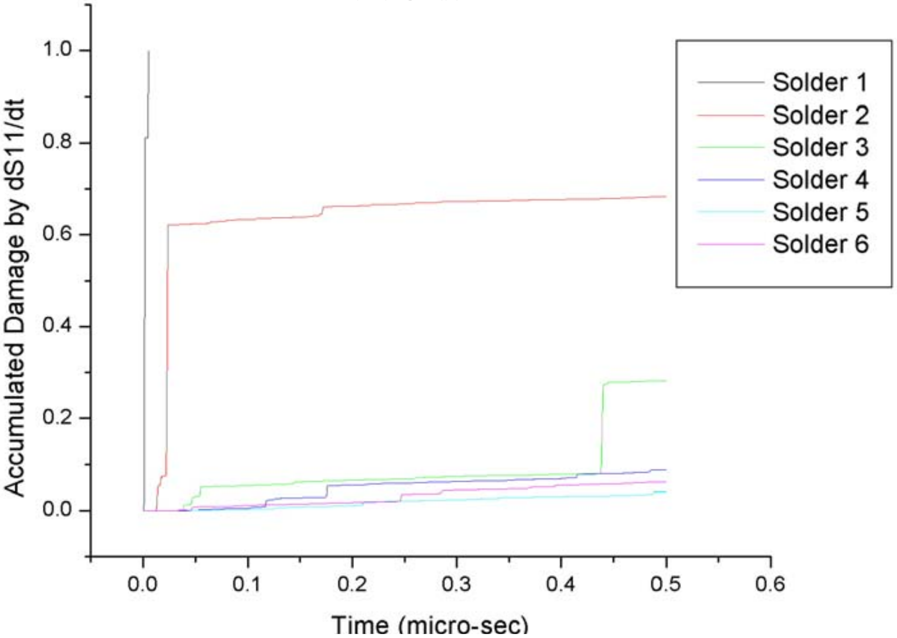


Fig. 5.7 Accumulated damage by dS12/dt
at locations within underfill
(Elastic vs. Viscoelastic)

Elastic Underfill



Viscoelastic Underfill

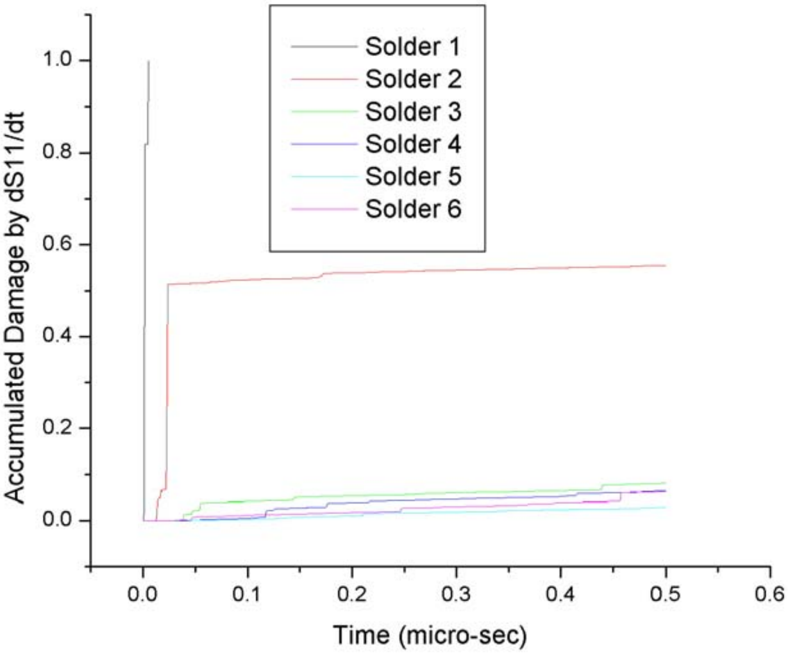
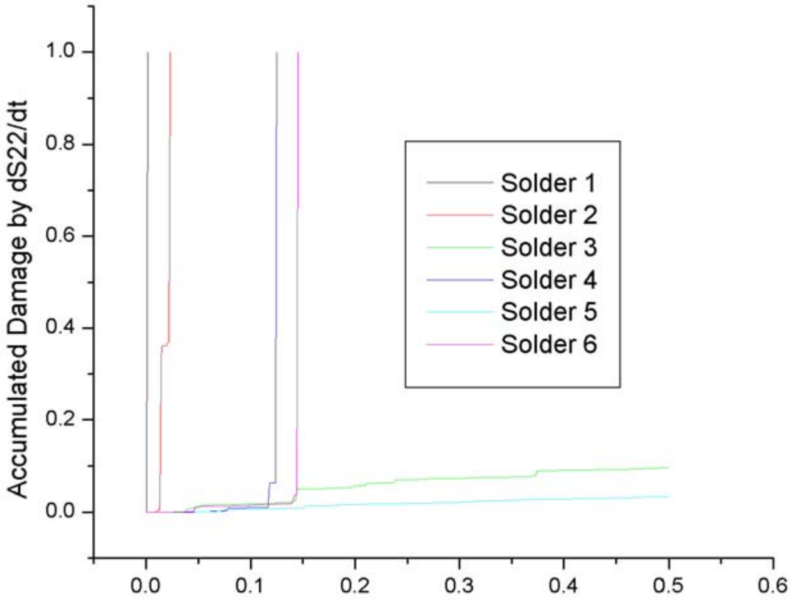


Fig. 5.8 Accumulated damage by dS11/dt
at locations within the 3rd solder joint
with elastic vs. viscoelastic underfill material


Elastic Underfill

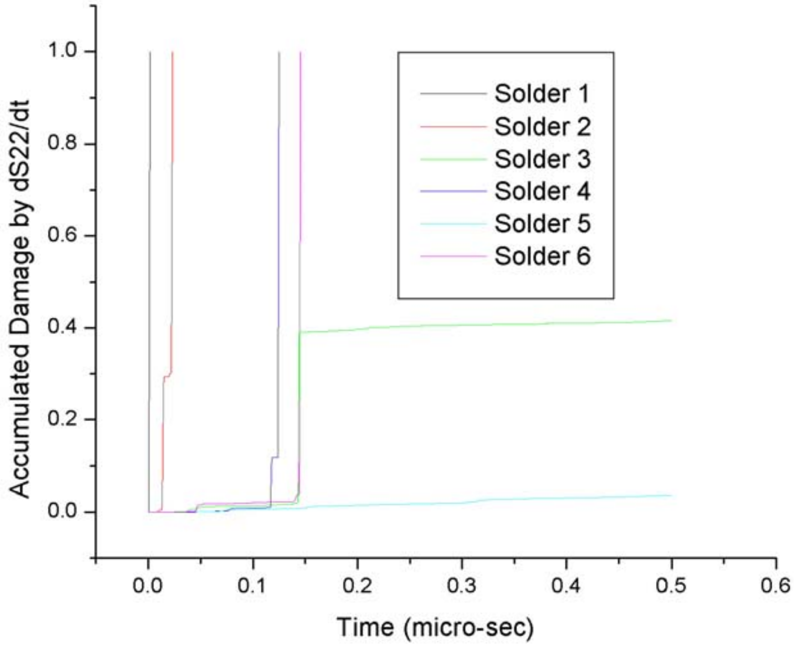

Viscoelastic Underfill

Fig. 5.9 Accumulated damage by dS22/dt
at locations within the 3rd solder joint
with elastic vs. viscoelastic underfill material

Since there are reflections from boundaries and various interfaces within the complex flip-chip configuration, it is not possible to trace the exact path of each wave in time. However, contrary to expectation, there is more accumulated fatigue damages by the dS22/dt wave at some solder joints when viscoelastic underfill material is incorporated. Except for certain locations in the solder joints, the underfill being viscoelastic demonstrates almost the same trend as the case with elastic underfills in general. In summary, wave attenuation in response to the employing of viscoelastic underfill material is found to be insignificant.

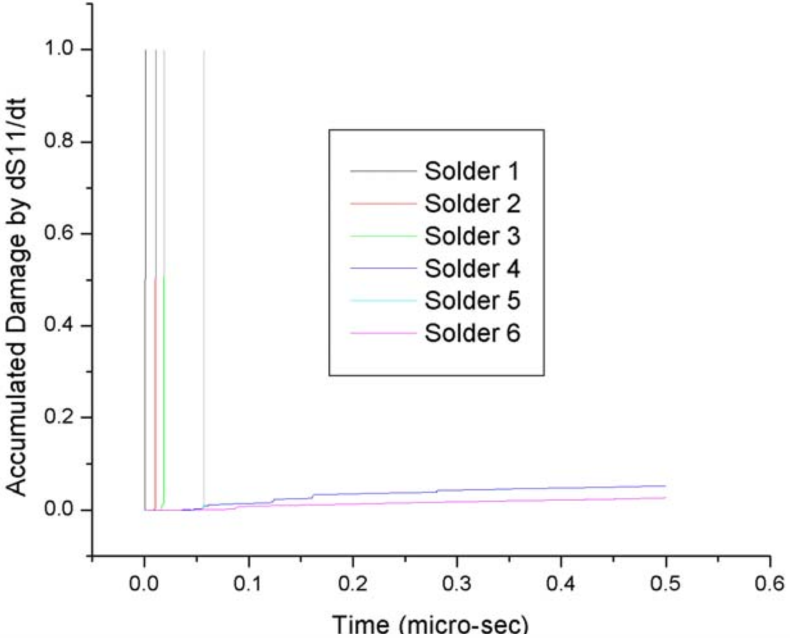
5.2 Optimal Material Characterization in Response to the Short-Time Scale Effect

In Chapter II, it was shown that there is an optimal material combination of E and CTE for the long-time scale thermal cycling tests. For specific fillers to be used for underfill materials, the flip-chip package showed different performance with various filler contents. In this section, how the flip-chip package responds at short-time scale to various underfill material combinations is investigated. Optimal material characterization for specific filler-matrix underfill is also studied.

Three (3) different filler-matrix systems for underfill were studied in Chapter II at long-time scale. Interestingly, among those fillers, silica(filler)-epoxy(matrix) underfill system showed maximized performance at around 85 wt% for the thermal cycling tests. The short-time scale response of the same silica filler underfill system is studied and optimal composition suggestion is then discussed. The basic material properties are the same as in Table 2.3. Material specs for different content of silica filler are plotted in Figs. 2.6, 2.7 and 2.8. Based on these silica-epoxy underfill systems, five (5) different underfill materials (with silica filler contents of 50 wt%, 60 wt%, 70 wt%, 80 wt% and 90 wt% for each) are incorporated for FEA simulation of wave propagation in the exact same way for the same flip-chip configuration as in Chapter III. Thus generated stress waves are interpreted again using the accumulated fatigue damage approach and the analyzed results are presented in Figs. 5.10-5.11. By dS11/dt power density wave, underfill systems with silica filler contents of 60 wt%, 70 wt% and 80 wt% show similar performance with three locations failing within the 3rd solder joint. When silica filler content is lowered to 50 wt%, another location of 5 fails by dS11/dt fatigue damage. Underfill system with silica filler content of 90 wt% shows the worst-case scenario by adding one more failing location (location 4). From the short-time scale effect's point of view, this combination is not recommended for flip-chip underfill system.

Similarly, by dS22/dt power density wave, silica filler 60 wt% and 70 wt% underfill systems show the best performance (three locations failed by accumulated damage). Five locations within the 3rd solder joints are identified to have high probability to fail by the dS22/dt wave for silica filler 80 wt% underfill system, and 90 wt% system shows the worst performance with all six locations expected to fail within less than 0.3 μsec. All results are summarized in Table 5.2 for comparison. To prevent short-time scale failure of wave-induced microcracking, underfill system with silica filler of 60 wt% or 70 wt% is recommended (70 wt% is slightly better) for the current flip-chip packaging configurations.

silica 50 wt% underfill



silica 60wt% underfill

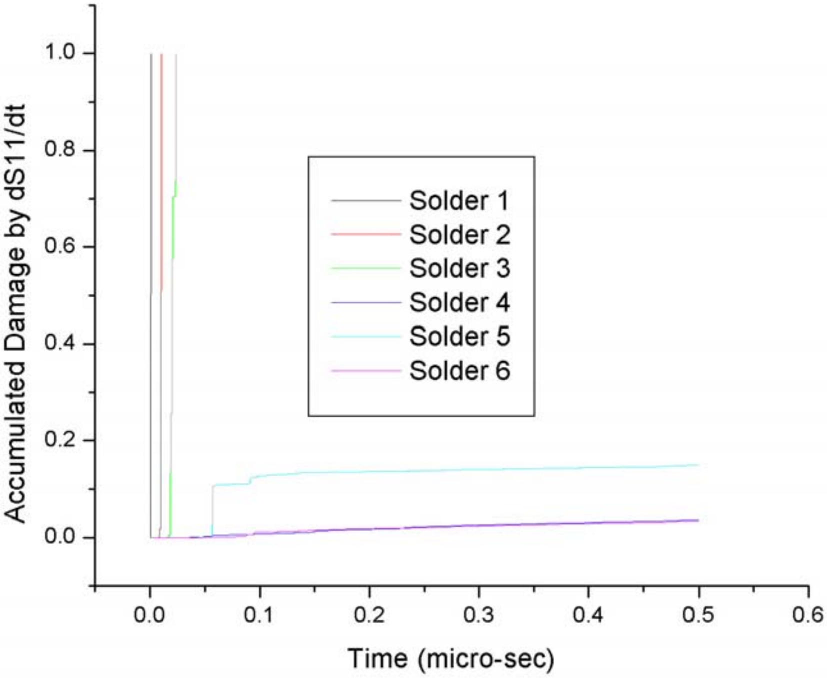
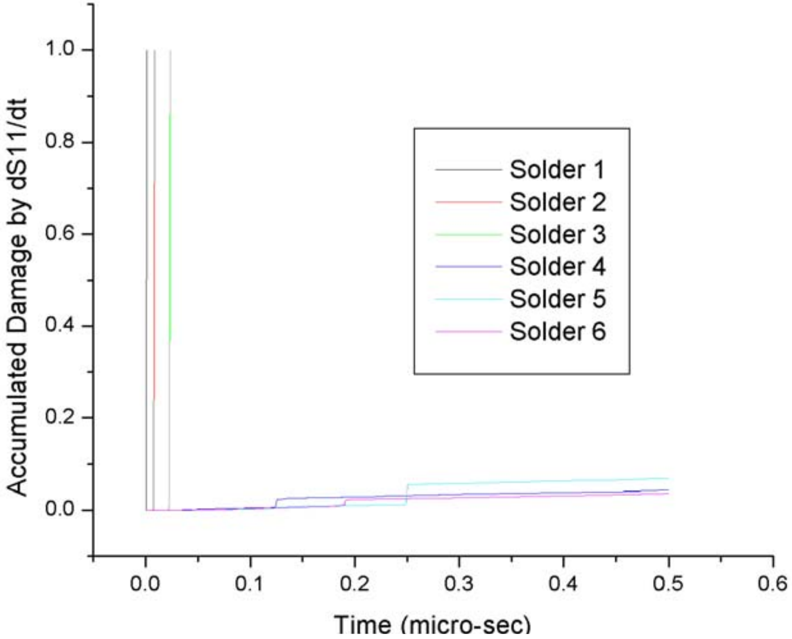


Fig. 5.10 Accumulated damage by dS11/dt
at locations within the 3rd solder joint with various silica filler contents

silica 70 wt% underfill



silica 80 wt% underfill

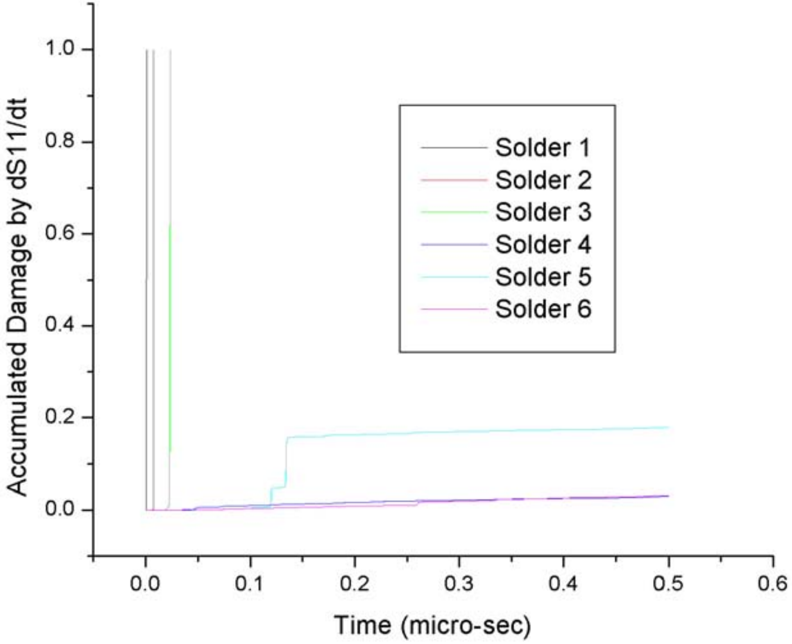
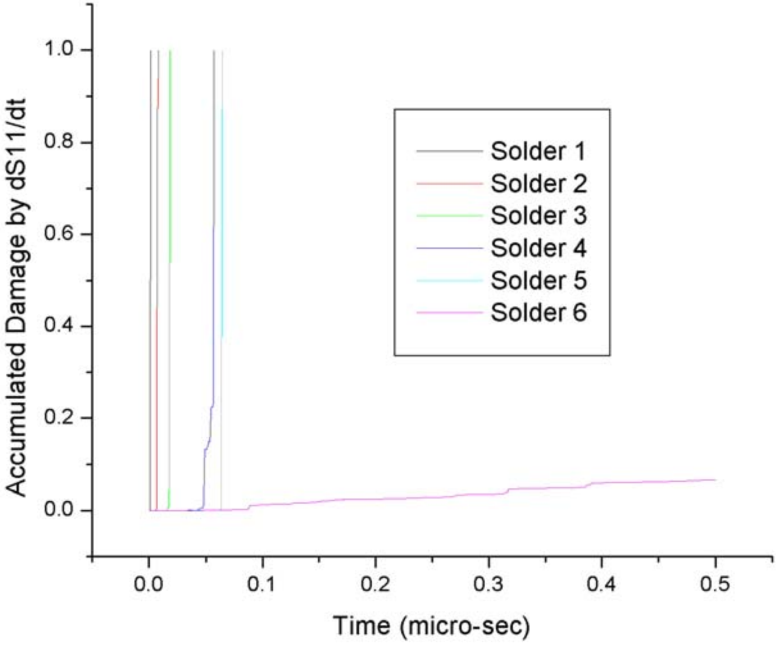


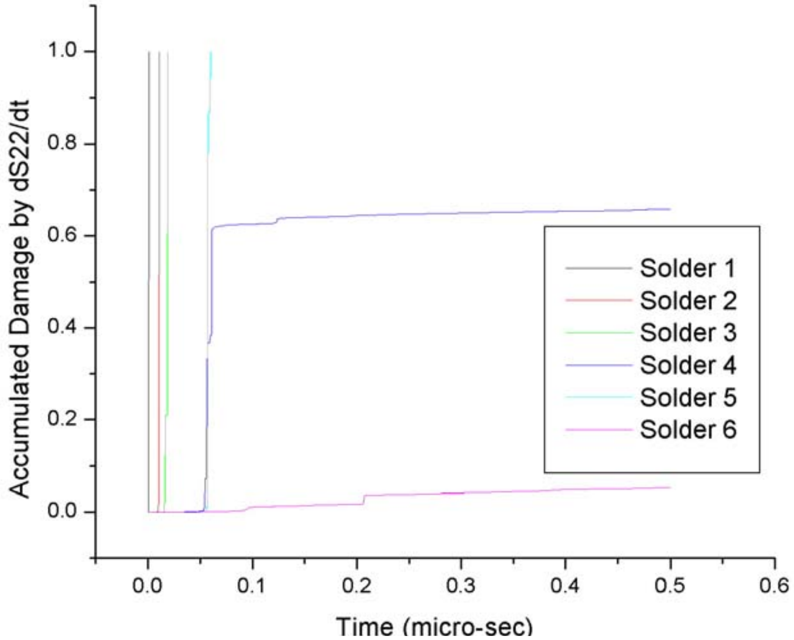
Fig. 5.10 Continued



silica 90 wt% underfill

Fig. 5.10 Continued

silica 50 wt% underfill



silica 60 wt% underfill

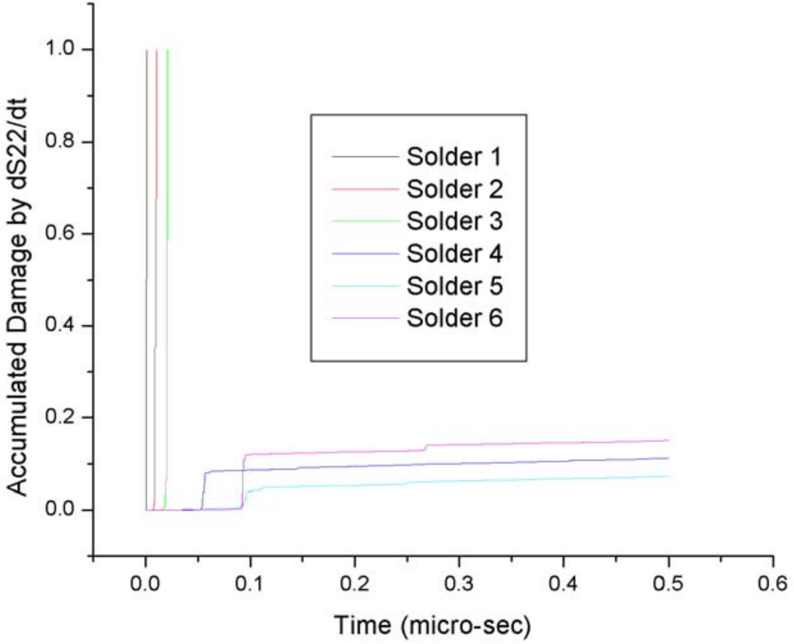
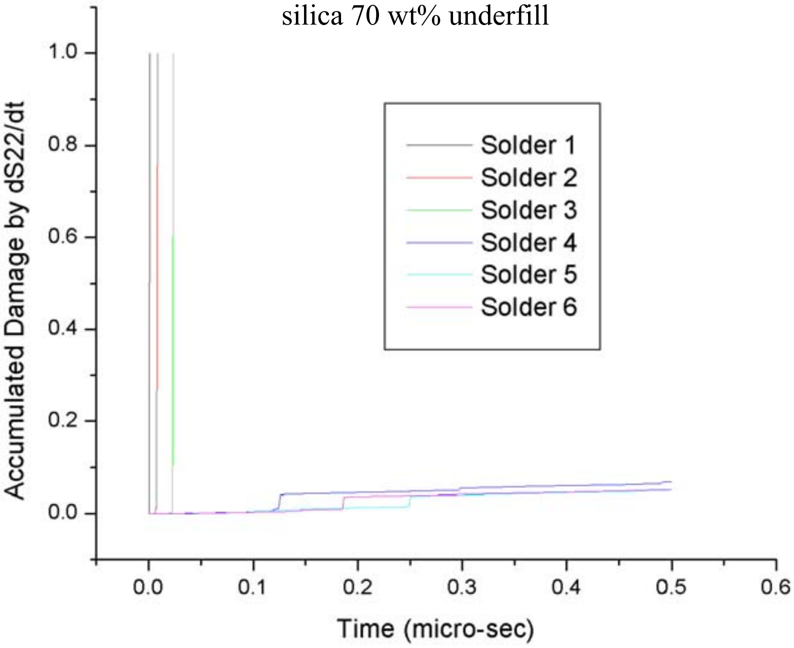


Fig. 5.11 Accumulated damage by dS22/dt
at locations within the 4th solder joint with various silica filler contents



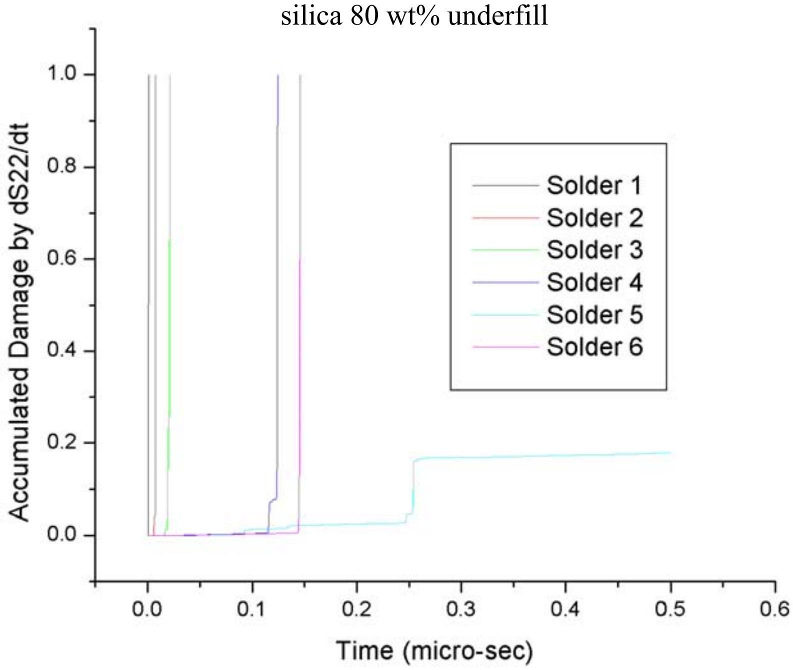


Fig. 5.11 Continued

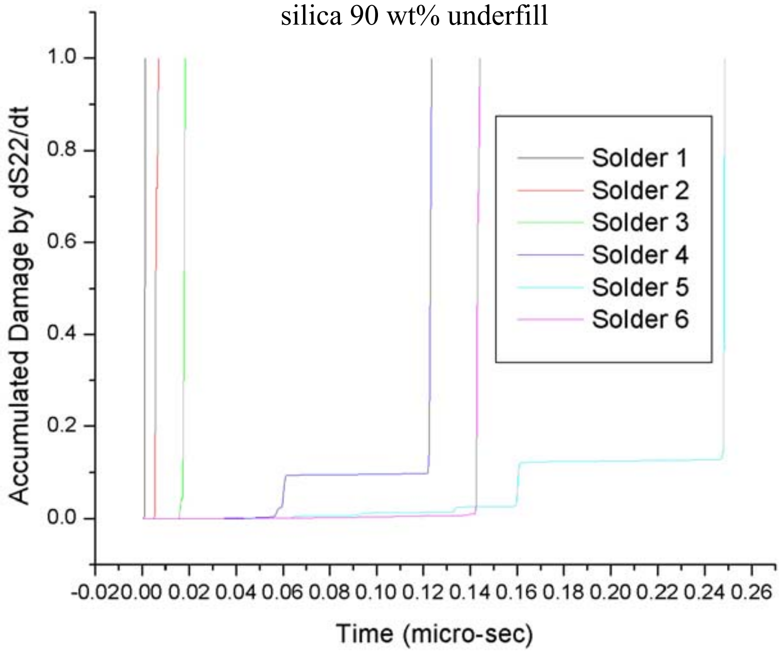


Fig. 5.11 Continued

Table 5.2 Accumulated fatigue damage within the 3rd solder joint
for different contents of silica filler within the underfill

Silica filler wt%	Number of failure locations within 3rd solder joint by accumulated fatigue damage	
	dS11/dt	dS22/dt
50	4	4
60	3	3
70	3	3
80	3	5
90	5	6

CHAPTER VI

SHORT-TIME SCALE EFFECT WITH DIFFERENT INTERCONNECTING MATERIALS

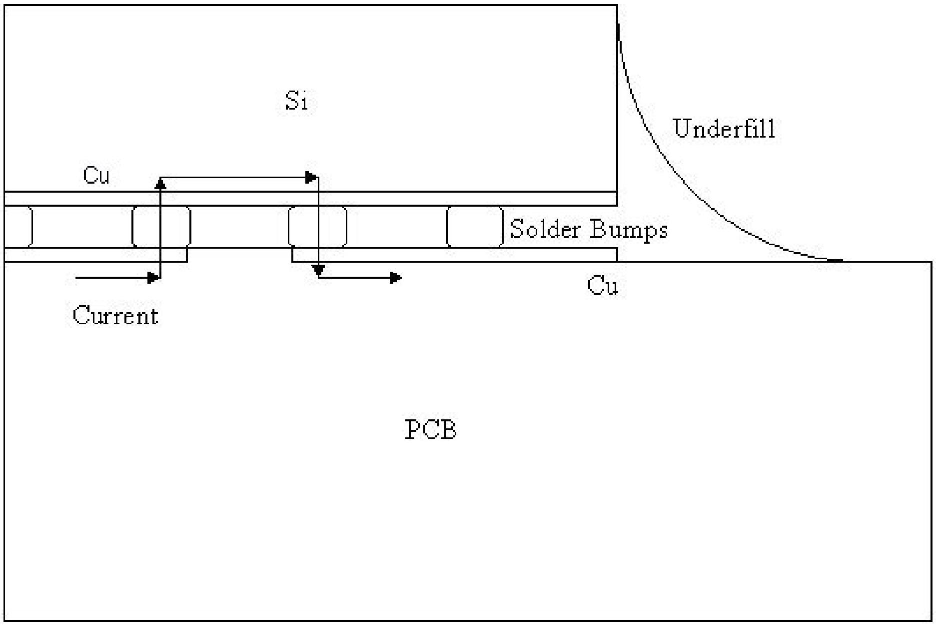
6.1 IC Transition from Al to Cu Interconnecting Layers

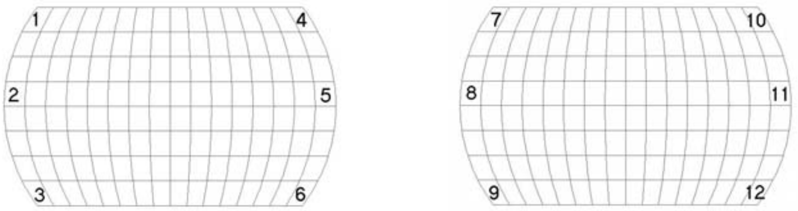
As Al is commonly used in IC devices as the conductor layer interconnecting in-chip components, investigations performed in Chapters II through V have not considered layer materials other than Al. However, recently Cu has been quickly replacing Al in the electronic packaging industry. Although Al is a good conductor compatible with silicon materials, it quickly forms a robust, chemically stable and electrically insulating oxide that creates a connection challenge [20]. Al oxide is easily removed in the wire bonding process, thus rendering a reliable connection. However, given the thin, fragile layers in ICs, Al is not easily soldered. There are only a handful of bumping processes that can be used directly with Al. Many fabricators have converted from Al to Cu and several developments in the past few years have resolved the numerous problems associated with using copper metal in place of aluminum as the interconnect metal. Cu is more conductive than Al and it allows higher frequencies to be used with smaller line width. In the following, Cu is used in place of Al as the interconnect material. Procedures followed in Chapters III and IV are again engaged to investigate the implication of employing Cu as the interconnect material from the short-time scale perspective.

6.2 Wave Propagation in Flip-Chip with Cu Layers

In Fig. 6.1, the flip-chip configuration is shown with Cu layers. The same FE mesh in Fig. 3.2 is used and the same material properties tabulated in Tables 2.2 and 3.1-3.2 are incorporated. Because it has 69% higher thermal conductivity and 60% higher electrical conductivity than Al, Cu would generate less heat by Joule heating and be more effective in conducting heat than would Al. These differences in material property are expected to have some noticeable effects on short-time scale wave motion. In Fig. 6.2, the ECDM contour inside the flip-chip in response to a 0.5A current flow is illustrated for the two interconnect materials. It can be seen that the maximum ECDM corresponding to Cu layer is reduced by 22% at the corner of the 3rd solder joint which is directly affected by the large rapid transient thermal gradient. In Figs. 6.3 - 6.5, normal and shear power density waves extracted at the location 1 of the 3rd solder joint (Fig. 6.1) are plotted. It is seen that the difference between the two material cases is as much as one order-of-magnitude. The corresponding STFT time-frequency analysis results shown in Figs. 6.6 to 6.8 again show the characteristics of being dispersive and broadband, and the initial high frequencies ranging up to 600 MHz are seen attenuated to below 300 MHz within the (short) time window of observation.

The magnitudes and frequency responses of the power density waves corresponding to the Al and Cu layer were briefly examined. To evaluate the effects of these power density waves, it is also needed to evaluate the accumulated damage by fatigue loadings these power density waves could be capable of inducing. The same principle of decomposing the power density waves into multiple signals with dominant frequencies at a particular time and evaluating the accumulated damages by each power density wave is applied. For the locations within the 3rd and 4th solder joints in Fig. 6.1, the estimated accumulated damages by the normal and shear power density waves are plotted in Figs. 6.9 to 6.14 for both Al and Cu layers. Although the corresponding time-frequency responses all assume similar trends, as the power density waves with the Cu layer are of small magnitude compared to those with the Al layer, the induced accumulated damages are expected to be small compared to the cases with Al.

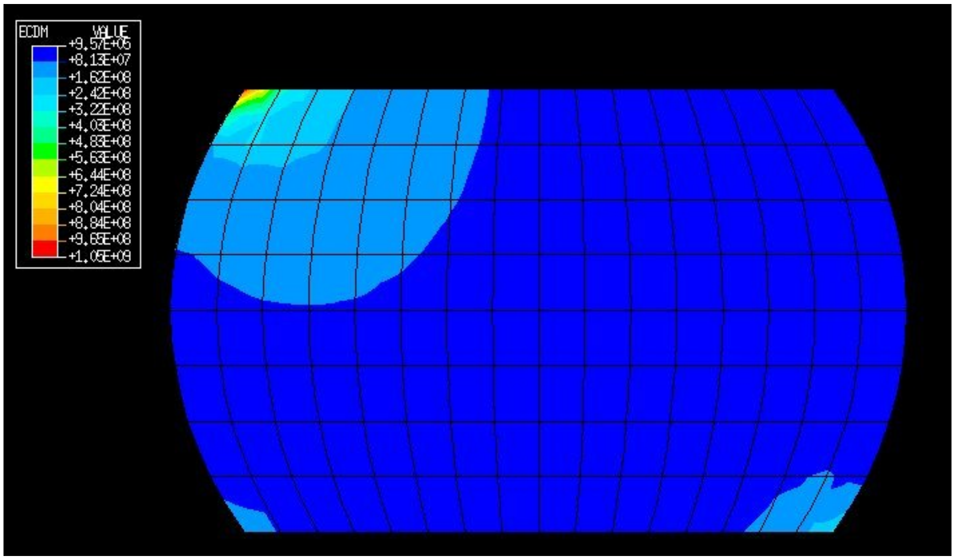




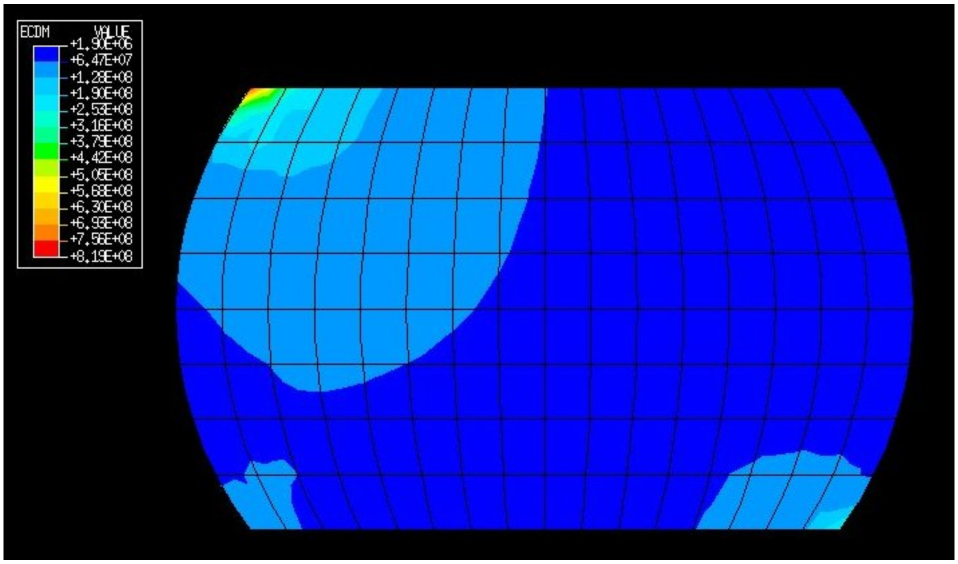
3rd solder joint

4th solder joint

Fig. 6.1 Flip-Chip configuration (Cu top layer)
and locations for accumulated damage estimation

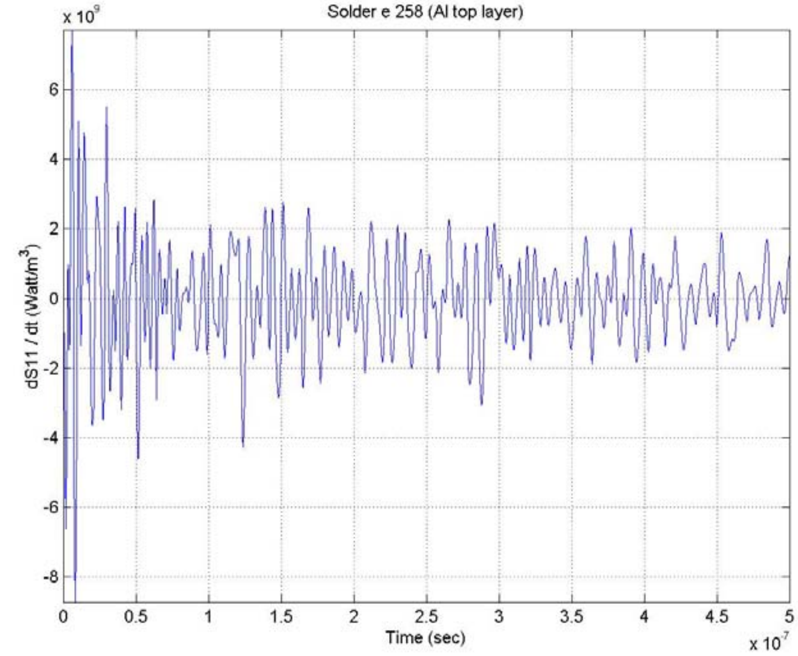


(a) ECDM contour in the 3rd solder joint
with Al top layer

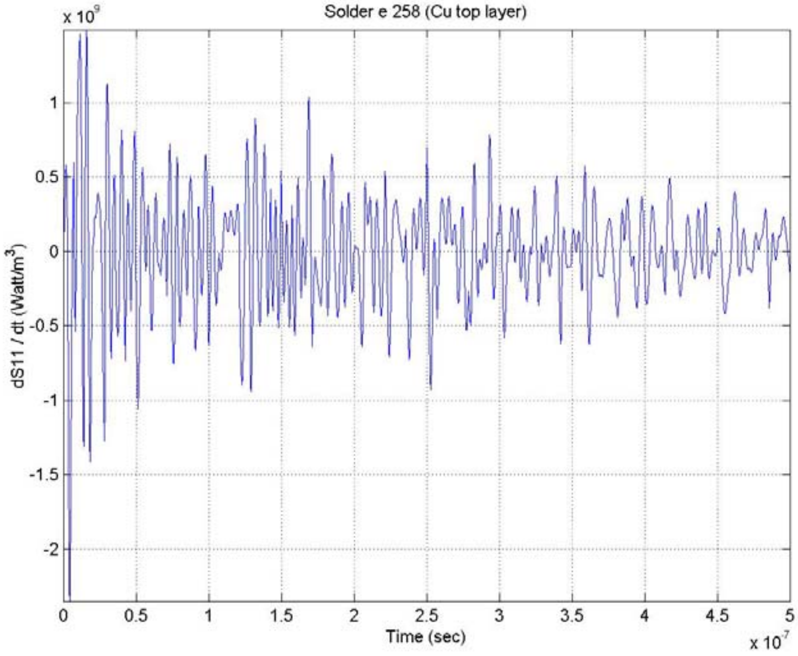


(b) ECDM contour in the 3rd solder joint
with Cu top layer

Fig. 6.2 ECDM contour inside flip-chip

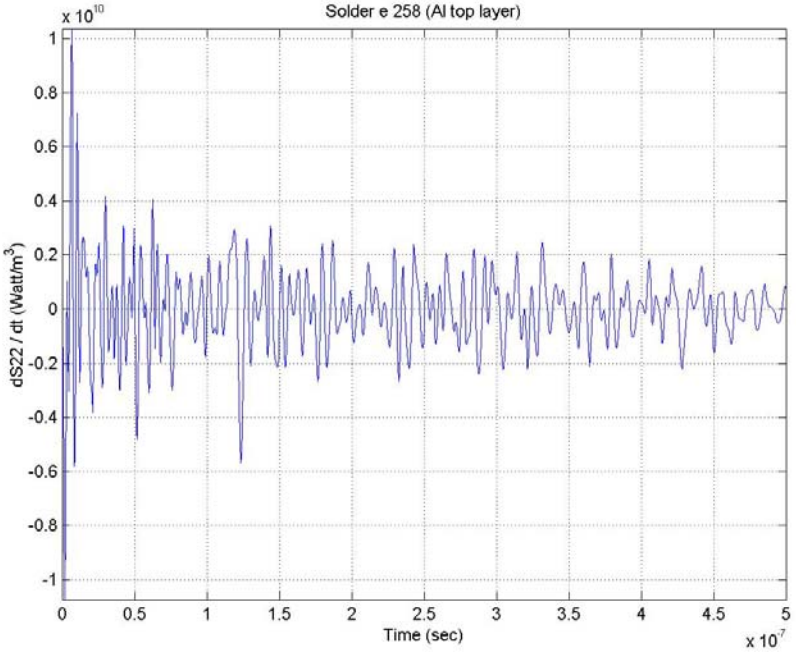


(a) Al top layer

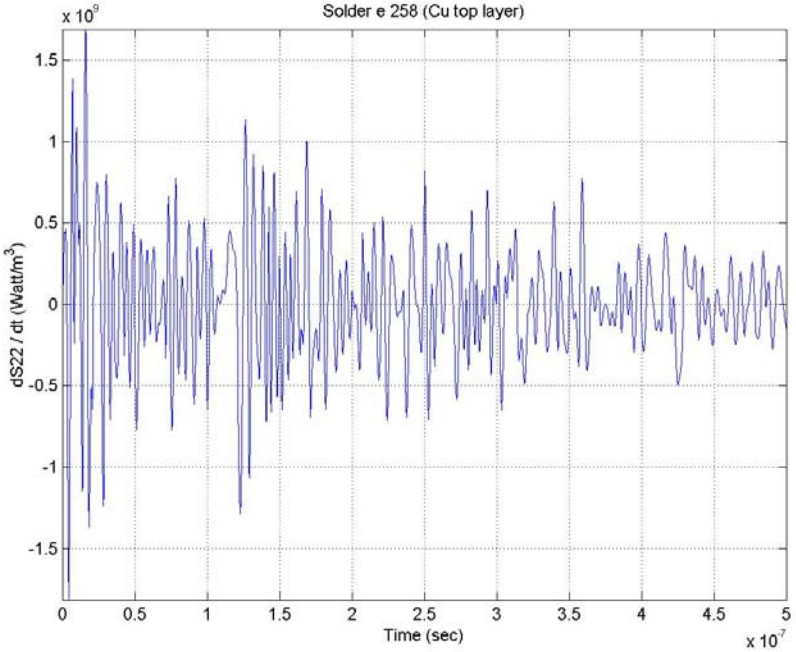


(b) Cu top layer

Fig. 6.3 dS11/dt power density wave at location 1 of the 3rd solder joint

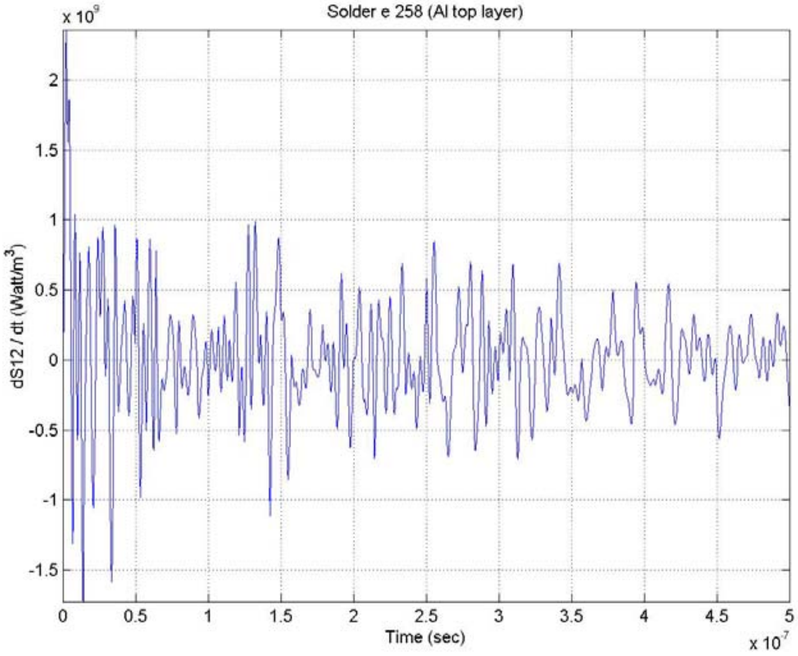


(a) Al top layer

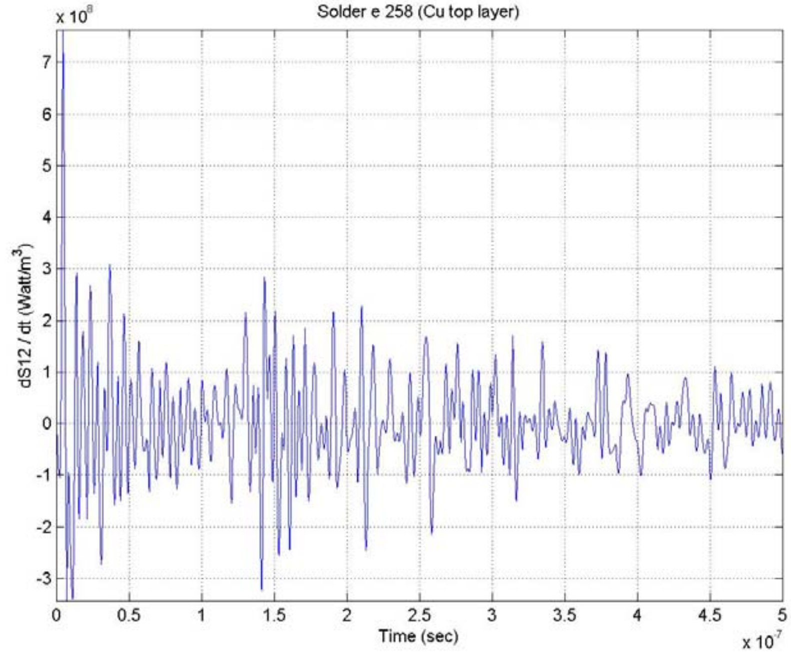


(b) Cu top layer

Fig. 6.4 dS22/dt power density wave
at location 1 of the 3rd solder joint

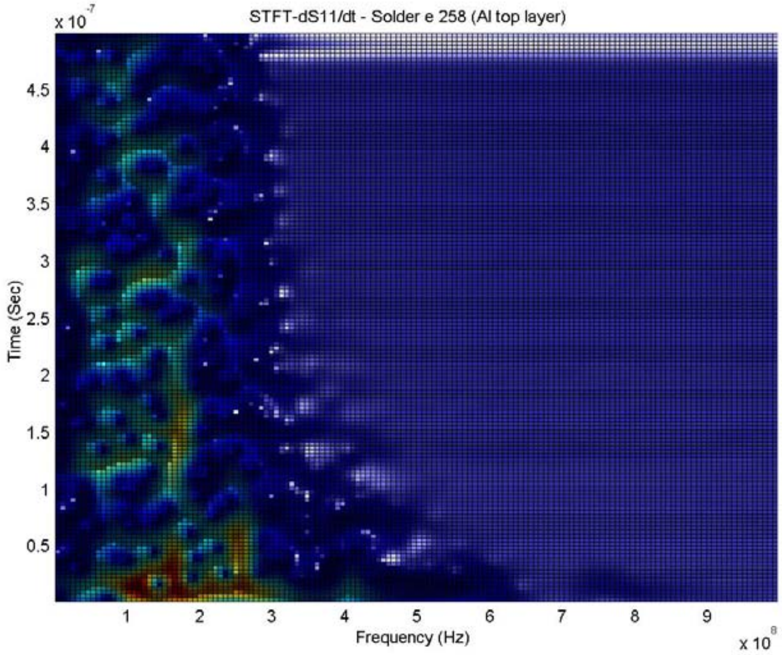


(a) Al top layer

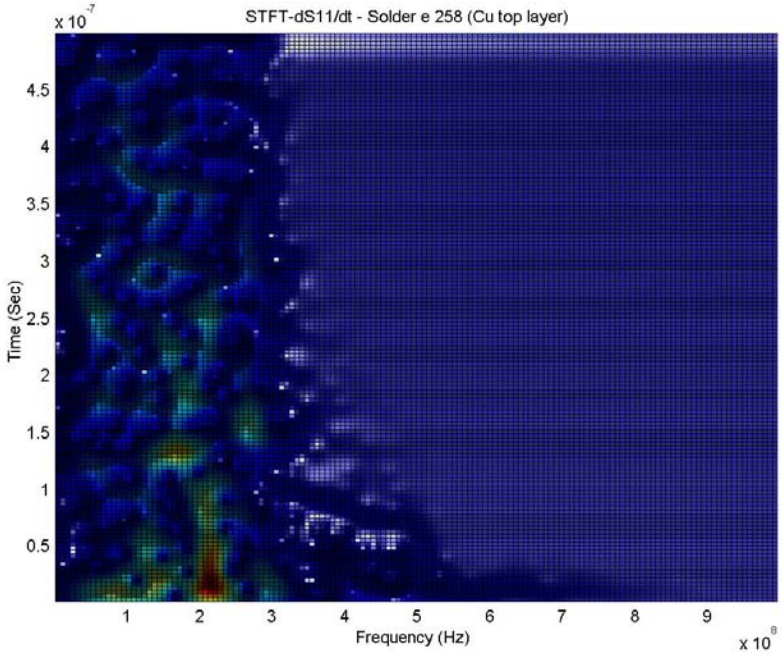


(b) Cu top layer

Fig. 6.5 dS12/dt Power density wave
at location 1 of the 3rd solder joint

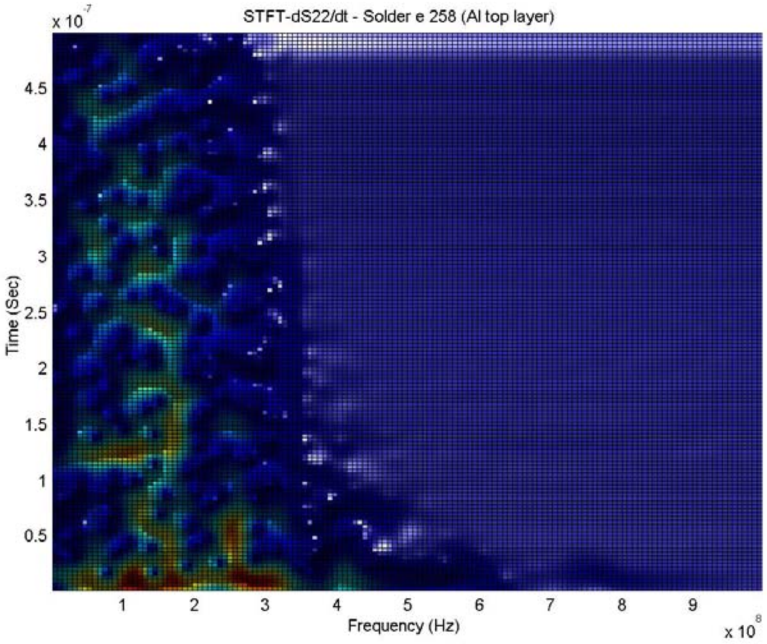


(a) Al top layer

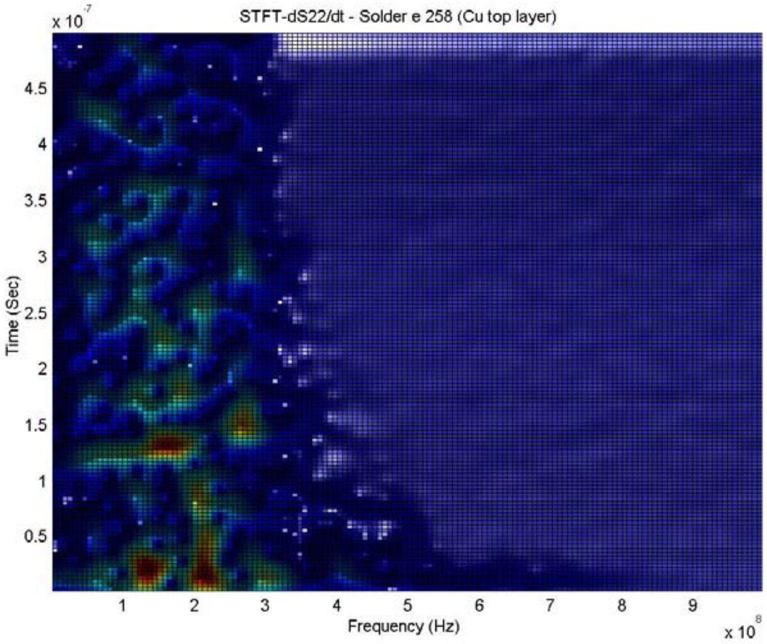


(b) Cu top layer

Fig. 6.6 STFT analysis of dS11/dt wave
at location 1 of the 3rd solder joint

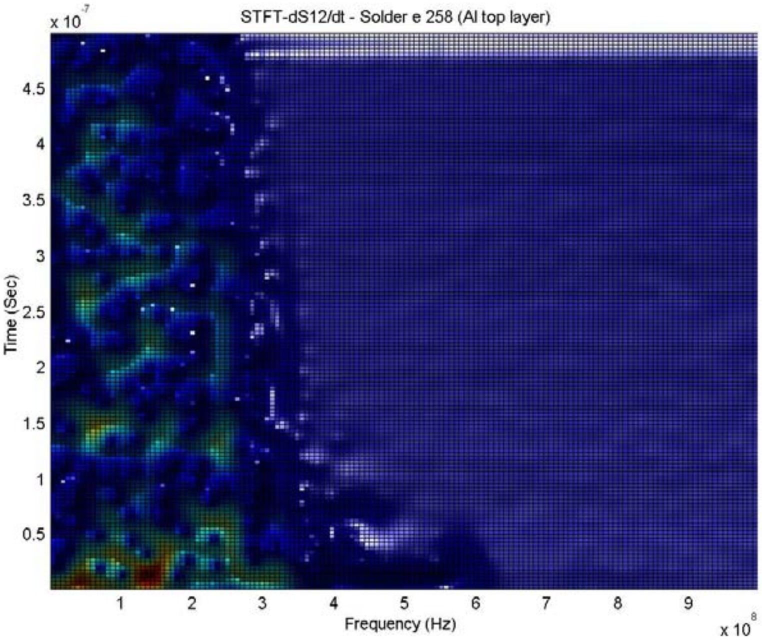


(a) Al top layer

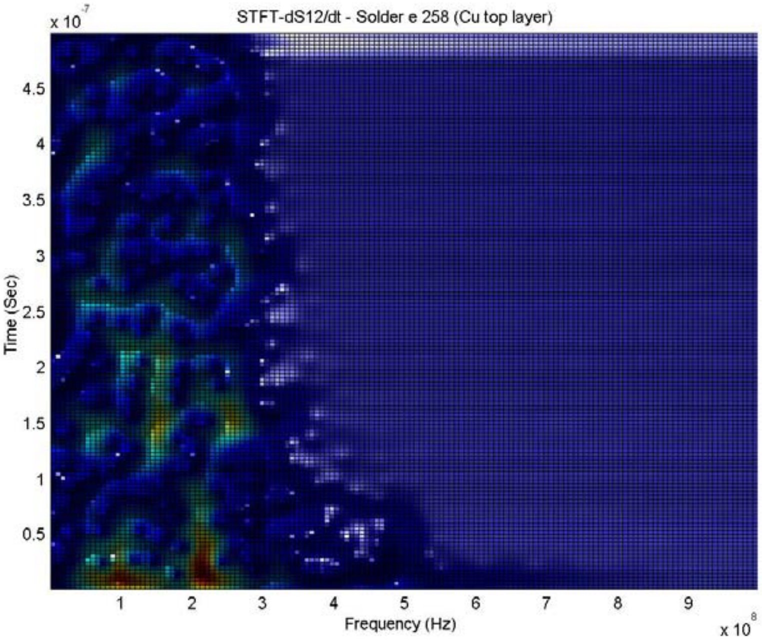


(b) Cu top layer

Fig. 6.7 STFT analysis of dS22/dt wave at location 1 of the 3rd solder joint

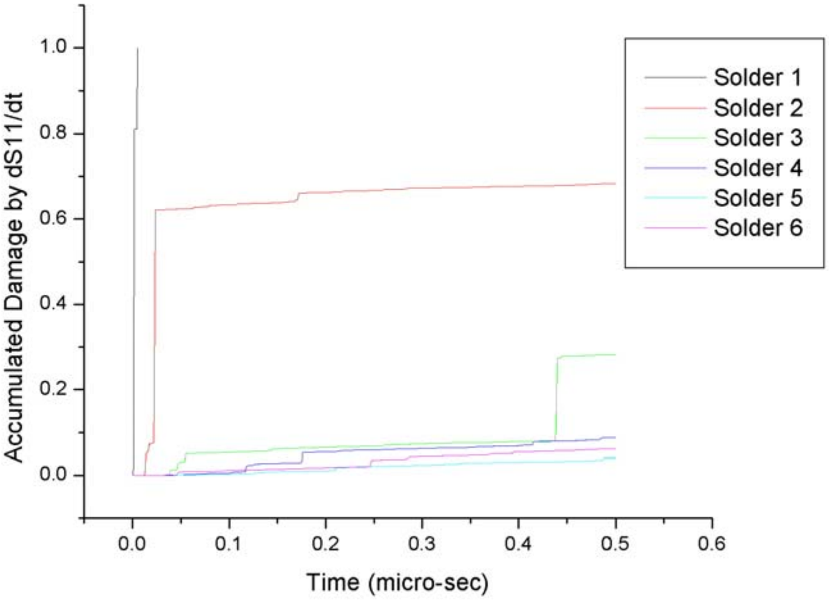


(a) Al top layer

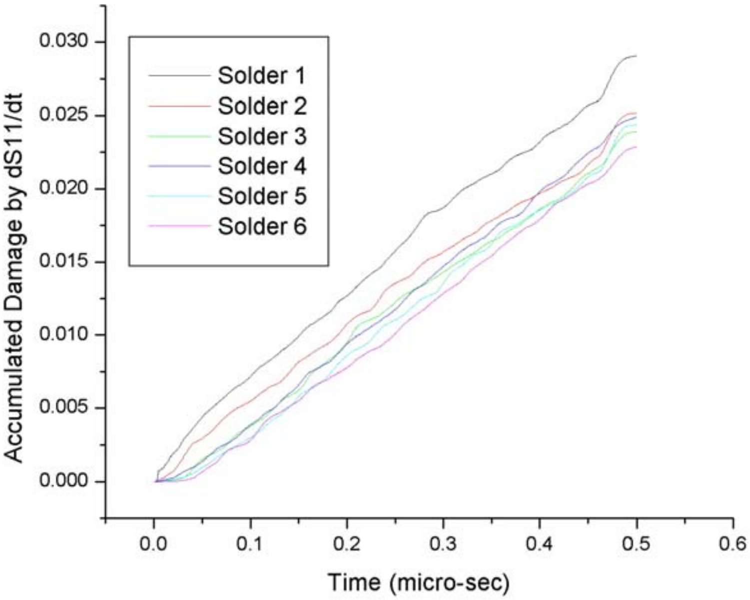


(b) Cu top layer

Fig. 6.8 STFT analysis of dS12/dt wave
at location 1 of the 3rd solder joint

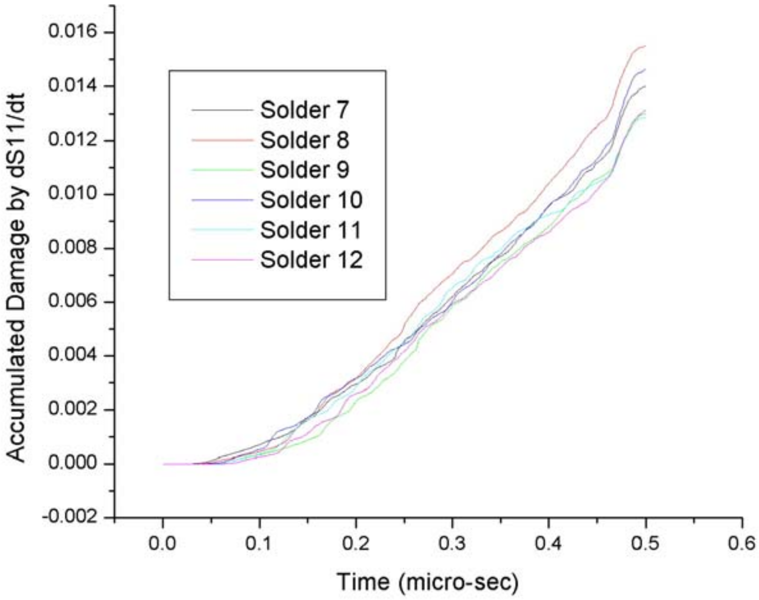


(a) Al top layer

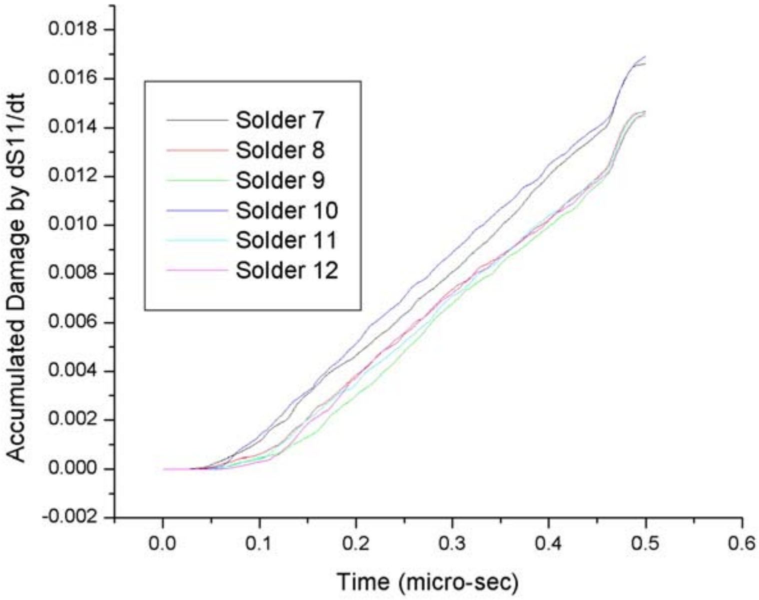


(b) Cu top layer

Fig. 6.9 Accumulated damage by dS11/dt at locations within 3rd solder joint

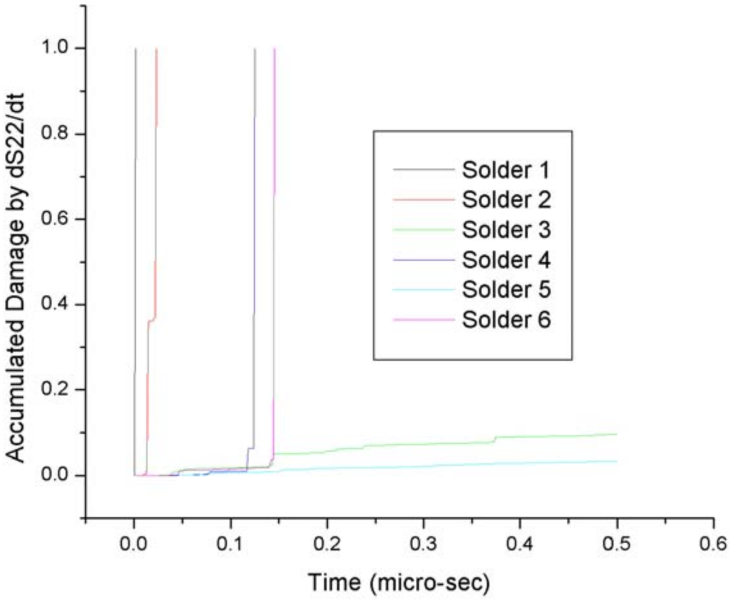


(a) Al top layer

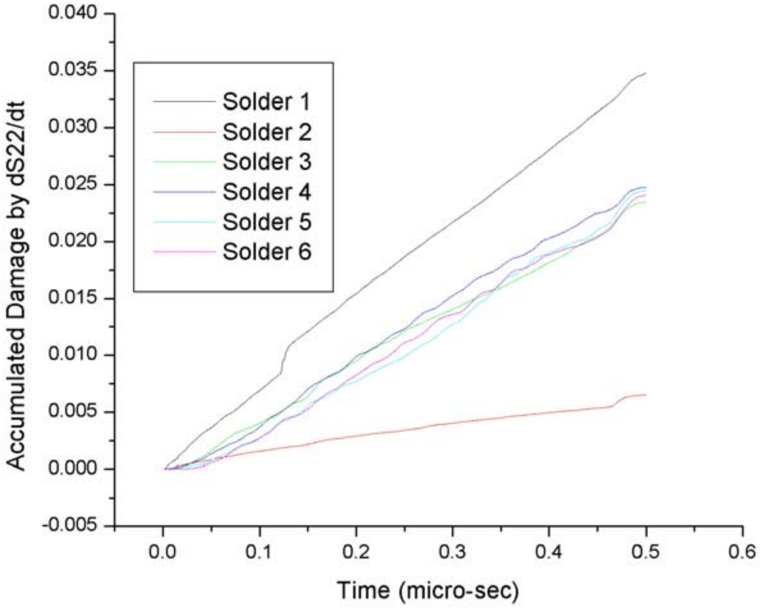


(b) Cu top layer

Fig. 6.10 Accumulated damage by dS11/dt
at locations within 4th solder joint

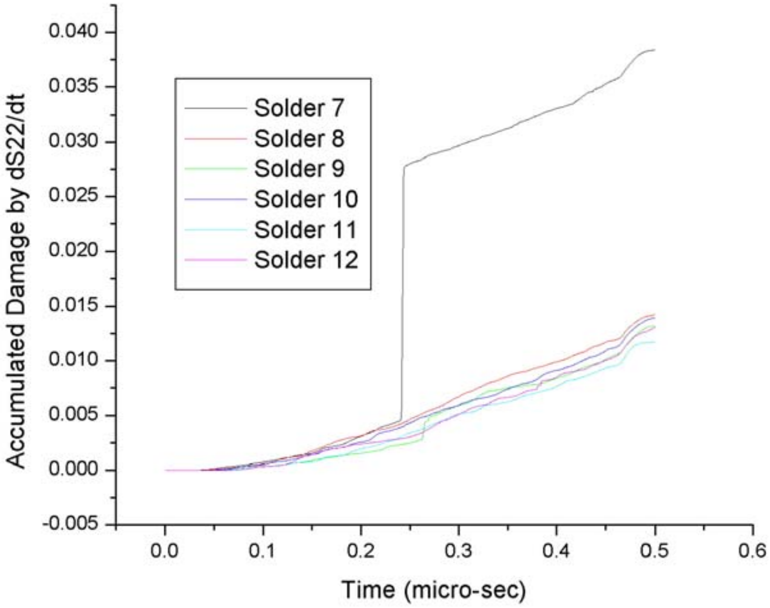


(a) Al top layer

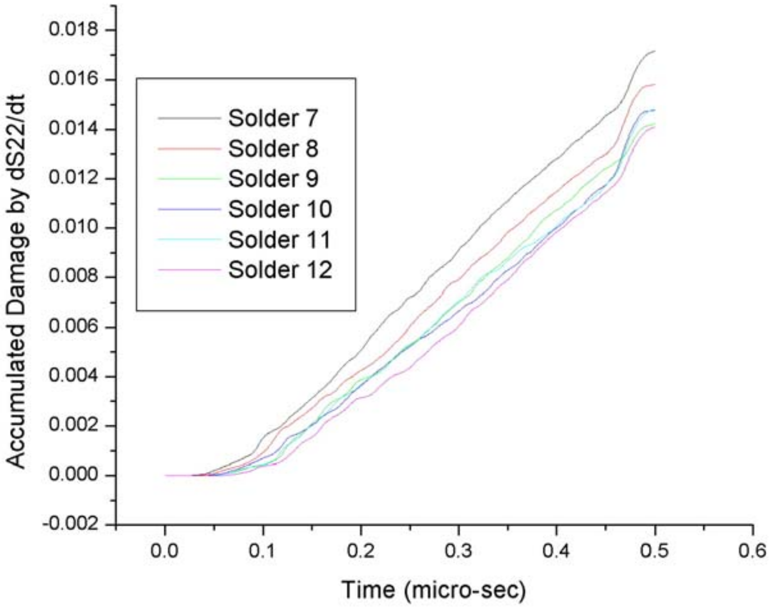


(b) Cu top layer

Fig. 6.11 Accumulated damage by dS22/dt
at locations within 3rd solder joint

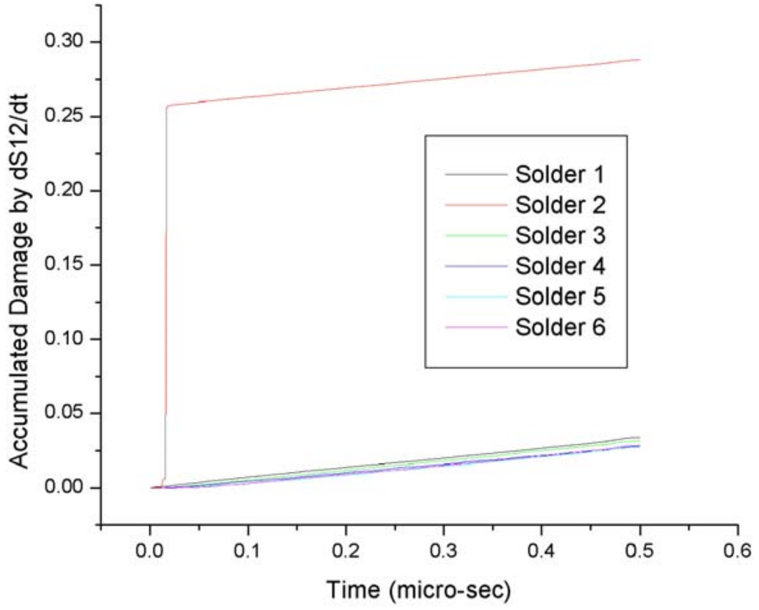


(a) Al top layer

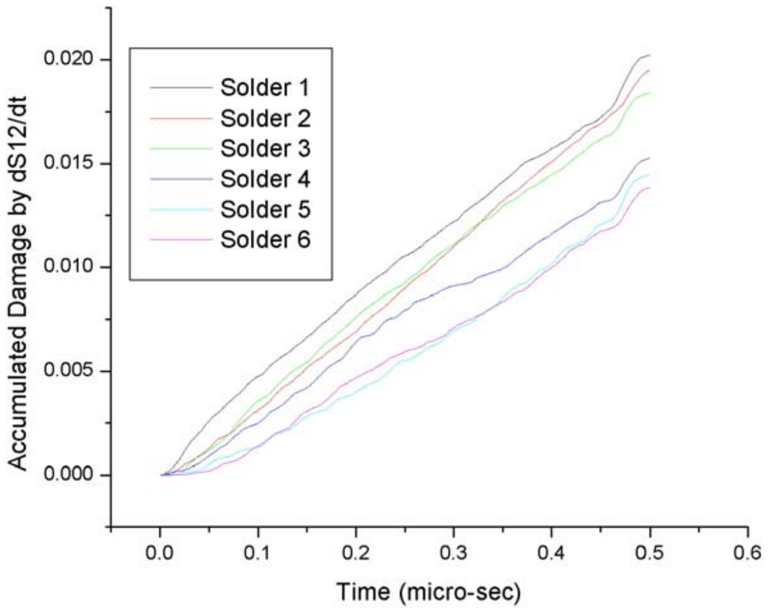


(b) Cu top layer

Fig. 6.12 Accumulated damage by dS22/dt at locations within 4th solder joint

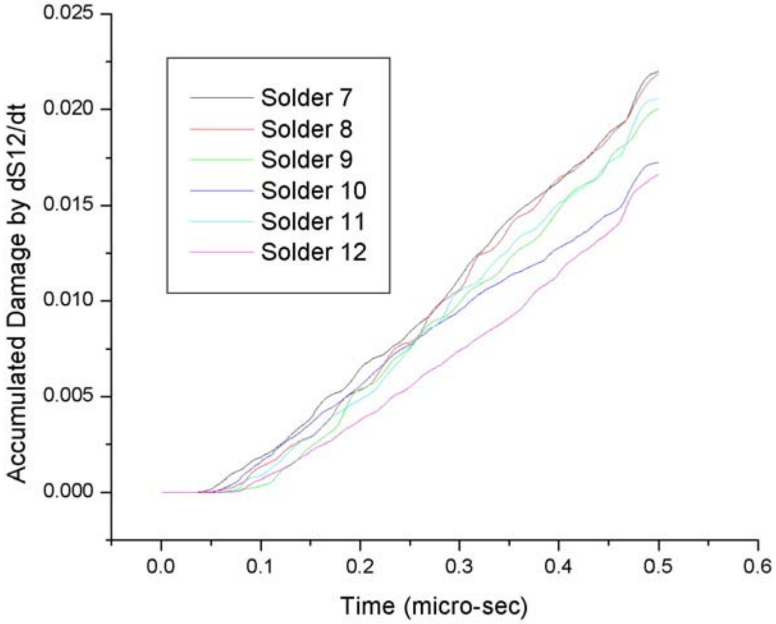


(a) Al top layer

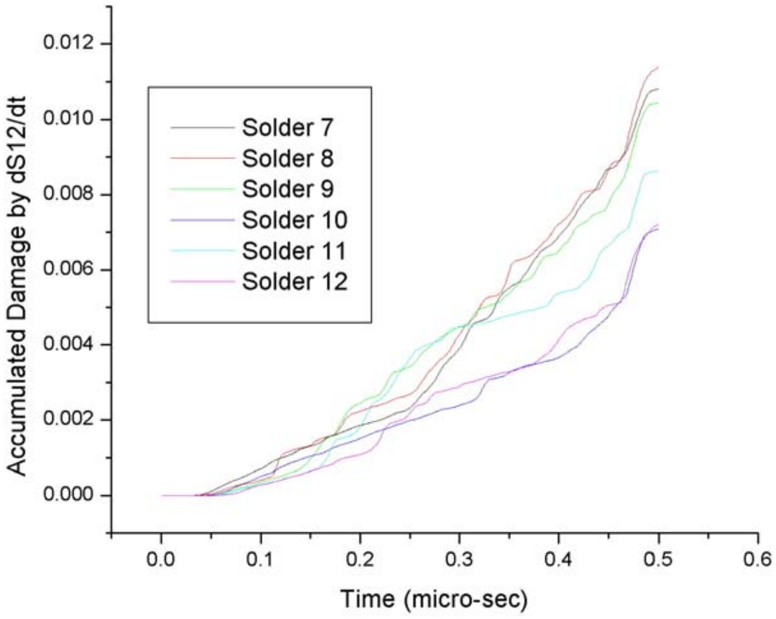


(b) Cu top layer

Fig. 6.13 Accumulated damage by dS12/dt
at locations within 3rd solder joint



(a) Al top layer



(b) Cu top layer

Fig. 6.14 Accumulated damage by dS12/dt
at locations within 4th solder joint

This is confirmed in Figs. 6.9 to 6.14. Within the 3rd solder joint, two locations fail by the dS11/dt wave with Al layers: However, no location fails with Cu layers, with the maximum accumulated damage being only 3%. For the 4th solder joint, the estimated accumulated damage by the dS11/dt wave is in the same range (less than 2%) as the 3rd solder joint. By the dS22/dt wave, four locations fail within the 3rd solder joint with Al layers. However, none of the locations fail with Cu layers in which the maximum accumulated damage is less than 4%. For the 4th solder joint, the accumulated damage by the dS22/dt wave would not be of concern for both Al and Cu layers. The dS12/dt wave does not deliver much damage with Al layers for the 3rd and 4th solder joint where 28.8% maximum accumulated damage within the 3rd solder joint is observed. In addition, the estimated damage values are even less with the Cu layer case.

6.3 Discussion and Problems with Cu as Interconnecting Material

The wave behaviors in flip-chip in response to Al and Cu interconnect layers were explored. The estimated accumulated damages by power density waves in response to large transient thermal gradient within solder joints with the Cu layer are negligibly small compared to the Al layer case. It is attributable to the material property of Cu of higher electrical and thermal conductivities than those of Al, enabling the smaller amount of heat generated due to small electrical resistivity (large electrical conductivity) be effectively conducted to adjacent areas and materials. From the short-time scale point of view, this means that there would not be much local heat build-up during the initial period of the whole time window, thus the relative expansions of the Cu layer and the corner of the 3rd solder (that is on the fore-mentioned current flow path) would both be a lot less than the Al layer case. This is why the generated stress waves and power densities have small magnitude compared to the Al layer case and also negligible accumulated damage within each solder joint. Thus, if the short-time scale effect is to be concerned, Cu as the interconnecting material is recommended for flip-chips.

It should be noted that the flip-chip model used in the dissertation (as in Figs. 3.1 and 6.1) is an idealized one. In reality, the package would include dielectric layers, passivation, solder mask, among others which all are not included in the model. Usually Al is used in the metal layer with silicon dioxide (SiO_2) to form dielectric layers. Given the trend for increased integration, significant power loss, improved heat dissipation, reduced interconnect RC delays and less cross-talk between adjacent metal lines, using Cu for metal layers is being considered the choice for advanced IC circuits [48,49]. Also, Cu interconnecting material is commonly used with low-k dielectric materials having a less dielectric constant than that of SiO_2 to achieve significantly reduced capacitance. However, if SiO_2 is replaced by low-k dielectric materials of lower modulus, lower fracture toughness and poor adhesion, it would have a negative impact on the flip-chip reliability. It is known that thermal deformation inside the package coupled into the interconnect structure can significantly increase the probability for interfacial delamination. Flip-chips with Cu/low-k structures can be negatively affected in this regard [50]. Further research would be needed to resolve the problem.

CHAPTER VII

CONCLUSIONS AND FUTURE WORK

7.1 Observations Made in the Research

For the well-established thermal cycling tests of long-time scale, optimization of underfill material property was studied with the help of micromechanics-based effective material property prediction and FEA. Optimal material composition can be proposed using this approach for any specific epoxy-filler combination. For example, for the flip-chip with underfill of epoxy-silica filler composite, an optimal performance could be achieved when the silica filler content is maintained about 85 wt%.

Based on the knowledge established through exploring the coupled governing field equations, improved power cycling tests using the notion of electrical-thermal-mechanical excitations was proposed and analysis of flip-chips in response to current flow upon power-on was performed. Regions of high ECDM and large magnitude heat fluxes were identified. The stress waves induced within the first few nanoseconds were of low magnitude and extremely high frequency and they attenuated significantly beyond this initial transient period. What distinguishes this short-time analysis from the long-time analysis is that only a very localized region is affected by electrical joule heating while all other regions remain unaffected. In contrast to the short-time scale scenario, the whole package of small feature size is subjected to a near isothermal state undergoing thermal cycling tests of long-time scale. Thus the area seeing this large thermal transient gradient underwent a rapid expansion and consequently acted as the origin of propagating waves. How the various components in the flip-chip respond to these waves was studied in Chapter IV.

As the most important part of the dissertation, Chapter IV presented an approach for interpreting the dynamic stress waves of short-time scale. Employing the notion of power density and the simultaneous time-frequency resolution provided by the STFT analysis, it was shown that the induced stress waves can be related to experimental fatigue data, allowing the accumulated damage to be estimated for normal and shear power density waves at various locations including interfaces.

To investigate the effect of material viscoelasticity on short-time scale waves, underfills were modeled as a series of spring and dashpot elements following the Maxwell model. In general, underfill material viscoelasticity did help decrease the accumulated damages within the flip-chip only to an insignificant degree. At some locations, the accumulated damage was seen even to increase. A material property characterization study was also performed to determine the optimal underfill material of epoxy and silica filler composite. Analysis of accumulated damages revealed that, among 50 wt% ~ 90 wt% filler content considered, filler content of 60 wt% and 70 wt% gave the best (optimal) performance in response to short-time scale effects.

The impact of employing Cu interconnecting materials on the short-time scale effect was also investigated. Since Cu has higher electrical and thermal conductivity, the maximum ECDM within solder joints with Cu layer was seen to reduce by 22% and the generated power density waves were of one order magnitude less than the case with Al layer. Though the time-frequency response was of the similar trend, the estimated damage accumulation with the Cu layer was negligible. None of the locations considered in solder joints demonstrated a high probability for microcracking.

7.2 Conclusions

The need for short product turn-around time has rendered FEA an effective tool in initial design or post-failure evaluation of electronic packages. As one of the most important long-time scale testing procedures analyses, thermal cycling FEA is implemented for optimizing underfill materials in order to attain maximal flip-chip performance. As demonstrated, FEA-based thermal cycling tests can be applied to any epoxy-filler systems to identify optimal material properties. Knowledge thus obtained should then be combined with those obtained through considering the short-time scale effects to establish a complete knowledge base essential for improved electronic packaging reliability. The demands for high clock speeds, high power and large current magnitude in flip-chips of small dimension have inevitably raised the concern for rapid thermal transients and large thermal gradients that could severely compromise package performance. To address the concern, the dissertation presents an approach employing coupled electrical-thermal-mechanical multi-physics to establish better understanding of the short-lived waves (short-time scale effects) and their impact on reliability.

As the generated stress waves propagate in all directions and each material component responds differently depending on the location, the notions of high cycle fatigue and power density enabled accumulated damages to be evaluated. There were several locations within solder joints and along interfaces between different materials found to be more vulnerable than others to power density waves. Considering that the model under investigation is an idealized one and there is no established data available for shearing failure at interfaces, all numerical results corresponding to shear power density failure should be interpreted as a qualitative measure for failure probability in the relative sense. Accumulated damage approach by power density waves have helped identify short-time scale failure modes and would be particularly valuable for improving flip-chip design by suppressing or discouraging short-time stress wave propagation.

With their damping characteristics inherent of all viscoelastic polymeric materials, underfill materials could be effective in attenuating stress wave propagation at the short-time scale. However, investigation showed that underfill materials being elastic or viscoelastic do not affect short-time scale wave motions in flip-chip. In thermal cycling tests of long-time scale, solder joints are fully encapsulated by underfill, thus helping achieve desirable overall stress redistribution within the package. However, the critical propagation path of short-time scale stress wave is not through the underfill material, but through Al layers and corners of solder joints located along the path of electrical current. This is one of the reasons as to why viscoelastic underfill is not effective in discouraging short-time scale effects. Nonetheless, an epoxy-filler system was proposed that is optimal for short-time scale effect. Investigations performed on Al and Cu interconnecting layers showed that, with its better electrical and thermal performance than Al, the inclusion of Cu layers significantly helped decrease the magnitudes of induced stresses and power densities and result in negligible accumulated damages. From the perspective of short-time scale effect, Cu layers are therefore preferred. In summary,

- For thermal cycling tests of long-time scale, micromechanics-based effective material prediction of underfill and FEA can help identify optimal epoxy-filler underfill systems.
- Multi-physics study of flip-chips subject to instantaneous power-on reveals high ECDM regions and large magnitude heat fluxes.
- Short-time stress waves are highly dispersive and characteristically of broadband, low magnitude and high frequency.

- Power density interpretation of high cycle fatigue combined with STFT analysis enablesthe evaluation of accumulated damages and identification of probable regions of microcracking and interfacial delamination.
- Underfill viscoelasticity is insignificant in attenuating short-time scale effects.
- Underfill materials optimal for short-time scale effects can be formulated using the proposed approach.
- Research results imply that a compromise between long-time and short-time scale properties would be required to achieve overall optimal packaging material design.
- Cu interconnecting layer system is preferred to Al layer system if short-time scale effect is concerned.

7.3 Research Contributions

The research is the first to investigate the effect of electrical-thermal-mechanical excitation at short-time scale on electronic packaging reliability. Additionally, that (1) realistic flip-chip responses upon power-on can be realized and failure modes resulting from wave phenomena can be investigated, and (2) packaging material design optimal for short-time and long-time effects can be formulated and enable higher packaging reliability as a result. As microelectronic manufacturing is a business of billions of dollars a year, the research reported herein would not just render high fabrication yield, but also bring out significant impact on packaging development, packaging material formulation and micro-circuit layout design.

7.4 Recommendations for Future Work

Effort should be made to further develop the identification of high cycle fatigue related failure mechanism. As dynamic shearing failure modes of delamination and debond are not well understood and no such data is available, a way to establish and quantify such failures is needed. Though the time and geometrical scales of the problem that this dissertation volume addressed are beyond the reach of contemporary measurement techniques, nevertheless, experimental verification of short-time scale effects should be planned upon the availability of technology.

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APPENDIX A

```
**%  =============================================================
**%
**%          Electro-Thermal Analysis of Flip-Chip
**%          with time step = 5.E-10 (sec) / total time = 5.E-7 (sec)
**%
**%           UNITS: M-m (newton)
**%                ... LENGTH : M
**%                ... TIME   : sec
**%                ... MASS   : kilogram (kg)
**%                ... FORCE  : newton
**%                ... TEMPERATURE : deg Celsius
**%
**%  =============================================================
**%
**%
*HEADING
*NODE, NSET=ALLNODES, SYSTEM=R
       1,-3.6370519E-03, 2.5424972E-03, 0.0000000E+00
.....
  786703,-2.3183020E-03, 2.2024950E-03, 0.0000000E+00
*ELEMENT, TYPE=DC2D6E   , ELSET=ABAQUS PLANE STRAIN
 176225, 429292, 429293, 628071, 449454, 628015, 628018
.....
 176362, 628036, 628034, 628681, 628035, 628718, 628677
*ELEMENT, TYPE=DC2D8E   , ELSET=ABAQUS PLANE STRAIN_1
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.....
 228082, 749941, 749938, 750169, 750172, 749939, 749937, 750170, 749940
*NSET,NSET=BC-CENTER
  123859,  123860,  123861,  123862,  123863,  123879,  123880,  123881,  123882,  123883,  123884
.....
  747760,  747761,  747762,  747763,  749610,  749611,  749612,  749613,  749614,  749615,  749616
*NSET,NSET=WATCH
       1,      34,      53,      54,      55,      56,      57,      58,      59,      60,      61
.....
  786587,  786588,  786590,  786591,  786592
*NSET,NSET=PCB
     563,    1309,   12872,   12873,   12874,   12875,   12876,   12877,   12878,   12879,   12880
.....
  786701,  786702,  786703
*NSET,NSET=AL-LAYER
     339,     340,     357,     358,     359,     360,     361,     362,     363,     364,     365
.....
  429376,  429377,  429378,  429379,  429380,  429381,  429382,  429383,  429384,  429385
*NSET,NSET=SOLDER-2-BOT
       1,      34,      53,      54,      55,      56,      57,      58,      59,      60,      61
.....
  124315,  124316,  124317,  124318,  124319,  124320,  124321,  124322,  124323,  124324,  124325
*NSET,NSET=SOLDER-3-BOT
     338,     356,     372,     373,     374,     375,     376,     377,     378,     379,     380
.....
    1299,    1300,    1301,    1302,    1303,    1304,    1305,    1306,    1307,    1308,    1309
*NSET,NSET=BC-BOTTOM
  708428,  743533,  743534,  743535,  743536,  743539,  743540,  743541,  743542,  743545,  743546
.....
  786534,  786535,  786572,  786573
*NSET,NSET=UNDER
     338,     339,     387,     388,     389,     390,     391,     392,     393,     394,     395
.....
  128361,  128362,  128363,  128364
*NSET,NSET=SOLDER
```

```
     1,      34,      53,      54,      55,      56,      57,      58,      59,      60,      61
.....
 124328,  124329,  124330,  124331,  124332,  124333
*NSET,NSET=PCB
     1,      34,      53,      54,      55,      56,      57,      58,      59,      60,      61
.....
 398417,  398418,  398419,  398420,  398421,  398422,  398423,  398424,  398425,  398426
*NSET,NSET=ALL
     1,      34,      53,      54,      55,      56,      57,      58,      59,      60,      61
.....
 786698,  786699,  786700,  786701,  786702,  786703
*NSET,NSET=CU-LAYER-1
     1,      34,      53,      54,      55,      56,      57,      58,      59,      60,      61
.....
 396075,  396076,  396077
*NSET,NSET=CU-LAYER-2
   338,     356,     372,     373,     374,     375,     376,     377,     378,     379,     380
.....
 398417,  398418,  398419,  398420,  398421,  398422,  398423,  398424,  398425,  398426
*NSET,NSET=CU-LAYER-2-BC
  20705,  341348,  341377
*NSET,NSET=CU-LAYER-1-BC
 128345,  346463,  346558
*ELSET,ELSET=FILM-1
 125450,  125451,  125452,  125453,  125454,  125455,  125456,  125457,  125458,  125459,  125460
.....
 125715,  125716,  125717,  125718,  125719,  125720,  125721,  125722
*ELSET,ELSET=FILM-2-1
 176225,  176230,  176236,  176239,  176244,  176246,  176261,  176263,  176265,  176266,  176267
.....
 176361,  176362
*ELSET,ELSET=FILM-2-2
 176218,  176219,  176220,  176221,  176222,  176223,  176224,  176226,  176227,  176228,  176229
.....
 176349,  176360
*ELSET,ELSET=FILM-3
 228011,  228012,  228013,  228014,  228015,  228016,  228017,  228018,  228019,  228020,  228021
.....
 228077,  228078,  228079,  228080,  228081,  228082
*ELSET,ELSET=FILM-4
 227667,  227668,  227669,  227670,  227671,  227672,  227673,  227674,  227675,  227676,  227677
.....
 228082,
*ELSET,ELSET=FILM-5
 215445,  215446,  215447,  215448,  215449,  215450,  215451,  215452,  215453,  215454,  215455
.....
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 118723,  118724,  118725,  118726,  118727,  118728,  118729,  118730,  118731,  118732,  118733
.....
 125719,  125720,  125721,  125722
 227176,  227274,  227372,  227470,  227568,  227666,  227764
*ELSET,ELSET=UNDER
  26228,   26229,   26230,   26231,   26232,   26233,   26234,   26235,   26236,   26237,   26238
.....
 176361,  176362
*ELSET,ELSET=SOLDER
    65,      66,      67,      68,      69,      70,      71,      72,      73,      74,      75
.....
  36370,   36371,   36372,   36373,   36374,   36375,   36376,   36377
*ELSET,ELSET=PCB
  97503,   97504,   97505,   97506,   97507,   97508,   97509,   97510,   97511,   97512,   97513
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 228073,  228074,  228075,  228076,  228077,  228078,  228079,  228080,  228081,  228082
*ELSET,ELSET=TEMP-WATCH
    65,      66,      67,      68,      69,      70,      71,      72,      73,      74,      75
.....
```

```
 227836,  227837,  227838,  227839
*ELSET,ELSET=WATCH
    65,      66,      67,      68,      69,      70,      71,      72,      73,      74,      75
.....
 227121,  227219,  227317,  227415,  227513,  227611,  227709
*ELSET,ELSET=AL-LAYER
 125723,  125724,  125725,  125726,  125727,  125728,  125729,  125730,  125731,  125732,  125733
.....
 125855,  125856,  125857,  125858,  125859,  125860,  125861,  125862
*ELSET,ELSET=CU-LAYER
  97683,   97684,   97685,   97686,   97687,   97688,   97689,   97855,   97859,   97860,   97861
.....
  97847,   97848,   97849,   97850,   97851,   97852,   97853,   97854
*ELSET,ELSET=ALL
    65,      66,      67,      68,      69,      70,      71,      72,      73,      74,      75
.....
 228075,  228076,  228077,  228078,  228079,  228080,  228081,  228082
**
*SOLID SECTION,ELSET=SI,MATERIAL=MSI
1.2E-3
*MATERIAL,NAME=MSI
*conductivity
148.
*density
2330.
*specific heat
712.
*ELECTRICAL CONDUCTIVITY
3.413E-4
*JOULE HEAT FRACTION
 1.0
**
*SOLID SECTION,ELSET=SOLDER,MATERIAL=MSOLDER
0.085E-3
*MATERIAL,NAME=MSOLDER
*conductivity
51.
*density
8470.
*specific heat
151.
*ELECTRICAL CONDUCTIVITY
7.0E+6
*JOULE HEAT FRACTION
 1.0
**
*SOLID SECTION,ELSET=PCB,MATERIAL=MPCB
2.E-3
*MATERIAL,NAME=MPCB
*conductivity
13.
*density
1938.
*specific heat
879.
*ELECTRICAL CONDUCTIVITY
1.E-30
*JOULE HEAT FRACTION
 1.0
**
*SOLID SECTION,ELSET=UNDER,MATERIAL=MUNDER
1.2E-3
*MATERIAL,NAME=MUNDER
*conductivity
1.6
*density
```

```
6080.
*specific heat
674.
*ELECTRICAL CONDUCTIVITY
1.E-30
*JOULE HEAT FRACTION
 1.0
**
*SOLID SECTION,ELSET=CU-LAYER,MATERIAL=MCOPPER
0.085E-3
*MATERIAL,NAME=MCOPPER
*conductivity
401
*density
8940
*specific heat
380.
*ELECTRICAL CONDUCTIVITY
5.977E+7
*JOULE HEAT FRACTION
 1.0
**
*SOLID SECTION,ELSET=AL-LAYER,MATERIAL=MAL
0.085E-3
*MATERIAL,NAME=MAL
*conductivity
237
*density
2700
*specific heat
900
*ELECTRICAL CONDUCTIVITY
3.745E+7
*JOULE HEAT FRACTION
 1.0
**
*initial conditions,type=temperature
ALLNODES,25.00
**
*restart,write,frequency=10000
**
*STEP,INC=10000000
  STEP 1: JOULE HEATING ANALYSIS W/O RAMP CURRENT
*COUPLED THERMAL-ELECTRICAL
5.E-10,5.E-7
*boundary
CU-LAYER-2-BC,9,,0
*cecurrent
CU-LAYER-1-BC,9, 0.1667
*film
FILM-1,f3,25,50
FILM-2-1,f3,25,50
FILM-2-2,f1,25,50
FILM-3,f1,25,5
FILM-4,f4,25,5
FILM-5,f3,25,5
**
*node file
NT
*el file, elset=watch, frequency=0
ECDM
*node print,nset=watch, frequency=0
NT
*el print, elset=watch, frequency=0
ECDM,HFL
**
```

```
*OUTPUT, FIELD, FREQUENCY=0
**
*file format, zero increment,ascii
**
*end step
```

APPENDIX B

```
**%  ============================================================
**%
**%          Mechanical Analysis of Flip-Chip
**%          with time step = 5.E-10 (sec) / total time = 5.E-7 (sec)
**%
**%           UNITS: M-m (newton)
**%                ... LENGTH : M
**%                ... TIME   : sec
**%                ... MASS   : kilogram (kg)
**%                ... FORCE  : newton
**%                ... TEMPERATURE : deg Celsius
**%
**%  ============================================================
**%
**%
*HEADING
*NODE, NSET=ALLNODES, SYSTEM=R
       1,-3.6370519E-03, 2.5424972E-03, 0.0000000E+00
.....
    786703,-2.3183020E-03, 2.2024950E-03, 0.0000000E+00
*ELEMENT, TYPE=CPE6   , ELSET=ABAQUS PLANE STRAIN
 176225, 429292, 429293, 628071, 449454, 628015, 628018
.....
 176362, 628036, 628034, 628681, 628035, 628718, 628677
*ELEMENT, TYPE=CPE8R   , ELSET=ABAQUS PLANE STRAIN_1
    65,    370,    340,    342,    410,    371,    341,    409,    402
.....
 228082, 749941, 749938, 750169, 750172, 749939, 749937, 750170, 749940
*NSET,NSET=BC-CENTER
  123859,  123860,  123861,  123862,  123863,  123879,  123880,  123881,  123882,  123883,  123884
.....
  747760,  747761,  747762,  747763,  749610,  749611,  749612,  749613,  749614,  749615,  749616
*NSET,NSET=WATCH
      1,     34,     53,     54,     55,     56,     57,     58,     59,     60,     61
.....
  786587,  786588,  786590,  786591,  786592
*NSET,NSET=PCB
    563,    1309,   12872,   12873,   12874,   12875,   12876,   12877,   12878,   12879,   12880
.....
  786701,  786702,  786703
*NSET,NSET=AL-LAYER
    339,    340,    357,    358,    359,    360,    361,    362,    363,    364,    365
.....
  429376,  429377,  429378,  429379,  429380,  429381,  429382,  429383,  429384,  429385
*NSET,NSET=SOLDER-2-BOT
      1,     34,     53,     54,     55,     56,     57,     58,     59,     60,     61
.....
  124315,  124316,  124317,  124318,  124319,  124320,  124321,  124322,  124323,  124324,  124325
*NSET,NSET=SOLDER-3-BOT
    338,    356,    372,    373,    374,    375,    376,    377,    378,    379,    380
.....
   1299,   1300,   1301,   1302,   1303,   1304,   1305,   1306,   1307,   1308,   1309
*NSET,NSET=BC-BOTTOM
  708428,  743533,  743534,  743535,  743536,  743539,  743540,  743541,  743542,  743545,  743546
.....
  786534,  786535,  786572,  786573
*NSET,NSET=UNDER
    338,    339,    387,    388,    389,    390,    391,    392,    393,    394,    395
.....
  128361,  128362,  128363,  128364
*NSET,NSET=SOLDER
```

```
     1,     34,     53,     54,     55,     56,     57,     58,     59,     60,     61
.....
 124328, 124329, 124330, 124331, 124332, 124333
*NSET,NSET=PCB
     1,     34,     53,     54,     55,     56,     57,     58,     59,     60,     61
.....
 398417, 398418, 398419, 398420, 398421, 398422, 398423, 398424, 398425, 398426
*NSET,NSET=ALL
     1,     34,     53,     54,     55,     56,     57,     58,     59,     60,     61
.....
 786698, 786699, 786700, 786701, 786702, 786703
*NSET,NSET=CU-LAYER-1
     1,     34,     53,     54,     55,     56,     57,     58,     59,     60,     61
.....
 396075, 396076, 396077
*NSET,NSET=CU-LAYER-2
   338,    356,    372,    373,    374,    375,    376,    377,    378,    379,    380
.....
 398417, 398418, 398419, 398420, 398421, 398422, 398423, 398424, 398425, 398426
*NSET,NSET=CU-LAYER-2-BC
  20705, 341348, 341377
*NSET,NSET=CU-LAYER-1-BC
 128345, 346463, 346558
*ELSET,ELSET=FILM-1
 125450, 125451, 125452, 125453, 125454, 125455, 125456, 125457, 125458, 125459, 125460
.....
 125715, 125716, 125717, 125718, 125719, 125720, 125721, 125722
*ELSET,ELSET=FILM-2-1
 176225, 176230, 176236, 176239, 176244, 176246, 176261, 176263, 176265, 176266, 176267
.....
 176361, 176362
*ELSET,ELSET=FILM-2-2
 176218, 176219, 176220, 176221, 176222, 176223, 176224, 176226, 176227, 176228, 176229
.....
 176349, 176360
*ELSET,ELSET=FILM-3
 228011, 228012, 228013, 228014, 228015, 228016, 228017, 228018, 228019, 228020, 228021
.....
 228077, 228078, 228079, 228080, 228081, 228082
*ELSET,ELSET=FILM-4
 227667, 227668, 227669, 227670, 227671, 227672, 227673, 227674, 227675, 227676, 227677
.....
 228082,
*ELSET,ELSET=FILM-5
 215445, 215446, 215447, 215448, 215449, 215450, 215451, 215452, 215453, 215454, 215455
.....
*ELSET,ELSET=SI
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.....
 125719, 125720, 125721, 125722
 227176, 227274, 227372, 227470, 227568, 227666, 227764
*ELSET,ELSET=UNDER
  26228,  26229,  26230,  26231,  26232,  26233,  26234,  26235,  26236,  26237,  26238
.....
 176361, 176362
*ELSET,ELSET=SOLDER
    65,     66,     67,     68,     69,     70,     71,     72,     73,     74,     75
.....
  36370,  36371,  36372,  36373,  36374,  36375,  36376,  36377
*ELSET,ELSET=PCB
  97503,  97504,  97505,  97506,  97507,  97508,  97509,  97510,  97511,  97512,  97513
.....
 228073, 228074, 228075, 228076, 228077, 228078, 228079, 228080, 228081, 228082
*ELSET,ELSET=TEMP-WATCH
    65,     66,     67,     68,     69,     70,     71,     72,     73,     74,     75
.....
```

```
 227836,  227837,  227838,  227839
*ELSET,ELSET=WATCH
     65,      66,      67,      68,      69,      70,      71,      72,      73,      74,      75
.....
 227121,  227219,  227317,  227415,  227513,  227611,  227709
*ELSET,ELSET=AL-LAYER
 125723,  125724,  125725,  125726,  125727,  125728,  125729,  125730,  125731,  125732,  125733
.....
 125855,  125856,  125857,  125858,  125859,  125860,  125861,  125862
*ELSET,ELSET=CU-LAYER
  97683,   97684,   97685,   97686,   97687,   97688,   97689,   97855,   97859,   97860,   97861
.....
  97847,   97848,   97849,   97850,   97851,   97852,   97853,   97854
*ELSET,ELSET=ALL
     65,      66,      67,      68,      69,      70,      71,      72,      73,      74,      75
.....
 228075,  228076,  228077,  228078,  228079,  228080,  228081,  228082
**
*SOLID SECTION,ELSET=SI,MATERIAL=MSI
1.2E-3
*MATERIAL,NAME=MSI
*ELASTIC,TYPE=ISOTROPIC
131.E+9, 0.3
*EXPANSION,TYPE=ISO
 2.8E-06
*density
2330.
**
*SOLID SECTION,ELSET=SOLDER,MATERIAL=MSOLDER
0.085E-3
*MATERIAL,NAME=MSOLDER
*ELASTIC,TYPE=ISOTROPIC
35.52E+9, 0.4, -40
29.80E+9, 0.4, 25
25.40E+9, 0.4, 75
21.00E+9, 0.4, 125
*EXPANSION, TYPE=ISO
 21.E-6
*PLASTIC
26.59E+6, 0, -40.
20.285E+6, 0, 25.
15.435E+6, 0, 75.
10.585E+6, 0, 125.
**
*density
8470.
**
*SOLID SECTION,ELSET=PCB,MATERIAL=MPCB
2.E-3
*MATERIAL,NAME=MPCB
*ELASTIC,TYPE=ISOTROPIC
22.E+9, 0.28
*EXPANSION,TYPE=ISO
 18.E-06
*density
1938.
**
*SOLID SECTION,ELSET=UNDER,MATERIAL=MUNDER
1.2E-3
*MATERIAL,NAME=MUNDER
*ELASTIC,TYPE=ISOTROPIC
8.E+9, 0.35
*EXPANSION,TYPE=ISO
 38.E-06
*density
6080.
```

```
**
*SOLID SECTION,ELSET=CU-LAYER,MATERIAL=MCU
0.085E-3
*MATERIAL,NAME=MCU
*ELASTIC,TYPE=ISOTROPIC
117.E+9, 0.35
*EXPANSION,TYPE=ISO
16.8E-06
*density
8940.
**
*SOLID SECTION,ELSET=AL-LAYER,MATERIAL=MAL
0.085E-3
*MATERIAL,NAME=MAL
*ELASTIC,TYPE=ISOTROPIC
70.E+9, 0.33
*EXPANSION,TYPE=ISO
22.4E-06
*density
2700.
**
*boundary
BC-CENTER,1
BC-BOTTOM,2
**
*initial conditions,type=temperature,file=Appendix-A,step=1,inc=0
*restart,write,frequency=0
*step, inc=100000
*dynamic
5.E-10,5.E-7
*temperature, file=Appendix-A,bstep=1,binc=1,estep=1,einc=1000
**
*el print, elset=watch,frequency=1, POSITION=CENTROIDAL
mises,s
*el print, elset=watch,frequency=1, POSITION=CENTROIDAL
sp,tresc
*node print,nset=watch,frequency=0
u
*el file, elset=watch,frequency=0, POSITION=CENTROIDAL
s
*node file,nset=watch,frequency=0
u
*OUTPUT, FIELD, FREQUENCY=0
*file format, zero increment
*end step
**ECDM,HFL
**
*OUTPUT, FIELD, FREQUENCY=0
**
*file format, zero increment,ascii
**
*end step
```

VITA

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He came to the United States in August 1999 to pursue higher education and joined the Ph.D. program at Texas A&M University. He worked under the supervision of Dr. Chii-Der Steve Suh in the field of electronic packaging reliability and graduated in August 2004. His permanent address is Hongjaewon Hyundai APT 101-1501, Hongjae-4 dong 459, Seodaemoon-gu, Seoul, Korea, 120-788.