LOW-POWER CURRENT-MODE

ADC FOR CMOS SENSOR IC

A Thesis

by

ANUJ AGARWAL

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2005

Major Subject: Electrical Engineering

LOW-POWER CURRENT-MODE

ADC FOR CMOS SENSOR IC

A Thesis

by

ANUJ AGARWAL

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Approved by:

Chair of Committee,   Sameer Sonkusale
Committee Members,   Aydin Karsilayan
                        Laszlo Kish
                        Alexander Parlos
Head of Department,   Chanan Singh

August 2005

Major Subject: Electrical Engineering

ABSTRACT

Low-power Current-Mode ADC for

CMOS Sensor IC. (August 2005)

Anuj Agarwal, B. Tech., Indian Institute of Technology, Kanpur

Chair of Advisory Committee: Dr. Sameer Sonkusale

A low-energy current-mode algorithmic pipelined ADC targeted for use in distributed sensor networks is presented. The individual nodes combine sensing, computation and communications into an extremely small volume. The nodes operate with very low duty cycle due to limited energy.

Ideally these sensor networks will be massive in size and dense in order to promote redundancy. In addition the networks will be collectively intelligent and adaptive. To achieve these goals, distributed sensor networks will require very small, inexpensive nodes that run for long periods of time on very little energy. One component of such network nodes is an A/D converter. An ADC acts as a crucial interface between the sensed environment and the sensor network as a whole. The work presented here focuses on moderate resolution, and moderate speed, but ultra-low-power ADCs. The 6 bit current-mode algorithmic pipelined ADC reported here consumes 8 pJ/bit samples at 0.65V supply and 130 kS/s. The current was chosen as the information carrying quantity instead of voltage as it is more favorable for low-voltage and low-power applications. The reference current chosen was 150nA. All the blocks are using transistors operating in subthreshold or weak inversion region of operation, to work in low-voltage and low current supply.

The DNL and INL plots are given in simulation results section. The area of the overall ADC was 0.046 mm^2 only.

To My Family, Friends and Teachers

ACKNOWLEDGMENTS

I gratefully acknowledge the support, guidance and encouragement that I received from my advisor, Dr. Sameer Sonkusale, throughout the course of my studies. Dr. Sonkusale has this amazing ability to penetrate to core of any problem and solve it from the basics. This ability of his was a great source of inspiration to me and which is possibly the best training I can get to solve any problem. Working under him has been a very illuminating experience.

I would like to thank all my committee members: Dr. Aydin Karsilayan, Dr Laszlo Kish and Dr. Alexander Parlos. I am grateful to Dr. Reza Langari for his support. He was kind enough to act as substitute at my thesis defense.

I am also thankful to Dr. Jose Silva-Martinez and Dr. Ugur Cilingiroglu for their excellent course on analog circuit design and device physics respectively. Their careful and systematic approach of dealing with things, their patience while dealing with students trying to understand their confusion, and providing the correct cure have made a deep impression on me.

This work benefited greatly from the interaction with all the members of the AMSC group. In particular I would like to thank Youngbok Kim, Manisha Gambhir, Vijayakumar Dhanasekaran and Sivasankari Krishnanji for their constant support and encouragement, without which this project would not have been possible. In spite of busy schedules, they always had time to listen to me and help me out with my problems.
I would also like to acknowledge Raman, Anmol, Manik, Rajnish, Ashish, Mandar, Sudhir and Himanshu for the good time that I had with them at Texas A&M University. Their company never let me feel away from home.

Finally, I thank my parents, and also Mitali, Swati, Saurabh, Nikita and Nimish for their love and support. I thank them for giving me the constant love, encouragement, inspiration and motivation without which this research would not have been possible.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER I

INTRODUCTION

Over the last decade, much of the research on analog-to-digital converters (ADC) has been focused on developing architectures such as pipelined [1] and sigma-delta converters [2], and pushing the limits of performance in resolution and speed. The work presented here focuses on moderate resolution, and moderate speed, but ultra-low-power ADCs. Such ADCs will be critical in the emergence of large scale sensor networks. Distributed sensors utilizing low-power sensor motes are becoming a popular solution for data gathering in hazardous environment. Integrated CMOS sensors with built-in data acquisition signal conditioning and transmission are needed for such applications. However, there is strict energy consumption limit for these sensors, since most of these sensors plan to use energy from scavenging the environment, or through a single battery to last a lifetime. The ADC used in such sensors act as the crucial interface between the sensed environment and the sensor network as a whole. The network exploits the spatial redundancy of the sensors in any available location to obtain accurate sensor data. Hence resolution and accuracy of the ADC in a single sensor mote is not critical. However, due to strict power budget, there is a stringent requirement on its energy consumption and area. Leveraging both CMOS device scaling and MEMS technologies, each mote will integrate sensing, computation, communications and power into a volume on the order of 1 mm^3. The list of potential applications is tremendous, ranging from smart building environments, tracking wildlife populations, monitoring crops and livestock, and measuring and predicting weather patterns.

This thesis follows the style of *IEEE Journal of Solid State Circuits.*
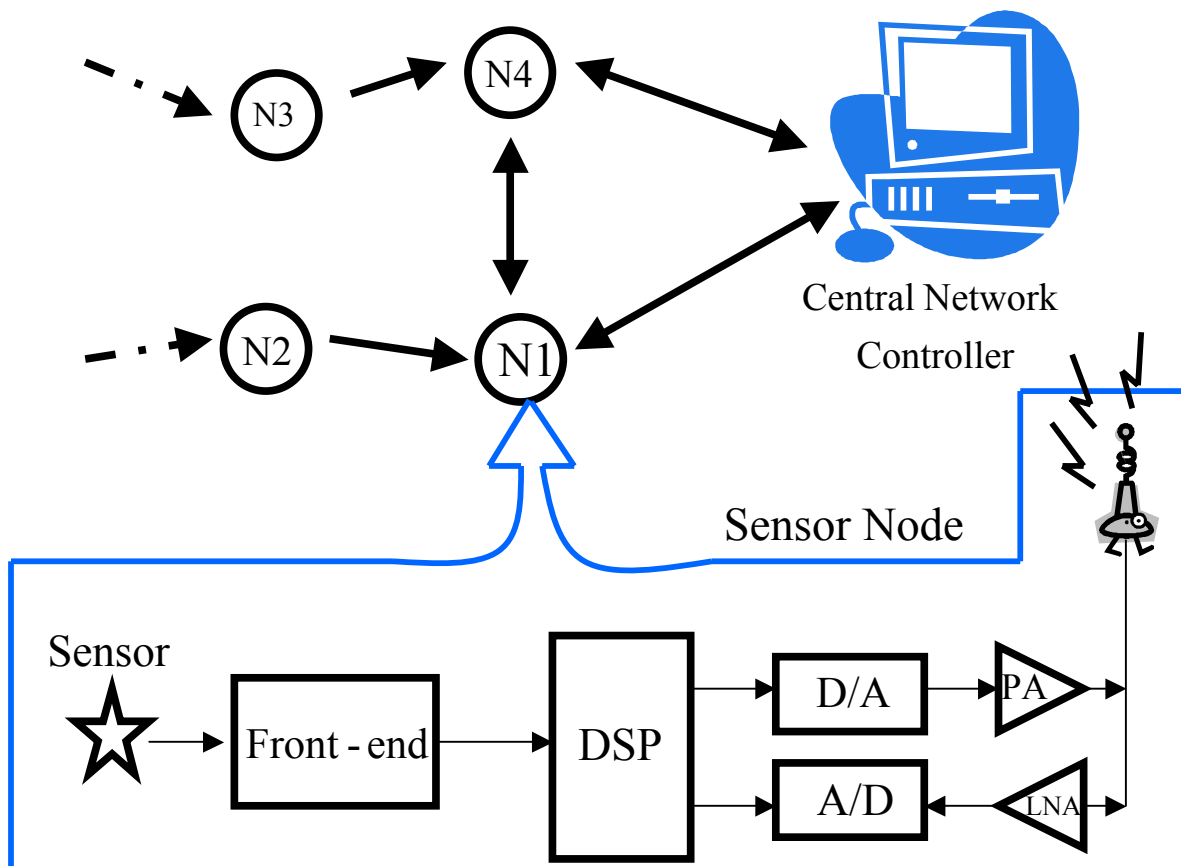
Figure 1.1 The conceptual example of distributed sensing using N redundant sensors.

An autonomous node in a sensor network ideally contains a sensor, a readout circuit, a digital signal processing part to process information from the sensor and a RF communication circuit. The central base station which functions as a network controller collects the data from all the sensor nodes and extracts meaningful information of the target material by performing advanced digital signal processing. Fig.1.1 demonstrates the conceptual block diagram of distributed sensing using N redundant sensors. As seen, the system has the front-end which converts the raw signal from the sensor to the electrical signal. At the second stage, ADC converts the electrical signals into the digital signals which are much easier to process. The digital signals so received are converted into analog signal in order to be transmitted as the radio frequency signal through Power Amplifier. Also, the control signals from Central Network Controller and that sensor data from neighboring nodes come via the same antenna, the low noise amplifier and the A/D converter.

The performance and flexibility of the mote's integrated ADC is critical. The ADC provides the interface between the sensed environment or quantity and the sensor network as a whole. Low-power consumption is paramount, and a standby mode is also required. This work describes the design of the ADC in order to meet the unique requirements of distributed sensor networks. However, the ADC presented here is well suited for many energy constrained systems, such as hearing aids [3], micro robotic systems [4], and insect flight recorders.

1.1   Thesis Guide

A brief description of what is to follow is given below. The thesis has been divided into 6 different chapters.

Chapters II discuss the fundamental limits which are to be taken in consideration while designing an ADC for a particular range of resolution and speed.

Chapter III presents the application of the ADC in Nanowell sensor IC and defines the specifications of the ADC.

Chapter IV surveys the different architecture of ADCs and determines the suitable architecture for the present application.

Chapter V gives an overview of subthreshold region of operation. Its discussion is important as all the transistors are working in weak inversion region and therefore its understanding is important for the design.

The core of the thesis is in Chapter VI. The architecture used is described and the working of all the individual blocks is presented.

Chapter VII presents the simulation results for DNL, INL and SNDR of the ADC.

Chapter VIII presents the performance summary and future work.

CHAPTER II

FUNDAMENTAL LIMITS

Low-power design begins with analyzing and understanding the fundamental limits that constrain the design of the particular circuit or system. For ADC design, these limits ultimately determine the total energy that must be consumed during a data conversion cycle for a given resolution and sampling rate. While it is generally impractical to actually design circuits and systems based on fundamental limits alone, a good understanding of these limits is critical to achieving an optimized design.

2.1 Quantization Noise

Quantization noise is present in all ADCs, including "ideal" converters. Even a perfect ADC generates a quantized output from a continuous input signal. Thus, quantization noise limits the information content of the ADC output. While the input signal can assume any level within the conversion range and can even go beyond the allowed input range, the output is confined to a set of discrete output values. The mere process of converting a continuous analog input signal to a discrete digital output code results in a loss of amplitude information about that input signal. The amount of amplitude information lost in the conversion process depends on the resolution (number of bits) of the ADC.

The transfer curve of an ideal 3-bit ADC is shown in Figure 2.1. Note that while the input signal is continuous, the output signal takes on only discrete (quantized) steps. Thus, there is a many-to-one mapping from the input signal to the output signal, as a particular output value corresponds to a range of input signal values. The quantization of the ADC output implies that there is a difference between the input signal value and the

output signal representing that input. As a thought experiment, assume
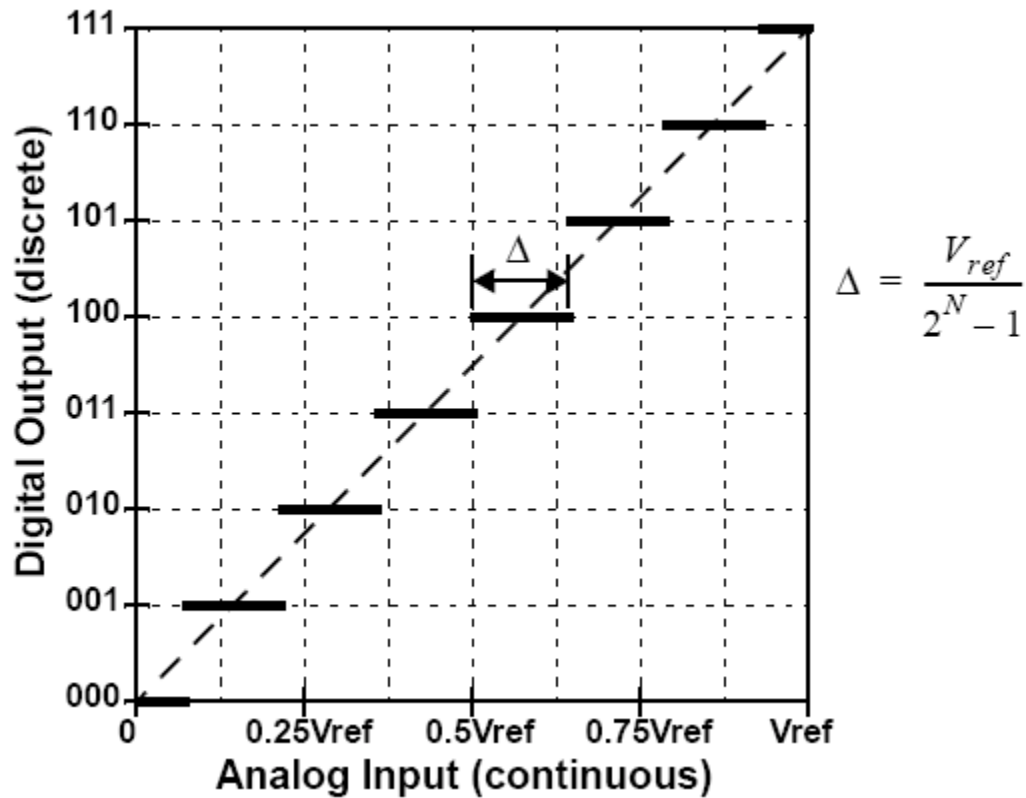
Figure 2.1 Transfer function of an ideal 3-bit ADC. For an N-bit ADC there are 2N output levels corresponding to input voltage ranges of width Δ. In this example, N = 3, meaning there are 8 output levels, and the analog code width Δ= *Vref*/ 7.

that the output of the ideal ADC depicted in Figure 2.1 is passed to an ideal digital-to-analog converter (DAC) so that the input signal is converted from the analog domain, into the digital domain, and then back again to the analog domain. The resulting output of the DAC is not a replica of the original input signal even though both the ADC and DAC are ideal. Instead, due to the ADC quantization, the output contains an input signal dependent error. Figure 2.2 shows the resulting error of the DAC output as a function of the ADC input. Note that this error is due only to the ADC and is called the quantization error of the ADC [5].
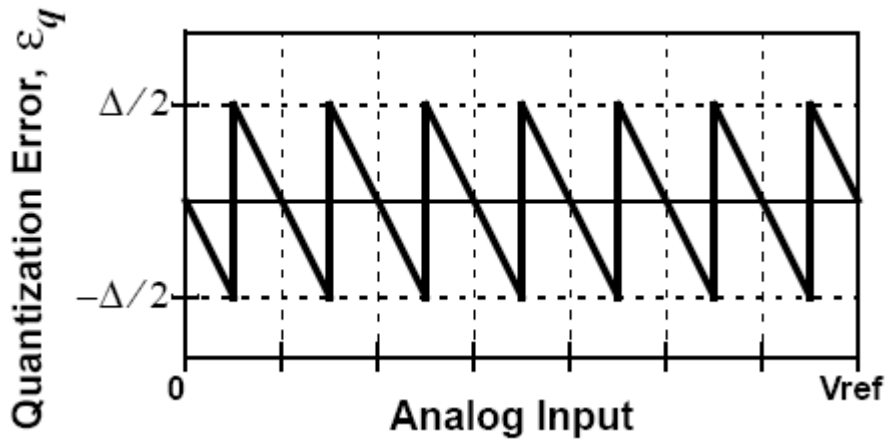
Figure 2.2 Error at the DAC output (from an ideal ADC-DAC series connection). The error comes purely from the quantization error of the ideal 3-bit ADC.

It is clear from Figure 2.2 that the quantization error as a function of time is determined by the input signal time domain behavior. While the quantization error signal can be calculated if the input signal is known this is useless since there is no need for an ADC at all if the input signal is known. Thus it can be concluded that some amount of quantization error exists for all real input signals, but it is not possible to know the exact characteristics of the quantization error.

One approach to approximate the quantization noise for general input signals is to assume that the quantization error takes on a uniform distribution between the limits – Δ/2 and Δ/2, independent of the actual input signal. This approximation works well if the input signal is at least several least-significant-bits (LSB = Δ) in magnitude [5] and "busy" in the bandwidth of the ADC (contains frequency content over the entire bandwidth). Furthermore, the approximation requires that the resolution of the ADC is 4 bits or more [6]. In this case the total quantization noise power is constant, and exhibits a white frequency spectrum. The total quantization noise power is given by [6]

$$P_{QN} = \overline{\varepsilon_q^2} = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} \varepsilon_q^2 d\varepsilon_q = \frac{\Delta^2}{12} \qquad (2.1)$$

Fortunately these conditions are met to a reasonable degree in most systems and Equation (2.1) is a good general approximation of the quantization noise. The result of the quantization error is that even an ideal ADC has noise at the output.

The signal-to-noise ratio (SNR) of the ADC is defined as the signal power divided by the noise power in the output. Since quantization noise is essentially constant and independent of the input signal, smaller input signals result in less total SNR. Assuming an input signal of a full-scale sinusoid, the peak power in the input signal is given by

$$\hat{P}_{sig} = \frac{\Delta^2 . 2^{2N}}{8}$$

(2.2)

where N is the number of bits in the ADC. Given this peak signal power and the quantization noise inherent in the ADC given by Equation (2.1), the peak SNR for the ADC can be shown to be [6]

$$\hat{SNR} = \frac{\hat{P}_{sig}}{P_{QN}} = \frac{3}{2} . 2^{2N}$$

(2.3)

$$\hat{SNR}[dB] = 6.02 N + 1.76$$

(2.4)

Note that this is the maximum SNR achievable for any N-bit ADC, even an ideal ADC. In practice, this SNR is not actually achievable. Test system limitations and other noise sources in the ADC degrade the measured peak SNR of any real ADC.

2.2 Device Noise

Device noise is present in any real circuit, independent of the circuit architecture or technology (e.g. CMOS, bipolar, vacuum tube). While not a fundamental property of the conversion process itself as with quantization noise, device noise plays a critical role in determining ADC performance. Unlike quantization noise, the circuit designer has some control over device noise through appropriate architectural and circuit design decisions. Good circuit design minimizes the power consumption of the overall ADC while achieving the required level of noise performance.

In complementary metal-oxide semiconductor (CMOS) circuits, device noise typically arises in the form of thermal noise, flicker noise, and shot noise. Thermal noise

is present in field-effect transistors (FETs) and resistors, flicker noise is present in all transistors and diodes, and shot noise is present in bipolar transistors and diodes. All of these noise sources may be present in a CMOS ADC, corrupting the desired signal values in circuits and thus limiting the achievable resolution.

Thermal noise is often the major device noise contribution limiting ADC resolution in CMOS circuits since it is present in both FETs and resistors. It arises from the random movement of electrons due to their thermal energy and thus increases with temperature. Thermal noise is associated with resistive channels for carriers, so it is present in both conventional resistors as well as FETs, which can be modeled as voltage-controlled resistors for the purposes of device noise discussions. Note that neglecting base, collector and emitter resistances, thermal noise is not present in bipolar devices because device conduction occurs through potential (diode) junctions rather than resistive channels as in FETs [7]. Thermal noise exhibits no frequency dependence, having a uniform (or "white") power spectrum.

Flicker noise is another significant noise source in CMOS circuits, particularly at low frequency. The flicker noise power is directly proportional to the device current and depends on device geometry, while exhibiting an inverse relationship with frequency. Due to its inverse relationship with frequency, flicker noise is sometimes referred to as 1/f noise. Since the noise increases with lowered frequency, flicker noise is generally the dominant noise source in a circuit for low frequencies. In FETs, it is commonly believed that flicker noise comes from defects in the gate-oxide/silicon interface [8]. Flicker noise in bipolar devices is caused mainly by traps from defects in the emitter-base depletion region [7].

Shot noise is present in both diodes and bipolar transistors, where there is direct current (DC) flow though junction diodes. Shot noise arises due to the quantization of charge [7]. As carriers cross the potential barrier at a junction, they do so individually and independently from one another, but at an average rate given by the DC current. This implies that DC current flow in a junction diode can be modeled as a Poisson process [9]. As such, the shot noise power is proportional to the DC junction current and, like thermal noise, it has a white frequency spectrum.

In general any of these noise sources–thermal, flicker, and shot noise–will affect the achievable resolution of the converter for a given power consumption. The actual noise will depend upon the architecture and circuit implementation. That said, thermal noise tends to be the most important type of device noise in most CMOS circuits. The effects of flicker noise can often be minimized using circuit techniques such as chopper stabilization [10], while shot noise is usually not important in CMOS, since it is only present in bipolar transistors and junction diodes.

It is important to note that while device noise can never be completely eliminated in a real circuit, it can always be reduced enough to achieve a given ADC resolution for most practical cases by increasing the power consumption of the circuit. This is due to the fact that signal power grows faster than noise power for increased device currents, allowing the necessary amount of SNR to be realized by using enough power in the circuit. In this way, device noise contrasts with quantization noise, which is an inherent property of the ADC and cannot be reduced at all for a given ADC resolution.

2.3 Circuit Nonidealities

Circuit nonidealities are an important class of errors which can degrade the resolution of the ADC. Circuit nonidealities are defined in this work as errors attributable to the imperfect physical implementation of circuits. Examples of circuit nonidealities include gain, settling, and harmonic distortion errors in amplifiers, charge injection and settling accuracy in switching circuits, hysteresis errors in comparators, and clock skew and jitter in timing circuits. These errors arise from systematic or inherent nonidealities in the implementation of the chosen circuit architecture. Such imperfections are distinct from errors such as random input offset in amplifiers and comparators, which are usually due to variations in the individual devices or process. These errors are defined as device matching errors and are discussed in Section 2.4.

In practice, many circuit nonidealities will exist in an actual ADC. The effects of these errors are typically difficult to relate to the final performance of the ADC itself since they can produce a large variety of behaviors in the ADC. Due to this analytical complexity, the effects of circuit nonidealities must be analyzed individually to determine

how they degrade ADC performance. Fortunately, circuit nonidealities can in principle be reduced to a degree that makes them unimportant or eliminated entirely with careful circuit design. Minimizing the effects of particular circuit nonidealities usually requires the use of more devices (increasing area) and/or more power in the circuit.

2.4 Device Matching

Nearly all ADC architectures depend upon device matching on some level. Indeed, practically all analog circuits rely at least partly on matched active and/or passive components. Depending on the type of ADC architecture and other error sources such as device noise and circuit nonidealities, device matching can be a dominant factor in determining the resolution of the converter. This is unfortunate because device matching error is limited by manufacturing, and so is present in all designs. Fortunately, many techniques have been developed in order tolerate device matching error such as common centroid layout [11] and dynamic element matching [12].

To investigate how device matching affects ADC performance, it is necessary to consider the statistics of the manufacturing processes in integrated circuit fabrication. For both passive and active devices, there are basically two types of random variations which occur during manufacturing–peripheral and areal fluctuations [11]. Peripheral fluctuations occur along the edges of devices, creating "ragged" edges. Increasing the device periphery tends to reduce the total peripheral error as the fluctuations tend to cancel out over larger device peripheries. Areal fluctuations occur throughout the whole device, leading to variations in device properties over the entire area. Increasing the device area reduces the total amount of areal matching error due to the tendency for the variations to cancel. Given the scaling properties of both peripheral and areal fluctuations, achieving more precise device matching invariably translates into making larger devices. For a given level of device matching, the actual device sizes are determined using manufacturing statistics from process modeling and prior fabrication runs.

Matching error can usually be modeled as a Gaussian distribution described by a mean and a standard deviation. The mean of the matching error distribution captures any systematic mismatch in the manufacturing process or actual circuit layout. Often these

systematic matching errors are unimportant in the way they affect the ADC performance or can be made to approach zero when careful layout techniques and/or clever circuit design are employed. The standard deviation of the matching error is a measure of the random mismatch inherent in the manufacturing process and material properties. Unlike systematic mismatch, it is usually difficult or even impossible to eliminate the effects of this random portion of the matching error.

Since the random matching error is generally difficult to eliminate or design around with appropriate circuit techniques, it is important to understand the general form of the error for various device types. The standard deviation of matching error (which corresponds to the random mismatch) is usually inversely proportional to the size of the devices. For capacitors, the standard deviation of the matching error typically takes the form of [11]

$$\sigma_C = \frac{1}{\sqrt{C}} \sqrt{k_{a1} + \frac{k_{p1}}{\sqrt{C}}} \tag{2.5}$$

where ka1 and kp1 are the areal and peripheral fluctuation constants. The values of these constants are device, process, and layout dependent. The standard deviation of the matching error takes a very similar form for resistors [11]

$$\sigma_R = \frac{1}{W\sqrt{R}} \sqrt{k_{a2} + \frac{k_{p2}}{W}} \tag{2.6}$$

where W is the cross-sectional width of the resistor and ka2 and kp2 are again the areal and peripheral fluctuation constants. The threshold voltage and the transconductance parameter k' of FETs also exhibit matching error, with the standard deviation of these errors given by

$$\sigma_{Vth} = \frac{k_{a3}}{\sqrt{WL}} \tag{2.7}$$

$$\sigma_{k'} = \frac{k_{a4}}{\sqrt{WL}} \tag{2.8}$$

Equation (2.5)-(2.8) show that it is necessary to increase the physical size of the device to obtain better device matching, consistent with intuition regarding both peripheral and areal fluctuations. The required increase in device size usually results in a corresponding increase in power consumption in order to maintain the same system performance. Thus as in the cases of device noise and circuit nonidealities, the designer is faced with the tradeoff of increased performance for increased power consumption and die area.

CHAPTER III

APPLICATION AND SPECIFICATION OF ADC

The ADC has been targeted for a distributed chemical sensor network which uses distributed sensor motes to detect harmful molecules through an on chip Broadband Dielectric Spectroscopy (BDS) technique.
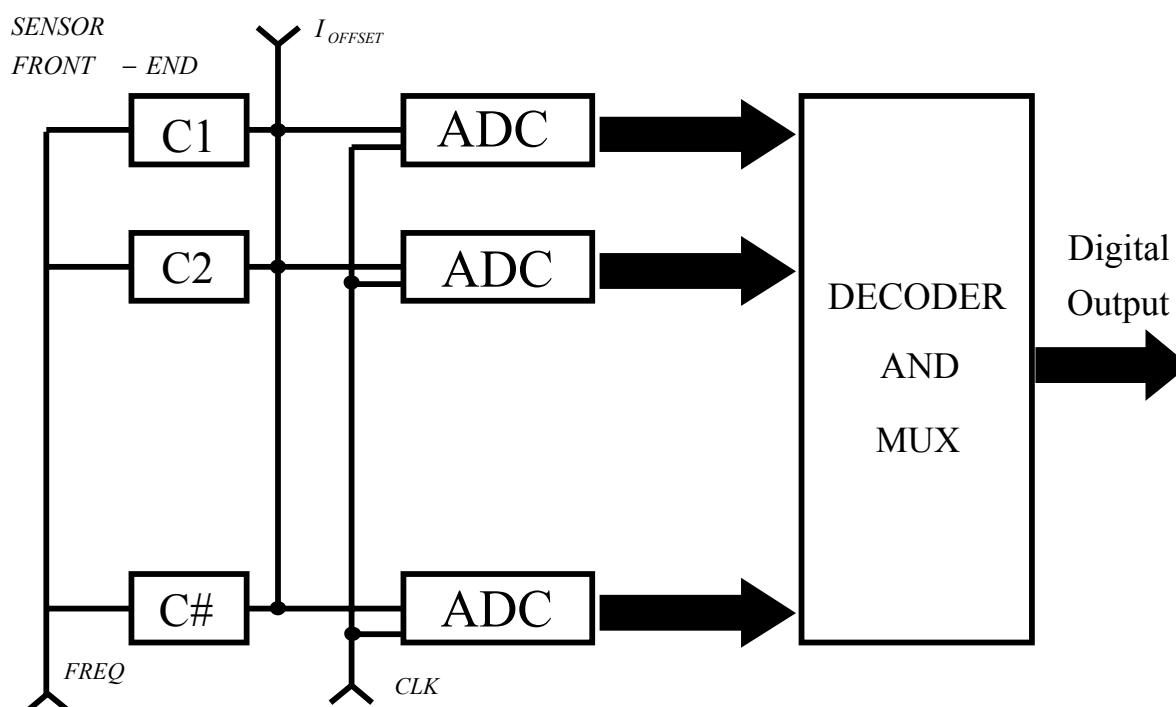

Figure 3.1 System level block diagram of the CMOS sensor IC.

Fig 3.1 shows a system level block diagram of the CMOS sensor IC. The sensor device used in this research is a Nanowell capacitor [13]. Recently, a novel innovative

photo-lithographic method was used to fabricate very large scale Nanowell arrays in silicon [14]. The lateral dimension of the Nanowell (10-100nm) is defined by anodic oxidation of Ti or Si (Fig. 3.2). The Nanowell, 10-50nm wide, 10 – 1000nm long and 60nm deep, is essentially a parallel plate capacitor. The dimension of the capacitor enables trapping of single biomolecules. Trapping of molecules is achieved through positive dielectrophoresis, in which a non-uniform electric field induces a net dipole moment and corresponding attractive force on a polarizable molecule. By tuning the frequency and the voltage applied to the Nanowell, the target molecules can be forced in a resonant motion for measurement. Moreover, by changing the frequency and voltage of the applied signal, we can alter the polarizability of the medium and the trapped molecules. It is a very useful technique to release the already trapped molecules from the Nanowell to alter the frequency and polarity of the electric field for the future use of the nano-capacitor [15]. Detection of the trapped molecules for its material properties is performed using broadband dielectric spectroscopy (BDS). BDS measures the complex permittivity of the molecule as a function of the frequency. An overview of the BDS technique is provided in the next section.

3.1 Broadband Dielectric Spectroscopy

Broadband Dielectric Spectroscopy (BDS) is widely used for investigating the characteristics of a great number of materials. The interaction of electomagnetic (EM) radiation with molecular system induces quantized transitions between the electronic, vibrational and rotational molecular energy states. Those interactions can be observed by UV/visible and infra-red absorption spectroscopies at the high frequency. The dielectric dispersion and absorption phenomena that occur in the wide high frequency range are due to the dipole relaxation arising from the reorientational motions of molecular dipoles and electrical conduction arising from the transitional motions of electric charge [15].
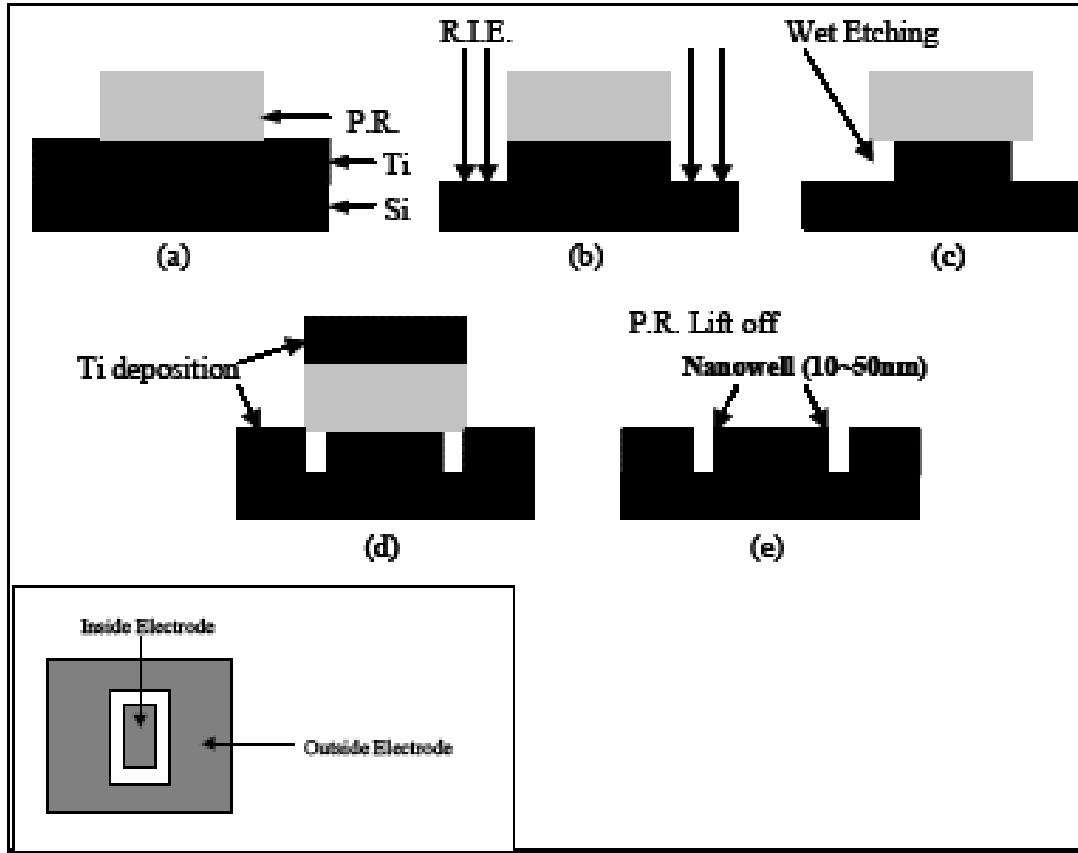
F**igure 3.2** Fabrication of the Nanowell device.
(Top view of the capacitor shown at the bottom)

Therefore, these effects can dominantly influence the dielectric properties of the material in the relevant frequency range. At the microelectronics side, the dielectric properties of the material are expressed by the complex electrical impedance. The underlying effects mentioned above and their impact on the impedance can be modeled by a couple of standard models such as Debye, Cole-Cole and Cole-Davison models [13].

$$\varepsilon = \varepsilon^* - j\varepsilon^{**} \tag{3.1}$$

$$\varepsilon^* = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1 + (\omega\tau)^2} \tag{3.2}$$

$$\varepsilon^{**} = \frac{\omega\tau(\varepsilon_s - \varepsilon_\infty)}{1 + (\omega\tau)^2} + \frac{\sigma_{dc}}{\omega\varepsilon_0} \tag{3.3}$$

The classical physical behavior of the frequency dependence of the real and imaginary parts of the permittivity was described by Debye [15]. His model can be summarized by (3.1), (3.2) and (3.3), where ε_∞ is the absolute value of the permittivity at infinite frequency, ε_s is the absolute value of the permittivity at zero frequency, ε_0 is the vacuums permittivity and σ_{dc} is the DC conductivity of the system. Fig.3.3 shows us the graphical way of expression of the frequency-dependence of the permittivity of the measured material according to (3.1), (3.2) and (3.3) [15]. BDS measures the real and imaginary part of the capacitance C = C(e,w), where e is the complex permittivity and w is the frequency of the applied electric field. Each molecule or combination thereof provides a unique signature in the dielectric spectrum as a function of frequency for purpose of detection and analysis.

If we can realize the cost-effective dielectric constant sensing CMOS circuitry with that tiny capacitor, we can build up a very good chemical or biological sensing system with the economical CMOS technology. One drawback of the CMOS technology for BDS is the limited frequency range for analysis. However for most molecules, the frequency range (0 ~ 1GHz) provide enough information for selectivity. Therefore, the sensing technique can emerge to be one of the promising sensing solutions with low cost.
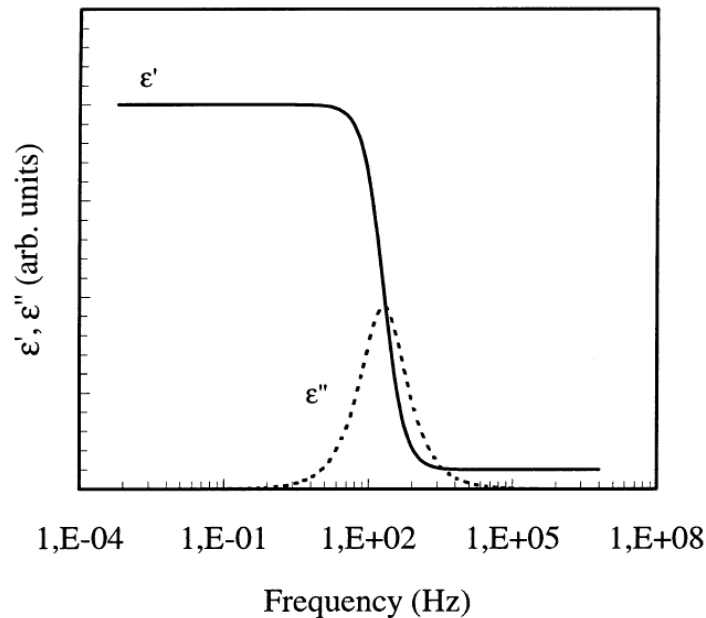
Figure 3.3 Sketch of the frequency variation of the real and imaginary parts of the complex relative permittivity of the material [16].

Fig. 3.4 shows the conceptual diagram of the front-end of the sensor [17]. First of all, the mismatch between the reference capacitor and the sensed capacitor is modulated and amplified using a common mode error amplifier working as the capacitance value detector in the first stage. Next, the modulated signal is demodulated at the mixer stage. The phase shifter should be applied between the oscillator and the mixer input to sense both of the amplitude change and the phase change by use of quadrature modulation. Since the demodulated signal has very weak signal power, we need an additional gain stage of a conventional OTA. Finally, the demodulated signal is low-pass filtered through the OTA-C filter and converted into current. The current domain output can then be fed to a low-power current-mode ADC for digitization [18,19].
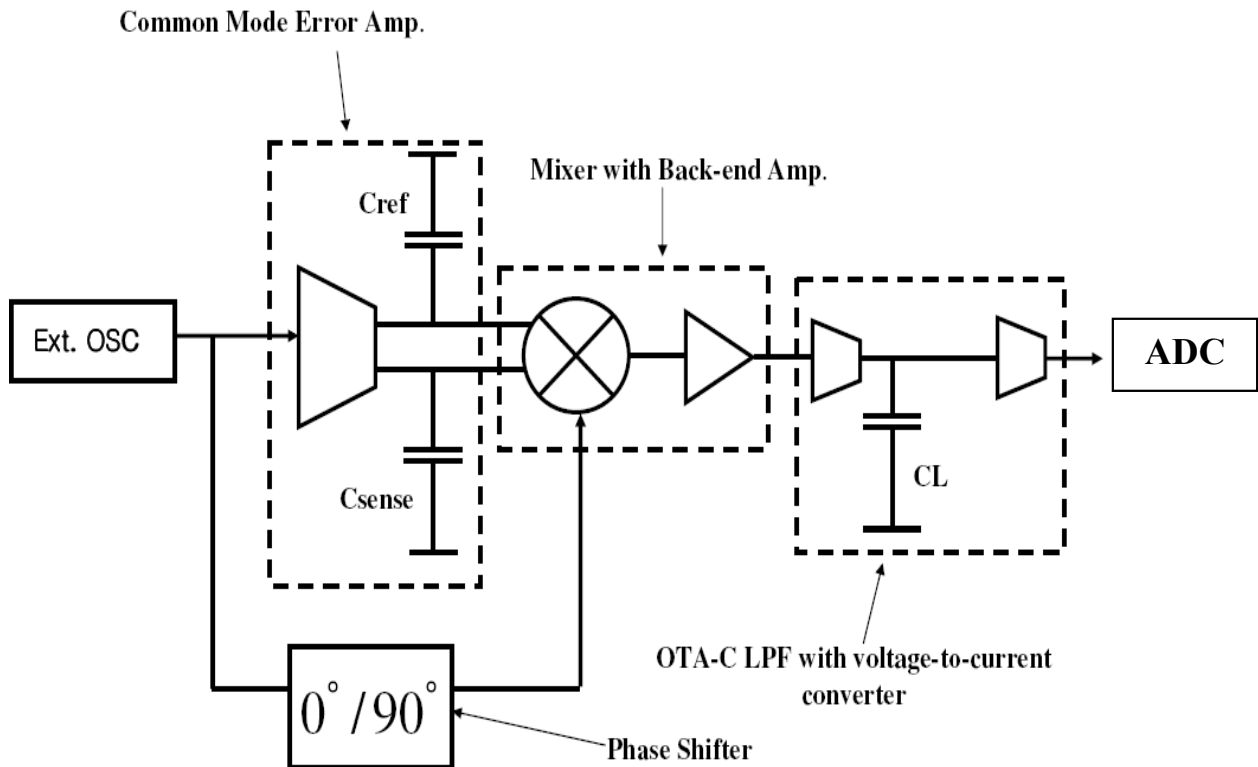
Figure 3.4 Conceptual diagram of the front-end circuit system showing the application of ADC.

3.2 Specification of ADC

In distributed sensor networks, the hardware and software burdens are moved from the individual sensor node and into the network as a whole. Each node may have very limited capability, but the entire network of sensor nodes can still be quite powerful by utilizing the collective sensing and processing of all the nodes. By reducing the capabilities of the individual nodes, they can be made to operate using very little energy while simultaneously relaxing the performance specifications. Given the modest performance requirements of the sensor node, the ADC specifications are not particularly stringent. Achieving higher performance would require an unnecessary increase in power consumption. Since the nodes are likely to have a variety of integrated sensors, it is desirable for the ADC architecture to have a rail-to-rail input conversion range. This allows for maximum use out of a single ADC. Ideally, the architecture only uses power when taking a sample, and then only uses as much energy as is absolutely necessary to compute the sample. Energy could be further saved if the sample resolution is dynamically adjustable. Given these considerations and the end application, the ADC was designed to meet or exceed the following performance specifications:

1. Resolution equal to 6-bits

2. Sampling rate greater than 100 kHz

3. Supply voltage of <1V (derived from two series solar cells)

4. Ultra low-power consumption (~ few μW)

5. Very small area

To obtain low-power consumption the ADC was designed with MOS transistors working in a subthreshold region, so that they can work under low-voltage and low current supply. Also current was chosen as the information carrying quantity (as explained in the next section).

3.3 Processing in Current Domain

For low-voltage ultra-low-power analog IC's the total design process must be considered, in which transfer quality plays a dominant role. The current becomes more favorable than voltage as the information-carrying quantity in a low-voltage and low-power environment [20].

Disadvantage of the use of voltage as the information-carrying quantity is that, when the circuits are "voltage-driven," i.e., from a low-impedance source, the equivalent input noise voltage is predominantly the result of the input noise voltage of the input stage. For bipolar transistors and CMOS transistors in weak inversion, this input noise voltage is inversely proportional to the bias (collector or drain) current, and thus, in order to obtain a low input noise voltage, these bias currents must be rather large. This, of course, is in sharp contrast with our low-power requirement.

When, however, the circuits are "current-driven," thus with a high impedance, the equivalent input noise current is mainly determined by the input noise current of the input stage. Since the equivalent input noise current of bipolar transistors is proportional to the bias current, this call for small bias currents, which is in line with the low-power requirement. This favors the choice of current as the information-carrying quantity.

The influence of parasitic admittances in parallel with the signal path can be reduced by terminating the signal path with low impedance. The parasitic admittances then have no voltages across their terminals and thus no current flows in them. The influence of parasitic impedances in series with the signal path can be reduced by terminating the signal path with high impedance. Then no current flows in the parasitic impedances and thus there is no voltage across their terminals. In low-power integrated circuits, often the parasitic admittances, i.e., the node capacitances, e.g., the transistors junction capacitances, due to their (non-linear) voltage dependency, have more influence on the signal behavior than the parasitic impedances, i.e., the branch inductances and resistances, e.g., the transistors' bulk resistances. Therefore it is convenient to terminate the signal paths with low impedances as much as possible. In this situation it is best to choose current as the information-carrying quantity.

Current-mode signal processing techniques have been extensively adopted in several applications that involve low-power, high-speed, or complex arithmetic computation in integrated circuits. Such applications include data converters, filters, and cellular neural networks [21]-[23]. Current-mode ICs have several important features. First, current-mode circuits can easily implement the basic functions of inversion, scaling, and summation, without using op amps [24]. Second, the voltage swing required in current-mode circuits is smaller than that required in voltage-mode circuits. Third, the current switch can achieve high-speed operation in many applications. These features make the high-performance current-mode design feasible.

CHAPTER IV

ADC ARCHITECTURE

When designing ultra-low-power circuits, energy considerations drive the design process from the choice of architecture all the way to the actual circuit Implementation. Choosing architecture is a critical point in the design process for such systems. A proper choice of architecture can lead to dramatic energy savings compared with alternatives. Conversely, a poor architectural decision can result in a sub-optimal design regardless of how well the individual circuit blocks are designed. While energy consumption is paramount in this application space, there are many other considerations driving the choice of ADC architecture.

4.1 ADC Architecture Survey

Figure 4.1 groups various ADC architectures that vary roughly by their achievable resolution, speed and power consumption [25]. Since low-power consumption is the primary design goal, Figure 4.1 shows that many architectures are poor choices. Time interleaved ADCs require multiple sets of analog hardware, leading to high power consumption but very fast sampling rates [26]. Flash converters [27] use a large number of comparators
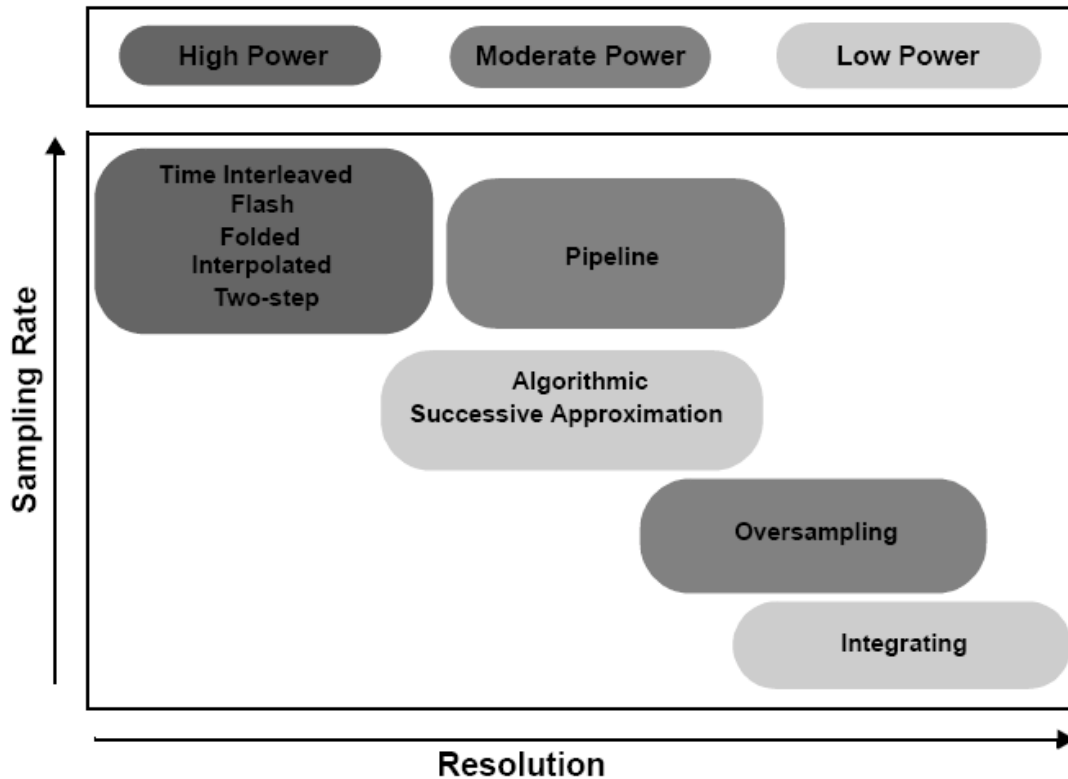
Figure 4.1 Common ADC architectures grouped by resolution, sampling rate and power consumption (adapted from [25]). The boundaries shown and power consumption categories are purely representative, as individual ADC performance and power consumption varies significantly.

for a given resolution, making them impractical in most applications requiring more than 8 bits of resolution. Folding and/or interpolation [28] can help reduce the number of comparators required, but the architecture is still not well suited for low-power applications. Multi-step [29] ADC also require a relatively large amount of analog hardware, resulting in excessive power consumption for application in distributed sensor networks.

Some of the other ADC architectures, such as Delta-Sigma, Successive Approximation, Integrating and Algorithmic, have been reported to work with low-power consumption, low supply voltage and with moderate resolution and speed [30]-[32]. Some of the already existing low–power architectures are reviewed.

1) Delta- Sigma ADC
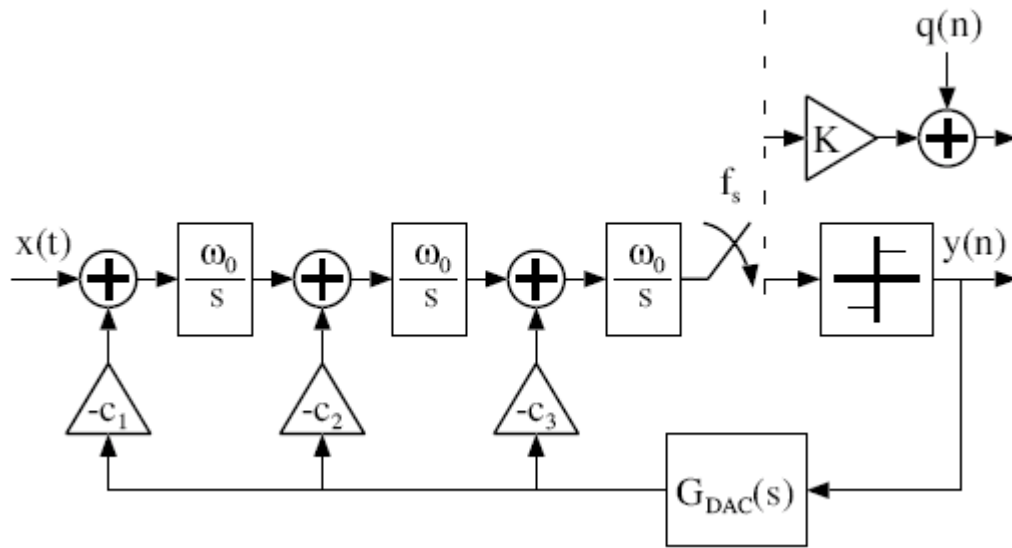
Figure 4.2 Continuous-time 3rd order Σ Δ-modulator block diagram [32].

Fig 4.2 shows the block diagram of a third order low-pass Σ Δ ADC employing a continuous time loop filter. The ADC [32] was reported to have a resolution of 10 bits and a dynamic range (DR) of 67 dB at a sampling rate of fs = 1.4MHz, while drawing a bias current of 60 μA from a modest supply voltage of 1.8V, thus consuming 108 μW of power. The ADC was designed in a 0.35-μm CMOS technology.

2) Successive Approximation

Shown in Fig 4.3, the successive approximation architecture uses only one comparator, along with simple digital logic and a switching network to implement the search algorithm. The ADC [30] was designed in a 0.25-μm CMOS process and was reported to consume 31pJ/8-bit sample at 1-V supply and 100 KS/s.

Figure 4.3 Successive approximation architecture (shown for an 8-bit converter) [30].

Fig 4.4 shows the modified successive approximation architecture used. The ADC [31] was designed in a 0.18-μm CMOS process and had a power consumption of 30 μW and 0.85 μW for supply voltages of 1 and 0.5 V, at sampling rates of 150 and 4.1 KS/s, respectively.

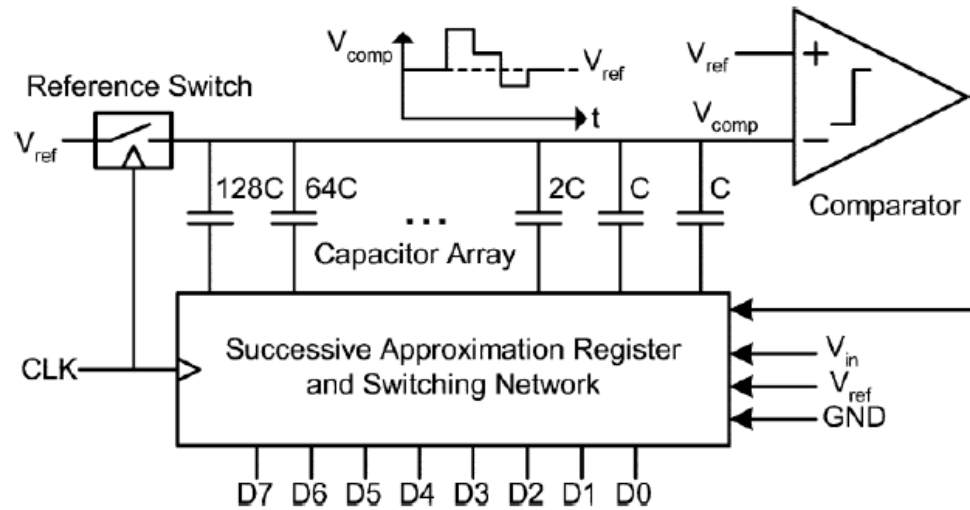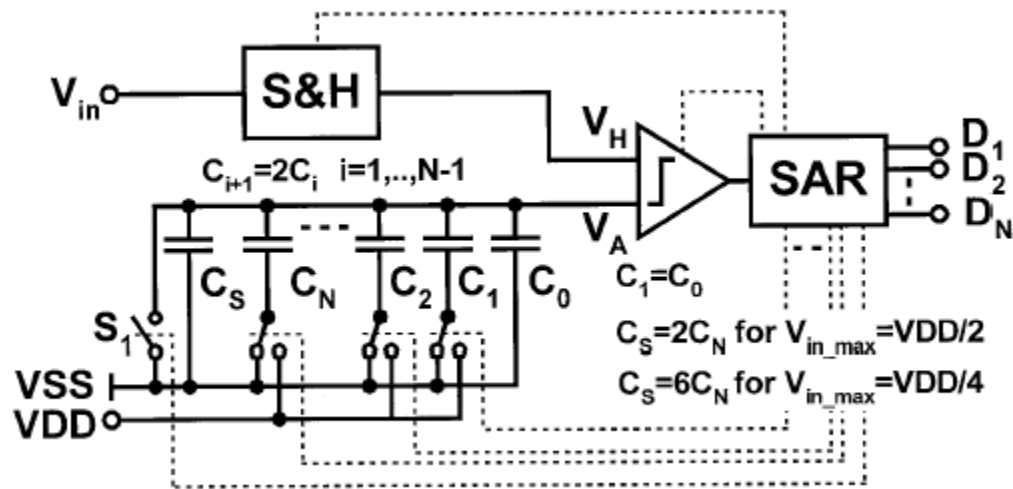**Figure 4.4** Modified successive approximation architecture [31].

3) Integrating ADC
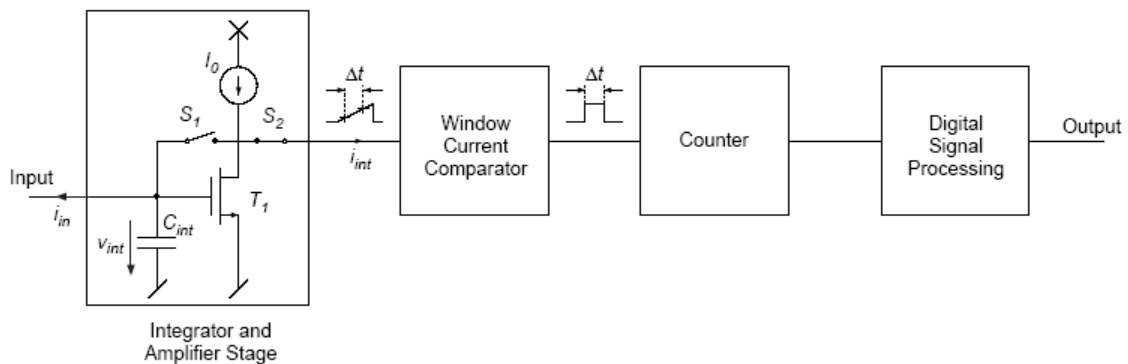
Figure 4.5 Block diagram of the integrating ADC architecture [33].

Fig 4.5 shows an integrating ADC using a single transistor as integrator and amplifier for very low (1 fA minimum) input currents. The ADC [33] was designed in a 1-μm CMOS process and supply voltage was 3.3 V.

4) Algorithmic/Cyclic Architecture

Fig 4.6 shows the classical cyclic/algorithmic topology with 1.5 b per cycle. The ADC [34] consumption, measured on 10 chip samples and averaged, was reported to be 8.18 μW for the analog part and of 9.71 μW for the digital one, using a supply battery of 2.8 V. The converter has a resolution of 10-b, its typical operating clock frequency is 32 KHz (2.9 KS/s sampling rate) and is able to reach the same resolution at 2 V (0.7 KS/s sampling rate), with a dissipation of 1 μW and 1.3 μW for analog and digital part, respectively. The circuit has been fabricated in AMS BiCMOS 0.8-μm BYQ technology.
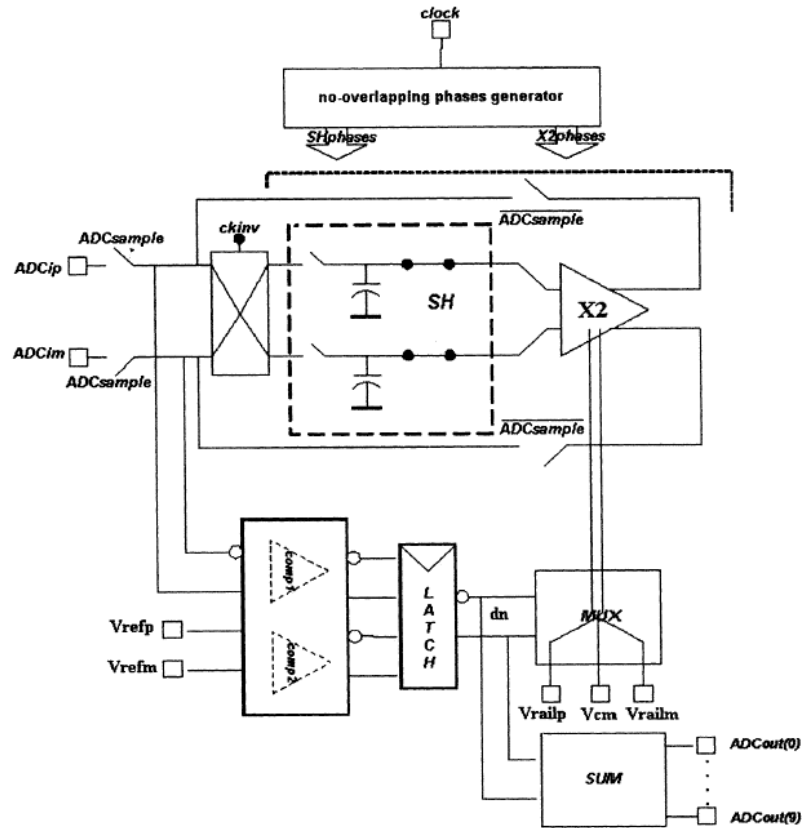
Figure 4.6 Algorithmic ADC schematic diagram [34].

The features of all the ADCs are summarized in the Table 4.1.

Table 4.1 Summary of performances of low-power ADCs.

Architecture	Technology	Supply voltage	Sampling Rate	Power(μW)
Delta-Sigma [32]	0.35-μm CMOS	1.8 V	1.4 MS/s	108
Successive Approximation[30]	0.25-μm CMOS	1V	100 KS/s	3.1
Successive Approximation[31]	0.18-μm CMOS	1 V	150 KS/s	30
		0.5 V	4.1 KS/s	0.85
Integrating [33]	1-μm CMOS	3.3 V	-----	-----
Algorithmic [34]	AMS BiCMOS 0.8-μm BYQ	2.8 V	2.9 KS/s	8.18 + 9.71
		2 V	0.7 KS/s	1 + 1.3

Oversampled converters such as sigma-delta converters are potentially viable for this application. Sigma-delta ADCs can be made to be low-power [35] for a given resolution and sampling rate, however they are complex–requiring sophisticated clocking and filtering. In addition, the oversampled clock needs to be much faster than the desired sampling rate. Generating the oversampled clock on each sensor node would likely offset any energy savings achieved in the rest of the ADC.

Continuing the survey of common architectures, integrating (single and dual slope) converters [25] possess many of the desired architectural features. They require very little analog circuitry, making them very low-power. However they require accurate timing which may be difficult to achieve without a high precision clock. It is unlikely that such a clock would exist on the mote since generating this clock could consume quite a lot of power due to the precision requirements. Another disadvantage is that the conversion speed is very slow, in addition to the fact that the conversion period varies with input signal. The variable conversion period complicates the overall system design for the sensor node as a whole as different ADC samples will take different amounts of time.

The charge redistribution successive approximation architecture [25], [30], [31] is a viable architecture for this application space. The general architecture of a general successive approximation ADC usually consists of a rail-to rail analog comparator, a digital-to-analog converter and a successive approximation register (SAR). In general, the SAR is designed into the digital circuitry. The DAC required in the ADC is designed based on a R-2R ladder. Thus, both of them are suitable for the standard CMOS technology VLSI implementation. However, realizing high-accuracy and rail-to-rail MOS comparator concurrently remains a problem because of MOS device mismatches [5], [6] and threshold voltage limitations [7]. Also the accuracy of a successive approximation converter depends on the matching accuracy of the on-chip passive components because the converter employs the ratio matched components as a precision reference element. In order to maintain ratio accuracy, such precision components require a large area and cannot be easily scaled down.

Algorithmic converters [36] offers all the advantages of the successive approximation architecture, while combining full flexibility to choose current as the

information carrying quantity. Current-mode circuits offer the advantages of inherent low-voltage swing and no need for linear capacitors, as opposed to that used in switched capacitor techniques for voltage-mode algorithmic ADC's.

Another advantage of algorithmic converter block is that it can be easily repeated to make a pipelined algorithmic converter by simply placing a current-mode sample and hold blocks (SI) in between each block [18]. The energy consumption depends on the number of blocks cascaded i.e. N, where N is the number of bits of resolution desired in the resulting conversion.

Recently, current-mode circuit techniques which process the active signals in the current domain have been proposed to design the current-mode ADC [19], [37], [21].Thus, they are suitable for low-voltage applications. Though Nairn and Salama has demonstrated a 6-bit current-mode algorithmic ADC [19] with very small chip area and low-power dissipation, enhancements were needed to further reduce the power consumption and to reduce the supply voltage without significantly increasing the chip area. Thus, the current-mode algorithmic ADC was chosen and the architecture was modified as to work with low-voltage and current supply as to have low-power consumption. The design presented makes use of the transistors operating in subthreshold region, so that the can work under low-voltage and low current supply.

CHAPTER V

SUBTHRESHOLD REGION

One of the novel features of the design of the current-mode ADC proposed in this project is that it consumes ultra low-power. Such low-power consumption can be achieved by many techniques which makes low-voltage application possible. Few of these techniques are using bulk-driven MOSFETs [38], floating gate MOSFETs[39] etc. But low-voltage alone is not sufficient to achieve ultra low-power, current consumption should also be lowered accordingly and moreover the above mentioned techniques have other issues associated with them, like higher input referred noise due to smaller equivalent transconductance. To achieve ultra low-power operation in this design, the transistors were operated in subthreshold or weak inversion region of operation. So operation of MOSFET in this region, its modeling, its noise analysis and its leakage problem need to be discussed.

5.1 Operation in Subthreshold Region

Subthreshold or weak inversion conduction current between source and drain in an MOS transistor occurs when gate voltage is below V_{th} (threshold voltage). The weak inversion region is seen in Fig.5.1 as the linear region of the curve (semilog plot) [40]. In the weak inversion, the minority carrier concentration is small, but not zero.
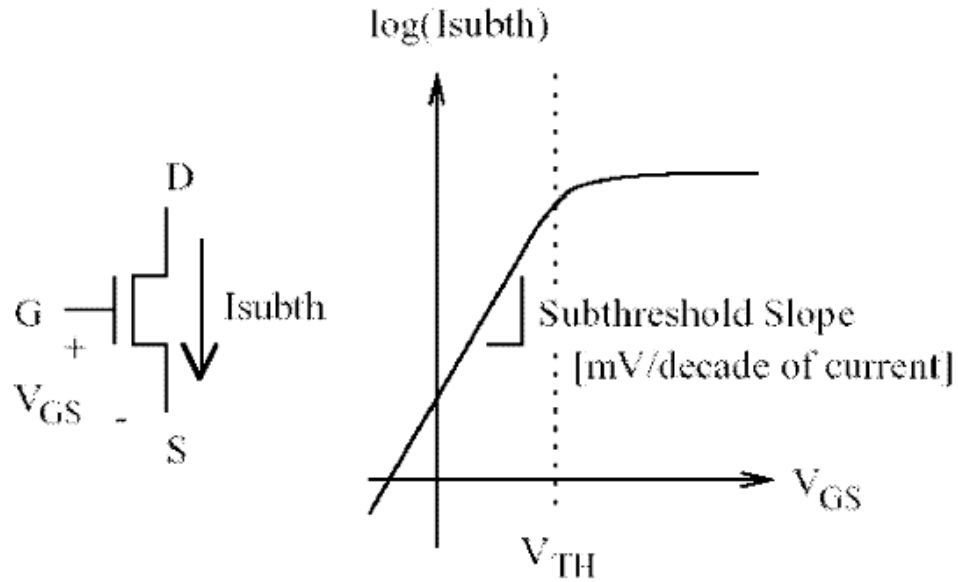
Figure 5.1 Subthreshold current in a NMOS transistor. The weak inversion region is shown as the linear region of the curve.

Fig. 5.2 shows the variation of minority carrier concentration along the length of the channel for an n-channel MOSFET biased in the weak inversion region [40]. Let us consider that the source of the n-channel MOSFET is grounded, $V_g < V_{th}$, and the drain to source voltage $|V_{ds}| > 0.1$ V. For such weak inversion condition, V_{ds} drops almost entirely across the reverse-biased substrate-drain pn junction. As a result, the variation of the electrostatic potential ϕ_s at the semiconductor surface along the channel (the y axis) is small.

Figure 5.2 Variation of minority carrier concentration in the channel of MOSFET biased in weak inversion.

The component of the electric field vector E(Ey), being equal to, $\partial\phi/\partial y$ is also small. With both the number of mobile carriers and the longitudinal electric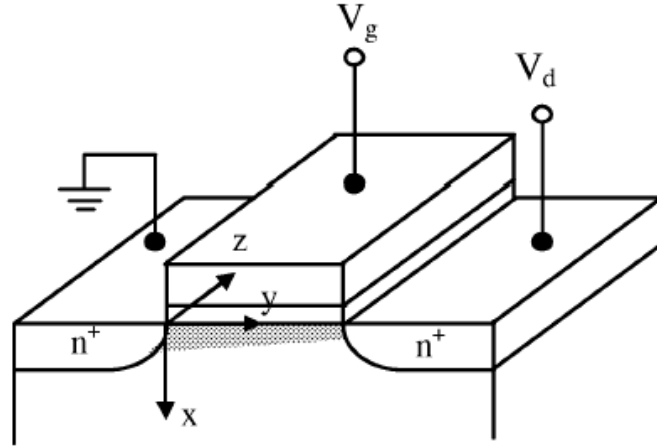 field small, the drift component of the subthreshold drain-to-source current is negligible. Therefore, unlike the strong inversion region in which the drift current dominates, the subthreshold conduction is dominated by the diffusion current. The carriers move by diffusion along the surface similar to charge transport across the base of bipolar transistors. The exponential relation between driving voltage on the gate and the drain current is a straight line in a semilog plot of ID versus Vg (see Fig. 5.1). Weak inversion typically dominates modern device off-state leakage due to the low V_{th}. The weak inversion current can be expressed based on the following [41]:

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L} (m-1)(\upsilon_T)^2 \times e^{(V_g - V_{th})/m\upsilon_T} \times (1 - e^{-\upsilon_{DS}/\upsilon_T}) \tag{5.1}$$

where

$$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\dfrac{\varepsilon_{si}}{W_{dm}}}{\dfrac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}} \tag{5.2}$$

where V_{th} is the threshold voltage, and υ_T =kT/q is the thermal voltage. C_{ox} is the gate oxide capacitance; μ_0 is the zero bias mobility; and m is the subthreshold swing coefficient (also called body effect coefficient). W_{dm} is the maximum depletion layer width, and t_{ox} is the gate oxide thickness. C_{dm} is the capacitance of the depletion layer.

5.2 Modeling in Subthreshold Region

The accurate modeling of MOS transistors in moderate and weak inversion regions are not guaranteed as moderate region is considered just a transition region through which one fits an approximate curve. So couple of tests should be performed to verify the modeling of the MOSFET [42], which were finding in accordance with the required graphs. The graphs were obtained by simulating a NMOS transistor in Cadence, whose drain was given a fixed dc bias, source was grounded and gate voltage was swept over the entire range. The simulation was performed so as to confirm if the MOS device is modeled correctly for weak inversion region of operation. Fig 5.3 and Fig 5.4 confirmed the modeling [42]. This was important since all the blocks in ADC are using transistors working in subthreshold region; hence the simulation performed on these blocks and as a result on the overall ADC will give the accurate results.
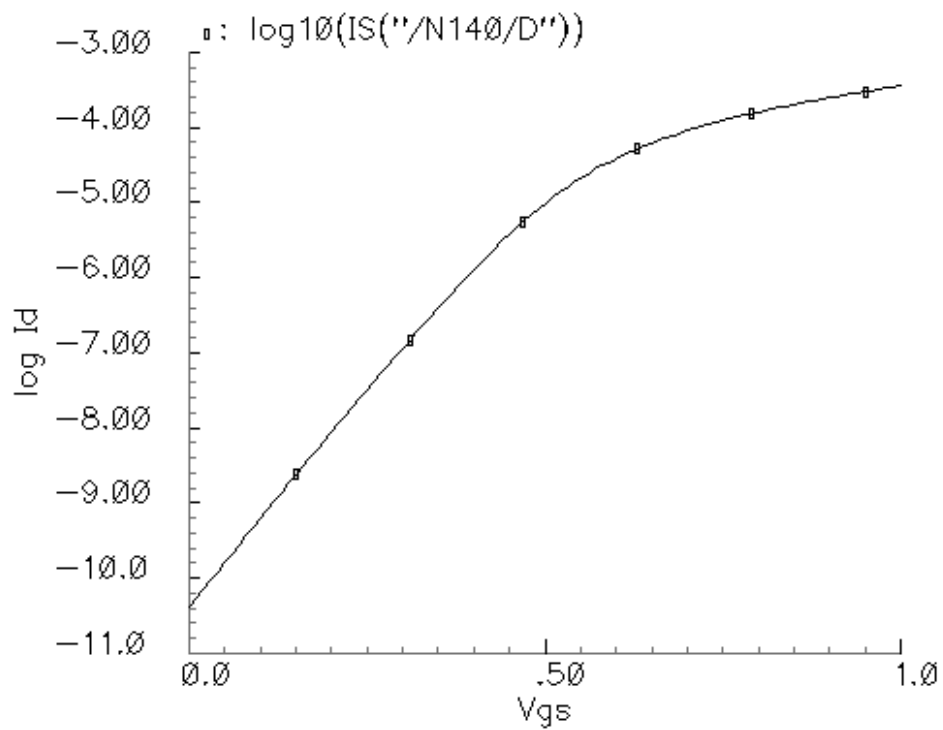
□: log10(IS("/N14Ø/D"))

Figure 5.3 Log Id versus Vgs for fixed Vds.

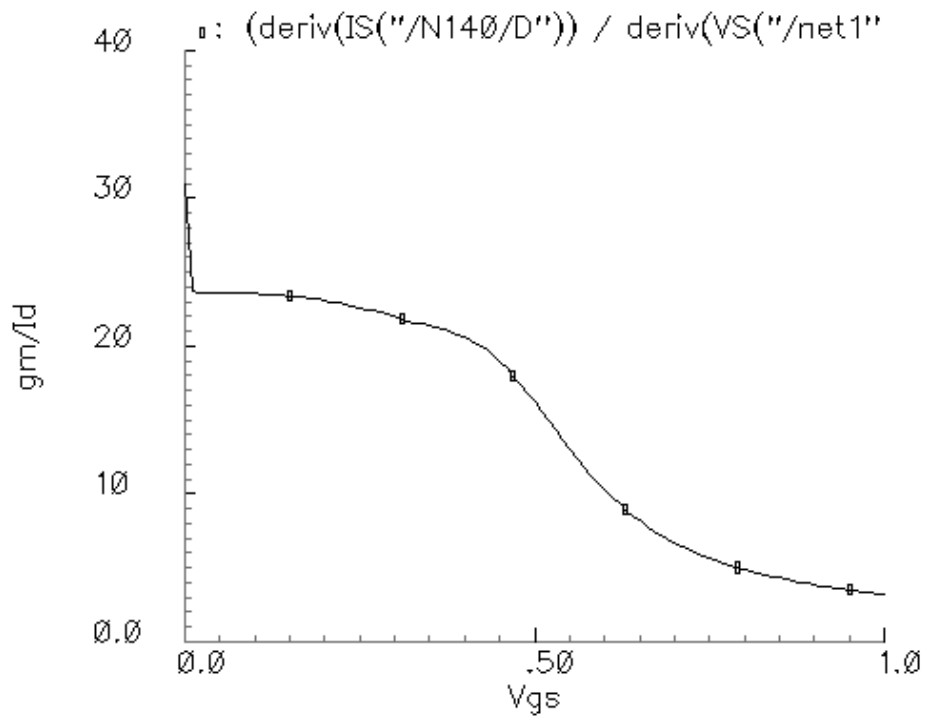□: (deriv(IS("/N14Ø/D")) / deriv(VS("/net1"

Figure 5.4 gm/Id versus Vgs .

5.3 Noise in Subthreshold

The excess noise of CMOS transistors is dominated by 1/f noise up to relatively high frequencies of the order of several tens of kilohertz[43]. SPICE models are commonly used as a basis for analog design. The basic SPICE noise model equation for the drain current of CMOS transistors, which consider the low frequency noise, is

$$S_{I_d} = \frac{KF.I_d^{AF}}{f^{EF}C_{ox}WL_{eff}}$$

(5.3)

Where

S_{Id} drain 1/f noise current spectral density;

I_d drain current;

C_{ox} oxide capacitance per unit area;

KF flicker noise coefficient;

AF flicker noise exponent;

EF flicker noise frequency exponent;

W, L_{eff} width and effective length of the transistor gate area, respectively

At weak inversion below threshold [43]

$$S_{V_g} \cong \frac{1}{C_{ox}^2} S_{Q_{inv}}(f) = \frac{1}{C_{ox}^2}\left[\frac{C_{inv}}{C_{ox}+C_d+C_{inv}}\right]^2 \frac{q^2 N_{ot}}{WL}\frac{1}{f}$$

(5.4)

where C_d and C_{inv} are, respectively, the depletion and the inversion capacitance. N_{ot} is the equivalent density of oxide traps, which is defined as

$$N_{ot}\left[cm^{-2}\right] = \frac{kTN_t(E)}{\gamma}$$

(5.5)

and $N_t(E)$ [cm^{-3}eV^{-1}] is the density of oxide traps per unit volume and unit energy, while γ is the McWhorter tunneling parameter, which depend on the effective of the tunneling carrier as well as the barrier height.

Since at subthreshold $C_{inv} \ll C_{ox} + C_d$ and the capacitive ratio between the oxide capacitance and the depletion capacitance is defined by n= $(C_{ox} + C_d)/C_{ox}$, then

$$S_{V_g} \cong \left[\frac{C_{inv}}{C_{ox}}\right]^2 \frac{1}{n^2} \frac{q^2 N_{ot}}{C_{ox}} WL \frac{1}{f} \tag{5.6}$$

Hence, the model predicts that at subthreshold S_{Vg} will be significantly reduced compared to that in saturation. At subthreshold, the drain current is related to gate voltage by $I_d = I_o \exp(qVg/nkT)$, where n is determined by the capacitive divider ratio defined above. Hence, $g_m = qI_D C_{ox}/kT(C_{ox} + C_d)$ and

$$S_{I_d} = \frac{C_{inv}^2}{(C_{ox} + C_d)^4} \frac{q^4}{(kT)^2} I_d^2 \frac{N_{ot}}{WLf}$$

$$= \left(\frac{C_{inv}}{C_{ox}}\right)^2 \frac{1}{n^4} \left(\frac{q}{kT}\right)^2 \frac{q^2 N_{ot}}{C_{ox}^2} \frac{I_d^2}{WL \cdot f} \tag{5.7}$$

Expression (5.7) predicts that S_{Id} increases with I_d^2 as shown by the experimental results discussed below. Expression (5.7) corresponds to the SPICE equation (5.3), if $KF = (C_{inv}^2/C_{ox}^3)(1/n^4)(q/kT)^2 q^2 N_{ot}$ and for AF=2, EF=1. Once again the voltage dependence induced by N_{ot} is not considered. In addition, there is a voltage dependence of C_{inv} that can be considered only roughly constant assuming $\phi_s = (3/2) \phi_f$ where ϕ_s is the silicon band loading and ϕ_f is the Fermi energy level. Also, it must be noticed that due to the difference in the value of AF between the linear or saturation region and the subthreshold region, KF has different dimensions. Namely, KF is measured in [Amper X F] in the saturation and the linear region, and in [F] in the subthreshold region.

5.4 Leakage in Subthreshold

The prominence of leakage currents in modern integrated circuits (ICs) has been spurred by the continued scaling of both supply voltage and threshold voltage [44]. Leakage currents for advanced CMOS technology include conventional DIBL leakage and gate leakage. The DIBL leakage characteristics exhibit surface punchthrough conduction mechanisms that are exponentially dependent on channel length, drain bias

and temperature. The gate leakage current depends exponentially on oxide thickness and gate bias. The most critical bias for gate leakage corresponds to $V_{gate}=V_{DD}$ and $V_{drain}=0V$ where the leakage current occurs across the entire device area. The conventional off-state bias of $V_{gate}=0V$ and $V_{drain}=V_{DD}$ will have an increasingly significant contribution from the gate due to tunneling; however, the magnitude of gate leakage is very small since the effective tunneling area is concentrated at the gate to drain overlap region. The comparison of BSIM3 fit and analytical fit for current dependence on gate length in shown in Fig 5.5. [44]
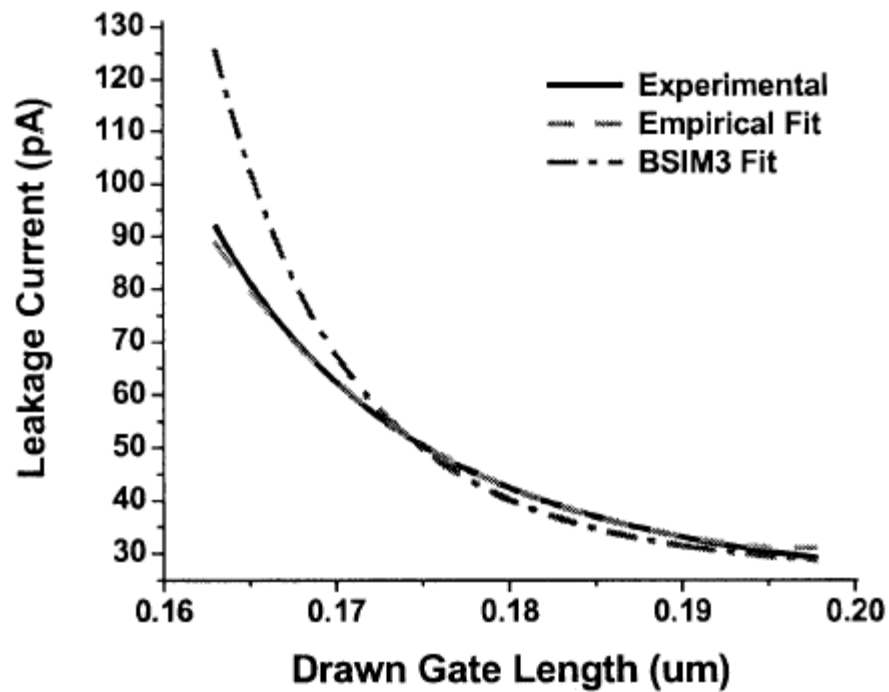
Figure 5.5 Comparison of BSIM3 fit and analytical fit for I dependence on gate length [44].

5.5 Summary

As expression (5.7) shows that noise power is directly proportional to the drain current so the reference current chosen in the design of ADC was very small 150nA, which in turn also lead to low-power consumption. Also the area of MOSFET i.e. W and L were chosen large as that too reduces the total noise.Fig 5.5 makes it clear that larger

the gate length, smaller is the leakage current. Hence, gate lengths were made larger and thus, the overall leakage current is effectively negligible as we are dealing with currents in nano-amperes and the leakage current is in the order of few pico-amperes.

CHAPTER VI

CURRENT-MODE ALGORITHMIC PIPELINE

The final choice of the current-mode algorithmic pipelined converter was driven by energy considerations, ease of design, and hardware flexibility. The operation of the ADC is relatively straight forward. To produce 6-bit algorithmic pipelined current-mode converter 6-bit cells are cascaded with output current of one cell connected to the input of the following cell. A current-mode S/H block was introduced between each cell to make pipelined operation possible as illustrated in Fig 6.1. The input current is compared with the reference current during the conversion cycle to perform a 1-b algorithmic analog-to-digital conversion [19]. The input to the following stage is dependent upon the decision made in the previous stage. If the input current is I_{in} the output I_{out} is given as follows

$$I_{out} = \begin{cases} 2I_{in} \\ 2I_{in} - I_{ref} \end{cases} if \begin{cases} 2I_{in} < I_{ref} \\ 2I_{in} > I_{ref} \end{cases} \qquad \textbf{(6.1)}$$

In pipeline ADC each stage carries out an operation on a sample, provides the output for the following sampler, and, once that sampler has acquired the data, begins the same operation on the next sample. Thus, at any given time, all the stages are processing different samples concurrently, and hence the throughput rate depends only on the speed of each stage [6].

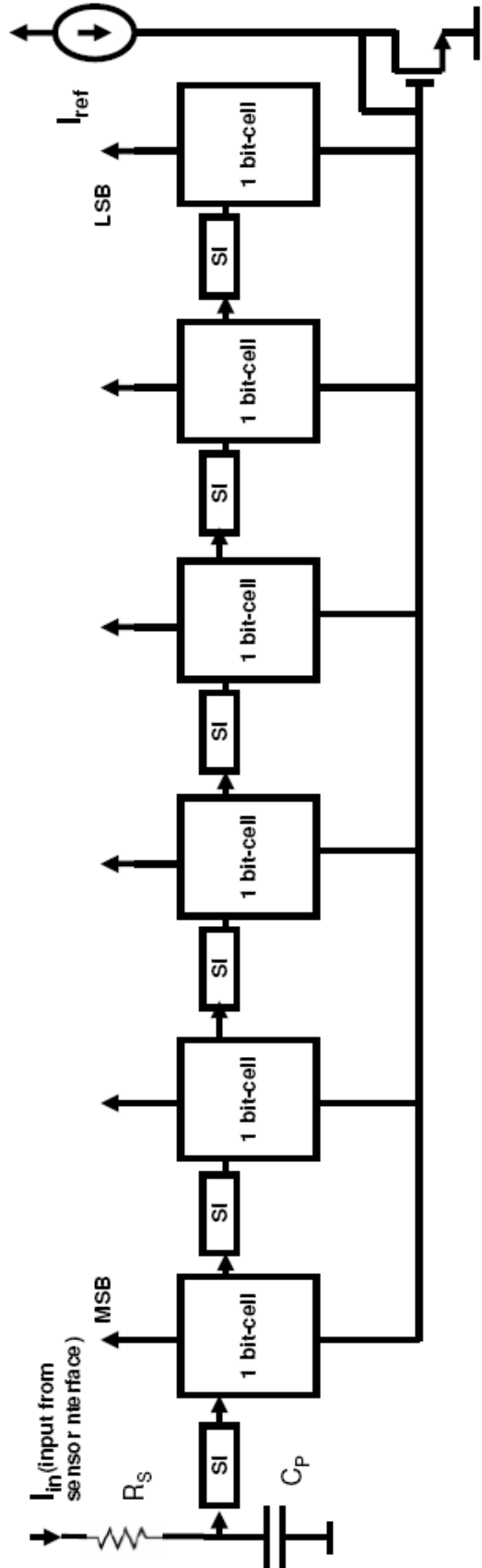**Figure 6.1** 1-bit cells are cascaded to form a 6-bit algorithmic pipelined converter. SI block is the current-mode sample and hold block. I_{ref} is the reference current which is mirrored in all the blocks by using a diode connected transistor.

6.1 Circuit Building Blocks

It is important to analyze the function of every circuit building block and how the implementation and performance of those blocks will affect the ADC as a whole. Understanding these relationships is important in order to achieve a final design which will in fact meet all of the desired specifications. The important point here was that all the blocks had transistors working in ***subthreshold or weak inversion*** region.

The ADC was designed in TSMC SCN6M_DEEP CMOS 0.18μm technology.

6.1.1 1-bit Stage

The circuit schematic of the 1-bit stage is shown below. The conversion is explained as follows [19]. The current input I_{in} is first doubled using the current mirror composed of M1 and M2, where M2 is twice the size of M1. The signal $2I_{in}$ is mirrored from M4 through M5 to the comparator and through M6 to the output. Comparator is used to compare $2I_{in}$ with I_{ref}, the reference current (from M11). If $2I_{in}$ is less than I_{ref}, the digital output goes low and M8 remains off, resulting in an output current of $2I_{in}$ (from M6). On the other hand, if $2I_{in}$ exceeds I_{ref}, the digital output will be high causing M7 to be on. With M7 on, I_{ref} from M8 and M9 will be subtracted from $2I_{in}$ (from M6) resulting in an output current of $2I_{in}$-I_{ref} which is equivalent to the residue of the conversion. This completes the 1-b algorithmic conversion. A low biasing trickle current was continuously provided through the mirroring transistors to maintain their operating point. The biasing circuit is also shown and to implement the cascode current mirror, the low-voltage implementation was used due to headroom voltage considerations.

Special attentions need to be taken during the layout of the bit-stage as slight mismatches can lead to wrong mirroring and this error propagates to the other stages, causing missing codes. Fig 6.2 shows that the threshold voltage of the MOSFET doesn't vary much if channel length used are larger. Hence to improve the device matching, both the channel length and channel width was selected to be significantly larger than the minimum feature size [45] Fig 6.2. Though, ideally all the bit stages should be identical but there was slight difference between the first stage and rest of the stage because of the biasing

current used in the circuit. The transistors M3 and M3' shown in the first stage (Fig 6.3) are not present in the rest of the stages as the required I_{bias} is provided by the previous, stages irrespective of the digital output.
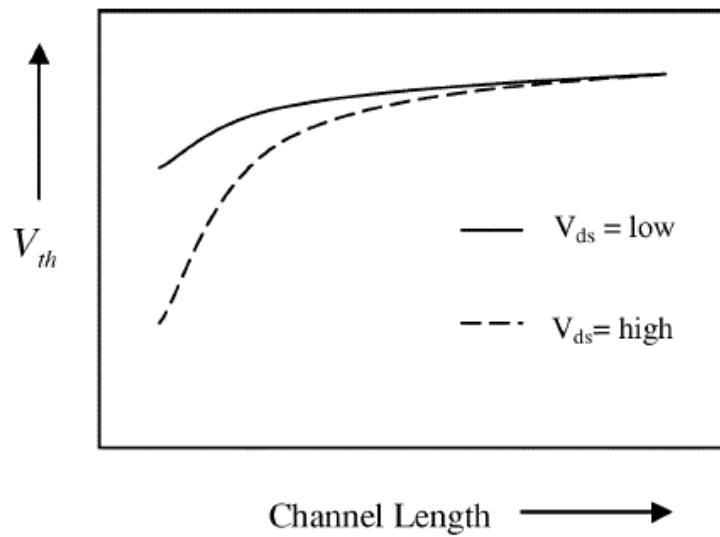

Figure 6.2 Threshold voltage rolloff with change in channel length; V_{th} reduction is more severe at higher drain bias.
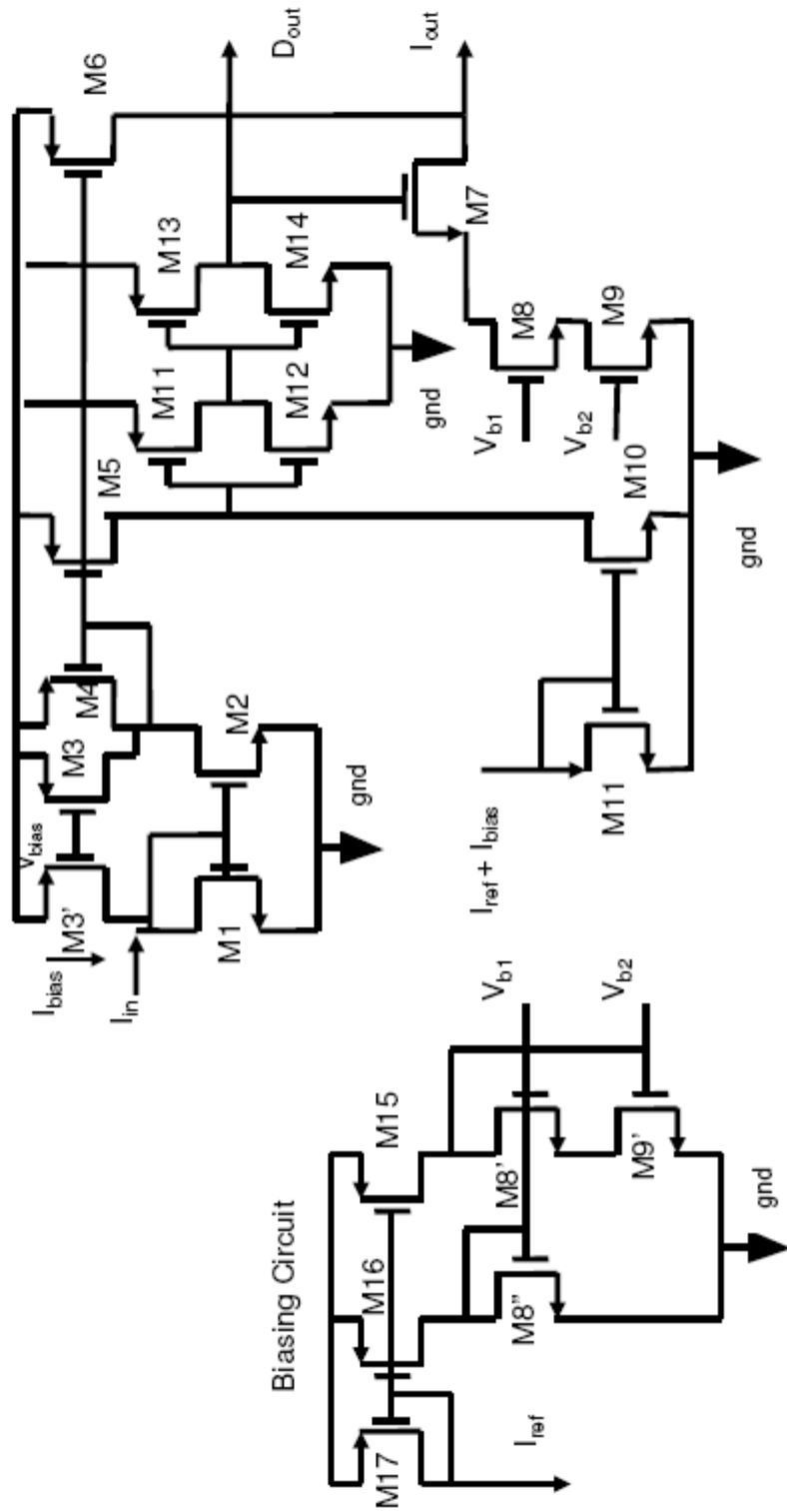
Figure 6.3 A 1-bit cell, which performs the current-mode algorithmic conversion. Two inverters are cascaded to form the comparator.

Fig 6.4 and Fig 6.5 shows the 3dB bandwidth and the input referred noise current density for the 1-bit stage respectively.
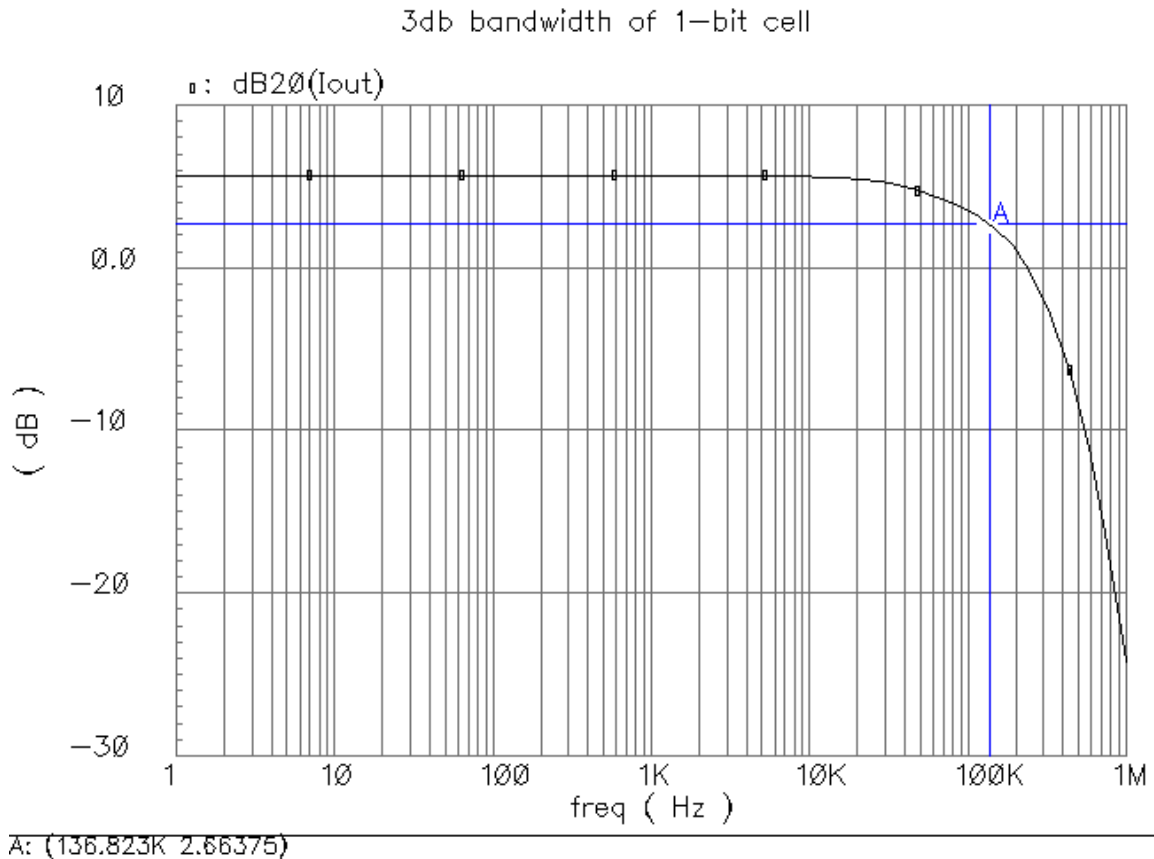

Figure 6.4 3dB bandwidth of the bit cell. The BW was around 136KHz.

The total noise of the ADC is dominated by 1/f noise as it is operating at low frequencies. Drain current I_d, was chosen to be a small number which satisfy both are low-power and low noise requirement. Also the total input referred noise should be atleast 2-5 times less than the minimum detectable signal value. Since the input current varies from 0-150 nA and 1 LSB current value is 2.34 nA ($\frac{150nA}{2^6}$), so taking minimum detectable signal value to be 0.6 nA (~LSB/4). The input referred noise sould be 2-5 times less than the value calculated by

$$\sqrt{\frac{(\min Signal)^2}{B.W}} = \sqrt{\frac{(0.6 \times 10^{-9})^2}{136 \times 10^3}} = 1.627 \frac{pA}{\sqrt{Hz}} \qquad \textbf{(6.2)}$$

The simulated value from Fig 6.5 is around $750 \frac{fA}{\sqrt{Hz}}$ which is around 2-3 times less than the value in equation 6.2 and hence in acceptable limit.
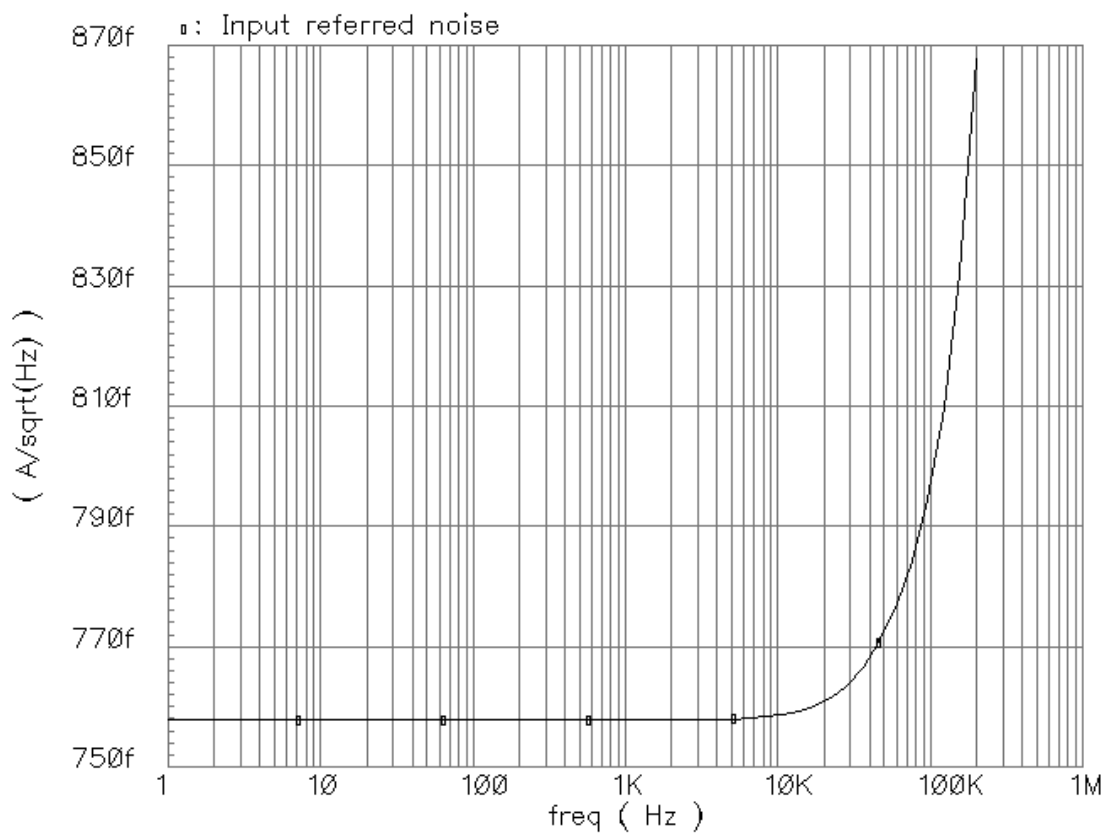
res input_noise schematic

Figure 6.5 Input referred noised density for the bit cell. The transistors in bit-cell are working in weak inversion region.

6.1.2 Current S/H Circuit (SI Block)

In its simplest form the SI block (current-mode sample and hold) can be implemented as shown in Fig 6.6[46].
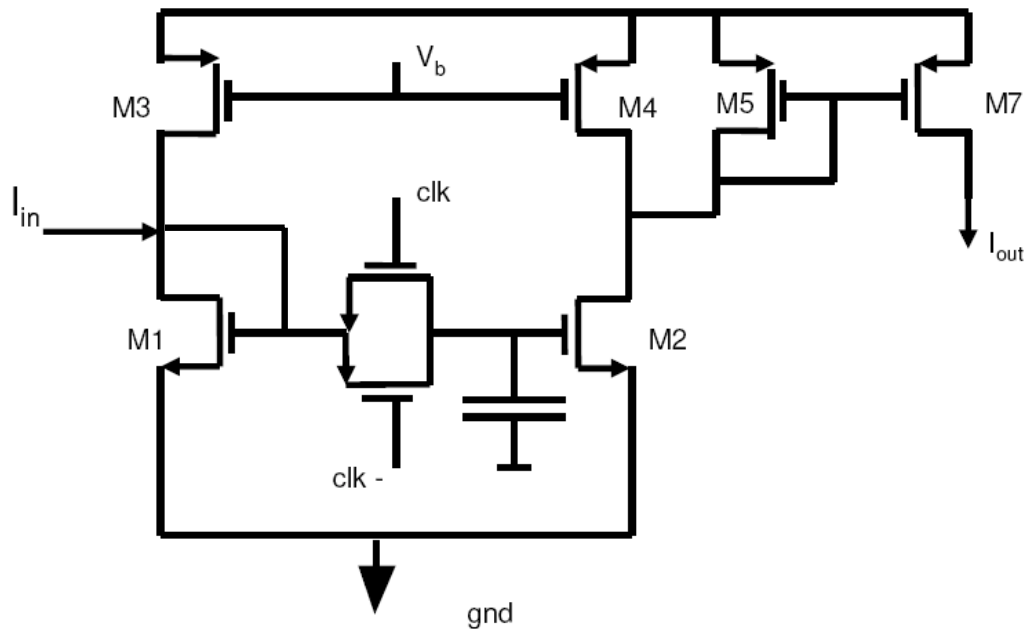

Figure 6.6 Basic current-mode sample and hold block (SI-block).

For this circuit, the sampling is accomplished by closing the CMOS switch thereby allowing Iout to track Iin. Then during the hold phase, switch is opened and Iout is held constant due to the charge trapped on the capacitance at gate of M2. Such a circuit's accuracy is primarily limited by matching of M1 and M2 and also the mismatch between threshold voltages (V_{th}) of the two devices due to their operation in subthreshold region. Hence, to achieve a reasonable level of accuracy, large slow devices were used for the current mirror [45].

The layout of the SI block was done so as to reduce as much mismatches as possible between the transistors M1 and M2. Hence, the common centroid methodology was used in the layout [11], so to evenly distribute the process variations.

6.1.3 Comparator

An appropriate current comparator can be implemented using the inverter cascade [19], Fig 6.7. Although a comparator of this type will display a poor PSSR when used as a voltage comparator, this problem is not significant when used as a current comparator. The first inverter in this circuit operates as an integrating current-to-voltage converter and hence effectively filters out the power supply noise. At the same time, the integrating nature of the comparator ensures that there is no inherent dc offset in the comparator. Consequently, the inverter cascade provides a simple, small and effective current-to-voltage converter/comparator.

The comparator is the main block which determines the speed of the overall design, as the clock should sample only after the first decision is made by the comparator.
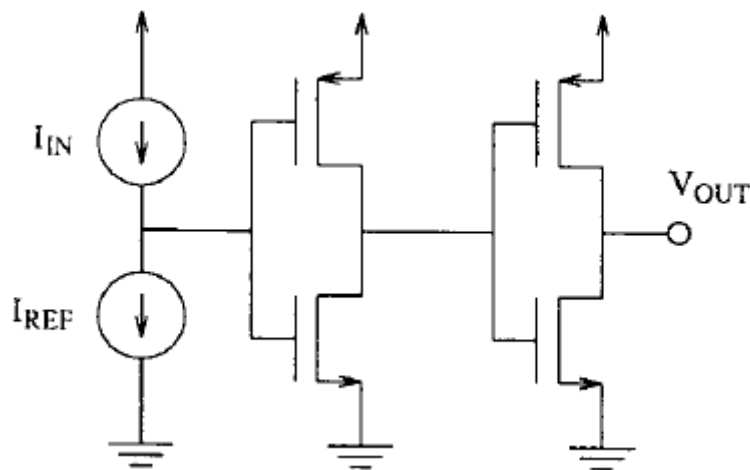
Figure 6.7 Current comparator. Two inverters cascaded in series [19].

6.1.4 Current Mirrors

Current Mirrors are the basic unit in both, the bit-cell and SI block, so they must display excellent current matching, for that, the device must display high output resistance and good device matching characteristics. The output impedance of the CMOS transistors is very high in subthreshold region due to very small value of current flowing through them. A slight mismatch in V_{th} (threshold voltage) can lead to large mismatch between the input and the output mirrored current. To improve the device matching, both

the channel length and channel width was selected to be significantly larger than the minimum feature size [45]. Fig 6.8 and Fig 6.9 shows the mirroring error due to process variations i.e. assuming the standard deviation of threshold voltage and mobility is about 0.5%, through the Monte Carlo simulation.
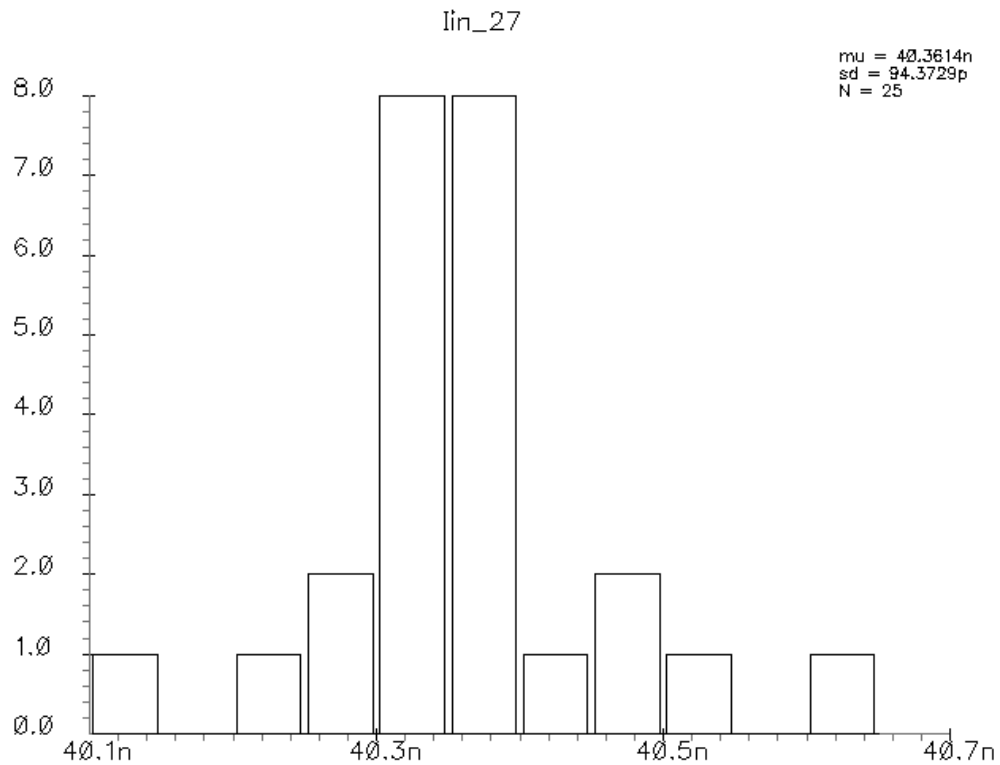
Figure 6.8 The Monte Carlo simulation result for input current of 40nA, assuming 0.5% standard deviation of threshold voltage and mobility.

Iout_27

mu = 40.956n
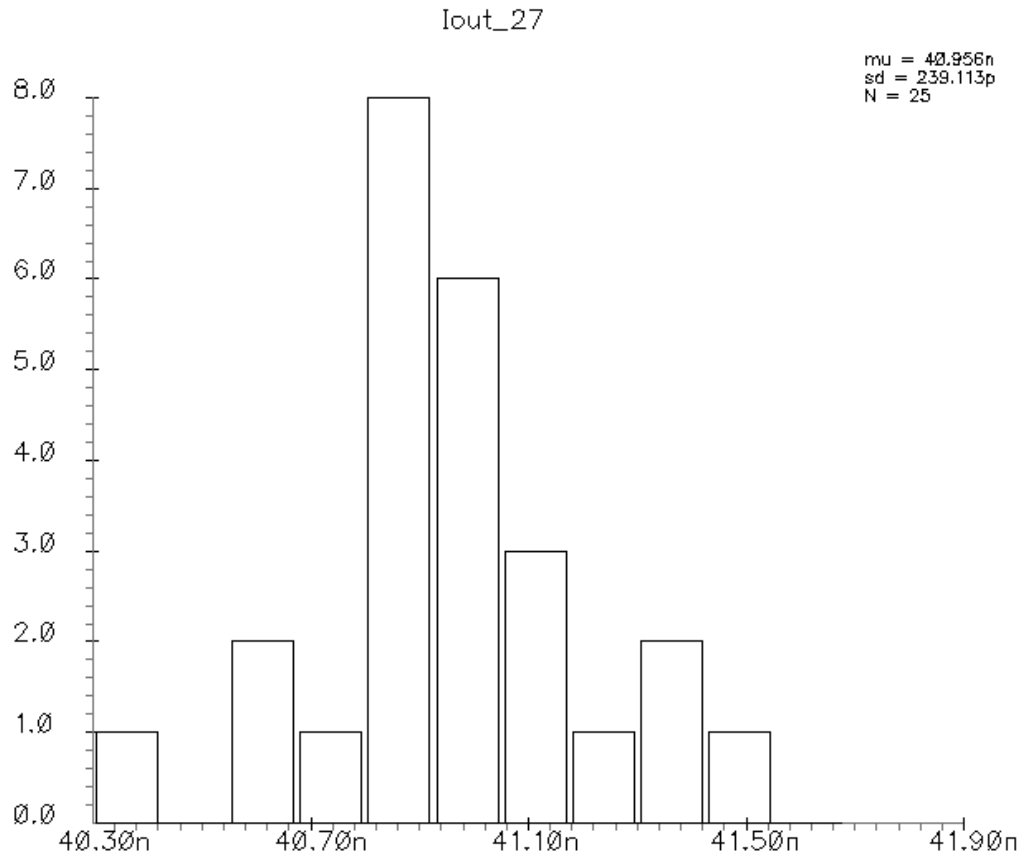sd = 239.113p
N = 25

Figure 6.9 The Monte Carlo simulation result for mirrored current corresponding to the above input current, assuming 0.5% standard deviation of threshold voltage and mobility.

Basically for a mean input current of 40.36nA the mirrored output current is 40.95nA, which shows the mirroring is quite accurate.

6.2 Layout

The layout of the ADC was done in TSMC SCN6M_DEEP CMOS 0.18μm technology, Fig 6.10. There were two types of power supplies, analog power supply for the blocks like bit-cell and SI block and digital supply for comparator and D-flip flops. The layout of each individual blocks were done so as to minimize the mismatches. Hence, the common centroid methodology was used in the layout [11], so to evenly distribute the process variations, wherever possible.
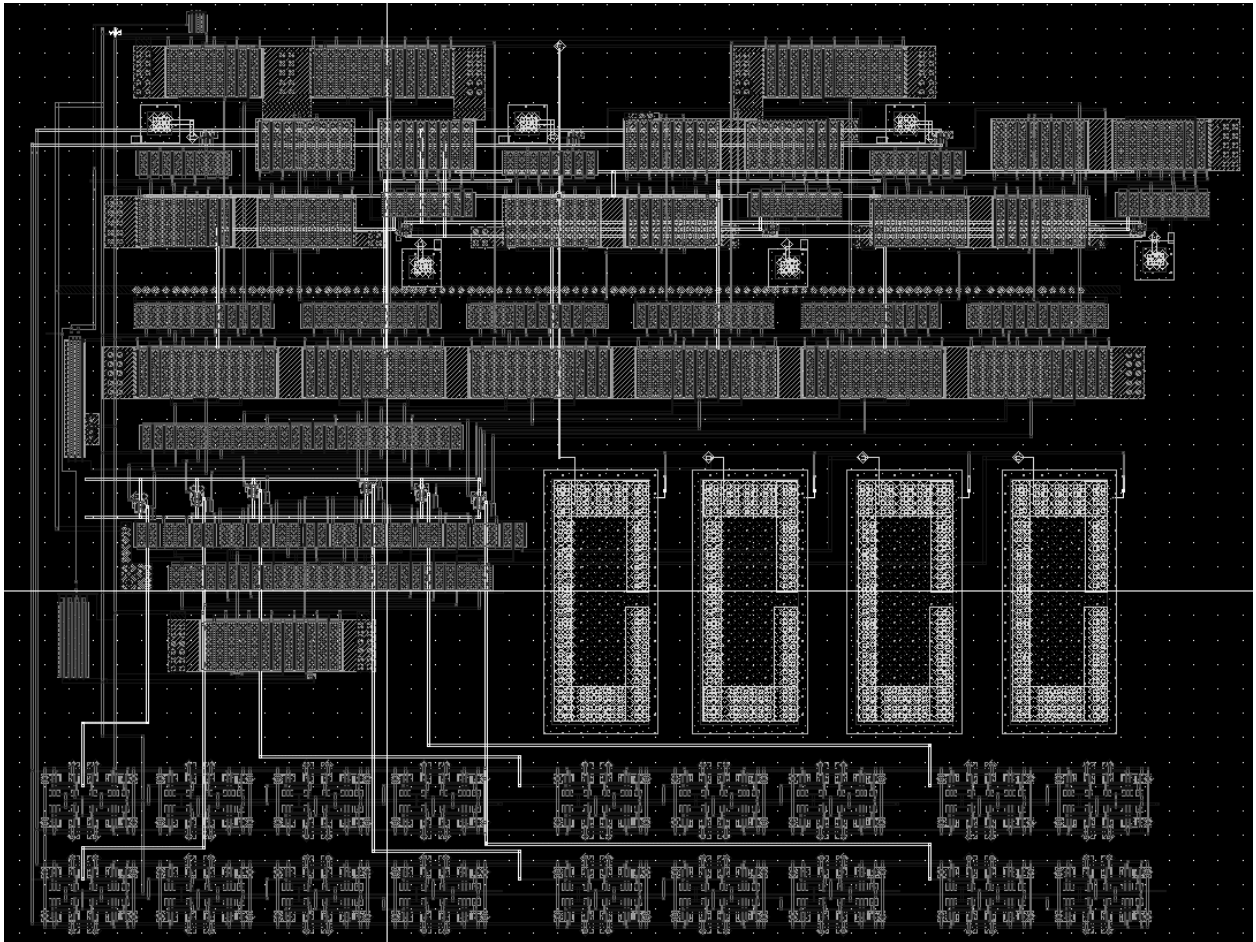
Figure 6.10 Layout of the ADC. The ADC was designed in TSMC SCN6M_DEEP CMOS 0.18μm technology.

The total area of the ADC was 0.046 mm^2 with aspect ratio of almost 1:1. Total of 6 metal layers were used during the layout so as to make the routing as compact as possible. Table 6.1 shows the average area of each individual block.

Table 6.1 Average area occupied by individual blocks.

Block Name	Area Occupied (μm^2)
1 Bit-Cell	3112
SI Block	1015
D-Flip Flop	352
Capacitor	3000

CHAPTER VII

SIMULATION RESULTS

Substantial testing of an ADC is required to determine the actual performance. One of the difficulties in testing comes from the fact that the ADC input is a continuous time, continuous amplitude signal, while the output of the ADC is a discrete time, quantized signal. The measurement setup must be able to produce accurate and precise input to the ADC while also storing the resulting digital output codes. Testing is further complicated by the fact that the input signal for the ADC must be many times more accurate than the ADC under test in order to obtain meaningful results. Since most modern signal sources are based on DACs, the signal source DAC must be linear to many more bits (typically 4 or more) of resolution than the ADC itself. Otherwise, it is not possible to capture the true ADC performance [5].

7.1 Differential and Integral Nonlinearity

There are many different metrics used to characterize ADC performance. Depending on the particular application, the ADC performance is often specified in different ways. The two most common ADC specifications for all applications are differential nonlinearity (DNL) error and integral nonlinearity (INL) error.

One very common and straightforward method used to determine the DNL and INL for an ADC is histogram testing. Histogram testing subjects the ADC to an input with a known time domain characteristic with some ideal output code histogram. Then the ADC is subjected to this input and the actual histogram of output codes is compared with the ideal output histogram to determine the error in the ADC. Assuming that the ADC transfer function is monotonic and does not contain "sparkle" codes (occasional grossly erroneous output codes) [5], the code histograms can be used to determine the DNL and

INL of the ADC. Since histograms do not contain any information about when the actual samples occurred, the histogram method can be misleading if the converter in fact does have a non-monotonic transfer function or exhibits "sparkle" codes. Noisy decision levels can also increase the amount of measurement error associated with using the histogram method to determine DNL and INL. Fortunately, many converter architectures are inherently monotonic and free from "sparkle" codes. If there is doubt, the ADC under test can be checked quickly for monotonicity and the amount of noise in the decision levels once. Assuming that the converter is found to be well behaved, histograms can then be used for determining the DNL and INL.

Fig 7.1 and Fig 7.2 shows the typical plots of differential non-linearity (DNL) and integral non-linearity (INL) error of the designed ADC. The simulation condition for Fig 7.1 and Fig 7.2 were a ramp input with a period of 4.88 ms, 130 KHz sampling rate and a 0.65 V supply voltage. Then the DNL and INL of the ADC were calculated using histogram testing.
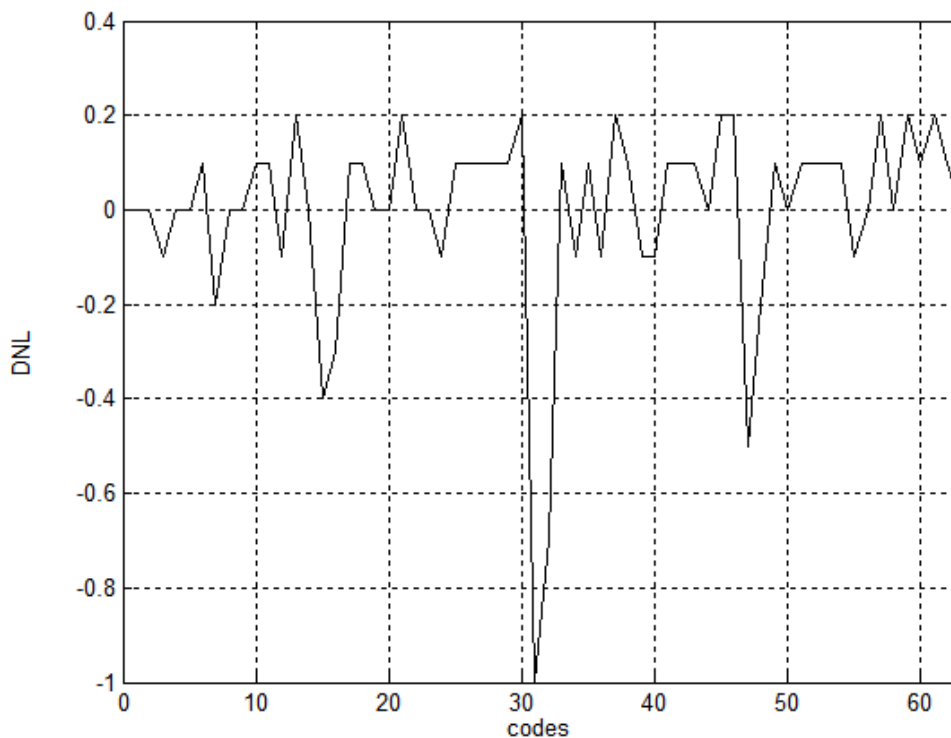

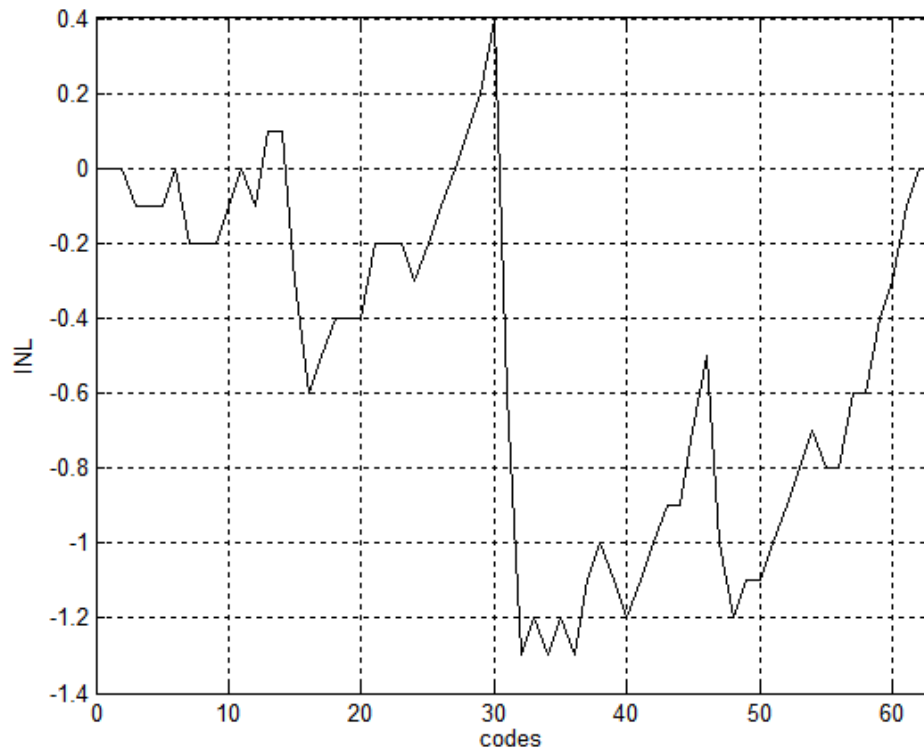**Figure 7.1** Differential non-linearity (DNL) simulated for the ADC.

Figure 7.2 Integral non-linearity (INL) measured for the ADC.

Note that the major errors in the DNL and INL occur at output codes corresponding to when all the comparator output need to have a transition, from 0 to 1 for MSB and from 1 to 0 for all the other bits. The major DNL occur at output code 32 (that code is missing) as the output takes transition from 011110 to 100000 directly. This is possibly due to mismatches in current mirroring. Though the mirroring error in single current mirror is small but the error accumulates when it propagates from the first block to the last block, resulting in error of more than 1 LSB.

7.2 Signal-to-Noise and Distortion Ratio

In many applications the dynamic performance of the ADC is the paramount. To test the dynamic performance, sinusoidal input signals are often used, which are quantized by the ADC and the digital signal codes are analyzed for frequency content

using a fast Fourier transform (FFT). Fig 7.3 shows an FFT for the 6-bit ADC sampling at 130 KHz and a full scale sinusoidal signal of 256 Hz.
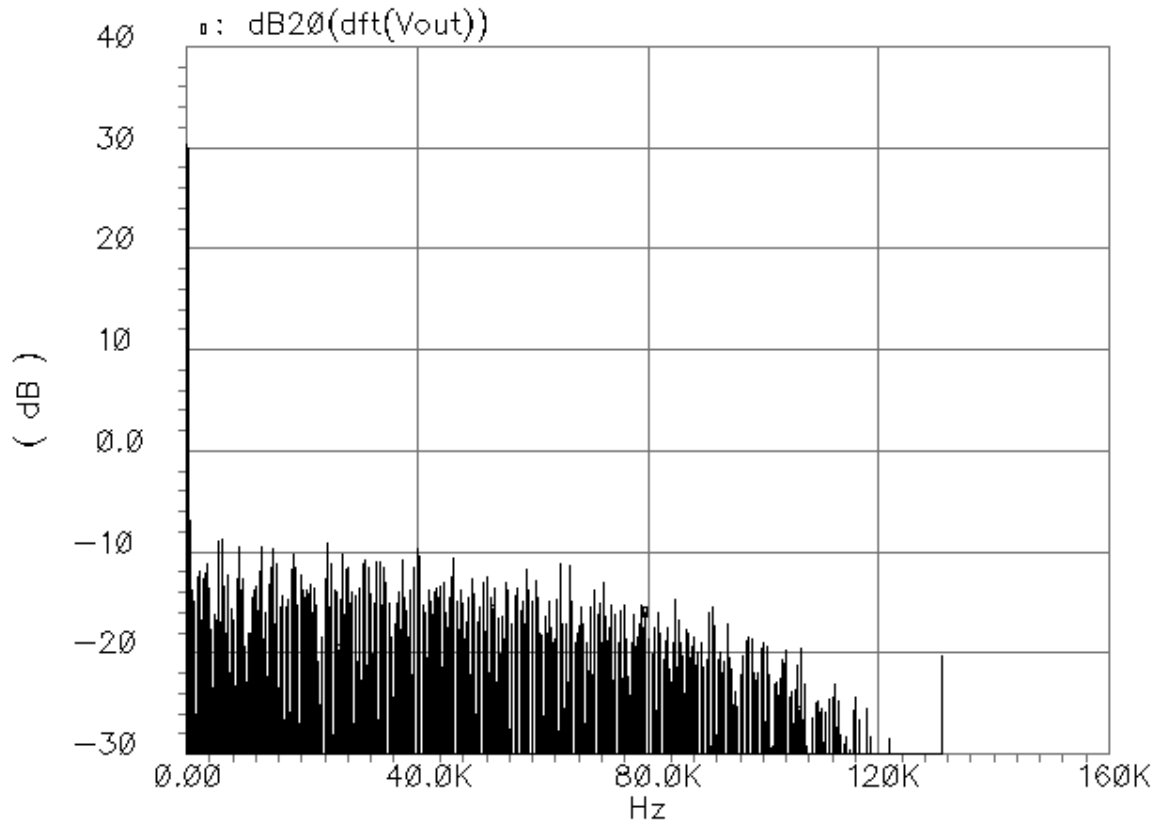

Figure 7.3 FFT plot for the 6-bit ADC with full scale sinusoidal input.

This frequency power spectrum can be used to determine the signal-to-noise and distortion ratio (SNDR), and the corresponding effective number of bits (ENOB). The ENOB is defined as

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

where SNDR is in dB.

Figure 7.4 Zoomed plot of the FFT plot shown in Fig 6.5. It shows that a relatively strong second and the third harmonics are present in the output, degrading the SNDR from the ideal, which would be 38 dB according to Equation (2.4).

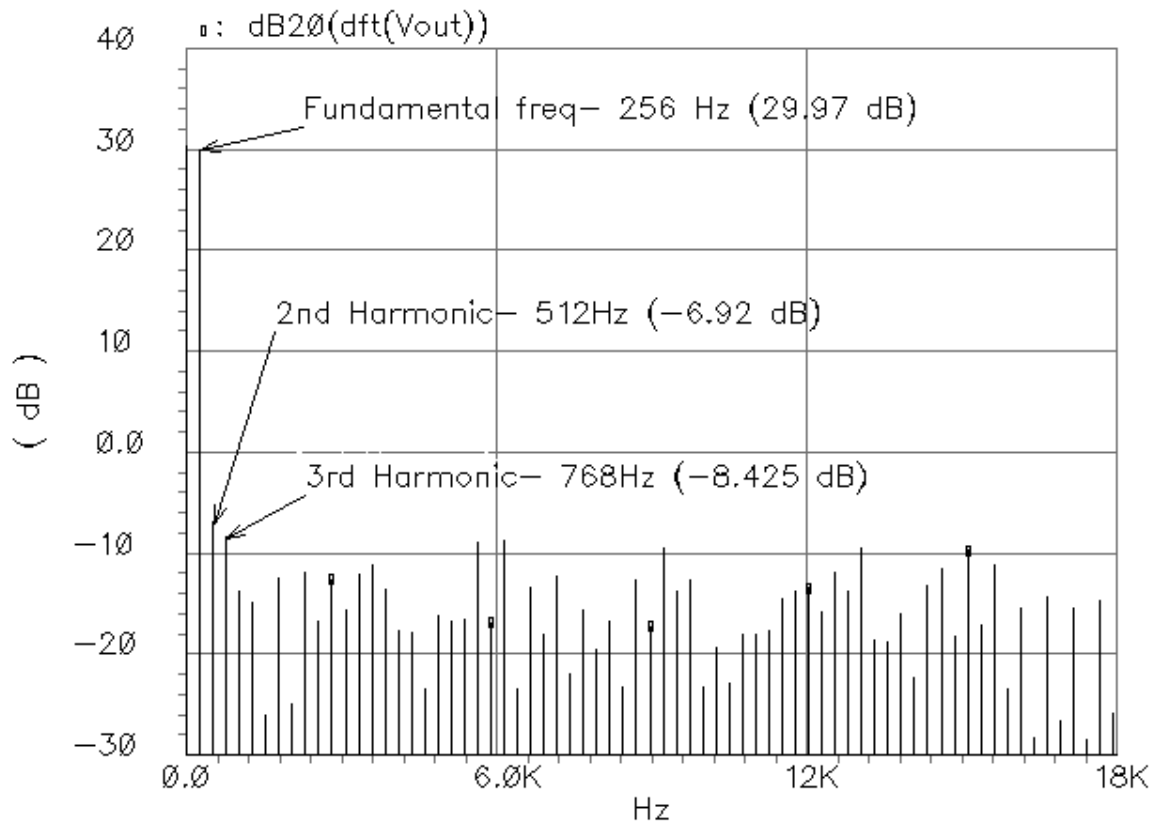Fig 7.4 shows the zoomed plot of the FFT plot shown in Fig 7.3. It shows that a relatively strong second and third harmonics are present in the output, degrading the SNDR from the ideal, which would be 38 dB according to the Equation (2.4). The SNDR was calculated to be 34.6 dB, giving ~5.5 ENOB.

7.3 Chip Photographs
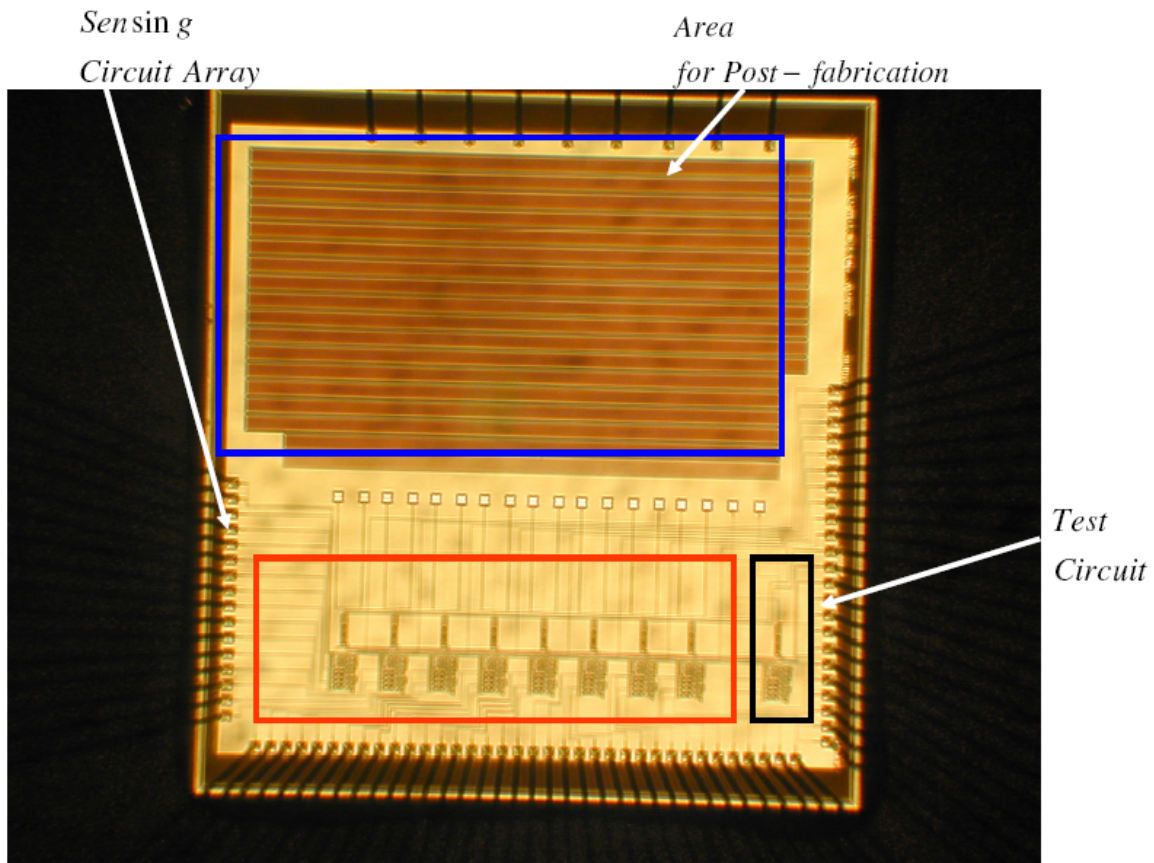
Figure 7.5 Nanowell sensor IC full micro photograph.

The whole top-view photo of the Nanowell sensor IC is shown in Fig. 7.5. The size of the chip is 4 mm by 4 mm and it was fabricated with TSMC 0.18um CMOS technology and packaged with PGA145M package. It has 8 channels which integrate one readout circuit and one low-power current-mode ADC converter. Also, for future testing, it also has one testing circuit. For the post-fabrication process which places a very tiny capacitor device on the wafer, a wide empty area is also fabricated. The capacitors are supposed to be placed on the area.
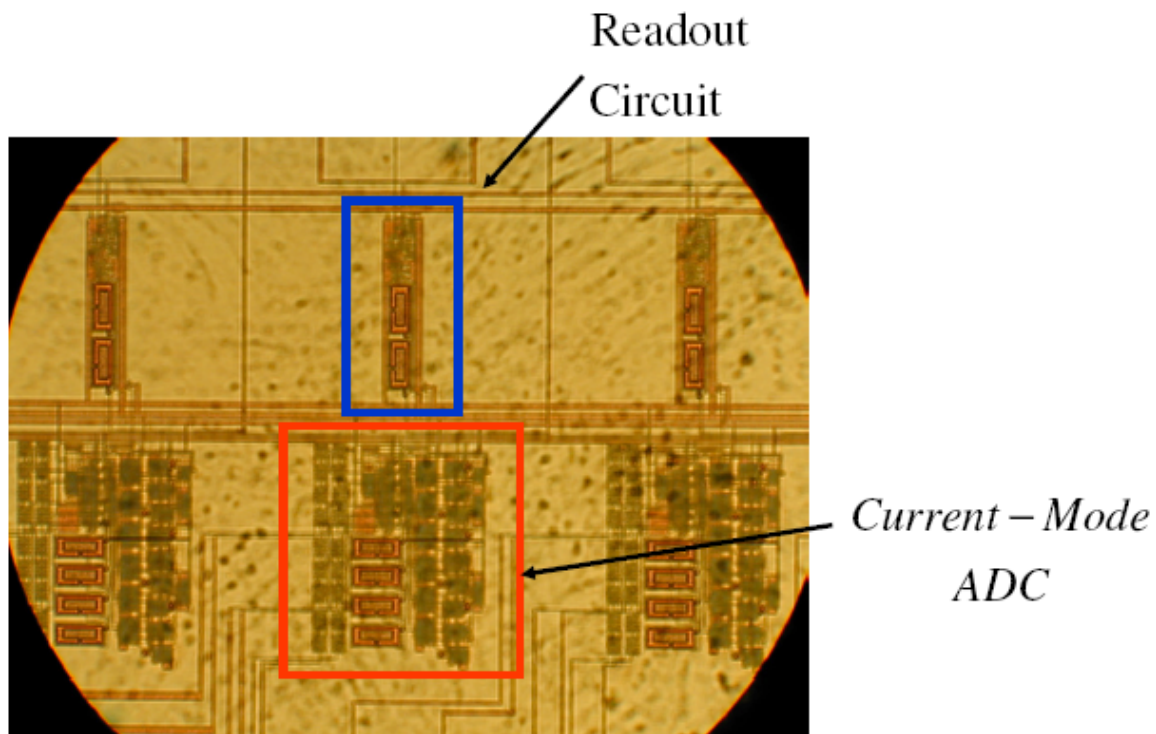
Figure 7.6 Zoomed photograph of one front-end channel.

Fig. 7.6 shows the zoomed photography of one front-end channel including one capacitance readout circuit and low-power current-mode ADC [18].

7.4 PCB Layout
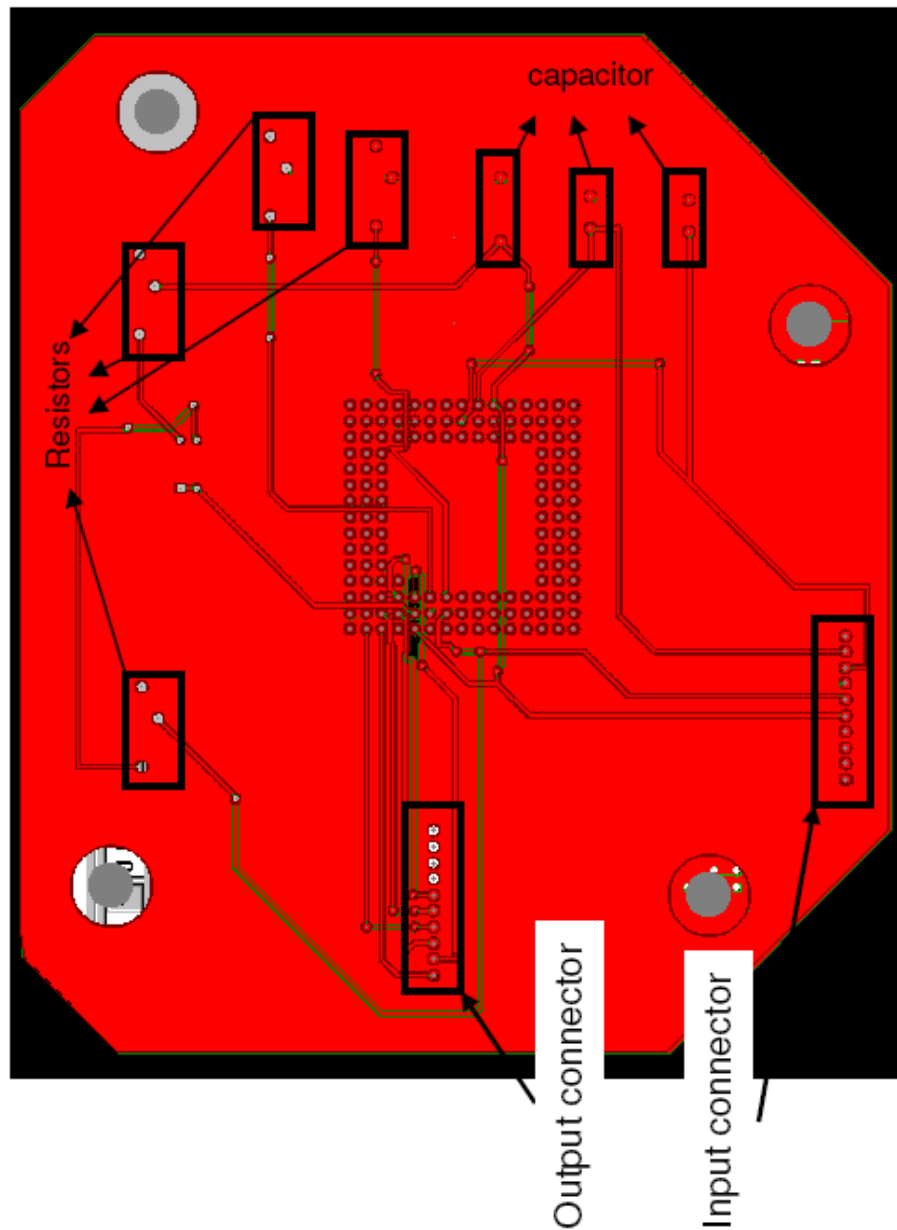
Figure 7.7 PCB layout for Nanowell sensor IC.

Fig 7.7 shows the PCB layout of the test board. It has one input connector for voltage supply and ground. It also has an output connector for the ADC outputs. Also there are several resistors to generate the proper input currents and capacitors for better power supply quality.

7.5 Testing

(1) Test set-up
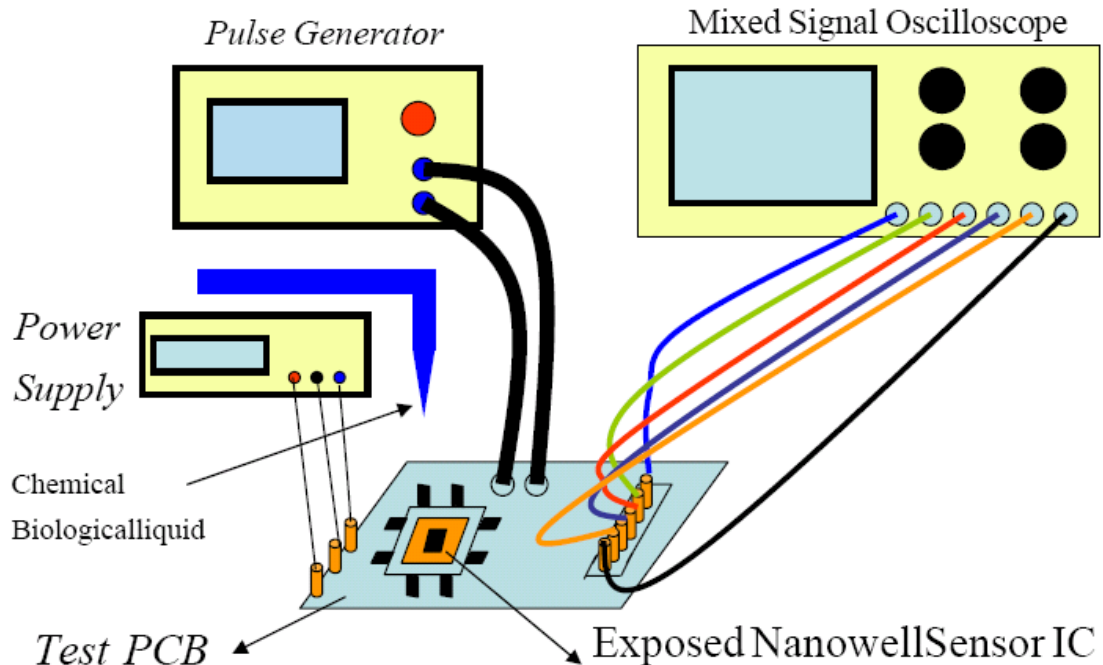
Figure 7.8 Nanowell sensor IC test set-ups.

Fig. 7.8 shows the whole test set-up for the Nanowell sensor IC. First of all, the PCB where the chip is placed is designed. Also, the mixed signal oscilloscope is connected to the output ports of the PCB. Moreover, to provide the clock to the control digital circuitry of the chip and the high frequency common mode signal to the readout circuitry, one function generator is connected. Of course, one power supply is used to provide VDD, VSS and GND power connection to the PCB. Finally, very precise liquid control equipment is required to drop a very small chemical or biological liquid on the exposed chip to change the dielectric constant of the tiny capacitors placed on the empty area of the chip.

(2) Test Result

The capacitor fabrication on the chip is delayed until now. Therefore, the actual testing will be the future work which will be done after the post-fabrication process is

successfully finished**.** Though we had provided test circuit to test the individual blocks, which was tested. Fig 7.9 shows actual test set-up for the testing of the chip. The input was current which was generated by a voltage difference across a resistor. The reference current was also generated using power supply and the resistor. The currents required were I_{ref} as 150nA, I_{bias} as 20nA and summation of these two, $I_{bias} + I_{ref}$ as 170nA. These currents were generated by a common reference voltage which was coming from the reference generator circuit from the front-end. The reference generator circuit required input current of the value of 150μA which was provided through a voltage difference across a resistor. The inverter chip was used to generate the inverted clock as both clock and inverted clock are required in the chip.
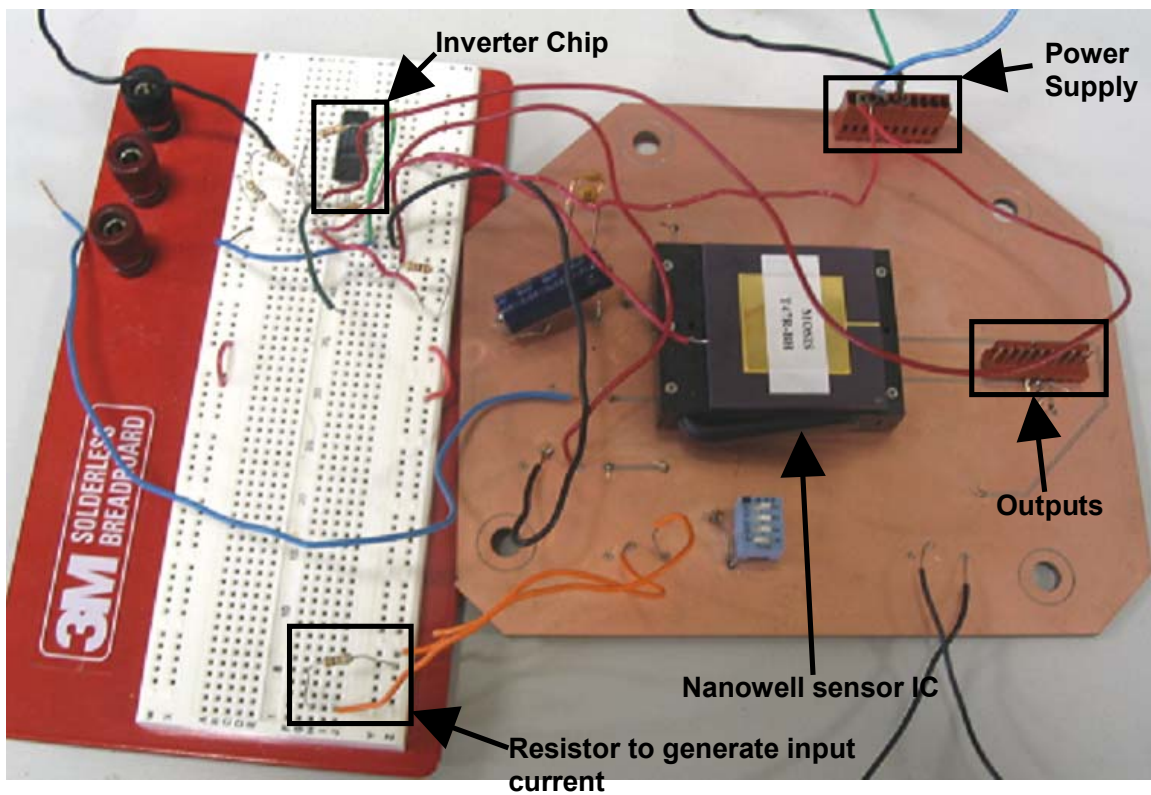
Figure 7.9 Actual test set-up.

During the testing, when a current between 0-150nA was given as the input no output was observed. After checking all the circuits major cause was found to be the reference circuit, as instead of the expected values of I_{bias} =20 nA, I_{ref} = 150nA and I_{ref} + I_{bias} =170nA, the outputs were find to be lot different and the major error was found in the 170nA current, which on doing Monte Carlo analysis only for process variations varied upto 800nA Fig 7.10, making the chip dead for current inputs upto 150nA.
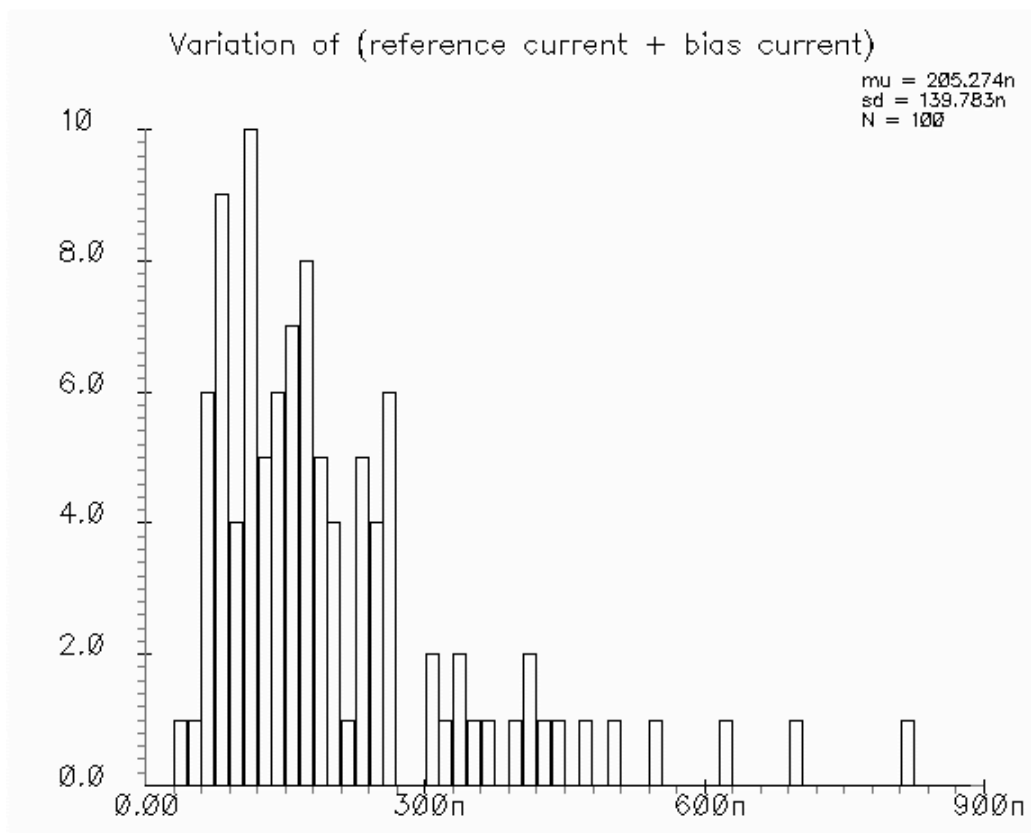
Figure 7.10 Monte Carlo analysis for the reference current + bias current generation.

Then input current was increased further and still no outputs were observed till the value reached upto 5µA. Thus, the chip was giving the digital outputs for the input currents larger than 5µA. This shows the current was going to much higher values as predicted in the simulations. This was probably due to other mismatches which causes the

variation in reference voltage and in turn in the currents generated. It was found out that reference circuit was nothing but just couple of current mirrors which were scaling down the input current of 150μA to 150nA and the reference voltage was generated by forcing that current through a diode connected transistor. So in turn, the mismatches in current mirror was causing an error in the output current and hence in reference voltage.

The best possible way to overcome the given error is to have these reference currents to be provided by outside, so we can have a proper control over their values.

CHAPTER VIII

SUMMARY

A 6-bit, 130 KS/s, 0.65 V ADC was discussed for sensor network application. It was argued that for such systems, where energy consumption is paramount and resolution and sampling rate are secondary, the current-mode algorithmic pipelined architecture is well suited.

The ADC performance is summarized in Table 8.1.

Table 8.1 Summary of ADC performance.

Technology	TSMC 0.18 μm
Voltage Supply	0.65 V
Reference Current	150 nA
Input signal	Current
Sampling Rate	130 KHz
ENOB	5.5 (256 Hz)
Power dissipation (0.65 V)	6 μW
Energy per sample (0.65 V)	8 pJ
Input Noise Current	$\sim 750 \ \dfrac{fA}{\sqrt{Hz}}$

8.1 Further Work

The ADC presented in this work performed well and achieved the required design goals. As with any design though, there are improvements that could be made. Two areas which are particularly interesting to pursue are achieving lower power consumption and increasing the resolution of the ADC.

The energy per sample of the current-mode algorithmic pipelined ADC is limited by the matching errors and the input noise as they directly affect the lowest value of

reference current that can be chosen. Hence, the power consumed can be reduced if we can achieve better current mirroring without increasing the supply voltage and scaling the reference current down.

Though the resolution of the ADC can be increased by simply increasing the number of bit-cells but that again is restricted by the mismatches as the error propagates from the first block to the last and keeps on accumulating. Therefore, the last block sees the accumulated error and which can cross over 1 LSB and giving missing codes in the ADC output. Thus, cascode current mirrors can be used to improve the accuracy, though that might cause the power consumption to increase.

8.2 Conclusion

A wireless sensor network is one of the greatest achievements in the history of wireless network architecture. All the sensor nodes are widely distributed in the network. Each node watches the local environment, locally collecting, processing and storing the data for sharing with other nodes via wireless link. The network extracts the meaningful information to the end user from the data collected from the participating nodes. The Nanowell sensor device [13] or the traditional Taguchi type sensor [47] might be the potential candidates of the novel sensor device used in the widely distributed sensor network. To implement the whole system which uses the Nanowell sensor device for chemical or biological material sensing, a low-power and small size capacitance value sensing readout circuit is required. Also, it has to be integrated together with the back-end low-power current-mode ADC on the same chip. The low-power current-mode ADC has been designed and fabricated with TSMC 0.18um CMOS technology. In the simulation result, the power consumption for 6-bit ADC was 6 μW, with a power supply of 0.65 V.

REFERENCES

[1] T.B. Cho and P.R. Gray,"A 10 b, 20 Msample/s, 35 mW Pipeline ADC," *IEEE J. Solid State Circuits*, vol. 30, no. 3, pp. 166-172, Mar. 1995.

[2] B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters," *IEEE J. Solid State Circuits*, vol. 23, no. 6, pp.1298-1308, Dec. 1988.

[3] H. Neuteboom, B.M.J. Kup, and M. Janssens, "A DSP-Based Hearing Instrument IC," *IEEE J. Solid State Circuits*, vol. 32, no. 11, pp. 1790-1806, Nov. 1997.

[4] R. Yeh and K.S.J. Pister, "Design of Low-Power Articulated Microrobots," in *Proc. Int. Conference on Robotics and Automation, Workshop on Mobile Micro-Robots*, San Francisco, CA, April 23-28, 2000, pp. 21-28.

[5] M. Mahoney, *DSP-Based Testing of Analog and Mixed-Signal Circuits*, IEEE Computer Society Press, Washington, DC, 1987.

[6] B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, Piscataway, NJ, 1995.

[7] P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed., John Wiley and Sons, Inc., New York, NY, 1993.

[8] A. Nemirovsky and A. Ron, "A Revised Model for Carrier Trapping-Detrapping 1/f Noise," *Solid-State Electronics*, vol. 41, no. 11, pp. 1811-1818, 1997.

[9] A. L. Garcia, *Probability and Random Processes for Electrical Engineering*, 2nd ed., Addison Wesley Publishing Company, Inc., Reading, MA, 1994.

[10] C.B. Wang, "A 20-bit 25-kHz Delta-Sigma A/D Converter Utilizing a Frequency-Shaped Chopper Stabilization Scheme," *IEEE J. Solid State Circuits*, vol. 36, no. 3, pp. 566-569, Mar. 2001.

[11] A. Hastings, *The Art of Analog Layout,* Prentice-Hall, Inc, Upper Saddle River, NJ, 2001.

[12] R.J. Van De Plassche, "Dynamic Element Matching for High-Accuracy Monolithic D/A Converters," *IEEE J. Solid State Circuits*, vol. SC-11, no. 6, pp. 795-800, Dec. 1976.

[13] S. Sonkusale, M.Cheng, L.Kish, A. Agarwal, Y.Kim, C. Liu and S. Seo, "A CMOS Sensor Array IC of Nanowell Devices for Molecular Sensing", *Third IEEE Conference on Sensors*, vol. 2, Oct. 24-27, Vienna 2004, pp. 963-966.

[14] S. Hashioka, "10 nm Size Fabrication of Semiconductor Substrate and Metal Thin Lines by Conventional Photolithography", *Intl. Micro.and Nano. Conf.*, Tokyo, Japan July, 2000, pp. 184-185.

[15] K. Schönhals and A. Schönhals, *Broadband Dielectric Spectroscopy*, Springer, Berlin, Germany, 2003.

[16] P.Q. Mantas, "Dielectric Response of Materials: Extension to the Debye Model", *J. the European Ceramic Society*, vol. 19, pp. 2079-2086, Oct. 1999.

[17] Y. Kim, A. Agarwal and S. Sonkusale, "Broadband Dielectric Spectroscopy CMOS Readout Circuit for Molecular Sensing,"*ISCAS 2005 Conference*, Kobe, Japan, 23-26 May, 2005, pp. 5906-5909.

[18] A. Agarwal, Y. Kim and S. Sonkusale, "Low-power Current-mode ADC for CMOS Sensor IC," *ISCAS 2005 Conference*, Kobe, Japan, 23-26 May, 2005, pp. 584-587.

[19] D.G Nairn and C.A.T Salama "Current-mode Algorithmic Analog-to-Digital Converters," *IEEE J. Solid State Circuits*, vol. 25, no. 4, pp. 997-1004, Aug. 1990.

[20] W.A. Serdijn; J. Mulder; D. Rocha and L.C.C. Marques, "Advances in Low-Voltage Ultra-Low-Power Analog Circuit Design"; *Int. Conference of Electronics, Circuits and Systems, ICECS*, vol. 3, 2-5 Sept. 2001, pp. 1533-1536.

[21] C.Y. Wu and Y.Y. Liow "New Current-Mode Wave-Pipelined Architectures for High-Speed Analog-to-Digital Converters," *Circuits and Systems*, IEEE, vol. 51, pp. 25 – 37, Jan. 2004.

[22] C. Toumazou, J.B. Hughes, and N.C. Battersby, Eds., *Switched Currents:An Analouge Technique for Digital Technology*. Peter Peregrinus, London, U.K., 1993.

[23] C. Toumazou, F.J. Lidegy, and D.G. Haigh, *Analouge IC Design: The Current-Mode Approach*. Peter Peregrinus, London, U.K., 1990.

[24] J.B. Hughes, N.C. Bird, and I.C. Macbeth, "Switched Currents-a New Technique for Analog Sample-Data Signal Processing," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 3,Portland, OR, 8-11 May 1989, pp. III1584–III1587.

[25] D.A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley and Sons, Inc, New York, NY, 1997.

[26] K. Poulton, R. Neff, A. Muto, W. Liu, A. Burstein, and M. Heshami, "A 4 GSample/s 8b ADC in 0.35μm CMOS," *IEEE Int. Solid-State Circuits Conference Dig. Tech. Papers*, San Francisco, CA, Feb. 3-7, 2002, pp. 166-167.

[27] J. Spalding and D. Dalton, "A 200 Msample/s 6b Flash ADC in 0.6μm CMOS,"*IEEE Int. Solid-State Circuits Conference Dig. Tech. Papers*, San Francisco, CA, Feb. 8-10, 1996, pp. 320-321.

[28] P. Vorenkamp and R. Roovers, "A 12-b, 60-MSample/s Cascaded Folding and Interpolating ADC," *IEEE J. Solid State Circuits*, vol. 32, no. 12, pp. 1876-1886, Dec. 1997.

[29] M.K. Mayes and S.W. Chin, "A Multistep A/D Converter Family with Efficient Architecture," *IEEE J. Solid State Circuits*, vol. 24, no. 6, pp. 1492- 1497, Dec. 1989.

[30] M.D. Scott; B.E. Boser and K.S.J. Pister, "An Ultra Low Energy ADC for Smart Dust," *IEEE J. Solid State Circuits*, vol. 38, no. 7, pp. 1123-1129, July 2003.

[31] J. Sauerbrey; D.S. Landsiedel and R. Thewes "A 0.5 V 1-uW Successive Approximation ADC" *IEEE J. Solid State Circuits*, vol. 38, no. 7, pp. 1261-1265, July 2003.

[32] J Nielsen and E .Bruun; "A Low-Power 10-bit Continuous-Time CMOS /spl Sigma//splDelta/A/Dconverter"; *Circuits and Systems, 2004*, vol. 1, pp. I - 417-20, 23-26 May 2004.

[33] M. Uster; T. Loeliger; "Integrating ADC Using a Single Transistor as Integrator and Amplifier for Very Low (1 fA minimum) Input Currents" *Advanced A/D and D/A Conversion Techniques and their Applications*, pp. 86 - 89, 27-28 July 1999.

[34] G. Bonfini and A.S. Brogna; "An Ultra Low-Power Switched Opamp-based 10-B Integrated ADC for Implantable Biomedical Applications" *ISCAS IEEE*, vol. 51, no. 1, pp. 174 - 177, Jan. 2004.

[35] R. Reutemann, P. Balmelli, and Q. Huang, "A 33mW 14b 2.5MSample/s $\Delta\Sigma$ A/D Converter in 0.25µm Digital CMOS.", *IEEE Int. Solid-State Circuits Conference Dig. Tech. Papers*, San Francisco, CA, Feb. 3-7, 2002, pp. 316-317.

[36] A.M. Mallinson and P. Spitalny, "A 17b Algorithmic ADC," *IEEE Int. Solid-State Circuits Conference Dig. Tech. Papers*, San Francisco, CA, Feb. 19-21, 1992, pp. 40-41.

[37] C. C. Chen and C. Y. Wu; "Design Techniques for 1.5-V Low-Power CMOS Current-Mode Cyclic Analog-to-Digital Converters," *Circuits and Systems II, IEEE*, vol. 45, pp. 28 – 40, Jan. 1998.

[38] A. Guzinski, M. Bialko, and J. C. Matheau, "Bodydriven Differential Amplifier for Application in Continuous Time Active-C Filter," in *Proc. European Conf. Circuit Theory and Design (ECCTD '87)*, Paris 1987, pp. 315-320.

[39] E. S¨ackinger and W. Guggenbuhl, "An Analog Trimming Circuit Based on a Floating-Gate Device," *IEEE J. Solid State Circuits*, vol. 23, no. 6, pp. 1437–1440, Dec. 1988.

[40] K. Roy; S. Mukhopadhyay, H.M. Meimand; "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits", *Proceedings of the IEEE,* vol. 91, no. 2, pp. 305 – 327, Feb. 2003.

[41] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge Univ. Press, New York, 1998.

[42] Y.P Tsividis and Ken Suyama, "MOSFET Modeling for Analog Circuit CAD: Problems and Prospects", *IEEE, J. Solid State Circuits*, vol 29, no. 3, pp. 210-216, March 1994.

[43] Y. Nemirovsky; I. Brouk and C.G Jakobson, "1/f Noise in CMOS Transistors for Analog Applications", *Electron Devices, IEEE Transactions* vol. 48, no. 5, pp. 921 – 927, May 2001.

[44] R. Rao; A. Srivastava; D. Blaauw and D. Sylvester; "Statistical Analysis of Subthreshold Leakage Current for VLSI Circuits" *VLSI Systems, IEEE Transactions* on vol. 12, no. 2, pp.131 - 139, Feb. 2004.

[45] J.-B. Shyu; G.C. Temes and F. Krummenacher, "Random Error Effects in Matched MOS Capacitors and Current Sources," *IEEE J. Solid State Circuits*, no 6, pp: 948 – 956, Dec 1984.

[46] D.G. Nairn, "Amplifiers for High-Speed Current-Mode Sample-and-Hold Circuits," *Proceedings ISCAS '92*, vol. 4 pp: 2045 - 2048, 3-6 May 1992.

[47] N. Taguchi, Japan Patent, 45 38,200; U.S. Patent 3,695,848 (1972)

VITA

Name: Anuj Agarwal

Address: Department of Electrical Engineering, Texas A&M University,
                   College Station, TX 77843-3128

Email Address: write2anuj@hotmail.com

Education: B.Tech, Electrical Engineering, Indian Institute of Technology,
                   Kanpur, India, 2003.