DESIGN OF HIGH PERFORMANCE FREQUENCY SYNTHESIZERS IN COMMUNICATION SYSTEMS

A Dissertation

by

SUNG TAE MOON

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2005

Major Subject: Electrical Engineering

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Approved as to style and content by:

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ABSTRACT

Design of High Performance Frequency Synthesizers
in Communication Systems. (May 2005)
Sung Tae Moon, B.S., Seoul National University
Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

Frequency synthesizer is a key building block of fully-integrated wireless communication systems. Design of a frequency synthesizer requires the understanding of not only the circuit-level but also of the transceiver system-level considerations. This dissertation presents a full cycle of the synthesizer design procedure starting from the interpretation of standards to the testing and measurement results.

A new methodology of interpreting communication standards into low level circuit specifications is developed to clarify how the requirements are calculated. A detailed procedure to determine important design variables is presented incorporating the fundamental theory and non-ideal effects such as phase noise and reference spurs. The design procedure can be easily adopted for different applications.

A BiCMOS frequency synthesizer compliant for both wireless local area network (WLAN) 802.11a and 802.11b standards is presented as a design example. The two standards are carefully studied according to the proposed standard interpretation method. In order to satisfy stringent requirements due to the multi-standard architecture, an improved adaptive dual-loop phase-locked loop (PLL) architecture is proposed. The proposed improvements include a new loop filter topology with an active capacitance multiplier and a tunable dead zone circuit. These improvements are crucial for monolithic integration of the synthesizer with no off-chip components.

The proposed architecture extends the operation limit of conventional integer-

N type synthesizers by providing better reference spur rejection and settling time performance while making it more suitable for monolithic integration. It opens a new possibility of using an integer-N architecture for various other communication standards, while maintaining the benefit of the integer-N architecture; an optimal performance in area and power consumption.

To my beloved wife Sung Hwa and son Hahnseok

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CHAPTER I

INTRODUCTION

A. Background and Motivation

Wireless communication gained popularity as the electronics industry introduces accessible consumer products leading the emerging market. Recent advance of personal electronic devices demands a high performance network connectivity between the devices to provide users maximum efficiency and convenience. Wireless local area network (WLAN) is one of the most popular among many short-distance communication standards such as Bluetooth and HiperLAN. WLAN has become the preferred choice over other standards due to its transparency to users accustomed to well established wired local area network (LAN).

Two major limitations of WLAN systems have been low data rate and high cost. The former is being overcome by allocating new frequency bands for WLAN service. Among these are the industrial-scientific-medical (ISM) band at 2.4 GHz and the unlicensed national information infrastructure (U-NII) band at 5 GHz. New standards have been developed with still others under development to take advantage of these frequency bands.

To be cost effective, a practical implementation of WLAN emerged as the 802.11b supplement, specifying the physical layer extension in the 2.4-GHz band. However, a 11 Mbit/sec throughput turns out to be not enough as the usage model shifted from text-based content to multimedia content. 802.11a extends the capability of WLAN by moving the physical layer extension into 5-GHz band. With wider bandwidth available, a 802.11a transceiver can reach a throughput of 54 Mbit/sec.

The journal model is *IEEE Transactions on Automatic Control*.

The most effective way to save production cost and to minimize form factor has been a monolithic implementation of entire RF transceiver on a single chip. Even though 802.11b and 802.11a both provide same services to user, due to the popularity of 802.11b equipment, most of the new products have to support both standards at the same time. The cost of supporting both standards, however, is a major concern. Therefore, a multi-standard transceiver is essential to keep the size and cost at a minimum, while maximizing the amount of shared building blocks in both operating modes.

The increasing demand for high-performance WLAN system is the motivation for studying here the design of fully integrated receiver for multi-standard 2.4 GHz and 5 GHz. In this dissertation we focus only on the frequency synthesizer and describe how new architectures and circuit topologies enable us to reduce the cost and power consumption while achieving high performance and high integration.

B. Organization

The main objective of this dissertation is to study the design procedure of high performance frequency synthesizers for multiple wireless communication standards. To prove the effectiveness of the procedure we demonstrate in the context of a multi-standard WLAN 802.11a and 802.11b receiver. The design procedure developed in this study applies to various wireless communication standards and is not limited to WLAN application.

The following chapter introduces three short-range wireless communication standards and discuss how the information in the given standard document can be translated into more specific circuit level requirements. In this chapter we cover Bluetooth, WLAN 802.11a and WLAN 802.11b standards.

Chapter III deals with phase-locked loop (PLL) based frequency synthesizers, which are an essential part of any modern wireless system. In this chapter we specifically examine system level PLL design strategies. The trade-off effect of loop bandwidth and phase margin on loop settling time, stability, spur levels, and output phase noise are studied and design recommendations are developed. We show a very simple and effective design procedure for WLAN 802.11b synthesizer as an example. We also present a brief review of recent advances on frequency synthesizer design.

Chapter IV focus on high frequency and low noise voltage controlled oscillator (VCO) design techniques. In this chapter we review existing low phase noise VCO design procedures and present recent development on low noise techniques.

In chapter V we put the theoretical developments of the previous chapters into practice and present the implementation of a fully integrated BiCMOS frequency synthesizer for multi-standard WLAN 802.11a and 802.11b at 5 GHz/2.4 GHz. The experimental results show a superior spur rejection performance while meeting all specifications of both target standards. Finally chapter VI concludes with a summary and a list of suggestions for future work.

CHAPTER II

INTERPRETING STANDARDS INTO SPECIFICATIONS

A. Introduction

Wireless communication – as the counterpart of *wired* communication such as telephone and local area network (LAN) – found a revived popularity after introduction of cellular phone and other personal electronic devices such as personal digital assistant (PDA), portable personal computer (PC) and MP3 player. It is highly desirable for those mobile devices to have a wireless connectivity to other similar devices or broader network, namely the internet. There is a variety of communication standards to meet different requirements and accommodate usage models. The circuit design must be as flexible and agile as possible to keep up with rapid advances. Therefore, it is imperative to develop a systematic procedure to translate the requirements of a standard into lower level circuit specifications. These relations are generally intuitively clear to most circuit designers but when it reaches to the point when accurately establishing the detailed numerical specs, such as settling time and phase noise, confusion and indetermination rule as appropriate literature is lacking or hard to find.

Fig. 1 shows relationships between standards and circuit specifications, concerning the design of frequency synthesizer. Usually a multitude of information from standard documents have influences on the calculation of each specification. Then the determined specifications affect more than one building blocks and even the architecture of the synthesizer itself. Among the building blocks, the loop filter need the most information from the specifications. This is because the loop filter is the only building block that has enough flexibility and open variables to balance the trade-off of the conflicting requirements. Other building blocks such as VCO and

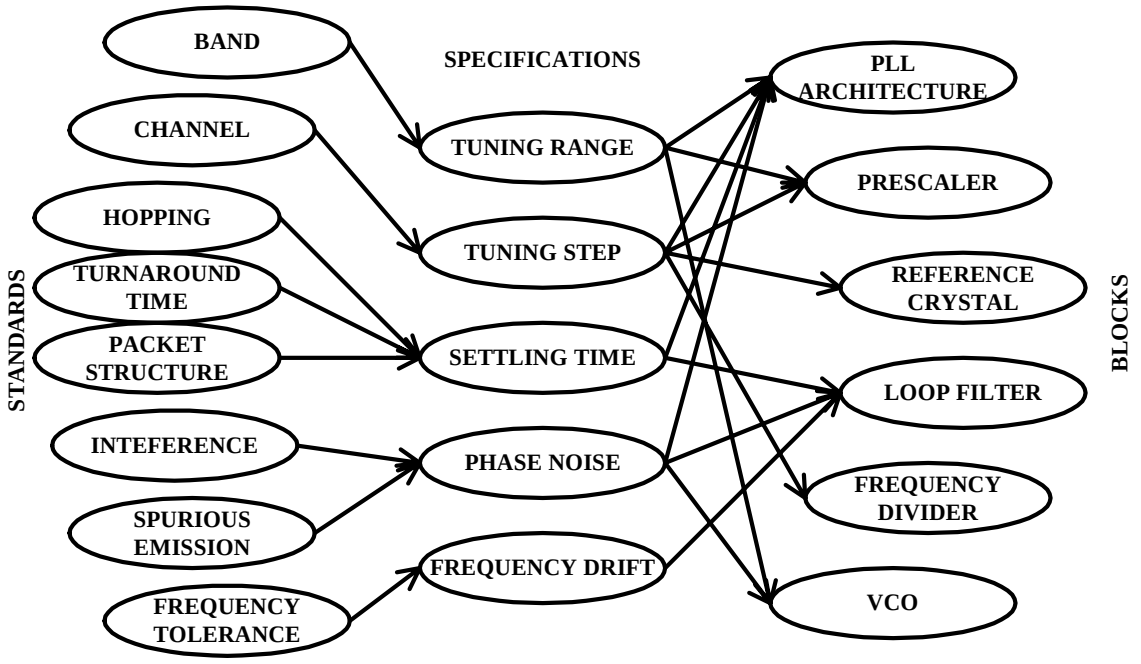


Fig. 1. From standards to specifications

prescaler have also critical effect on the performance. However, there are limitations how far the performance of those building blocks can be improved within the boundary of the given process technology without being excessively expensive in terms of power dissipation and chip area. Once the performance of the other building blocks is determined, the loop filter can compensate for their shortcomings.

The detailed specifications for the transistor-level design of frequency synthesizers are not readily available from the standard, but are embedded within the description of the requirements for the communication system. Also, particular characteristics of the system design set constrains in the specifications of the frequency synthesizer. For example, even though the RF frequencies are set for a given standard, the selection of a given intermediate frequency (IF) determines the required output frequency range of the synthesizer. Table I is used to illustrate the information in some standard documents, that is relevant to frequency synthesizer design. Full details of several

Table I. Short range wireless communications standards

	Bluetooth	802.11a	802.11b	802.11g
Bit rate	1 Mbps	54 Mbps	11 Mbps	54 Mbps
Sensitivity	-70 dBm	-82 dBm	-76 dBm	-76 dBm
Frame Error Rate	10^{-3} (BER)	10^{-5}	8×10^{-2}	8×10^{-2}
Band (MHz)	2400–2479	5180–5805	2412–2472	2412–2472
Channel Spacing	1 MHz	20 MHz	5 MHz	20 MHz
Accuracy	±75 kHz	±20 ppm	±25 ppm	±25 ppm
Settling	< 259 μs	224 μs	224 μs	224 μs
Interference	+40 dB at 3 MHz	+32 dB at 40 MHz	+35 dB at 25 MHz	+35 dB at 25 MHz

wireless communication standards can be found in [1–4].

B. Frequency Band and Tuning Range

Every communication standard utilizes a specific frequency band in the spectrum of electro-magnetic waves according to the usage models, and the regulations of the governing body. For instance, the 2.4 GHz ISM band is most popular for short range communication standards such as Bluetooth and Wireless LAN, because the usage of the ISM band is free and the frequency is high enough to limit the reach of the transmitted signal.

The architecture of the entire receiver in which the synthesizer is being part has significant effect on the tuning range specification. What is given in the standard documents is the center frequency of each channels that the standard specifies for a multiple access purpose. In order to down-convert the signal of a given channel to an IF, the carrier signal from the synthesizer should be IF away from the center

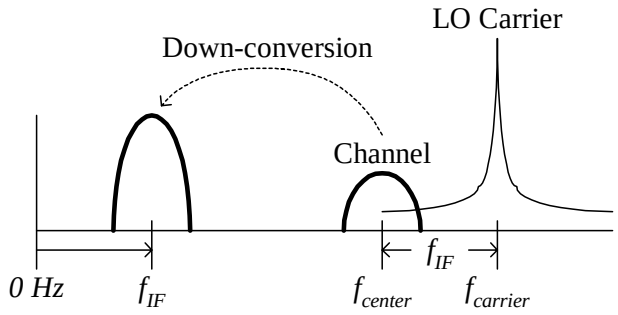


Fig. 2. Channel center frequency and carrier frequency

frequency. Fig. 2 shows the relationship between the channel center frequency and the carrier frequency. The carrier frequency can be either higher or lower than the channel center frequency depending on the architecture of image rejection mechanisms employed by the receiver system. In the case of a direct-conversion receiver, where the IF is zero, the carrier frequencies and the channel center frequencies are identical.

In PLL based frequency synthesizers, the tuning range of the VCO determines the limits on the overall system tuning range. The tuning range of the VCO should be much larger than the frequency band of interest since it has large range of uncertainty due to process variations and modelling uncertainties. A 20% deviation in either inductance or capacitance in a LC oscillator result in more then 10% error in the output frequency.

More rigorous analysis of the effect of process variations on the tuning range is as follows. Fig. 3 depicts the situation where the tuning range of a VCO is affected by process variations. While the standard document specifies the tuning range of the synthesizer from f_{spec_low} to f_{spec_high}, a real implementation of the VCO has tuning range target from f_{target_low} to f_{target_high}. In order to compensate the effect of process variations, the tuning range of the real implementation should be larger than the specification given by the standard. Now we quantify exactly how much overhead is required. Assuming the carrier frequency is tuned by a LC-tank resonator,

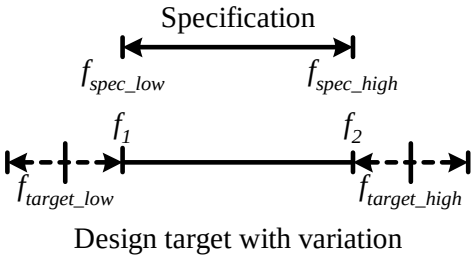


Fig. 3. Determining tuning range specification under process variations

$$f_{target\_low} = \frac{1}{2\pi\sqrt{LC_{max}}} \tag{2.1}$$

$$f_{target\_high} = \frac{1}{2\pi\sqrt{LC_{min}}} \tag{2.2}$$

where C_{max} and C_{min} are the capacitance limits of the varactor to be designed. The passive circuit elements L and C can vary due to the process variations. The range of the variation is defined as,

$$\alpha L < L < \beta L \tag{2.3}$$

$$\gamma C < C < \delta C \tag{2.4}$$

α, β, γ, and δ are the ratios of the variation where $0 < \alpha, \gamma < 1$ and $\beta, \delta > 1$. As shown in the lower portion of Fig. 3, the variation of the circuit elements may shift the low frequency boundary from f_{target_low} to f_1, and the high frequency boundary from f_{target_high} to f_2. These new boundaries can be expressed as,

$$f_1 = \frac{1}{2\pi\sqrt{\alpha L\gamma C_{max}}} \tag{2.5}$$

$$f_2 = \frac{1}{2\pi\sqrt{\beta L\delta C_{min}}} \tag{2.6}$$

From (2.1) and (2.2),

$$f_1 = \frac{f_{target\_low}}{\sqrt{\alpha\gamma}} \tag{2.7}$$

$$f_2 = \frac{f_{target\_high}}{\sqrt{\beta\delta}} \tag{2.8}$$

The new boundaries, f_1 and f_2 must cover the required tuning range from f_{spec_low} to f_{spec_high}.

$$f_{spec\_low} > f_1 \tag{2.9}$$

$$f_{spec\_high} < f_2 \tag{2.10}$$

Combined with (2.7) and (2.8), the new requirements are,

$$f_{target\_low} < \sqrt{\alpha\gamma} f_{spec\_low} \tag{2.11}$$

$$f_{target\_high} > \sqrt{\beta\delta} f_{spec\_high} \tag{2.12}$$

The new requirements may seem to have just small differences, but in reality they have significant effect on the tuning range specifications. We can verify this in the following example. For Bluetooth receiver, the synthesizer is required to provide carrier frequencies from 2.4 GHz to 2.48 GHz. If we assume ±10% variation for both inductor and capacitor, the ratios of variation are $\alpha = \gamma = 0.9$, and $\beta = \delta = 1.1$. From (2.11) and (2.12),

$$f_{target\_low} < 0.9 f_{spec\_low} = 2.16 \text{ GHz} \tag{2.13}$$

$$f_{target\_high} > 1.1 f_{spec\_high} = 2.728 \text{ GHz} \tag{2.14}$$

The new requirements state that the tuning range is increased from 80 MHz to 568 MHz, which is 7-times wider than the previous requirement. In terms of percentage value, the tuning range is increased from 3.28% to 23%. Other examples including WLAN 802.11a and 802.11b standards with 10% and 20% process variations are summarized in Table II. All the examples show drastic increase in tuning range requirements even with a relaxed process variation assumption of 10%. This

Table II. Tuning range requirements under process variations (unit:MHz)

	Standard	10% variation	20% variation
Bluetooth	2400–2480 (Δ80)	2160–2728 (Δ568)	1920–2976 (Δ1056)
802.11a	5180–5805 (Δ625)	4662–6386 (Δ1724)	4144–6966 (Δ2822)
802.11b	2412–2472 (Δ60)	2170–2720 (Δ550)	1929–2967 (Δ1038)

is generally true in the cases of narrow-band communication standards with high frequency carriers in GHz range.

Due to the extremely stringent requirement, it is normally not practical to design a VCO covering the tuning range extended by process variations. A popular solution to this is to implement an off-line discrete tuning capability using capacitor banks. Digital input bits are selected before the operation of the receiver compensating for the effect of process variations by trimming the varactor. Each chip from a single wafer may require different tuning input bits since process variation highly depend on the location of the chip on the wafer. Some well-controlled analog CMOS/BiCMOS process technologies have better than 10% process variations for special inductors and capacitors, limiting the expansion of tuning range due to uncertainty.

C. Channel Agility and Settling Time

Whenever the transmission or reception channel switches in a communication system, the transceiver must change its local oscillator frequency to synchronize with the received/transmitted signal. Since most frequency synthesizers utilize a feedback

mechanism to control the accuracy of the output frequency, and minimize the difference between the output and the target frequency, the switching of the output frequency cannot be instantaneous. The output frequency approximately follows the step response of a second order system for very small phase errors. This condition holds only when the frequency step is much smaller than the center frequency, as in narrow-band systems. For large frequency steps in wide-band systems, the response will slow down due to very non-linear behavior associated with large phase errors.

Frequency hopping, turnaround time and packet structure determines how fast the loop has to settle below certain limit. For instance in the Bluetooth standard, the frequency synthesizer settling time is not clearly defined, but it can be calculated from the relationship between the time slot length and the packet length. Detailed information about packet structure can be found on Section 4.6 of the Bluetooth standard document [4]. Fig. 4 summarizes all the different types of packet structure and their timing specifications.

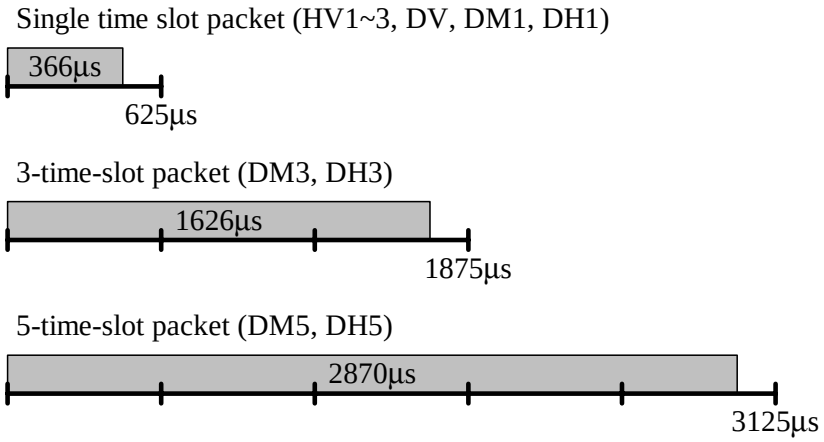


Fig. 4. Bluetooth packet length

Since the Bluetooth standard uses frequency hopping at 1600 hops per second, the transceiver is only allowed to transmit within a time slot of $T_{slot} = 625$ μs. The length of a standard single packet to be transmitted in a time slot is 366 bit

Table III. Settling time requirements

	Downtime (T_{down})	75% of T_{down}	50% of T_{down}
Bluetooth	229 μs	171 μs	114 μs
802.11a	224 μs	168 μs	112 μs
802.11b	224 μs	168 μs	112 μs

long, corresponding to $T_{pkt} = 366$ μs. In addition, Section 9.1 Master/Slave Timing Synchronization from [4] specifies an uncertainty window of $\pm 10\mu$s due to the timing mismatch between the transmitting device and the receiving device. This subtracts $T_{uncertainty} = 20\mu$s from the downtime. Thus the downtime between two consecutive time slots is,

$$T_{down} = T_{slot} - T_{pkt} - T_{uncertainty} = 239 \ \mu\text{s} \tag{2.15}$$

The transceiver must complete a transition between transmitting and receiving during the T_{down} period, including the settling of the frequency synthesizer. Likewise, the downtime of the multiple time slot packets can be calculated in similar fashion. The worst case is a 3-time-slot packet, which has 229 μs of downtime. Note that the settling time of the frequency synthesizer is only a fraction of the turnaround time because the blocks following the mixer, such as variable gain amplifier (VGA), also need certain amount of time to settle once the frequency synthesizer is settled.

Wireless LAN standards explicitly specify channel agility to be 224 μs in the standard Section 18.4.6.12 [5]. A frequency synthesizer is considered to be settled when the center frequency is stable within the frequency accuracy limit, which is ± 60 kHz for the case of 802.11b. Finally Table III summarizes the settling time requirements for Bluetooth, WLAN 802.11a, and 802.11b. T_{down} is a theoretical maximum of the settling time for synthesizer. 75% and 50% of T_{down} is also shown

for more realistic specifications. Generally a settling time of in the order of 100 μs is required for safe operation.

D. Spectral Purity

The spectral purity of the local oscillator is usually not explicitly specified in most of the communication standards. Instead, phase noise and spurious signal specifications are usually derived from adjacent channel interference requirements [6]. The strongest adjacent channel interferences of several popular short-range standards are listed in Table I.

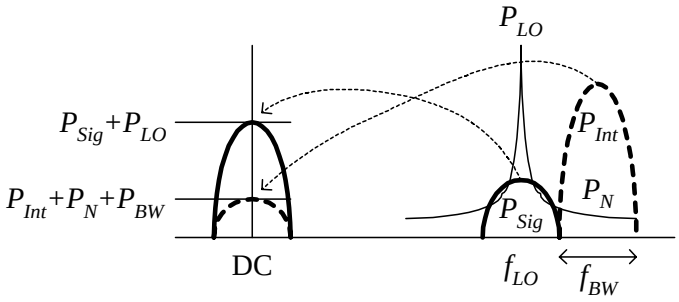


Fig. 5. The effect of phase noise and interference

The effect of phase noise and adjacent channel interference is shown in Fig. 5. While the signal (P_{Sig}) is downconverted to DC or IF by the LO signal (P_{LO}), the interference (P_{Int}) is also downconverted to DC or IF by the phase noise (P_N) and is added to the signal of interest. Since the phase noise is a random process, the effective bandwidth (P_{BW}) is added to calculate the total power. The signal to noise ratio (SNR) of the baseband signal is the difference of the power of the two, and it must be larger than the minimum SNR required to meet the receiver bit error rate (BER) requirement

$$SNR = (P_{Sig} + P_{LO}) - (P_{Int} + P_N + P_{BW}) > SNR_{min} \tag{2.16}$$

After rearrangement,

$$P_N - P_{LO} < (P_{Sig} - P_{Int}) - P_{BW} - SNR_{min} \tag{2.17}$$

where $P_N - P_{LO}$ denotes the phase noise requirement in dBc – a power spectrum density relative to the carrier power. For example, from Table I, Bluetooth standard specifies an interferer of +40 dB at 3 MHz away from the desired signal. The channel bandwidth is 1 MHz, which translates into $P_{BW} = 10 \log 10^6 = 60$ dB. The minimum SNR requirement for a BER of 10^{-3} is 18 dB, which can be determined from system level baseband simulations[1]. SytemView™software is used to simulate GFSK coded baseband signal for Bluetooth system. The BER of the final signal is measured while sweeping the additional noise power. Substituting these numbers in (2.17), the phase noise requirement is −118 dBc at 3 MHz from carrier. This calculation assumes the phase noise is white within the channel bandwidth. A realistic design goal should include some margin from the calculated value.

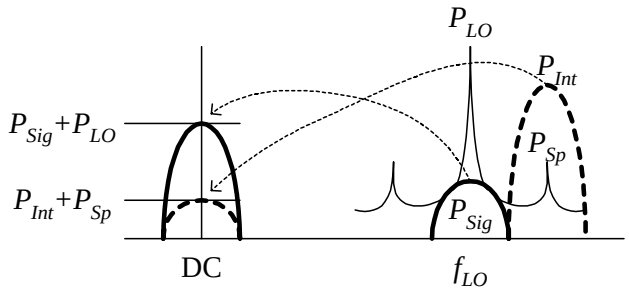


Fig. 6. The effect of reference spur and interference

Reference spur can be a especially serious problem if the system uses narrow channel spacing and the spur coincide with the adjacent channels as shown in Fig. 6.

[1]Since the adjacent channel downconversion due to phase noise is an additive noise to the existing noise in the received signal, SNR_{min} must be 3 dB higher than the calculated value.

This kind of situation can happen when implementing Bluetooth transceivers with an integer-N type frequency synthesizer. The calculation is similar to the previously presented for phase noise case except that the interference is downconverted by spurious signal, which is considered as a single tone. With the SNR of the baseband signal being,

$$SNR = (P_{Sig} + P_{LO}) - (P_{Int} + P_{Sp}) > SNR_{min} \tag{2.18}$$

After rearrangement,

$$P_{Sp} - P_{LO} < P_{Sig} - P_{Int} - SNR_{min} \tag{2.19}$$

where $P_{Sp} - P_{LO}$ denotes the power of spurious signal in dBc, relative to the carrier power. For example, Bluetooth standard specifies an interferer of +30 dB ($P_{Sig} - P_{Int}$) at 2 MHz away from the desired signal. The reference spur can be also at 2 MHz away from the carrier if the frequency of the reference signal is 2 MHz. The minimum SNR requirement is 18 dB (SNR_{min}), same as the previous example. Substituting the numbers in equation (2.19), the spurious signal requirement results in -48 dBc at 2 MHz from carrier.

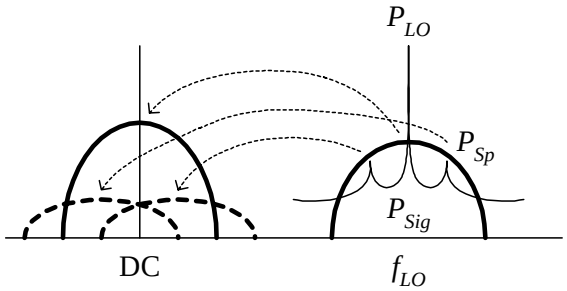


Fig. 7. The effect of reference spur in 802.11b system

In the case of Wireless LAN 802.11b as shown in Fig. 7, the reference spur can fall *within* the received signal, not the adjacent channel because the channel bandwidth can be larger than the reference frequency. The SNR of the received signal is degraded

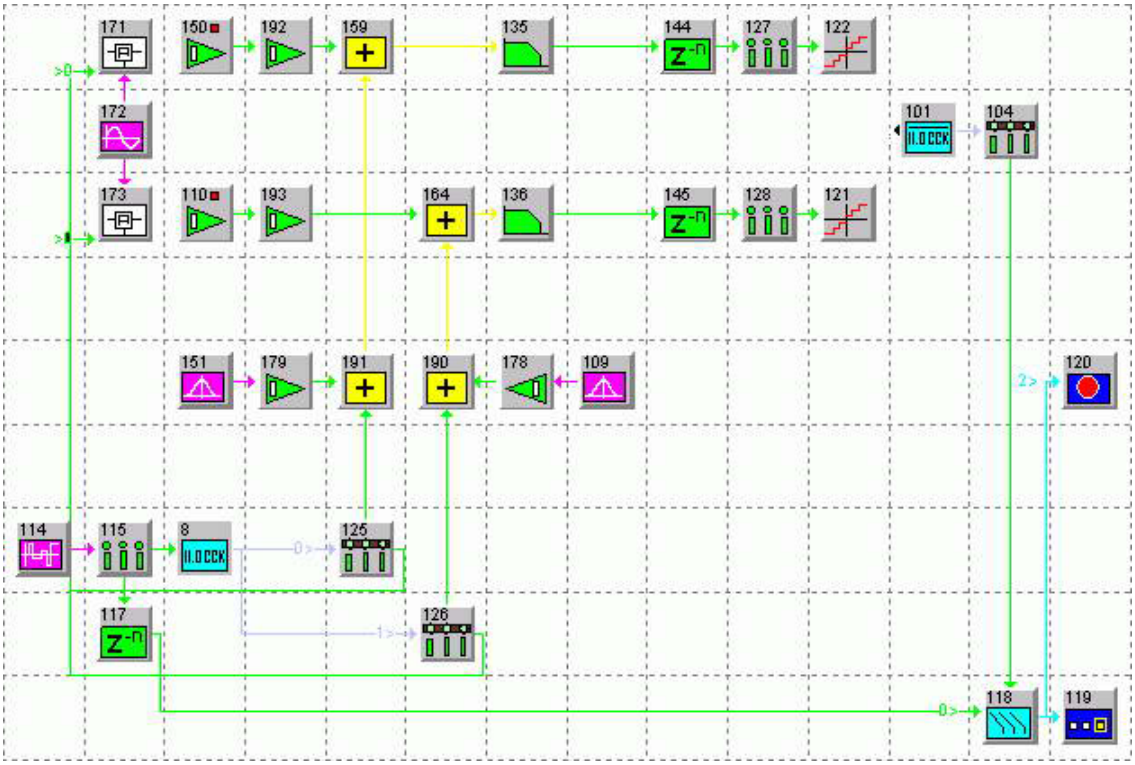


Fig. 8. Block diagram of SystemView^{TM} setup

by a pair of downconverted signals of itself due to spurs. If we assume the effect of the downconverted signals due to spurs is comparable to that of the existing input noise, we can calculate the SNR at the output of the mixer as,

$$SNR = (P_{Sig} + P_{LO}) - (P_{Sig} + P_{Sp} + 6\ dB) > SNR_{min} \tag{2.20}$$

where 6 dB comes from the fact that there are two side bands (+3 dB) and existing input noise (+3 dB). After rearrangement,

$$P_{Sp} - P_{LO} < -SNR_{min} - 6\ \text{dB} \tag{2.21}$$

Since the minimum SNR requirement at the output of the mixer is 21.5 dB, the spur requirement is less than 27.5 dB.

More accurate result can be found from system level simulations taking into account the effect of filtering and correlation factor. Also, the dynamics of the spurs such as sensitivity to input SNR and BER can be determined by simulating the specific level of spur that degrades the receiver BER below the given specification. The complementary code keying (CCK) coded baseband signal of 802.11b system is simulated using SytemView^{TM}software. The block diagram of the setup in SytemView^{TM}is shown in Fig. 8. Source signal is a random digital bit stream generated by token #114 on the lower left corner. The source signal is CCK coded by an encoder token #8. The baseband signal is formed by adding (token #190 and #191) the encoded source signal and white noise (noise source token #151 and #109). The power of the added white noise can be adjusted by gain stages (token #178 and #179), so that the signal-to-noise ratio (SNR) of the input signal can be programmed. The same source signal is redirected and then up-converted (mixer token #171 and #173) by 2 MHz to emulate the spurious signals at the same frequency offset away from the carrier. The baseband signal and the up-converted spurious signal is added (token #159 and #164) to simulate the degradation due to reciprocal mixing. The mixed baseband signal is filtered by a pair of low pass filters (token #135 and #136). Decoding of the final signal is done by a CCK decoder (token #101). Finally the degradation of the signal is measured in terms of BER by BER measurement block (token #118) comparing the original bit stream from the source and the output bit stream from the decoder.

Simulation results are presented in Fig. 9. The SNR of the input signal swept from 10.5 dB to 14 dB, while four different spur power of -34, -28, -22 and -16 dB are degrading the input signal. The result shows that the reference spur must be at least 25 dB below the carrier signal to keep a BER better than 10^{-5} when the input SNR is 12 dB. This requirement needs additional margin for a realistic design

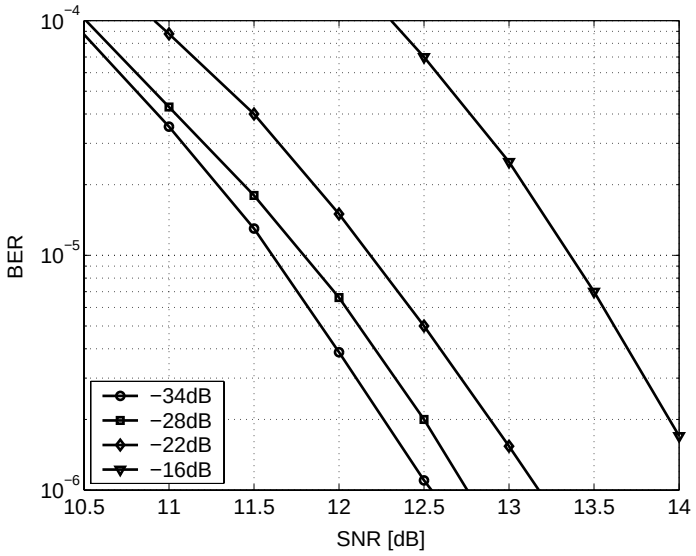


Fig. 9. The effect of reference spur at 2 MHz in 802.11b system

Table IV. Spectral purity requirements

	Reference spurs	Phase noise
Bluetooth	−54 dBc at 2 MHz offset	−124 dBc/Hz at 3 MHz offset
802.11a	−40 dBc at 2.5 MHz offset	−126 dBc/Hz at 40 MHz offset
802.11b	−40 dBc at 2 MHz offset	−126 dBc/Hz at 25 MHz offset

because it is sensitive to the variation of the input SNR: if the input SNR drops to 11.5 dB, the spur rejection requirement is increased by 9 dB, resulting in 34 dB below the carrier.

Table IV summarizes the reference spurs and phase noise specifications calculated for Bluetooth and WLAN standards. All the specifications assume 6 dB margin from the raw calculated values. More robust design can use higher margin such as 12 dB.

Table V. Summary of specification mapping

Standard		Specification	
General	802.11b	General	802.11b
Frequency Band	2412–2472 MHz	Tuning range	2412–2472 MHz
Channel spacing	5 MHz	Tuning step	1 MHz
Hopping rate	N/A	Settling time	224 μs
Packet structure	N/A	Settling time	N/A
Interference	+35 dB at 25 MHz	Phase noise	−126 dBc at 25 MHz
Interference	N/A	Spur rejection	−25 dBc at 2 MHz

Table V summarizes the mapping relationship between the communication standard and the building block specification. It is possible for several aspects of the standard to be mapped into a single specification, and vice versa. For illustration purpose, a specific example for 802.11b standard is given in separate columns. Note that the example shown here is only valid for a direct-conversion type receiver architecture, but is not universally applicable. Depending on the choice of IF, the tuning range and step may result in different values.

CHAPTER III

FREQUENCY SYNTHESIZER: A PRIMER

A. Introduction

A frequency synthesizer (FS) is a device capable of generating a set of signals of given output frequencies with very high accuracy and precision from a single reference frequency. The signal generated at the output of the frequency synthesizer is commonly known as local oscillator (LO) signal, since it is used in communication systems as the reference oscillator for frequency translation as shown in Fig. 10. The reference signal at high frequency is used to downconvert the incoming signal into a lower frequency where it can be processed to extract the information it is carrying. The same reference signal can be used to upconvert a desired message to an RF frequency, such that it can be transmitted over the medium.

Normally, the FS output signal is a sinusoidal tone plus harmonic tones that are added due to non-linearities. Fundamentally, the whole frequency synthesizer system is designed to ensure the accuracy of its output frequency under any condition. In fact, the accuracy requirements are so tight that the accuracy are in the order of tens of ppm. For example, the final frequency accuracy in Wireless LAN 802.11a standard is 20 ppm, which translates into 116 kHz for a carrier frequency of 5.805 GHz [1]. In

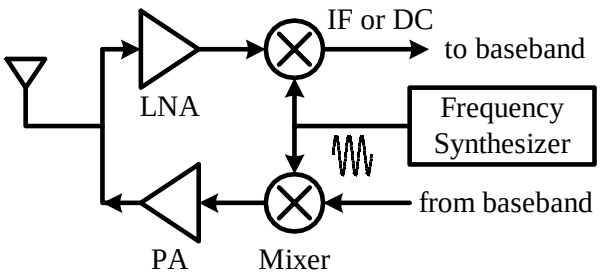
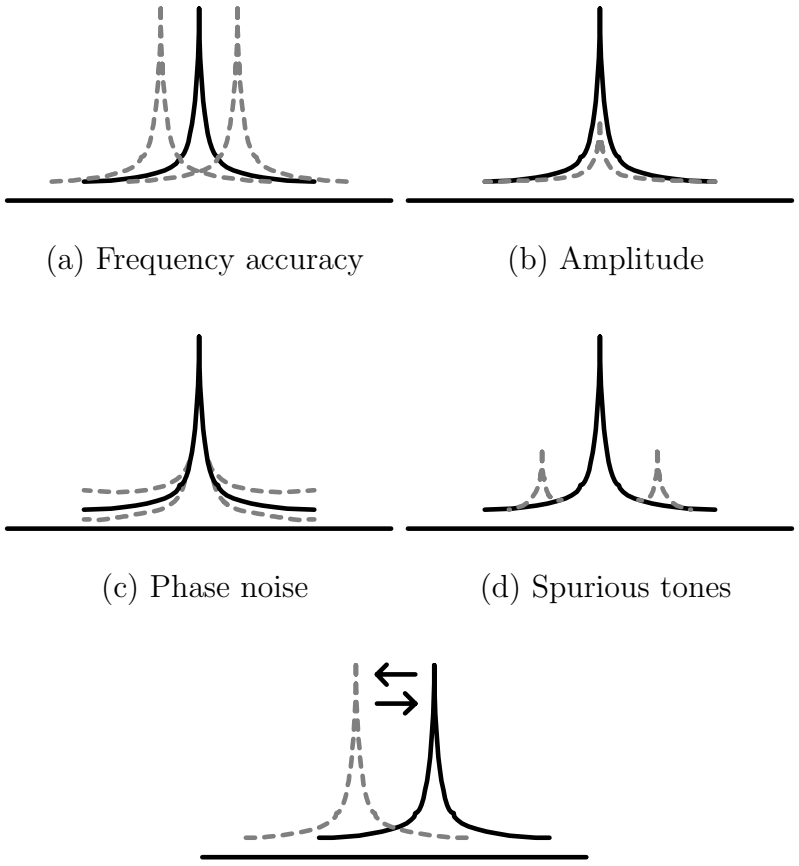


Fig. 10. The role of a frequency synthesizer in a communication transceiver

addition to the frequency accuracy, the spectral purity of the output signal and the settling time determine the performance merits of a frequency synthesizer.



(a) Frequency accuracy (b) Amplitude

(c) Phase noise (d) Spurious tones

(e) Settling time

Fig. 11. Performance merits of frequency synthesizer

Five important performance merits of frequency synthesizer are illustrated in Fig. 11. Amplitude requirement is usually dictated by mixers, which take the output of synthesizer as one of its inputs. The mixers require the amplitude of the LO signal to be higher than certain level so that the conversion gain is large enough for the incoming RF signal. However, the amplitude cannot be indefinitely large since it can leak through the mixer and affect the performance of the front end low noise

amplifier (LNA). Eventually the leaked LO signal is mixed with itself and appear as a DC offset at the output of the mixer. The DC offset due to LO leakage is one of the most critical problem in direct-conversion architecture receiver.

The spectral purity requirement can be divided into two aspects: phase noise and spurious tones. Phase noise is random deviation of the frequency of the synthesizer output due to noise injected into the oscillator. The spectrum shows different levels of skirts around the carrier frequency as shown in Fig. 11(c). All the building blocks of a synthesizer can affect the phase noise performance. In wireless systems, the phase noise contribution of the oscillator itself has the most prominent effect on the overall transceiver operation. Spurious tones occur when the input reference frequency modulates the VCO, generating sidebands around the carrier. The sidebands are exactly input reference frequency away from the carrier in the spectrum. If the reference frequency is small enough that the sidebands fall in the band of interest, they can have serious detrimental effect.

Although the design of a frequency synthesizer is based on the traditional design methodology of a PLL, monolithic implementations for mobile systems have their own nuances. Due to sampling nature of frequency divider, the loop characteristic of frequency synthesizer deviates from well known second order PLL. A practical design procedure to meet stability limit and settling time is derived from analytic transfer function. In a fully integrated system, frequency synthesizer design is a major challenge since it has to meet stringent and conflicting requirements.

This chapter discusses the general design considerations and recent developments of frequency synthesizers designs. Section B and C covers the details of conventional frequency synthesizer. Section D deals with the non-ideal effects, such as phase noise and reference spurs. Section E summarizes the recent development of advanced techniques to improve the performance of frequency synthesizers. We assume the

reader has a basic understanding of PLL operation [7] and builds on that knowledge to describe more detailed design issues particular to wireless communications frequency synthesizers.

B. Types of Frequency Synthesizers

1. PLL Based Integer-N Synthesizer

The most popular technique of frequency synthesis is based on the use of a PLL. The loop is synchronized or locked when the phase of the input signal and the phase of the output from the frequency divider are aligned. As shown in Fig. 12, the output of the VCO in the integer-N synthesizer is divided and phase-locked to a stable reference signal. Once the loop is locked, the output frequency equals the reference frequency times N.

$$f_{out} = N \cdot f_{REF} \tag{3.1}$$

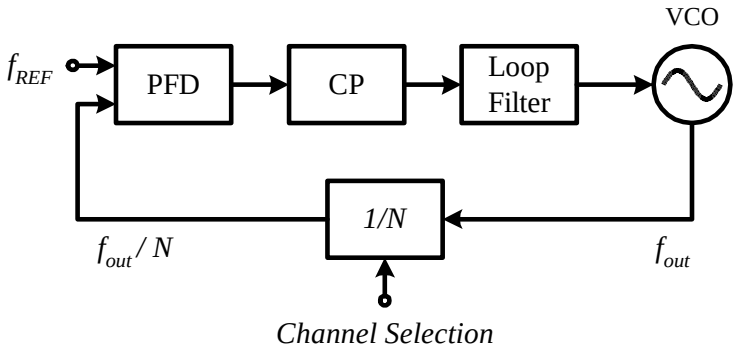


Fig. 12. Integer-N architecture

Integer-N architecture is the preferred solution for minimizing power consumption and die area due to its simplicity. The integer-N architecture, however, lacks the flexibility of arbitrarily choosing f_{REF} as is possible in more complex architectures. Since f_{REF} is fixed by channel spacing requirements, the loop bandwidth can

be severely limited, especially since it has to be significantly lower than f_{REF} for stability considerations.

Although, the integer-N synthesizers can generate output frequencies in steps of f_{REF}, the channel spacing is not necessarily equal to f_{REF}. The maximum possible f_{REF} can be calculated as follows: First, the channel frequencies must be integer multiples of f_{REF} as shown in equation (3.1), but at the same time the channel spacing also has to be an integer multiple of f_{REF}. To satisfy both conditions, the f_{REF} has to be the greatest common divisor (GCD) of the channel frequency and the channel spacing. For example, Wireless LAN 802.11b standard specifies channels from 2412 MHz to 2472 MHz in steps of 5 MHz. Thus, the maximum possible f_{REF} is $GCD(2412 \text{ MHz}, 5 \text{ MHz}) = 1$ MHz. For a different example, Wireless LAN 802.11a standard specifies a channel at 5805 MHz and a step of 20 MHz. In this case, the maximum possible f_{REF} is $GCD(5805 \text{ MHz}, 20 \text{ MHz}) = 5$ MHz.

2. PLL Based Fractional-N Synthesizer

An inherent shortcoming of the integer-N synthesizer is the limited option for the reference frequency, f_{REF}, because of the integer-only multiplication. A fractional-N synthesizer architecture solves this problem by allowing fractional feedback ratios. Shown in Fig. 13, the fractional-N synthesizer has a dual modulus divider that can switch its division ratio between N and $N + 1$. By dividing the VCO frequency by N during K VCO cycles and $N + 1$ during $(2^k - K)$ VCO cycles, it is possible to make the average division ratio equal to $N + K/2^k$, assuming a k bits accumulator controlling the prescaler. Thus,

$$f_{out} = (N + \alpha) \cdot f_{REF} \quad \text{,where } 0 < \alpha < 1 \tag{3.2}$$

However, if the division modulus is switched periodically, the output is modulated

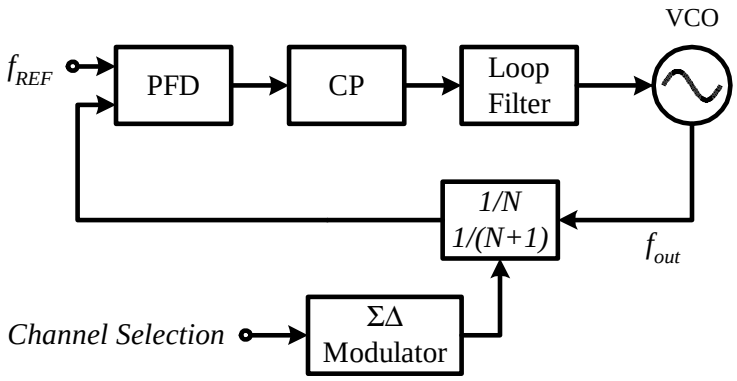


Fig. 13. Fractional-N architecture

by the beat frequency of the fractional modulus. It can be shown that the output spectrum has tones at αf_{REF}, $2\alpha f_{REF}$ and so on, relative to the carrier frequency. These are fractional spurs and can be problematic since they are very close to the carrier.

The fractional spurs can be reduced by breaking the regularity of the division modulus switching period, effectively making the beat frequency randomized. A dithering mechanism using $\Sigma\Delta$ modulator can not only randomize the beat frequency, but shape the noise spectrum so that it has more power at higher frequency. The high frequency quantization noise is filtered by the loop filter of the PLL. A combination of the order of the $\Sigma\Delta$ modulator and loop filter order can reduce the high frequency quantization noise at levels that make the effect of the noise negligible [8].

3. Direct Digital Synthesizer (DDS)

A fundamental reason that a feedback control loop is used in the implementation of frequency synthesizers is because the relationship between the control voltage and the output frequency of a VCO is unpredictable and subject to variations from unwanted excitations. If a VCO's output signal frequency were always predictable with no

variation, there would be no need to use feedback control to correct the error in frequency. The output of the VCO would be used directly as the final output of the frequency synthesizer. In this hypothetical system, there would be no problem of stability and settling time. The settling time would be only limited by the gate delay of the channel selection input.

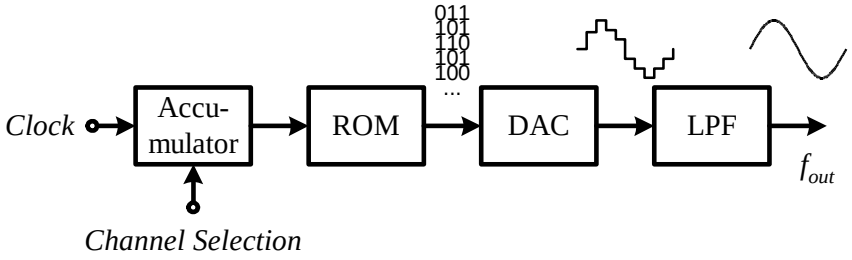


Fig. 14. Direct digital synthesizer block diagram

DDS generates its output signal from the digital domain and converts it in analog waveform through a digital-to-analog converter (DAC) and filtering as shown in Fig. 14. Since the waveform is directly shaped from the amplitude values from a read-only-memory (ROM), it doesn't require feedback and it has all the advantages of the hypothetical system previously described. In addition, it has other advantages such as low phase noise and possibility of direct digital modulation. The DDS is a suitable choice when the carrier frequency has to be settled very fast with very low phase noise [9]. The application of the FS is to generate frequency-hopped carrier signals for NMT-900 cell phone standard. Another usage of DDS is when extremely fine frequency resolution is required [10]. This synthesizer covers a bandwidth from DC to 75 MHz in steps of 0.035 Hz with a switching speed of 6.7 ns.

The most serious shortcoming of DDS is speed: the clock of the digital circuitry has to be at least twice as high as the output frequency. Operating a ROM and a DAC at 4.8 GHz to generate 2.4 GHz output signals can be challenging in current

technologies, if at all possible, and power consumption will be prohibitively high. In addition, large quantization noise and harmonic distortion of high speed DACs can degrade the spectral purity of the output signal. Using an analog mixer to upconvert a low frequency synthesized signal, in order to generate high frequency outputs without an excessively high frequency clock, has been reported in literature [11]. However, it is a costly solution since it needs an extra analog PLL and high frequency mixers.

C. Phase Locked Loop (PLL) Design

This section covers the fundamentals of PLL design for frequency synthesizers. Rather than focusing on circuit implementation issues, system level designs such as loop transfer function and stability considerations are addressed with insightful observations. Extensive PLL design techniques can be found in [7, 12, 13].

1. Charge Pump PLL

Virtually all of the PLL-based frequency synthesizers utilize a charge pump PLL that was first introduced by Gardner [14]. Charge pump PLL has important advantages that make it suitable for the implementation of frequency synthesizers. These advantages include:

1. The operation of phase frequency detector (PFD) makes the frequency acquisition range not limited by loop bandwidth but only by VCO tuning range.

2. Due to poles at the origin, charge pump PLL has infinite open-loop gain at DC, which make the static phase error to be ideally zero.

Since the role of a frequency synthesizer is to generate a signal with precise frequency over given bandwidth, acquisition is more important operation rather than

tracking as in data/clock recovery system. Whenever the transceiver needs to switch between channels, the loop has to go out of lock and then acquire the new frequency. The fact that the reference frequency is fixed further diminishes the importance of tracking behavior. Emphasis on the acquisition suggests that the ideal PLL architecture for frequency synthesizers should incorporate PFD that gives full range acquisition.

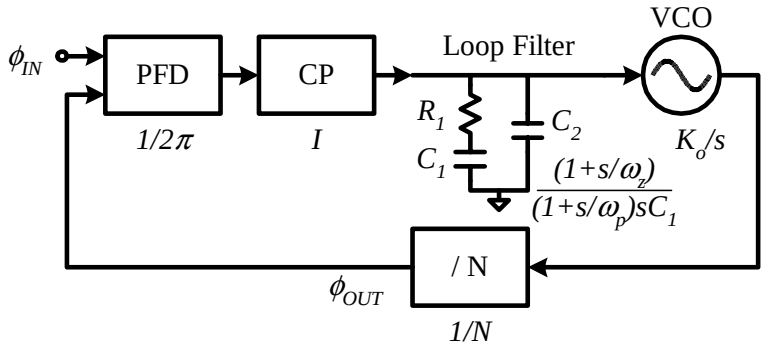


Fig. 15. Charge pump PLL block diagram and linear approximation

A simplified block diagram of the charge pump (CP) PLL is shown in Fig. 15. The fundamental process of operation is as follows. First, the VCO oscillates at its natural frequency assuming the control voltage is arbitrary at the beginning. The PFD compares the phase difference between the reference signal ϕ_{IN} and the VCO output divided by the frequency divider, ϕ_{OUT}. The output of the PFD is a series of pulses whose duty cycle is proportional to the phase difference $\phi_{IN} - \phi_{OUT}$. The CP converts the voltage pulses into current pulses with a predetermined amplitude I. The loop filter converts the current pulses into a low-pass filtered voltage signal that controls the frequency of the VCO. If the feedback is negative, the error between ϕ_{IN} and ϕ_{OUT} gradually become smaller and smaller until $\phi_{IN} = \phi_{OUT}$. In this state the loop is referred to be *locked*. Once the loop is locked, the frequency of the VCO output is equal to the frequency of the reference multiplied by the feedback factor N.

The process of locking is not instantaneous because the loop has a limited bandwidth. The transfer function of the loop has to be studied to estimate the behavior of the loop during its transient operation. Since the operation of the PFD and CP is performed in the discrete-time domain, the complete transfer function becomes complicated due to the z-transform representation. A more intuitive equation can be obtained by assuming the phase error is small. With this assumption, the PFD and CP are modelled as simple gain blocks, $1/2\pi$ and I respectively, as shown in Fig. 15.

The linear approximation gives two critical equations useful for the initial design of a PLL. The first equation is an open-loop transfer function which is ϕ_{OUT}/ϕ_{IN} assuming the loop is opened between the frequency divider and the PFD.

$$H_{open}(s) = \frac{\phi_{OUT}}{\phi_{IN}} \tag{3.3}$$

$$= \frac{K_D K_o (1 + s/\omega_z)}{(1 + s/\omega_p)s^2} \tag{3.4}$$

where $K_D = I/(2\pi C_1 N)$, $\omega_z = 1/(R_1 C_1)$ and $\omega_p \simeq 1/(R_1 C_2)$. The open-loop transfer function is important because its phase margin indicates how stable the system will be after the loop is closed. Note that there are two poles at the origin and a stabilizing zero is required to compensate for them. Details of PLL stability are covered in section 2.

The second equation is a closed-loop transfer function ϕ_{OUT}/ϕ_{IN}. It can be also calculated from $H_{open}(s)/(1 + H_{open}(s))$.

$$H_{closed}(s) = \frac{\phi_{OUT}}{\phi_{IN}} \tag{3.5}$$

$$= \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/(K_D K_o) + s^3/(\omega_p K_D K_o)} \tag{3.6}$$

For simplicity, it is assumed that ω_p is placed at very high frequency with respect to the natural frequency $\omega_n = \sqrt{K_D K_o}$, then the transfer function becomes second

order.

$$H'_{closed}(s) \simeq \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/(K_D K_o)} \tag{3.7}$$

The step response of the closed-loop transfer function shows the locking transient, and settling time performance can be determined from the transient waveform. Analytic solution of the settling time can be derived from the second order transfer function. The details of the settling analysis is covered in section 3.

2. Stability

As in any feedback system, stability is one of the most important aspects of the design considerations of frequency synthesizers. A potentially unstable synthesizer will generate an output signal whose frequency doesn't converge but *oscillates* between certain frequency limits. The unstable output signal appears similar to narrow-band FM modulated signal. An example of the measurement result of an unstable synthesizer is shown in Fig. 16. The loop is forced to be unstable by increasing the charge pump current over the limit. The waveform shows the transient response of the VCO control voltage. The control voltage starts at high voltage level and then tries to acquire a new level at lower voltage as the channel selection input changes. However, it fails to settle at the destination voltage level but oscillate until the next channel selection forces it back to the original voltage level. Note that the loop is stable at higher control voltage level. This shows the stability condition of the loop depends on current state of the operation.

There are two sources for the stability limit in charge pump PLL. The first comes from the fact that the operation of PFD and CP is in the discrete-time domain. Loop bandwidth has to be carefully chosen so that the linear approximation is not violated i.e. $\omega_c < \omega_{REF}$. The second comes from the two poles at the origin in the open-loop

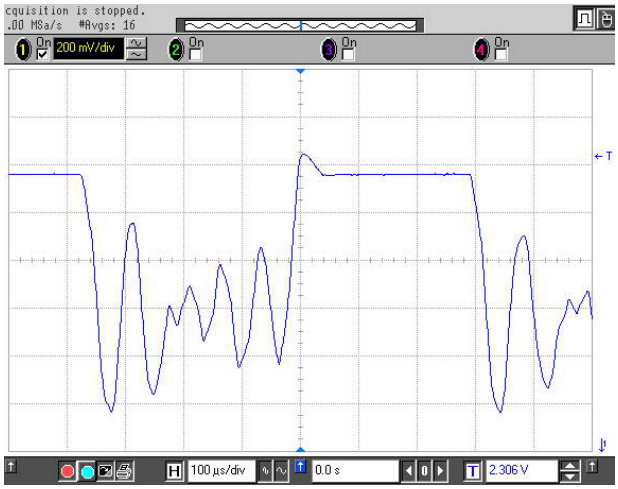


Fig. 16. Measurement results of an unstable synthesizer

transfer function. A stabilizing zero can compensate for the effect of the double poles at crossover frequency. More detailed analysis on stability limit follows.

First, the charge pump PLL has a critical stability limitation due to the discrete nature of the PFD and CP output. The PLL operates as a sampled system and not as a straightforward continuous-time circuit. It is known that a sampled second-order PLL will become unstable if the loop gain is made so large that the bandwidth becomes comparable to the sampling frequency. Limited loop gain sets upper boundary of the loop bandwidth obtainable for a given input reference frequency. Gardner's stability limit [14] states that:

$$\omega_n^2 < \frac{\omega_{REF}^2}{\pi(\pi + \omega_{REF}/\omega_z)} \tag{3.8}$$

The relationship between the natural frequency (ω_n) and the loop bandwidth (ω_c) is approximately:

$$\omega_c \simeq \omega_n^2/\omega_z \tag{3.9}$$

for critically damped and overdamped system. Substituting (3.9) into (3.8), it can

be rewritten as:

$$\omega_c < \frac{\omega_{REF}}{\pi(1 + \pi\omega_z/\omega_{REF})} \tag{3.10}$$

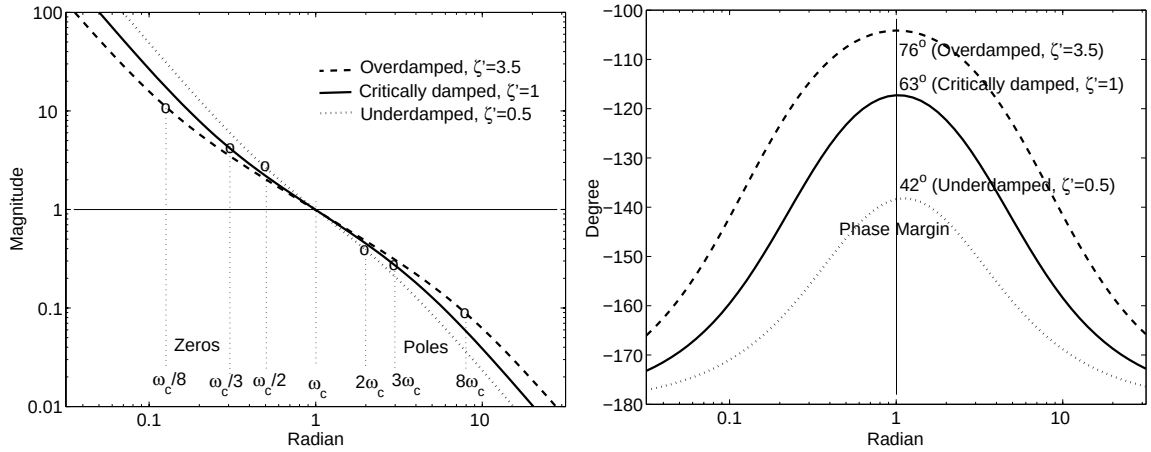
which indicates that the loop bandwidth (ω_c) has to be significantly lower than the frequency of the reference input signal (ω_{REF}). Commonly ω_c is chosen below one-tenth of ω_{REF} to guarantee stability. Another important factor to consider when determining the loop bandwidth is the size of the capacitors to realize the bandwidth. If the loop bandwidth is too narrow, the size of the capacitors can be excessively large to be implemented in a fully-integrated solution. Using dual-pass active filter [15] or impedance multiplier [16] are proposed to emulate a large capacitance without consuming huge die area. Their application is limited to a multiplication factor no more than 20 due to uncertainties from mismatch. Furthermore, the additional active device in the signal path can degrade phase noise and increase reference spurs due to leakage current.

The second stability limit comes from the open-loop transfer function. As has already been shown in equation (3.3), the open-loop transfer function of a charge pump PLL has two poles at the origin, which makes the loop inherently unstable. A zero should be placed at a lower frequency than the crossover frequency to make the phase margin large enough ($> 45°$). Since the zero reduces the slope of the magnitude response, an additional pole at a higher frequency than the crossover frequency is also required to maintain adequate spurious signal rejection.

Three examples of different pole/zero placements are shown in Fig. 17. The open-loop transfer functions of those three examples referred to (3.3) are

$$H_{under}(s) = \frac{1 + 2s}{2(1 + s/2)s^2} \tag{3.11}$$

$$H_{critical}(s) = \frac{1 + 3s}{3(1 + s/3)s^2} \tag{3.12}$$



(a) Magnitude (b) Phase

Fig. 17. The effect of pole/zero placement on phase margin. (a) Pole/zero are placed 2, 3 and 8 times crossover frequency ω_c. (b) Phase margin increases from 42° to 76° as pole/zero are placed farther apart.

$$H_{over}(s) = \frac{1+8s}{8(1+s/8)s^2} \tag{3.13}$$

When a zero is located at 1/3 of the crossover frequency (w_c) and a pole is placed at 3 times of w_c, the loop is critically damped with the pseudo-damping ratio (ζ') of 1. A phase margin of 63° can be achieved. When the zero is at $w_c/2$ and the pole is at $2w_c$, the loop is underdamped with the damping ratio of 0.5. With an underdamped loop, the phase margin is lowered to 42° and the transient signal overshoots. When the zero is at $w_c/8$ and the pole is at $8w_c$, the loop is overdamped with a damping ratio of 3.5. With an overdamped loop, the phase margin is increased to 76° but the settling time is degraded due to slow response.

3. Settling Time

Settling time is another important performance metric that is directly related to the loop transfer function. Settling time determines how fast the frequency synthesizer

can change the frequency of its output signal.

The transient step response of the third-order system can be calculated from the closed-loop transfer function shown in the equation (3.6). The transfer function can be greatly simplified by placing the stabilizing zero (ω_z) and the additional pole (ω_p) at the equal ratio-distance (α^2) from the crossover frequency (ω_c) [17]. With this placement strategy, we can determine the frequencies as,

$$\omega_z = \omega_c/\alpha^2 \tag{3.14}$$

$$\omega_p = \omega_c \times \alpha^2 \tag{3.15}$$

$$\omega_c = \alpha\omega_n = \sqrt{\omega_z\omega_p} \tag{3.16}$$

$$\omega_n = \sqrt{K_D K_o} \tag{3.17}$$

With the above assumption, the closed-loop transfer function can be simplified as,

$$H_{closed}(s) = \frac{\alpha^4\omega_n^2(s+\omega_z)}{s^3 + \alpha^3\omega_n s^2 + \alpha^4\omega_n^2 s + (\alpha\omega_n)^3} \tag{3.18}$$

$$= \frac{\alpha^4\omega_n^2(s+\omega_z)}{(s+\alpha\omega_n)\{s^2 + \alpha\omega_n(\alpha^2-1)s + (\alpha\omega_n)^2\}} \tag{3.19}$$

$$= \frac{\alpha^2\omega_n'^2(s+\omega_z)}{(s+\omega_n')(s^2 + 2\zeta'\omega_n' s + \omega_n'^2)} \tag{3.20}$$

The equation (3.19) shows that this system has one real pole at $-\alpha\omega_n$ and two complex conjugate poles. We can define a pseudo-damping factor (ζ') and natural frequency (ω_n') for the complex conjugate poles [18] as follows;

$$\omega_n' = \alpha\omega_n \tag{3.21}$$

$$2\zeta'\omega_n' = \alpha\omega_n(\alpha^2-1) \tag{3.22}$$

$$\Rightarrow \zeta' = (\alpha^2-1)/2 \tag{3.23}$$

Note that the damping factor of the second-order approximation (ζ) is defined as $\zeta = \omega_n/(2\omega_z)$. The relationship between the second-order damping factor and the pseudo-damping factor can be shown as

$$\zeta = \frac{\sqrt{2\zeta' + 1}}{2} \tag{3.24}$$

The step response can be calculated by inverse Laplace transform of equation (3.20). The result is,

$$h(t) = 1 + \frac{\zeta' e^{-\omega'_n t}}{\zeta' - 1} + \frac{e^{(\sqrt{\zeta'^2 - 1} - \zeta')\omega'_n t}}{2\zeta' - 2} + \frac{e^{(-\sqrt{\zeta'^2 - 1} - \zeta')\omega'_n t}}{2\zeta' - 2} \tag{3.25}$$

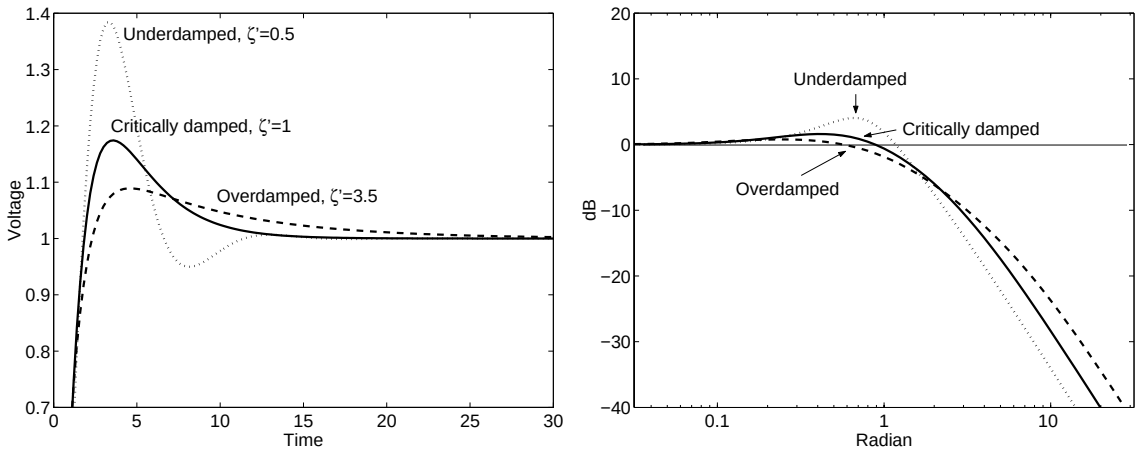
$$= 1 + \frac{\zeta' e^{-\omega'_n t}}{\zeta' - 1} + \frac{e^{-\zeta'\omega'_n t}}{\zeta' - 1} \cos(\sqrt{1 - \zeta'^2}\omega'_n t) \qquad \text{(when } \zeta' < 1\text{)} \tag{3.26}$$

If the pseudo-damping factor is larger than one ($\zeta' > 1$), then there are no complex-conjugate poles; all three poles are on real axis. The transient response is non-oscillatory and has a tendency for sluggish response. The system will behave like an overdamped system. However, the response have a overshoot due to multiple exponent terms, unlike the overdamped second-order system. If the pseudo-damping factor is equal to one ($\zeta' = 1$), all three poles are coincide at the same frequency of ω'_n. The transient response is still non-oscillatory and has larger overshoot than the overdamped response. If the pseudo-damping factor is less than one ($\zeta' < 1$), the complex-conjugate poles will add ripple to the response curve. The effect of the pseudo-damping factor is summarized in Table VI.

Three examples of the transient step responses of the third-order transfer functions are shown in Fig. 18(a). The closed-loop transfer functions of the examples

Table VI. The effect of pseudo-damping factor in third order system

Pseudo-damping factor (ζ')	Pole/zero placement (α^2)	Phase margin	Maximum overshoot
0.5 (under)	2	42°	40%
1 (critical)	3	63°	20%
3.5 (over)	8	76°	10%



(a) (b)

Fig. 18. Third-order closed loop characteristics. (a) Transient response of underdamped, critically damped and overdamped system (b) Magnitude plot of the closed-loop transfer function shows peaking in underdamped system.

are:

$$\zeta' = 0.5 \;\Rightarrow\; H_{under}(s) = \frac{1+2s}{(1+s)(1+s+s^2)} \tag{3.27}$$

$$\zeta' = 1 \;\Rightarrow\; H_{critical}(s) = \frac{1+3s}{(1+s)(1+2s+s^2)} \tag{3.28}$$

$$\zeta' = 3.5 \;\Rightarrow\; H_{over}(s) = \frac{1+8s}{(1+s)(1+7s+s^2)} \tag{3.29}$$

Normally a critically damped loop works best for a typical frequency synthesizer de-

sign. Underdamping is not desirable since it increases overshoot in transient response while not improving settling time performance considerably. A slightly underdamped loop can be beneficial to keep the optimal settling time when the process variation is significant. When using an underdamped loop, the overshoot has to be kept within the dynamic range of the charge pump and the tuning range of the VCO, otherwise the settling time performance will be degraded.

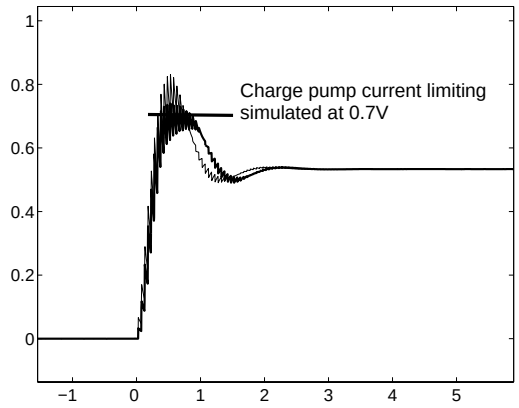


Fig. 19. A simulation result of a settling time degradation due to charge pump current limitation

Once the control voltage reaches the point where the charge pump transistors operate in ohmic region, the charge pump current start to decrease. The loop gain drops proportionally to the charge pump current, and the loop is prone to sluggish response. A simulation shown in Fig. 19 is done with a model in Matlab simulink. The system has an underdamped response as in equation (3.27). The normal transient response is shown in grey waveform. Then the loop gain is dropped to 20% once the control voltage reaches 0.7 V. The settling time degradation is shown in black waveform. If the dynamic range of the charge pump is severely limited, as in a low-voltage design, an overdamped loop can be a better choice to minimize the overshoot. However, the loop bandwidth has to be increased to compensate for the degraded

settling time due to overdamping.

The overshoot in transient response also translates into gain peaking in the frequency domain. Fig. 18(b) shows that an underdamped system has excessive gain peaking due to the stabilizing zero. The gain peaking amplifies the phase noise of the reference signal at the output of the frequency synthesizer. It is recommended to use an overdamped system if the close-in phase noise of the reference signal has considerable effect on the performance. While this issue is almost never of concern in RF system designs, it can be a significant problem in some digital networks, such as token rings [19].

An analytical solution for the settling time can be obtained from the step response of the second-order closed-loop transfer function, equation (3.7). The second-order equation is used because it can provide simpler and more intuitive results. Since equation (3.7) does not take into account the effect of the additional pole, the actual settling time is longer than the analytic solution may suggest, depending on the location of the additional pole. Settling time is a function of the natural frequency (ω_n') and the pseudo-damping factor (ζ'). It can be shown that

$$t_s \simeq \begin{cases} \frac{1}{\zeta'\omega_n'} \ln \frac{\Delta f}{\delta f_o \sqrt{1-\zeta'^2}} & \text{if } \zeta' < 1 \text{ (underdamped)} \\ \frac{1}{\zeta'\omega_n'} \ln \frac{\Delta f}{\delta f_o} & \text{if } \zeta' = 1 \text{ (critically damped)} \\ \frac{1}{(\zeta' - \sqrt{\zeta'^2-1})\omega_n'} \ln \frac{\Delta f(\sqrt{\zeta'^2-1}+\zeta')}{2\delta f_o \sqrt{\zeta'^2-1}} & \text{if } \zeta' > 1 \text{ (overdamped)} \end{cases} \tag{3.30}$$

where f_o is the frequency from which the synthesizer starts the transition, Δf is the amount of frequency jump, and δ is the settling accuracy. As the loop bandwidth ω_c increases, the settling time gets shorter if the damping ratio is fixed. The effect of the damping ratio on settling time is shown in Fig. 20. It is a plot of equation (3.30) with ω_c fixed but not ω_n, which is more realistic in the sense of design procedure. In this

condition, the settling time is fastest when the loop is critically damped, and further underdamping does not improve the settling time. Note that the analytic solution in equation (3.30) is only an approximated result for the second-order closed-loop transfer function, but not for the third-order one.

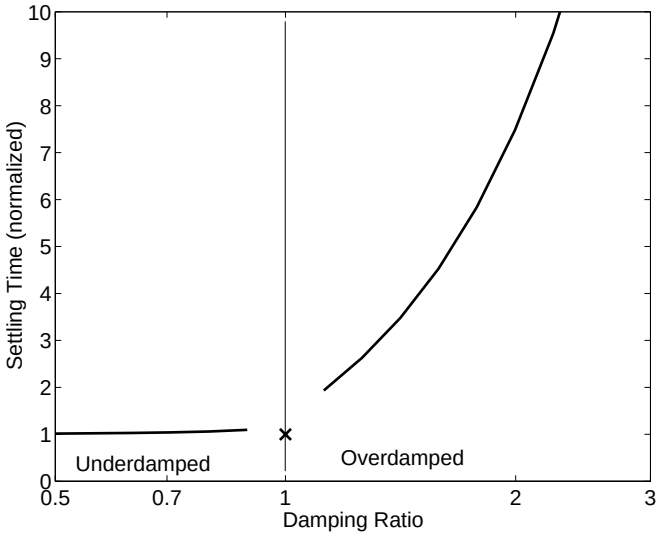


Fig. 20. Settling time vs. damping factor for a second-order PLL

It is apparent that the settling time equation can be used as a quick feasibility test in deciding which architecture to use for target application. Settling test gives a clear idea if it is possible to use Integer-N architecture for given communication standard in early design process, since almost all the design variables are already given. For example, in Bluetooth standard, with $\zeta = 1.2$ for good stability, the settling time required for 0.001% settling is 119 μs. Since the settling time is well below the requirement 239 μs, it is viable to start designing Integer-N frequency synthesizer for Bluetooth receiver. On the contrary, in Global Systems for Mobile Communication (GSM) standard, with the same condition as previous example, the settling time is 292 μs. This is unacceptable even after tweaking to reduce the settling time by risking stability since the entire slot length of the GSM packet is just 577 μs.

Table VII. Summary of PLL design trade-offs

	Loop bandwidth	Damping
Faster settling	wide	under
Better stability	narrow	over
Lower phase noise	wide	N/A
Better spur rejection	narrow	N/A
Low jitter peaking	N/A	over
Low overshoot	N/A	over
Smaller capacitor size	wide	N/A

Finally, the trade-offs of design choices are summarized in Table VII. Loop bandwidth and damping ratios have to be determined carefully, depending on the requirement of the target application, since they improve some aspects of the performance, and deteriorate others at the same time. For instance, in the frequency synthesizer design in [20], the loop bandwidth is $f_c = 830$ kHz and the damping factor is $\zeta = 0.75$, while the reference frequency is $f_{REF} = 11.75$ MHz. Since the loop bandwidth is close to the maximum of the Gardner's limit and the damping is underdamped, the PLL shows a fast settling time performance of 40 μs. However, stability of the system is easily disturbed during the measurement and the transient response waveform shows a large overshoot and ringing. In another design example in [15], the loop bandwidth is $f_c = 45$ kHz and the damping factor is $\zeta = 1$, while the reference frequency is $f_{REF} = 26.6$ MHz. Relatively low loop bandwidth leads to a slow settling time of 250 μs.

4. PLL Design Procedure with an Example

In this section, an example of the design procedure of the frequency synthesizer compliant for Wireless LAN 802.11b standard is presented. The procedure details the considerations for stability and settling time of loop filter design. The same procedure can be applied to different communication standards with minimal modifications.

1. The first step is to determine the reference frequency f_{REF}. For 802.11b standard, the output frequency must cover the range from 2412 MHz to 2472 MHz in steps of 5 MHz. If the quadrature outputs are to be generated by a divide-by-two circuit, the VCO output frequency has to be twice the requirement. Now the system must cover the range from 4824 MHz to 4944 MHz in steps of 10 MHz. Since $GCD(4824, 10) = 2$, the maximum f_{REF} possible is 2 MHz.

2. From the Gardner's stability limit, the loop bandwidth ω_c has to be well below ω_{REF}. Considering that the settling time requirement is relatively relaxed, it is beneficial to make the loop bandwidth very narrow to reduce reference spur. Let $\omega_c = 2\pi \times 30$ kHz, then the loop bandwidth is 66 times below f_{REF}.

3. For optimal settling time performance, place the zero and pole at 1/4 and 4 times the ω_c, resulting the placement ratio of $\alpha^2 = 4$. The second-order approximated transfer function is critically damped with $\zeta = 1$. The third-order transfer function is slightly overdamped with the pseudo-damping ratio of $\zeta' = 1.5$.

4. From equations (3.7) and (3.9), the natural frequency is $\omega_n = \omega_c/(2\zeta) = 2\pi \times 15$ kHz.

5. Now that ω_n and ζ are determined, the settling time can be estimated from the closed form equation (3.30). Using $f_o = 4824$, $\Delta f = 120$ and $\alpha = 25 \times 10^{-6}$,

the estimated settling is $t_s = 73$ μs. It is faster than the required 224 μs by a good margin.

6. From the loop bandwidth and the damping factor, the location of the stabilizing zero can be determined as $\omega_z = \omega_c/(\alpha^2) = 2\pi \times 7.5$ kHz

7. For a good reference spur rejection performance, it is best to place the additional pole as close to the crossover frequency as possible without degrading phase margin. The optimal location of the additional pole is $\omega_p = \omega_c \times \alpha^2 = 2\pi \times 120$ kHz

8. Assuming the VCO gain $K_o = 2\pi \times 300$ MHz/V, the PFD-CP gain is $K_D = \omega_n^2/K_o = 4.7$ V/rad.

9. Assuming the charge pump current $I = 30\mu$A, the rest of the circuit elements can be calculated as follows:
   $C_1 = I/(2\pi K_D N) = 420$ pF
   $R_1 = 1/(\omega_z C_1) = 50.5$ kΩ
   $C_2 = 1/(\omega_p R) = 26.3$ pF

D. Non-ideal Effects

1. Phase Noise

Phase noise is a measure of random uncertainty in the instantaneous frequency of the frequency synthesizer output. Phase noise appears as random variations of zero crossing point in time-domain measurement, and appears as a skirt around the carrier frequency in frequency-domain measurement.

Leeson proposed a simple calculation methodology based on a linear time-invariant (LTI) model [21]. More detailed observation can be made by utilizing a linear time-

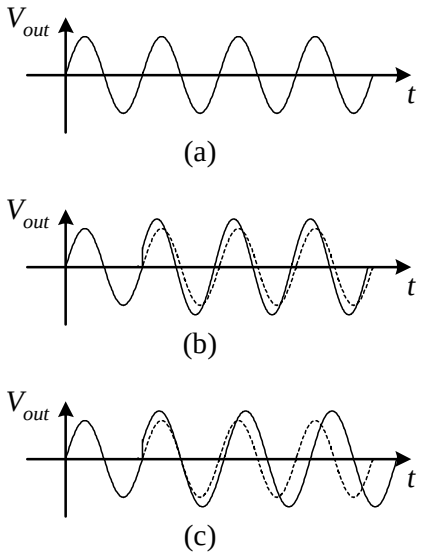


Fig. 21. Time domain explanation of phase noise. (a) Ideal waveform (b) Phase error due to impulse input (c) Effect of different amplitude in non-linear system

variant (LTV) [19] and a non-linear time-variant (NLTV) model. In Fig. 21, we assume that the system is oscillating with some constant amplitude until the impulse occurs. We consider how the system responds to an impulse depending on the linearity and time-variance. In Fig. 21(b) an impulse is injected at the time that displaces the zero crossings. Hence, an impulsive input produces a step in phase. Since the phase displacement depends on when the impulse is applied, the system is obviously time-varying. In a non-linear model as shown in Fig. 21(c), the increased amplitude changes the gain of the transfer function of the non-linear system. Changed gain in turn alters the frequency where the phase inversion occurs. Thus not only the phase, but also the frequency of the oscillation is affected by an impulsive input in non-linear time-variant model. The implication is that a well-controlled amplitude is critical for reducing phase noise in RF oscillators where the usage of an amplitude limiter is prohibitive.

There are several sources of the noise in a synthesizer. The two main noise sources

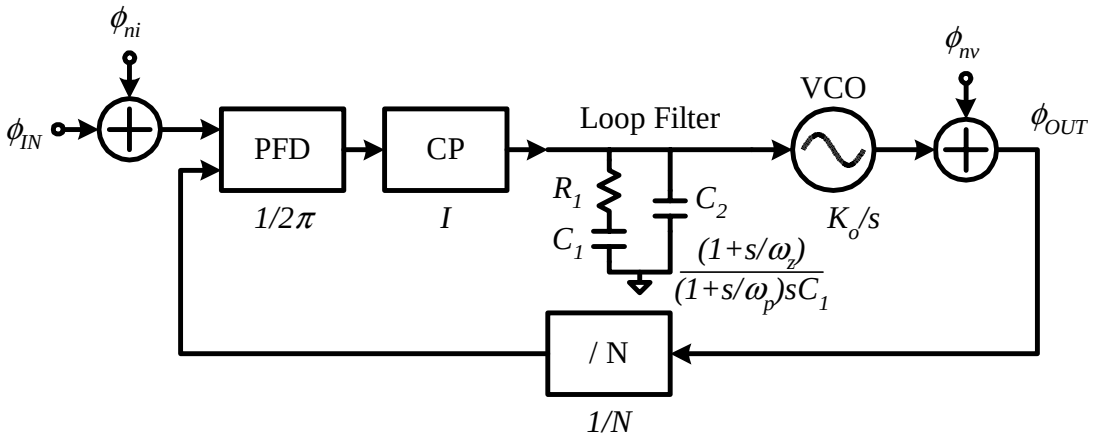


Fig. 22. Noise injection in linear model of PLL

are the noise the VCO, modelled by ϕ_{nv}, and the noise from the reference frequency signal, ϕ_{ni}. Fig. 22 shows a linear model of PLL with the noise input of the VCO and the reference signal included. The noise contribution from the PFD, CP, and loop filter can all be merged into the reference noise, ϕ_{ni}. The transfer function of the noise from ϕ_{ni} to ϕ_{OUT} is similar to the closed loop transfer function of input-output phase shown in (3.6).

$$H_{ni}(s) = \frac{\phi_{OUT}}{\phi_{ni}} \tag{3.31}$$

$$= \frac{N(1 + s/\omega_z)}{1 + s/\omega_z + s^2/(K_D K_o) + s^3/(\omega_p K_D K_o)} \tag{3.32}$$

Although it has low-pass filter characteristics, the transfer function has a gain of N at low frequencies. This low frequency noise amplification is expected from the frequency multiplication of the synthesizer as shown in (3.1). If there is a small phase variation in the reference signal, the phase variation is multiplied by N at the output since the period of the output signal is N times smaller than the input. However, at high frequencies, ϕ_{ni} is attenuated at a roll-off rate of -40 dB/decade. The corner frequency is approximately equal to the loop bandwidth given in (3.9).

The transfer function of the VCO noise from ϕ_{nv} to ϕ_{OUT} shows different behavior. It has high-pass filter characteristics unlike the reference noise.

$$H_{nv}(s) = \frac{\phi_{OUT}}{\phi_{nv}} \tag{3.33}$$

$$= \frac{s^2/(K_D K_o) + s^3/(\omega_p K_D K_o)}{1 + s/\omega_z + s^2/(K_D K_o) + s^3/(\omega_p K_D K_o)} \tag{3.34}$$

At low frequencies, the VCO noise is attenuated at a roll-off rate of -40 dB/decade. At high frequencies, the transfer function converges to unity, which makes the VCO noise shows up at the output without being filtered. The reason behind the reversed filtering effect of the the VCO noise can be explained intuitively. Since the VCO noise is an internally injected within the loop, the loop has to counteract to the noisy input so that the output signal is as tightly locked to the clean reference signal as possible. The loop's ability to force locking is only effective within the loop bandwidth. Once the frequency of noise exceeds the loop bandwidth, the loop has no effect on the injected signal since the system is simply not fast enough to react to the noise. Thus the VCO noise is effectively high-pass filtered.

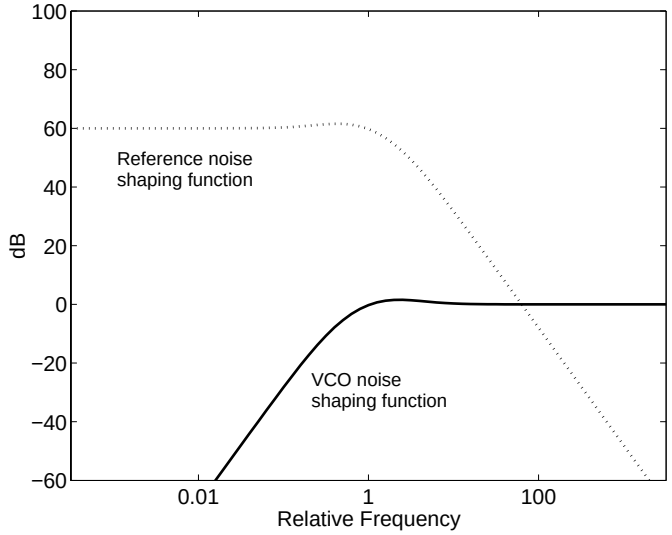


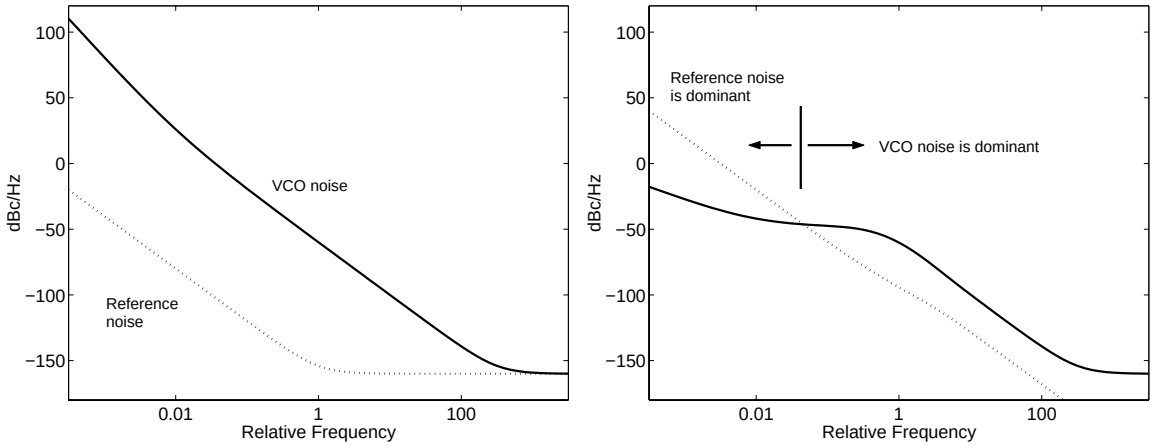
Fig. 23. Phase noise shaping functions

Examples of the phase noise transfer functions are shown in Fig. 23. The solid line is the high-pass characteristic of a VCO phase noise shaping function and the dotted line is a low-pass characteristic of a reference phase noise shaping function. The actual transfer functions are

$$H_{ni}(s) = \frac{1000(1+4s)}{1+4s+4s^2+s^3} \tag{3.35}$$

$$H_{nv}(s) = \frac{(4s^2+s^3)}{1+4s+4s^2+s^3} \tag{3.36}$$

We are summing a multiplication factor of $N = 1000$ in (3.35). Due to the multiplication factor, there is a 60 dB gain for the reference noise transfer function at low frequencies. It looks as if the contribution of the reference noise is much higher than that of the VCO noise, but the absolute value of the reference noise should be much smaller than the VCO noise.



(a) (b)

Fig. 24. Phase noise (a) Raw phase noise of reference and VCO (b) Phase noise contributions after being shaped in PLL

Examples of reference noise and VCO noise are shown in Fig. 24(a). The solid line is VCO phase noise, and the dotted line is reference phase noise. In this example,

the reference noise is many orders of magnitude smaller than the VCO noise. Note that the VCO phase noise has a steeper slope at low frequencies due to flicker noise contribution. Fig. 24(b) depicts the phase noises after the noise shaping function is applied. As expected, the reference phase noise is dominant at low frequencies, and the VCO phase noise is dominant at high frequencies.

Typically at low frequencies the synthesizer noise is dominated by reference noise and at high frequencies by VCO noise. Considering that interference and spurious emission are relatively far from the center frequency, the overall phase noise is predominated by the VCO since the PLL cannot reject the noise from VCO outside the loop bandwidth. Fractional-N architecture can increase loop bandwidth somewhat, but still it is not practical to widen the loop bandwidth enough to cover interference signals. Moreover, wide bandwidth loop filter has less attenuation for the noise from the reference oscillator as shown in the noise shaping function, Fig. 23. Thus there is a trade-off between the close-in phase noise and the loop bandwidth. The close-in phase noise is calculated only from the reference oscillator on the bases that the VCO noise is attenuated enough below the loop bandwidth. Usually the close-in phase noise has less impact than the VCO phase noise on the overall receiver performance.

2. Reference Spurs

Reference spurs are another undesirable signals besides phase noise that can negatively impact the performance of synthesizers. Spurious tones are the most difficult problem in synthesizer design since it is hard to predict them in the circuit simulation process. Only lab measurement can show real extent of spurious tones after the test chip is done, since most of the spurious tones are due to coupling from other building blocks of the whole system.

Reference spurs rise from the coupling of the input reference frequency to the

VCO control voltage. The reference frequency can couple through up/down pulse mismatch in PFD and charge injection mismatch in CP. There are other direct coupling paths such as die substrate and power supply rails as shown in Fig. 25.

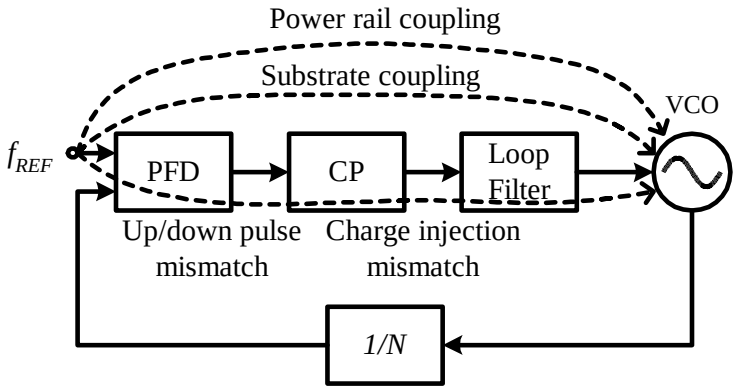


Fig. 25. Reference signal coupling paths

The coupled reference frequency affects the control voltage of the VCO. The phase of the VCO output signal is modulated by the periodic disturbance from the coupling. Fig. 26 depicts the modulation of the output signal. The mechanisms of reference spurs can be quantified as follows. The control voltage of the VCO has a DC component and a pulsed modulating component. The DC component can be ignored for simplicity in calculation of frequency modulation. Using Fourier series expansion, the control voltage is

$$V_c(t) = \sum_{i=1}^{n} a_i \cos(i\omega_m t) \tag{3.37}$$

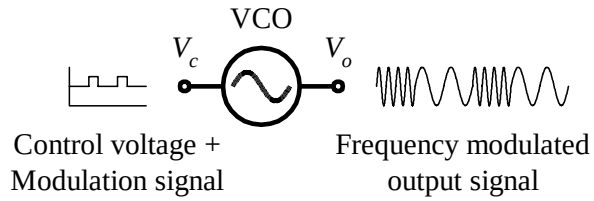


Fig. 26. VCO output is modulated by coupled reference signal

where ω_m is the radian frequency of the reference signal, $2\pi f_{REF}$. Since V_c determines the frequency of the VCO, the phase of the VCO is an integral of the instantaneous frequency. Thus the output of the VCO is

$$V_o(t) = V_A \cos(\omega_o t + K_o \int V_c(t)) \tag{3.38}$$

where V_A is an amplitude of the output signal, ω_o is a free running frequency, and K_o is the VCO gain. Substituting (3.37) into (3.38),

$$V_o(t) = V_A \cos(\omega_o t + K_o \int \sum_{i=1}^{n} a_i \cos(i\omega_m t)) \tag{3.39}$$

$$= V_A \cos(\omega_o t + K_o \sum_{i=1}^{n} \frac{a_i}{i\omega_m} \sin(i\omega_m t)) \tag{3.40}$$

Using the narrow band FM approximation,[1]

$$V_o(t) \simeq V_A \cos(\omega_o t) - V_A K_o \sum_{i=1}^{n} \frac{a_i}{i\omega_m} \sin(i\omega_m t) \sin(\omega_o t) \tag{3.41}$$

$$= V_A \cos(\omega_o t) + V_A K_o \sum_{i=1}^{n} \frac{a_i}{2i\omega_m} \big\{ \cos(\omega_o + i\omega_m)t - \cos(\omega_o - i\omega_m)t \big\} \tag{3.42}$$

(3.42) shows that there are spurious tones at the harmonics of the reference signal away from the carrier. The strongest spurs are the ones from the fundamental frequency of the reference signal, ω_m. The amplitude of the reference spurs relative to that of the carrier signal can be calculated as

$$A_{spur} = \frac{K_o a_i}{2i\omega_m} \tag{3.43}$$

[1] If $B \to 0$, $\cos B \simeq 1$ and $\sin B \simeq B$

$$\begin{aligned} \cos(A + B) &= \cos A \cos B - \sin A \sin B \\ &\simeq \cos A - B \sin A \end{aligned}$$

From the above equation, it is clear how the reference spurs can be reduced. For a given ω_m, K_o and a_i must be decreased in order to reduce A_{spur}. Reducing the VCO gain K_o is increasingly difficult as process technology scales down since the voltage headroom is getting smaller. There are several factors that influence the amplitude of the modulating signal (a_i). Apparently the coupling of the reference signal must be weakened to reduce a_i. That can be done by reducing up/down timing mismatch in PFD and reducing leakage current in CP. Substrate coupling can be alleviated by layout techniques such as multiple guard rings around critical path and separation of blocks by deep trench and careful placement. Once the precautionary measures have been done, the only factor that a designer have any control upon is the bandwidth of the loop filter. The lower the bandwidth, the smaller the amplitude a_i. Thus it is beneficial to have the loop bandwidth as low as possible within the limitation of settling time.

An interesting observation can be made on the behavior of the reference spurs when the carrier frequency is lowered by frequency division circuits. When the frequency division occurs, the phase of the VCO output in (3.38) is divided. Assuming divide-by-two operation, (3.38) becomes

$$V_o'(t) = V_A \cos\left(\frac{\omega_o t + K_o \int V_c(t)}{2}\right) \tag{3.44}$$

Following the same derivation, the final equation for the carrier signal plus spurs is

$$V_o'(t) = V_A \cos\left(\frac{\omega_o t}{2}\right) + \frac{V_A K_o}{2} \sum_{i=1}^{n} \frac{a_i}{2i\omega_m} \left\{ \cos(\frac{\omega_o}{2} + i\omega_m)t - \cos(\frac{\omega_o}{2} - i\omega_m)t \right\} \tag{3.45}$$

The result shows that while the carrier frequency is divided by two, the modulation frequency is not affected. Instead, the amplitude of the spurs is divided by two. The example of the effect of divide-by-two operation on spurs is depicted in Fig. 27. Although the spectrum seem to be compressed in frequency axis after division, the

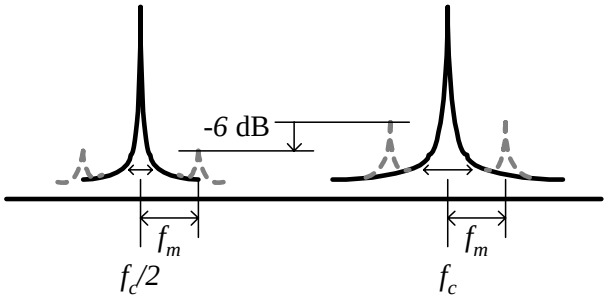


Fig. 27. The effect of frequency divide-by-two on reference spurs

offset frequency of the spurs remain unchanged. 6 dB improvement on the reference spurs rejection only comes from the reduced amplitude of the spurs.

E. Recent FS Design Techniques Progress

Even though frequency synthesizer theory is very mature, there is still a large research effort aimed to improve performance and optimize implementations for new technologies and emerging standards. One of the main drivers for research in frequency synthesizers has been the need to generate increasingly higher frequencies while decreasing power consumption. This section presents a brief review of recent advances in frequency synthesizer design.

1. Novel Architectures

The frequency synthesizer architecture is generally based on a phase-locked loop. Dual loop architectures [22, 23] have been presented trying to alleviate the trade-off between loop bandwidth and frequency steps in integer synthesizers. An area and power consumption penalty is paid for the relaxed trade-off. A nested architecture is proposed in [24] to obtain a wide-band PLL while maintaining fine frequency resolution and spurs rejection. A stabilization technique [25] introduces a zero in the open-loop transfer function through the use of a discrete-time delay cell and relaxes

the trade-off between the settling speed and the magnitude of output sidebands.

2. Linearization Techniques

In an effort to reduce spurious tones, [26] uses charge pump averaging and reduces the magnitude of the fractional spurs to levels below the noise floor. [27] introduces a phase noise cancellation and charge pump linearization technique performed by a DAC driven by a mismatch shaping DAC controlled by a modulator which compensates quantization errors introduced by the loop modulator. Another option for charge pump linearization is to add a replica charge pump and a bias controller to compensate the current mismatch in the charge pump [28]. This technique allowed a reduction of 8.6 dB of the spurious tones.

3. Digital Phase-Locked Loop

With the improvement of digital CMOS processes, there has been an increased interest in all-digital RF frequency synthesizers [29–31]. One of the main advantages of all-digital frequency synthesizers is the elimination of the PFD - charge pump non linearity, the easy integration in modern technologies and a reduced dependence on process variations. [29] presents a digital PLL with a DAC to control the VCO voltage and a digital phase-frequency detector (DPFD) accompanied by an adaptive loop control that helps to obtain fast acquisition. This frequency synthesizer is mainly oriented to clock generation.

4. Fast Settling Techniques

Fast settling techniques try to relax the trade-off between settling time and loop bandwidth by providing additional means to speed the frequency switching process. In [32], a switchable-capacitor array that tunes the output frequency, and a dual loop

filter operating in the capacitance domain are proposed. A settling time smaller than 100 μs is obtained. A locking time as short as 30 μs is reported in [33] which uses a discrete-time loop filter with a stabilization zero created in the discrete-time. A different technique is used by [34] where 64 identical charge pumps are enabled and the loop resistor is reduced by 8x, effectively increasing the loop bandwidth by 8x only during the switching of the synthesizer. A settling time of 10 μs is reported.

5. VCO

RF oscillator design is challenging due to the uncertainty in the modelling of its passive devices. Hence, it is the building block that has received more attention in the last few years. [35] reports a phase noise of -139 dBc/Hz at 3 MHz offset using a low inductor quality factor (Q) of 6 for an oscillation frequency of 1.8 GHz in a noise shifting differential Colpitts VCO that uses current switching to reduce the phase noise. [36] achieves -139 dBc/Hz at 3 MHz offset at 1.7 GHz by adding a voltage regulator to the VCO and thus reducing its sensitivity to the supply noise. A 36 GHz VCO is presented in [37], 60 GHz and 100 GHz VCOs in 90 nm technology are presented in [38] and a 63 GHz VCO in standard 0.25 μm CMOS technology in [39]. Circular-geometry oscillators based in slab inductors are presented in [40] and a circular standing wave oscillator in [41]. A stable fine-tuning loop is combined with an unstable coarse-tuning loop in parallel, and as a result, a stable PLL with a relatively wide tuning range of 600 MHz for a 4.3 GHz oscillator is obtained in [42], [43] shows a 20 GHz VCO with 25% tuning range achieved through the small parasitic capacitance of a negative-resistance cell. [44] utilizes a single loop horseshoe inductor with a quality factor larger than 20 and an accumulation MOS varactor with Cmax/Cmin ratio of 6 to provide a 58.7% tuning range between 3 and 5.6 GHz. Finally, [45] introduces the first digitally controlled oscillator (DCO) incorporating dithering to increase the

frequency resolution of the DCO.

6. Quadrature Generation

Quadrature generation is an important part of the signal processing in an RF front-end. Most of the modern communication standards use phase or frequency modulation schemes, which require quadrature mixing to extract the information contained in both sides of the spectra [6].

The most widely used technique involves the use of passive polyphase networks conformed of integrated resistors and capacitors. To improve the accuracy of the 90 phase shift, the order of the phase shift network has to be increased to spread the absolute value of the passive components. Phase errors as low as 3 can be obtained due to process variations of the passive elements [46–48]. A drawback of this technique is that the higher the order of the polyphase network, the larger the insertion loss of the LO signal – 3 dB of attenuation per stage. Another common technique for quadrature signal generation is the use of a VCO signal generated at twice the desired LO frequency. This technique provides a broadband range of quadrature outputs, but increases the power consumption by 20 to 30% due to higher operating frequencies. The accuracy of the phase generation is limited by the matching of the flip-flops in the frequency divider and the duty cycle error of the VCO output [49].

Calibration techniques are also found in the literature; they measure the phase imbalance of the quadrature outputs and compensate it. In [50], a delay locked loop (DLL) is used to adjust the phase error in a quadrature generator. A phase detector controls the current in the phase shifter and adjusts the phase different between two split paths. The circuit proposed in [51, 52] changes the duty cycle of the clock signal to compensate for the phase imbalance at the output of the divide-by-two circuit by adding a DC level component to the flip-flop clock. A self-calibration loop tunes each

branch of the phase shifter sequentially to average the phase error generated due to mismatches in the passive components [53].

7. Prescaler

Being one of the most power hungry blocks in the synthesizer, along with the VCO, a lot of effort has been placed into reducing its power consumption. [54] uses dynamic-logic frequency dividers based on true-single-phase-clock (TSPC) latches optimized for low power and high speed operation. Exploiting dynamic loading, [55] achieves a 1 V 2.5 mW divide-by-two flip-flop operating up to 5.2 GHz in 0.35 μm CMOS technology. A very low power divider is presented in [56], based in a quasi-differential locking divider operating up to 4.3 GHz while consuming 44 μW from a 0.7 V power supply in a 0.35 μm CMOS process. Another approach to improve power consumption is to use the injection-locked oscillator as a frequency divider. [57] shows that the injection-locked frequency divider can provide a high speed divide-by-two circuit with substantially lower power consumption than its digital counterparts.

As can be seen from the previous list of highlighted papers, there are open problems in almost every major building block of the frequency synthesizer. In particular, new architectures that allow to relax the bandwidth and settling time trade-offs, and optimization of VCO performance, along with power efficient frequency dividers, are areas for research focus.

F. Conclusion

A description of frequency synthesizers that emphasizes the key design parameters and specifications for their use in wireless applications has been presented. The mapping between the communication standard into particular specifications has been

highlighted for parameters such as phase noise, settling time, and spurious rejection. A discussion on stability limits has been presented to establish the limits on the ratio of loop bandwidth with respect to the reference frequency and the relative location of the poles, zero and crossover frequency. The main design trade-offs between noise, bandwidth and stability have been described, as well as the implications on settling time and stability of the relative location of the pole and zero on the transfer function. A brief survey of the latest advances on the design of frequency synthesizers helps to identify the areas where most of the design effort needs to be put to improve the performance of the circuit.

CHAPTER IV

VOLTAGE CONTROLLED OSCILLATOR DESIGN

A. Introduction

The Voltage Controlled Oscillator (VCO) in wireless communication transceivers plays the role as a local oscillator of the mixer for downconverting the received RF signal to low intermediate frequency (IF). As the name implies, a VCO should produce a periodic output signal with its frequency controlled by an input voltage signal. Typically a VCO must be accompanied by a feedback control system to stabilize its output frequency. A stand-alone VCO is exposed to strong disturbances from power supply and couplings through die substrate. The frequency of a VCO is most vulnerable to the external disturbances due to its high sensitivity to input control voltage.

The design process of RF VCO is unique among analog circuits because it involves detailed design of passive elements such as inductors and capacitors. It also shares a common problem of any high frequency analog circuits; while the overall circuit topology is not so complicated, each component must be carefully modelled, simulated, and laid out since they are highly sensitive to parasitic elements and process variations.

In this chapter, two VCO design examples for two different specifications are presented. The first example is a VCO designed for a Bluetooth transceiver using 0.35 μm CMOS process. The second example is a VCO designed for a multi-standard Wireless LAN 802.11a and 802.11b receiver using 0.25 μm SiGe BiCMOS process. We focus on these specific examples rather than general issues of VCO design in order to emphasize practical aspects of the design process.

Table VIII. VCO specifications

	Bluetooth	Multi-standard
Tuning range	2160–2728 MHz	4340–6386 Mbps
Tuning sensitivity	150 MHz/V	350 MHz/V
Phase noise	−124 dBc/Hz at 3 MHz offset	−126 dBc/Hz at 40 MHz offset
I/Q Magnitude mismatch	5%	5%
I/Q Phase mismatch	15°	10°

B. Specifications Study

The circuit specifications for Bluetooth and multi-standard VCO are summarized in Table VIII. Details of the derivation of specifications from the standards are discussed in Chapter II.

The tuning range specifications have 10% margin added to the target frequency band. The tuning sensitivity specifications are more like a limitation on maximum value it can take rather than target value. It is always desirable to have the tuning sensitivity as low as possible because it reduces noise susceptibility of VCO. For example, a tuning sensitivity of 150 MHz/V results in 150 kHz of frequency perturbation in VCO output when control voltage has 1 mV variation. In Table VIII, multi-standard VCO is allowed to have larger tuning sensitivity since the BiCMOS technology that the system is built with offers better options for noise isolation. In addition, it actually need higher tuning sensitivity because of wider tuning range. While lower tuning sensitivity is desirable, it should be large enough to cover the tuning range with given voltage headroom. For Bluetooth VCO, the required voltage headroom to meet the

tuning range specification is,

$$\Delta V_{BT} = \frac{2479 - 2400}{150} = 0.53 \text{ V} \tag{4.1}$$

Note that we are considering only the frequency band required without added margin. In order to cover the extended tuning range, a much wider voltage headroom is required. The new voltage headroom is,

$$\Delta V_{BText} = \frac{2728 - 2160}{150} = 3.79 \text{ V} \tag{4.2}$$

V_{BText}, in fact, exceeds the maximum voltage limit of the given 0.35 μm CMOS process. Unless the tuning sensitivity is substantially increased, it is impossible to build a VCO that has full coverage of the extended tuning range. In order to solve this problem, we introduce a secondary tuning mechanism, usually a bank of capacitors programmable digitally. The secondary tuning adjusts the main tuning range close to the standard requirement in case of process variation. Once adjusted, only the main tuning is required to cover the required frequency range as long as the ΔV_{BT} is within the voltage limit. Detailed discussion of the secondary tuning mechanism is given later in section IV-4.

C. Circuit Topology

Among many different topologies of VCO implementations, the most popular choice for high frequency narrow-band transceiver is LC-tuned negative-resistance oscillator. LC-tuned oscillator has several important advantages over other oscillator topologies that make it more suitable for RF communication applications.

1. The frequency of operation is in GHz range, which can be too high for relaxation type oscillators. Ring oscillators can produce GHz output without problem.

Table IX. Ring oscillator applications

Application	Frequency	Year	Reference
Multi-phase clock	622 MHz	1997	[59]
Frequency synthesizer	2.4 GHz	2004	[60]
Clock recovery	10 GHz	2002	[61]

2. Since LC tank works as a tuned resonator, LC-tuned oscillators generally have better phase noise performance than any other topologies for a given power consumption. Ring oscillators can achieve a good phase noise performance [58], but with higher power consumption. To meet the phase noise requirement without consuming too much power, LC-tuned oscillator is better choice.

3. The required tuning range is relatively narrow compared to the carrier frequency. They are 3.3%, 2.5%, and 11.4% for Bluetooth, 802.11b, and 802.11a standards respectively. Narrow tuning range is essential to be able to use CMOS varactors in the LC tank.

The well-known terrible phase noise performance of ring oscillators comes from several factors. First, the resonator Q of a ring oscillator is poor; in fact, it is unity, since the energy stored in the node capacitance is discharged every cycle. Next, energy is restored to the resonator during the edges, rather than the voltage maxima. The effect of noise from the driver is maximum during the edges, so this degrades the phase noise performance of ring oscillators. As a consequence, ring oscillators are found only in the applications where the phase noise performance is noncritical, or inside wideband PLLs that can clean up the spectrum.

The state-of-art design examples of ring oscillators are summarized in Table IX. The first example utilizes 9-stage ring oscillator to produce 9 different phase outputs.

Multi-phase output is something that LC-tuned oscillator cannot produce easily. The second example utilizes a high frequency ring oscillator in 2.4 GHz frequency synthesizer. The synthesizer has two cascaded PLLs, one of which is a fractional-N type that has a wideband loop filter that has high rejection of phase noise. This implementation has large die are overhead due to multiple PLLs. The third example utilizes a two-stage ring oscillator at 10 GHz for clock recovery application. The phase noise requirement is −94 dBc/Hz at 2 MHz, which is much more relaxed than that of typical RF applications. For comparison, the Bluetooth standard specifies −124 dBc/Hz at 3 MHz, which is 30 dB higher requirement.

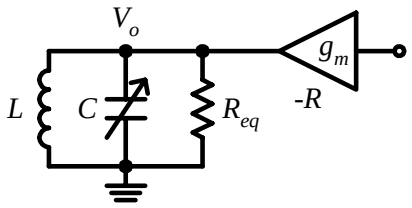


Fig. 28. LC-tuned oscillator concept

A conceptual schematic of a LC-tuned VCO is shown in Fig. 28. R_{eq} represents a total equivalent loss from the inductor, the capacitor, and the transistors. Without R_{eq}, the oscillation at V_o node can be sustained ideally with no power consumption. In reality, a transconductance g_m of the driver compensates the loss of R_{eq}, so that the oscillation can be sustained. The frequency of oscillation is tuned by resonance frequency of the LC tank,

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{4.3}$$

A variable capacitor, or a varactor, can change its capacitance relative to the voltage potential between its two nodes. Thus the center frequency of the VCO is controlled

by a voltage input to the varactor.

$$\omega_o(V) = \frac{1}{\sqrt{LC(V)}} \tag{4.4}$$

Various implementations of the LC-tuned oscillator are shown in Fig. 29. While all the examples have an LC tank in common, the driver can be any cross-coupled pair of NMOS, PMOS, both NMOS and PMOS, or bipolar transistors. Since NMOS pair can provide higher g_m than PMOS pair with same amount of current, using NMOS pair driver is a better choice for power conservation. However, using PMOS pair has an advantage of lower noise because the tail current source can attenuate the voltage ripples on the power supply rail. By using both NMOS and PMOS pair drivers, the benefits of both high g_m and noise blocking can be achieved. Disadvantage of the complementary pair drivers is that the swing of the output signal is limited due to the voltage headroom limitation. Limited swing results in smaller output signal amplitude. Depending on the available supply voltage, the complementary pair driver topology can be more detrimental than beneficial.

As discussed in the previous section, one of the critical concerns for the LC-tuned oscillator is the tuning range. Although the tuning range of the normal operation is relatively small, process variation can alter the whole range of the frequency tuning of the VCO. It is required to have some sort of secondary tuning to compensate the process variation.

The most challenging part of designing LC-tuned oscillator in a fully-integrated implementation is the need of on-chip inductors. What makes it challenging is that a typical implementation of an on-chip inductor has a very high loss, since the quality factor (Q) of reasonably sized on-chip inductors is very low – less than 10 usually. High g_m is required to compensate the loss for sustained oscillation. High g_m and low Q both lead to poor phase noise performance. Secondly, since the quality factor

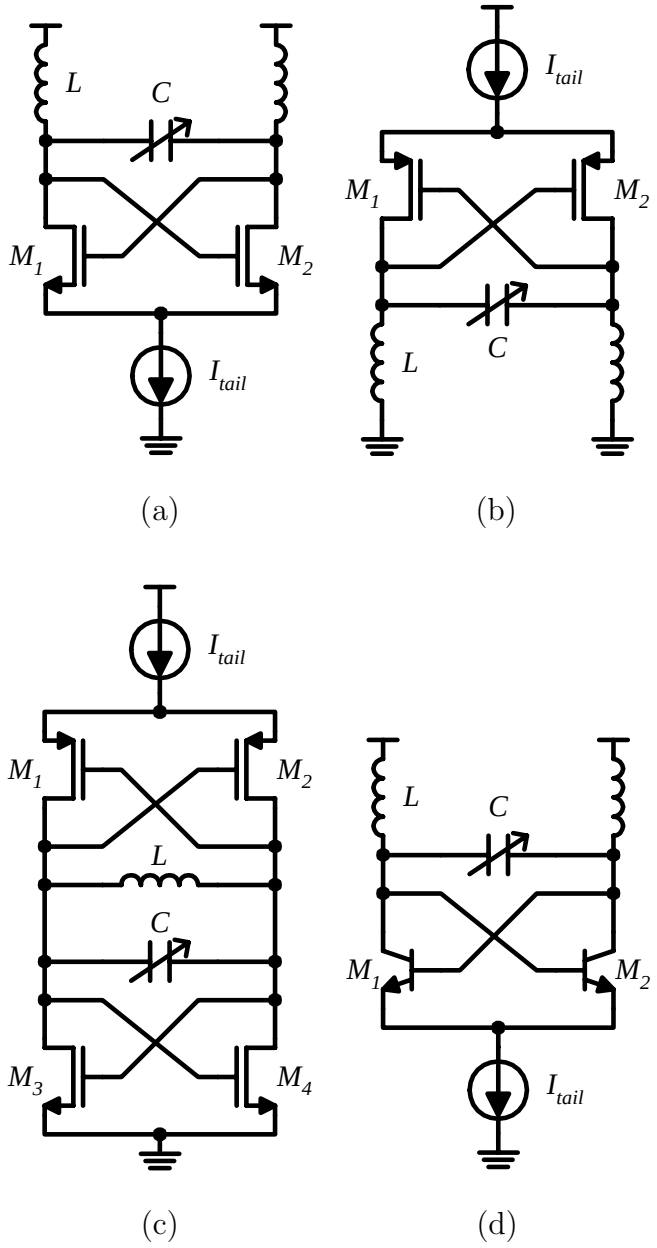


Fig. 29. Examples of LC-tuned VCO's. (a) NMOS pair driver (b) PMOS pair driver (c) NMOS+PMOS complementary pair drivers (d) Bipolar driver

is directly proportional to the size of the inductor, a good quality on-chip inductor takes large area on the die. Typically more than 50% of the area of a VCO is the on-chip inductor.

Another problem with LC-tuned oscillator is that it does not have quadrature output inherently as is the case with the ring or relaxation oscillators. It is required to have an extra I/Q generator from the output of the LC-tuned oscillator. Although the polyphase network is commonly used to do the I/Q generations, since it is made of passive components such as resistors and capacitors, it is prone to process variations. Extra caution is required during layout of this passive polyphase network to prevent large magnitude/phase mismatches.

D. Design Trade-offs

Apparently from Fig. 29, there are only a few variables involved in a VCO design. Initially, all the parameters that a designer need to decide on are the inductance (L), the capacitance (C), the bias current (I_{tail}), and the size of the driver transistors. However, all the parameters are closely related to the performance of the VCO and often they trade-off each other for a common factor [62, 63]. The following sections identify most of the important trade-offs of VCO design parameters to provide clear guidelines for the initial design of a VCO.

1. Power-Noise Trade-off

The first trade-off in VCO design we investigate is the one between power consumption and phase noise. It is intuitive to estimate that the higher the power consumption, the lower the phase noise. For example, if we assume there were two identical oscillators with equal phase noise, and if the outputs of the two oscillators would be summed

into a single output, the output signal power would be doubled while the output noise power would be only grown by $\sqrt{2}$ since they are random processes. Thus the phase noise would be decreased by $\sqrt{2}$ while consuming twice the power. More analytic observation can lead to an important design guideline regarding the inductance and the bias current.

The first equation that is needed to calculate power-noise trade-off is the signal power of the oscillator output. Since the tank is considered as a passive block, the amplitude of the output signal V_{signal} linearly grows with the bias current until it hits the supply voltage or MOS transistors enter triode region. The bias current is converted into voltage by the equivalent resistance of the tank R_{eq} in Fig. 28. Since the quality factor of the inductor is the lowest, we can assume the R_{eq} is dominated by the parallel resistance of the inductor R_p.[1] So the signal power can be expressed as,

$$V_{signal}^2 = \begin{cases} I_{tail}^2 R_p^2 = I_{tail}^2 (\omega_o L)^4 / R_s^2 & \text{, when drivers are active} \\ V_{limit}^2 & \text{, when drivers are non-active} \end{cases} \tag{4.5}$$

The next equation needed is the noise power of the output. In Fig. 28, the noise current from the active devices enters the tank circuit and shaped by the impedance of the tank. It can be shown that the power density of the output noise is [6],

$$v_n^2 = 4kT\gamma g_m \frac{R_p^2}{4Q_L^2} \Big(\frac{\omega_o}{\Delta\omega}\Big)^2 \tag{4.6}$$

$$= kT\gamma g_m (\omega_o L)^4 \Big(\frac{\omega_o}{\Delta\omega}\Big)^2 \tag{4.7}$$

which shows the output noise power is proportional to the inductance for a given

[1]Series-parallel conversion of a lossy inductor is valid only close to the resonant frequency. It can be shown that $R_p = Q_L^2 R_s$, where R_s is a series resistance and Q_L is a quality factor of the inductor, defined as $Q_L = \omega_o L / R_s$

oscillation frequency.

The phase noise is a relative power of output noise with respect to the signal power. Thus it is calculated from (4.7) divided by (4.5). The phase noise equation is,

$$PN = \frac{V_{signal}^2}{v_n^2} = \begin{cases} \frac{kT\gamma g_m}{I_{tail}^2 Q_L^2}\left(\frac{\omega_o}{\Delta\omega}\right)^2 & \text{, when drivers are active} \\ \frac{kT\gamma g_m(\omega_o L)^4}{V_{limit}^2}\left(\frac{\omega_o}{\Delta\omega}\right)^2 & \text{, when drivers are non-active} \end{cases} \tag{4.8}$$

From equation (4.8), the phase noise can be decreased either by increasing I_{tail} (consuming more power) or by increasing the quality factor of the inductor Q_L. Q_L can be increased by having larger inductance L or smaller series resistance R_s since $Q_L = \omega_o L/R_s$.

From this observation, it is clear that the bias current I_{tail} should be as large as possible to reduce the phase noise. However, the phase noise cannot be indefinitely small since the amplitude of the signal has a limit of V_{limit} due to saturation of the drivers. Once the limit is reached, increasing I_{tail} has no effect on the phase noise performance.

Usually the power consumption requirement of any wireless system is very stringent. So it is safe to say that we should use maximum power available for VCO to increase the amplitude of the oscillation and reduce phase noise.

- Rule #1 : Increase I_{tail} until the drivers saturate for a better phase noise performance.

2. Inductance-Noise Trade-off

Since there is no other amplitude limiting mechanism in the LC-tuned VCO shown in Fig. 29, the drivers eventually saturate if I_{tail} is increased too much. Once the drivers are not active, the phase noise is directly proportional to the inductance from (2.17).

Therefore the inductance should be decreased for better phase noise performance in saturation.

Decreasing inductance has negative effect on the signal amplitude. From equation (4.5), I_{tail} should be increased to compensate for the loss and keep the amplitude unchanged.

- Rule #2 : Use minimum L that satisfies the signal amplitude requirement to minimize phase noise in saturation.

3. Inductance-Tuning Range Trade-off

The oscillation frequency is determined by the varying capacitance value. If the maximum and the minimum capacitance is given, the tuning range can be calculated from (4.3). The maximum frequency is obtained when the capacitance is the smallest,

$$\omega_{max} = \frac{1}{\sqrt{LC_{min}}} \tag{4.9}$$

And the frequency is minimum when the capacitance is the largest,

$$\omega_{min} = \frac{1}{\sqrt{LC_{max}}} \tag{4.10}$$

Since the tuning range is the difference between the maximum frequency and the minimum frequency,

$$\Delta\omega = \omega_{max} - \omega_{min} = \frac{1}{\sqrt{L}}\left(\frac{1}{\sqrt{C_{min}}} - \frac{1}{\sqrt{C_{max}}}\right) \tag{4.11}$$

This shows that the tuning range is inversely proportional to the absolute value of the inductance. However, the inductance cannot be just decreased to increase the tuning range since decreased inductance also shifts the frequency band to higher frequency. The capacitance has to be increased to maintain the frequency band. Since it is easier

Table X. VCO design procedure

Step	Parameter	Action
1	L	Use an arbitrary small value L
2	I_{tail}	Increase I_{tail} until amplitude is maximum.
3	$Power$	Check if power dissipation is within limit. If not, decrease I_{tail} and increase L. If it is, increase I_{tail} and decrease L. Repeat until L is minimized.
4	PN	Check if phase noise requirement is met. If not, increase Q of the inductor. Repeat until PN meets the specification.

to make a varactor with large capacitance variation when the mean capacitance is large, reducing inductance helps to increase tuning range eventually.

- Rule #3 : Use minimum L to maximize tuning range width.

Using the three design rules described so far, a simple design procedure is suggested in Table X. Finding optimal design values is an iterative process. There are various points where the previous steps need to be repeated and the design values revised. Detailed design examples of real VCO design are given in the following sections.

E. Bluetooth CMOS VCO Design Details

The schematic of a CMOS VCO for Bluetooth standard is shown in Fig. 30. The building blocks of the circuit can be identified as; current mirror to provide tail

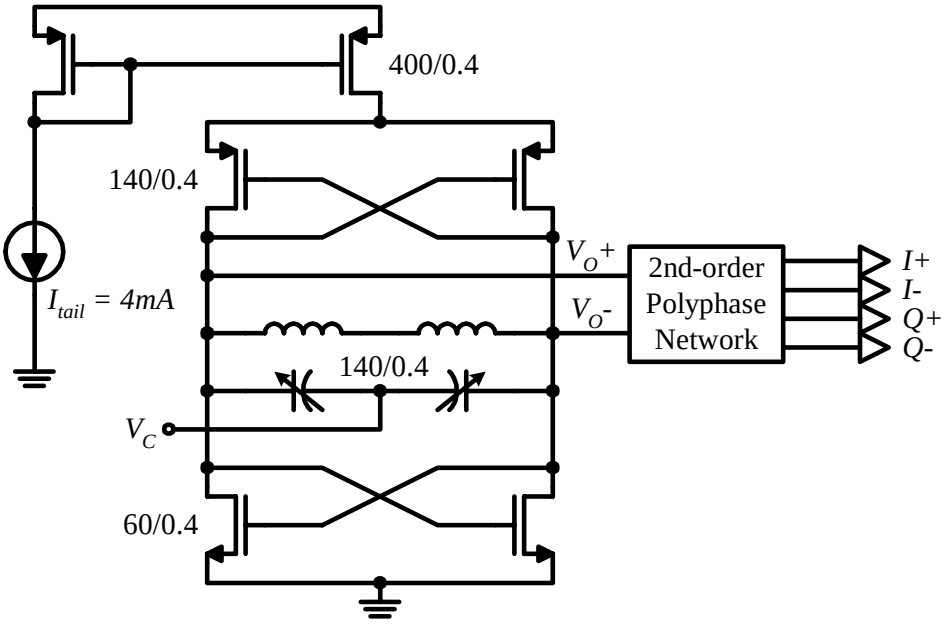


Fig. 30. Schematic of a CMOS Bluetooth VCO

current bias, NMOS and PMOS pairs to drive the oscillation, LC tank for tuning the frequency, I/Q generator (polyphase network) and buffers.

The following procedure shows how each design variable is calculated. It deviates from the procedure described in Table X a little bit because the power consumption is too limited. Instead of starting from inductance value, the following procedure begins with a fixed bias current.

1. Bias Current

Due to the power consumption constraint, the bias current for the VCO is set at the maximum of 4 mA.

$$I_{tail} = 4 \text{ mA} \tag{4.12}$$

2. Inductor in Standard CMOS Process

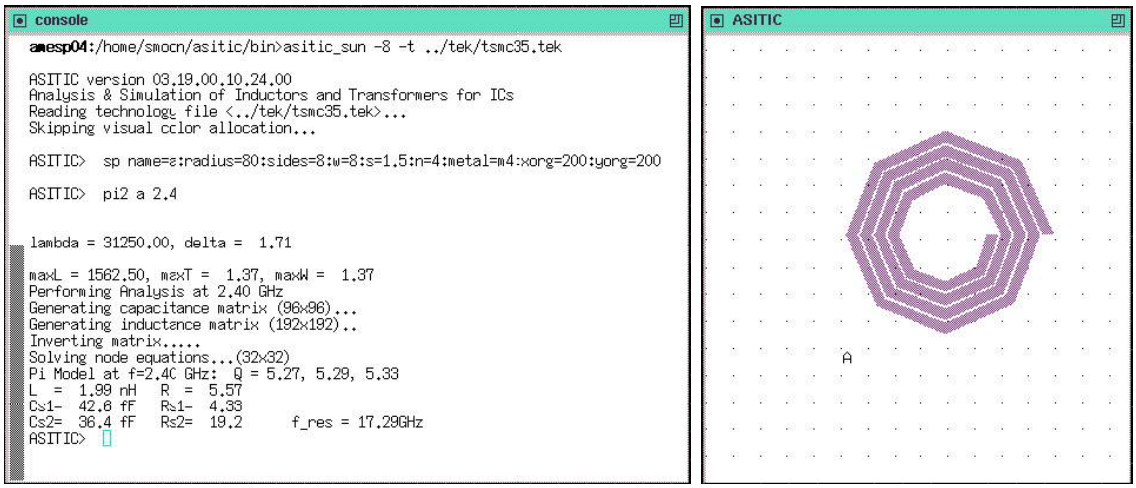
Traditionally, an inductor is something that should be avoided in analog circuit design because it is impossible to be integrated in an IC mainly due to the size. However, as the frequency of operation is getting higher and higher, it became viable to use an inductor in the design of a RF analog circuitry since the size of the inductor is inversely proportional to the frequency of operation.

Calculating the inductance and other parasitic elements of an on-chip spiral inductor is not a simple matter. Sophisticated Electro-Magnetic (EM) simulation is required for accurate calculation. But a simplified equation can provide valuable intuition for the initial design process. An empirical formula that has reasonable accuracy for a square shaped spiral is given in [64],

$$L \simeq 1.3 \times 10^{-7} \frac{A_m^{5/3}}{A_{tot}^{1/6} W^{1.75} (W+G)^{0.25}} \tag{4.13}$$

where A_m is the metal area, A_{tot} is the total inductor area, W is the track width, and G is the track spacing. It is clear that in order to maximize the inductance, W and G should be minimized while using the maximum metal area A_m from the given total inductor area A_{tot}.

Another important parameter of an inductor design is quality factor. For a given inductance, the quality factor is roughly proportional to the track width W since the series resistance contributes the loss of an inductor the most. Once the track width is increased larger than the skin depth for the operating frequency, series resistance does not decrease anymore. Increasing the track width further will degrade the quality factor due to substrate loss. We can summarize a set of rules for design of a on-chip spiral inductor.



(a) (b)

Fig. 31. ASITIC usage example. (a) Command window (b) Spiral inductor for Bluetooth VCO.

1. Increase the track width for better Q.

2. Limit the track width below the skin depth.

3. To keep the inductance unchanged, the total area has to be increased proportionally.

4. If the total area is too large, the substrate loss become significant and Q does not improve anymore.

5. Limit the total area to keep the self-resonance frequency is well above the operating frequency.

6. Use hollow-centered coil to improve Q by reducing the loss due to the Eddy current.

Actual design of the inductor is done by using ASITIC inductor modelling CAD

Table XI. Spiral inductor parameters for Bluetooth VCO

Radius	80 μm
Metal width	8 μm
Metal spacing	1.5 μm
Number of turns	4
Inductance L	1.99 nH
Quality factor Q	5.27
Series resistance R_s	5.57 Ω
Self-resonant frequency f_{res}	17.29 GHz

tool.[2] By using ASITIC, we can design, analyze, and model the electrical and magnetic behavior of any passive metal structures residing above a lossy conductive substrate. Fig. 31(a) shows an example of ASITIC command window. Fig. 31(b) shows the spiral structure generated by ASITIC for Bluetooth VCO. The spiral inductor for the Bluetooth VCO has the parameters given in Table XI.

The most serious challenge in making a spiral on-chip inductor for the target Bluetooth transceiver is that only very limited area is allowed for the VCO. After an intensive optimization and iterative simulations, we could design an inductor with Q of 5.27 and self-resonant frequency f_{res} of 17.2 GHz and inductance L of 1.99 nH using the maximum die area allowed, which is 200 μm $\times$ 200 μm. Relatively high f_{res} suggests that it is possible to increase the overall size of the inductor for a better quality factor. The lumped-element model of the inductor is shown in Fig. 32. Note that this model is only valid at a single frequency, 2.4 GHz in this case.

Now we need to verify if the designed inductor meets the amplitude requirement

[2]ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for ICs) is developed by Ali M. Niknejad from U. C. Berkley.

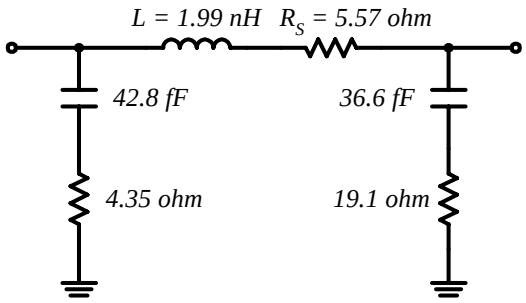


Fig. 32. On-chip spiral inductor model

for our application. We can calculate the output amplitude from equation (4.5).

$$V_{signal} = I_{tail} R_p = I_{tail} Q_L^2 R_s \tag{4.14}$$

$$= 4 \text{ mA} \times 5.27^2 \times 5.57 \ \Omega \tag{4.15}$$

$$\simeq 0.619 \text{ V} \tag{4.16}$$

Since V_{signal} is a peak-to-peak amplitude of one side of a differential signal, the power of the final single ended signal is approximately 6 dBm.[3] The front-end mixer that follows the VCO dictates the output signal amplitude requirement. The requirement for Bluetooth transceiver is 0 dBm. A margin of 6 dB is reserved for non-ideal losses from other sources. The assumption that we have agreed for the calculation is that the loss of the inductor is dominant, which is not entirely true since other sources such as the non-ideality of the varactor and the output resistance of the transistors are present.

[3]dBm is a measure of power of a signal with respect to 1 mW reference. It also assumes a 50 Ω load. $dBm = 10 \log\{V_{rms}^2/(50 \ \Omega \times 1 \text{ mW})\}$

3. CMOS Varactor

In VCO design, it is required to have a varactor[4] to set the resonant frequency of the tank circuit according to the desired output frequency. Traditionally in bipolar process, a diode can be used as a voltage-controlled variable capacitor since the junction capacitance is a function of the voltage applied across itself. However, in CMOS process, there is no well controlled PN junction available unlike bipolar process. So varactors in CMOS process depend on the capacitance between the gate and the channel or the bulk. The gate capacitance is well controlled during fabrication process and we can get reasonably high capacitance density due to the thin oxide layer as a dielectric material.

The behavior of capacitance variation between gate and bulk nodes changes depending on the operation mode of the transistor as following [65].

1. Accumulation mode

   Fig. 33 shows accumulated electrons on the surface beneath the gate area form a conducting plate. The capacitance between the gate and the bulk is the same as the oxide capacitance C_{OX}.

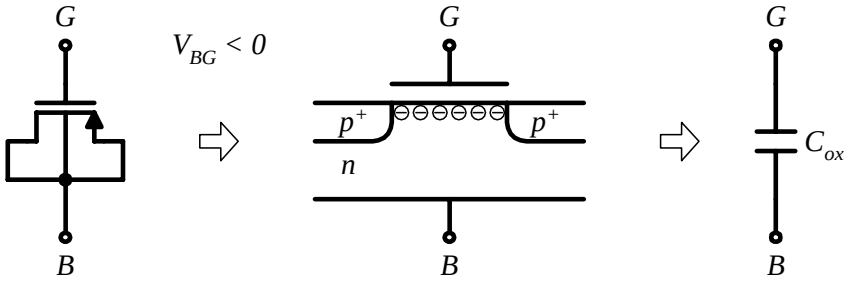


Fig. 33. Accumulation mode capacitance

[4]The name comes from a variable reactor.

2. Depletion mode

   Fig. 34 shows depletion region pushes the electrons away from the surface and the total capacitance become a serial combination of the oxide capacitance C_{OX} and the depletion capacitance C_d. Usually C_d is smaller than C_{OX}, in turn, result in smaller capacitance in total.

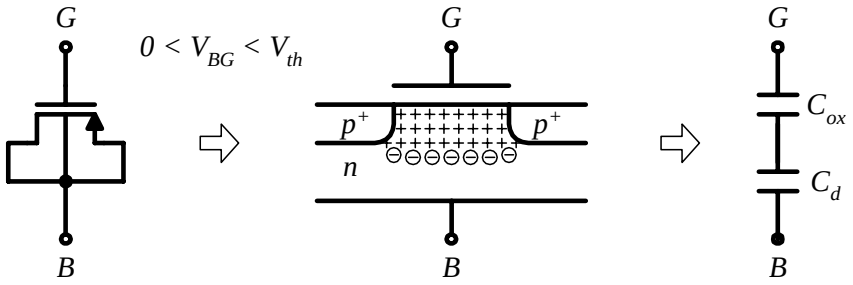


Fig. 34. Depletion mode capacitance

3. Inversion mode

   As shown in Fig. 35, once the gate voltage pass the threshold voltage, the holes injected from the drain and the source area begin to form an inversion layer underneath the gate area. Therefore, the total capacitance is again equal to the oxide capacitance C_{OX}.

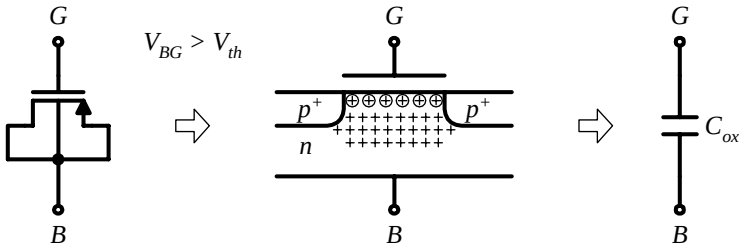
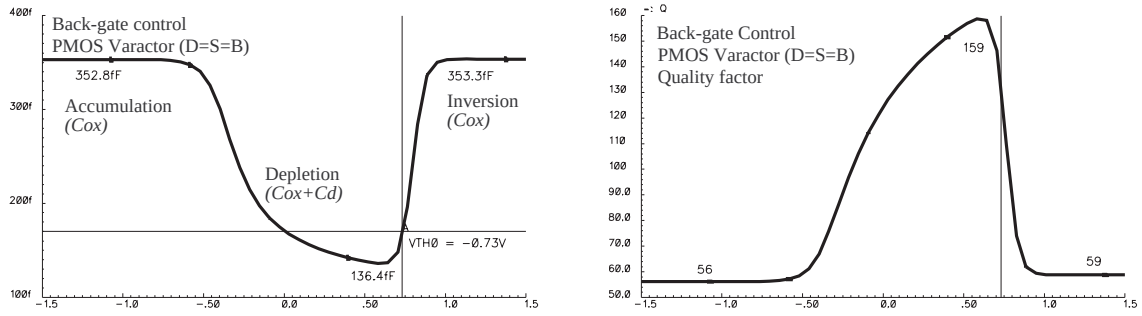


Fig. 35. Inversion mode capacitance

From the discussion above, it is clear that the variation of the capacitance is not linear in MOS transistor. In fact, the slope of the capacitance goes up and down



(a) (b)

Fig. 36. CMOS varactor capacitance variation. (a) capacitance (b) quality factor

as shown in Fig. 36. In other words, the capacitance variation is not linear and non-monotonic.

This non-monotonic nature of the MOS varactor raises a serious problem when controlling the capacitance in a feedback loop. If the sign of the slope of the capacitance is changed from the normal operation point, the feedback becomes feedforward and the loop would lose control and saturate. Moreover, the point of the slope reverse is depend on the threshold voltage of the transistor, which has large process variation during the fabrication. To solve this problem, two alternatives are provided.

1. Accumulation/Depletion mode CMOS varactor

   Shown in Fig. 37, this varactor is a non-standard device that has n^+ in the drain and source region of a transistor instead of p^+. Since there is no p-type semiconductor to provide the hole in this device, the inversion cannot be formed even after the threshold voltage.

   Generally the accumulation/depletion mode varactor is considered to have better quality as a varactor compared to the inversion mode ones. However, since this device is non-standard, exclusive modelling is required to characterize the accurate operation of the device. Even worse, it may not be permitted to be

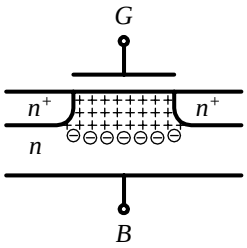


Fig. 37. Accumulation/Depletion mode CMOS varactor

processed at all.

2. Inversion mode CMOS varactor

   As shown in Fig. 38, the bulk of the inversion mode varactor is connected to the highest voltage available. In this case, V_{BG} cannot go below zero and no accumulation is possible.

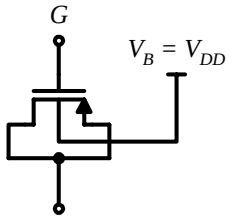
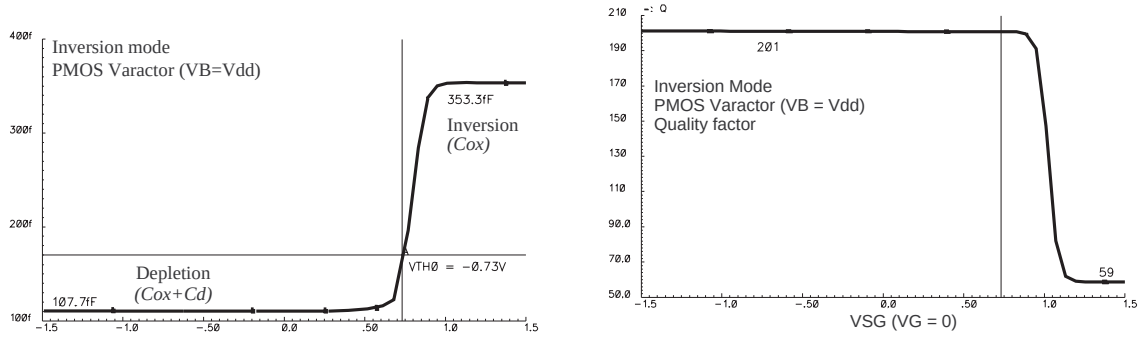


Fig. 38. Inversion mode MOS varactor

   Compare Fig. 36 with Fig. 39 and note that the capacitance of the inversion mode varactor is monotonically increasing.

   Although the inversion mode varactor has poor quality compared to the accumulation/depletion varactor, it is a popular choice since it is a standard PMOS device and the model is readily available.

Now, we are going to calculate how much capacitance is required to meet the frequency tuning range specification, regardless what type of varactor is being used. Once the inductance L is decided, it is a simple matter to calculate the capacitance



(a) (b)

Fig. 39. Capacitance variation of the inversion mode CMOS varactor. (a) capacitance (b) quality factor

C since the frequency of oscillation f_o is the resonant frequency of the tank. To make the resonant frequency 2.4 GHz with L of 1.99 nH,

$$C_{tank} = \frac{1}{\omega_o^2 L} = \frac{1}{(2\pi \times 2.4 \text{ GHz})^2 \times 1.99 \text{ nH}} \tag{4.17}$$

$$= 2.21\text{pF} \tag{4.18}$$

Note that this capacitance is the total capacitance of the tank, not the capacitance of the varactor alone. The tank capacitance can be expressed as

$$C_{tank} = C_v + C_L + C_{CMOS} + C_{load} \tag{4.19}$$

where C_v is the capacitance of the varactor, C_{MOS} is the parasitic capacitance of the CMOS transistors, C_L is the parallel capacitance of the inductor, and C_{load} is the loading input capacitance of the buffer that follows the VCO output. Because of the parasitics, the varactor can control only a portion of the total tank capacitance.

From circuit simulations, the total parasitic capacitance is approximately 1.21 pF. That leaves us 1 pF to be used for the varactor capacitance C_v. Usually the ratio between the maximum ($C_{v_{max}}$) and the minimum ($C_{v_{min}}$) capacitance we can get

from a MOS varactor is fixed regardless the size of the capacitance. From another circuit simulations shown in Fig. 39, we know the ratio is about 3 for 0.35 μm CMOS technology since the minimum capacitance in depletion mode is 107.7 pF and the maximum capacitance in inversion mode is 353.3 pF. The ratio highly depend of which technology the varactor is fabricated.

$$C_{v_{max}} = 3 \times C_{v_{min}} \tag{4.20}$$

In order to make the mean value of the varactor capacitance to be 1 pF,

$$\frac{C_{v_{min}} + C_{v_{max}}}{2} = \frac{C_{v_{min}} + 3C_{v_{min}}}{2} = 2C_{v_{min}} = 1 \text{ pF} \tag{4.21}$$

From (4.20) and (4.19), the minimum and the maximum total capacitance are calculated as,

$$C_{tank_{min}} = C_{v_{min}} + C_L + C_{CMOS} + C_{load} = 1.71 \text{ pF} \tag{4.22}$$

$$C_{tank_{max}} = 3C_{v_{min}} + C_L + C_{CMOS} + C_{load} = 2.71 \text{ pF} \tag{4.23}$$

Using the capacitance values, the tuning range can be calculated.

$$f_{max} = \frac{1}{2\pi\sqrt{LC_{tank_{min}}}} = 2.728 \text{ GHz} \tag{4.24}$$

$$f_{min} = \frac{1}{2\pi\sqrt{LC_{tank_{max}}}} = 2.167 \text{ GHz} \tag{4.25}$$

$$\Delta f = f_{max} - f_{min} = 561 \text{ MHz} \tag{4.26}$$

Note that the frequency tuning range of the VCO is now, rather high, 561 MHz. From Table VIII, it actually covers the entire extended tuning range requirement that takes into account 10% process variation. However, we have already established in section IV-B, that the tuning sensitivity 150 MHz/V is too small to cover the entire extended tuning range. This only means that the tuning sensitivity of the designed

varactor is much higher than 150 MHz/V. We can calculate the tuning sensitivity from Fig. 39. The inversion mode varactor changes its capacitance from the minimum to the maximum when the bias voltage changes from 0.5 V to 1 V. Thus the tuning sensitivity is,

$$S_{tuning} = \frac{\Delta f}{1\text{ V} - 0.5\text{ V}} = 1122\text{ MHz/V} \tag{4.27}$$

which is way too high for the given specification. The increased sensitivity will result in higher phase noise and frequency drift. To decrease the tuning sensitivity, a discrete-tunable varactor array is introduced in the next section.

4. Discrete-Tunable Varactor Array

As we already discussed in previous section, there is a serious trade-off between the tuning range and the sensitivity. If the tuning range is wide, it is good for countering process variations, but it will increase the sensitivity of the frequency to control voltage noise, and vice versa. To solve this trade-off, the discrete-tunable varactor array is introduced.

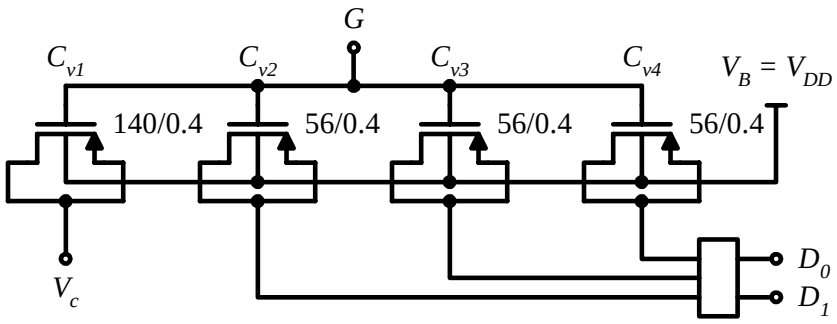


Fig. 40. Discrete-tunable inversion mode varactor array

As shown in Figure 40, the varactor array consists of two parts; a large inversion mode MOS varactor C_{v_1} that is controlled by V_c and several small same type MOS varactor controlled by the digital word D_0D_1. Now the tuning sensitivity is decided by

C_{v_1} only since it is the only varactor that is directly connected to the control voltage. And the total tuning range is decided by the combination of C_{v_1} and remaining small varactors $C_{v_2} \sim C_{v_4}$. In this way, we can make the tuning range wide enough to cover the process variations yet the tuning sensitivity is low enough to make the noise on the control voltage V_c negligible.

The simulation results show that by using the discrete-tunable varactor array, the VCO can cover the range of 2380 MHz $\sim$ 2730 MHz while maintaining the gain of less than 140 MHz/V.

5. CMOS Transistor Drivers

The size of the driver transistors can be calculated from the requirement of the size of the negative resistance to compensate the loss of the LC tank to sustain the oscillation. g_m of the cross-coupled MOS pairs must be high enough to compensate the loss of the tank. A simplified schematic to model the loss mechanisms is shown in Fig. 41. g_{o_N} and g_{o_P} represents finite output resistances of NMOS and PMOS pairs, respectively. Series resistances R_C and R_L are added to model lossy capacitor and inductor. R_P represents all other sources of loss not modelled by the added resistances.

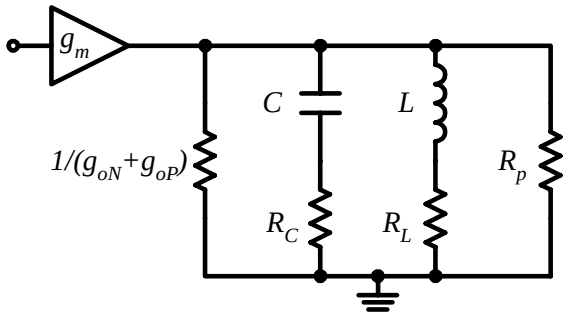


Fig. 41. VCO model for loss calculation

The series resistances of the varactor and the inductor, R_C and R_L can be con-

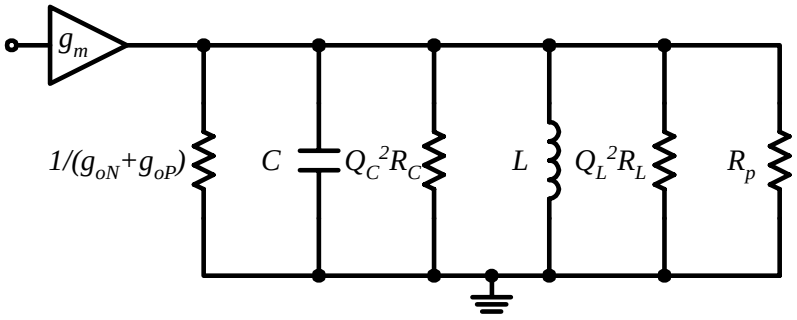


Fig. 42. VCO model after series-to-parallel conversion

verted into parallel resistors for easier calculations. Once converted into parallel resistors, the total loss is a parallel combination of all the resistors. The schematic after the series-to-parallel conversion is shown in Fig. 42. Quality factors Q_L and Q_C play a critical role in the conversion process. As noted in the Fig. 42, the higher the quality factor, the higher the parallel resistance. High parallel resistance results in less loss. The quality factors are defined as,

$$Q_L = \frac{\omega_o L}{R_L} \tag{4.28}$$

$$Q_C = \frac{1}{\omega_o C R_C} \tag{4.29}$$

The amount of g_m that is needed to compensate all the loss can be shown as,

$$g_m > \alpha_{min}\left\{g_{o_N} + g_{o_P} + \frac{1}{R_P} + \frac{1}{Q_C^2 R_C} + \frac{1}{Q_L^2 R_L}\right\} \tag{4.30}$$

where α_{min} is the excess small-signal loop gain of the system for the startup condition. Typically α_{min} must be higher than or equal to 3 to ensure the startup in the worst case condition and to overcome process variations.

The most dominant loss is the loss of the inductor due to low quality factor. It

is calculated as,

$$\frac{1}{Q_L^2 R_L} = \frac{1}{5.27^2 \times 5.57\ \Omega} \tag{4.31}$$

$$= 6.5\ \text{mS} \tag{4.32}$$

The next dominant loss source is the varactor. It is calculated as,

$$\frac{1}{Q_C^2 R_C} = \frac{1}{59^2 \times 0.56\ \Omega} \tag{4.33}$$

$$= 0.51\ \text{mS} \tag{4.34}$$

From equation (4.30), the minimum requirement of the driver transconductance is,

$$g_m > 21\ \text{mS} \tag{4.35}$$

When calculating the size of transistors from given transconductance, the minimum length of the given process technology should be used to minimize the effect of parasitic capacitances.

6. Layout

Fig. 43 shows the layout of the CMOS VCO for Bluetooth application. The VCO consists of four sub-blocks; MOS drivers, varactor, inductors, and phase shifter. It is important to make the layout as symmetric as possible so that the positive and the negative signal of the differential signal may see the same input and output impedances.

The layout of the spiral inductor is the most important in VCO layout. The detail of the inductor layout is shown in Fig. 44. There are a set of rules to follow during the spiral inductor layout to maximize its quality factor while minimizing the size.

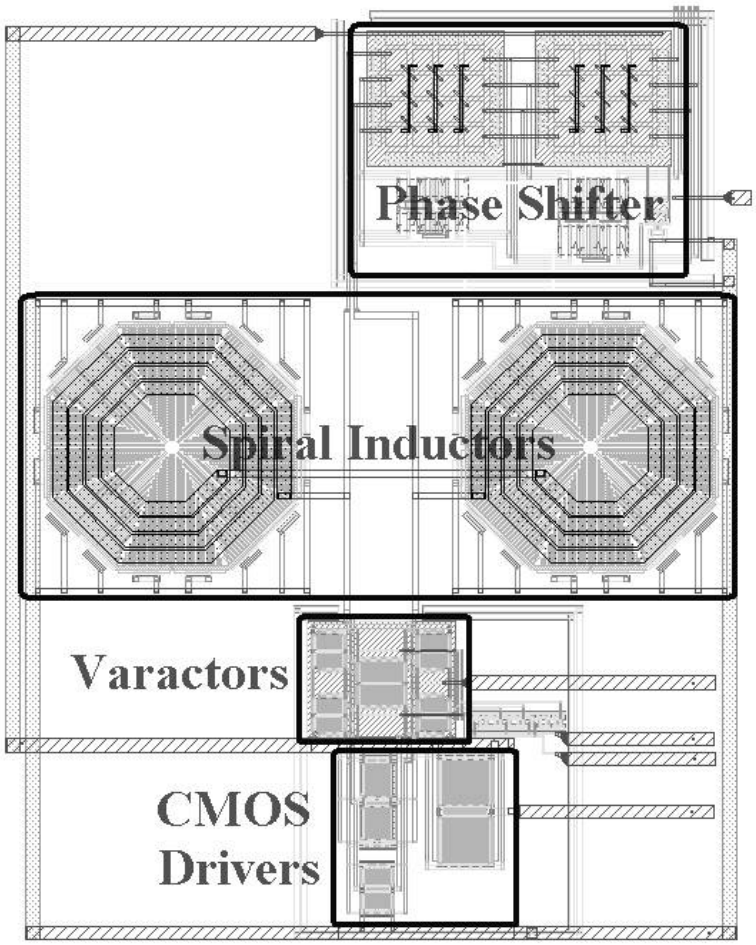


Fig. 43. Layout of CMOS VCO for Bluetooth application

1. Make the spiral as close to a circle as possible. It will maximize the inductance we can get from a given area. The one that is shown in Fig. 44 is in a octagonal shape since only diagonal path is allowed.

2. Use hollow centered spiral. Small spirals close to the center do not have significant contribution to the inductance. They only increase the loss due to Eddy current. Therefore, in order to increase the Q of the inductor, the center spirals should be removed.

3. Use a patterned ground shield underneath the spiral to reduce the effect of

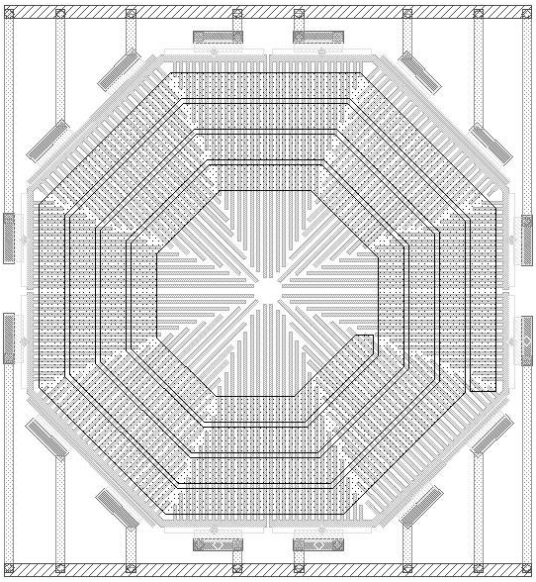


Fig. 44. Inductor layout detail

capacitive coupling to the substrate. The shield must be broken regularly in the direction perpendicular to the current flow to prevent magnetic coupling that increases loss.

4. Avoid any closed-loop ring around the spiral since it will contribute to signal loss. In Fig. 44, the connection between the patterned shield and the ground node is done by a broken ring and combed interconnects.

7. Simulation Results

The simulation results shown in this section are from a post-layout simulations. The circuit elements and parasitic components from the layout shown in Fig. 43 are extracted and simulated with Cadence Spectre simulator.

First of all, the oscillation startup condition is verified. In order to make the oscillation start regardless the initial state, the VCO must have enough g_m to compensate the loss of the tank and other non-ideality. Fig. 45 shows the VCO can start

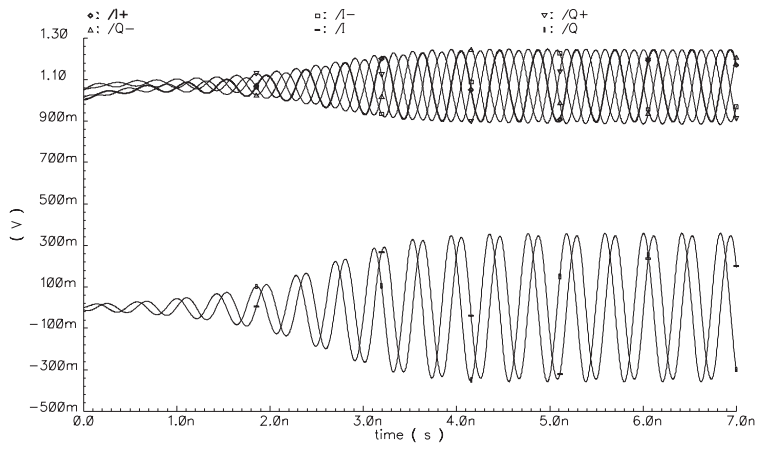


Fig. 45. Differential I and Q signals from a transient response of the VCO

oscillation without any significant startup kicking. The four waves shown on the top side are differential signal pairs of the in-phase (I) and quadrature (Q) outputs. The two waves on the bottom side are I and Q signal after a differential-to-single-ended conversion. The simulated signal amplitude is about 0 dBm, which is 6 dB lower than estimated in equation (4.14) due to additional loss. However, it is still within specification.

The next simulation results shown in Fig. 46 are the frequency tuning range and the sensitivity of the VCO. Each waveform shows the relationship between the control voltage (V_c) and the output frequency (f_o). Each tuning bracket of discrete coarse tuning has a frequency range of about 160 MHz over a control voltage variation of 1.2 V. Thus the frequency tuning sensitivity within a single bracket is

$$S_{tuning} = \frac{160 \text{ MHz}}{1.2 \text{ V}} = 133 \text{ MHz/V} \tag{4.36}$$

which is within the specification. Overall tuning range covered by all the coarse tuning brackets is from 2380 MHz to 2730 MHz, which results in a total frequency tuning range of 350 MHz.

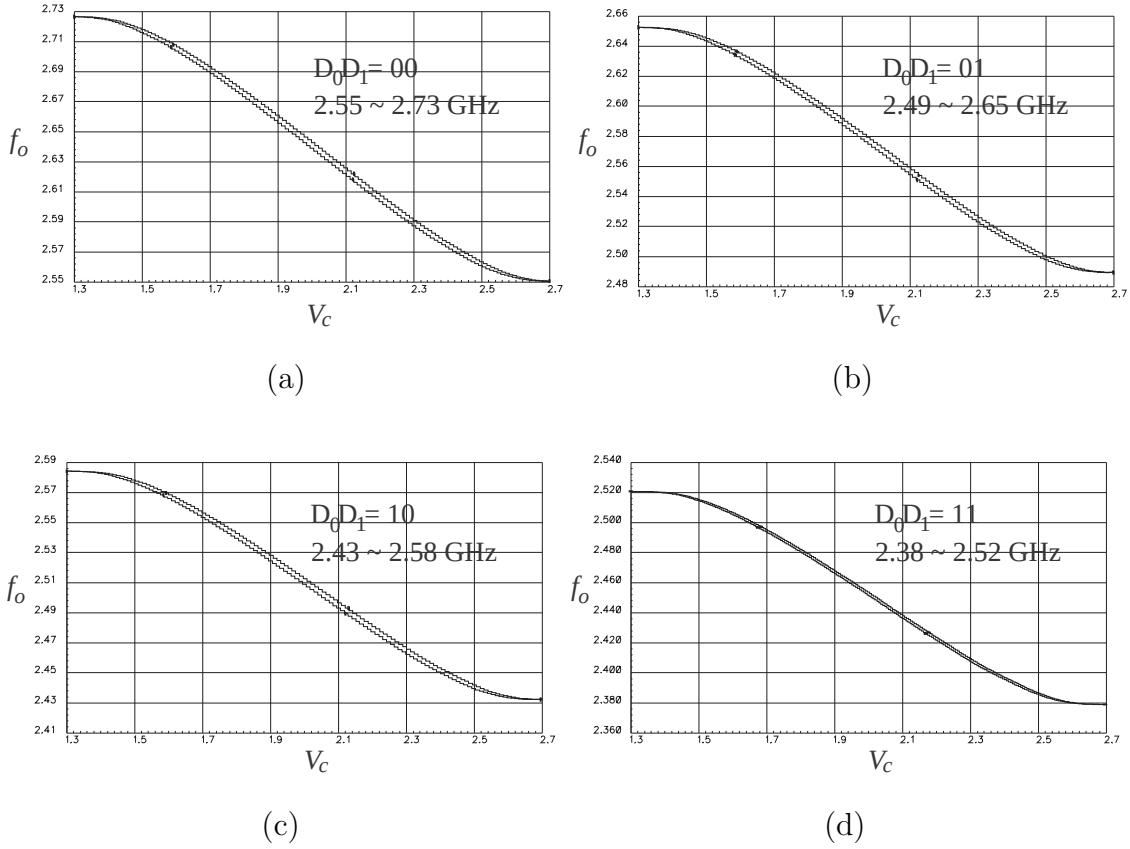


Fig. 46. Four coarse tuning brackets shows frequency tuning range and sensitivity. (a) $D_0D_1 = 00$ (b) $D_0D_1 = 01$ (c) $D_0D_1 = 10$ (d) $D_0D_1 = 11$

Phase noise is simulated with a periodic steady state (PSS) analysis in SpectreRF circuit simulator. PSS analysis can provide fairly accurate results since it takes into account the effect such as noise folding due to non linearity. Phase noise requirement of the VCO is less than -124 dBc/Hz at a frequency offset of 3 MHz from the carrier. The simulation result in Fig. 47 shows a 6 dB better result, -130 dBc/Hz at 3 MHz offset frequency. Note that -124 dBc/Hz requirement already has 6 dB margin from the absolute limit, but additional 6 dB margin in simulation is well reserved for the noise sources neglected in the circuit simulation, such as substrate coupling and power supply noise.

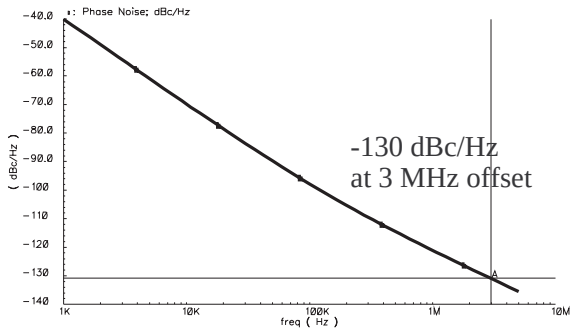


Fig. 47. Phase noise simulation result from PSS analysis

8. Testing and Measurement

The proposed Bluetooth receiver is fabricated in a 0.35-μm CMOS process. Fig. 48 shows the microphotograph of the fabricated chip with entire receiver building blocks. The VCO is located at the bottom left corner of the chip, occupying 470 μm $\times$ 590 μm of die area. The VCO dissipates 10 mA from a single 3.3 V supply.

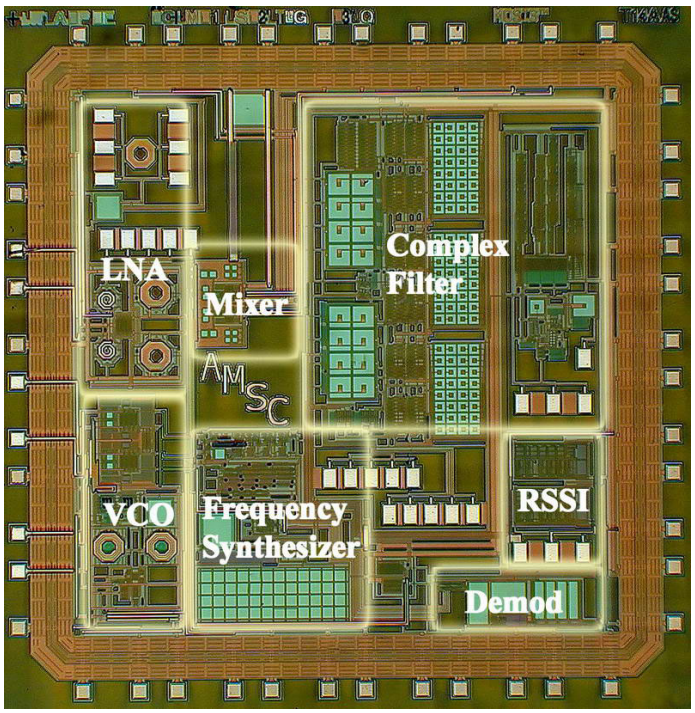


Fig. 48. Chip microphotograph of the Bluetooth receiver

Testing and measurement of the VCO is done exclusively with a spectrum analyzer. Spectrum analyzers can measure the power of the carrier signal, the tuning range, and the phase noise performances. Although spectrum analyzers can measure the power of the signal, but not as accurate as the measurement of a dedicated power meter such as HP E4419B. The spectrum analyzer used in this experiment is FSE model from Rohde & Schwarz.

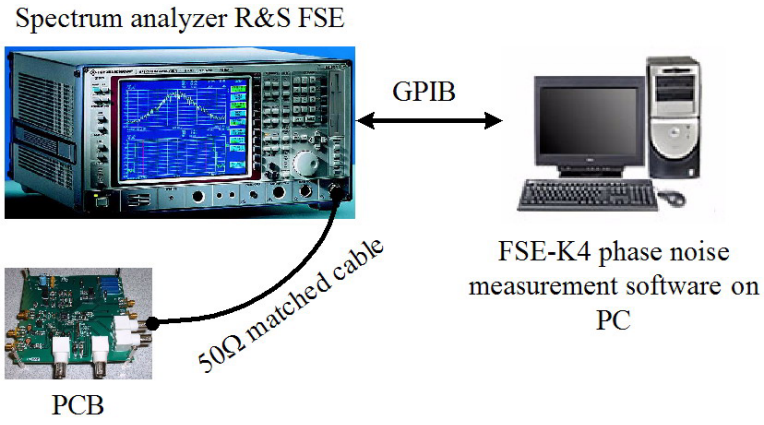
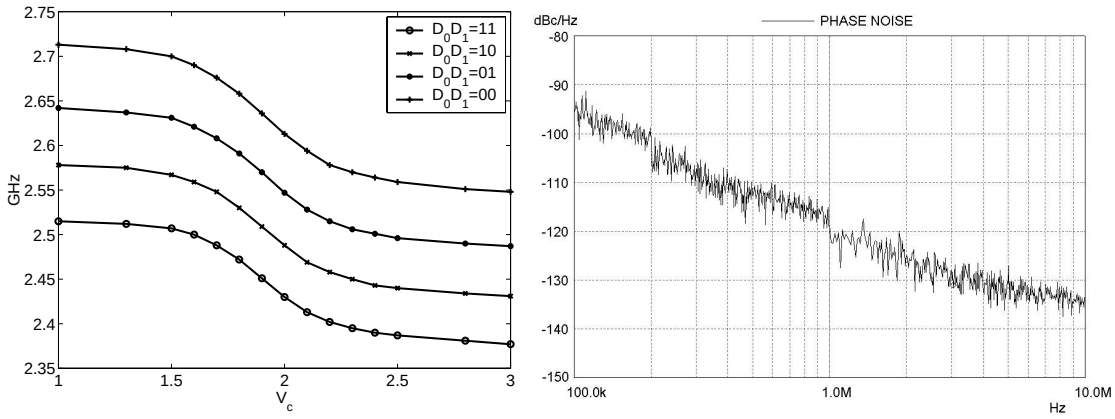


Fig. 49. VCO testing setup with a spectrum analyzer

A conceptual diagram of the testing setup is shown in Fig. 49. A printed circuit board (PCB) is developed especially for the testing of the Bluetooth receiver. The VCO testing is a part of the whole receiver testing. The output of the VCO is connect to the spectrum analyzer through 50 Ω matched high frequency cable. A matching network is recommended between the output pin of the chip and the 50 Ω connector to minimize the loss of signal.

The tuning range measurement is shown in Fig. 50(a). It shows a very good agreement with the simulation results in Fig. 46. The measured tuning range of four coarse tuning brackets is from 2370 MHz to 2720 MHz, with a total frequency tuning range of 350 MHz. The coarse tuning setting of $D_0D_1 = 11$ (the curve shown on the bottom) can cover entire band that is required for Bluetooth application. In an on-line



(a) (b)

Fig. 50. Experimental measurement results of Bluetooth VCO. (a) Tuning range measurement with four coarse tunings (b) Phase noise measurement output from FSE-K4 control software

operation of the frequency synthesizer, the coarse tuning does not have to change its setting from $D_0D_1 = 11$. However, each fabricated chip may have different variations on the frequency tuning range, and that can change the coarse tuning setting.

The phase noise measurement is done with a control software installed on a PC that is connected to the spectrum analyzer through a GPIB connection. Since phase noise is a sort of random process, measured power of the phase noise has direct relationship with resolution bandwidth settings of the spectrum analyzer. It becomes cumbersome to manually change the resolution bandwidth for each measurement point at different frequency offsets. The phase noise can be measured automatically by using control software FSE-K4 otherwise very time consuming if done manually. The result is shown in Fig. 50(b). The measured phase noise at 3 MHz offset from the carrier is about -128 dBc/Hz. Since the specification is -124 dBc/Hz, it still has 4 dB margin.

F. Multi-Standard BiCMOS VCO Design Details

The next example is a VCO designed for a multi-standard wireless LAN receiver for 802.11a and 802.11b standards. A BiCMOS process technology is chosen to utilize the bipolar transistors for minimum power consumption through out the whole receiver. A bipolar transistor can provide higher small-signal transconductance g_m than CMOS transistor with same amount of bias current. In addition to bipolar transistors, the IBM6HP BiCMOS technology provides unique options for designing the passive elements, specific for the process. The detail of the passive elements design is in the following sections.

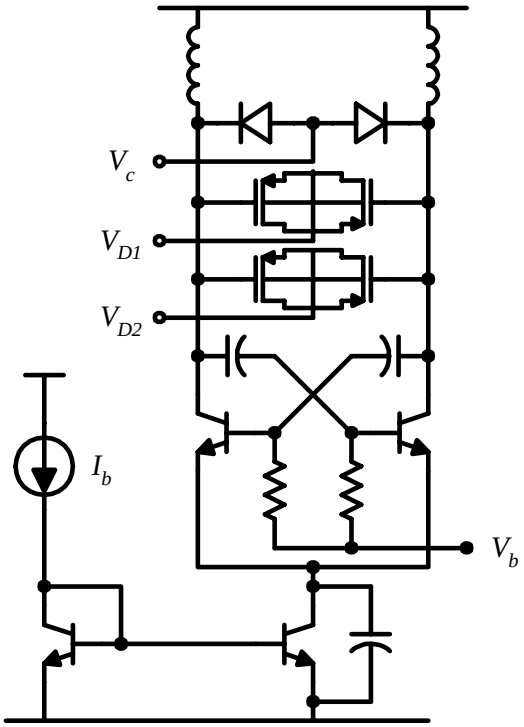


Fig. 51. Schematic of a BiCMOS VCO

The VCO is implemented with a LC-tuned negative-g_m oscillator as shown in Fig. 51. Since it has the same architecture as the previous example of CMOS VCO,

the overall design process is largely same. Fundamentally they share exactly same design trade-offs described in section IV-D.

Several circuit design techniques have been taken to improve the phase noise performance. First, base nodes of the bipolar transistor drivers are AC-coupled with oscillating nodes and biased by an extra DC biasing circuit to keep the transistors in the active region. Although the biasing circuit increases the effective base resistance, improved linearity helps to reduce the overall phase noise. Second, a bypass capacitor on the common emitter node reduces the noise contribution of the current bias transistors [66].

1. Bias Current

Just like the previous example, the power budget of the whole receiver system is extremely tight. The maximum total current allowed for the VCO is 11 mA, which is equivalent to 27.5 mW of power consumption from 2.5 V power supply. Since the 11 mA is a total current consumption limit, including a buffer between the VCO and the following mixer, we have to budget it carefully distributing the power among the VCO core, the bias circuits, and the buffer. After some preliminary circuit simulations, it is divided as; 6.5 mA for VCO core, 3 mA for buffer, and 1.5 mA for biasing. Less than half of the 6.5 mA budgeted for VCO core is actually used as the tail current source for the differential pair driver.

$$I_{tail} = 3 \text{ mA} \tag{4.37}$$

2. Inductor in Analog BiCMOS Process

Being an analog semiconductor process technology, the IBM6HP process provides special thick metal layer especially suited for a on-chip spiral inductor design. A

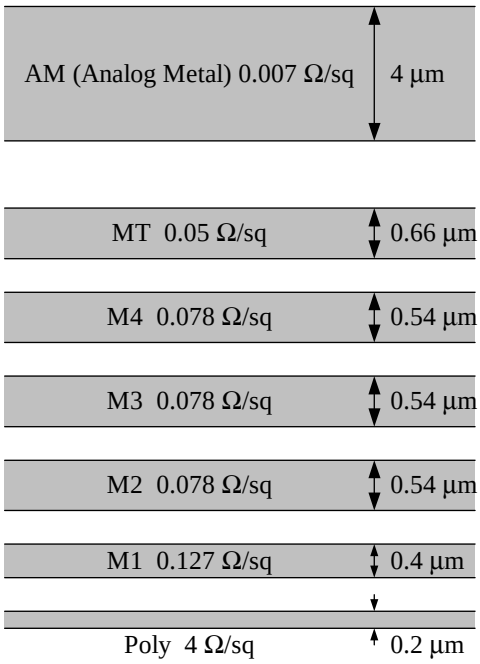


Fig. 52. Thickness and sheet resistivity of poly and metal interconnects in IBM6HP process

cross section of the poly and the metal layers available from the technology is shown in Fig. 52. The top-metal is called analog metal (AM) and it is made of aluminum with a thickness of 4 μm and a sheet resistivity of 7.25 m$\Omega/\square$. It is extremely good quality for analog design purpose, compared to the top-metal of the TSMC CMOS 0.35 μm process, which has a thickness of 1 μm and a sheet resistivity of 40 m$\Omega/\square$.

The inductor designed for the VCO is shown in Fig. 53. Underneath the spiral, there is a grid of deep-trench for better isolation of substrate coupled noise. Design parameters of the inductor are given in Table XII. Simulated quality factor of the 1.214 nH inductor is 13. Once the bias current and the inductor parameters are

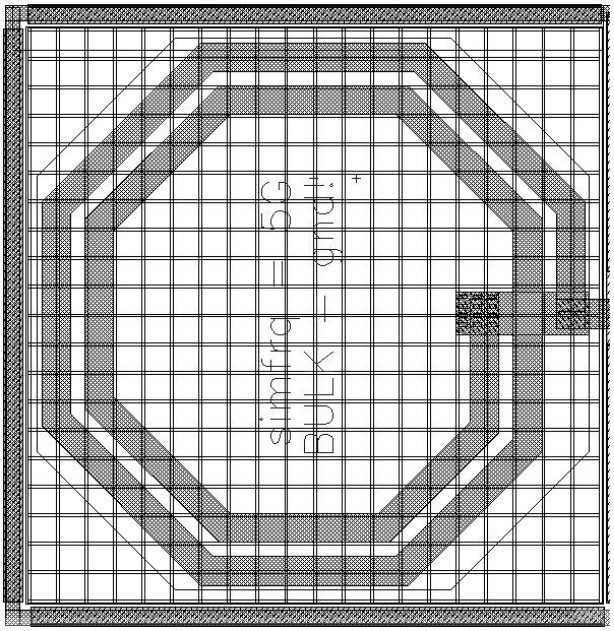


Fig. 53. Inductor layout for multi-standard VCO

known, we can calculate the output amplitude from equation (4.5).

$$V_{signal} = I_{tail} R_p = I_{tail} Q_L^2 R_s \tag{4.38}$$

$$= 3 \text{ mA} \times 13^2 \times 2.93\ \Omega \tag{4.39}$$

$$\simeq 1.49 \text{ V} \tag{4.40}$$

which is equivalent to 13.4 dBm. The requirement for multi-standard transceiver is 3 dBm. Like in the case of Bluetooth VCO, a margin of 10 dB is reserved for additional losses.

3. BiCMOS Varactor

In a bipolar semiconductor technology, it is possible to use a well-controlled intrinsic diode between base and collector as a varactor. In this case, the varactor is a diode with the properties of a voltage-dependent capacitor. Specifically, it is a variable-

Table XII. Spiral inductor parameters for multi-standard VCO

Dimension	190 μm $\times$ 190 μm
Metal width	10 μm
Metal spacing	5 μm
Number of turns	2
Inductance L	1.214 nH
Series resistance R_s	2.93 Ω
Quality factor Q	13

capacitance, pn-junction diode that makes good use of the voltage dependency of the depletion-area capacitance of the diode. All diodes exhibit this phenomenon to some degree, but specially made varactor diodes exploit the effect to boost the capacitance and variability range achieved - most diode fabrication attempts to achieve the opposite.

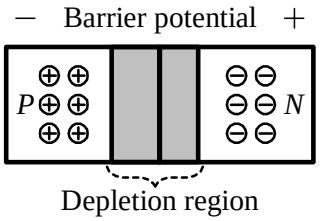


Fig. 54. PN-junction as a varactor

In Fig. 54, two materials are brought together to form a pn-junction diode. The different voltage levels in the two materials cause a depletion region, which contains no free electrons or holes. The movement of electrons through the materials creates an electric field across the depletion area that is described as a barrier potential and has the electrical characteristics of a charged capacitor.

It is operated reverse-biased so no current flows through it, but since the width

of the depletion region varies with the applied bias voltage, the capacitance of the diode can be made to vary. Generally, the depletion region width is proportional to the square root of the applied voltage; and capacitance is inversely proportional to the depletion region width. Thus, the capacitance is inversely proportional to the square root of applied voltage.

The varactor provided by IBM6HP process comes in a 2×20 μm standard layout cell. Unit mean capacitance of the varactor is 1.3 fF/μm^2, which result in 52 fF per cell. And the capacitance variation range is $\pm 20\%$ that can make the standard cell varactor vary from 42 fF to 62 fF.

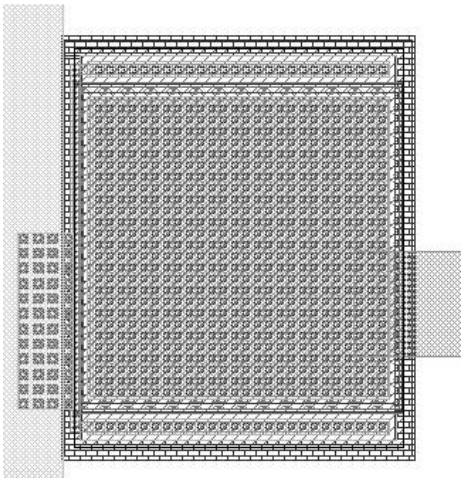


Fig. 55. Varactor layout

The layout of the varactor used in the VCO is shown in Fig. 55. The total effective area of the varactor is 20 μm $\times$ 20 μm and the capacitance varying range is from 416 fF to 624 fF. From preliminary simulations, a parasitic capacitance of 200 fF is added to the total capacitance. Thus the minimum and the maximum capacitances

are,

$$C_{min} = 616 \text{ fF} \tag{4.41}$$

$$C_{max} = 824 \text{ fF} \tag{4.42}$$

Using the capacitance values, the tuning range can be calculated as the following.

$$f_{max} = \frac{1}{2\pi\sqrt{LC_{min}}} = 5.820 \text{ GHz} \tag{4.43}$$

$$f_{min} = \frac{1}{2\pi\sqrt{LC_{max}}} = 5.032 \text{ GHz} \tag{4.44}$$

$$\Delta f = f_{max} - f_{min} = 788 \text{ MHz} \tag{4.45}$$

The varactor can provide the VCO with 788 MHz of tuning range; wide enough for both standards individually but not both at the same time. Discretely programmable capacitor banks are present to switch modes between the two standards. The program input of the capacitor banks are denoted as V_{D1} and V_{D2} in Fig. 51. Once the mode is set, there is no on-line switching involved during the channel transition.

4. Bipolar Transistor Driver

One of the most significant advantage of using bipolar transistor drivers in VCO circuit is that it can provide higher transconductance (g_m) when biased with an equal current. The g_m of a bipolar transistor is,

$$g_{m_{bipolar}} = \frac{I_c}{V_T} \tag{4.46}$$

where I_c is the collector bias current and V_T is the thermal voltage, kT/q. The limitation of CMOS g_m comes from the subthreshold conduction effect. In saturation

mode, a NMOS transistor has a g_m of

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{4.47}$$

where μ_n is the mobility of electrons, C_{ox} is the oxide capacitance, and I_D is the bias current. Equation (4.47) implies that g_m could be increased indefinitely with a fixed I_D by increasing the transistor width, W. However, a problem lies with the bias current. The bias current is expressed as,

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{4.48}$$

If W increases while I_D remains constant, then V_{GS} has to decreas and the device enters the subthreshold region. In the subthreshold region, I_D exhibits a exponential dependence on V_{GS}. It can be shown that,

$$I_{D_{sub}} = I_o \exp \frac{V_{GS}}{\zeta V_T} \tag{4.49}$$

where $\zeta > 1$ is a nonideality factor. As a result, the transconductance is calculated to be,

$$g_{m_{sub}} = \frac{I_D}{\zeta V_T} \tag{4.50}$$

Comparing (4.46) and (4.50), it is clear that MOS transistor has an inferior transconductance by a factor of ζ.

The required amount of g_m is calculated just like the CMOS case described in section IV-5. The amount of g_m that is needed to compensate the loss of inductor and the varactor is given as,

$$g_m > \alpha_{min} \left\{ \frac{1}{Q_C^2 R_C} + \frac{1}{Q_L^2 R_L} \right\} \tag{4.51}$$

where α_{min} is the excess small-signal loop gain of the system for the startup condition.

Like in CMOS VCO, α_{min} must be higher than or equal to 3 to ensure the startup of output oscillation.

The most dominant loss is the loss of the inductor due to low quality factor. It is calculated as,

$$\frac{1}{Q_L^2 R_L} = \frac{1}{13^2 \times 2.93\ \Omega} \tag{4.52}$$

$$= 0.002\ \text{mS} \tag{4.53}$$

and the next dominant loss source is the varactor. It is calculated as,

$$\frac{1}{Q_C^2 R_C} = \frac{1}{60^2 \times 1.02\ \Omega} \tag{4.54}$$

$$= 0.0003\ \text{mS} \tag{4.55}$$

From equation (4.51), the minimum requirement of the driver transconductance is,

$$g_m > 6.9\ \text{mS} \tag{4.56}$$

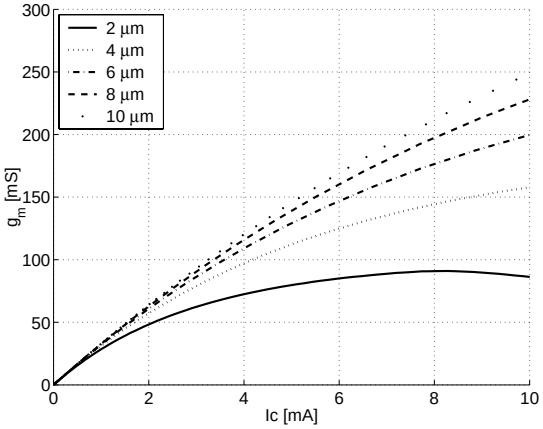


Fig. 56. g_m vs. bias current curves of bipolar transistors with different emitter length

Fig. 56 shows the variation of g_m vs. bias current. Each curve is drawn for bipolar transistor with different emitter length ranging from 2 μm to 10 μm. Ideally,

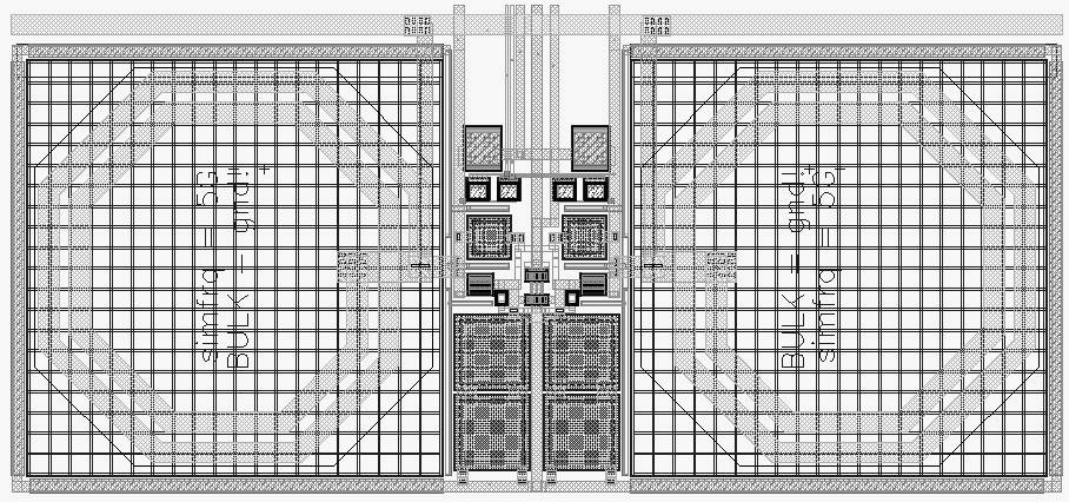


Fig. 57. BiCMOS VCO layout

the plot of g_m vs. I_c should be a straight line starting from the origin with a slope of $1/V_T$ as described in equation (4.46). In reality, if the emitter length is short, g_m is compressed as the bias current I_c increases due to collector current saturation. As the emitter length gets longer, g_m behaves more similar to the ideal case. Shorter emitter length is beneficial since smaller transistor has less parasitic capacitances, which in turn makes the transistor fast. g_m exceeds the required value of 6.9 mS even when the emitter area is much smaller than 2 μm. Although we could reduce I_c and use larger bipolar transistor to improve the power consumption performance, I_c must not be reduced since it will make the signal amplitude decrease according to 4.38). We can conclude that the bias current is limited by the signal amplitude requirement, not by the small signal g_m requirement.

5. Layout

The overall layout of the VCO is shown in Fig. 57. Symmetric layout is important for the differential signaling. Most of the area is occupied by the two inductors on both

sides. Rest of the components are placed between the inductors. The noise decoupling capacitors are laid out on the bottom part of the area between the inductors, which would have been wasted even if they were not present. Thus the addition of the noise decoupling capacitor does not increase overall area consumption of the VCO.

6. Testing and Measurement

The testing and measurement of the bipolar VCO for multi-standard receiver is done as a part of the frequency synthesizer testing. The detail of the measurement results is discussed in section V-E.

CHAPTER V

MULTI-STANDARD FREQUENCY SYNTHESIZER

A. Introduction

Wireless communication systems have gained popularity as the electronics industry introduces accessible consumer products leading the emerging market. WLAN is one of the most popular among many short-distance communication standards such as Bluetooth and HiperLAN. WLAN has become the preferred choice over other standards due to its transparency to users accustomed to well established Wired Local Area Network.

To be cost effective, a practical implementation of WLAN emerged as the 802.11b supplement, specifying the Physical Layer Extension in the 2.4-GHz band. However, a 11 Mbit/sec throughput turns out to be not enough as the usage model shifted from text-based content to multimedia content. 802.11a extends the capability of WLAN by moving the Physical Layer Extension into 5-GHz band. With wider bandwidth available, a 802.11a transceiver can reach a throughput of 54 Mbit/sec. Even though both 802.11b and 802.11a provide the same services to user, due to the popularity of 802.11b equipment, most of the new products have to support both standards at the same time. The cost of supporting both standards, however, is a major concern. Therefore, a multi-standard transceiver is essential to keep the size and cost at a minimum, while maximizing the amount of shared building blocks in both operating modes.

The specifications related to the frequency synthesizer design in both 802.11a and 802.11b standards require very similar performance [1, 2]. Due to this similarity, it is possible to design a single frequency synthesizer that meets the specifications of

both standards without duplication or switching of blocks involved. The details of the specifications are investigated in section B.

In fully integrated WLAN systems, the frequency synthesizer is a major design challenge. It has to meet stringent and conflicting requirements – such as having enough rejection for unwanted disturbances (narrow loop bandwidth) while keeping the settling time of the PLL fast enough to meet the channel switching requirement (wide loop bandwidth). Previous design efforts in [67, 68] showed that it is impossible for a conventional implementation of an integer-N synthesizer to meet both settling time and spurious signal rejection requirements for multi-standard 802.11a and 802.11b receiver. However, there are no 802.11a and 802.11b multi-standard frequency synthesizers for direct conversion receiver using an integer-N architecture reported yet. [69] utilizes a fractional-N architecture, which requires very large silicon area (3.22 mm^2) and high power consumption (231 mW). The integer-N implementation reported in [70] is targeted for a non-zero IF heterodyne receiver.

In section C and D, the problem of the conflicting bandwidth requirement is addressed by introducing an improved adaptive dual-loop PLL (ADPLL) architecture with a new loop filter topology that is better suited for spurious signal rejection and single-chip integration. Details of the circuit measurement follow in section E.

B. Specification Study

Table XIII summarizes the comparison between 802.11a and 802.11b standards [1, 2]. The most significant difference between 802.11a and 802.11b is their respective frequency band. To accommodate an increased throughput, 802.11a uses the 5 GHz ISM band instead of the 2.4 GHz ISM band. If a single VCO were to cover both 5 GHz and 2.4 GHz frequency bands, it would require a $\pm 41\%$ tuning range. Having

Table XIII. Wireless LAN 802.11a and 802.11b Standards

	802.11a	802.11b
Frequency band	5180–5805MHz	2412–2472MHz (4824–4944MHz)
Channel spacing	20MHz	5MHz (10MHz)
f_{REF}	2.5MHz	1MHz (2MHz)
Divider ratio	2072–2322	2412–2472
Settling time	224μs	224μs
Phase noise	-126dBc at 40MHz	-126dBc at 25MHz
Frequency accuracy	±100kHz	±120kHz

such wide tuning range is impractical since the VCO would require a very large capacitance, which degrades the phase noise performance.

An alternative solution is to synthesize at twice the frequency for 802.11b so that its band centers at 4.884 GHz as shown in Fig. 58. The actual output for the 2.4 GHz band 802.11b is generated with a divide-by-two circuit. With this approach, the VCO tuning range can be as low as ±9%, which can be easily achieved.

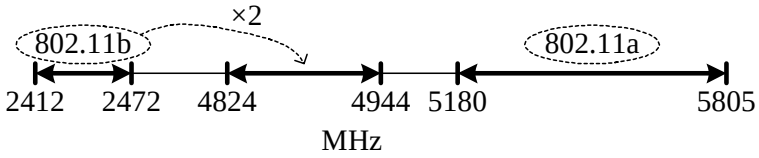


Fig. 58. Frequency band assignment

Since the target for the synthesizer is to use an integer-N architecture, the next step is to determine the reference frequency f_{REF} that allows to synthesize the required carrier signals for both standards and the corresponding frequency divider ratio. In an integer-N implementation, only integer multiples of f_{REF} can be synthe-

sized as output frequencies. For 802.11a, the highest possible f_{REF} is 5 MHz since all the channels are multiple of 5 MHz. But for 802.11b, the highest possible f_{REF} is 2 MHz since the channels are multiple of 2 MHz, even though the channel spacing is 10 MHz. In order to meet the specifications for both standards simultaneously, the loop has to be designed for the lowest f_{REF} requirement, 2 MHz for 802.11b mode. Although the maximum possible f_{REF} for 802.11a mode is 5 MHz, it is better to reduce it by half to 2.5 MHz to make the loop characteristic similar to each other for both standards.

One of the main problems of integer-N architectures is the spurious tones at the output of the VCO caused by the sampling process present in the phase frequency detector (PFD) and charge pump [7]. In narrow-band communication systems, these spurs usually lie outside the channel bandwidth and may downconvert adjacent channels into the desired channel. However, in the case of 802.11b, the reference spurs fall *within* the received signal because the channel bandwidth is larger than the reference frequency [71].

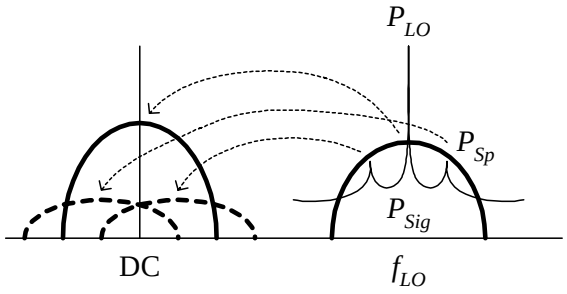


Fig. 59. The effect of reference spur down conversion in 802.11b system

The effect of reference spur down conversion is shown in Fig. 59, where P_{Sig}, P_{sp}, and P_{LO} are the power of received signal, spurs, and carrier signal, respectively. System level simulations are required to determine the specific level of spur that degrades the receiver bit error rate (BER) below the given specification. The CCK coded

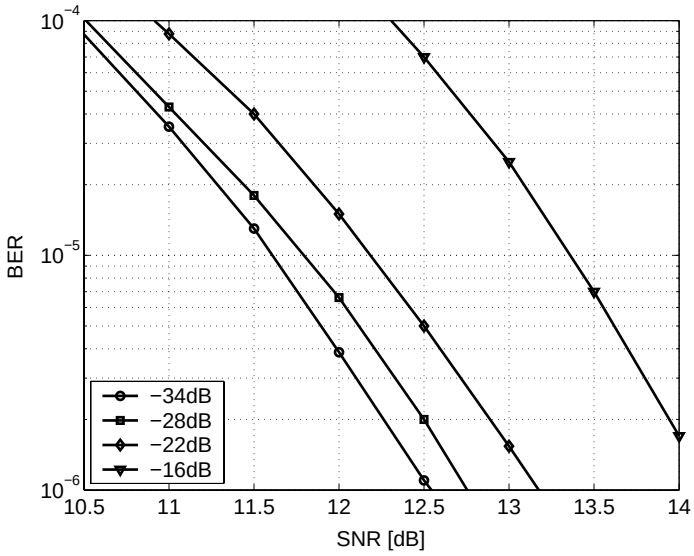


Fig. 60. Simulation results of BER degradation due to reference spur at 2 MHz in 802.11b system

baseband signal of 802.11b system is simulated using SytemView^{TM}software. The baseband signal is up-converted by 2 MHz and then added to the original baseband signal. The degradation of the final signal is measured in terms of BER. Simulation results of BER degradation are presented in Fig. 60. The SNR of the input signal is swept from 10.5 dB to 14 dB, while four different spur powers of -34, -28, -22, and -16 dB degrade the input signal. The results show that the reference spur must be at least 25 dB below the carrier signal to keep a BER better than 10^{-5} when the input SNR is 12 dB. This requirement needs additional margin for a realistic design because it is sensitive to the variation of the input SNR: if the input SNR drops to 11.5 dB, the spur rejection requirement is increased by 11 dB, resulting in 36 dB below the carrier.

Reference spur rejection can be improved by narrowing loop bandwidth. However, narrow bandwidth leads to slow settling time. To improve spur rejection while maintaining required settling time performance, an ADPLL architecture is investi-

gated in the next section.

C. System Architecture

Integer-N architecture is the preferred solution for minimizing power consumption and die area due to its simplicity. But it lacks the flexibility of arbitrary f_{REF} as in more complex fractional-N architecture. In integer-N architecture, the output carrier frequencies must be integer multiples of f_{REF}. Thus the loop bandwidth is limited by the fixed f_{REF}. Stability considerations limit the loop bandwidth to less than 1/10th of f_{REF} [14]. The limitation on f_{REF} becomes more severe in a narrow-band system such as wireless LAN, since the spacing between two consecutive channels is very close.

Narrow loop bandwidth is beneficial when there are strong disturbances in the forward path of the loop. It is particulary useful to reject reference spurs since the unwanted signal will experience a low-pass transfer function when appears at the output of the frequency synthesizer. However, if the bandwidth is too narrow, the loop time constant becomes too slow to meet the settling time requirement.

Several techniques have been proposed to relax the tradeoff between settling time and spur rejection [14, 72]. A common technique is the so-called gear shifting, which involves increasing the loop bandwidth during a frequency transition [73]. One of the main disadvantages of this technique is the introduction of glitches on the VCO control line during the bandwidth switching. This glitches introduce extra phase error in the loop and can degrade the improved settling time. The problem of slow settling time can be avoided by utilizing the adaptive dual-loop PLL (ADPLL) as a speedup method, which also eliminates the introduction of glitches during bandwidth switching [74]. The fundamental idea of the adaptive dual-loop PLL is shown in

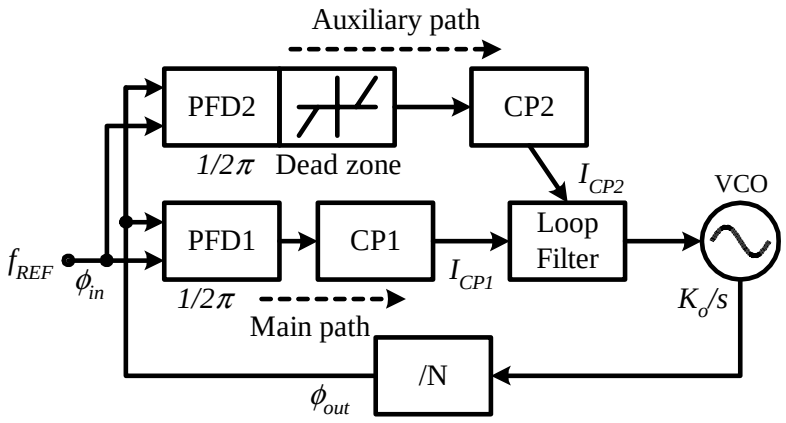


Fig. 61. Adaptive dual-loop phase locked loop (PLL) architecture

Fig. 61. When the loop is stable, and thus the phase error small, only the main loop is active and the synthesizer operates with a narrow loop bandwidth. If the divider ratio changes, and the phase error becomes large due to a frequency step in the feedback path, the auxiliary path becomes active and pushes the loop bandwidth to a higher frequency. Once the output signal is close enough to the target frequency, the auxiliary path is disabled and only the main loop is active. The loop bandwidth returns to its original value so that any spurious signal is rejected.

Normally, the ADPLL is used when there is a need to speed-up the loop to meet settling time requirement [75]. However, there are still some challenging issues in using the ADPLL as a spur rejection scheme in fully-integrated design. The increased spur rejection is obtained through a considerable reduction of loop loop bandwidth on the main path. In order to reduce the loop bandwidth substantially, very large capacitors may be required, which can be prohibitively large. Thus the direct application of an ADPLL may not be a practical solution for spur rejection. To overcome this problem without a considerable penalty in silicon area, an active capacitor multiplier is introduced to implement large capacitors. Details of the implementation of the capacitor multiplier are presented in section D-3.

D. Circuit Description

1. Phase Frequency Detector with Dead Zone Width Control

As shown in Fig. 61, the ADPLL requires two sets of phase frequency detectors and charge pumps to implement the adaptively adjustable loop bandwidth. A key element in ADPLL architecture is the PFD in auxiliary path that has an additional larger dead zone intentionally. Normally conventional PFD would have a dead zone cancellation circuit to prevent it in the first place, since dead zone degrades overall phase noise performance of a PLL. In the dead zone, a PFD practically stops working and does not produce UP/DOWN pulses. The ADPLL architecture takes advantage of this effect by using it as a method to effectively remove the auxiliary path from the PLL without glitch problem. Due to the dead zone, the auxiliary path stops producing pulses when the phase error is smaller than a predetermined phase error range. In other words, only when the loop is in transition state, the auxiliary path is operating and speed-up of the loop is accomplished [75].

The problem of implementing ADPLL for a narrow band system is that the phase error is quite small already even for the maximum frequency transition, which would generate the maximum phase error. The maximum phase error for 802.11b synthesis can be calculated when the frequency jumps from the lowest frequency 4824 MHz to the highest frequency 4944 MHz. Assuming the synthesizer is settled to produce 4824 MHz output, the signal after the frequency divider must be the same frequency as the reference signal since the PLL is locked to the reference. The period of the reference signal is,

$$P_1 = \frac{1}{2 \text{ MHz}} = 0.5 \ \mu\text{s} \tag{5.1}$$

In order to make the frequency transition, the division ratio has to change from 2412 to 2472 for the new output frequency. Right after the division ratio is changed,

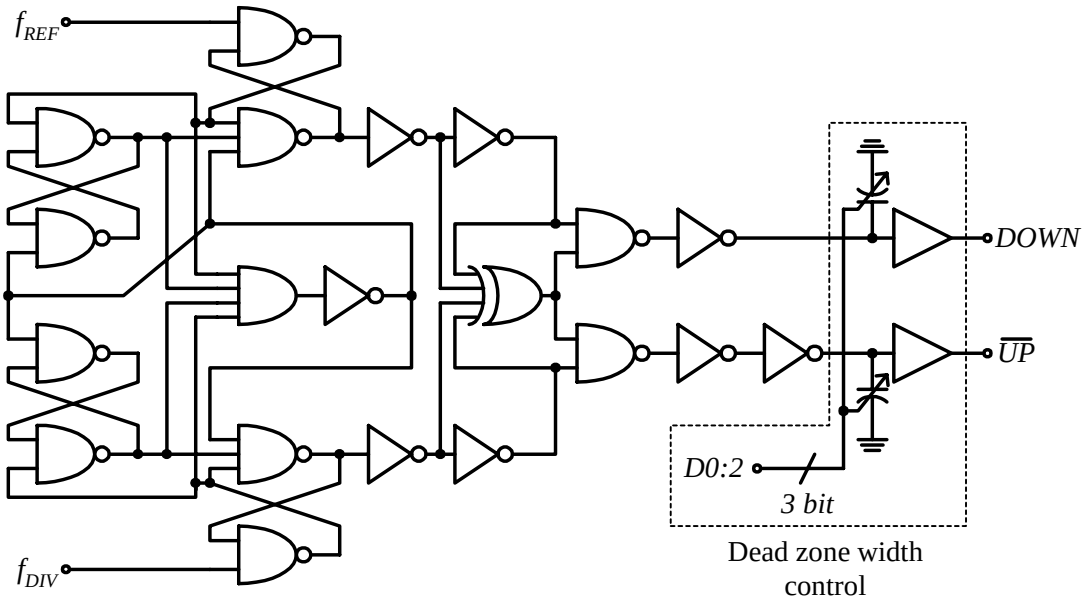


Fig. 62. PFD with dead zone control

the synthesizer output frequency is still unaffected. Now the signal after the frequency divider has longer period than before since the division ratio is increased. Thus the new period of the signal is,

$$P_2 = \frac{1}{4824 \text{ MHz}/2472} = 0.512 \ \mu\text{s} \tag{5.2}$$

P_1 and P_2 have a difference of only 12 ns in time. The phase error in terms of degree is,

$$E_P = 360\frac{P_2 - P_1}{P_1} = 8.96 \text{ degree} \tag{5.3}$$

This shows that the maximum phase error possible in 802.11b synthesizer must be less than 9 degree. The auxiliary PFD must be able to perceive this as a large phase error so that it can contribute to the speed-up process. If the dead zone in the auxiliary PFD is larger then 9 degree, the auxiliary path has no effect what so ever even during the frequency transition and there is no improvement in settling time. In order to have an optimum dead zone width with such fine resolution, it is necessary

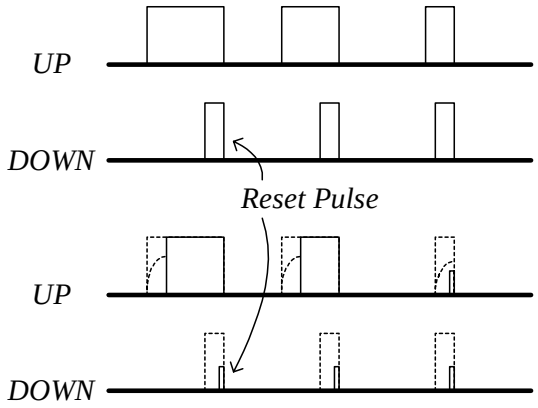


Fig. 63. The operation of the dead zone PFD

to have a tuning mechanism to counter the uncertainties due to process variation.

The proposed architecture of the PFD with dead zone width control is shown in Fig. 62. It is based on conventional digital implementation of PFD. But it has reduced reset pulse length due to reset pulse cancellation circuit. Dead zone is implemented by variable capacitors that increases rising time of the $UP/DOWN$ pulses. The operation is depicted in Fig. 63. The top set of $UP/DOWN$ pulses are from conventional PFD, and the bottom set of pulses are from dead zone PFD. In the dead zone PFD, the rising time is slower than the conventional one. Thus when the phase error is large, it generates narrower pulses compared to conventional PFD. Once the phase error drops below the dead zone width, the pulse become so narrow that it cannot rise high enough to turn on next gate. This effectively makes the dead zone PFD out of operation.

The width of the dead zone can be tuned through a 3-bit digitally programmable capacitor bank. The width of the dead zone also has a critical effect on the stability and the speed-up performance of the synthesizer. If the dead zone width is too narrow, the speed-up effect of the auxiliary path would be too pronounced and make the loop unstable. On the other hand, if the dead zone width is too wide, the effect

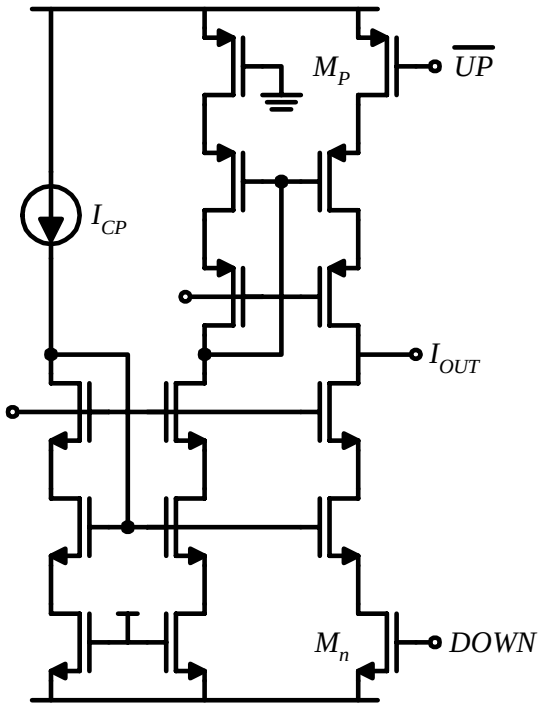
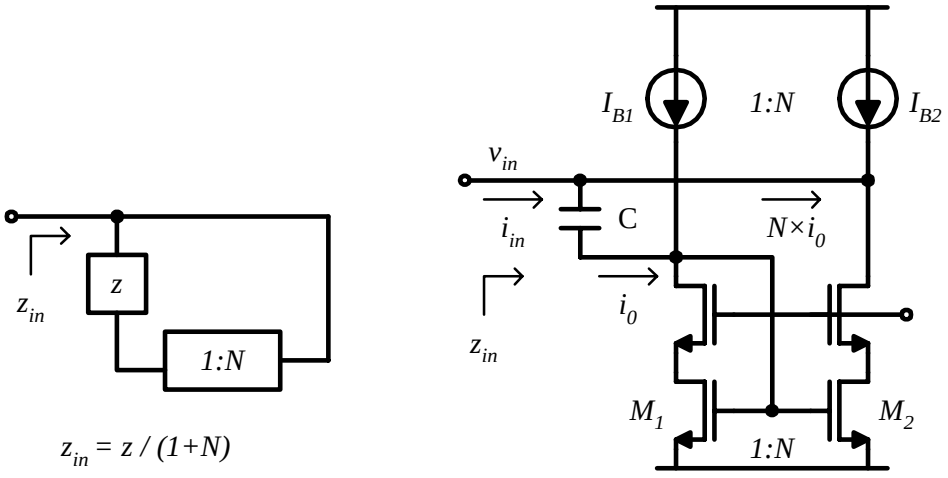


Fig. 64. Cascode charge pump

of the auxiliary path would be not enough to speed-up the settling of the synthesizer considerably. The proposed PFD with dead zone width control makes it possible to optimize the dead zone width by tuning it off-line. It can be done by testing the settling time performance of the stand alone frequency synthesizer before turning on the whole receiver. The tuning is required only once per chip since the process variation is the main source of the uncertainty. Once tuned, no switching is necessary during a normal operation.

2. Charge Pump

The PFD is followed by a charge pump shown in Fig. 64, with a cascode output. The cascode transistors provide a larger output resistance that reduces the output voltage dependence of the output current. Switches M_p and M_n are sized to reduce the current



(a) (b)

Fig. 65. Active capacitance multiplier. (a) Conceptual diagram (b) Circuit implementation with bias

mismatch and switching time of the charge pump. The charge pump currents of the narrow-bandwidth main path and wide-bandwidth auxiliary path (I_{CP1} and I_{CP2} in Fig. 61) are 9.7 μA and 197 μA, respectively. This is a factor of nearly 20. The choice of CP currents is intimately related to the values of the loop filter components and stability considerations. Details of the loop filter design are presented in section D-4.

3. Capacitance Multiplier

Before discussing the loop filter, how to obtain a large capacitance in small area is discussed. It is critical because the loop bandwidth has to be very low to obtain high spur rejection, requiring a very large capacitance.

The principle of active capacitance multiplication is shown in Fig. 65 [76]. The current i_0 flowing through capacitor C is mirrored with a ratio of $1 : N$ by M_2 and subtracted from the input node. This extra current extraction (Ni_0) is seen from the input as larger total current variation for a given input voltage, or equivalently a

lower input impedance. The impedance seen from the input port z_{in} equals,

$$z_{in} = \frac{v_{in}}{i_0 + Ni_0} = \frac{v_{in}}{sCv_{in} + sCNv_{in}} = \frac{1}{sC(1+N)} \tag{5.4}$$

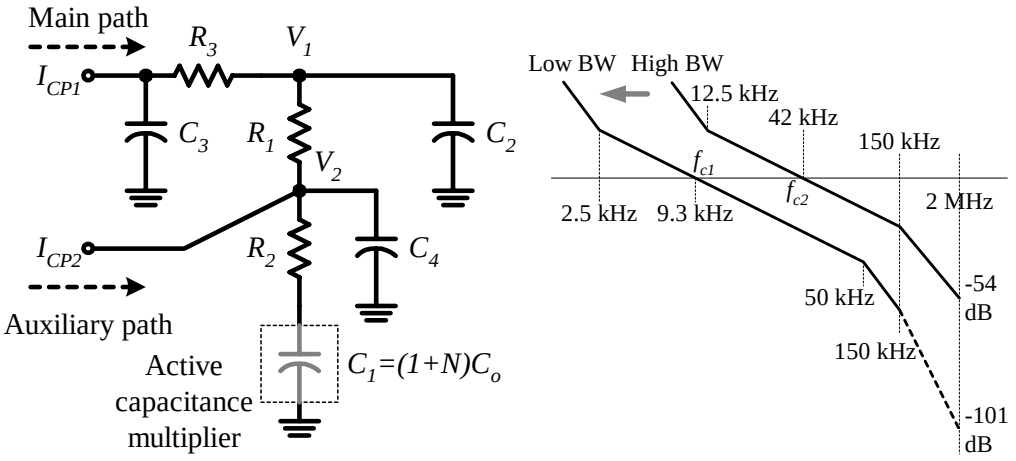
Equation (5.4) shows that the effective capacitance is multiplied by a factor of $(1 + N)$.

Leakage current at the input of the capacitance multiplier due to finite output impedance can be a problem in the capacitance multiplier [16]. However, the attenuation of the loop filter at the reference frequency is kept large enough such that the effect of the leakage current on the reference spurs is minimized. Also, a large transistor length and small bias current are used to help reduce the amount of leakage current.

4. Loop Filter

The loop filter is the most important block in this PLL design because it determines the characteristics of closed loop behavior on both operation modes: locked state and frequency transition. Settling time and spur rejection depend on loop bandwidth. Measurement results from previous designs [67, 68] showed that a 36 kHz loop bandwidth is wide enough for the synthesizer to meet the settling time requirement but so wide that it does not provides adequate rejection for spurious signals. It is not possible to further reduce the loop bandwidth since it would prevent the loop from meeting the settling time requirement.

An adaptive dual loop scheme solves this dilemma by featuring a loop filter that can change its bandwidth and stability consideration depending on the operation mode. To avoid the glitch problem, there is no switch in the loop filter to discretely alter the value of its passive elements. The loop filter changes its transfer characteristic by gradually shifting which combinations of its two input ports receive current



(a) (b)

Fig. 66. Dual bandwidth loop filer. (a) Schematic of dual bandwidth loop filter with active capacitance multiplier (b) Bode plot of $H_{main}(s)$ and $H_{aux}(s)$ shows transition of transfer function

pulses from charge pump outputs.

The circuit implementation of the proposed loop filter is shown in Fig. 66(a). Two different open loop transfer function can be derived by substituting the loop filter into the ADPLL system shown in Fig. 61. One is a transfer function following the main path of the loop, which has narrow bandwidth for high spur rejection. The other is a transfer function following the auxiliary path of the loop, which has wide bandwidth for settling time speed-up.

The main path has a charge pump current I_{CP1}. The effect of the auxiliary path can be ignored for now by assuming $I_{CP2} = 0$. The transimpedance from I_{CP1} to note V_1 is,

$$Z_{main}(s) = \frac{V_1}{I_{CP1}}\bigg|_{I_{CP2}=0} \simeq \frac{1 + s(R_1 + R_2)C_1}{C_1 s(1 + s(R_1 + R_2)C_2)(1 + sR_3C_3)(1 + sR_2C_4)} \quad (5.5)$$

Using the above equation, the open loop transfer function of the main path calculated

from Fig. 61 is,

$$H_{main}(s) = \frac{\phi_{out}}{\phi_{in}} \simeq \frac{K_o I_{CP1}(1 + s(R_1 + R_2)C_1)}{2\pi N C_1 s^2 (1 + s(R_1 + R_2)C_2)(1 + sR_3C_3)(1 + sR_2C_4)} \tag{5.6}$$

where K_o is the VCO gain. Similarly, the auxiliary path has a charge pump current I_{CP2}. The transimpedance from I_{CP2} to note V_1 is,

$$Z_{aux}(s) = \left.\frac{V_1}{I_{CP2}}\right|_{I_{CP1}=0} \simeq \frac{1 + sR_2C_1}{C_1 s(1 + s(R_1 + R_2)C_2)(1 + sR_2C_4)} \tag{5.7}$$

Using the above equation, the open loop transfer function of the auxiliary path is,

$$H_{aux}(s) = \frac{\phi_{out}}{\phi_{in}} \simeq \frac{K_o I_{CP2}(1 + sR_2C_1)}{2\pi N C_1 s^2 (1 + s(R_1 + R_2)C_2)(1 + sR_2C_4)} \tag{5.8}$$

Note that not only $H_{main}(s)$ has an additional pole at $1/R_3C_3$, but it also has a zero at the frequency of $1/(R_1 + R_2)C_1$ – lower than that of $H_{aux}(s)$. Observe that by using a factor of 3 for the separations between pole/zero and crossover frequency, it is ensured that the damping factor of the closed loop transfer function is larger then 0.8, so that the overshoot in transient response does not cause serious problem. A factor of 4 makes the loop critically damped. Stability constraints can be met by following the guidelines described below.

1. Low bandwidth loop

   (a) Zero at $1/(R_1 + R_2)C_1$ has to be at least 3 times lower than crossover frequency (f_{c_1}).

   (b) Pole at $1/R_3C_3$ has to be at least 3 times higher than crossover frequency (f_{c_1}).

   (c) Additional pole at $1/(R_1 + R_2)C_2$ has to be at least 3 time higher than pole frequency.

2. High bandwidth loop

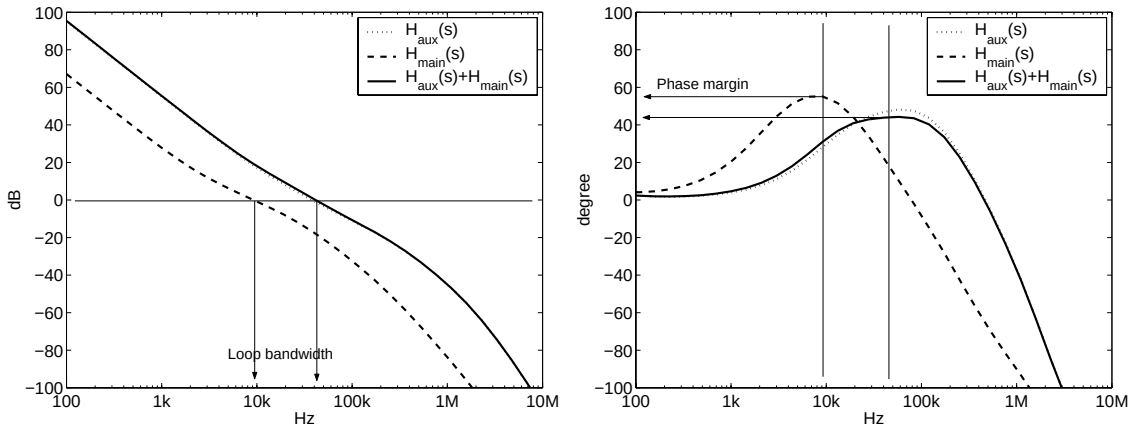
   (a) Zero at $1/R_2C_1$ has be at least 3 times lower than crossover frequency (f_{c_2}).

   (b) Pole at $1/(R_1 + R_2)C_2$ has to be at least 3 times higher than crossover frequency (f_{c_2}).

Fig. 66(b) shows the actual locations of poles and zeros for this implementation. Only the main path is active in steady state operation and the loop bandwidth is kept narrow at 9.3 kHz. At the beginning of a frequency transition, if the phase error is larger than the width of the dead zone specified by the PFD in the auxiliary path, both PFD's produce UP/DOWN pulses. In this case, both the main and the auxiliary path becomes active and the loop bandwidth is pushed to 42 kHz for faster settling. Since both paths are active, the equivalent total transfer function of the loop filter is the addition of $H_{main}(s)$ and $H_{aux}(s)$. However, since the charge pump output current of the auxiliary path (I_{CP2}) is much larger than the output current of the main path (I_{CP1}), the transfer function of the wide bandwidth path, $H_{aux}(s)$ has a dominant effect on the loop. The total transfer function can be expressed as,

$$H_{total}(s) = \begin{cases} H_{main}(s) & \text{when in steady state} \\ H_{main}(s) + H_{aux}(s) \simeq H_{aux}(s) & \text{when in transition} \end{cases} \tag{5.9}$$

As the phase error gets smaller, it becomes comparable to the width of the dead zone. The auxiliary loop PFD stops producing any output once the phase error drops below the dead zone limit and it does not have an effect on the loop anymore. The loop gradually shifts back to narrow bandwidth transfer function, so that it can have more rejection for spurious signals. In this implementation spur rejection performance at 2 MHz is improved by 47 dB.



(a) (b)

Fig. 67. Simulation result of open loop transfer functions $H_{main}(s)$ and $H_{aux}(s)$. (a) Magnitude (b) Phase

The actual simulation result of the open loop transfer function of the main and the auxiliary loop is shown in Fig. 67. The broken line is $H_{main}(s)$, the dotted line is $H_{aux}(s)$, and the solid line is $H_{main}(s) + H_{aux}(s)$. As expected, $H_{main}(s) + H_{aux}(s)$ is dominated by $H_{aux}(s)$. The phase waveform in Fig. 67(b) shows the phase margin of $H_{main}(s)$ is higher than that of $H_{aux}(s)$ for better stability.

Note that C_4 in Fig. 66(a) is seemingly unimportant since it does not have a significant contribution to the transfer functions. However, it is essential for filtering non-linear pulsed current from the charge pumps preceding the loop filter as shown in Fig. 68. With C_4 of 1 pF, the voltage peak is larger than 0.5 V. Once C_4 is increased to 10 pF, the peak is decreased below 0.1 V. Care should be taken to suppress such voltage peaks since the effect of C_4 only appears as a high frequency pole in the linear model in equation (5.6) and (5.8). Only rigorous circuit simulation can accurately predict its detrimental effect. While a large value of C_4 provides better filtering, it should be small enough so that its effect does not degrade the overall phase margin.

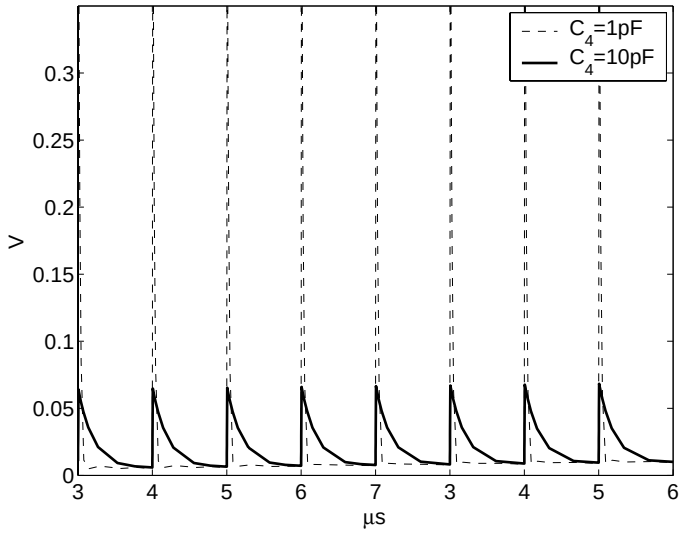


Fig. 68. Voltage peaks on V_2 node in Fig. 66(a) due to pulsed current output from the charge pump

Finally the parameters of the PLL design is summarized in Table XIV. The bandwidth of the main loop is kept at 9.3 kHz while the largest passive capacitor is only 39 pF. The active capacitance multiplier makes the effective capacitance as large as 975 pF. All the passive elements are integrated on-chip.

It is worthwhile to verify how much of die area is saved by utilizing the active capacitance multiplier. The chosen process technology, IBM6HP BiCMOS, has a metal-insulator-metal (MIM) capacitance density of 0.7 fF/μm^2. Thus 975 pF capacitor would occupy 975 pF/0.7 fF/μm^2 $\simeq$ 1.4 mm^2. The active capacitance multiplier with 39 pF passive capacitor occupies 0.06 mm^2, which is only 4.3% of the are 975 pF capacitor would consume. This shows that the active capacitance multiplier is an essential part of implementing a low-spur frequency synthesizer based on reduced loop bandwidth. Without it, the proposed solution for spur rejection becomes very expensive because of the increased overhead in die area.

Table XIV. PLL design parameters

	Auxiliary loop	Main loop
Loop bandwidth	42 kHz	9.3 kHz
f_{zero}	12.5 kHz	2.5 kHz
f_{pole}	150 kHz	150 kHz, 50 kHz
Phase margin	47°	55°
I_{cp}	197 μA	7.9 μA
Passive elements	R_1	51 kΩ
	R_2	12.7 kΩ
	R_3	95.5 kΩ
	C_1	39 pF × 25
	C_2	16.7 pF
	C_3	33.4 pF
	C_4	10 pF

5. VCO

The VCO is implemented with a LC-tuned negative-gm oscillator as shown in Fig. 69. The details of the VCO design has been covered in section IV-F. BiCMOS technology provides some unique options for designing the passive tank elements. Special low-resistance, top-metal layer is utilized for the on-chip inductor. Simulated quality factor of the 1.5 nH inductor is 13. The intrinsic base-collector diode of a bipolar device is used as a varactor, which provides a ±17% capacitor variation range. The varactor can provide the VCO with 760 MHz of tuning range; wide enough for both standards individually but not both at the same time. Discretely programmable capacitor banks are present to switch modes between the two standards. Once the

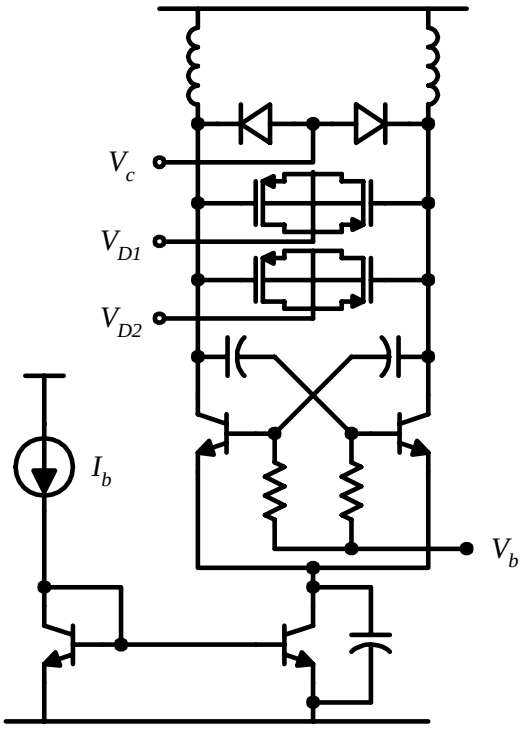


Fig. 69. Schematic of VCO

mode is set, there is no on-line switching involved during the channel transition.

Several measures have been taken to meet the phase noise requirement. Base nodes of the bipolar transistor drivers are AC-coupled with oscillating nodes and biased by an extra DC biasing circuit to keep the transistors in the active region. Although the biasing circuit increases the effective base resistance, improved linearity helps to reduce the overall phase noise. A bypass capacitor on the common emitter node reduces the noise contribution of the current bias transistors [66].

6. Prescaler

A 15/16 dual-modulus phase switching prescaler follows the VCO. The prescaler is comprised of three stages of cascaded asynchronous dividers, an 8-to-1 multiplexer, phase selection circuitry and a final divide-by-two stage, as shown in Fig. 70. The

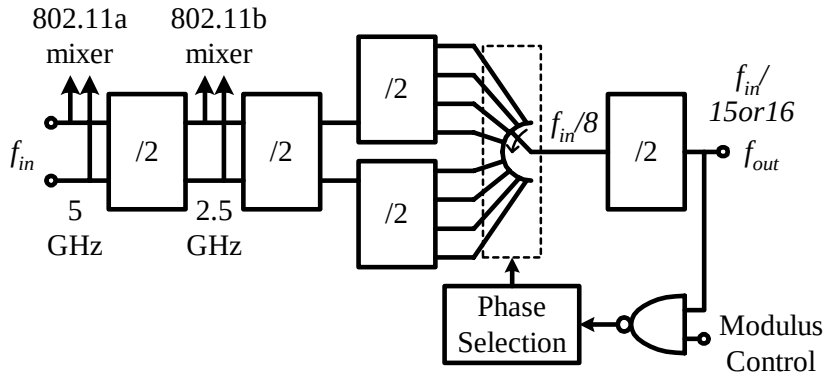


Fig. 70. 15/16 phase switching prescaler block diagram

output of the VCO itself provides the local signal for 802.11a standard at 5 GHz range. The output of the first asynchronous divider provides the local signal for 802.11b standard at 2.4 GHz range. The use of asynchronous frequency dividers reduces the power consumption of the prescaler compared to conventional dividers operating at the same frequency [63].

The output of the third stage of dividers generate eight phases separated by a 45° each at a frequency corresponding to 1/8 of the VCO frequency. By controlling the sequence of phase selection switching block, the divider can perform either divide-by-16 operation or divide-by-15 operation.

E. Testing and Measurement

The proposed synthesizer was fabricated through MOSIS in a 0.25-μm BiCMOS process. Fig. 71 shows the microphotograph of the fabricated chip. The synthesizer dissipates 70 mW from a single 2.5 V supply including all the biasing circuits on the PCB, and occupies a chip area of 1.7 mm^2. An effective capacitance of 975 pF is implemented with the active capacitance multiplier occupying only 0.06 mm^2 of die area with minimal overhead on power consumption; the bias current needed for the

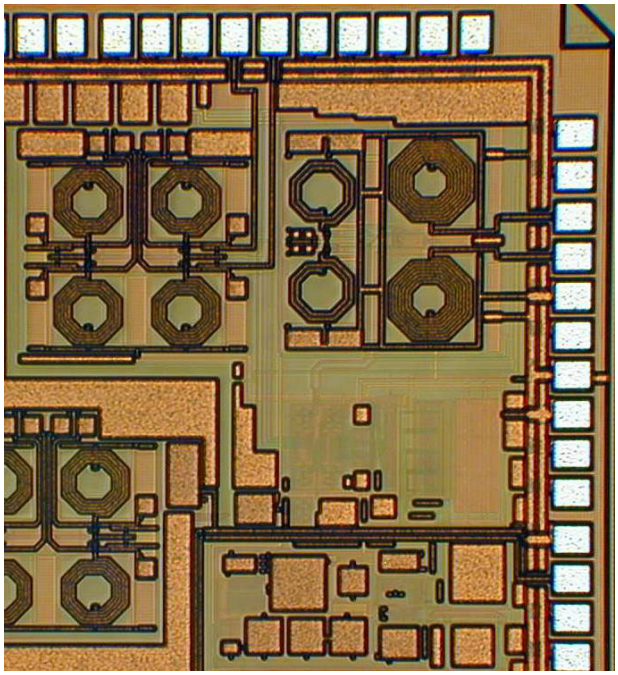


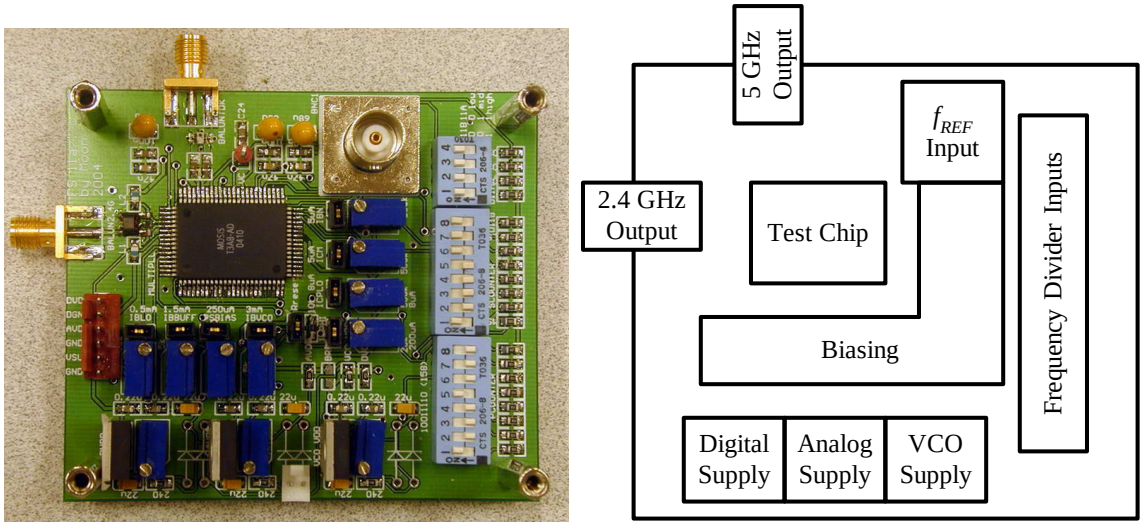
Fig. 71. Chip microphotograph of the multi-standard frequency synthesizer

capacitance multiplier is 10 μA.

1. Printed Circuit Board (PCB) Design

An exclusive PCB is designed and fabricated for measurement of the chip. A photo shot of the PCB is shown in Fig. 72(a). Block diagram shown in Fig. 72(b) presents general features of the PCB. On the bottom portion, there are three variable voltage regulators to supply the digital blocks, the VCO, and the rest of the analog blocks separately. The separation of the digital and the analog power supply prevents the supply noise of the digital blocks from degrading the sensitive analog blocks. Among the analog blocks, the VCO is separated from the rest. It has been reported in [77] that an integrated voltage regulator dedicated for VCO supply can improve the performance of the VCO.

The test chip is placed close to the top left corner so that the critical interconnects



(a) (b)

Fig. 72. PCB for the multi-standard synthesizer testing. (a) Photo shot (b) Block diagram

for RF output can be as short as possible. Differential outputs from the chip is converted to single ended signals by passive baluns placed next to the output pins. 2.4 GHz and 5 GHz outputs need different types of balun because transformer used as the balun has a narrow band characteristic.

Simple current biasing circuits are composed of 8 pairs of 18-turn potentiometers and shorting jumpers for current measurement. High turn potentiometers are required for precise current adjustment.

On the righthand side, a series of DIP switches set the digital input words for several blocks including; low frequency counters as part of frequency divider, VCO coarse tuning for band selection between 802.11a and 802.11b, dead zone width control of the auxiliary PFD.

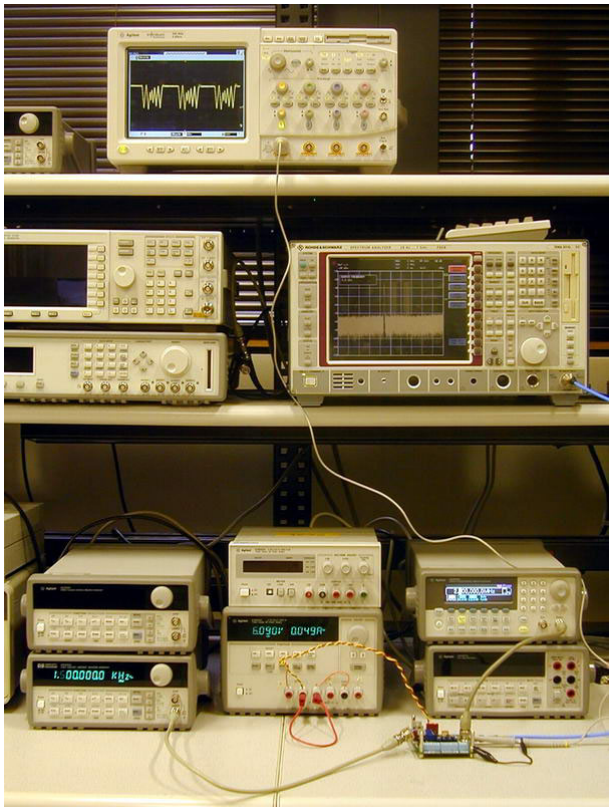


Fig. 73. Testing bench setup

2. Testing Setup

Testing bench setup is shown in Fig. 73. The equipments used in the testing are listed below.

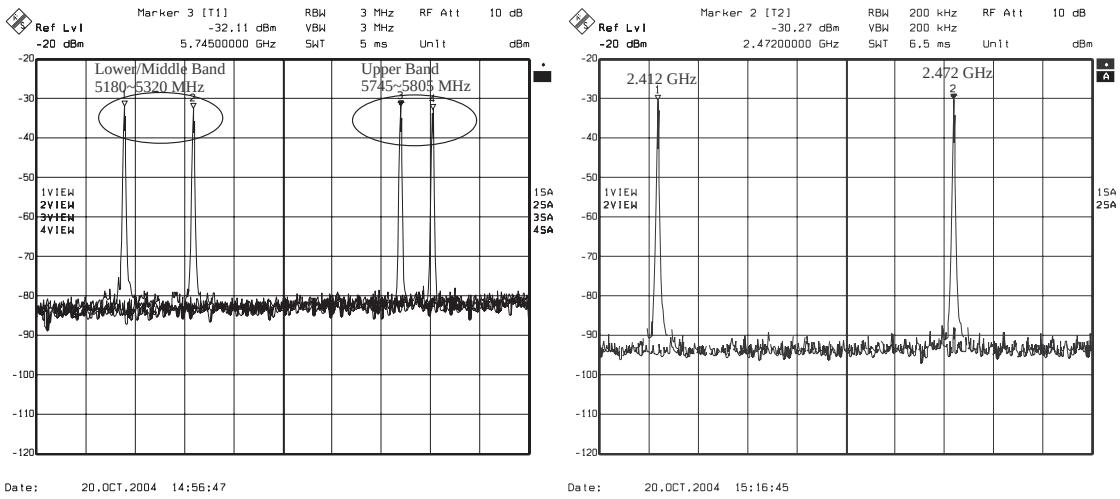
- Agilent Infiniium Oscilloscope (on the top shelf) for settling time measurement
- Rohde & Schwarz FSEB Spectrum analyzer (on the middle shelf) for output power spectrum measurement
- Agilent 33250A Function Generator (on the bench, right) for reference frequency source
- HP 33120A Function Generator (on the bench, left) for hopping channel center

frequency

- Agilent E3631A Power Supply (on the bench, middle)

3. Measurement Results

First, the tuning range of the frequency synthesizer is measured by the spectrum analyzer. The carrier center frequency is synthesized from the lowest channel to the highest.

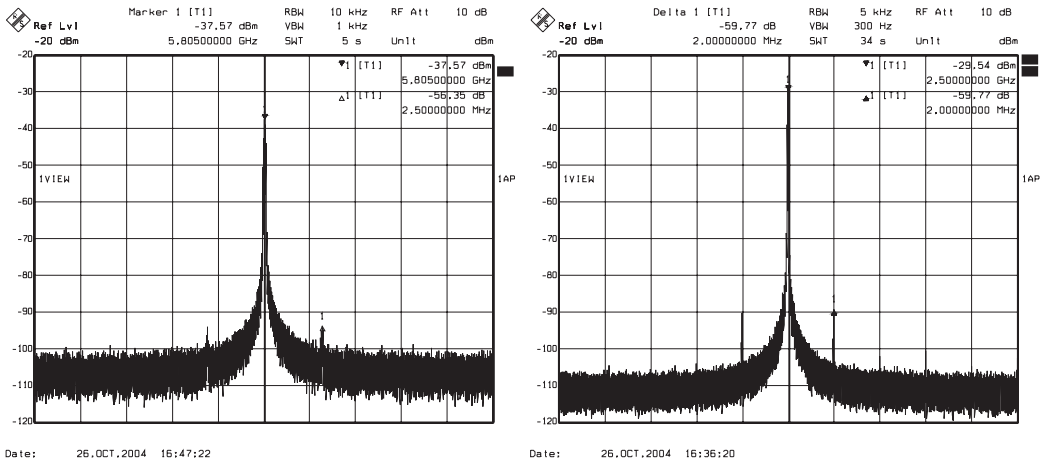


(a) (b)

Fig. 74. Measured tuning range. (a) 802.11a (b) 802.11b

Fig. 74(a) shows the tuning range of the synthesizer in 802.11a mode. 802.11a standard specifies three separate bands; U-NII lower band (5180–5240 MHz), U-NII middle band (5260–5320 GHz), and U-NII upper band (5745–5805 MHz). The result shows that the synthesizer can generate all the center frequencies required by the standard. Fig. 74(b) shows the tuning range in 802.11b mode. Changing modes between 802.11a and 802.11b is done by digital input bits. The effective size of the varactor in the VCO is increased so that the free running frequency of the VCO can

cover 4824–4944 MHz range. The output for 802.11b mode is generated by a divide-by-two circuit, which makes the frequency coverage from 2412 MHz to 2472 MHz. The result also shows a full coverage of the required center frequencies.



(a) (b)

Fig. 75. Measured output spectra. (a) 802.11a at 5.805 GHz (b) 802.11b at 2.500 GHz

The next measurement shows the reference spur rejection performance of the synthesizer. Fig. 75(a) and (b) shows the spectrum of the output signal for 802.11a at 5.805 GHz, and for 802.11b at 2.500 GHz respectively. The reference spurs are 56 dB below carrier at an offset of 2.5 MHz for 5.805 GHz output, and 59 dB below carrier at an offset frequency of 2 MHz for 2.500 GHz output. The reference spur is lower for the 2.500 GHz output even though the reference signal is closer to the carrier. This is because the 2.500 GHz output is produced by dividing 5 GHz signal by two, that results in 6 dB reduction of the modulated spurious signals including reference spurs and phase noise.

The reference spurs can be increased intentionally by disabling the main path of the ADPLL. With only the auxiliary path active, the loop should be unstable theoretically. In the testing session, the PLL lost its locked state occasionally in

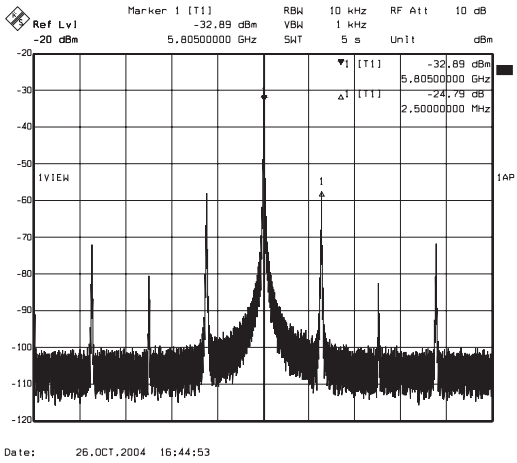


Fig. 76. High reference spurs are generated by disabling the main path

random incidents and had to reacquire the locked state. However, it was possible to measure a output spectrum as long as the center frequency is not actively changed by frequency hopping input. Fig. 76 shows the output spectrum with increased reference spurs for 802.11a mode. The spurious tones are increased by 31 dB, resulting at 25 dB below the carrier signal. Note that along with the increased fundamental term of the reference spur, the third harmonic term become significant in the high spur measurement.

Fig. 77. Settling time measurements with and without the auxiliary loop for speed-up

The settling behavior of the synthesizer is studied by observing the waveform of the VCO control voltage during a frequency transition. Fig. 77 shows a settling time of about 80 μs. The effective loop bandwidth of this settling time is 42 kHz as shown in Fig. 66(b). The figure also shows that the settling time is increased to about 250 μs when the high bandwidth loop is disabled. It can be done by disabling the auxiliary path. Unlike disabling the main path, it does not involve stability problem. The slow slope in Fig. 77 clearly shows that it can settle with no problem when the output frequency is changed. The effective loop bandwidth of 250 μs settling is 9.3 kHz.

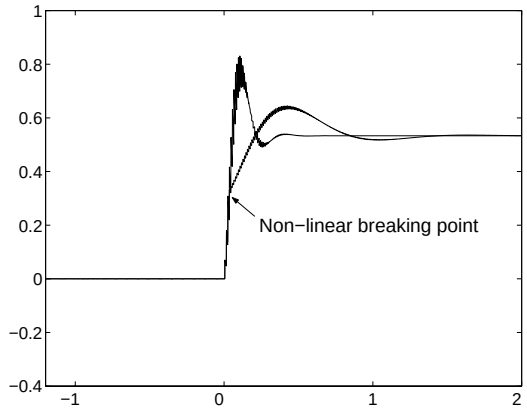


Fig. 78. Simulation result of a non-linear slow response

It is worthwhile to note that the slow response shown in Fig. 77 has very non-linear characteristic. At the beginning of the transition, the waveform rises as fast as the fast response. Then it is abruptly slowed down and follows a conventional characteristic of a slow linear step response. It seems as if the auxiliary path still can affect the transient response even when it is disabled by removing the bias current of the auxiliary charge pump. When the phase error is very large at the beginning of a transition, the dead zone PFD can generate pulses that can be capacitively coupled to the output of the charge pump, even when the charge pump is not active. Once the

phase error gets low enough, the effect of the capacitive coupling become insignificant to the overall response of the loop. A simulation result on Matlab model is shown in Fig. 78. Both the main and auxiliary path is active until the transient waveform reaches 0.3 V, and then only the main loop is active during the rest of the transition. Reduced bandwidth of the main loop slows down the transition considerably after the initial jump. However, this should not affect the normal operation of the ADPLL when both main and auxiliary charge pump are active.

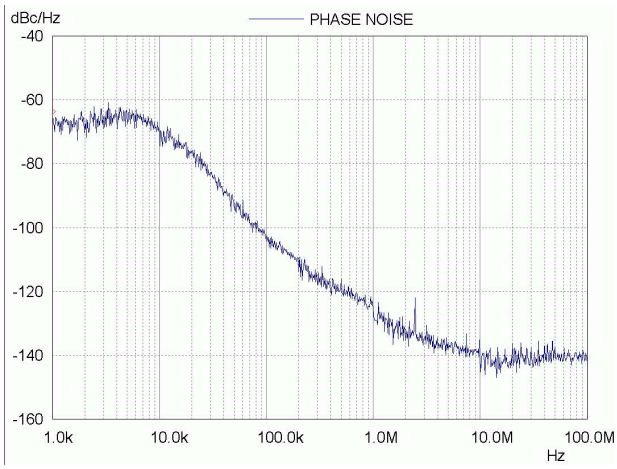
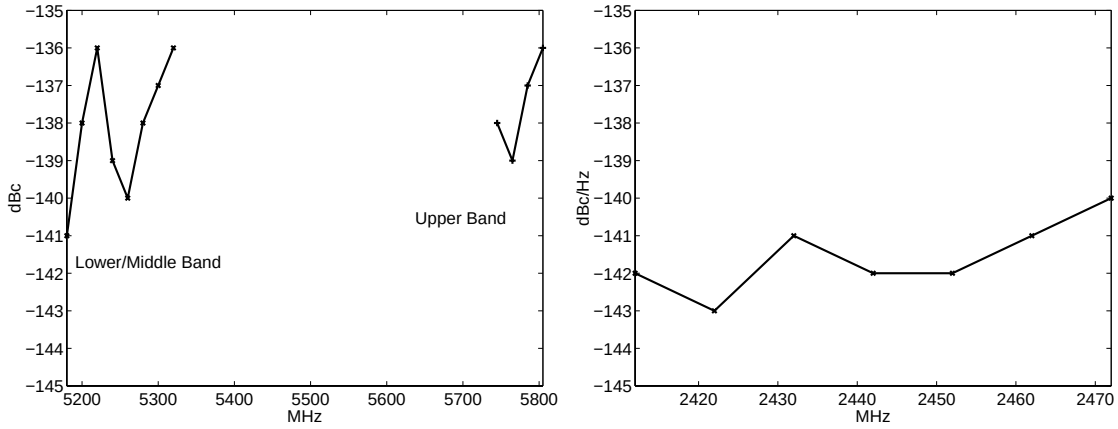


Fig. 79. A sample phase noise measurement

The phase noise is measured for every carrier frequency required in both standards. A sample of phase noise measurement result is shown in Fig. 79. The phase noise measurement environment is same as described in the previous chapter section IV-8. Measured results are summarized in Fig. 80. For 802.11a, the phase noise spans from -141 to -136 dBc/Hz at 40 MHz offset frequency. For 802.11b, the phase noise performance is better, spanning from -143 to -140 dBc/Hz at 25 MHz offset frequency. This is due to the same reason as aforementioned 6 dB reduction of modulated spurious signals by divide-by-two operation. Finally, the measurement results are summarized in Table XV.



(a) (b)

Fig. 80. Phase noise of each channel carrier. (a) 802.11a (b) 802.11b

Table XV. Measurement results summary

	802.11a	802.11b
Tuning range	5180 $\sim$ 5805 MHz	2412 $\sim$ 2472 MHz
Spurs	-56 dBc at 2.5 MHz	-59 dBc at 2 MHz
Settling time	$\simeq 80$ μs	< 80 μs
Phase noise	$-141 \sim -136$ dBc/Hz at 40 MHz offset	$-143 \sim -140$ dBc/Hz at 25 MHz offset

CHAPTER VI

CONCLUSIONS

In this dissertation we discussed a design procedure of frequency synthesizers and proposed an improved circuit architecture for better performance. We demonstrated the design of a multi-standard frequency synthesizer for WLAN application, covering from the interpretation of standards to the testing and measurements.

A new methodology of interpreting communication standards into low level circuit specifications was developed to clarify how the requirements are calculated. The highlighted parameters included: phase noise, settling time, and spurious rejection. We studied two Wireless LAN standards, 802.11a and 802.11b, using the new methodology, and clearly defined the requirements to be met by circuit implementations.

Once the requirements were specified, we presented a detailed procedure to determine important design variables from the specifications. The procedure incorporated the fundamental theory such as stability and settling time of feedback system, and non-ideal effects such as phase noise and reference spurs. The design procedure can be easily adopted for different applications and is not limited to WLAN application.

A BiCMOS frequency synthesizer compliant for both WLAN 802.11a and 802.11b standards was presented as a design example. An integer-N architecture was chosen for optimal performance in area and power consumption. However, satisfying both standards imposed stringent design requirements due to the limitations of the integer-N architecture. An improved adaptive dual-loop PLL architecture with a new loop filter topology and a tunable dead zone was proposed to improve reference spur rejection and settling time performance.

The improvements made it possible to implement an integer-N type synthesizer with a reference frequency of as low as 2 MHz, while keeping the reference spurs and

settling time within specification. The synthesizer is fabricated in a 0.25 μm BiCMOS process and dissipates 70 mW from a single 2.5 V supply, and it occupies a silicon area of 1.7 mm^2. Test-chip measurement results show -56 dBc reference spurs at a frequency offset of 2 MHz, thanks to a very low loop bandwidth of 9.3 kHz, which is realized with an effective capacitance of 975 pF occupying only 0.06 mm^2 of chip area. Even with the low loop bandwidth, the speed-up effect of the adaptive dual loop PLL kept the settling time close to 80 μs.

We demonstrated that the proposed architecture could extend the operation limit of conventional integer-N type synthesizers. The new architecture made it viable to use integer-N synthesizers for more demanding applications, including a multi-standard WLAN transceiver. It opened new opportunities of designing high performance frequency synthesizers. The most attractive benefit of the new architecture is that it maintains the benefit of the integer-N architecture with minimal cost in chip area and power consumption.

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APPENDIX A

ROUTH-HURWITZ STABILITY CRITERION

The Routh-Hurwitz stability criterion is a method for determining whether or not a system is stable based upon the coefficients in the system's characteristic equation. It is particularly useful for higher-order systems because it does not require the polynomial expressions in the transfer function to be factored.

The procedure for using the Routh-Hurwitz criterion is as follows:

1. Write the characteristic equation (a polynomial in s) in the following form:

$$a_0 s^n + a_1 s^{n-1} + \ldots + a_{n-1} s + a_n = 0$$

2. If any of the coefficients are zero or negative and at least one of the coefficients are positive, there is a root or roots that are imaginary or that have positive real parts. Therefore, the system is unstable.

3. If all coefficients are positive, arrange the coefficients in rows and columns in the following pattern:

$$\begin{array}{cccccc}
s^n & a_0 & a_2 & a_4 & a_6 & \cdots \\
s^{n-1} & a_1 & a_3 & a_5 & a_7 & \cdots \\
s^{n-2} & b_1 & b_2 & b_3 & b_4 & \cdots \\
s^{n-3} & c_1 & c_2 & c_3 & c_4 & \cdots \\
s^{n-4} & d_1 & d_2 & d_3 & d_4 & \cdots \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots
\end{array}$$

$$\begin{array}{ll} s^2 & e_1 \quad e_2 \\ s^1 & f_1 \\ s^0 & g_1 \end{array}$$

where the coefficients are:

$$\begin{array}{lll} b_1 = \dfrac{a_1 a_2 - a_0 a_3}{a_1}, & b_2 = \dfrac{a_1 a_4 - a_0 a_5}{a_1}, & b_3 = \dfrac{a_1 a_6 - a_0 a_7}{a_1} \quad \cdots \\ c_1 = \dfrac{b_1 a_3 - a_1 b_2}{b_1}, & c_2 = \dfrac{b_1 a_5 - a_1 b_3}{b_1}, & c_3 = \dfrac{b_1 a_7 - a_1 b_4}{b_1} \quad \cdots \\ d_1 = \dfrac{c_1 b_2 - b_1 c_2}{c_1}, & d_2 = \dfrac{c_1 b_3 - b_1 c_3}{c_1}, & \cdots \end{array}$$

The Routh-Hurwitz stability criterion states that the number of roots with positive real parts is equal to the number of changes in sign of the coefficients in the first column of the matrix. Note that the exact values are not required for the coefficients; only the sign matters.

If a system is stable (all of its poles are in the left half of the complex plane), then all the coefficients a_i must be positive and all terms in the first column of the matrix must be positive.

For example, given a system with characteristic equation

$$a_2 s^2 + a_1 s + a_0 = 0$$

we can determine which values of a_i will make the system stable and which will make the system unstable.

Arranged in matrix form, the coefficients are

$$\begin{array}{lll} s^2 & a_2 & a_0 \\ s & a_1 & \\ 1 & a_1 a_0 / a_2 & \end{array}$$

The Routh-Hurwitz criterion states that all of the coefficients in the first column of coefficients must be positive, so for this case we must have $a_2 > 0$ and $a_1 > 0$. Since a_2 and a_1 are positive, a_0 must be greater than 0 as well.

As another example, consider the system with characteristic equation

$$s^3 + s^2 + 2s + 24 = 0$$

Arranged in matrix form, the coefficients are

$$\begin{array}{cc} s^3 & 1 \quad 2 \\ s^2 & 1 \quad 24 \\ s & -22 \\ 1 & 24 \end{array}$$

Since at least one of the coefficients (-22) is less than zero, this system is unstable. In fact, it has two roots in the right half-plane.

In the case of the third-order closed-loop transfer function of PLL as shown in equation (3.6), the characteristic equation is

$$s^3/(\omega_p K_D K_o) + s^2/(K_D K_o) + s/\omega_z + 1 = 0 \tag{A.1}$$

The coefficients matrix is;

$$\begin{array}{cc} s^3 & 1/(\omega_p K_D K_o) \quad 1/\omega_z \\ s^2 & 1/(K_D K_o) \quad 1 \\ s & 1/\omega_z - 1/\omega_p \\ 1 & 1 \end{array}$$

In order to make this system stable, all of the coefficients in the first column of coefficients must be positive. Thus the condition when the PLL is stable can be

derived as,

$$\omega_p > \omega_z \tag{A.2}$$

which states and the frequency of the additional pole must be higher then the frequency of the stabilizing zero.

APPENDIX B

GARDNER'S STABILITY LIMIT

Linearized PLL model is based on averaged-response, time-continuous, constant-element operation of the loop. There are features arising from the actual discontinuous operation that need attention, even for narrow bandwidths. In some sense, the loop operates on a sampled basis and not as a straightforward continuous-time circuit. In particular, an analog, second-order PLL is unconditionally stable for any value of loop gain, but the sampled equivalent will go unstable if the gain is made too large.

The end result is the characteristic equation (denominator of the transfer function equation (3.7)) of the sampled PLL in the z-plane, which has the form

$$D(z) = (z-1)^2 + (z-1)\frac{2\pi\omega_z K'}{\omega_{REF}}(1 + \frac{2\pi\omega_z}{\omega_{REF}}) + \frac{4\pi^2\omega_z^2 K'}{\omega_{REF}^2} \tag{B.1}$$

where $K' = (\omega_n/\omega_z)^2$ may be regarded as a normalized loop gain, ω_{REF} is the input frequency, and ω_z is the filter zero frequency.

Transient response for small phase errors and loop stability are studied by examining the locations of the zeros of D(z) – the poles of the z-domain transfer function. The root locus shows pole locations in the z plane for varying K'; an example is sketched in Fig. 81. The shape of the locus is very similar to that of a conventional second-order loop in the s-plane.

The two poles start at $z = 1$ for $K' = 0$ and move on a circle with center at $z = (1 + 2\pi\omega_z/\omega_{REF})^{-1}$ for values of

$$K' < \frac{4}{(1 + 2\pi\omega_z/\omega_{REF})^2} \tag{B.2}$$

For larger K', the poles lie on the real axis; one pole migrates towards the center of the locus circle and the other migrates towards $-\infty$.

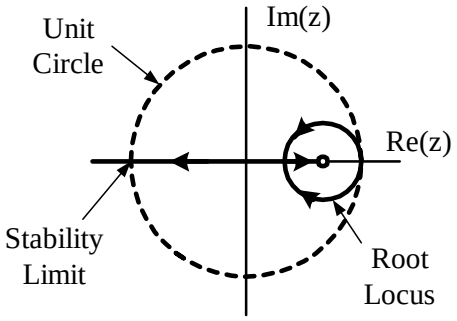

Fig. 81. Root locus plot of second-order loop in z-plane.

The loop is stable only if the poles lie inside the unit circle. Instability results where the outbound pole crosses the unit circle at $z = -1$, as noted in Fig. 81. Normalized gain at the crossing point is

$$K' = -\frac{1}{\frac{\pi\omega_z}{\omega_{REF}}\left(1+\frac{\pi\omega_z}{\omega_{REF}}\right)} \tag{B.3}$$

This value of K' is the stability limit. It can be rearranged by substituting K' with $(\omega_n/\omega_z)^2$, and the result is same as shown in equation (3.8).

We can observe the discrete-time domain behavior of the system from the inverse z-transform of equation (B.1). The partial fraction of the transfer function has a form of,

$$H(z) = \frac{a_1 z}{z-1+b_1} - \frac{a_1 z}{z-1+b_2} \tag{B.4}$$

where $a_1 \simeq \Omega_o\omega_z/\omega_n^2$, $b_1 \simeq 2\pi\omega_n^2(\pi+\omega_{REF}/\omega_z)/\omega_{REF}^2$, and $b_2 \simeq 2\pi^2\omega_n^2/\omega_{REF}^2$. Ω_o is an initial condition.

The inverse z-transform of equation B.4 is,

$$h(n) = a_1(1-b_1)^n - a_1(1-b_2)^n \tag{B.5}$$

Damping of the transient response depend on the range of the coefficient b_1 and b_2. When $0 < b_1, b_2 < 1$, the system is overdamped. The response is an exponential

decay. When $b_1 = b_2 = 1$, the system is critically damped. When $1 < b_1, b_2 < 2$, the system is underdamped and the response start to show oscillatory behavior since $(1 - b_x) < 0$. Once b_1 and b_2 reaches the value of 2, the system becomes unstable. The stability limit shown in equation (B.3) is obtained when $b_1 = 2$.

VITA

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