A SINGLE STAGE HIGH-FREQUENCY RECTIFIER FOR EV CHARGING APPLICATIONS

A Thesis

by

ERICK IVAN POOL MAZUN

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Chair of Committee,	Prasad Enjeti
Committee Members,	Mehrdad Ehsani
	Shankar P. Bhattacharyya
	Zhizhang Xie
Head of Department,	Miroslav Begovic

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ABSTRACT

In this work, a single-stage three-phase rectifier topology with high-frequency isolation for EV (Electric Vehicle) fast-charging stations is proposed. By using a multi-pulse approach, low-order harmonics in the input current are shown to be eliminated over a wide range. A SST (Solid State Transformer) is used to create a HF (High-frequency) galvanic isolation for the system with respect to the MV (Medium Voltage) grid. The proposed topology has the following advantages: no bulky DC-link capacitor, HF galvanic isolation, high power density, and simple control scheme. The novelty of the proposed topology is its low complexity, ease of control and robust operation due to it's inherited 12-pulse rectifier behavior. The approach is easily scalable to several hundreds of kilowatts and is ideal for driving high power Level-3 EV fast-charging stations. A simplified output voltage regulation scheme for the proposed topology is discussed. This output voltage regulation capability enables the circuit to be used as a single-stage topology for Level-3 charge stations with AC bus architecture. Furthermore, the topology can also be considered as an alternative to improve the power density in Level-3 charge stations with DC bus architectures. Experimental results on a scale down laboratory prototype at 208V, 2kW are discussed.

CONTRIBUTORS AND FUNDING SOURCES

The work in this dissertation was guided by the dissertation committee consisting of Professor Prasad Enjeti, Professor Mehrdad Ehsani, Professor Shankar P. Bhattacharyya from the Electrical and Computer Engineering Department, and Professor Zhizhang Xie from the Mathematics Department.

The development and design of the high-frequency transformer used in this work was done in collaboration with Dr. Ira J. Pitel from Magna-Power Inc. The circuits from the experimental prototype were built and design by myself at Magna-Power Inc. headquarters located at Flemington, New Jersey, USA.

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1. INTRODUCTION

1.1. Introduction

The global stock of electric cars surpassed 3 million marks in 2017. It expanded by 56% compared with 2016 according to the International Energy Agency (IEA) [1] as depicted in Figure 1-1.Taking into account the supportive polices and cost reductions outlook in the EV market, the number of light-duty vehicles on the road will reach 125 million by 2030. Moreover, urban buses are also experiencing a transition to electric drivetrains, which will increase a demand of Level-3 battery chargers [1]. It is clear that publicly accessible charger infrastructure will require a considerable growth to cover this energy demand during upcoming years.

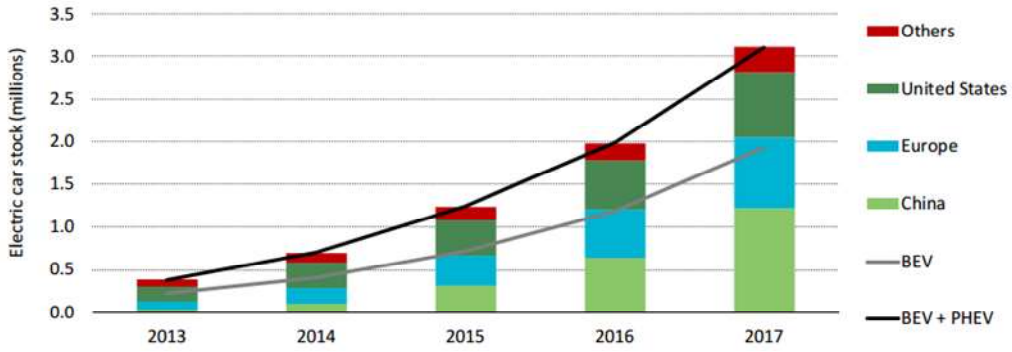

Figure 1-1 Global electric car stock, 2013-2017. Reprinted from [1]

Battery chargers for electrical vehicles can be performed thorough two general approaches On-board and Off-board. On-board approach consist on battery chargers located within vehicle's structure and is limited to slow charging; whereas, Off-board are mostly used for fast charge stations due to its higher power capabilities (>50 kW) [2,3].

Table 1-1 shows the classification of battery chargers depending of the power supplied. It can be noticed that battery chargers with power levels higher than 240 kW are considered within the Level-3 category. This type of battery charger is used to perform ultra-fast charging in off-board charging stations.

Table 1-1 Clasification of EV battery chargers according to its power level

Charge Method	Supplied DC Voltage Range (V)	Maximum Current (A)	Power Level (kW)
DC Level 1	200-450 V DC	≤ 80A DC	≤ 36 kW
DC Level 2	200-450 V DC	≤ 200A DC	≤ 90 kW
DC Level 3	200-600 V DC	≤ 400A DC	≤ 240 kW

Figure 1-2 provides an overview of the number of chargers deployed until 2017.It can be noticed an on-going trend of charging infrastructure from 2010 to 2017 for all types of chargers [1]. Furthermore, the number of public available chargers is considerably lower than private charging. Private charging stations are usually installed either at home or workplaces; thus, due to power limitations in household grid installations, these type of chargers are designed as AC Level-1 and Level-2 chargers as classified in Table 2.

To satisfy the high power demand, off-board battery chargers use three-phase MV utility input. depicts two system architectures for Level-3 battery charger stations. Fig 1-3(a) shows a common AC-link approach, where the MV utility is scaled down and

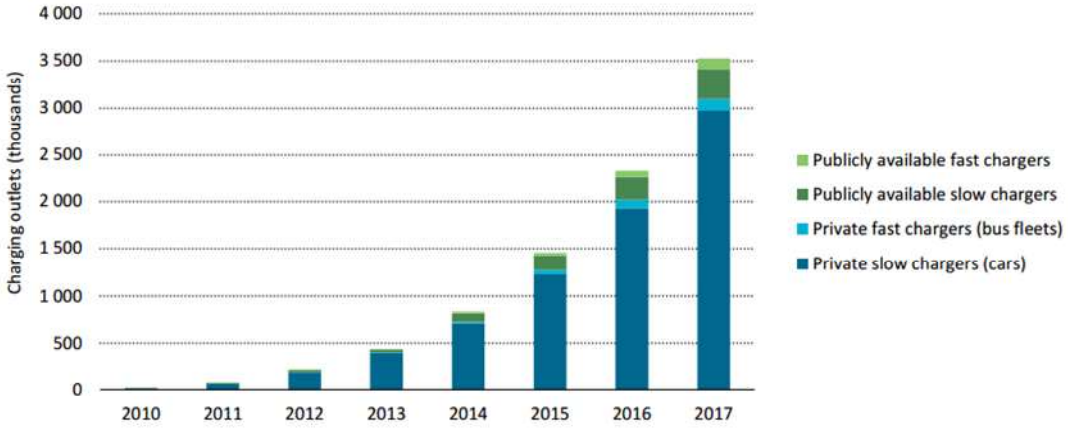

Figure 1-2 Evolution of available battery charger outlets from 2010 to 2017. Reprinted from [1]

isolated by a step-down transformer. The line-frequency step-down transformer creates an AC-link bus from which multiple 2-stage non-isolated rectifiers are connected in parallel. (b) illustrates an architecture with common DC-link. In [4] and [5] multi-pulse based rectifier is chosen to generate the common DC-link, achieving a 0.98 PF with THD < 5%.

Table 1-2 AC level 1 and level 2 battery charger clasification

Charge Method	Nominal Supply voltage (V)	Maximum Current (A)	Branch Circuit Breaker Rating (A)	Output Power Level (kW)
AC Level 1	120 V AC, 1-phase	12 A	15 A	1.08
	102 V AC, 1-phase	16 A	20 A	1.44
AC Level 2	208 to 240 V AC, 1-phase	16 A	20 A	3.3
	208 to 240 V AC, 1-phase	32 A	40 A	6.6
	208 to 240 V AC, 1-phase	≤80 A	Per NEC 635	≤14.4

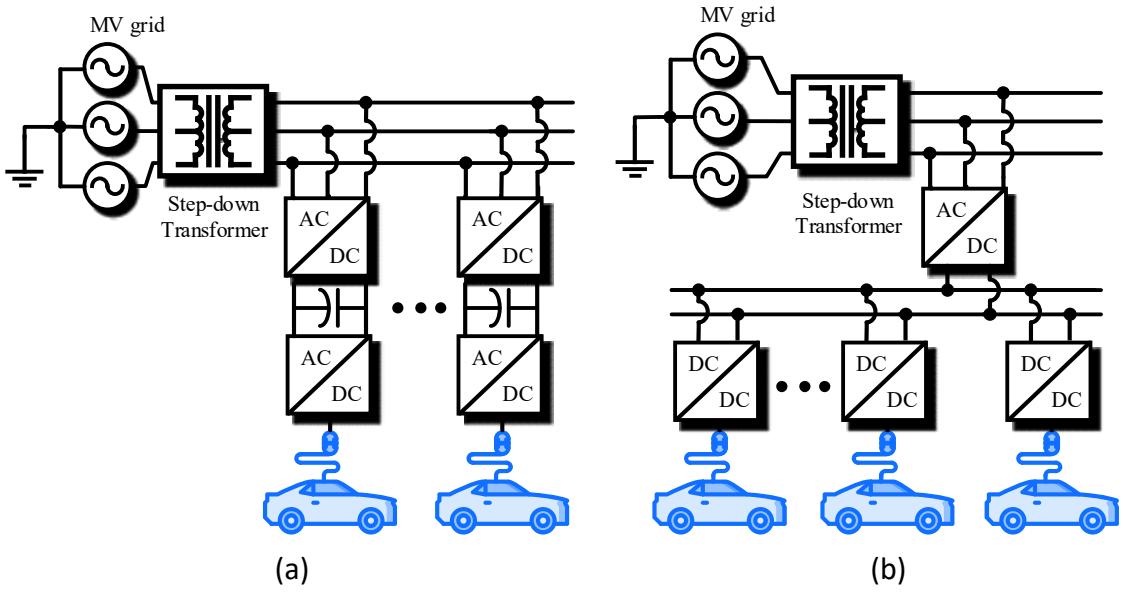

Figure 1-3 System level architecture for Level-3 battery charging station (a) AC bus approach (b) DC bus approach

To further improve the power density, galvanic isolation can be included within the rectifier topology as shown in Figure 1-4. The charger architecture depicted in Figure 1-4(a) is usually implemented with a 2-stage converter which block diagram is depicted in Figure 1-4(b). The rectification stage in Figure 1-4(b) has the task of generating high quality input current with close to unit power factor and low harmonic distortion through a PFC (Power Factor Correction) scheme. This stage is usually implemented with the traditional six switches VSI but some other approaches like Four-legged three phase converters [6],[7] or VIENNA rectifier [8] are also popular. After the rectification stage, a DC-DC converter is connected through a DC link capacitor to achieve DC voltage regulation at the output and to create a galvanic isolation. This stage is implemented by full-bridge isolated topologies with ZVS schemes to improve efficiency due to their HF

(high-frequency) operation as described in [9]-[11]. Another alternative for this stage is LLC half bridge resonant topologies as the one proposed in [12].

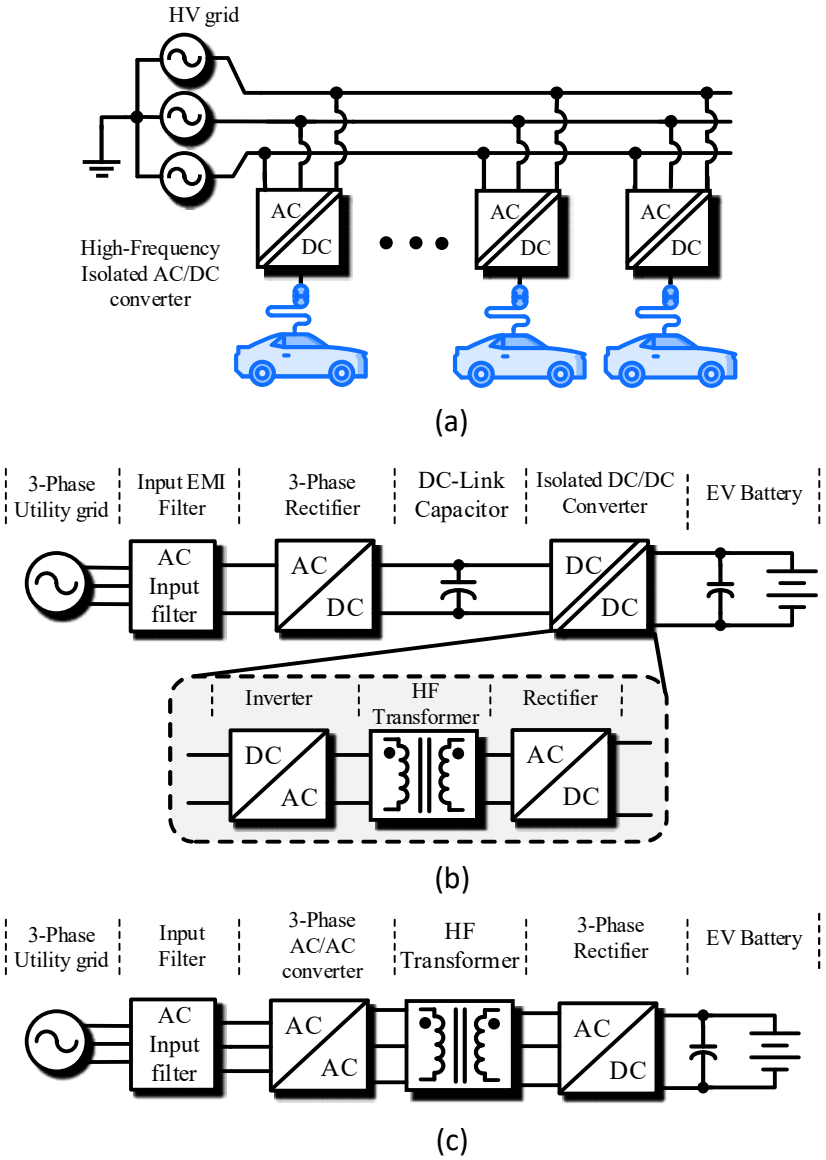

Figure 1-4 Level-3 battery charger with Isolated high-frequency rectifier (a) system level architecture diagram (b) 2-stage high frequency rectifier with dc-link (c) single-stage high frequency rectifier with no dc-link.

Besides the conventional two-stage converters from Figure 1-4(b), single-stage three-phase AC-DC converters are also possible to implement as depicted in Figure 1-4(c) by using a matrix-type converter as in [13]. In both [14] and [15], three matrix-type converters are used to modulate the utility three-phase voltage followed by a high-frequency isolation transformer and finally connected to a diode rectifier. This type of converters confers additional advantages compared to a conventional two-stage topology with those improvements regarding to efficiency, power density and reliability due to its single stage nature.

Multi-pulse topologies are popular systems in industry due to their low complexity and high robustness [16]-[19]. These types of topologies are generally used to deliver high power in the order of hundreds of kilowatts due to their high reliability. The topology proposed in this thesis is based in the multi-pulse converter presented in [20] implemented for a high frequency case; moreover, DC voltage output regulation can now be achieved due to the high frequency modulation scheme implemented. The direct topology proposed in this paper takes advantage of multi-pulse converters simplicity and reliability to generate high quality input current with high-frequency isolation feature without complicated control schemes. The output voltage and power are easily regulated with a simple duty cycle control of the high frequency stage. Through mathematical analysis, it is proved that the proposed converter behaves as a buck-type topology; thus, a PI controller ensures closed loop control for both DC voltage and current regulation.

1.2. Research objective

The objective of this thesis is to propose and analyze a direct three-phase rectifier with high frequency isolation as a possible topology for fast EV battery chargers.

The characteristics of the proposed topology has high-frequency isolation with DC voltage regulation and generates high quality input current in a single circuit; thus, the power density of an overall battery charger system is improved. Reduced Total Harmonic Distortion (THD) is achieved by use of a 12-pulse rectifier topology. The results will be proved scalable for a higher number of pulses (18, 24-pulses) to improve THD of the utility input current even further. THD levels will be proved to facilitate the compliance of IEEE-519 harmonics standards.

An emphasis on practical implementation will be made considering practical limitations and considerations for a fully functional 2kW prototype.

1.3. Thesis outline

The contents of the thesis are organized in the following manner.

Section 1 discuss the importance of EV charging and the classification of this type of systems according with the amount of power that they can deliver. The main two architectures for Level-3 fast charging are introduced.

Section 2 consist on a review of the state of the art topologies for two Level-3 battery charging station architecture: common DC-bus architecture and common AC-bus architecture. Additionally, a review of three-phase diode rectifier converter and the principle of harmonica cancelation with phase shift transformer is done.

The proposed topology will be describe in Section 3. A mathematical description of the topology is discussed. The modulation scheme of the topology is describe in this section. Also transformer, input filter and output filter design are addressed.

Section 4 presents a design example for a system rated at 50 kW. Simulation results are discussed and efficiency analysis results are provided.

Section 5 consist describes the practical implementation of the modulation scheme in a Digital Signal Processor (DSP). Experimental results for a 2kW experimental prototype are discussed.

Finally, section 6 provides a general conclusion and discusses further improvements for future work.

1.4. Section Conclusion

In this section the importance of the battery charging system was stated together with a classification. According to the output power level EV battery chargers can be classified in three categories. Level-1 and Level-2 chargers are mostly used in domestic or private chargers due to the limited amount of power that domestic electrical installations can handle. Battery chargers with power rating >50kW are classified as Level-3 chargers. This type of system are usually build as off-board chargers due to its connection to Medium Voltage (MV) lines. Level-3 chargers were also classified according to its architecture in two main groups. Common DC-bus architecture and common AC-bus architecture.

2. DETAILED REVIEW EV FAST CHARGING TOPOLOGIES

2.1. Common DC-Link Architecture

One of the state of the art architectures for Level-3 chargers is shown at Figure 1-3 (b). A common DC-Link infrastructure has the following advantages

- Only one AC-DC stage is needed
- Non-isolated DC-DC converter at the output
- Integration with PV energy storage

This type of architecture uses a single AC-DC rectification stage which generates a DC-bus at the output to distribute the power among multiple non-isolated DC-DC stages. State of the art topologies for this two stages are discussed below.

2.1.1. AC-DC rectifier

The state of the art approach for a DC-Link architecture use a 12-pulse rectifier with active filtering to improve THD at both DC and AC side.

In literature, there are multiple approaches to build the 12-pulse rectifier with high quality input current. One of the most popular approaches is the use of an auxiliary Active Power Filter (APF) at the DC-side of the 12-pulse rectifier.

In [20] the 12-pulse diode rectifier with high quality input current (less than 1% THD) depicted in Figure 2-1 is proposed. In [20] is proved that the if the three-phase diode rectifiers currents I_{d1} and I_{d2} have a shape as the one depicted in Figure 2-2(a) , the input currents I_a, I_b, and I_c will result in a pure sinusoidal waveform as shown in Figure

2-2(b). In practice, I_X (from Figure 2-2(a)) is approximated to a triangular waveform with a frequency of 360 Hz. With this approximation, a THD of 2% is achieved in experimental results. The main disadvantage of the approach proposed in [20] is the use of an additional 360 Hz transformer to implement the current injection at the DC side. The additional 360 Hz transformer adds volume and additional losses to the overall system.

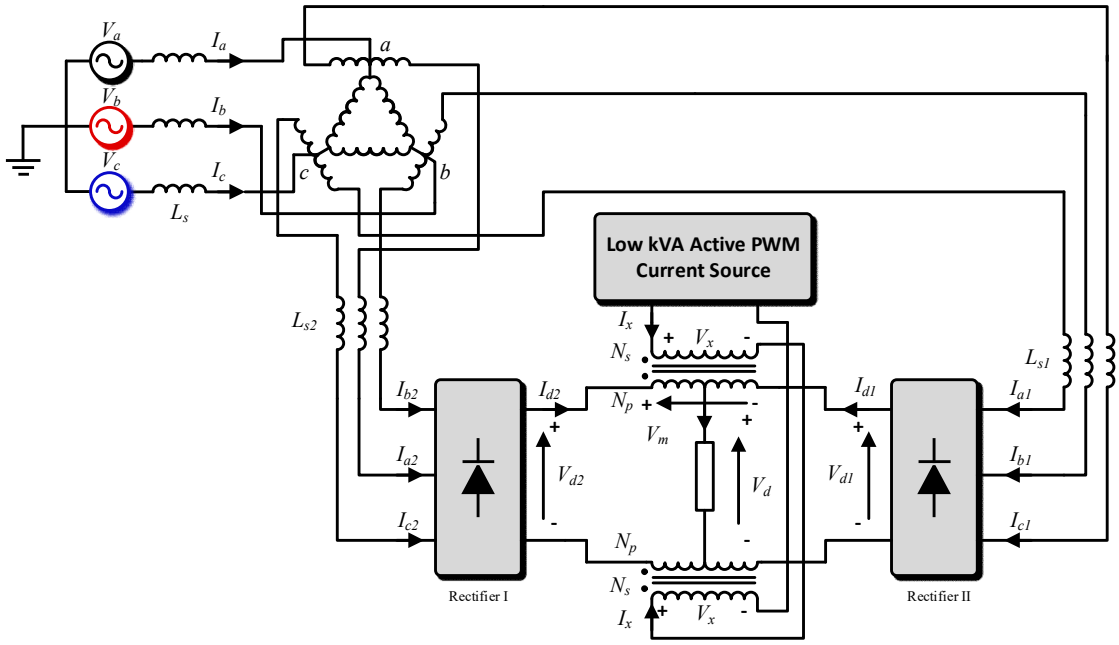

Figure 2-1 12-pulse rectifier with Active Power Filter. Adapted from [20].

Based on the same APF approach, [21] proposes a method to achieve high quality input power using a buck-boost topology (Refer to Figure 2-3). The method proposed in [21] also works under the principle of shaping the DC side diode currents i_{rec1} and i_{rec2} (refer to Figure 2-3) into triangular waveforms to achieve sinusoidal input currents as shown in Figure 2-4.

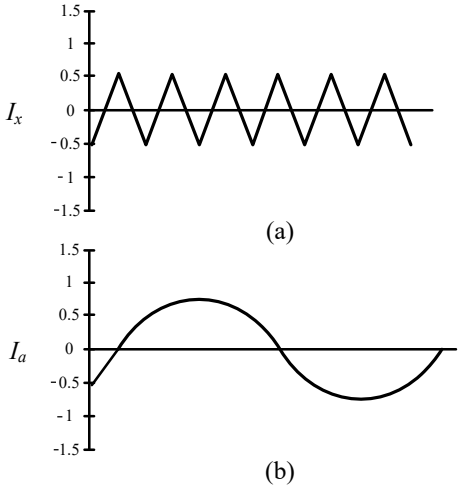

Figure 2-2 (a) Injected current I_x in the DC side. (b) Input line current I_a as a pure sinusoidal

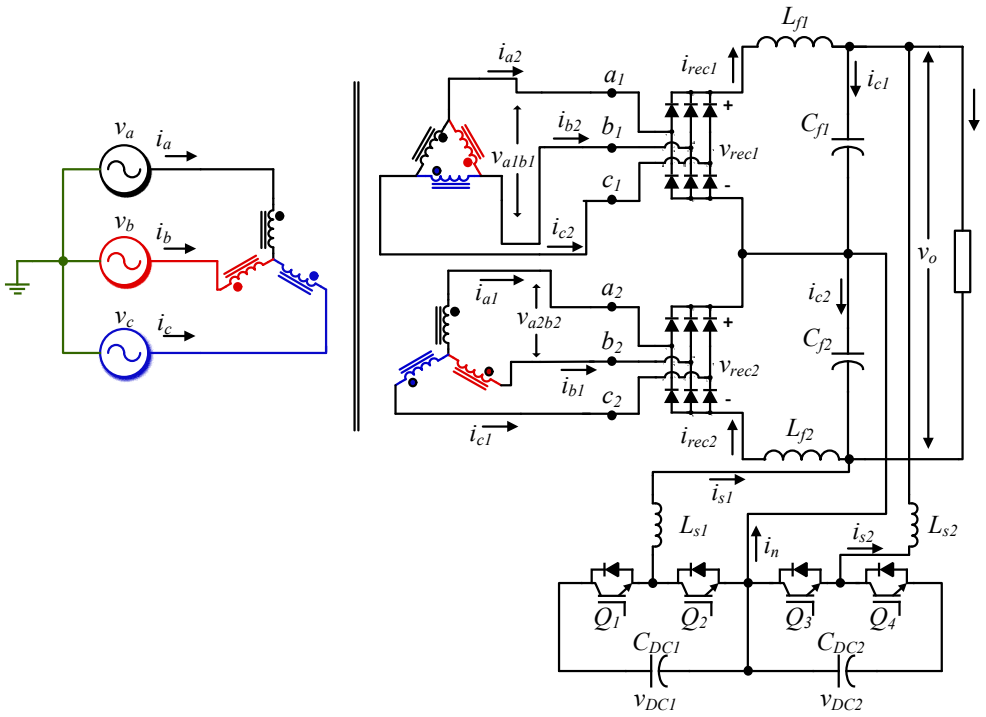

Figure 2-3 Active Power Filter. A buck-boost topology is used to inject current at the DC side to shape i_{rec1} and i_{rec2} as triangular currents at 360 Hz. Adapted from [22]

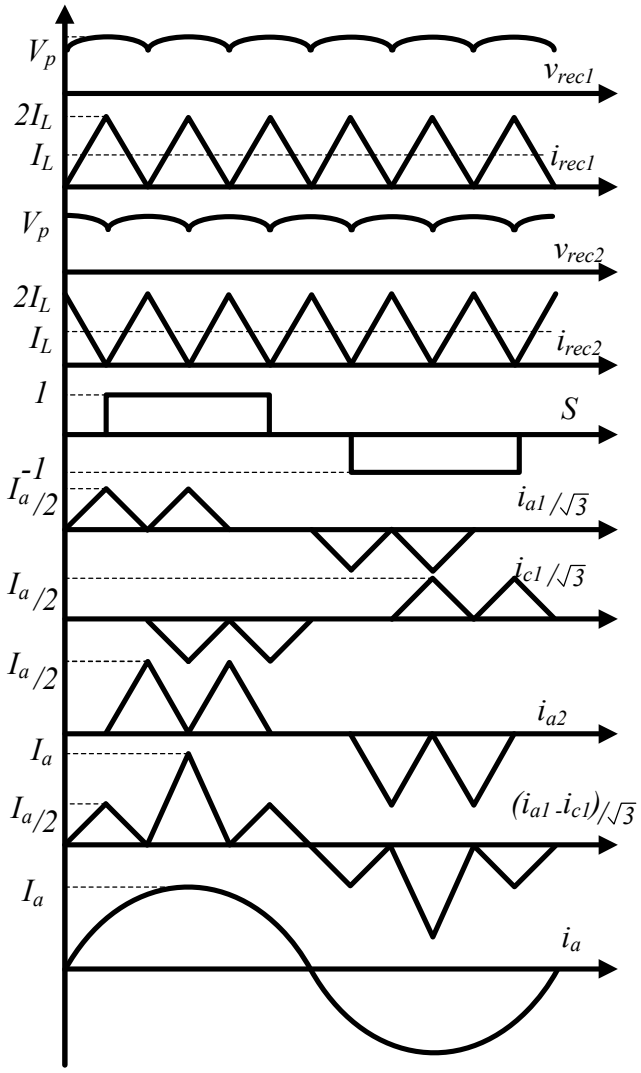

Figure 2-4 Main signal waveforms from Figure 2-3.

In this approach the output filter inductor and capacitor (L_f and C_f) are designed to resonate at 360 Hz to help the triangular waveform tracking. That way the proposed control simplifies and allows reducing both the DC and AC distortions at the output and input respectively.

By using this approach THD values of up to 2% can be achieved; thus , making it suitable to comply THD standard limits (<5%). Moreover, with this approach the need of an additional 360 Hz transformer is eliminated.

2.1.2. DC-DC non-isolated stage

One of the advantages of a DC-bus architecture is the fact that the DC-DC stages do not need additional galvanic isolation since the AC-DC phase shift transformer of the rectification stage creates a galvanic isolation between the Medium Voltage (MV) line and the DC outputs connected to the vehicles. An alternative for this stage is given by interleaved buck converters as the one shown in Figure 2-5 [23].

The effective switching frequency of the interleaved system is n times the switching frequency of one leg, where n is the number of interleaving legs. The result of this approach generates a higher frequency system, reduces current ripple (and therefore smaller DC output filters) and reduces EMI. Moreover, the lack of transformer on the system also contributes to decrease the volume of this stage.

As an example, a three-leg interleaved buck converter is shown in Figure 2-6.This circuit is controlled by phase shifted PWM in which each pulse is shifted by $n/360°$ i.e. the PWM signals T_1, T_2 and T_3 have 120° phase shift.

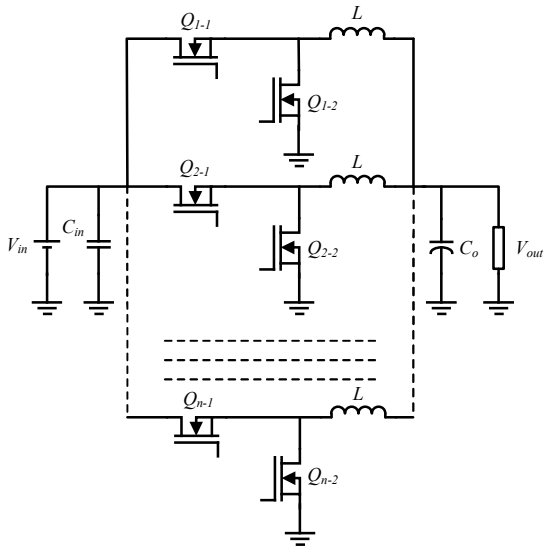

Figure 2-5 Interleaved boost converter. Q_{n-1} and Q_{n-2} switch in a complementary way. The topology operates with phase-shifted PWM signals at $n/360°$ where n is the number of boost modules connected in parallel. The output filter for this topology can be design to filter n times the switching frequency of each module. Adapted from [23].

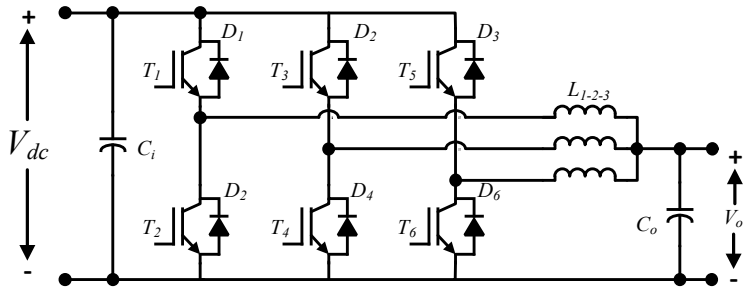

Figure 2-6 Interleaved boost example for $n = 3$. Each leg of the circuit operates with a 120° phase-shift from each other

2.2. AC bus architecture

The second approach to build a Level-3 charging station is the common AC bus architecture as shown in (a). It can be notice that this approach also uses a line

frequency transformer to step down the MV grid. In the case shown at (a) non isolated AC-DC converters can be connected to the common AC bus at the output of the transformer. This way the DC outputs have still galvanic isolation and each AC-DC converter is build as an individual module.

One way to improve the power density of the system is to include the galvanic isolation within the two-stage AC-DC converters as depicted in Figure 1-4(b). In this case, a second stage consisting of an isolated DC-DC converter is used. It has to be mentioned that the transformer of the DC-DC converter operates at high-frequencies; thus, reducing the size of the overall system. The main advantages of an AC-bus architecture are:

- High power density by using HF transformer
- Modular structure, because each AC-DC converter are independent from each other

The most popular state of the art topologies for a two-stage MV three-phase rectifier are discussed below.

2.2.1. AC-DC PFC stage.

Usually the first stage of a two-stage rectifier consist of a non-isolated AC-DC converter. One of the most popular approach is to use a Four-legged PFC rectifier as the one shown in Figure 2-7. This approach is mostly used because of its benefits against failures [6][7].

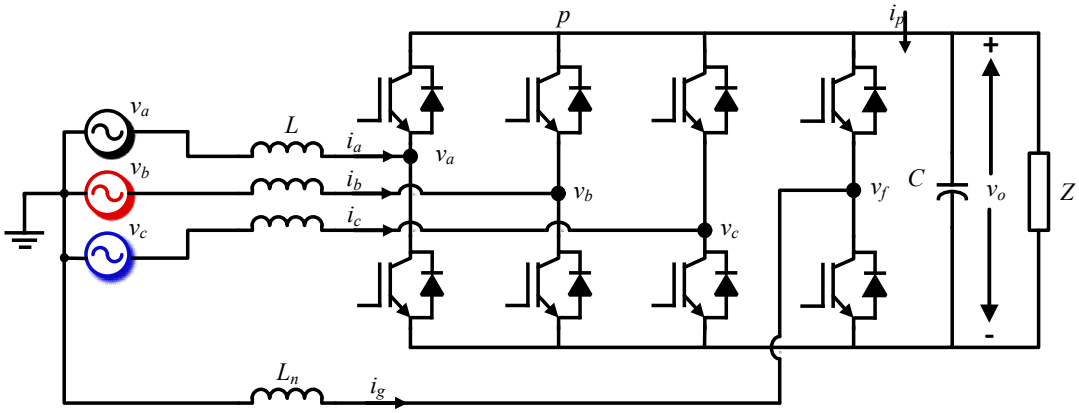

Figure 2-7 Four-legged VSI. The forth leg of the circuit is used to compensate the zero-sequence of the rotational frame voltage in case one of the main legs fails.

A three-phase Voltage Source Inverter is usually modeled by using Coordinate Transformations or Space Vectors to generate a rotational reference frame [24-23]. This method transforms the three voltage and current inputs into two decoupled constant values, one for the active power and one for the reactive. By using this approach the three phase input currents are basically modeled as two constant values which makes simple to track the input currents to achieve close to unity power factor and low THD values. In fact with this method instead of tracking time varying signals the problem is reduced to track two constant values which can be achieved by using the popular PI controller. The method consist on generating a projection of three vectors into a plane as depicted in Figure 2-8(a). By using the fact that a planes equation is given by:

$$ax + by + cz = d \tag{2.1}$$

This same idea is used to project three vector over a plane to get an equivalent transformation into two vectors α and β in Figure 2-8.

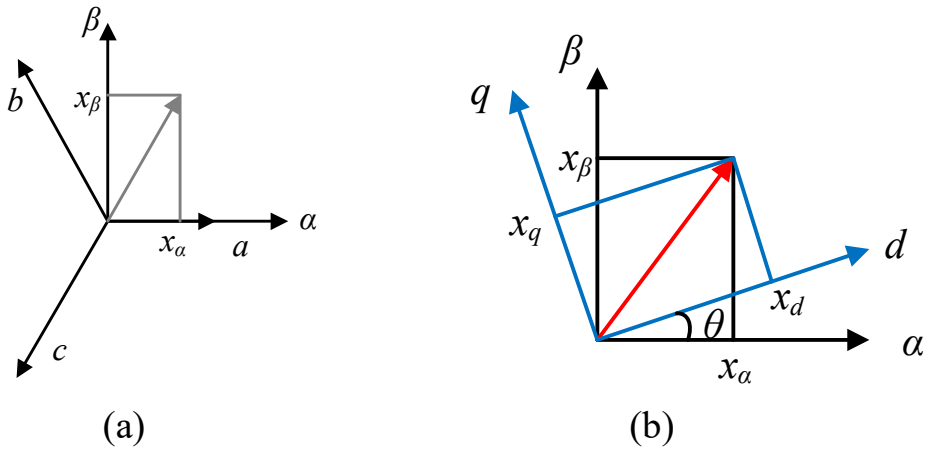

Figure 2-8 (a) stationary reference frame $\alpha\beta$ and (b) rotational reference frame qd

If the three vectors a,b and c sum to zero the transformation from abc to $\alpha\beta$ is given by the following transformation matrix:

$$C_{\alpha\beta} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \tag{2.2}$$

However, in a more general case when the vector a, b and c do not sum up to zero a zero sequence vector has to be considered and the transformation matrix is given by:

$$C_{\alpha\beta} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ \frac{\sqrt{2}}{3} & \frac{\sqrt{2}}{3} & \frac{\sqrt{2}}{3} \end{bmatrix} \tag{2.3}$$

To get a rotational reference frame and to represent the vector α and β as 2 constants, the following transformation matrix is used

$$R(\theta) = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{2.4}$$

The rotational reference frame transformation is given by

$$f_{qd0} = T_{qd0}(\theta) f_{abc} \tag{2.5}$$

Where

$$T_{qd}\ (\theta) = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{2.6}$$

Therefore the "abc" transformation to a rotational reference frame is given by equation (2.7)

$$\begin{bmatrix} f_{qs}(\theta) \\ f_{ds}(\theta) \\ f_{0s} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} \tag{2.7}$$

In a conventional three-legged Voltage Source Inverter (VSI) if one of the legs fails that leg is disconnected by a fuse which will allow the other 2 legs operate. However, since the system will now be unbalanced the maximum output power of the converter is one-third of the original. In order to solve this issue a Fourth-leg is

introduced which mid-point is connected to the neutral of the utility input voltage. In this case, if one leg fails and is disconnected, the fourth leg is controlled in such a way that the zero sequence of the rotational frame voltage is compensated; thus, the other 2 legs keep working as in the case of a balanced circuits and the total output of the system is kept at two-thirds of the original one.

Another AC-DC topology suited for fast charging stations is the VIENNA rectifier depicted in Figure 2-9 [8]. VIENNA rectifier works as three-modular boost-PFC circuits which use the output voltage generated by a 6-pulse rectifier as the source of power to shape the input voltage of the utility. This idea is easy to understand by looking at the equivalent circuit depicted in Figure 2-9(a).

Since the operational principle is based on a boost-PFC topology, it can be noticed that the topology does not have bidirectional power flow; however, this does not represent a problem in a Level-3 off-board charger. One of the advantages of this topology is that each one of active switches commutated in a stand-alone manner with the diodes; therefore, there is no need for dead-times because the diodes will only conduct as soon as the switch is turn-off making the topology robust.

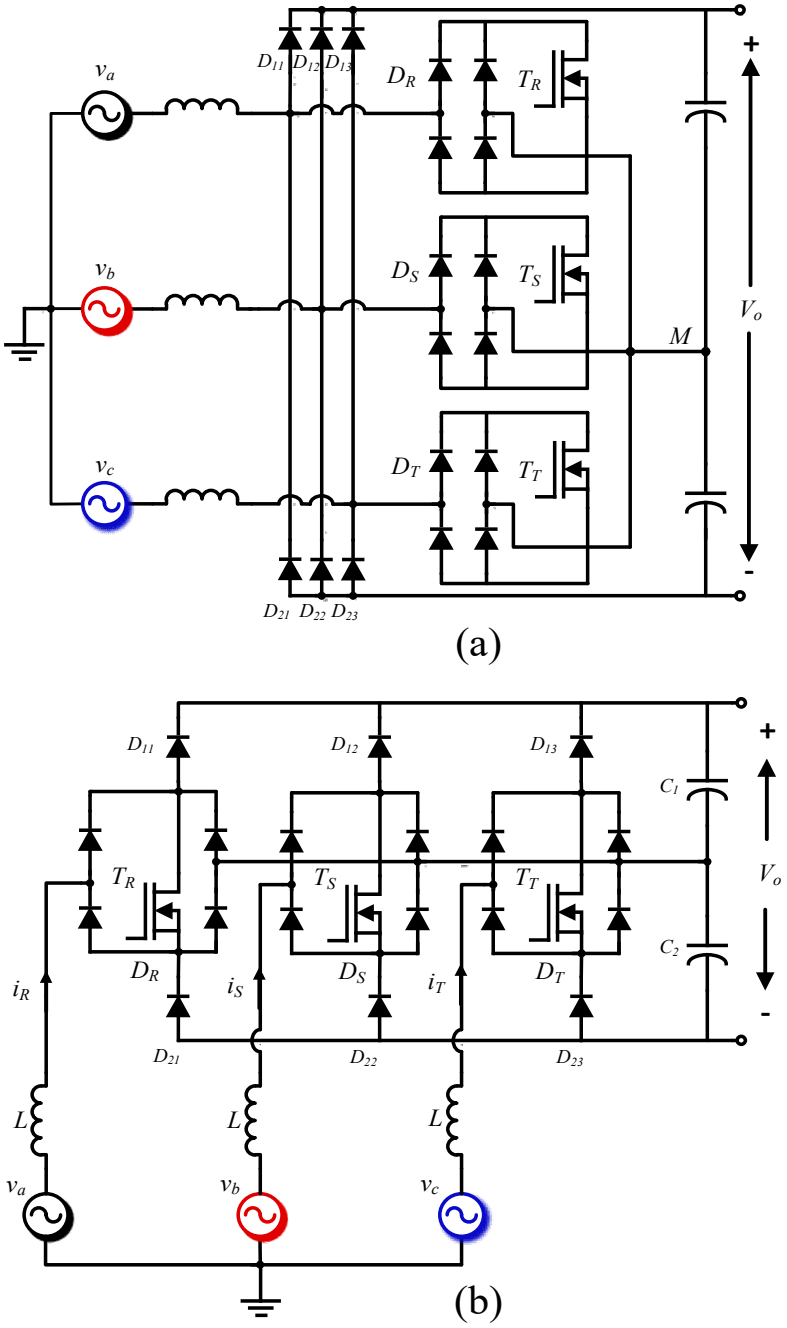

Figure 2-9 Basic structure of VIENNA rectifier system. (a) Proof of concept circuit with a boost PFC circuit per face. (b) Final realization of VIENNA rectifier. The voltage stress of diodes D_{1j} and D_{2j} is one half of the output voltage compared with the circuit presented in (a). The configuration presented in (b) is more suitable for high frequency applications.

2.2.2. DC-DC Power converters

The second stage in a two-stage AC-DC rectifier is usually built using DC-DC topologies with isolating HF transformer to reduce the size of passive elements [9-11]. Since the frequency of operation affects the efficiency performance of the DC-DC converter due to switching losses, Zero Voltage Switching (ZVS) topologies are preferred. One of the predilected topologies for this is stage is the phase-shifted ZVS full-bridge DC-DC converter depicted in Figure 2-10. By using, the parasitic inductance of the HF transformer and the parasitic capacitance of the semiconductor devices resonance is achieved without additional components.

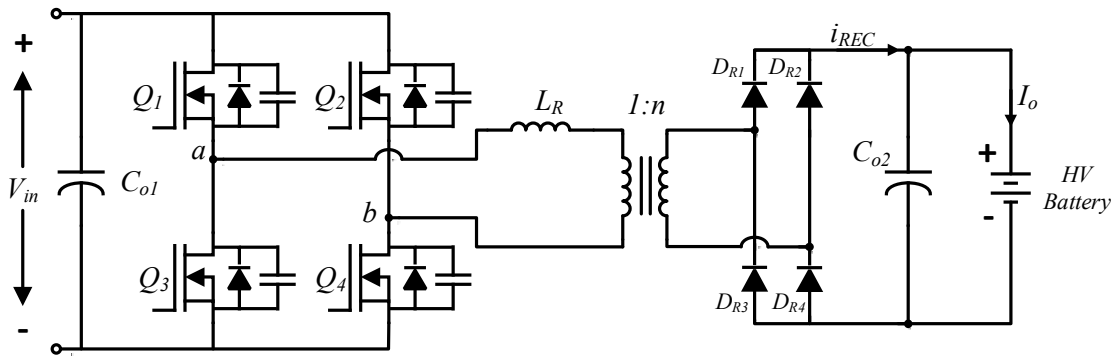

Figure 2-10 DC-DC full-bridge converter. This circuit can achieve ZVS by using the parasitic capacitance of the switches and the parasitic inductance of the transformer.

The oscillations between leakage inductance and parasitic capacitance can be minimized by shifting pulses from $Q2$ and $Q4$ with respect to $Q1$ and $Q3$. This approach allows to achieve ZVS over an specific power level as the resonance depends on the load current. EV batteries appear as variable loads at the DC output; therefore, the DC-DC converter in this stage must me able to operate at light loads and have a good efficiency performance even under those conditions.

Another potential topology used for the DC-DC stage is the half-bridge LLC converter shown at Figure 2-11. Some of its advantages are: lower number of semiconductor devices, the ability to operate ZCS over a wide range of loads, low voltage stress, and only one capacitor as output filter [12]. In this case, additional resonant capacitors are needed on the primary side, as well as an additional inductor to generate the resonant effect. The main disadvantage of this topology is that the output voltage is controlled by changing the switching frequency of switches $Q1$ and $Q2$. This characteristic makes the design of the output filter more complicated due to the big range of frequencies that the filter needs to cover depending on the output load.

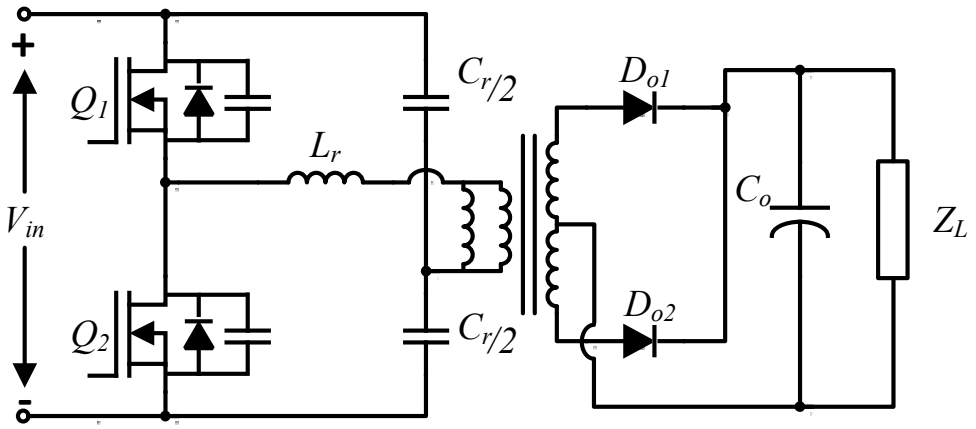

Figure 2-11 LCL converter with high frequency isolation. Voltage regulation is achieved by changing the switching frequency of switches Q_1 and Q_2 due to the resonant circuit from by L_r and C_r.

Table 2-1 contains a comparison between the full bridge, LLC and interleaved buck topology presented in previous sections. It can be noticed that the interleaved boost has an efficiency in between the full bridge and LLC converters with ZVS. Although the LLC is more efficient, the control of the topology is made by changing the switching frequency which complicate the design of the additional passive components. The only

drawback of the interleaved buck is its lack of galvanic isolation. However, this disadvantage can be solved by using the topology in a DC-bus architecture Level-3 battery charger station. It is clear that a DC bus architecture has potential to improve its power density if the first stage AC-DC gets rid of the line-frequency transformer. By having this idea in mind the topology proposed in section 4 aims to achieve an equivalent 12-pulse rectifier with high frequency isolation.

Table 2-1: DC-DC converters comparison

Parameter	Phase Shifted Full Bridge	LLC	Interleaved Buck
Output Capacitor (μF)	100	500	1
Output Inductor (μH)	96	-	-
Active Switches	4	2	3
Transfer Capacitor (μF)	-	11(820 V)	-
Transfer Inductor (mH)	-	-	3 x 1.1
Transformer	1	1	-
Isolation	Yes	Yes	No
Control	PWM	Freq.	PWM
Efficiency	94%	97%	96%

2.3. Basic topologies review

The topologies proposed in this thesis is based on a 12-pulse rectifier. The basic concepts of line-frequency rectifiers are discussed bellow

2.3.1. Six pulse rectifier

Six-pulse rectifiers are mostly used in industrial applications where three-phase ac voltages are available. Compared to a single phase rectifier, a three-phase rectifier has higher power capabilities and lower ripple content at the output. To simplify the analysis of a six-pulse rectifier a constant current source can be connected to the DC output as

depicted in Figure 2-12. This assumption is equivalent to consider a ripple free current at the DC side due to an infinite inductance.

In the three-phase diode rectifier of Figure 2-12 the diodes with its anode at the highest potential will conduct and the other two become reverse biased a summary of the waveforms is depicted in Figure 2-13.

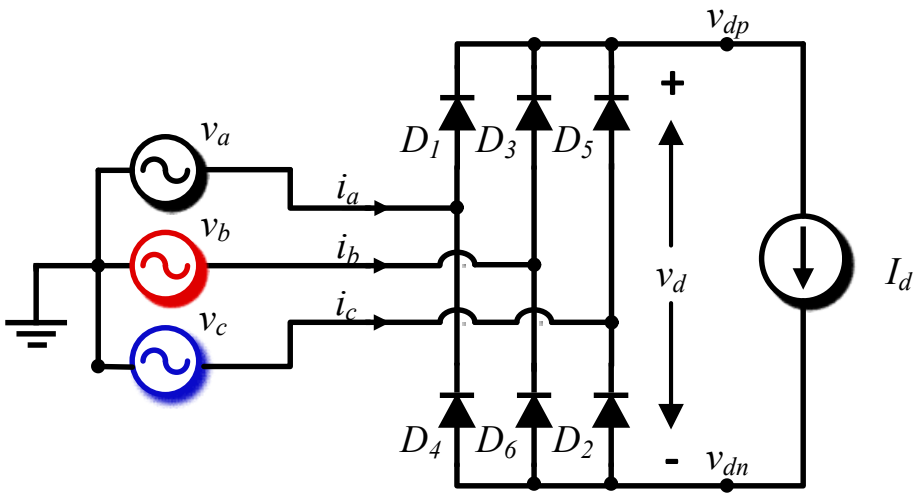

Figure 2-12 Ideal Three-phase diode rectifier. The current source at the DC side models a ripple free output.

From Figure 2-13(c) it can be seen that v_d consist of six segments per cycle of line frequency. This is the reason why a three-phase rectifier is also called six-pulse rectifier. Each diode of the six pulse rectifier conduct for 120°, from Figure 2-13 it can be noticed that

$$i_a = \begin{cases} I_d \text{ when } D_1 \text{ is conducting} \\ -I_d \text{ when } D_4 \text{ is conducting} \\ 0 \text{ when neither } D_1 \text{ or } D_4 \text{ conduct} \end{cases} \quad (2.7)$$

$$i_b = \begin{cases} I_d \text{ when } D_3 \text{ is conducting} \\ -I_d \text{ when } D_6 \text{ is conducting} \\ 0 \text{ when neither } D_3 \text{ or } D_6 \text{ conduct} \end{cases} \quad (2.8)$$

$$i_c = \begin{cases} I_d \; when \; D_2 \; is \; conducting \\ -I_d \; when \; D_5 \; is \; conducting \\ 0 \; when \; neither \; D_2 \; or \; D_5 \; conduct \end{cases} \quad (2.9)$$

To obtain the average value of the output dc voltage, it is enough to consider only one of the six segments of v_d and obtain the average in an interval of $\frac{\pi}{3}$ rad. Arbitrarily the time origin $t = 0$ can be choosen as in Figure 2-13 to match with the maximum of one the pulses from v_d.

Notice that each segment of v_d is given in terms of line-to-line voltages; thus

$$v_d = v_{ab} = \sqrt{2}V_{LL}cos\omega t \quad -\frac{1}{6}\pi < \omega t < \frac{1}{6}\pi \quad (2.10)$$

Where V_{LL} is the rms value of the line-to-line voltages.

By Fourier series analysis it can be obtained that [26]

$$v_d = \frac{3}{\pi}\sqrt{2}V_{LL}\left(1 - \sum_{k=1}^{+\infty}\frac{2}{36k^2 - 1}\cos(6k\omega t)\right) \quad (2.11)$$

From (2.11) it can be noticed that the DC component V_{d0} is given by

$$V_{d0} = \frac{3}{\pi}\sqrt{2}V_{LL} \quad (2.12)$$

On the other hand, the Fourier series of one of the line currents is given by

$$i_s(\omega t) = \sum_{n=1,5,7\ldots}^{\infty} I_d\left(\frac{4}{n\pi}\cos\left(\frac{n\pi}{6}\right)\right)\cdot \sin(n\omega t) \quad (2.13)$$

Where i_s can represent any of the line current i_a, i_b and i_c. From (2.13) it can be seen that the rms value of the fundamental frequency component of any line current is given by

$$i_{s1} = \frac{\sqrt{6}}{\pi} I_d \tag{2.14}$$

Therefore, the output power in the ideal six-pulse rectifier is given by

$$P_{out} = V_{d0} I_d = \frac{3}{\pi} \sqrt{2} V_{LL} I_d \tag{2.15}$$

Since the circuit is lossless the input power is also equal to the output power; thus

$$P_{in} = P_{out} = \frac{3}{\pi} \sqrt{2} V_{LL} I_d \tag{2.16}$$

On the other hand the apparent power observed at the rectifier input is given by

$$S_{in} = 3 V_{rms} i_{s1} = \sqrt{2} V_{LL} I_d \tag{2.17}$$

Where V_{rms} is the rms value of the line-to-neutral voltage.

Finally the ideal power factor of the three-phase diode rectifier can bi computed by the following equation

$$PF = \frac{P_{in}}{S_{in}} = 0.955 \tag{2.18}$$

It can be noticed that the Power Factor (PF) obtained is reasonably good and satisfies almost all of the power factor standards.

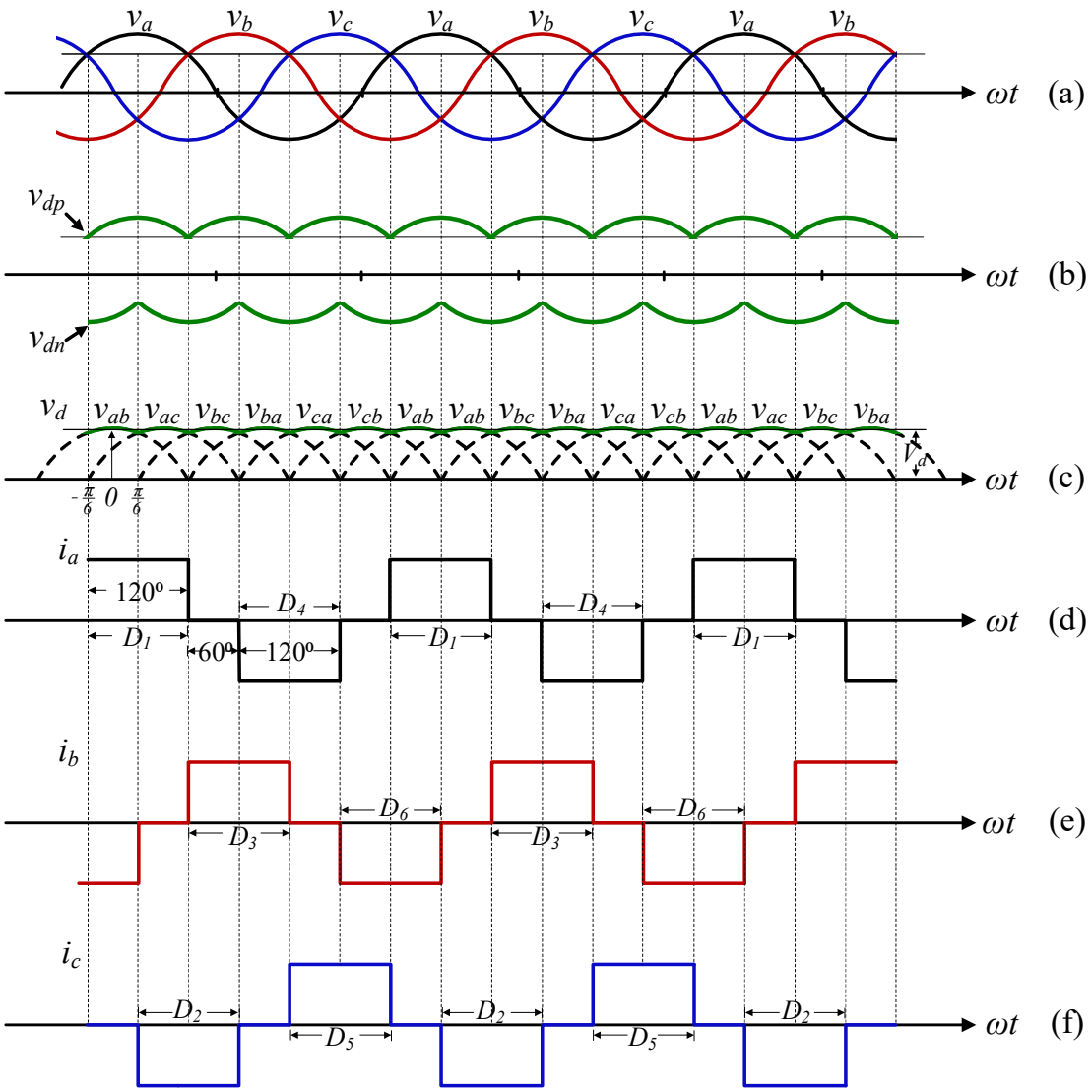

Figure 2-13 Main waveforms of ideal three-phase diode rectifier. (a) Line voltages v_a, v_b, and v_c (b) Node voltages $v_{dp}$and v_{dn} (c) six-pulse output voltage $v_d = v_{dp} - v_{dn}$(d) phase a diode input current i_a(e) phase b diode input current i_b and (f) phase c diode input current i_c.

The THD of a signal with rms value F can be defined as follow

$$THD = \frac{\sqrt{F^2 - F_1^2}}{F_1} \tag{2.19}$$

Where F_1^2 is the rms value of the fundamental component. The ideal total harmonic distortion of a three-phase diode rectifier is 31% [27]. To improve the THD performance multiple six-pulses can be connected in series and further cancelation of harmonics can be achieved by using a phase shift transformer [28]. Further analysis of harmonics elimination is presented in the following section.

2.3.2. Harmonic elimination with phase shift transformer

If the harmonic currents of more than one rectifier are phase shifted from each other, it is possible to achieve harmonic current cancelation.

Figure 2-14 depicts a delta/star transformer connected to a three-phase rectifier. Assuming that the voltage ratio of V_{ab1}/V_{ab2} of the transformer is unity; i.e., $n_1/n_2 = \sqrt{3}$. The transformer has a phase shift of 30° or $\angle V_{ab1} - \angle V_{ab2} = 30°$. As discussed in the analysis of the ideal six-pulse rectifier (refer to eq.()), the currents i_a, i_b and i_c are defined as follow

$$i_a = \sum_{n=1,5,7\ldots}^{\infty} I_n \cdot \sin(n\omega t) \tag{2.20}$$

$$i_b = \sum_{n=1,5,7\ldots}^{\infty} I_n \cdot \sin(n\omega t - 120°) \tag{2.21}$$

$$i_c = \sum_{n=1,5,7\ldots}^{\infty} I_n \cdot \sin(n\omega t - 240°) \tag{2.22}$$

Where I_n is the amplitude of the nth harmonic of the current defined as

$$I_n = I_d\left(\frac{4}{n\pi}\cos\left(\frac{n\pi}{6}\right)\right) \quad n = 1,5,7\ldots \tag{2.23}$$

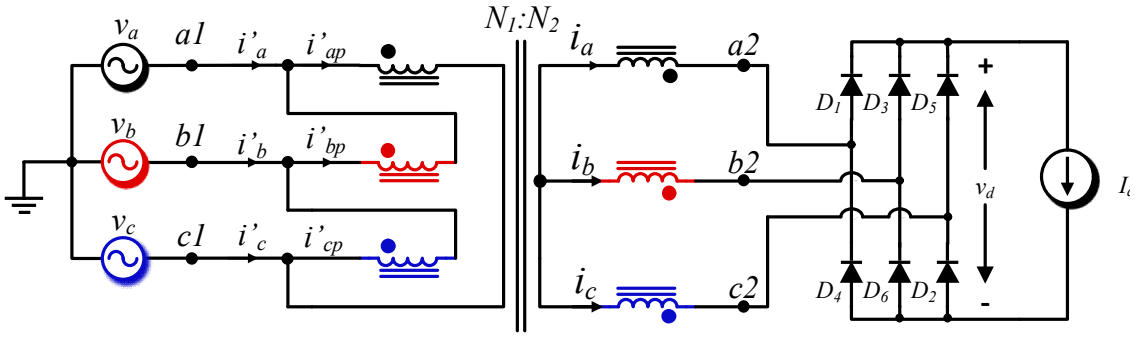

Figure 2-14 General harmonics phase shift analysis for delta/star connection of a three-phase diode rectifier. In this case $\delta = \angle v_{a1} - \angle v_{a2} = -30°$

When i_a and i_b are referred at the primary side , the currents i'_{ap} and i'_{bp} in the primary winding can be described by

$$i'_{ap} = i_a \frac{n_2}{n_1} = \frac{1}{\sqrt{3}}(I_1 \sin(\omega t) + I_5 \sin(5\omega t) + I_7 \sin(7\omega t) + I_{11} \sin(11\omega t) + \cdots) \quad (2.24)$$

$$i'_{bp} = i_b \frac{n_2}{n_1} =$$

$$\frac{1}{\sqrt{3}}(I_1 \sin(\omega t - 120°) + I_5 \sin(5\omega t - 240°) + I_7 \sin(7\omega t - 120°)$$

$$+ I_{11} \sin(11\omega t - 240°)$$

$$+ \cdots) \quad (2.25)$$

From (2.24) and (2.25) it can be seen that

$$i'_a = i'_{ap} - i'_{bp}$$

$$= I_1 \sin(\omega t + 30°) + I_5 \sin(5\omega t - 30°) + I_7 \sin(7\omega t + 30°)$$

$$+ I_{11} \sin(11\omega t - 30)$$

$$+ \cdots \quad (2.26)$$

$$= \sum_{n=1,7,13\ldots}^{\infty} I_n \sin(n\omega t - \delta) + \sum_{n=5,11,17\ldots}^{\infty} I_n \sin(n\omega t + \delta) \qquad (2.27)$$

The first sum of harmonics of (2.27) include all the positive sequence harmonics ($n = 1,7,13 \ldots$) whicle the second sum of harmonics correspond to the negative sequence harmonics ($n = 5,11,17 \ldots$).

Comparing the primary line current i'_a in (2.26) with the secondary side current i_a in (2.20) we have

$$\angle i'_{an} = \angle i_{an} - \delta \quad n = 1,7,13,19 \ldots \qquad (2.28)$$

$$\angle i'_{an} = \angle i_{an} - \delta \quad n = 5,11,17,23 \ldots \qquad (2.29)$$

Where $\angle i'_{an}$ and $\angle i_{an}$ are the phase angles of the nth- order harmonic currents i'_{an} and i_{an} respectively.

In Figure 2-15 a 12-pulse rectifier is shown which can use to explain the principle of harmonic cancelation with a phase shift transformer. The phase shift angle of the star/delta is $\delta = 30°$ while the phase shift angle of the star/star connection is 0°. The voltage ratio is $V_{ab}/V_{a1b1} = V_{ab}/V_{a2b2} = 2$. On the other hand the secondary side currents can be express as

$$i_{as} \sum_{n=1,5,7,11,13}^{\infty} I_n \sin(n\omega t + \delta) \qquad (2.30)$$

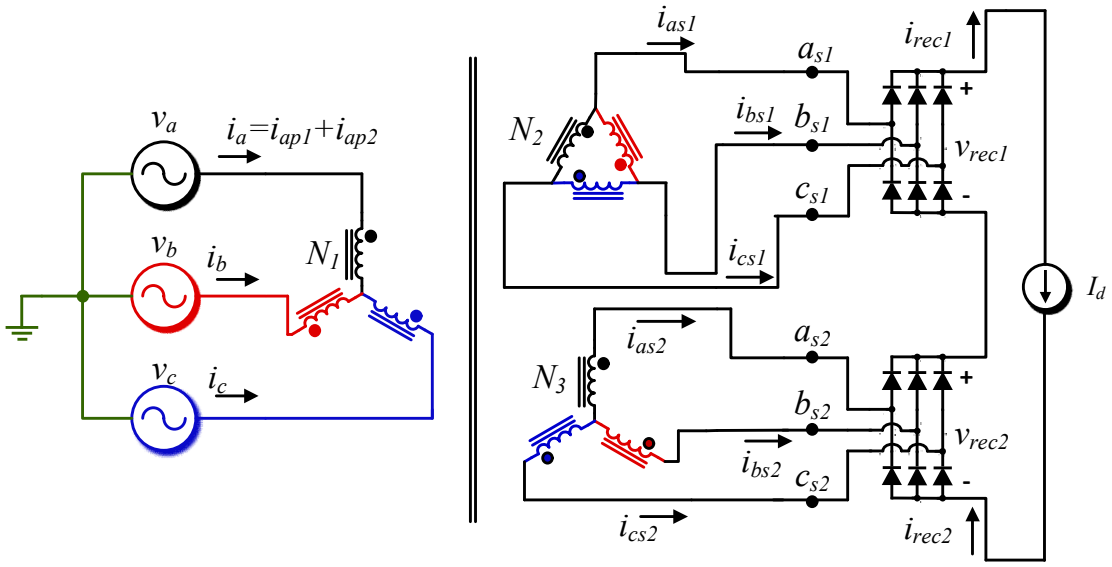

Figure 2-15 Harmonic cancelation example for ideal 12-pulse rectifier

$$i_{as2} \sum_{n=1,5,7,11,13}^{\infty} I_n \sin(n\omega t) \tag{2.31}$$

When i_{as1} is refered to the primary side, the phase angle of the harmonics can be expreesed by using (), e.i.

$$i_{ap1} = \frac{1}{2}\left(\sum_{n=1,7,13\ldots}^{\infty} I_n \sin(n(\omega t+\delta)-\delta) + \sum_{n=5,11,17\ldots}^{\infty} I_n \sin(n(\omega t+\delta)+\delta \right) \tag{2.32}$$

$$i_{ap} = \frac{1}{2}(I_1 \sin(\omega t) - I_5 \sin(5\omega t) - I_7 \sin(7\omega t) + I_{11} \sin(11\omega t) + I_{13} \sin(13\omega t) - \cdots) \tag{2.33}$$

Also the reflection of the harmonics from the star/star connection is given by

$$i_{ap2}$$

$$= \frac{1}{2}(I_1 \sin(\omega t) + I_5 \sin(5\omega t) + I_7 \sin(7\omega t) + I_{11} \sin(11\omega t) + I_{13} \sin(13\omega t)$$

$$- \cdots) \quad (2.34)$$

From (2.33) and (2.34) it can be seen that the $6n \pm 1$ harmonics have a 180° degrees phase shift from each other. Since the primary current is equal to the sum of all the current reflections from secondary to primary

$$i_a = i_{ap1} + i_{ap2} \quad (2.35)$$

Therefore, 5th 7th 11th 13th ... harmonics are canceled and the primary current has a better THD performance.

2.4. Section Conclusion

In this section a review of the state of the art of topologies for Level-3 battery charge stations was presented. For the DC- bus architectures, 12-pulse rectifier topologies to achieve high quality input current and to generate galvanic isolation for the DC side of the system were discussed. Two topologies with Active Power Filters are to reduce THD of the system to values of <5% were presented as examples. Finally, a description of the interleaved buck converter was given as a possible approach to achieve DC voltage regulation. The DC-bus architecture has the main advantage of more efficient and simple DC-DC converter modules at the output. However the main drawback of this architecture consist in the use of a line frequency transformer from the 12-pulse rectifier. On the other hand AC-bus architecture topologies such as four-leg VSI and VIENNA and ZVS topologies were discussed. It was mentioned that VSI and

VIENNA rectifier work as a first stage of a two stage converter topology for AC-bus architecture. It was mentioned that the main advantage of an AC-bus architecture consist in a higher power density due to the use of a high frequency transformer in the DC-DC stage of this two stage architecture. Finally a review of three-phase diode rectifiers and harmonic cancelation was given. It was proved that by using phase shift transformers the input current quality can be improved by cancelation of low order harmonics.

3. PROPOSED TOPOLOGY*

The proposed three-phase AC-DC rectifier with high-frequency isolation is shown in Figure 3-1. The proposed system employs three unidirectional AC-AC converters, one connected to each phase. Each AC-AC converter consists of a single-phase bridge rectifier, a small film capacitor, and a full-bridge inverter. The inputs for each AC-AC converter are line-to-line voltages. The function of the AC-AC converters is to generate a high-frequency signal (20kHz) which is applied to the primary winding of the transformer (see Figure 3-2(f)). Moreover, the DC output can be regulated by using square-wave PWM in the full-bridge converters.

$$v_{AB} = \sqrt{2}\, V_{LL} \sin(\omega t) \tag{3.1}$$

$$s_d = \frac{4}{\pi} \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n} \sin(n\omega t) \tag{3.2}$$

$$v_{pa} = v_{AB} \cdot s_d = \sqrt{2}\, V_{LL} \left(\frac{2}{\pi} - \frac{4}{\pi} \sum_{n=2,4,6\ldots}^{\infty} \frac{\cos(n\omega t)}{n^2 - 1} \right) \tag{3.3}$$

The modulation signals of the full-bridge inverters $s_{inv\_i} \quad (i \in \{1,2,3\})$ in the AC-AC converter are synchronized in such a way that the overall switching function for the three converters is the same pure square wave with a fundamental frequency

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 E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 573-580.

of 20 kHz. Figure 3-2 depicts the sequence of switching functions to generate the modulation signal s_{sw} of the full bridge inverter in the AC-AC converter for phase "ab". Fig. 4 (a) and (b) show the

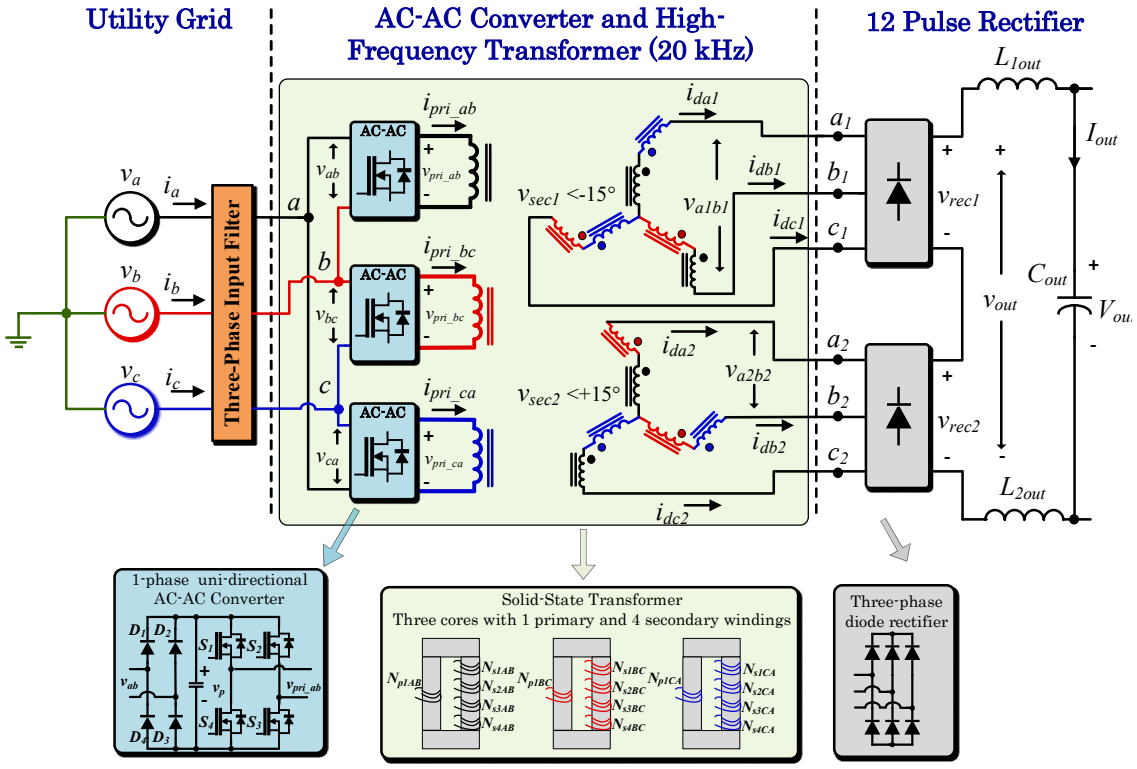

Figure 3-1 Proposed Single-Stage Three-Phase AC to DC Rectifier with High frequency Isolation. Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

line-to-line voltage v_{ab} and diode rectifier switching function s_{da} respectively. Notice that the multiplication of both results in v_{pa} depicted in Figure 3-2(c). Moreover, v_{pa} is applied to the full bridge inverter which has a switching function s_{inv_1} designed in such a way that $s_{da} \cdot s_{inv\_1} = s_{sw}$. Under this modulation scheme, the utility voltages are essentially being

multiplied with the overall HF (High-Frequency) switching function s_{sw} and thus a HF AC link is created at the output of each AC-AC converter as portrayed in Figure 3-2(f). Since the input phase voltages are displaced 120 degree and the three AC-AC converters have the same overall switching function s_{sw}, the voltages across the transformer windings sum to zero allowing the magnetic flux to be balanced. The blocking voltage of the semiconductor devices in the AC-AC converters must be rated for the peak of the utility line-to-line voltages.

The overall switching function of s_{sw} is given by equation (4) and the resulting voltage across the transformer winding connected to the AC-AC converter with phase "ab" is given by equation (3.5). In equation (3.4), D refers to the duty cycle and ω_s corresponds to the frequency of s_{sw}. Figure 3-3 (a) depicts signal s_{sw}. It can be seen that when $D < 0.5$ zero states are produced in this signal.

$$s_{sw} = \sum_{k=1}^{\infty} \frac{1}{k\pi}\left[\sin(2\pi kD) - \sin\left(2\pi k\left(\frac{1}{2}+D\right)\right)\right]\sin(k\omega_s t) + \cdots$$
$$\ldots + \frac{1}{2\pi k}\left(1 - \cos(2\pi kD) + \cos\left(k2\pi\left(\frac{1}{2}+D\right)\right) - \cos(k\pi)\right)\cos(k\omega_s t) \qquad (3.4)$$

$$v_{pr\ ab} = v_{ab} \cdot s_{sw} \qquad (3.5)$$

The voltages across the transformer windings connected to the AC-AC converters associated with phases "bc" and "ca" have the same expression except for a 120 degrees

phase shift. By inspecting (3.4) and (3.5) it can be seen that the fundamental frequency of the voltage across the transformer depends primarily on ω_s.

It is also evident that the three-phase HF AC link across the transformer windings are a function of the duty cycle D impliying that the output DC voltage can be regulated by adjusting the duty cycle of the AC-AC converters.

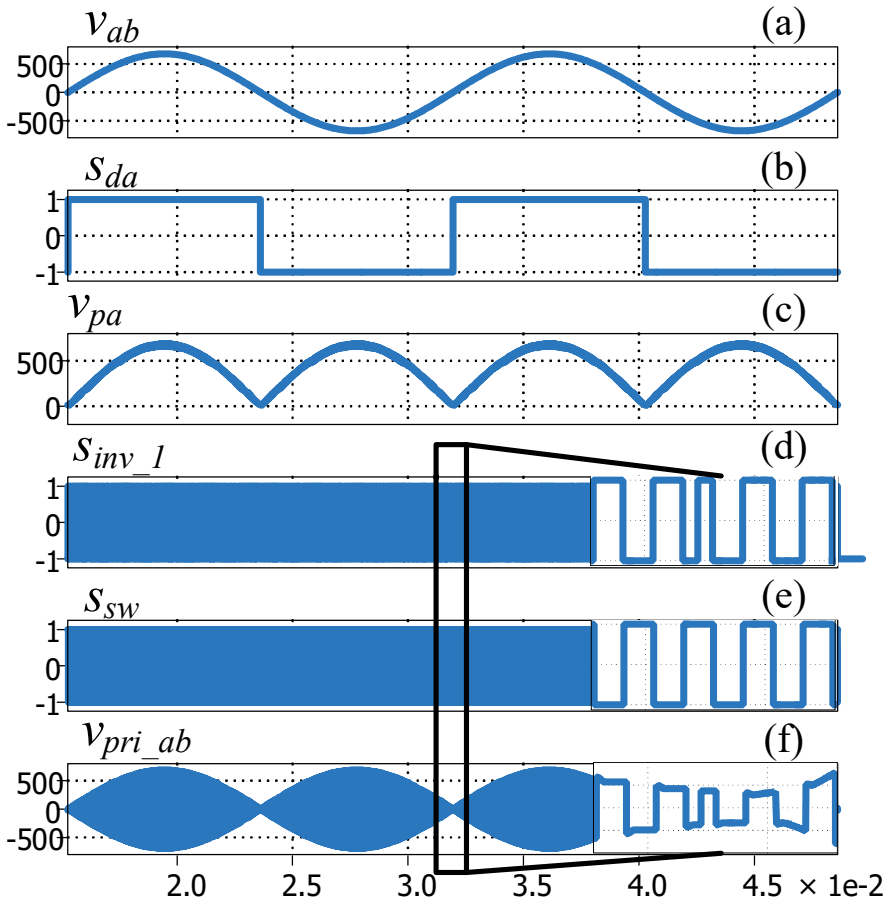

Figure 3-2 Switching functions and modulation signals of proposed topology (a) Line-to-line input voltage (b) Diode rectifier switching function (c) Rectified sine wave ($V_{AB} \cdot S_d$) (d) Inverter switching function (e) AC-AC overall switching function ($S_d \cdot S_{inv,1}$) (f) Primary winding HF voltage ($V_{AB} \cdot S_{SW}$)

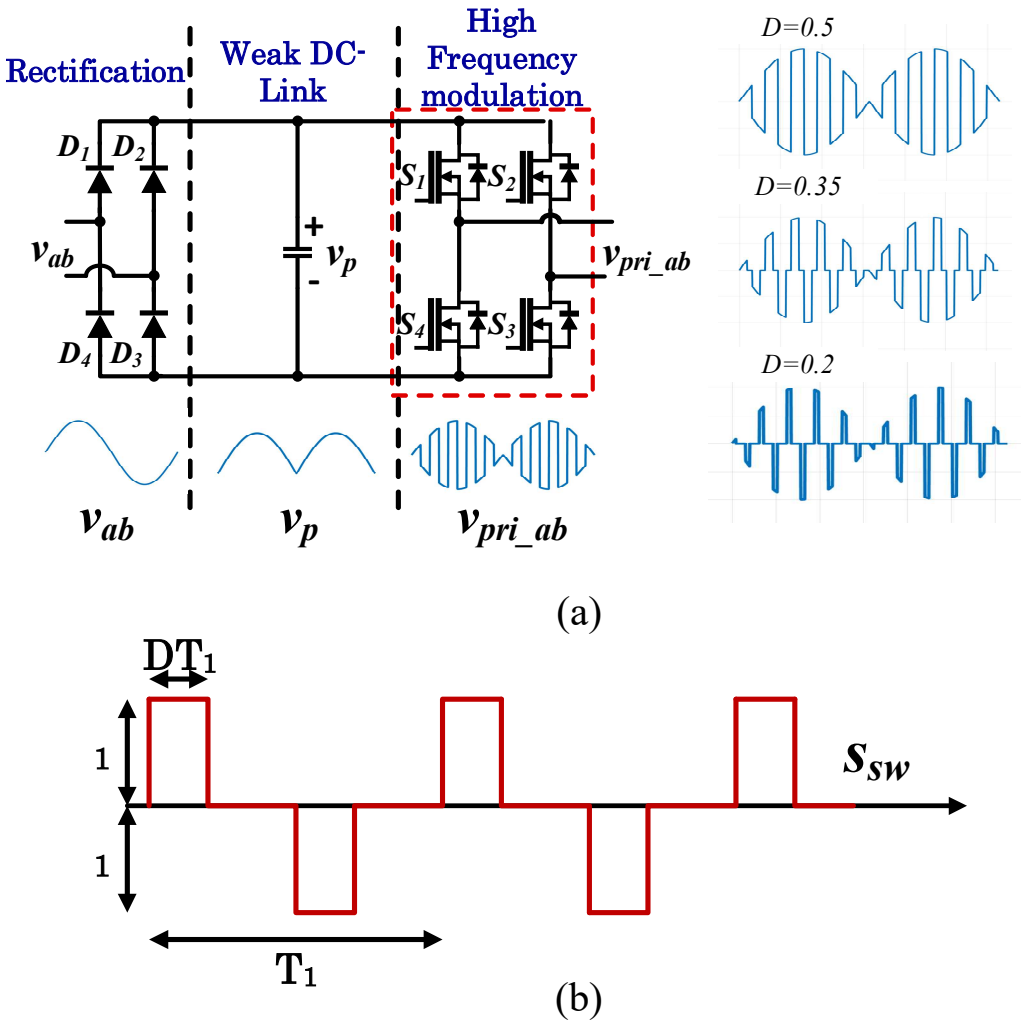

Figure 3-3 Operation principle of AC-AC converter modules (a) Modulation of full-bridge of each AC-AC converter changes the primary average voltage as a function of duty cycle D and (b) S_{sw} overall switching function of all three AC-AC converters. Notice that for the three AC-AC converters the switching function is the same.

At 50% duty cycle operation, the voltage across the transformer windings appears as in Figure 3-2(f). The maximum DC output voltage is obtained at 50% duty cycle. For duty cycles above 50%, short circuits across the pulsating DC voltage occurs and should be avoided. For duty cycles below 50%, zero states are introduced in the HF AC link voltages

and the output DC is decreased. Despite modulation simplicity, the utility line-to-line voltages must be sensed in order to determine their zero crossing points. The switching function s_{da} for each single-phase rectifier in the AC-AC converters can be determined from the zero crossing point information. After obtaining the respective switching functions s_{da}, s_{db}, s_{dc}, the switching functions of each full-bridge inverter, namely s_{inv1}, s_{inv} , s_{inv3}, can be synchronized to achieve an overall high frequency switching function s_{sw} that is the same for the three inverters.

3.1. Modulation scheme

Figure 3-4 depicts the modulation scheme used for the proposed topology for the case when $D = 0.5$. Referring to Figure 3-4 C1 and C2 are two high frequency sawtooth carriers phase shifted by 180 degrees from each other. During the positive cycle of the input voltage v_{ab}, the carrier C_1 is compared with a reference D(duty cycle) to generate the signal N_2 which correspond to the gating signals of S_1 and S_3 during the positive cycle. Similarly, the carrier C_2 is compared with D to generate the signal N_3 which correspond to the gating signals for S_2 and S_4 during the positive half cycle. On the other hand, during the negative cycle, the gating signals logic is exchanged i.e. the carrier with C_1 now generates the gating signals for S_2 and S_4 and carrier C_2 generates the signals for S_1 and S_3 respectively. By using this modulation scheme, the switching function of the full bridge inverter in the primary side results in the switching function S_{inv_1} as shown in Fig.4 (d) for $D = 0.5$.

Notice that for the case when $D = 0.5$ signals N_2 and N_3 are complementary. However, this does not hold for the case when $D < 0.5$ as depicted in Figure 3-5. This is the reason why two sawtooth carriers need to be use in practice to be able to change the value of D. Figure 3-6 depicts the logic circuits to obtain the gating signals S_1, S_2, S_3 and S_4 for $D \leq 0.5$. It is also important to mention that in order to keep near-perfect volt-second balance during each line frequency cycle, the switching frequency of the AC-AC converters must be a multiple of the line frequency. In addition, the HF PWM signals from the full bridge inverters must be synchronized with respect to one of the line-to-line voltages at the input. By taking these last considerations, failures due to transformer core saturation are avoided.

3.2. 12-Pulse Diode Rectifier

Two sets of three-voltages v_{a1}, v_{b1}, v_{c1} and v_{a2}, v_{b2}, v_{c2} are fed to the 12-pulse diode rectifier. These sets of voltages have a fundamental frequency close to 20 kHz and are phase shifted 30 degrees from each other with respect to their line-frequency modulating voltages (sine wave envelope). This phase shift enables a 12-pulse DC output voltage and elimination of low order current harmonics on the utility side. The operation of the 12-pulse diode rectifier is similar to the conventional line frequency multi-pulse systems. The main difference is that the 12-pulse diodes must switch at 20kHz. Therefore, fast switching frequency diodes must be used in this topology.

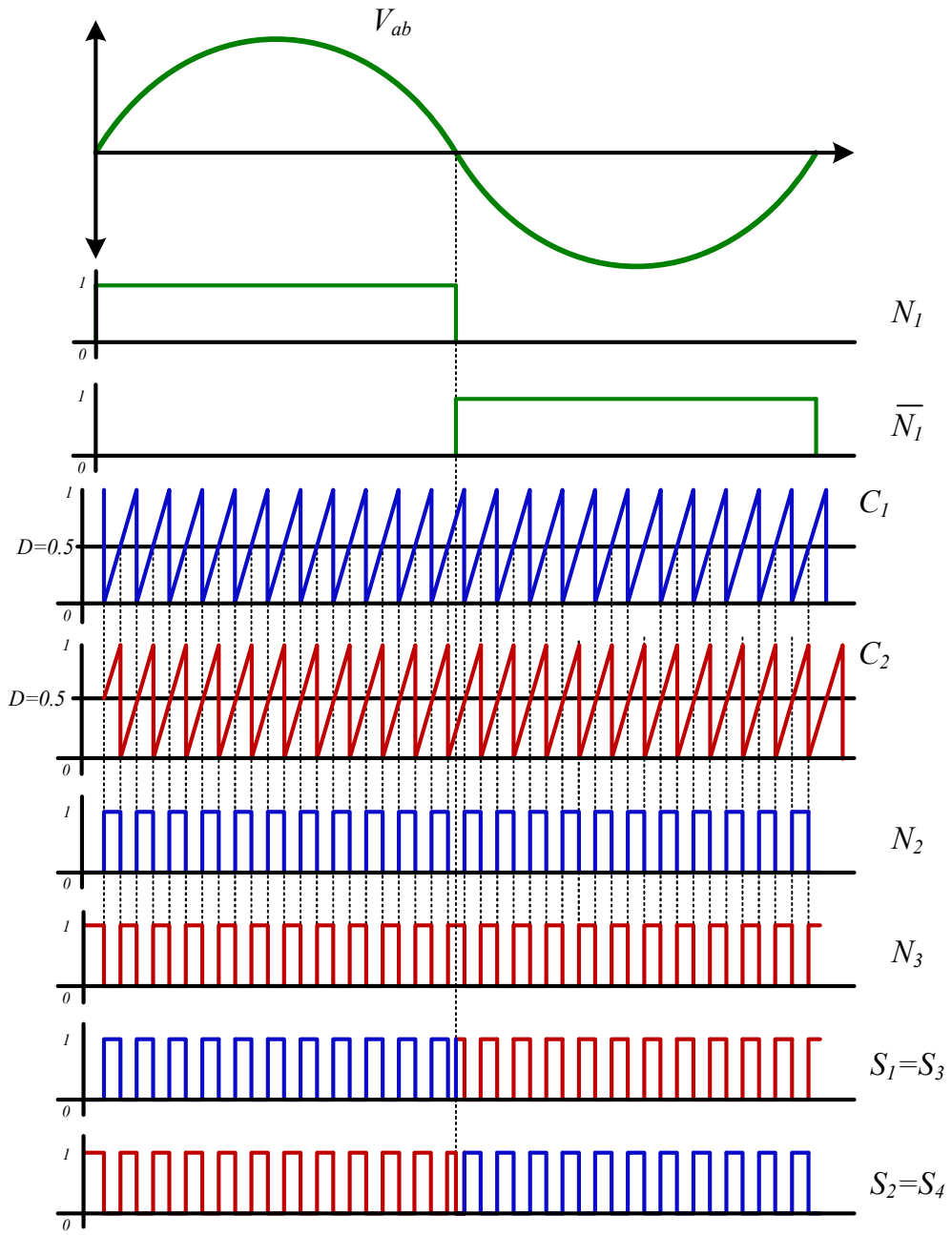

Figure 3-4 Modulation scheme for $D = 0.5$. N_1 and $\overline{N_1}$ represent the sign of the line-to-line voltage and its complementary signal respectively. C_1 and C_2 are the high-frequency carries implemented as counting up saw tooth signals phase shifted 180° from each other. Each carrier is compare with the duty cycle value to generate signals N_2 and N_3 which are complementary for the case when $D = 0.5$. By using logic combinations of N_1 , $\overline{N_1}$, N_2, and N_3 the gating signals for switches S_1, S_2, S_3, and S_4 are obtained.

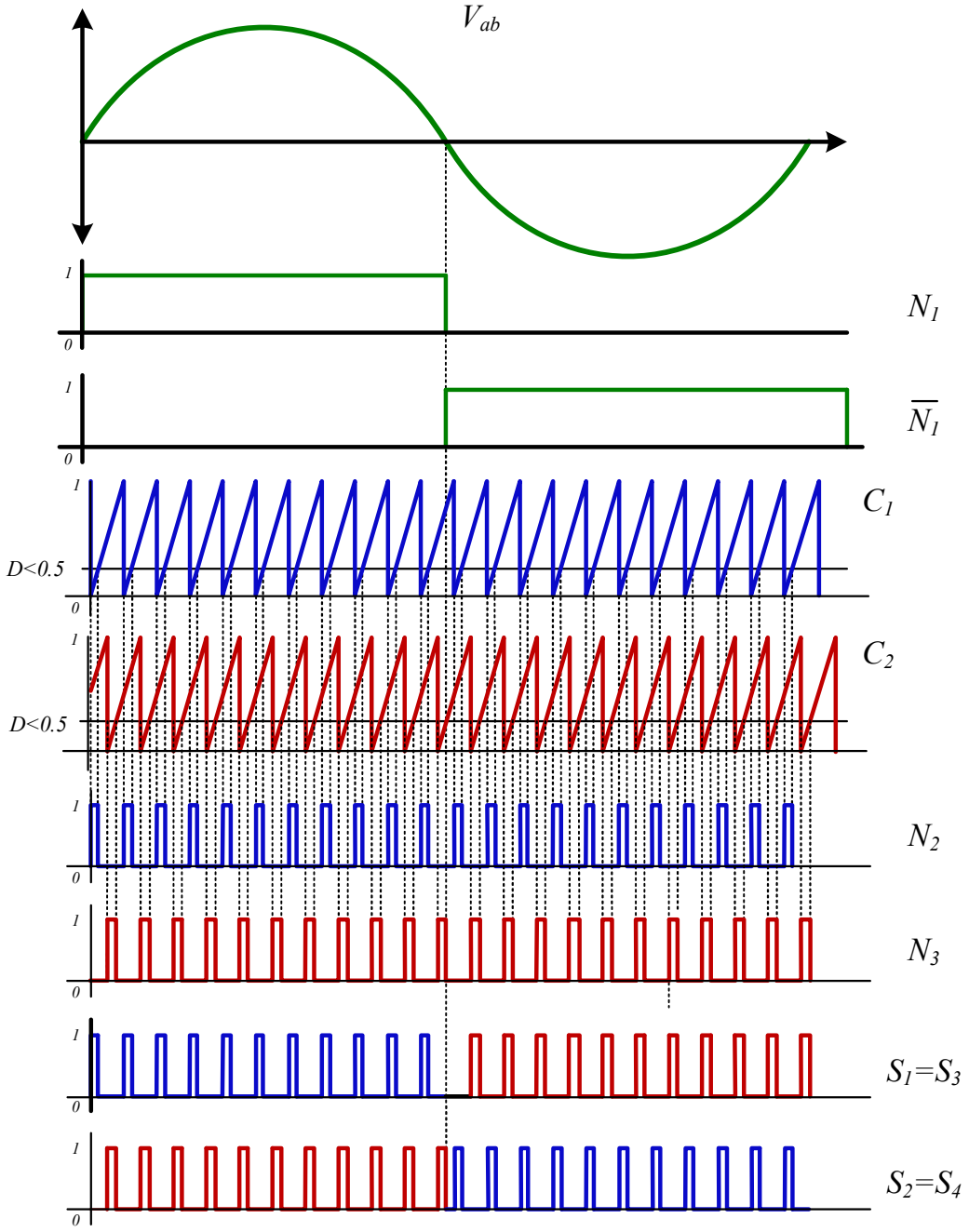

Figure 3-5 Modulation scheme for $0 < D < 0.5$. In this case N_2 and N_3 are not complementary signals from each other.

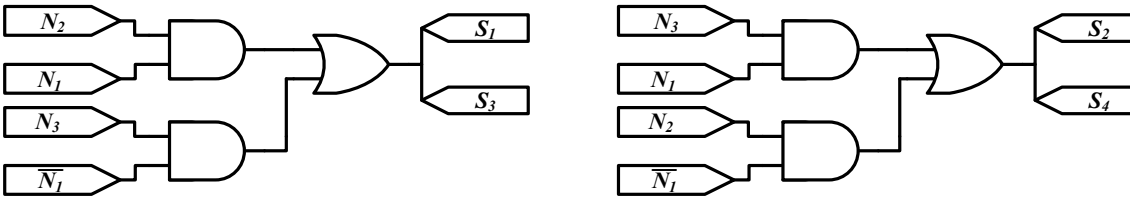

Figure 3-6 General logic for proposed modulation scheme when for $0 \leq D \leq 5$

3.3. Output Voltage Analysis

The output voltage produced by the 12-pulse diode rectifier is the sum of voltages v_{rec1} and v_{rec2} and is described by (3.6), where v_{rec1} and v_{rec2} are the individual voltages produced by each six-pulse diode rectifier.

$$v_{out} = v_{rec1}(\omega t) + v_{rec2}(\omega t) \tag{3.6}$$

In a conventional three-phase diode rectifier, the switching function of the diodes is defined by equation (3.7).

$$s_d(\omega t) = \sum_{n=1,3,5,7\ldots}^{\infty} \left(\frac{4}{n\pi}\cos\left(\frac{n\pi}{6}\right)\right) \cdot \sin(n\omega t) \tag{3.7}$$

This switching function is modulated by s_{sw} producing a high frequency switching function. For ease of manipulation, the new switching function of the three-phase diode rectifier with high frequency input voltage s_{dHF} is defined as indicated in equation (3.8).

$$s_{dHF} = s_d(\omega t) \cdot s_{sw} \tag{3.8}$$

In these equations s_{sw} refers to the square wave switching function described by equation (3.4).

With these definitions, the voltage v_{rec1} can be written as follows:

$$v_{rec1}(\omega_s t) = v_{a1}s_{dHF} + v_{b1}s_{dHF} + v_{c1}s_{dHF} \tag{3.9}$$

The voltages v_{a1}, v_{b1}, v_{c1} represent the secondary side line-to-neutral voltages of the zig-zag windings creating a -15 degree phase shift. These secondary side voltages are expressed in equations (10-12) respectively assuming ideal conditions (i.e. no voltage drops in the semiconductor devices in the primary side).

$$v_{a1} = \sqrt{2}V_{LL}\sin\left(\omega t - \frac{\pi}{12}\right)\cdot s_{sw} \tag{3.10}$$

$$v_{b1} = \sqrt{2}\,V_{LL}\sin\left(\omega t - \frac{\pi}{12} - \frac{2\pi}{3}\right)\cdot s_{sw} \tag{3.11}$$

$$v_{c1} = \sqrt{2}V_{LL}\sin\left(\omega t - \frac{\pi}{12} + \frac{2\pi}{3}\right)\cdot s_{sw} \tag{3.12}$$

Notice that the secondary voltages are also modulated by s_{sw}; thus having a high frequency behavior.

Substituting equations (3.8) and (3.10-3.12) into equation (3.9) yields:

$$v_{rec1} = s_{sw}\cdot s_{sw}\cdot\sqrt{2}V_{LL}\begin{bmatrix}\sin\left(\omega t - \frac{\pi}{12}\right)s_d\left(\omega t - \frac{\pi}{12}\right)\\ +\sin\left(\omega t - \frac{\pi}{12} - \frac{2\pi}{3}\right)s_d\left(\omega t - \frac{\pi}{12} - \frac{2\pi}{3}\right)\\ +\sin\left(\omega t - \frac{\pi}{12} + \frac{2\pi}{3}\right)s_d\left(\omega t - \frac{\pi}{12} + \frac{2\pi}{3}\right)\end{bmatrix} \tag{3.13}$$

From equation (13), it can be noticed that both high-frequency components of the diodes switching function and secondary voltages multiply each other resulting in a signal $s_{sw}\cdot$

s_{sw}. From Fig. 5 (b) it can be seen that $s_{sw} \cdot s_{sw}$ is a square wave of double the frequency of s_{sw} which has an average DC value given by $2D$.

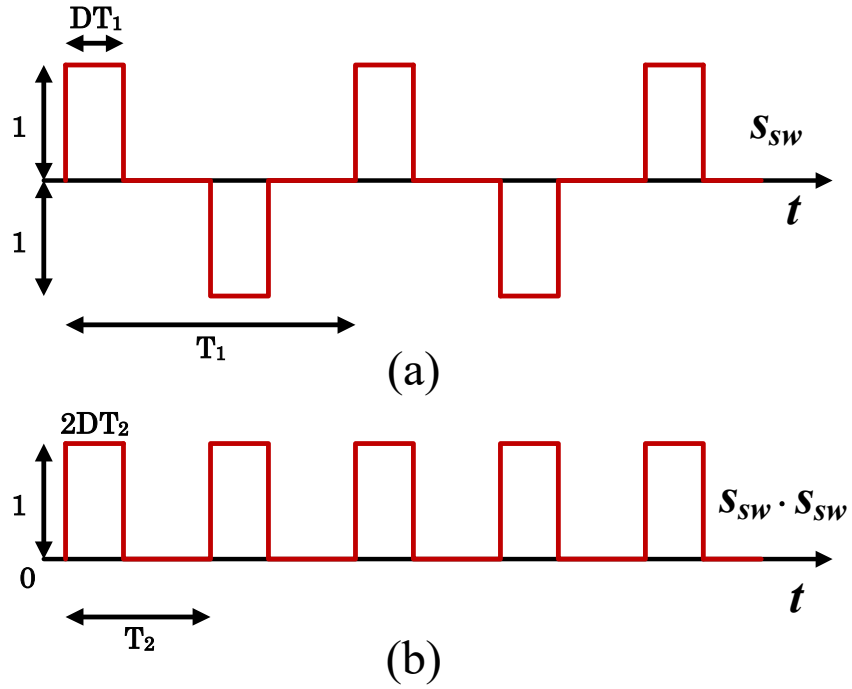

Figure 3-7 (a) High frequency quasi-square wave switching function S_{sw} and (b) high-frequency switching function $S_{sw} \cdot S_{sw}$ modulating the secondary output signals. Notice that the $T_1 = 2T_2$; thus , the secondary voltages and currents have two-times the high-frequency component. Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

Equation (3.13) can be simplified to the conventional six-pulse rectifier equation resulting in (3.14).

$$v_{rec1} = s_{sw} \cdot s_{sw} \cdot \frac{3\sqrt{2}}{\pi} V_{LL} \left[1 - \sum_{n=1}^{\infty} \frac{2}{36n^2 - 1} \cos(6n\omega t) \right] \qquad (3.14)$$

v_{rec2} can be derived using the same idea that $s_{sw} \cdot s_{sw}$ will be multiplied by the conventional six-pulse function, but in this case a +15 degree phase shift is considered; therefore, the sum of both v_{rec1} and v_{rec2} will generate a signal with spectral components at 12 times the line frequency multiplied by the high frequency modulating signal $s_{sw} \cdot s_{sw}$ resulting in equation (3.15).

$$v_{out} = s_{sw} \cdot s_{sw} \cdot \frac{6\sqrt{2}}{\pi} V_{LL} \left[1 - \sum_{n=1}^{\infty} \frac{2}{144n^2 - 1} \cos(12n\omega t) \right] \tag{3.15}$$

Since $s_{sw} \cdot s_{sw}$ has a DC component given by $2D$ as depicted in Figure 3-7 (b), the amplitude of the DC value of the 12-pulse output and the respective harmonics inside the brackets are scaled down by changing the value of *D*. Therefore, the DC output voltage input-output relationship is given by equation (16) where V_{LL} corresponds to the line-to-line RMS input voltage and with $0 < D \leq 0.5$. This shows that the proposed converter is a buck-type rectifier topology.

$$V_{out} = \frac{12D\sqrt{2}}{\pi} V_{LL} \tag{3.16}$$

Likewise, harmonic components at $(2k\omega_s \pm 12n\omega)$ will be generated by interaction of the function $s_{sw} \cdot s_{sw}$ with the low order harmonics inside the brackets of equation (3.15). These high frequency components generate a chopped 12-pulse voltage at the output, which means that high frequency SiC diodes are required for practical implementation of this topology.

3.4. HF Ferrite Core Transformer

The HF ferrite core transformer plays an important role in the power density of the proposed topology. The switching frequency of the AC-AC converters determines the transformer operation frequency. The selection of the switching frequency must take into account the tradeoff between power density and efficiency. Although increasing the frequency of operation reduces the size of the transformer, it also increases the core losses of the transformer and switching losses from the devices.

Selection of the appropriate magnetic core is essential to achieve high power density and high efficiency. For MF applications, magnetic core materials such as ferrite, amorphous, and silicon steel cores exhibit significant core losses. Therefore, a silicon steel core is not suitable for this application. Amorphous and ferrite materials exhibit high resistivity in a wide frequency range and are good alternatives for 20 kHz operation [28]. Compared to amorphous materials ferrite is considerably cheaper. Taking into account the price of the core material, a ferrite core material (3C94) was selected for the transformer core of this project.

The transformer was built using three independent two-limb transformers employing ferrite blocks to form a core structure as shown in Fig. 6. This structure allows the transformer to avoid core saturation due to unbalanced flux.

The transformer consists of three primary windings, one per phase, and a total of 12 secondary windings to achieve a 30 degree phase shift to feed two sets of three phase diode rectifiers (refer to Figure 3-1). The secondary windings are connected in zig-zag fashion

to result in a 30 degree phase shift. The turn ratios between primary and secondary windings are given in equation (3.17).

In a conventional 12-pulse rectifier a star-delta winding connection is used in the secondary side to generate a net 30° phase shift difference. However, this approach can generate differences in the leakage inductances of the terminals feeding the three-phase rectifiers at the output.

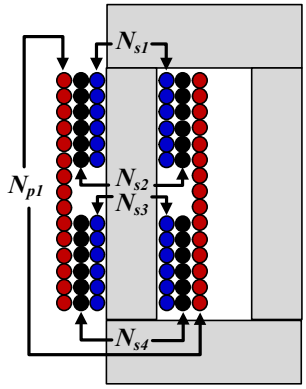

Figure 3-8 High-Frequency Ferrite core transformer. Each phase is connected independently to a two-limb transformer with N_{p1} turns at the primary and four secondary windings with N_{s1}, N_{s2}, N_{s3}, N_{s4} representing the number of turns respectively. Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

This leakage inductance difference is due to the unequal turn ratio in the star-delta connected windings. Moreover, this issue leads to unequal current sharing between the diode bridges. To solve this problem, the transformer can be connected in a zig-zag arrangement. A transformer connected in zig-zag possess balanced leakage inductances on the secondary side because the turns-ratio of the windings per phase is the same. The proposed HF transformer consist of two zig-zag connections on the secondary side, each

one creating a set of three-phase voltages that feed the output six-pulse rectifiers. The two sets of three-phase voltages out the zig-zag connection have a 30° phase shift with respect to each other. One of the zig-zag connections creates a set of three-phase voltages with +15° phase difference with respect to the primary side voltages. Likewise, the second zig-zag connections creates a set of three=phase voltages with a -15° phase difference with respect to the primary side voltages.

A phasor diagram of the primary side windings and the secondary windings is shown in Figure 3-9. It can be seen that in this case the line-to-line voltages from an equilateral triangle. For the mathematical analysis voltage V_{an} was chosen as the reference i.e. its phase angle is equal to zero.

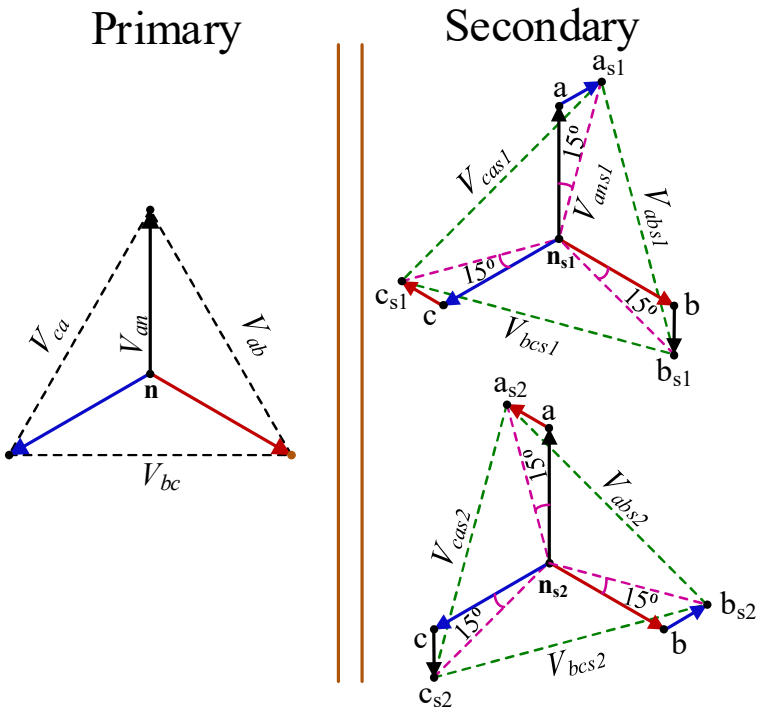

Figure 3-9 Phasor diagram of zig-zag transformer connection

The phasor expressions for V_{bn} V_{cn}, V_c and V_{ca} are given below.

$$V_{an} = 1\angle 0°$$

$$V_{bn} = 1\angle -120°$$

$$V_{cn} = 1\angle +120°$$

$$V_{ab} = \sqrt{3}\angle 30°$$

$$V_{bc} = \sqrt{3}\angle -90°$$

$$V_{ca} = \sqrt{3}\angle 150°$$

As mentioned before, one of the three-phase output sets will be shifted $-15°$ with respect to the primary voltages. To achieve that, two scaled down vectors at the secondary side are used as depicted in the Figure 3-9. For example in Figure 3-9 the vector V_{as} is gotten by the sum of scaled down vectors V_{as1} and V_{cs1}. The factors that will scale those vectors are given by the turn ratios of the corresponding secondary windings. For the first zig-zag secondary output the turn ratios can be calculated as follow:

$$N_{s1}V_{an} - N_{s2}V_{cn} = N_{s1}\angle 0° - N_{s2}\angle 120° = 1\angle -15° \qquad (3.17)$$

Which is a 2 equations 2 unknown system that we have to solve for N_{s1} and N_{s2}. Likewise, for the zig-zag secondary outputs rotated $+15°$ are obtained by the sum of scaled vector V_{at} and V_{bt}. By referring to Figure 3-9. we can notice that the equations to solve for this case are given by (3.18)

$$N_{s3}V_{an} - N_{s4}V_{bn} = N_{s1}\angle 0° - N_{s2}\angle -120° = 1\angle +15° \tag{3.18}$$

Notice that for the equations (3.17) and (3.18) were obtained in such a way that the secondary side line-to-neutral voltage V_{ans} has the same magnitude the is primary side counterpart. However, in this specific application the primary side will connected in a line-to-line arrangement. Since the secondary side voltages connected to the diode rectifiers are the line-to-neutral voltage, the turn ratio values must include an additional factor $\frac{1}{\sqrt{3}}$ to have a 1:1 proportion between the line-to-line primary voltage and the line-to-neutral secondary voltage. Therefore, equations (3.17) and (3.18) are modified as follow

$$N_{s1}V_{an} - N_{s2}V_{cn} = N_{s1}\angle 0° - N_{s2}\angle 120° = \frac{1}{\sqrt{3}}\angle -15° \tag{3.19}$$

$$N_{s3}V_{an} - N_{s4}V_{bn} = N_{s1}\angle 0° - N_{s2}\angle -120° = \frac{1}{\sqrt{3}}\angle +15° \tag{3.20}$$

By solving for N_{s1} N_{s2} N_{s3} N_{s4} the turn ratio values to generate the respective $-15°$ and $+15°$ phase shift are

$$N_{s1} = \frac{\sqrt{2}}{3}$$

$$N_{s2} = \frac{\sqrt{3}-1}{3\sqrt{2}}$$

$$N_{s3} = \frac{\sqrt{2}}{3}$$

$$N_{s4} = \frac{\sqrt{3}-1}{3\sqrt{2}}$$

Finally, the turn ratios are obtained

$$N_{P1}: N_{s1}: N_{s2}: N_{s3}: N_{s4} =$$
$$1: K_t \cdot \frac{\sqrt{2}}{3}: K_t \cdot \frac{\sqrt{3}-1}{3\sqrt{2}}: K_t \cdot \frac{\sqrt{2}}{3}: K_t \cdot \frac{\sqrt{3}-1}{3\sqrt{2}} \quad (3.21)$$

$$1: K_t \cdot \frac{\sqrt{2}}{3}: K_t \cdot \frac{\sqrt{3}-1}{3\sqrt{2}}: K_t \cdot \frac{\sqrt{2}}{3}: K_t \cdot \frac{\sqrt{3}-1}{3\sqrt{2}}$$

Where K_t is a constant designed according to the desired DC output (V_{out}) of the converter and the given input line-to-line RMS voltage, V_{LL}:

$$K_t = \frac{\pi \cdot V_{out}}{6\sqrt{2}V_{LL}} \quad (3.22)$$

3.5. Input Current Analysis

Through mathematical analysis it is demonstrated that the utility input current's dominant harmonics are the 11th and 13th. Lower order harmonics e.i. 5th and 7th are eliminated by the 30 degree phase shift in the zig-zag transformer connections. To perform the analysis, the output current I_{out} is assumed to be ideally DC. Analysis is shown for phase "a". The utility input current is given by equation (3.23), where s_{sw} refers to the AC-

AC converter overall switching function given in equation (3.4) and i_{pri_ab} is the current flowing through the primary winding.

$$i_a = s_{sw} \cdot i_{pri\_ab} \tag{3.23}$$

By VA balance, a relationship between the primary side and secondary side currents is obtained. In equation (3.24), N_p refers to the number of turns in the primary winding and $N_{s1ab}, N_{s2ab}, N_{s3ab}, N_{s4ab}$ refer to the number of turns in the secondary windings associated with phase "ab". The turns-ratio relation in (3.21) is used in (3.24). Similarly, i_{as} , $i_{as2}, i_{as3}, i_{as4}$ are the currents flowing through the secondary windings associated with phase "a"; these currents can be expressed in terms of the currents flowing through the output six-pulse diode rectifiers as follows:

$$N_p i_{pri\_ab} = N_{s1ab} i_{as} + N_{s2ab} i_{as} + N_{s3a}\ i_{as3} + N_{s4ab} i_{as4} \tag{3.24}$$

$$i_{as1} = i_{da} \tag{3.25}$$

$$i_{as2} = -i_{d1b} \tag{3.26}$$

$$i_{as} = i_{d2a} \tag{3.27}$$

$$i_{as} = -i_{d2c} \tag{3.28}$$

Substitution of (3.25-3.28) into (3.24) results in (3.29):

$$i_{pri\_ab} = N_{s1}(i_{da} + i_{da2}) - N_{s2}(i_{db} + i_{dc2}) \tag{3.29}$$

The currents flowing through the output diode rectifiers (i.e. i_{da} , i_{da} , i_{db2}, i_{dc2}) have a quasi-square wave nature as determined by (3.30) but also have the overall switching function s_{sw} operating on them. These currents are given by (3.31-3.34) respectively.

$$s_{di} = \sum_{n=1,3,5,7\ldots}^{\infty} \left(\frac{4I_{out}}{n\pi}\cos\left(\frac{n\pi}{6}\right)\right)\sin(n\omega t) \tag{3.30}$$

$$i_{da1} = s_{di}\left(\omega t - \frac{\pi}{12}\right)\cdot s_{sw} \tag{3.31}$$

$$i_{db} = s_{di}\left(\omega t - \frac{\pi}{12} - \frac{2\pi}{3}\right)\cdot s_{sw} \tag{3.32}$$

$$i_{da2} = s_{di}\left(\omega t + \frac{\pi}{12}\right)\cdot s_{sw} \tag{3.33}$$

$$i_{dc} = s_{di}\left(\omega t + \frac{\pi}{12} + \frac{2\pi}{3}\right)\cdot s_{sw} \tag{3.34}$$

The -15 and +15 phase shift is evident from (3.31) to (3.34). Substituting equations (3.31-3.34) into (3.29) yields:

$$i_{pri\_ab} = s_{sw}\cdot\left\{\begin{matrix} N_{s1ab}\left[s_{di}\left(\omega t - \frac{\pi}{12}\right) + s_{di}\left(\omega t + \frac{\pi}{12}\right)\right] - \\ N_{s2ab}\left[s_{di}\left(\omega t - \frac{\pi}{12} - \frac{2\pi}{3}\right) + s_{di}\left(\omega t + \frac{\pi}{12} + \frac{2\pi}{3}\right)\right] \end{matrix}\right\} \tag{3.35}$$

Then from (3.23), the utility input current, i_a , is given by:

$$i_a = s_{sw}\cdot s_{sw}\left\{\begin{matrix} N_{s1ab}\left[s_{di}\left(\omega t - \frac{\pi}{12}\right) + s_{di}\left(\omega t + \frac{\pi}{12}\right)\right] - \\ N_{s2ab}\left[s_{di}\left(\omega t - \frac{\pi}{12} - \frac{2\pi}{3}\right) + s_{di}\left(\omega t + \frac{\pi}{12} + \frac{2\pi}{3}\right)\right] \end{matrix}\right\} \tag{3.36}$$

Simplification of the terms inside the brackets of equation (3.36) yield to the conventional 12-pulse current expression resulting in:

$$i_a = s_{sw}\cdot s_{sw}\cdot\frac{4\sqrt{3}I_{out}}{\pi}\left\{\begin{matrix} \sin(\omega t) + \frac{1}{11}\sin(11\omega t) + \frac{1}{13}\sin(13\omega t) \\ + \frac{1}{23}\sin(23\omega t) + \frac{1}{25}\sin(25\omega t) + \cdots \end{matrix}\right\} \tag{3.37}$$

From equation (33), it is evident that the utility input current has a 12-pulse behavior. The 5th, 7th, 17th, 19th, etc. harmonics are eliminated. This analysis demonstrates that the

proposed topology has a high input current quality, which facilitates compliance with IEEE-519 harmonic standards. For $D < 0.5$ the term $s_{sw} \cdot s_{sw}$ on (3.37) produces frequency components at DC and even harmonics of ω_s (i.e. $2\omega_s$, $4\omega_s$, $6\omega_s$, $8\omega_s$, etc.). These frequency components interact with the fundamental frequency and with low order current harmonics of the utility current (i.e. 11ω, 13ω, 23ω, 25ω, etc.). Since the intended switching frequency is 20 kHz, the harmonics being produced by varying the duty cycle occur at high frequencies and the lower order harmonics remain intact. This means that regulating the output voltage by duty cycle control does not affect the input current quality. The theoretical THD of the utility input current is 16%. This is the same value for the conventional line frequency 12-pulse rectifier. Moreover, this same principle can be extended to 18- or 24-pulse converters to improve THD even further. Notice that the high frequency modulation of the line-to-line voltages will allow the design of a smaller phase shift transformer; thus, improving the power density of the system.

3.6. AC Input Filter Design

Due to the 12-pulse nature of the rectifier, an input LC filter has to be designed to handle low order harmonics (11^{th}, 13^{th} , etc.) Similar to the case presented in [7], a combination of LF harmonic traps tuned at 12^{th} and 24^{th} harmonics as discussed at [21] and [22]. For the high frequency switching harmonics, an additional LC filter has to be included tuned to filter out the harmonics at 2 times the switching frequency of the primary side of the converter. A per-phase circuit diagram of the proposed AC input filter is shown in Fig.7.

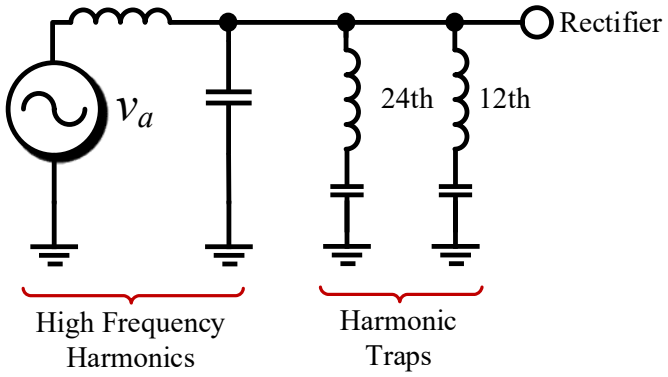

Figure 3-10 Per-phase equivalent circuit for AC input filter. Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

3.7. Output filter design

In order to operate the converter in Continuous Conduction Mode (CCM) the output inductance has to be properly designed.

For the conventional 12-pulse rectifier it is known that the DC output for a 6-pulse rectifier is given by

$$V_{out} = \frac{3\sqrt{2}}{\pi} V_{LL} \tag{3.38}$$

Lets assume that L and C at the output filter the signal $V_{ab} + V_{ab}$ are designed in such a way that a ripple free V_{out} is obtained

We can write the following equations:

$$V_{ab1} = \sqrt{2}\, V_{LL} \sin(\omega t) \tag{3.39}$$

$$V_{ab2} = \sqrt{2}\, V_{LL} \sin\left(\omega t - \frac{\pi}{6}\right) \tag{3.40}$$

$$V_d = \frac{6\sqrt{2}}{\pi}\, V_{LL} \tag{3.41}$$

From Fig. it can be seen that

$$\sqrt{2}\, V_{LL} \sin(\omega t) + \sqrt{2}\, V_{LL} \sin\left(\omega t - \frac{\pi}{6}\right) = \frac{6\sqrt{2}}{\pi}\, V_{LL} \tag{3.42}$$

Solving for ωt gives

$$\alpha = 1.681561\, rad$$

From the circuit's voltage loop

$$V_L + V_d - V_{ab} \; - V_{ab2} = 0$$

$$L\frac{di_L}{dt} + \frac{6\sqrt{2}}{\pi} V_{LL} - \sqrt{2} V_{LL} \sin\left(\omega t - \frac{\pi}{6}\right) - \sqrt{2} V_{LL} \sin(\omega t) = 0$$

$$i_L = \frac{1}{L}\int_{\alpha}^{\theta} (\sqrt{2}\, V_{LL} \sin(\omega t) + \sqrt{2}\, V_{LL} \sin\left(\omega t - \frac{\pi}{6}\right) - \frac{6\sqrt{2} V_{LL}}{\pi})\, d\omega t$$

By solving integration

$$i_L = \frac{\sqrt{2} V_{LL}}{L\omega}\left[\cos(\alpha) - \cos(\theta) + \cos\left(\alpha - \frac{\pi}{6}\right) - \cos\left(\theta - \frac{\pi}{6}\right) - \frac{6}{\pi}(\theta - \alpha)\right] \tag{3.43}$$

Where ω is the 60 Hz line-frequency.

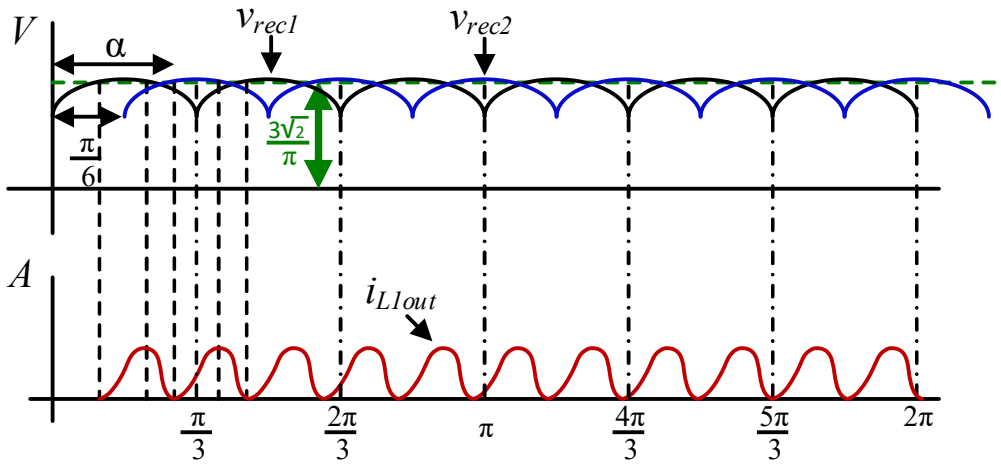

Figure 3-11 Design of minimum inductance for continuous conduction mode

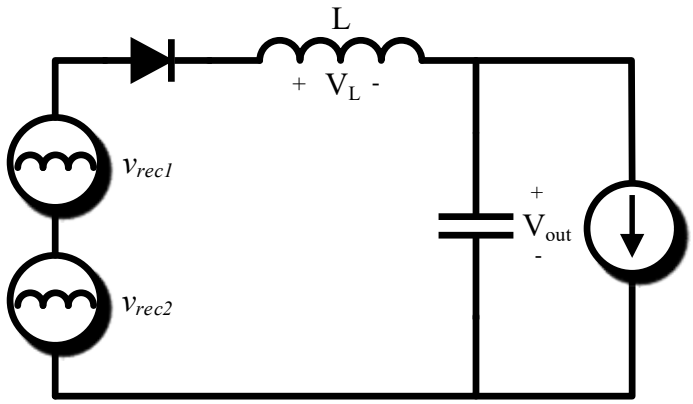

Figure 3-12 Equivalent circuit of 12 pulse rectifier

Once i_L is obtained we can calculate the average value of the signal and considering that

$$I_{out} = I_L \tag{3.44}$$

This means that the average value of i_L is the DC output current consumed by the load.

$$I_{out} = I_L = \frac{6}{\pi}\int_{\alpha}^{\alpha+\frac{\pi}{6}} i_L(\theta)d\theta$$

By Integrating

$$I_L = \frac{\sqrt{2}\,V_{LL}}{L\omega}\frac{6}{\pi} * (9.359719753 \text{ x } 10^{-4})$$

$$L_{min} = \frac{0.00252\,V_{LL}}{I_L\omega} \tag{3.45}$$

Equation (3.45) gives the equation to obtain the minimum inductance L_{min} to guarantee that the output current is continuous and operate the converter in CCM.

3.8. Voltage Regulation with Duty Cycle Control

One of the advantages of the proposed system is the simplicity of tis modulation and control scheme. From equation (3.4), it is clear that the output DC voltage can be regulated by duty cycle control. It was also determined that varying the duty cycle does not affect the utility input current. The output voltage is controlled by a simple proportional-integral (PI) controller. As observed in Figure 3-13, the error signal feeding the controller is the difference between the sensed output DC voltage and the desired voltage, V_{out}^{*}. Essentially, the PI controller dictates the required duty cycle operation to obtain the desired output voltage. This duty cycle value is fed to the modulation algorithm, which generates the gating signals for the switches S_n $(n \in \{1,2,3,4\})$ in the AC-AC converter.

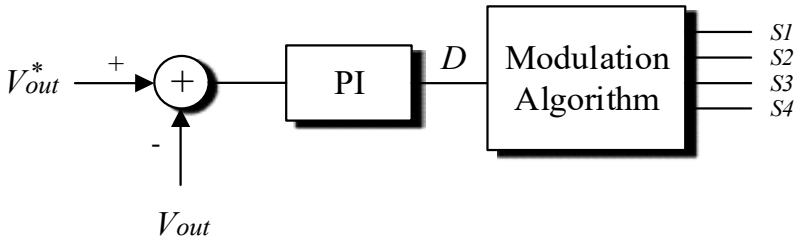

Figure 3-13 DC output voltage regulation block diagram. Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

3.9. Section Conclusion

In this section the proposed topology for a Level-3 EV charger was presented. The proposed topology was based on a 12-pulse rectifier topology. The modulation scheme of the proposed topology was discussed together with a mathematical analysis of voltage and currents. It was proved that the proposed topology has a DC output voltage with a high frequency behavior produced by the AC-AC converters at the primary side. Moreover, the input current harmonic cancelation characteristic from the line frequency 12-pulse was also proved to be conserved regardless of the high frequency behavior of the signals. On the other hand, an analysis of the high frequency transformer design was given along with the design of input and output filters for the overall system.

4. DESIGN EXAMPLE AND SIMULATION RESULTS

4.1. 50 kW Circuit design and simulation

A design example is presented below for a 480 V (line-to-line rms) input voltage, a maximum DC output of 500 V at 500 kW. The input voltage frequency is assumed to be 60 hz and the HF transformer is designed to operate at 20 kHz. Table 4-1 shows the specification values for this simulation example.

Table 4-1: Parameters for design example simulation

Operating conditions used for simulation in PLECS	
Grid voltage (line-to-line rms)	480 V rms
Grid frequency	60Hz
Output dc voltage	500 V
Rated power	50 kW
Switching Frequency	19.98 kHz
Input Inductor	25 µH
Output Inductor	320 µH
Output Capacitor	5 µF
Transformer K_t	0.38

In order to achieve a 500 V output the gain k_t can be calculated using equation (3.22)

$$K_t = \frac{\pi \cdot V_{out}}{6\sqrt{2}V_{LL}} = 0.38 \tag{4.1}$$

The turn ratio of the transformer can be calculated using equation (3.21)

$$N_{P1}: N_{s1}: N_{s2}: N_{s3}: N_{s4} = 1: K_t \cdot \frac{\sqrt{2}}{3}: K_t \cdot \frac{\sqrt{3}-1}{3\sqrt{2}}: K_t \cdot \frac{\sqrt{2}}{3}: K_t \cdot \frac{\sqrt{3}-1}{3\sqrt{2}} \tag{4.2}$$

Since k_t is known the values for N_{s1}, N_{s2}, N_{s3}, N_{s4} and thus the turn ratio between primary and secondary windings are obtained:

$$N_{P1}: N_{s1}: N_{s2}: N_{s3}: N_{s4} = 1: 0.1791: 0.0655: 0.1791: 0.0655 \quad (4.3)$$

To achieve CCM at 10% of rated load the output inductance can be calculated by assuming:

$$I_{out} = \frac{5\ kW}{500\ V} = 10\ A \quad (4.4)$$

Substituting in (3.45) gives

$$L_{min} = \frac{0.00252\ V_{LL}}{I_L \omega} = 320.85\ \mu H \approx 320\ \mu H \quad (4.5)$$

For this example we will only filter out the high-frequency components of the DC output voltage. Considering the value of L obtained in the previous stage and knowing that the cutoff frequency of a second order filter is given by

$$\omega_{co} = \frac{1}{\sqrt{LC}} \quad (4.6)$$

Since the switching frequency of the AC-AC converter was set at $20\ kHz$, the high frequency at the output of the rectifiers will be $40\ kHz$. Thus, to garatee that the high frequency component is filter out the cutoff frequency of the LC filter can be designed to be one tenth of $40\ kHz$ that is $4\ kHz$.

Therefore the value of the output capacitor will be

$$C = 4.94\ \mu F \approx 5 \mu F$$

Which can be approximated to $5\ \mu F$.

The proposed system was simulated to demonstrate its operation. Table 4-1 shows the parameters used for the numerical simulation. Figure 4-1 depicts the input current quality performance of the converter. Figure 4-1 (a) depicts the line-to-neutral voltage v_a and the input current i_a with a power factor of 0.98 due to the 12-pulse behavior. On the other hand, Figure 4-1(b) and (c) depict the utility input current, i_a, and its FFT repectively. Notice that i_a has a 12-pulse behavior with 5th and 7th harmonics eliminated as demonstrated in the previous section, and the 11th and 13th harmonics as the next most significant ones. Figure 4-2 shows the response of the system to a change of load. In Figure 4-2(d) , it can be noticed how the primary voltage changes its average value as a function of D shown in Figure 4-2(b) and, as a consequence, V_{out} is also affected as shown in Figure 4-2(c).

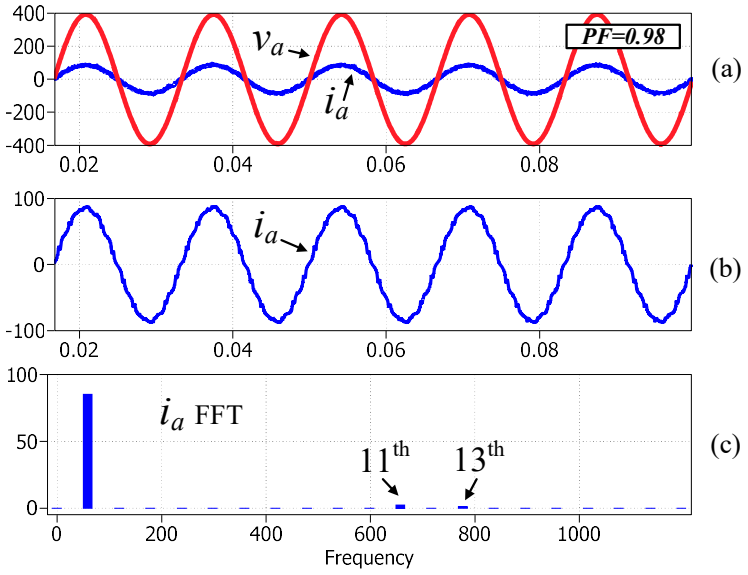

Figure 4-1 High-quality input current (a) v_a and i_a with a power factor of 0.98 for the proposed single-stage rectifier, (b) 12-pulse input current behavior of i_a and (c) Input current i_a FFT with 5th and 7th harmonics elimination

From the input current analysis, it was proved that the high frequency components do not affect the harmonic content of the current; however, THD is affected as the output power decreases far from the designed rated values. Figure 4-3 depicts a more detailed graphic of the THD and output voltage V_{out} behavior with respect to changes in the duty cycle D. It can be noticed that for changes between $D = 0.2$ and $D = 0.5$ the THD performance is maintained below 10% of THD; however, the harmonics content at the utility is affected at light load conditions.

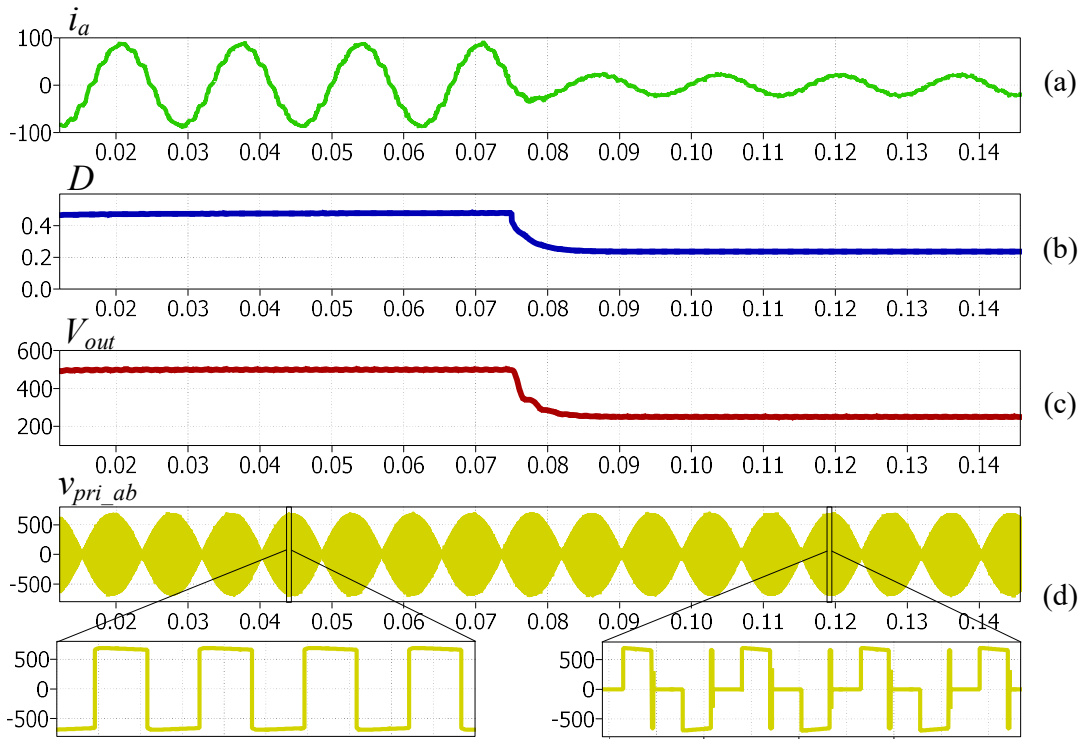

Figure 4-2 DC output change of load response from 50 kW to 10 kW (a) Input current i_a (b) Control signal D (c) DC output voltage V_{out} and (d) pirmary side high-frequency voltage v_{pri_ab}

Figure 4-4 depicts the primary side voltages modulated with a high frequency component due to the AC-AC converter switching function S_{sw}. Figure 4-5 depicts the FFT of the

three primary voltages v_{pru_ab}, v_{pri_bc} and v_{pri_ca}. From Figure 4-5(a) it can be noticed that the high frequency components are located at odd multiples of $\omega_s \pm \omega$. Figure 4-5(b) shows a zoom in capture of the first set of harmonics located at 19920 and 20040 Hz respectively. Figure 4-6 depicts the results obtained for the secondary voltages v_{a1b1} and v_{a2b2}. Notice that a 30° phase shift was introduced by the zig-zag transformer to

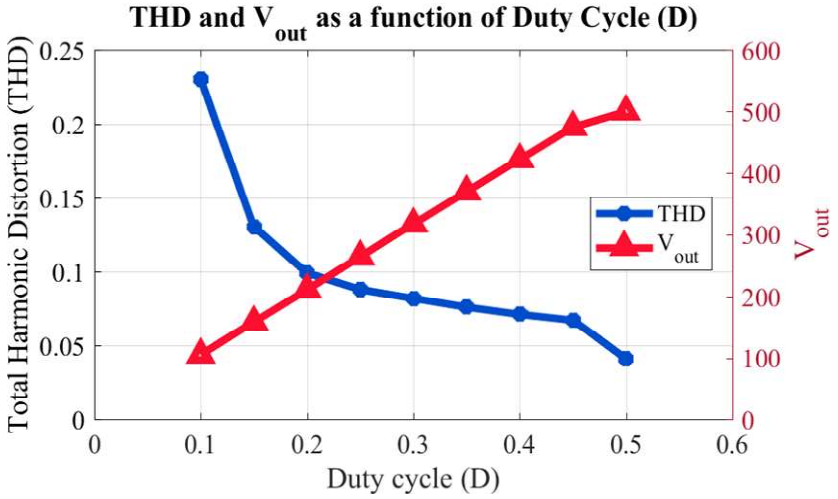

Figure 4-3 Total Hamonic Distortion (THD) and voltage output V_{out} as a function of duty cycle

generate the 12-pulse behavior at the DC output. Figure 4-7 depicts currents i_{da1} and i_{da2} (refer to Figure 3-1) which present a high frequency behavior as discussed in previous sections. Similar to the case with voltages v_{a1b1} and v_{a2b2}, a 30 ° phase shift is presented between current. Figure 4-8 depicts the output voltages v_{rec1}, v_{rec2} and v_{out} which have a high frequency behavior as discussed before. Figure 4-9 depicts the FFT of v_{rec1} and v_{rec2} from which it can be verified that the switching frequency of the high frequency switching function $S_{sw} * S_{sw}$ is 2 times of S_{sw} original switching frequency. Finally, an step response of the output voltages v_{rec1}, v_{re} and v_{out} is shown in Figure 4-10. It can

be noticed that the output voltage V_{out} is defined by the average value of v_{out} i.e. as the pulse widths of v_{out} decrees, the voltage output degreases and vice versa.

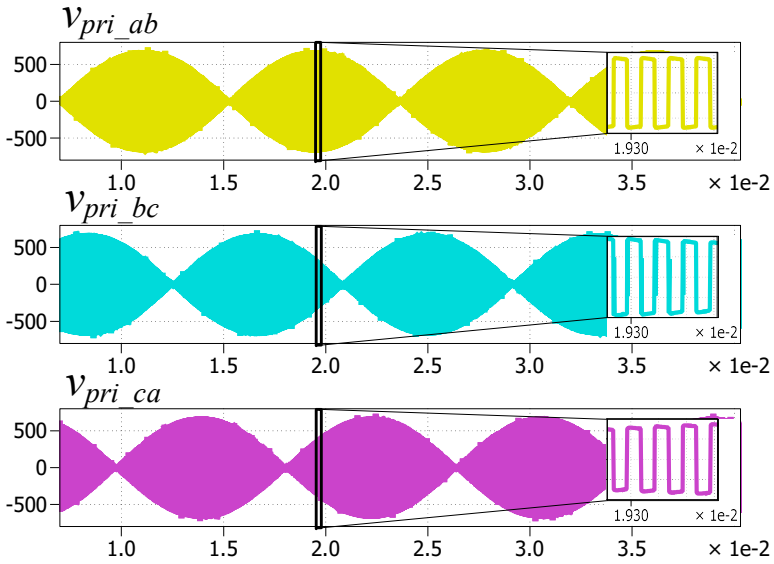

Figure 4-4 Primary side voltages v_{pru_ab}, v_{pri_bc} and v_{pri_ca}. Notice that the voltages have a high frequency component due to S_{sw} at $\omega_s = 19980$

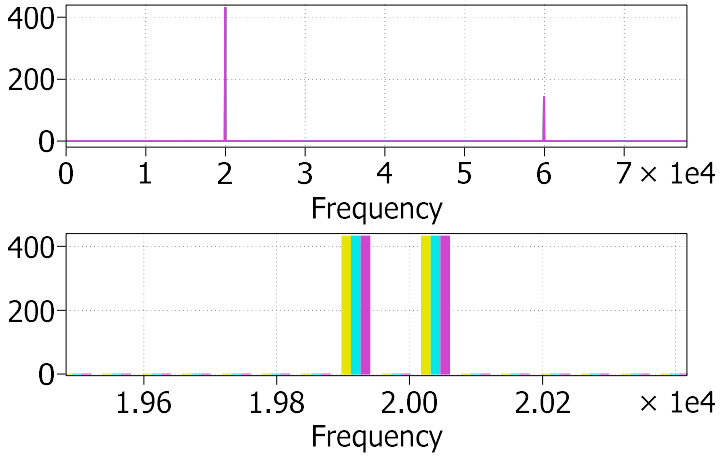

Figure 4-5 FFT of v_{prim_ab} , v_{prim_bc} , v_{prim_ca} it can be seen that the primary voltage have high frequency components at $\omega \pm \omega_s$ for odd numbers. In this case $\omega = 60\ Hz$ amd $\omega_s = 19980\ Hz$

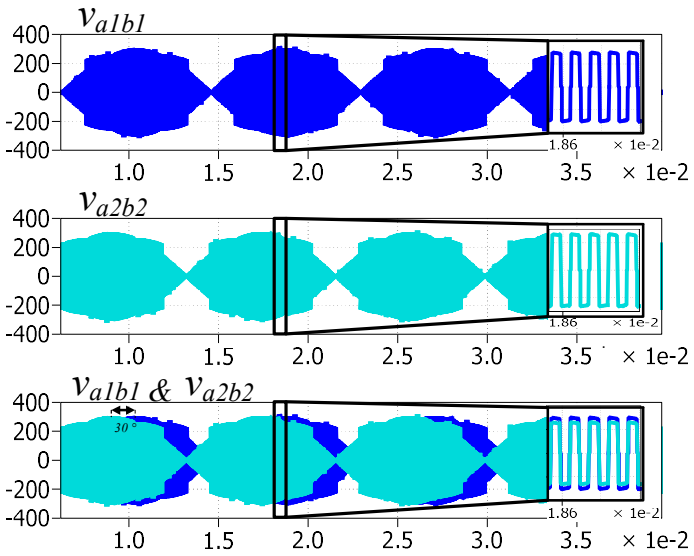

Figure 4-6 Secondary side voltages v_{a1b1} and v_{a2b2} . A 30°phase shift is introduced between voltage to achieve the 12 pulse operation. For the proposed approach both signals have a high frequency component as discussed in previous sections

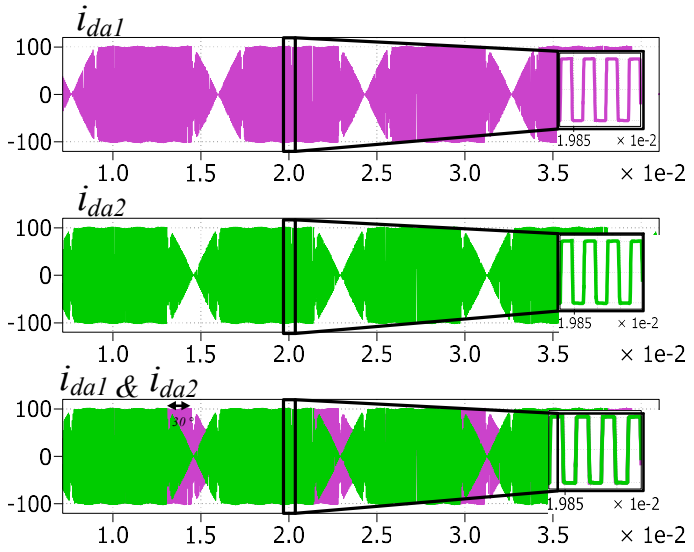

Figure 4-7 Secondary side currents i_{da1} and i_{da} . It can be noticed that the conventional quasi-square-wave of the diodes is multiplied by a high frequency component as discussed in previous sections. It can be notice that the currents have a 30° phase shift between each other.

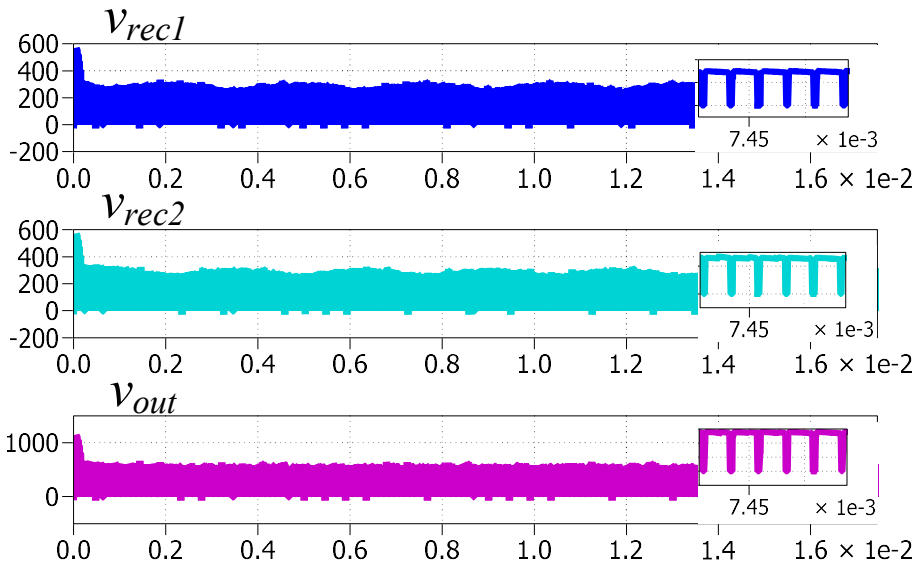

Figure 4-8 DC side output voltages v_{re} , v_{re} and v_{out} . As previously discussed the output voltage of each 6-pulse rectifier has a high frequency behavior

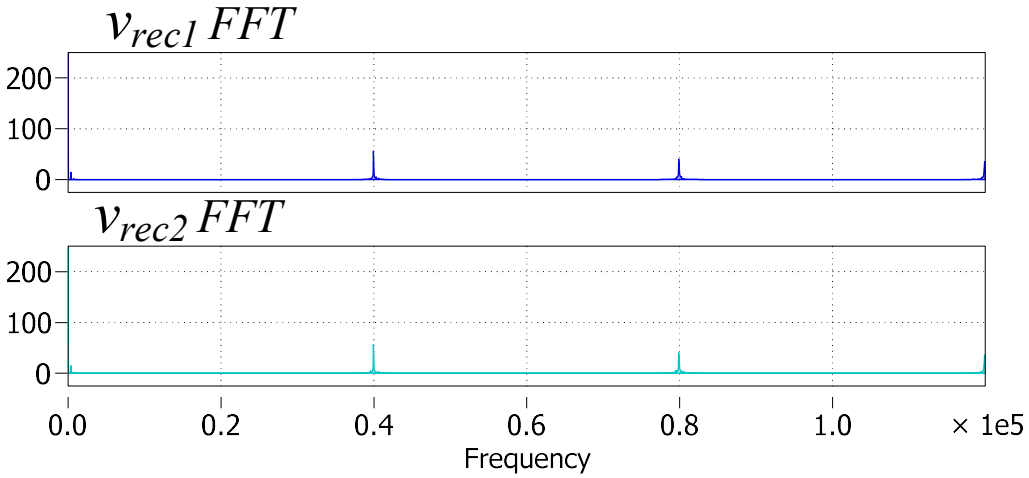

Figure 4-9 FFT of output voltages v_{re} and v_{re} . Notice that the harmonics are located at two times the switching frequency of S_{sw}.

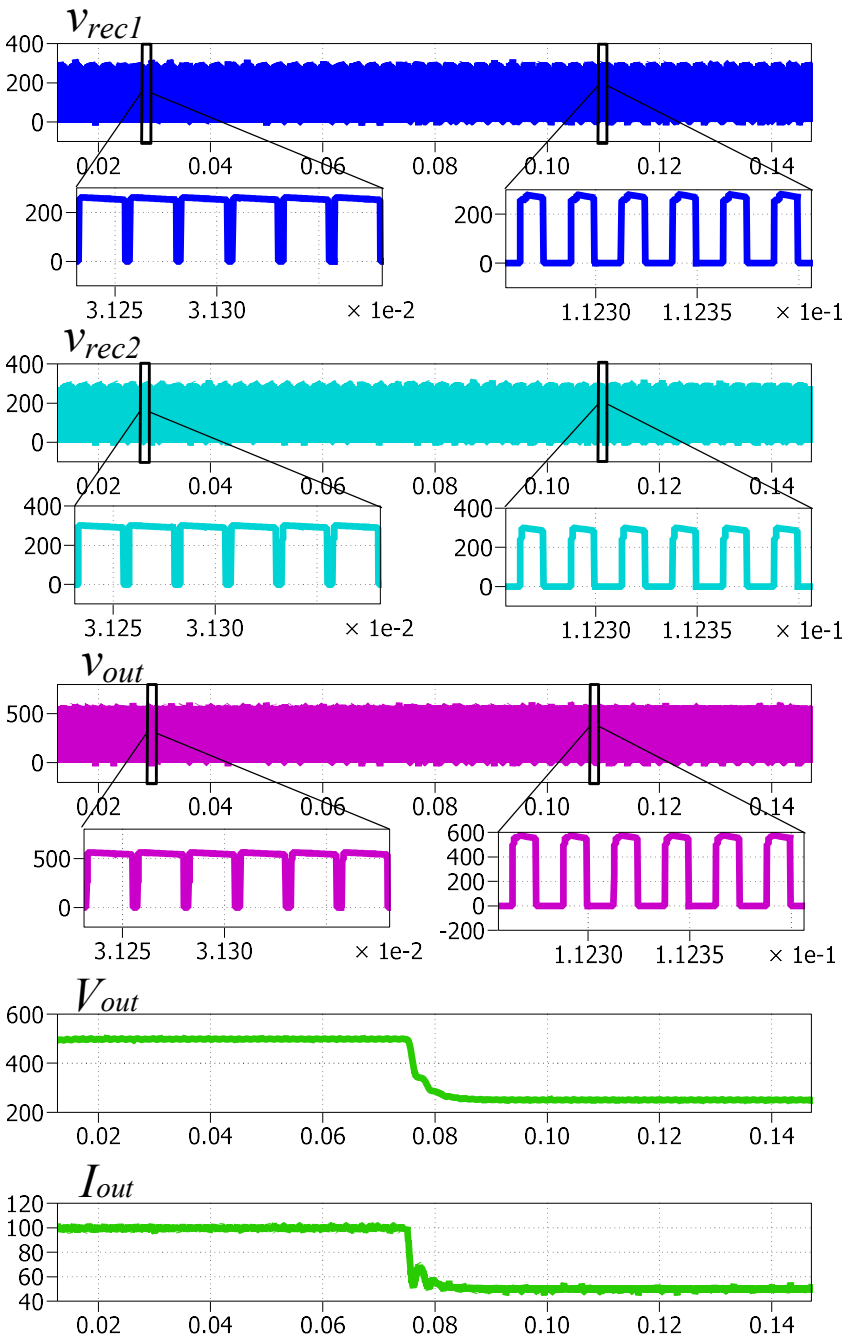

Figure 4-10 Output voltages change of load response. Notice that V_{out} changes according to the average value of voltage v_{out}. The pulse-width of v_{out} changes as a function of duty cycle D

4.2. Thermal simulation and efficiency analysis

In order to quantify the performance of the proposed converter, a thermal simulation was made using PLECS thermal library.

The thermal library allows to compute switching and conduction losses of the devices by using look-up tables with information extracted from the device datasheet.

Table 4-2 Experimental prototype devices

Components	Value/Details
IGBTs	600 V Power MOS7 APT50GP60B2DQ2
Input Diode Rectifier	1600 V / 35 A Diode Bridge FUO22-16N
3ϕ Diode Rectifier	600 V/ 86 A FRED VUE75-06N07

Table 4-3: Zigzag transformer specifications

Winding	P1	S1	S2	S3	S4	P2
Turns	12	11	4	4	11	12
Type	strand	strand	foil	foil	strand	strand
AWG	22	22	3.25x0.005	3.25x0.005	22	22
Strands	9	10	1	1	10	9
Core Material			3C94 FERROXCUBE			
Core Cross Sectional Area			$4.05\text{x}10^{-4}\ m^2$			
Volume of the core			$1.4013\text{x}10^{-4}\ m^3$			
Rated Power			10 kW			
Rated Frequency			20 kHz			

A thermal simulation for a 10 kW system with a temperature of $80°\ C$ was run using the datasheet information of the components listed in Table 4-2. Appendix A includes details of the look-up tables used in PLECS for each one of the listed components. The losses on the transformer were measured experimentally for the maximum rated value of 10 kW at 20 kHz; thus the information given at Figure 4-11 and the efficiency curve in Figure 4-12 include both winding and core losses of the transformer. As previously mentioned in section 2.C the zig-zag transformer was built using three independent cores with one primary and two secondary windings. Table III lists the specifications for an individual

core where the columns named P_n $(n \in \{1,2\})$ indicate the specifications for the primary winding. On the other hand, S_n $(n \in \{1,2,3,4\})$

indicates the specifications for each secondary winding. P_1 and P_2 were connected in series to create a single primary winding.

To calculate the core losses of the transformer the Steinmetz's equation was used [29]

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c l_m \tag{4.8}$$

Where $A_c * l_m$ are equivalent to the volume of the core, K_{fe}, ΔB and β are constants that can be obtained from manufacturer information and depend on the frequency of operation [29].

The core losses for the three cores of the zigzag transformer were obtained using information from Table 4-3 and the datasheet of the core [30].

From Figure 4-11 it can be noticed that most of the losses in the system are generated by conduction losses, more specifically, from both input and output rectifier diodes.

From the information obtained, some considerations can be taken into account to improve the efficiency. First, active switches can replace the input diodes of the AC-AC converters in order to avoid high conduction losses. Furthermore, the system in this case was operating at hard switching; therefore, soft-switching techniques can be implemented at the full bridge rectifier from the AC-AC converters in order to reduce the switching losses. Finally, the transformer's core material can be changed to an amorphous alloy to decrease the losses from the transformer.

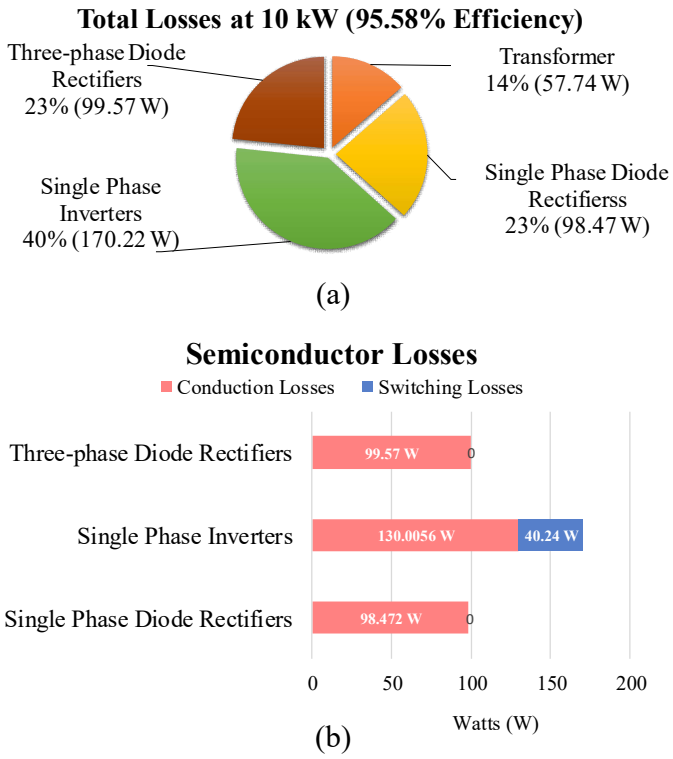

Figure 4-11 Power Losses breakdown for experimental prototype specifications at 10 kW and $V_{LL} = 208$ V. (a) Overall system losses and (b) conduction and switching losses from semiconductor devices at 10 kW operation

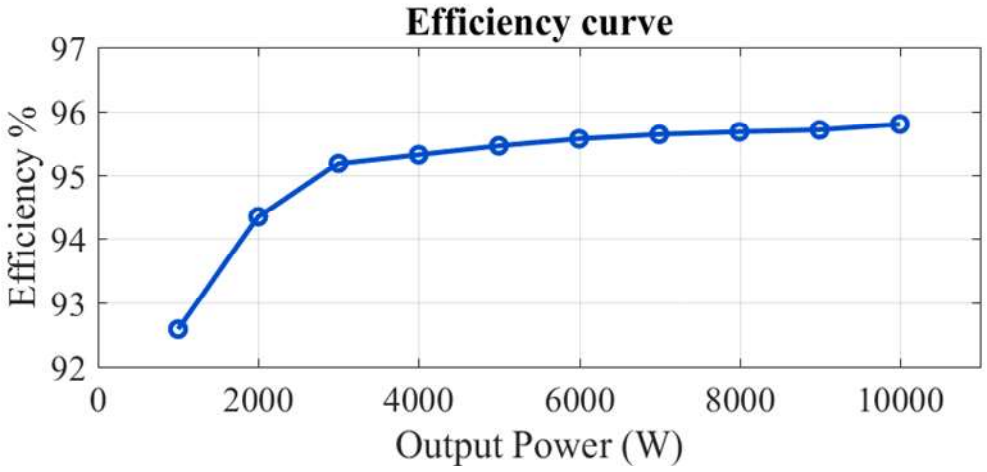

Figure 4-12 Efficiency curve of overall system with experimental prototype specifications for $V_{LL} = 208\,V$

4.3. Section Conclusion

In this section, a design example of the proposed topology at 50 kW with simulation results was presented. The calculations for transformer's turn ratio and output filter design were presented. The simulation results obtained matched with the mathematical analysis of voltage and currents from section 3. By simulation, it was proved that the primary side currents are basically multiplied by a high frequency square wave. From the simulation results it was also proved the idea of output voltage regulation by duty cycle control. Moreover, it was proved that the 12-pulse behavior of the system is maintained regardless of the high frequency operation of the system with elimination of 5^{th} and 7^{th} harmonics. Finally, the results of an efficiency analysis of the overall system was presented. The efficiency of the proposed system reached a peak of 95% and consideration for performance improvements were discussed.

5. EXPERIMENTAL PROTOTYPE*

5.1. DSP Implementation

An experimental prototype was built to validate the topology proposed in Section 3 and simulated in Section 4. In section 3.1 the modulation scheme for the AC-AC converter was discussed with details. The modulation scheme for the experimental prototype was designed by code in a Digital Signal Processor (DSP) TMS320F28377D and using the modulation scheme discussed in Section 3.1 (refer to Figure 3-5) for the general case when $D \leq 0.5$. Table 5-1 lists the DSP modules used and the signal output of the corresponding module.

Table 5-1: DSP Modules and signals

DSP Connection	Module	Signal
GPIO0	ePWM1	SYNC Rx
GPIO2	ePWM2	Module A S_1
GPIO4	ePWM3	Module A S_2
GPIO6	ePWM4	Module A S_1
GPIO8	ePWM5	Module A S_2
GPIO10	ePWM6	Module A S_1
GPIO12	ePWM7	Module A S_2
ADC0	ADC0	$sign(v_{ab})$
ADC1	ADC1	$sign(v_{bc})$
ADC2	ADC2	$sign(v_{ca})$
GPIO24	eCAP1	DAC1
GPIO25	eCAP2	DAC2
GPIO26	eCAP3	DAC3
GPIO20	TZ1	OC A
GPIO21	TZ2	OC B
GPIO22	TZ3	OC C
GPIO40	EXTSYNCIN1	SYNC Rx

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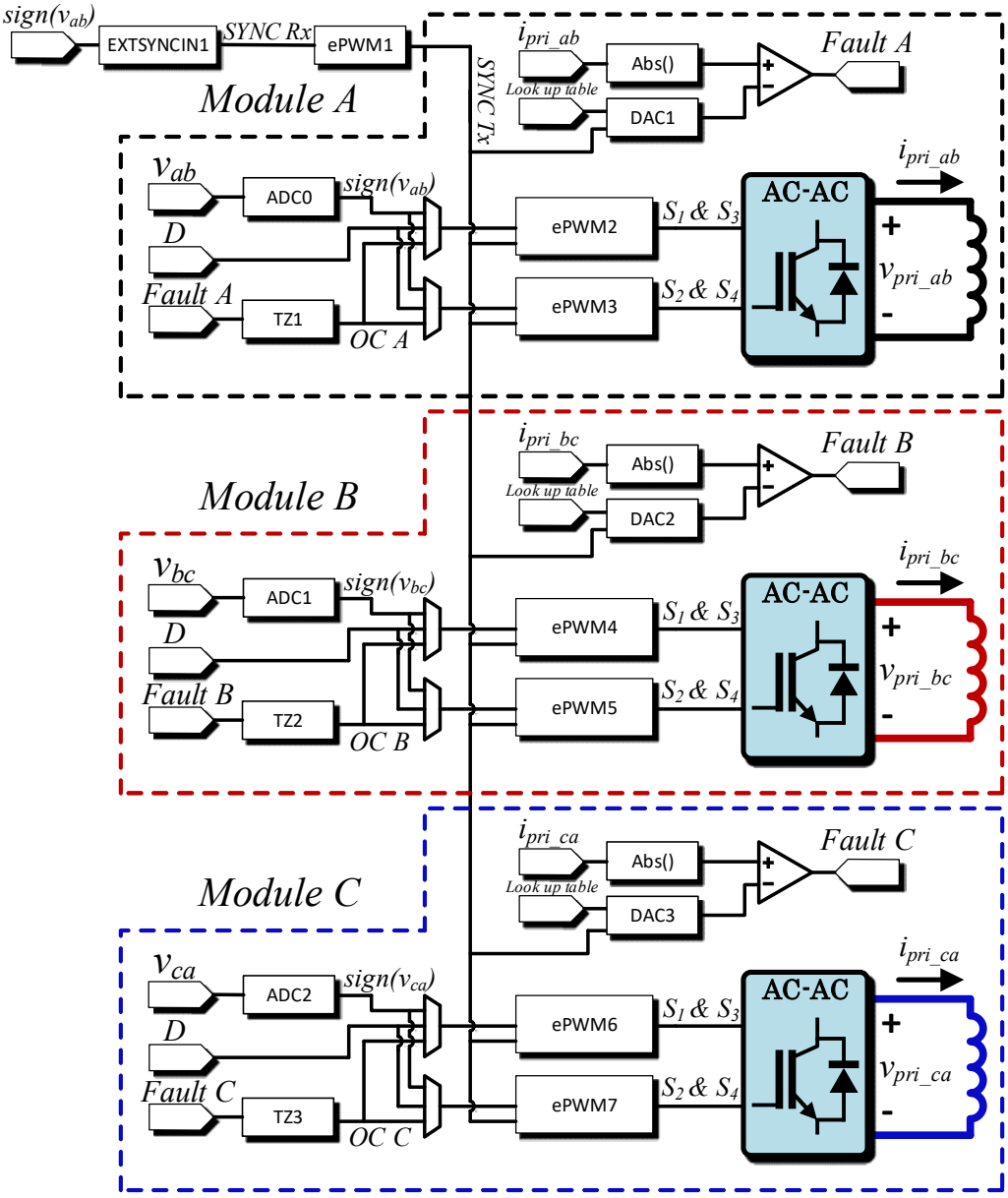

Figure 5-1 DSP code block diagram

Figure 5-1 depicts a block diagram of the DSP program. As mentioned in Section 3, in order to generate the switching function for the AC-AC converter the three line-to-line

input voltages have to be sensed. The output of the voltage sensor is feed to the corresponding ADC modules of the DSP. ADC0, ADC1 and ADC2 are used to generate the signals $sign(v_{ab})$, $sign(v_{bc})$ and $sign(v_{ca})$ respectively which are equivalent to the signal N_1 and $\overline{N_1}$ from Figure 3-5. The experimental prototype was built to operate in open loop; thus, the value of D was specified as a constant. Additionally an over current protection signal is generated by the Tripe Zone modules TZ1, TZ2 and TZ3. The Trip Zone modules allows each one of the ePWM modules to turn off in case the Fault A signal is set as logic zero (under normal operational conditions Fault A is logic one). Figure 5-2 shows an example of the operational principle of the overcurrent protection. In Figure 5-2(a) it can be noticed that DAC1 generates a rectified sine-wave. Also it can be noticed that $Abs(i_{pri_{ab}})$ has as threshold boundary given by DAC1. Figure 5-2(b) shows a zoomed-in version of the signals, it can be noticed that whenever $Abs(i_{pr\ _{ab}}) >$ DAC1the value of the signal $Fault\ A$ becomes zero logic. This event triggers an interruption inside the DSP code which turns-off the corresponding ePWM modules and therefore the current of the circuit becomes zero until the next cycle. In practice this scheme allows to protect the circuit against over current faults making the system more robust. It has to be mentioned that the envelope generated by DAC1 can have different shapes according to the values specified in its look-up table (refer to Figure 5-1).

From Figure 5-1, it can be seen that $sign(v_{ab})$ is feed as input to the module EXTSYNCIN1. This module allows to restart the counter register of ePWM1 which has the task of synchronize all the other ePWM and DAC modules. Since ePWM1 is

synchronized with the line-to-line voltage the rest of the ePWM and DAC modules are synchronized as well.

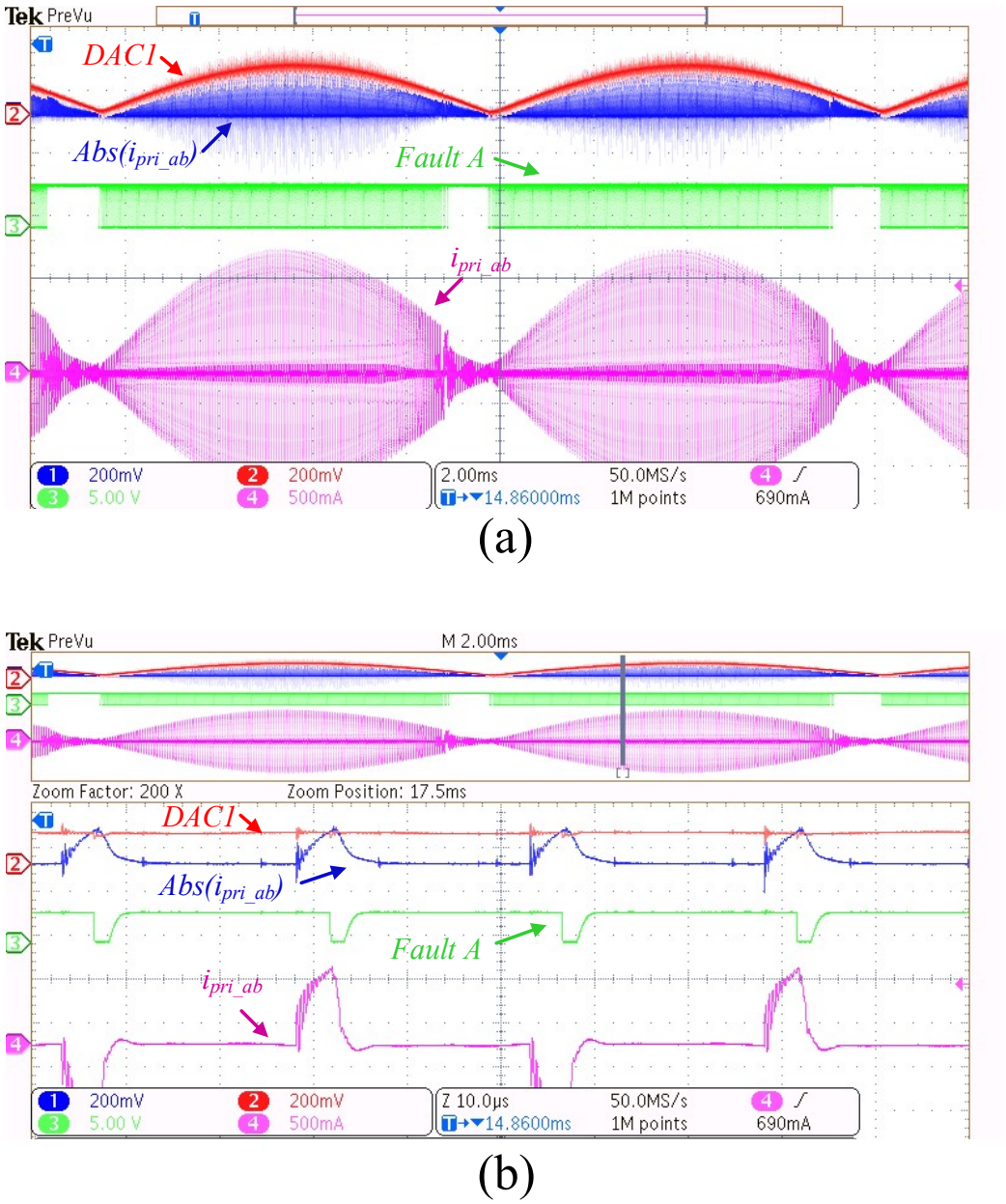

Figure 5-2: Overcurrent protection example (a) operational principle of current protection (b) operational principle of over current protection zoomed in

5.2. Experimental Results

A scaled down laboratory prototype rated at 208V (60Hz), 3-phase, 2kW was built and tested to validate the operation of the proposed system as depicted in Figure 5-3. A small input passive filter with $L_f = 19\ \mu H$ was used. The prototype was designed to generate a DC output of 500 V. An output LC filter with $C_{out} = 200\mu F$ and $L_{out} = 1\ mH$ was used to filter out high frequency components at the output. Three voltage sensors were used to detect the zero crossing of the line-to-line voltages. These signals were fed to the ADC modules of the microcontroller to synchronize the gating functions of the full-bridge inverters. Gating signals were generated using a TMS32928339D microcontroller. The switching frequency of the gating signals was set to 19.98 kHz (multiple of 60 Hz).

5.2.1. Primary side waveforms

shows some of the relevant waveforms for different duty cycle values. depicts the case for $D = 0.5$. In Figure 5-4(a) the primary side voltage v_{pri_ab} and primary current i_{pri_ab} are shown. It can be seen that both have a high frequency behavior. On the other hand, Figure 5-4(b) shows the input current i_a which has a 12-pulse behavior with 5th and 7th harmonic elimination as previously discussed in section 3.1 . Finally the filtered DC side signals are shown in Figure 5-4(c). For this case a DC voltage $V_{out} = 511.7\ V$ was obtained for a load power $P_{out} = 1.74$ kW.

To probe the voltage regulation characteristic of the proposed circuit, experimental results for two additional values of D were obtained. Figure 5-6 shows the

results obtained for $D = 0.35$. Figure 5-6(a) depicts the primary voltage v_{pri_ab} and current i_{pri_ab} form where it can be seen that the voltage and currents look similar to the case for $D = 0.5$.

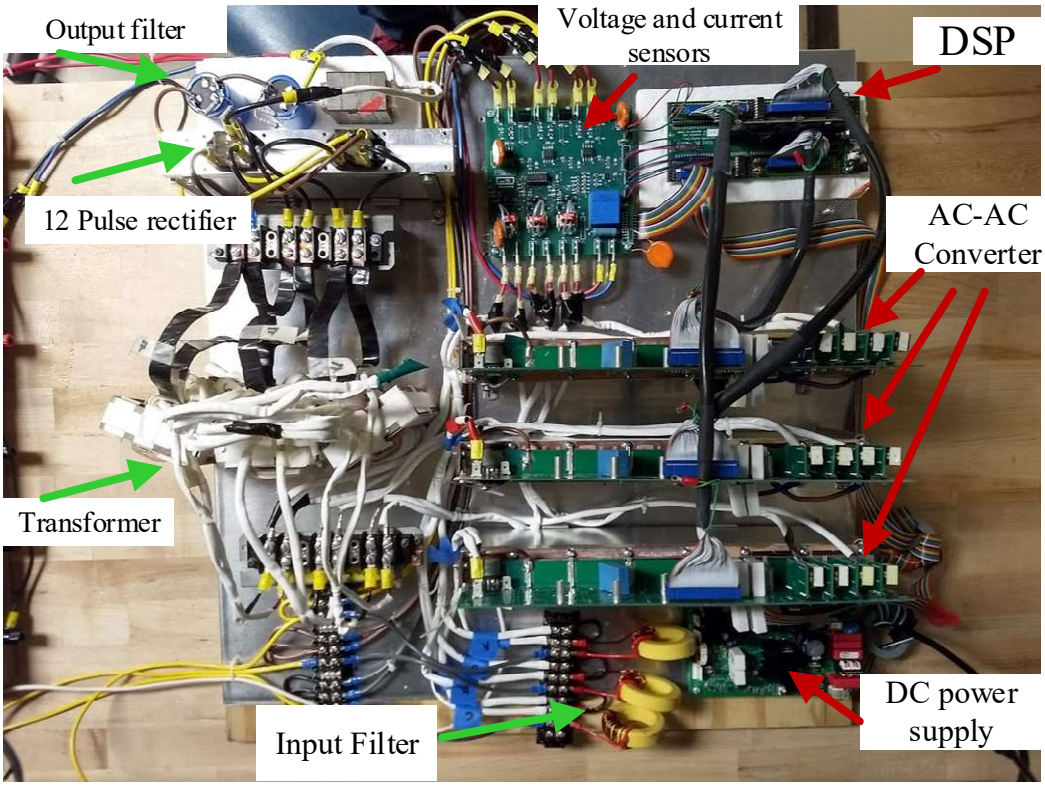

Figure 5-3 2 kW scaled down experimental prototype of the proposed three-phase AC-DC converter. Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

The reason why there is no significant changes in the primary voltage for this case is due to the effect of the parasitic inductance of the transformer windings which is depicted with more details in Figure 5-5. In fact the current i_{pri_ab} can be considered as the

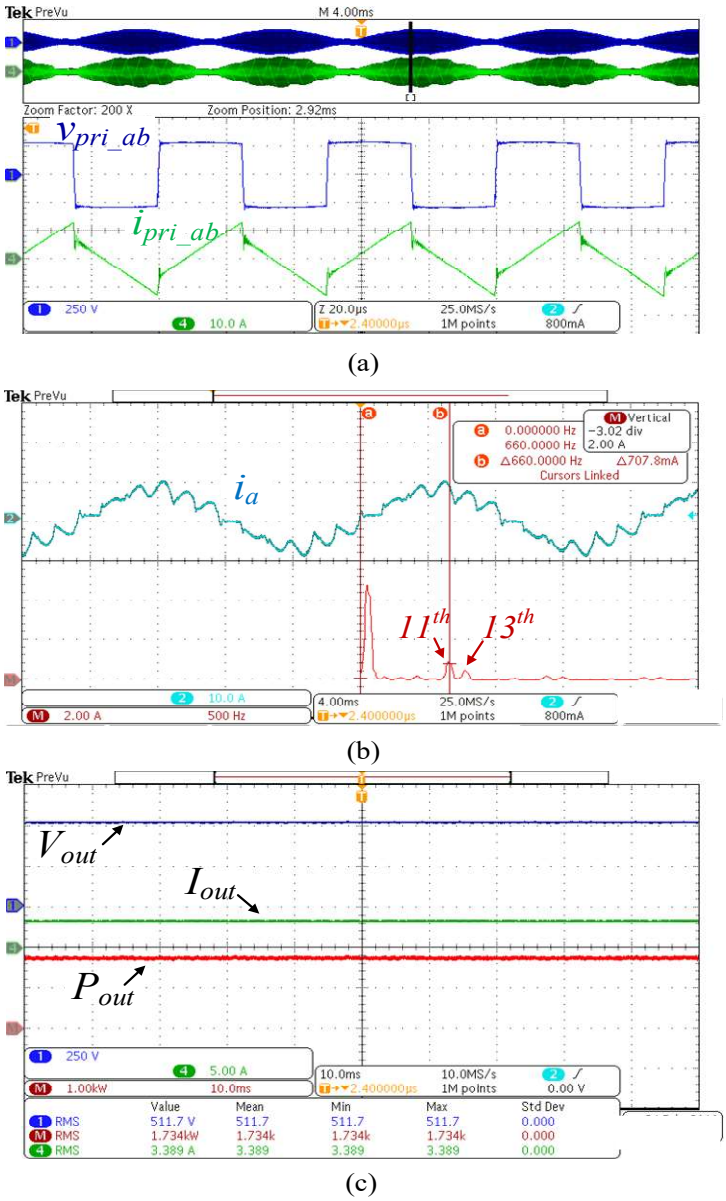

Figure 5-4 (a) Primary side signals v_{pri_ab} (y-axis-250 V/div and x-axis-20 μs/div), $i_{pr\ \_ab}$ (y-axis-10 A/div and x-axis-20 μs/div) and (b) utility input current i_a (y-axis-10 A/div and x-axis-4 ms/div) for D=0.5 with a THD=15% (c) Filtered DC voltage output V_{out}(y-axis-250 V/div and x-axis-10 ms/div), output current I_{out} (y-axis-5 A/div and x-axis-10 ms/div), and output power P_{out}(y-axis-1 kW/div and x-axis-10 ms/div). Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

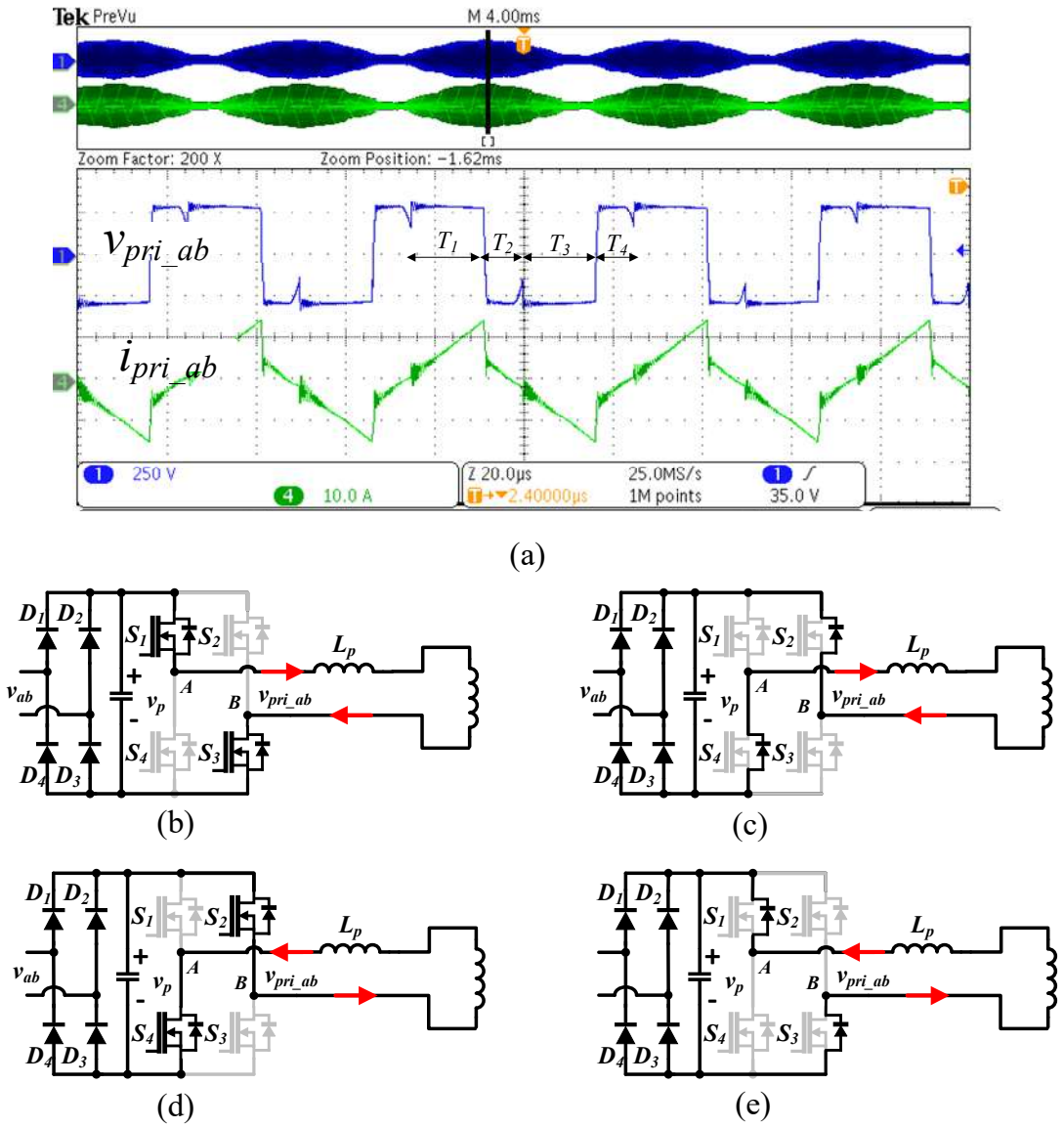

Figure 5-5 (a) Primary side experimental behavior due to parasitic inductance L_p. The parasitic inductance generate additional switching states on the AC-AC converter (b) Interval $T_1$when switches S_1 and S_3 are turned on (c) parasitic inductance energy release trough free-wheeling diodes during interval T_2 (d) Interval T_3 when switches S_2 and S_4 are turned on (e) parasitic inductance energy release trough free-wheeling diodes during interval T_4

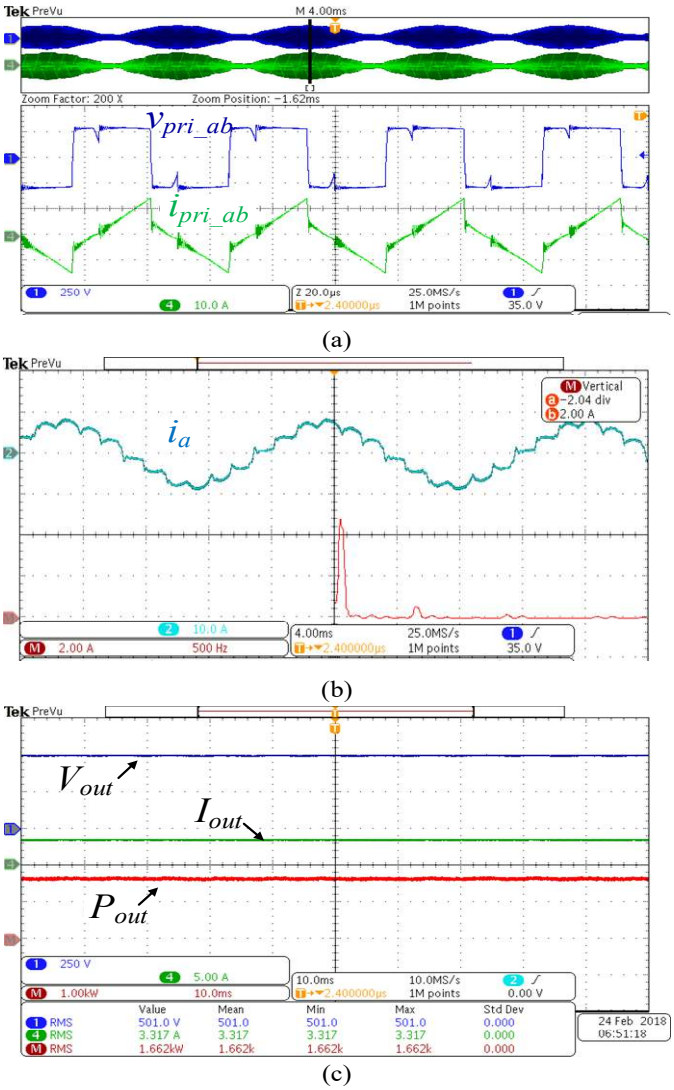

Figure 5-6 (a) Primary side signals v_{pri_ab} (y-axis-250 V/div and x-axis-20 μs/div), i_{pri_ab} (y-axis-10 A/div and x-axis-20 μs/div) and (b) utility input current i_a (y-axis-10 A/div and x-axis-4 ms/div) for D=0.35 with a THD=11.5% c) Filtered DC voltage output V_{out}(y-axis-250 V/div and x-axis-10 ms/div), output current I_{out} (y-axis-5 A/div and x-axis-10 ms/div), and output power P_{out}(y-axis-1 kW/div and x-axis-10 ms/div). Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

current of the primary parasitic inductance. Referring to Figure 5-5 during the interval T_1 $+v_p$ is connected to terminal A and $-v_p$ is connected to B , during this time the current of the parasitic inductance L_p is boosted. Once S_1 and S_3 are turned off, the current of the inductor starts to decrease but flowing at the same direction as in interval T_1. Therefore, the free-wheeling diodes of switches S_2 and S_4 generate a path for the current. This switching state is depicted in Figure 5-5(c). Notice that during the switching state depicted in Figure 5-5(c) terminal A is connected to $-v_p$ and terminal B to $+v_p$. Since v_p is a rectified sine wave as shown in Figure 3-2(c), the voltage seen at v_{pri_ab} during interval T_2 will be negative. During interval T_3
switches S_2 and S_4 are turned on and generate a negative current in the primary winding as depicted in Figure 5-5(d). Once S_2 and S_4 are turned off the free-wheeling diodes from S_1 and S_3 conduct until all the energy from L_p is drain completing the fourth interval T_4. Notice that during T_4 terminals A is connected to $+v_p$ and terminal B to $-v_p$. Therefore, despite the current being negative during this interval the voltage seen by v_{pri_ab} is positive. Figure 5-6 (b) shows the utility input current for $D = 0.35$ which conserve the elimination of 5ht and 7th harmonics with the staircase 12-pulse shape. The DC output signals are shown in Figure 5-6(c) for this case a voltage output $V_{out} = 501\ V$ with an output power of $P_{out} = 1.66\ kW$. It has to be mentioned that the reason why there was no a big change on the DC output V_{out} compared to the case when $D =$

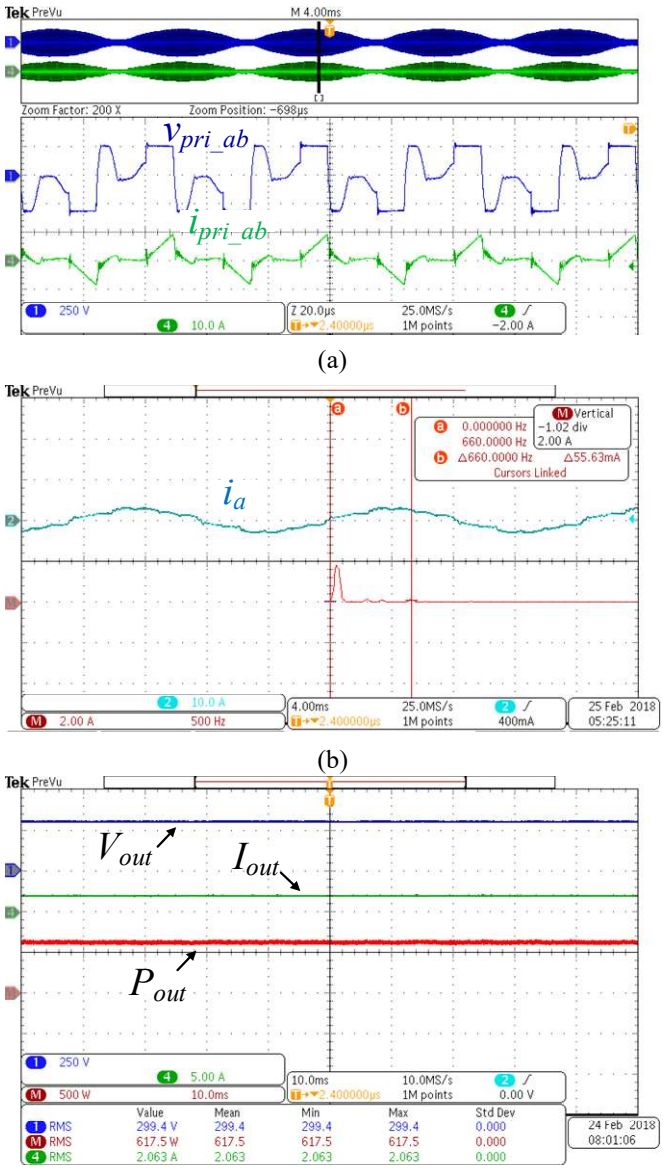

Figure 5-7 (a) Primary side signals v_{pri_ab} (y-axis-250 V/div and x-axis-20 μs/div), i_{pri_ab} (y-axis-10 A/div and x-axis-20 μs/div) and (b) utility input current i_a (y-axis-10 A/div and x-axis-4 ms/div) for D=0.2 with a THD=13.5% c) Filtered DC voltage output V_{out}(y-axis-250 V/div and x-axis-10 ms/div), output current I_{out} (y-axis-5 A/div and x-axis-10 ms/div), and output power P_{out}(y-axis-1 kW/div and x-axis-10 ms/div). Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

0.5 is because of the effect of the parasitic inductance. From Figure 5-5 it is clear that the zero states on voltage v_{pri_ab} are not generated due to the intervals T_2 and T_4 when the free-wheeling diodes conduct. This practical issue can be attenuated by making L_p as small as possible.

Finally, Figure 5-7 depicts the results for a case with $D = 0.2$. From Figure 5-7(a) it can be seen that the current and voltage are affected by the parasitic inductance as in the case where $D = 0.35$. However in Figure 5-7(a) it can be noticed that zero states in the voltage v_{pri_ab} are achieved and therefore the voltage at the DC side V_{out} has a more considerable change. For $D = 0.2$ a value of $V_{out} = 299\ V$ at $P_{out} = 617\ W$ (refer to Figure 5-7(c)). The 12 pulse behavior is also kept as seen in Figure 5-7(b) and elimination of 5th and 7th harmonics is achieved.

5.2.2. Secondary side waveforms

Results for the secondary side waveforms were obtained for a case when $D = 0.5$ Figure 5-8 shows the secondary voltages, v_{a1b1} and v_{a2b2}. It can be seen that v_{a1b1} and v_{a2b2} have a 30 degree phase shift with respect to each other to generate the 12-pulse behavior at the output. On the other hand, Figure 5-9 depicts the secondary currents of the circuit. It can be noticed that the signals have an envelope given by the quasi square wave function from equation (2.13) and depicted in Figure 2-13(d) from a line commutated three-phase diode rectifier; however, in this case a high frequency signal modulates the line frequency signal as discussed in section 3.5. Finally, Figure 5-10 shows the voltages v_{rec1}, v_{rec2}, and v_{out}. The average value of v_{rec1} was 245 V while the avergage value of

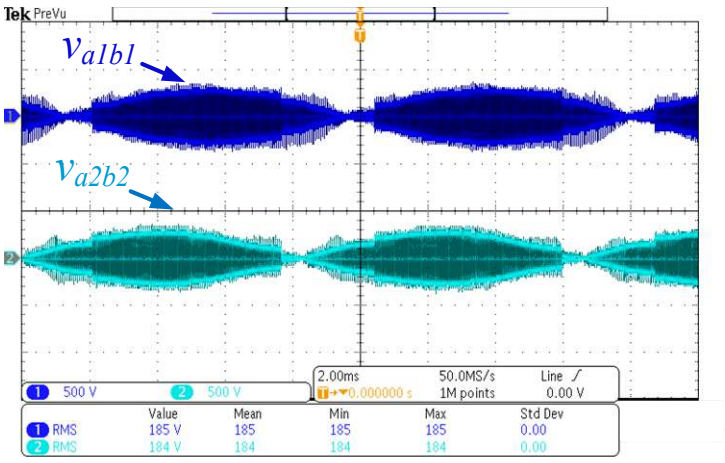

Figure 5-8 Secondary voltage v_{a1b1} (y-axis-500 V/div and x-axis-2 ms/div) with -15 ° phase shift and v_{a2b2} (y-axis-500 V/div and x-axis-2 ms/div) with $+15°$ phase shift. Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

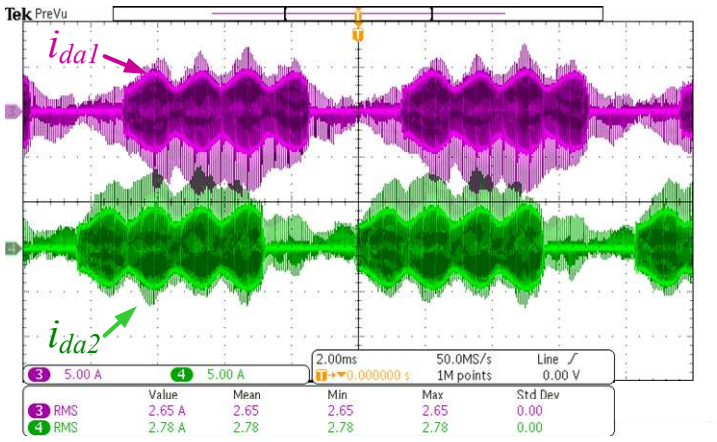

Figure 5-9 Secondary currents i_{da1} (y-axis-5 A/div and x-axis-2 ms/div) with -15° phase shift and i_{da} (y-axis-5 A/div and x-axis-2 ms/div) with +15° phase shift. Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

v_{rec1} was 265 V. v_{rec1} and v_{rec2} are connected in series the total average value of v_{out} was 520 V. As previously discussed 3.3, the voltage outputs of the 6-pulse diode rectifiers have a high-frequency behavior as proved in section 3.3 in equations (3.14) and (3.15).

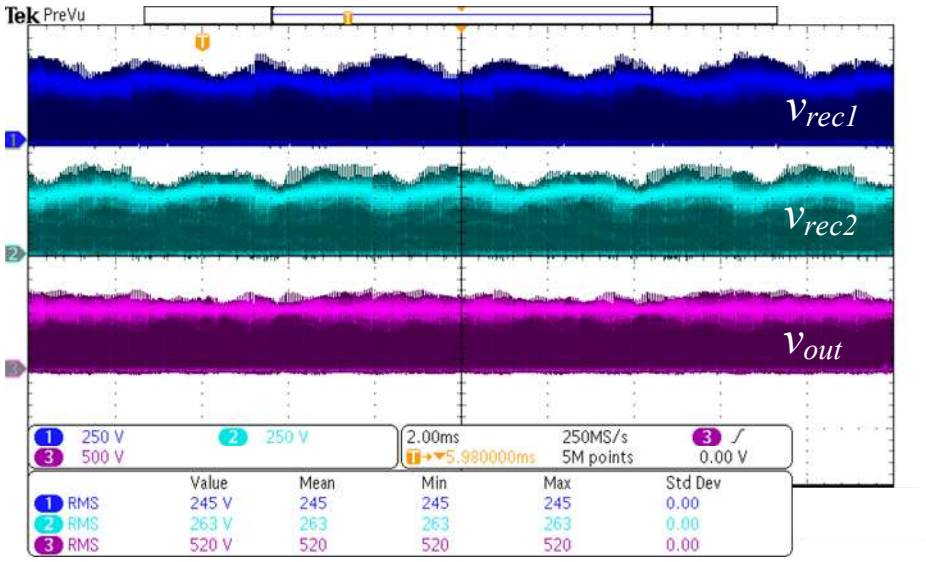

Figure 5-10 12-pulse high-frequency voltage output v_{out} (y-axis-500 V/div and x-axis-2 ms/div) and three-phase rectifier outputs v_{rec1} (y-axis-250 V/div and x-axis-2 ms/div) and v_{rec2} (y-axis-250 V/div and x-axis-2 ms/div). Reprinted with permission from ©2019 IEEE. E. Pool-Mazun, J. J. Sandoval, P. Enjeti and I. J. Pitel, "A Direct Switch-Mode Three-Phase AC to DC Rectifier with High-Frequency Isolation for Fast EV Battery Chargers," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 573-580.

5.3. Section Conclusion

In this section, a description of the experimental prototype implementation and results was given. Specifications about the DSP implementation was given along with the discussion of an over current protection scheme. On the other hand, experimental results of the output voltage regulation by duty cycle control were discussed for different

values of D. It was proved that changes in duty cycle D allow to control the DC output of the rectifier. Moreover, the effect of the parasitic inductance on the primary side and effects on the system were discussed. It could be observed that high values of parasitic inductance L_p affect the value of the DC output. Finally, experimental results of the secondary side voltage and currents were presented. It was proved that the signals correspond to their simulation counterparts.

6. CONCLUSION AND FUTURE WORK

6.1. Conclusion

In this work, a single-stage three-phase rectifier topology with high frequency isolation was proposed. By using a multi-pulse rectifier approach, low order harmonics were eliminated. The proposed high frequency modulation of the three-phase voltage input allowed an improvement of power density by replacement of the bulky line frequency transformer by a ferrite core, high-frequency transformer. This high-frequency galvanic isolation approach also allowed the elimination of the bulky DC-Link capacitor. Moreover, the proposed modulation scheme simplified the control design for output voltage regulation and achieved good THD performance in the utility input current without an active PFC scheme. The output voltage regulation capability of the topology enables its use as a direct architecture for Level-3 EV charging stations. Moreover, the proposed system can also be considered as an alternative for DC-bus Level-3 EV charging architectures to improve the power density of the system by replacing the line-frequency transformer of the conventional 12-pulse rectifier.

6.2. Future work

Future work will be done to explore the following:

- Improvement of THD performance
    - By controlling AC-AC converters
    - By using Active Power Filters (APF)
- Transformer and magnetics design for higher frequency cases and performance.
- Zero Voltage Switching (ZVS) of front end AC-AC converters.
- Math-model of overall system.

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APPENDIX A

PLECS THERMAL SIMULATION TABLES

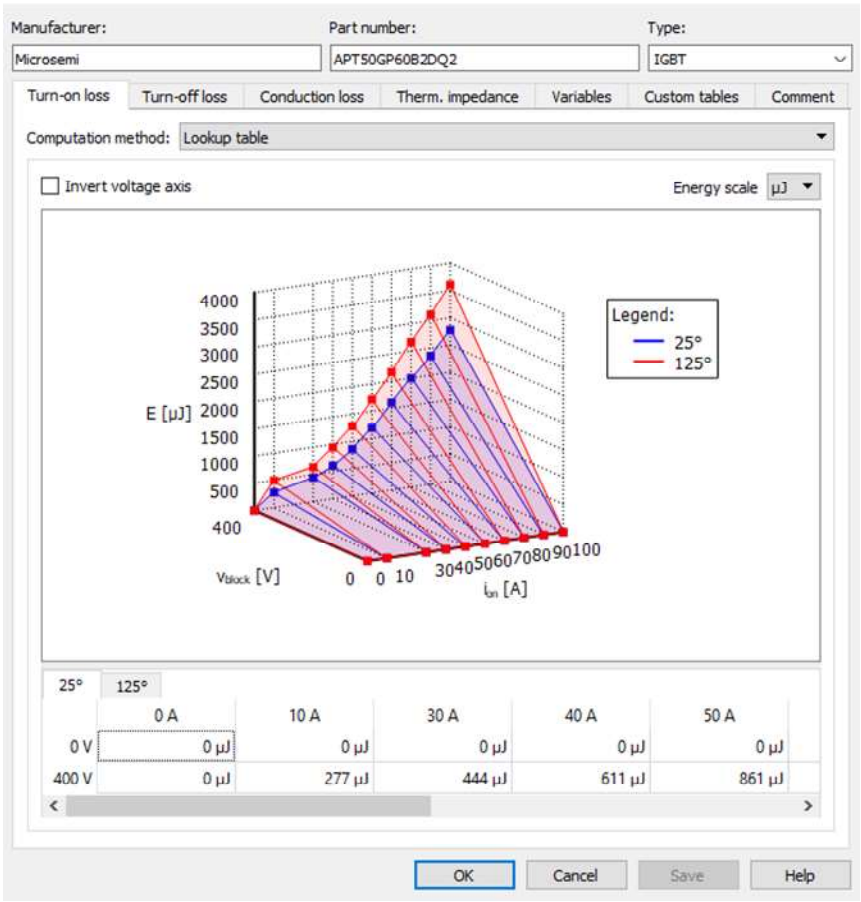

Figure A-1 APT50GP60B2DQ2 IGBT Turn-on losses curve

Table A-1: APT50GP60B2DQ2 IGBT Turn-on losses table at 25°

	0 A	10 A	30 A	40 A	50 A	60 A	70 A	80 A	90 A	100 A
0 V	0 *µJ*	0 *µJ*	0 *µJ*	0 *µJ*	0 *µJ*	0 *µJ*	0 *µJ*	0 *µJ*	0 *µJ*	0 *µJ*
400 V	0 *µJ*	277 *µJ*	444 *µJ*	611 *µJ*	861 *µJ*	1194 *µJ*	1611 *µJ*	2000 *µJ*	2361 *µJ*	2777 *µJ*

Table A-2 APT50GP60B2DQ2 IGBT Turn-on losses table at 125°

	0 A	10 A	30 A	40 A	50 A	60 A	70 A	80 A	90 A	100 A
0 V	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ
400 V	0 μJ	500 μJ	638 μJ	944 μJ	1277 μJ	1722 μJ	2166 μJ	2666 μJ	3111 μJ	3611 μJ

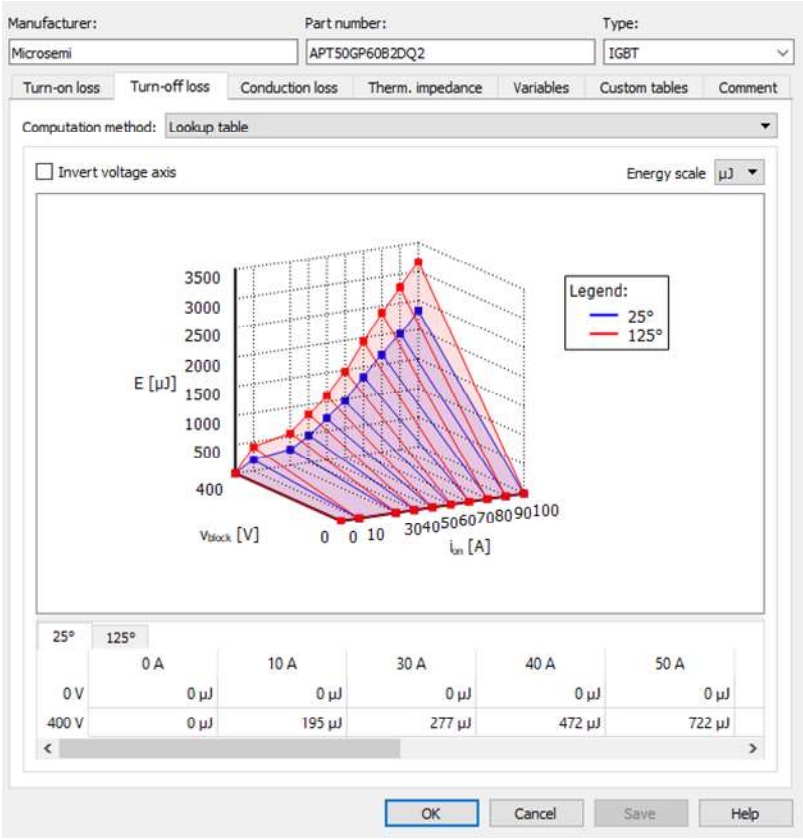

Figure A-2 APT50GP60B2DQ2 IGBT Turn-off losses curve

Table A-3: APT50GP60B2DQ2 IGBT Turn-off losses table at 25°

	0 A	10 A	30 A	40 A	50 A	60 A	70 A	80 A	90 A	100 A
0 V	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ
400 V	0 μJ	195 μJ	277 μJ	472 μJ	722 μJ	972 μJ	1333 μJ	1666 μJ	1972 μJ	2333 μJ

Table A-4 :APT50GP60B2DQ2 IGBT Turn-off losses table at 125°

	0 A	10 A	30 A	40 A	50 A	60 A	70 A	80 A	90 A	100 A
0 V	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ	0 μJ
400 V	0 μJ	416 μJ	555 μJ	833 μJ	1111 μJ	1472 μJ	1944 μJ	2388 μJ	2777 μJ	3166 μJ

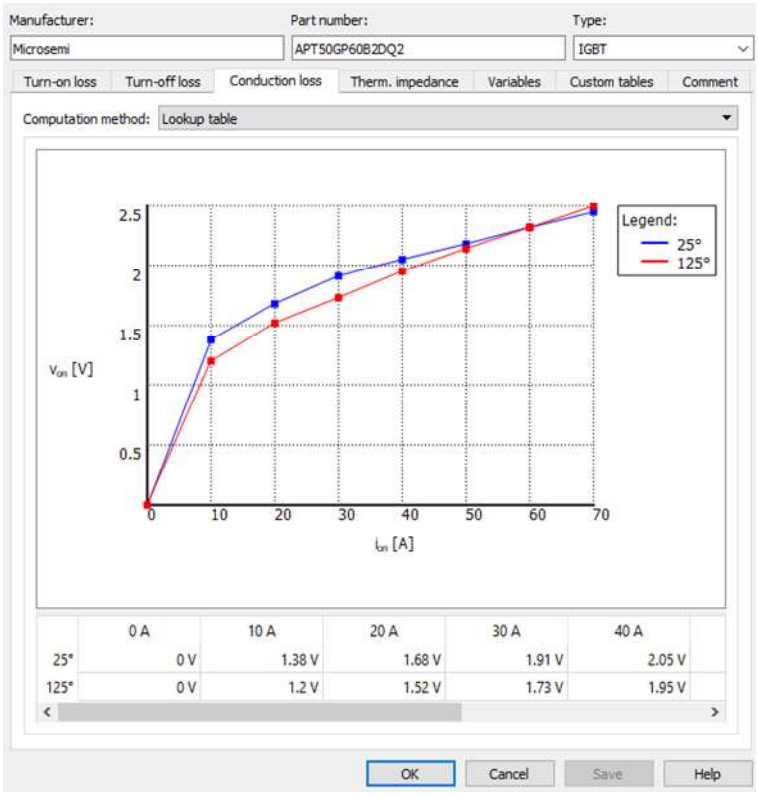

Figure A-3 APT50GP60B2DQ2 IGBT V-I curve

Table A-5: APT50GP60B2DQ2 IGBT conduction losses look-up table

	0 A	10 A	20 A	30 A	40 A	50 A	60 A	70 A
25°	0 V	1.38 V	1.68 V	1.91 V	2.05 V	2.18 V	2.32 V	2.45 V
125°	0 V	1.2 V	1.52 V	1.73 V	1.95 V	2.14 V	2.32 V	2.5 V

Table A-6: APT50GP60B2DQ2 IGBT Thermal junction impedance

	1	2	3	4
R	0.1 K/W	0.02 K/W	0.015 K/W	0.045 K/W
τ	0.0001 s	0.001 s	0.01 s	0.1 s

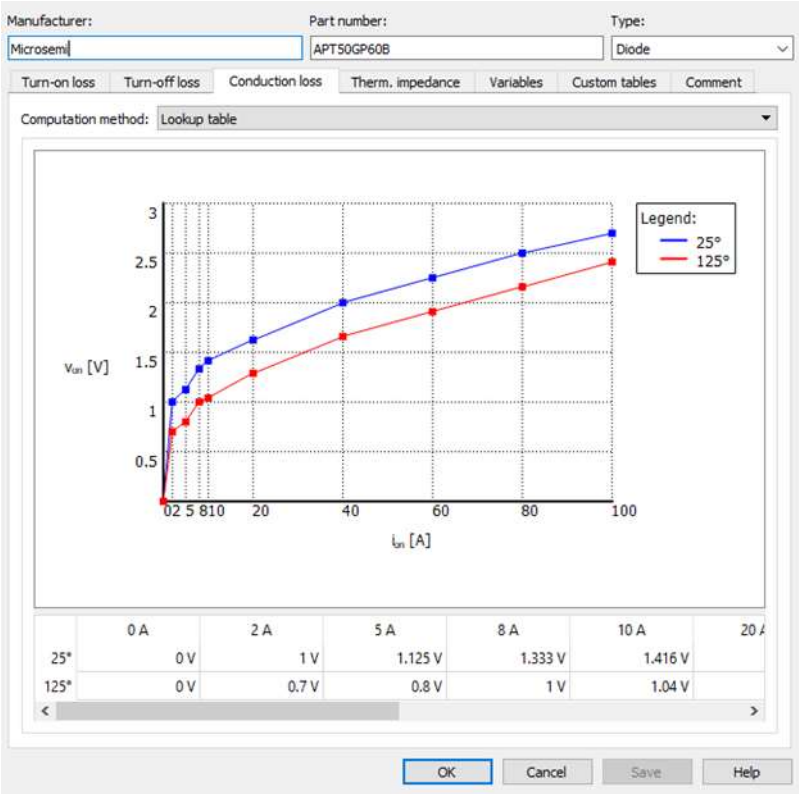

Figure A-4 APT50GP60B2DQ2 diode V-I curve

Table A-7: APT50GP60B2DQ2 diode conduction losses look-up table

	0 A	2 A	5 A	8 A	10 A	20 A	40 A	60 A	80 A	100 A
25°	0 V	1 V	1.12 V	1.33 V	1.41 V	1.62 V	2 V	2.25 V	2.5 V	2.7 V
125°	0 V	0.7 V	0.8 V	1 V	1.04 V	1.29 V	1.66 V	1.91 V	2.16 V	2.41 V

Table A-8: APT50GP60B2DQ2 diode Thermal junction impedance

	1	2	3	4
R	0.35 K/W	0.04 K/W	0.1 K/W	0.13 K/W
τ	0.0001 s	0.001 s	0.01 s	0.1 s

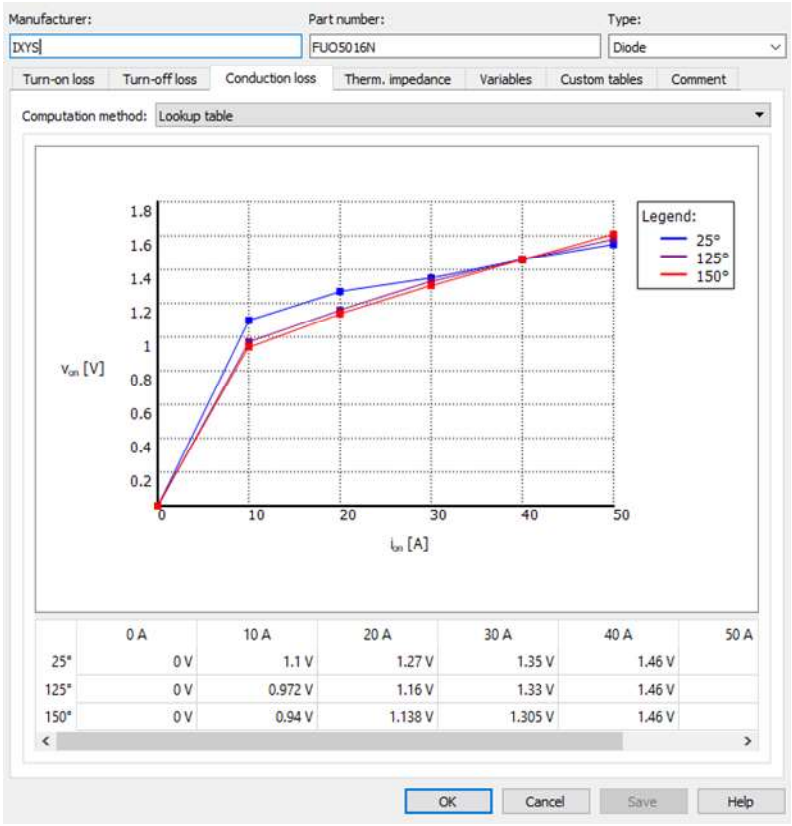

Figure A-5 FUO5016N diode V-I curve

Table A-9: FUO5016N diode conduction losses look-up table

	0 A	10 A	20 A	30 A	40 A	50 A
25°	0 V	1.1 V	1.27 V	1.35 V	1.46 V	1.55 V
125°	0 V	0.972 V	1.16 V	1.33 V	1.46 V	1.58 V
150°	0 V	0.94 V	1.13 V	1.3 V	1.46 V	1.61 V

Table A-10 FUO5016N diode Thermal junction impedance

	1	2	3	4
R	1.159 K/W	0.1286 K/W	0.2651 K/W	0.5473 K/W
τ	0.1015 s	0.2.041 s	0.696 s	1.316 s

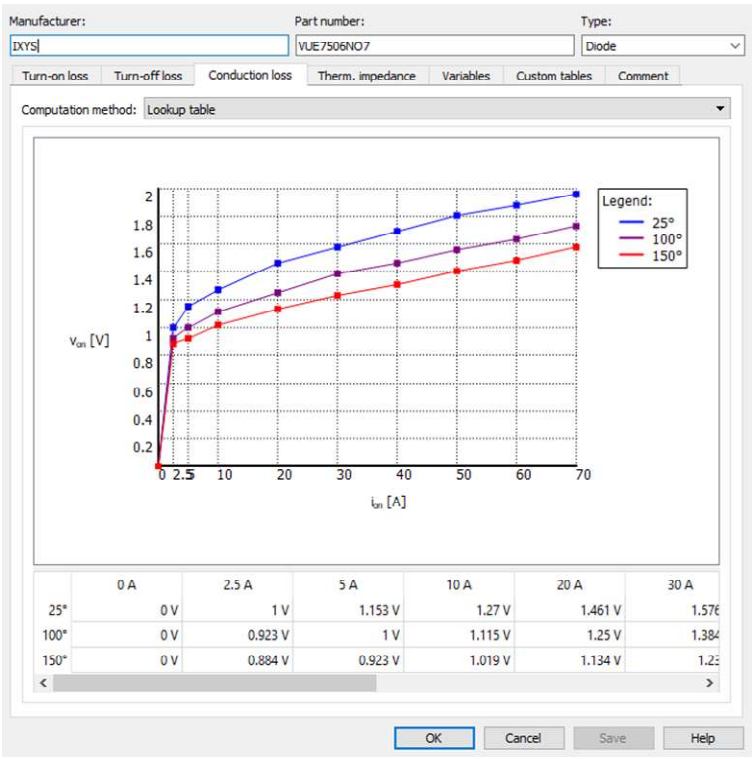

Figure A-6 VUE7506N07 diode V-I curve

Table A-11: VUE7506N07 diode conduction losses look-up table

	0 A	2.5 A	5 A	10 A	20 A	30 A	40 A	50 A	60 A	70 A
25°	0 V	1 V	1.15 V	1.27 V	1.46 V	1.57 V	1.69 V	1.8 V	1.88 V	1.96 V
125°	0 V	0.92 V	1 V	1.11 V	1.25 V	1.38 V	1.46 V	1.55 V	1.63 V	1.73 V
150°	0 V	0.88 V	0.92 V	1.01 V	1.13 V	1.23 V	1.3 V	1.4 V	1.48 V	1.57 V

Table A-12 : VUE7506N07 diode Thermal junction impedance

	1	2	3	4	5
R	0.004 K/W	0.034 K/W	0.142 K/W	0.42 K/W	0.3 K/W
τ	0.0003 s	0.003 s	0.02 s	0.2 s	1 s

APPENDIX B

TI TMS320F28379D CODE

```
#include "F28x_Project.h"     // Device Headerfile and Examples Include File
#include <math.h>
//#include "C28x_FPU_FastRTS.h"

// Constant definitions
#define PI            3.141592654
#define samples        500
#define step           0.0000333333333333
#define flat           0.8

void ConfigureADC(void);
void ConfigureEPWM(void);
void SetupADCEpwm(Uint16 channel);
void GPIOConfig(void);
void ConfigECap(void);

__interrupt void adca1_isr(void);
__interrupt void timer0_isr(void);

__interrupt void epwm1_isr(void);

__interrupt void epwm2_tzint_isr(void);
__interrupt void epwm3_tzint_isr(void);
__interrupt void epwm4_tzint_isr(void);
__interrupt void epwm5_tzint_isr(void);
__interrupt void epwm6_tzint_isr(void);
__interrupt void epwm7_tzint_isr(void);

__interrupt void ecap1_isr(void);
__interrupt void ecap2_isr(void);
__interrupt void ecap3_isr(void);

//buffer for storing conversion results
#define RESULTS_BUFFER_SIZE 256
Uint16 AdcaResults[RESULTS_BUFFER_SIZE];
Uint16 resultsIndex;
Uint16 bufferFull;
```

```
// ADC Result Values
Uint16 Voltage1=0;
Uint16 Voltage2=0;
Uint16 Voltage3=0;

// TZCounters
Uint16 EPwm2TZIntCount =0;
Uint16 EPwm3TZIntCount =0;
Uint16 EPwm4TZIntCount =0;
Uint16 EPwm5TZIntCount =0;
Uint16 EPwm6TZIntCount =0;
Uint16 EPwm7TZIntCount =0;

float sine_table[samples];
Uint16 N=0;

Uint16 index1=0;
Uint16 index2=167;
Uint16 index3=333;
Uint16 count=0;

Uint16 Flag1=0;
Uint16 Flag2=0;
Uint16 Flag3=0;

Uint16 FlagRise1=0;
Uint16 FlagFall1=0;
Uint16 FlagRise2=0;
Uint16 FlagFall2=0;
Uint16 FlagRise3=0;
Uint16 FlagFall3=0;

Uint16 D1=2500;
Uint16 D2=2500;
Uint16 D3=2500;

void main(void)
{
// Step 1. Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the F2837xD_SysCtrl.c file.
   InitSysCtrl();

// Step 2. Initialize GPIO:
```

```
// This example function is found in the F2837xD_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
   InitGpio(); // Skipped for this example

// Step 3. Clear all interrupts and initialize PIE vector table:
// Disable CPU interrupts
   DINT;

// Initialize the PIE control registers to their default state.
// The default state is all PIE interrupts disabled and flags
// are cleared.
// This function is found in the F2837xD_PieCtrl.c file.
   InitPieCtrl();

   CpuSysRegs.PCLKCR2.bit.EPWM1=1;
   CpuSysRegs.PCLKCR2.bit.EPWM2=1;
   CpuSysRegs.PCLKCR2.bit.EPWM3=1;
   CpuSysRegs.PCLKCR2.bit.EPWM4=1;
   CpuSysRegs.PCLKCR2.bit.EPWM5=1;
   CpuSysRegs.PCLKCR2.bit.EPWM6=1;
   CpuSysRegs.PCLKCR2.bit.EPWM7=1;

// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt
// Service Routines (ISR).
// This will populate the entire table, even if the interrupt
// is not used in this example.  This is useful for debug purposes.
// The shell ISR routines are found in F2837xD_DefaultIsr.c.
// This function is found in F2837xD_PieVect.c.
   InitPieVectTable();



//Map ISR functions
   EALLOW;
   PieVectTable.ADCA1_INT = &adca1_isr; //function for ADCA interrupt 1

   PieVectTable.EPWM1_INT= &epwm1_isr;

   PieVectTable.EPWM2_TZ_INT = &epwm2_tzint_isr;
   PieVectTable.EPWM3_TZ_INT = &epwm3_tzint_isr;
```

```
    PieVectTable.EPWM4_TZ_INT = &epwm4_tzint_isr;
    PieVectTable.EPWM5_TZ_INT = &epwm5_tzint_isr;
    PieVectTable.EPWM6_TZ_INT = &epwm6_tzint_isr;
    PieVectTable.EPWM7_TZ_INT = &epwm7_tzint_isr;

    PieVectTable.ECAP1_INT = &ecap1_isr;
    PieVectTable.ECAP2_INT = &ecap2_isr;
    PieVectTable.ECAP3_INT = &ecap3_isr;

    PieVectTable.TIMER0_INT =&timer0_isr;
    EDIS;

//Configure the ADC and power it up
    ConfigureADC();

//Configure eCap Modules
    ConfigECap();

//Setup the ADC for ePWM triggered conversions on channel 0
    SetupADCEpwm(0);

    //sync ePWM
        EALLOW;
        CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 0;
        EDIS;

        ConfigureEPWM();
        GPIOConfig();

        EALLOW;
        CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;
        EDIS;


          IER |= M_INT1; // Enable CPU Interrupt 1

          IER |= M_INT2; // Enable CPU Interrupt 2

          IER |= M_INT3; // Enable CPU Interrupt 3

          IER |= M_INT4;
 //enable PIE interrupt ADCA1

        PieCtrlRegs.PIEIER1.bit.INTx1 = 1;
```

```
// Enable ADCINT in PIE
      PieCtrlRegs.PIEIER1.bit.INTx6 = 1;

// Enable EPWM INTn in the PIE: Group 2 interrupt 1-6 (Group 2 correspond to Trip
Zone interrupts)
      //PieCtrlRegs.PIEIER2.bit.INTx1 = 1;// TZePWM1 interrupt enable
      PieCtrlRegs.PIEIER2.bit.INTx2 = 1;// TZePWM2 interrupt enable
      PieCtrlRegs.PIEIER2.bit.INTx3 = 1;// TZePWM3 interrupt enable
      PieCtrlRegs.PIEIER2.bit.INTx4 = 1;// TZePWM4 interrupt enable
      PieCtrlRegs.PIEIER2.bit.INTx5 = 1;// TZePWM5 interrupt enable
      PieCtrlRegs.PIEIER2.bit.INTx6 = 1;// TZePWM6 interrupt enable
      PieCtrlRegs.PIEIER2.bit.INTx7 = 1;// TZePWM7 interrupt enable

// Enable TIMER0 INT
      PieCtrlRegs.PIEIER1.bit.INTx7 = 1; // Timer0 interrupt enable

// EPWM Timer INT
       PieCtrlRegs.PIEIER3.bit.INTx1 = 1;// ePWM1 interrupt enable
       PieCtrlRegs.PIEIER3.bit.INTx2 = 1;// ePWM2 interrupt enable

// Enable eCAP Interrupt
     PieCtrlRegs.PIEIER4.bit.INTx1 =1; // eCAP1 INT
     PieCtrlRegs.PIEIER4.bit.INTx2 =1; // eCAP2 INT
     PieCtrlRegs.PIEIER4.bit.INTx3 =1; // eCAP3 INT

//Enable global Interrupts and higher priority real-time debug events:
  // IER |= M_INT1; //Enable group 1 interrupts
   EINT;  // Enable Global interrupt INTM
   ERTM;  // Enable Global realtime interrupt DBGM
// Configure Timer0 to trigger ADC1
   CpuTimer0Regs.TCR.bit.TSS=1; //stop the timer
   CpuTimer0Regs.PRD.all=9999; // CPUTimer0 interrupt
   CpuTimer0Regs.TCR.bit.TRB=1; //reload the timer
   CpuTimer0Regs.TCR.bit.TIE=1; // Enable the timer interrupt
   CpuTimer0Regs.TCR.bit.TSS=0; //start the timer


  //Generate Sine look up table

     for(N=0;N<samples;N++)
     {
          sine_table[N]=0;
     }
```

```
        N=0;
    for(N=0;N<samples;N++)
    {
        sine_table[N]=fabs(sin(2*PI*60*N*step));

        if(sine_table[N]<flat)
        {
       sine_table[N]=flat;
        }

    }

//take conversions indefinitely in loop
   do
   {
        if((Voltage1>1500)&&(Flag1==0))
                {
                        Flag1=1;
                 GpioDataRegs.GPCSET.bit.GPIO72=1; //SET GPIO15
                 EPwm2Regs.TBPHS.bit.TBPHS = 0x0000;
                 EPwm3Regs.TBPHS.bit.TBPHS = 2500;
                 FlagRise1=1;
                 if(EPwm2Regs.CMPA.bit.CMPA <= 1250)
                                {
                                        EPwm2Regs.AQSFRC.bit.ACTSFA=1; //Clear
low
                                        EPwm3Regs.AQSFRC.bit.ACTSFA=1; //Clear
low
                                }
                                else
                                {
                                        EPwm2Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                                        EPwm3Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                                }
                // EPwm3Regs.CMPA.bit.CMPA=2400;
                 EPwm2Regs.AQSFRC.bit.OTSFA=1;
                 EPwm3Regs.AQSFRC.bit.OTSFA=1;
                 ECap1Regs.TSCTR=0;
                 index1=0;



                }
```

```
            if ((Voltage1<1500) && (Flag1==1))
               {
                     Flag1=0;
                    GpioDataRegs.GPCCLEAR.bit.GPIO72=1; //CLEAR GPIO15
                    EPwm2Regs.TBPHS.bit.TBPHS=2500;
                       EPwm3Regs.TBPHS.bit.TBPHS = 0x0000;
                       FlagFall1=1;
                     if(EPwm2Regs.CMPA.bit.CMPA <= 1250)
                                 {
                                       EPwm2Regs.AQSFRC.bit.ACTSFA=1; //Clear
low
                                       EPwm3Regs.AQSFRC.bit.ACTSFA=1; //Clear
low

                                 }
                                 else
                                 {
                                       EPwm2Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                                       EPwm3Regs.AQSFRC.bit.ACTSFA=3; // Toggle

                                 }
                       // EPwm2Regs.CMPA.bit.CMPA=2400;
                    EPwm2Regs.AQSFRC.bit.OTSFA=1;
                    EPwm3Regs.AQSFRC.bit.OTSFA=1;
                    ECap1Regs.TSCTR=0;
                    index1=0;

               }

             if((Voltage2>1850)&&(Flag2==0))
                    {
                           Flag2=1;
                     GpioDataRegs.GPCSET.bit.GPIO74=1; //SET GPIO15
                     EPwm4Regs.TBPHS.bit.TBPHS = 2500;
                     EPwm5Regs.TBPHS.bit.TBPHS = 0;
                     FlagRise2=1;

                    if(EPwm4Regs.CMPA.bit.CMPA <= 1250)
                      {
                            EPwm4Regs.AQSFRC.bit.ACTSFA=1; //Clear low
                            EPwm5Regs.AQSFRC.bit.ACTSFA=1; //Clear low
                      }
                    else
                      {
```

```
            EPwm4Regs.AQSFRC.bit.ACTSFA=3; // Toggle
            EPwm5Regs.AQSFRC.bit.ACTSFA=3; // Toggle
           }
           EPwm4Regs.AQSFRC.bit.OTSFA=1;
           EPwm5Regs.AQSFRC.bit.OTSFA=1;
           ECap2Regs.TSCTR=0;
           index2=0;
          }
    if ((Voltage2<1850) && (Flag2==1))
    {
          Flag2=0;
          GpioDataRegs.GPCCLEAR.bit.GPIO74=1; //CLEAR GPIO15
          EPwm4Regs.TBPHS.bit.TBPHS = 0;
          EPwm5Regs.TBPHS.bit.TBPHS = 2500;
             FlagFall2=1;

         if(EPwm4Regs.CMPA.bit.CMPA <= 1250)
           {
                 EPwm4Regs.AQSFRC.bit.ACTSFA=1; //Clear low
                 EPwm5Regs.AQSFRC.bit.ACTSFA=1; //Clear low
           }
         else
           {
            EPwm4Regs.AQSFRC.bit.ACTSFA=3; // Toggle
            EPwm5Regs.AQSFRC.bit.ACTSFA=3; // Toggle
           }

          EPwm4Regs.AQSFRC.bit.OTSFA=1;
          EPwm5Regs.AQSFRC.bit.OTSFA=1;
          ECap2Regs.TSCTR=0;
          index2=0;
    }

if((Voltage3>1850)&&(Flag3==0))
          {
                  Flag3=1;
           GpioDataRegs.GPCSET.bit.GPIO76=1; //SET GPIO15
           EPwm6Regs.TBPHS.bit.TBPHS = 0;
           EPwm7Regs.TBPHS.bit.TBPHS = 2500;
           FlagRise3=1;

          if(EPwm6Regs.CMPA.bit.CMPA <= 1250)
         {
                 EPwm6Regs.AQSFRC.bit.ACTSFA=1; //Clear low
```

```
                    EPwm7Regs.AQSFRC.bit.ACTSFA=1; //Clear low
                  }
                 else
                   {
                    EPwm6Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                    EPwm7Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                   }
                  EPwm6Regs.AQSFRC.bit.OTSFA=1;
                  EPwm7Regs.AQSFRC.bit.OTSFA=1;
                  ECap3Regs.TSCTR=0;
                  index3=0;

                 }
 if ((Voltage3<1850) && (Flag3==1))
        {
           Flag3=0;
             GpioDataRegs.GPCCLEAR.bit.GPIO76=1; //CLEAR GPIO15
             EPwm6Regs.TBPHS.bit.TBPHS = 2500;
             EPwm7Regs.TBPHS.bit.TBPHS = 0;
                FlagFall3=1;

            if(EPwm6Regs.CMPA.bit.CMPA <= 1250)
              {
               EPwm6Regs.AQSFRC.bit.ACTSFA=1; //Clear low
               EPwm7Regs.AQSFRC.bit.ACTSFA=1; //Clear low
              }
            else
              {
               EPwm6Regs.AQSFRC.bit.ACTSFA=3; // Toggle
               EPwm7Regs.AQSFRC.bit.ACTSFA=3; // Toggle
               }
             EPwm6Regs.AQSFRC.bit.OTSFA=1;
             EPwm7Regs.AQSFRC.bit.OTSFA=1;
             ECap3Regs.TSCTR=0;
             index3=0;
        }

   //start ePWM
//EPwm1Regs.ETSEL.bit.SOCAEN = 1;  //enable SOCA
//EPwm1Regs.TBCTL.bit.CTRMODE = 0; //unfreeze, and enter up count mode

   //wait while ePWM causes ADC conversions, which then cause interrupts,
   //which fill the results buffer, eventually setting the bufferFull
   //flag
```

```
        //while(!bufferFull);
        //bufferFull = 0; //clear the buffer full flag

        //stop ePWM
      //EPwm1Regs.ETSEL.bit.SOCAEN = 0;  //disable SOCA
      //EPwm1Regs.TBCTL.bit.CTRMODE = 3; //freeze counter

        //at this point, AdcaResults[] contains a sequence of conversions
        //from the selected channel

        //software breakpoint, hit run again to get updated conversions
        //asm("   ESTOP0");


   }while(1);
}

//Write ADC configurations and power up the ADC for both ADC A and ADC B
void ConfigureADC(void)
{
        EALLOW;

        //write configurations
        AdcaRegs.ADCCTL2.bit.PRESCALE = 6; //set ADCCLK divider to /4
   AdcSetMode(ADC_ADCA, ADC_RESOLUTION_12BIT,
ADC_SIGNALMODE_SINGLE);

        //Set pulse positions to late
        AdcaRegs.ADCCTL1.bit.INTPULSEPOS = 1;

        //power up the ADC
        AdcaRegs.ADCCTL1.bit.ADCPWDNZ = 1;

        //delay for 1ms to allow ADC time to power up
        DELAY_US(1000);

        EDIS;
}

void ConfigureEPWM(void)
{
        //EPWM1
        //////////////////////////////////////////////////////////////////////////////////////////
/*      // Enable TZ1 as one shot trip sources
```

```
                EALLOW;
                EPwm1Regs.TZSEL.bit.CBC1 = 1;

                // What do we want the TZ1 to do?
                EPwm1Regs.TZCTL.bit.TZA = TZ_FORCE_HI;

                // Enable TZ interrupt
                EPwm1Regs.TZEINT.bit.OST = 1;
                EDIS;
*/

            EPwm1Regs.ETSEL.bit.INTSEL=1;
                EPwm1Regs.ETSEL.bit.INTEN=1;
                EPwm1Regs.ETPS.bit.INTPRD = 1;

                EPwm1Regs.TBPRD = 2500;                   // Set timer period
                EPwm1Regs.TBPHS.bit.TBPHS = 1250;         // Phase is 0
                EPwm1Regs.TBCTR = 0x0000;                 // Clear counter

                // Setup TBCLK
                EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; //
Count up-down
                EPwm1Regs.TBCTL.bit.PHSEN = TB_ENABLE;       // Enable phase
loading
                EPwm1Regs.TBCTL.bit.SYNCOSEL = 1;            // TBCTR=0
                EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;     // Clock ratio to
SYSCLKOUT
                EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;

                EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;    // Load
registers every ZERO
                EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;

                // Setup compare
                EPwm1Regs.CMPA.bit.CMPA = 2500;
                EPwm1Regs.CMPB.bit.CMPB= 2500;

                // Set actions
                EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;           // Set PWM1A on
CAU
                EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;         // Clear PWM1A
on CAD

                // Dead Band Module Configuration
```

```
                //EPwm1Regs.DBCTL.bit.OUT_MODE=3;
                //EPwm1Regs.DBCTL.bit.POLSEL=0;
                //EPwm1Regs.DBCTL.bit.IN_MODE=0;

                //EPwm1Regs.DBRED=0; // Rising Edge Delay
                //EPwm1Regs.DBFED=0; // Falling Edge Delay

        ////////////////////////////////////////////////////////////////////////////////

        //EPWM2
        ////////////////////////////////////////////////////////////////////////////////

  //Enable TZ1 and TZ2 as one cycle-by-cycle trip sources
    EALLOW;
    EPwm2Regs.TZSEL.bit.CBC1=1;

    // What do we want the TZ1 and TZ2 to do?
    EPwm2Regs.TZCTL.bit.TZA = TZ_FORCE_LO;
    //EPwm2Regs.TZCTL.bit.TZB = TZ_FORCE_LO;

    // Enable TZ interrupt
    EPwm2Regs.TZEINT.bit.CBC = 1;
    EDIS;

      //EPwm2Regs.ETSEL.bit.INTSEL=1;
      //EPwm2Regs.ETSEL.bit.INTEN=1;

   //Software force
                EPwm2Regs.AQSFRC.bit.ACTSFA=3; //Toggle

                EPwm2Regs.TBPRD = 2500;                 // Set timer period
                EPwm2Regs.TBPHS.bit.TBPHS = 0x0000;     // Phase is 0
                EPwm2Regs.TBCTR = 0x0000;               // Clear counter

        // Setup TBCLK
                EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; //
Count up-down
                EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;      // Enable phase
loading
                EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;   // Pass through
                EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;     // Clock ratio to
SYSCLKOUT
                EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
```

```
            EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;    // Load
registers every ZERO
            EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;

        // Setup compare
            EPwm2Regs.CMPA.bit.CMPA = D1;

        // Set actions
            EPwm2Regs.AQCTLA.bit.ZRO = AQ_SET;           // Set PWM1A on
CAU
            EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;         // Clear PWM1A
on CAD

        // Dead Band Module Configuration
        //      EPwm2Regs.DBCTL.bit.OUT_MODE=3;
        //      EPwm2Regs.DBCTL.bit.POLSEL=0;
        //      EPwm2Regs.DBCTL.bit.IN_MODE=0;

        //      EPwm2Regs.DBRED=0; // Rising Edge Delay
        //      EPwm2Regs.DBFED=0; // Falling Edge Delay

        ////////////////////////////////////////////////////////////////////////////////
        //EPWM3
        ////////////////////////////////////////////////////////////////////////////////
            //Enable TZ1 and TZ2 as one cycle-by-cycle trip sources
            EALLOW;
            EPwm3Regs.TZSEL.bit.CBC1 = 1;

                // What do we want the TZ1 and TZ2 to do?
            EPwm3Regs.TZCTL.bit.TZA = TZ_FORCE_LO;
            //EPwm3Regs.TZCTL.bit.TZB = TZ_FORCE_LO;

                // Enable TZ interrupt
    EPwm3Regs.TZEINT.bit.CBC = 1;
            EDIS;

            //Software force
            EPwm3Regs.AQSFRC.bit.ACTSFA=3; //toggle

            EPwm3Regs.TBPRD = 2500;                  // Set timer period
            EPwm3Regs.TBPHS.bit.TBPHS = 0;           // Phase is 0
            EPwm3Regs.TBCTR = 0x0000;                  // Clear counter

        // Setup TBCLK
```

```
                EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; //
Count up-down
                EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE;        // Enable phase
loading
                EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;    // Pass through
                EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;      // Clock ratio to
SYSCLKOUT
                EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1;

                EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;    // Load
registers every ZERO
                EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;

        // Setup compare
                EPwm3Regs.CMPA.bit.CMPA = D1;

        // Set actions
                EPwm3Regs.AQCTLA.bit.ZRO = AQ_SET;            // Set PWM1A on
CAU
                EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;          // Clear PWM1A
on CAD

        // Dead Band Module Configuration
                //EPwm3Regs.DBCTL.bit.OUT_MODE=3;
                //EPwm3Regs.DBCTL.bit.POLSEL=0;
                //EPwm3Regs.DBCTL.bit.IN_MODE=0;

           //EPwm3Regs.DBRED=0; // Rising Edge Delay
                //EPwm3Regs.DBFED=0; // Falling Edge Delay

        ////////////////////////////////////////////////////////////////////////////////////
  //EPWM4
        ////////////////////////////////////////////////////////////////////////////////////
        //Enable TZ1 and TZ2 as one cycle-by-cycle trip sources
                EALLOW;
                EPwm4Regs.TZSEL.bit.CBC2 = 1;

           // What do we want the TZ1 and TZ2 to do?
                EPwm4Regs.TZCTL.bit.TZA = TZ_FORCE_LO;

            // Enable TZ interrupt
           EPwm4Regs.TZEINT.bit.CBC = 1;
                EDIS;
        //Software force
```

```
        EPwm4Regs.AQSFRC.bit.ACTSFA=3; //toggle

        EPwm4Regs.TBPRD = 2500;                 // Set timer period
        EPwm4Regs.TBPHS.bit.TBPHS = 0x0000;     // Phase is 0
        EPwm4Regs.TBCTR = 0x0000;               // Clear counter

    // Setup TBCLK
        EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up-down
        EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE;  // Enable phase loading
        EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;  // Pass through
        EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;  // Clock ratio to SYSCLKOUT
        EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;

        EPwm4Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;  // Load registers every ZERO
        EPwm4Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;

    // Setup compare
        EPwm4Regs.CMPA.bit.CMPA = D2;
        //EPwm4Regs.CMPB.bit.CMPB = 1200;

    // Set actions
        EPwm4Regs.AQCTLA.bit.ZRO = AQ_SET;      // Set PWM1A on CAU
        EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;    // Clear PWM1A on CAD

    // Dead Band Module Configuration
        //EPwm4Regs.DBCTL.bit.OUT_MODE=3;
        //EPwm4Regs.DBCTL.bit.POLSEL=0;
        //EPwm4Regs.DBCTL.bit.IN_MODE=0;

        //EPwm4Regs.DBRED=0; // Rising Edge Delay
        //EPwm4Regs.DBFED=0; // Falling Edge Delay

    ////////////////////////////////////////////////////////////////////////////////////
  //EPWM5
    ////////////////////////////////////////////////////////////////////////////////////
    //Enable TZ1 and TZ2 as one cycle-by-cycle trip sources
        EALLOW;
        EPwm5Regs.TZSEL.bit.CBC2 = 1;
```

```
        // What do we want the TZ1 and TZ2 to do?
        EPwm5Regs.TZCTL.bit.TZA = TZ_FORCE_LO;


        // Enable TZ interrupt
        EPwm5Regs.TZEINT.bit.CBC = 1;
        EDIS;

        EPwm5Regs.TBPRD = 2500;                  // Set timer period
        EPwm5Regs.TBPHS.bit.TBPHS = 2500;        // Phase is 0
        EPwm5Regs.TBCTR = 0x0000;                // Clear counter
   //Software force
                        EPwm5Regs.AQSFRC.bit.ACTSFA=3; //toggle
    // Setup TBCLK
        EPwm5Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; //
Count up-down
        EPwm5Regs.TBCTL.bit.PHSEN = TB_ENABLE;      // Enable phase
loading
        EPwm5Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;   // Pass through
        EPwm5Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;     // Clock ratio to
SYSCLKOUT
        EPwm5Regs.TBCTL.bit.CLKDIV = TB_DIV1;

        EPwm5Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;   // Load
registers every ZERO
        EPwm5Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;

    // Setup compare
        EPwm5Regs.CMPA.bit.CMPA = D2;

    // Set actions
        EPwm5Regs.AQCTLA.bit.ZRO = AQ_SET;          // Set PWM1A on
CAU
        EPwm5Regs.AQCTLA.bit.CAU = AQ_CLEAR;        // Clear PWM1A
on CAD

    // Dead Band Module Configuration
        //EPwm5Regs.DBCTL.bit.OUT_MODE=3;
        //EPwm5Regs.DBCTL.bit.POLSEL=0;
        //EPwm5Regs.DBCTL.bit.IN_MODE=0;

        //EPwm5Regs.DBRED=0; // Rising Edge Delay
        //EPwm5Regs.DBFED=0; // Falling Edge Delay
```

```
        ////////////////////////////////////////////////////////////////////////////////////
    //EPWM6
        ////////////////////////////////////////////////////////////////////////////////////
        //Enable TZ1 and TZ2 as one cycle-by-cycle trip sources
                EALLOW;
                EPwm6Regs.TZSEL.bit.CBC3 = 1;

                // What do we want the TZ1 and TZ2 to do?
                EPwm6Regs.TZCTL.bit.TZA = TZ_FORCE_LO;


                 // Enable TZ interrupt
                EPwm6Regs.TZEINT.bit.CBC = 1;
                EDIS;

                EPwm6Regs.TBPRD = 2500;                       // Set timer period
                EPwm6Regs.TBPHS.bit.TBPHS = 0x0000;           // Phase is 0
                EPwm6Regs.TBCTR = 0x0000;                     // Clear counter
        //Software force
                EPwm6Regs.AQSFRC.bit.ACTSFA=3; //toggle

        // Setup TBCLK
                EPwm6Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; //
Count up-down
                EPwm6Regs.TBCTL.bit.PHSEN = TB_ENABLE;        // Enable phase
loading
                EPwm6Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;    // Pass through
                EPwm6Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;      // Clock ratio to
SYSCLKOUT
                EPwm6Regs.TBCTL.bit.CLKDIV = TB_DIV1;

                EPwm6Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;    // Load
registers every ZERO
                EPwm6Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;

        // Setup compare
                EPwm6Regs.CMPA.bit.CMPA = D3;

        // Set actions
                EPwm6Regs.AQCTLA.bit.ZRO = AQ_SET;            // Set PWM1A on
CAU
                EPwm6Regs.AQCTLA.bit.CAU = AQ_CLEAR;          // Clear PWM1A
on CAD
```

```
        // Dead Band Module Configuration
                //EPwm6Regs.DBCTL.bit.OUT_MODE=3;
                //EPwm6Regs.DBCTL.bit.POLSEL=0;
                //EPwm6Regs.DBCTL.bit.IN_MODE=0;

                //EPwm6Regs.DBRED=0; // Rising Edge Delay
                //EPwm6Regs.DBFED=0; // Falling Edge Delay

        ////////////////////////////////////////////////////////////////////////////////////
        //EPWM7
        ////////////////////////////////////////////////////////////////////////////////////
        //Enable TZ1 and TZ2 as one cycle-by-cycle trip sources
                EALLOW;
                EPwm7Regs.TZSEL.bit.CBC3 = 1;

                // What do we want the TZ1 and TZ2 to do?
                EPwm7Regs.TZCTL.bit.TZA = TZ_FORCE_LO;


                // Enable TZ interrupt
                EPwm7Regs.TZEINT.bit.CBC = 1;
                EDIS;

                EPwm7Regs.TBPRD = 2500;                 // Set timer period
                EPwm7Regs.TBPHS.bit.TBPHS = 2500;       // Phase is 0
                EPwm7Regs.TBCTR = 0x0000;               // Clear counter
        //Software force
                EPwm7Regs.AQSFRC.bit.ACTSFA=3; //toggle

        // Setup TBCLK
                EPwm7Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; //
Count up-down
                EPwm7Regs.TBCTL.bit.PHSEN = TB_ENABLE;      // Enable phase
loading
                EPwm7Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;  // Pass through
                EPwm7Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;    // Clock ratio to
SYSCLKOUT
                EPwm7Regs.TBCTL.bit.CLKDIV = TB_DIV1;
                EPwm7Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;  // Load
registers every ZERO
                EPwm7Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;

        // Setup compare
```

```
            EPwm7Regs.CMPA.bit.CMPA = D3;

        // Set actions
            EPwm7Regs.AQCTLA.bit.ZRO = AQ_SET;          // Set PWM1A on
CAU
            EPwm7Regs.AQCTLA.bit.CAU = AQ_CLEAR;        // Clear PWM1A
on CAD

        // Dead Band Module Configuration
            //EPwm7Regs.DBCTL.bit.OUT_MODE=3;
            //EPwm7Regs.DBCTL.bit.POLSEL=0;
            //EPwm7Regs.DBCTL.bit.IN_MODE=0;

            //EPwm7Regs.DBRED=0; // Rising Edge Delay
            //EPwm7Regs.DBFED=0; // Falling Edge Delay

        ////////////////////////////////////////////////////////////////////////////////////////
}

void ConfigECap(void)
{   ////////////////////////////////////////////////////////////////////////////////////////
        // ECAP module 1 config
           ECap1Regs.ECEINT.all=0;
           ECap1Regs.ECCLR.all = 0xFF;
          // ECap1Regs.ECCTL1.all = 0;         // Disable ECCTL1
          // ECap1Regs.ECCTL2.all = 0;
           ECap1Regs.ECEINT.bit.CTR_EQ_PRD=1;

           ECap1Regs.ECCTL2.bit.CAP_APWM = 1;
           ECap1Regs.CAP1 = 6666; // Set period value
           ECap1Regs.CAP2 = 2500; // Set compare value
           ECap1Regs.CTRPHS = 0; // make eCAP1 reference phase = zero
           ECap1Regs.ECCTL2.bit.APWMPOL = 0;

           ECap1Regs.ECCTL2.bit.SYNCI_EN = 0; // No sync in for Master
           ECap1Regs.ECCTL2.bit.SYNCO_SEL = 1; // eCAP1 is Master
           ECap1Regs.ECCTL2.bit.TSCTRSTOP = 1; // Allow TSCTR to run
        ////////////////////////////////////////////////////////////////////////////////////////
   // ECAP module 2 config
            ECap2Regs.ECEINT.all=0;
           ECap2Regs.ECCLR.all = 0xFF;
          //  ECap2Regs.ECCTL1.all = 0;         // Disable ECCTL1
          //  ECap2Regs.ECCTL2.all = 0;
           ECap2Regs.ECEINT.bit.CTR_EQ_PRD=1;
```

```
        ECap2Regs.ECCTL2.bit.CAP_APWM = 1;
        ECap2Regs.CAP1 = 6666; // Set period value
        ECap2Regs.CAP2 = 2500; // Set compare value
        ECap2Regs.CTRPHS = 0; // make eCAP1 reference phase = zero
        ECap2Regs.ECCTL2.bit.APWMPOL = 0;

        ECap2Regs.ECCTL2.bit.SYNCI_EN = 0; // No sync in for Master
        ECap2Regs.ECCTL2.bit.SYNCO_SEL = 1; // eCAP1 is Master
        ECap2Regs.ECCTL2.bit.TSCTRSTOP = 1; // Allow TSCTR to run
      ////////////////////////////////////////////////////////////////////////////////////////
      // ECAP module 3 config
            ECap3Regs.ECEINT.all=0;
        ECap3Regs.ECCLR.all = 0xFF;
        //ECap3Regs.ECCTL1.all = 0;         // Disable ECCTL1
       // ECap3Regs.ECCTL2.all = 0;
        ECap3Regs.ECEINT.bit.CTR_EQ_PRD=1;

        ECap3Regs.ECCTL2.bit.CAP_APWM = 1;
        ECap3Regs.CAP1 = 6666; // Set period value
        ECap3Regs.CAP2 = 2500; // Set compare value
        ECap3Regs.CTRPHS = 0; // make eCAP1 reference phase = zero
        ECap3Regs.ECCTL2.bit.APWMPOL = 0;

        ECap3Regs.ECCTL2.bit.SYNCI_EN = 0; // No sync in for Master
        ECap3Regs.ECCTL2.bit.SYNCO_SEL = 1; // eCAP1 is Master
        ECap3Regs.ECCTL2.bit.TSCTRSTOP = 1; // Allow TSCTR to run
      ////////////////////////////////////////////////////////////////////////////////////////
      // ECAP module 4 config
        ECap4Regs.ECCTL2.bit.CAP_APWM = 1;
        ECap4Regs.CAP1 = 7500; // Set period value
        ECap4Regs.CAP2 = 3750; // Set compare value
        ECap4Regs.CTRPHS = 0; // make eCAP1 reference phase = zero
        ECap4Regs.ECCTL2.bit.APWMPOL = 0;
        ECap4Regs.ECCTL2.bit.SYNCI_EN = 0; // No sync in for Master
        ECap4Regs.ECCTL2.bit.SYNCO_SEL = 1; // eCAP1 is Master
        ECap4Regs.ECCTL2.bit.TSCTRSTOP = 1; // Allow TSCTR to run
        ////////////////////////////////////////////////////////////////////////////////////////
}

void SetupADCEpwm(Uint16 channel)
{
      Uint16 acqps;
```

```
	//determine minimum acquisition window (in SYSCLKS) based on resolution
	if(ADC_RESOLUTION_12BIT == AdcaRegs.ADCCTL2.bit.RESOLUTION){
		acqps = 14; //75ns
	}
	else { //resolution is 16-bit
		acqps = 63; //320ns
	}

	//Select the channels to convert and end of conversion flag
	EALLOW;
	AdcaRegs.ADCSOC0CTL.bit.CHSEL = 0;  //SOC0 will convert pin A0
	AdcaRegs.ADCSOC0CTL.bit.ACQPS = acqps; //sample window is 100
SYSCLK cycles
	AdcaRegs.ADCSOC0CTL.bit.TRIGSEL = 1; //trigger on TIMER0 SOCA/C

	AdcaRegs.ADCSOC1CTL.bit.CHSEL = 1;  //SOC1 will convert pin A1
	AdcaRegs.ADCSOC1CTL.bit.ACQPS = acqps; //sample window is 100
SYSCLK cycles
	AdcaRegs.ADCSOC1CTL.bit.TRIGSEL = 1; //trigger on TIMER0 SOCA/C

	AdcaRegs.ADCSOC2CTL.bit.CHSEL = 2;  //SOC2 will convert pin A2
	AdcaRegs.ADCSOC2CTL.bit.ACQPS = acqps; //sample window is 100
SYSCLK cycles
	AdcaRegs.ADCSOC2CTL.bit.TRIGSEL = 1; //trigger on TIMER0 SOCA/C

	AdcaRegs.ADCINTSEL1N2.bit.INT1SEL = 0; //end of SOC0 will set INT1 flag
	AdcaRegs.ADCINTSEL1N2.bit.INT1E = 1;   //enable INT1 flag
	AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //make sure INT1 flag is
cleared

	EDIS;
}

void GPIOConfig(void)
{
	EALLOW;
	//EPWM GPIO outputs

	GpioCtrlRegs.GPAPUD.bit.GPIO0 = 1;    // Disable pull-up on GPIO0
(EPWM1A)
	GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;   // Configure GPIO0 as EPWM1A
	GpioCtrlRegs.GPAPUD.bit.GPIO2 = 1;    // Disable pull-up on GPIO2
(EPWM2A)
	GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1;   // Configure GPIO2 as EPWM2A
```

```
        GpioCtrlRegs.GPAPUD.bit.GPIO4 = 1;    // Disable pull-up on GPIO4
(EPWM3A)
        GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 1;   // Configure GPIO4 as EPWM3A
        GpioCtrlRegs.GPAPUD.bit.GPIO6 = 1;    // Disable pull-up on GPIO6
(EPWM4A)
        GpioCtrlRegs.GPAMUX1.bit.GPIO6 = 1;   // Configure GPIO6 as EPWM4A
        GpioCtrlRegs.GPAPUD.bit.GPIO8 = 1;    // Disable pull-up on GPIO8
(EPWM5A)
        GpioCtrlRegs.GPAMUX1.bit.GPIO8 = 1;   // Configure GPIO8 as EPWM5A
        GpioCtrlRegs.GPAPUD.bit.GPIO10 = 1;    // Disable pull-up on GPIO10
(EPWM6A)
        GpioCtrlRegs.GPAMUX1.bit.GPIO10 = 1;   // Configure GPIO10 as EPWM6A
        GpioCtrlRegs.GPAPUD.bit.GPIO12 = 1;    // Disable pull-up on GPIO12
(EPWM7A)
        GpioCtrlRegs.GPAMUX1.bit.GPIO12 = 1;   // Configure GPIO12 as EPWM7A
 EDIS;
        //GPIO for Zero Crossing Reference
EALLOW;
        GpioCtrlRegs.GPCGMUX1.bit.GPIO72=0;
        GpioCtrlRegs.GPCMUX1.bit.GPIO72=0;
        GpioCtrlRegs.GPCDIR.bit.GPIO72=1;

        GpioCtrlRegs.GPCGMUX1.bit.GPIO74=0;
        GpioCtrlRegs.GPCMUX1.bit.GPIO74=0;
        GpioCtrlRegs.GPCDIR.bit.GPIO74=1;

        GpioCtrlRegs.GPCGMUX1.bit.GPIO76=0;
        GpioCtrlRegs.GPCMUX1.bit.GPIO76=0;
        GpioCtrlRegs.GPCDIR.bit.GPIO76=1;
EDIS;
        //ECAP GPIO outputs
EALLOW;
   OutputXbarRegs.OUTPUT1MUX0TO15CFG.bit.MUX0 = 3;     // Select ECAP1 as
output for MUX0 and send this to OUTPUTXBAR1
   OutputXbarRegs.OUTPUT1MUXENABLE.bit.MUX0 = 1;       // Enable MUX0 for
ECAP1.OUT
   GpioCtrlRegs.GPAMUX2.bit.GPIO24=1;// Select OUTPUTXBAR1 on GPIO58
   GpioCtrlRegs.GPADIR.bit.GPIO24=1;       // GPIO58 as output

   OutputXbarRegs.OUTPUT2MUX0TO15CFG.bit.MUX2 = 3;     // Select ECAP2 as
output for MUX2 and send this to OUTPUTXBAR2
   OutputXbarRegs.OUTPUT2MUXENABLE.bit.MUX2 = 1;       // Enable MUX2 for
ECAP2.OUT
```

```
   GpioCtrlRegs.GPAMUX2.bit.GPIO25 = 1;          // Select OUTPUTXBAR2 on
GPIO59
   GpioCtrlRegs.GPADIR.bit.GPIO25=1;       // GPIO59 as output

   OutputXbarRegs.OUTPUT3MUX0TO15CFG.bit.MUX4 = 3;     // Select ECAP2 as
output for MUX2 and send this to OUTPUTXBAR2
   OutputXbarRegs.OUTPUT3MUXENABLE.bit.MUX4 = 1;        // Enable MUX4 for
ECAP3.OUT
   GpioCtrlRegs.GPAMUX2.bit.GPIO26 = 1;          // Select OUTPUTXBAR3 on
GPIO60
   GpioCtrlRegs.GPADIR.bit.GPIO26=1;       // GPIO60 as output
EDIS;

   //GpioCtrlRegs.GPAPUD.bit.GPIO20 = 0;    // Enable pull-up on GPIO20 (TZ1)

   //GpioCtrlRegs.GPAQSEL2.bit.GPIO20 = 3;  // Asynch input GPIO20 (TZ1)

  // InputXbarRegs.INPUT1SELECT = 20;
EALLOW;

   //TZ GPIO inputs
   GpioCtrlRegs.GPAPUD.bit.GPIO20 = 0;    // Enable pull-up on GPIO20 (TZ1)
   GpioCtrlRegs.GPAQSEL2.bit.GPIO20 = 3;  // Asynch input GPIO20 (TZ1)
   InputXbarRegs.INPUT1SELECT=20;

   GpioCtrlRegs.GPAPUD.bit.GPIO21 = 0;    // Enable pull-up on GPIO21 (TZ2)
   GpioCtrlRegs.GPAQSEL2.bit.GPIO21 = 3;  // Asynch input GPIO21 (TZ2)
   InputXbarRegs.INPUT2SELECT=21;

   GpioCtrlRegs.GPAPUD.bit.GPIO22 = 0;    // Enable pull-up on GPIO22 (TZ1)
   GpioCtrlRegs.GPAQSEL2.bit.GPIO22 = 3;  // Asynch input GPIO22 (TZ1)
   InputXbarRegs.INPUT3SELECT=22;


EDIS;
   //GpioCtrlRegs.GPAPUD.bit.GPIO22 = 0;    // Enable pull-up on GPIO22 (TZ3)

   //GpioCtrlRegs.GPAQSEL2.bit.GPIO22 = 3;  // Asynch input GPIO22 (TZ3)

   //InputXbarRegs.INPUT2SELECT = 22;

   //GpioCtrlRegs.GPBPUD.bit.GPIO41 = 0;    // Enable pull-up on GPIO41 ()

  // GpioCtrlRegs.GPBQSEL1.bit.GPIO41 = 0;  // Asynch input GPIO22 (TZ3)
```

```
    //InputXbarRegs.INPUT3SELECT = 23;
    EALLOW;
    InputXbarRegs.INPUT5SELECT = 40; //EXT SINCIN

        EDIS;

}
__interrupt void adca1_isr(void)
{
        Voltage1 = AdcaResultRegs.ADCRESULT0;
        Voltage2 = AdcaResultRegs.ADCRESULT1;
        Voltage3=  AdcaResultRegs.ADCRESULT2;

        AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //clear INT1 flag
        PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
}

__interrupt void epwm1_isr(void)
{
        if(D1!=2500)
        {
        if (FlagFall1 == 1)
        {

                //if(EPwm2Regs.CMPA.bit.CMPA >= 1250)
                //{
                //      EPwm2Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                        EPwm2Regs.AQSFRC.bit.OTSFA=1; // One shoot sofware state
                //}

                FlagFall1 =0;
        }

        if (FlagRise1 == 1)
        {
        //      if(EPwm3Regs.CMPA.bit.CMPA >= 1250)
                                //{
                                        //EPwm3Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                                //}
                //else
                //{
                //      EPwm3Regs.AQSFRC.bit.ACTSFA=1; // Toggle
```

```
            //}
            EPwm3Regs.AQSFRC.bit.OTSFA=1; // One shoot sofware state

          FlagRise1=0;
        }

        if (FlagFall2 == 1)
                {

                        if(EPwm5Regs.CMPA.bit.CMPA >= 1250)
                        {
                                EPwm5Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                                EPwm5Regs.AQSFRC.bit.OTSFA=1; // One shoot
sofware state
                        }

                        FlagFall2 =0;
                }

                if (FlagRise2 == 1)
                {
                        if(EPwm4Regs.CMPA.bit.CMPA >= 1250)
                                        {
                                                EPwm4Regs.AQSFRC.bit.ACTSFA=3; //
Toggle
                                        }
                        else
                        {
                                EPwm4Regs.AQSFRC.bit.ACTSFA=1; // Toggle

                        }
                        EPwm4Regs.AQSFRC.bit.OTSFA=1; // One shoot sofware state

                  FlagRise2=0;
                }

                if (FlagFall3 == 1)
                        {

                                if(EPwm6Regs.CMPA.bit.CMPA >= 1250)
                                {
                                        EPwm6Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                                        EPwm6Regs.AQSFRC.bit.OTSFA=1; // One shoot
sofware state
```

```
                        }

                        FlagFall3 =0;
                    }

                    if (FlagRise3 == 1)
                    {
                        if(EPwm7Regs.CMPA.bit.CMPA >= 1250)
                                {

        EPwm7Regs.AQSFRC.bit.ACTSFA=3; // Toggle
                                }
                        else
                        {
                                EPwm7Regs.AQSFRC.bit.ACTSFA=1; // Toggle

                        }
                        EPwm7Regs.AQSFRC.bit.OTSFA=1; // One shoot
sofware state

                      FlagRise3=0;
                    }
        }
         // Clear INT flag for this timer
           EPwm1Regs.ETCLR.bit.INT = 1;

           // Acknowledge this interrupt to receive more interrupts from group 3
           PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
}

__interrupt void epwm2_tzint_isr(void)
{
        EPwm2TZIntCount++;

        // To Re-enable the OST Interrupt, do the following:
        EALLOW;
        EPwm2Regs.TZCLR.bit.CBC = 1;
        EPwm2Regs.TZCLR.bit.INT = 1;
   EDIS;

   // Acknowledge this interrupt to receive more interrupts from group 2
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP2;
}
```

```
__interrupt void epwm3_tzint_isr(void)
{
        EPwm3TZIntCount++;

        // Clear the flags - we will continue to take
        // this interrupt until the TZ pin goes high
        EALLOW;
        EPwm3Regs.TZCLR.bit.CBC = 1;
        EPwm3Regs.TZCLR.bit.INT = 1;
        EDIS;

   // Acknowledge this interrupt to receive more interrupts from group 2
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP2;
}

__interrupt void epwm4_tzint_isr(void)
{
        EPwm4TZIntCount++;

        // To Re-enable the OST Interrupt, do the following:
        EALLOW;
        EPwm4Regs.TZCLR.bit.CBC = 1;
        EPwm4Regs.TZCLR.bit.INT = 1;
   EDIS;

   // Acknowledge this interrupt to receive more interrupts from group 2
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP2;
}

__interrupt void epwm5_tzint_isr(void)
{
        EPwm5TZIntCount++;

        // Clear the flags - we will continue to take
        // this interrupt until the TZ pin goes high
        EALLOW;
        EPwm5Regs.TZCLR.bit.CBC = 1;
        EPwm5Regs.TZCLR.bit.INT = 1;
        EDIS;

   // Acknowledge this interrupt to receive more interrupts from group 2
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP2;
}
```

```
__interrupt void epwm6_tzint_isr(void)
{
        EPwm6TZIntCount++;

        // To Re-enable the OST Interrupt, do the following:
        EALLOW;
        EPwm6Regs.TZCLR.bit.CBC = 1;
        EPwm6Regs.TZCLR.bit.INT = 1;
   EDIS;

   // Acknowledge this interrupt to receive more interrupts from group 2
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP2;
}

__interrupt void epwm7_tzint_isr(void)
{
        EPwm7TZIntCount++;

        // Clear the flags - we will continue to take
        // this interrupt until the TZ pin goes high
        EALLOW;
        EPwm7Regs.TZCLR.bit.CBC = 1;
        EPwm7Regs.TZCLR.bit.INT = 1;
        EDIS;

   // Acknowledge this interrupt to receive more interrupts from group 2
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP2;
}


__interrupt void timer0_isr(void)
{
         count++;
         PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
}
__interrupt void ecap1_isr(void)
{
        ECap1Regs.CAP4 = sine_table[index1]*6666;

                index1++; // Go to next sample in sin_table

                ///if (ECap1Regs.CAP2<400)
                //{
                //ECap1Regs.CAP2=0;
```

```
                //}

                if (index1>samples)
                {
                        index1=0;
                }

          ECap1Regs.ECCLR.bit.CTR_PRD=1;
          ECap1Regs.ECCLR.bit.INT = 1;
    PieCtrlRegs.PIEACK.all = PIEACK_GROUP4; //re-enable the PIEACK bit
}

__interrupt void ecap2_isr(void)
{
        ECap2Regs.CAP4 = sine_table[index2]*6666;

                index2++; // Go to next sample in sin_table

                if (index2>samples)
                {
                        index2=0;
                }

          ECap2Regs.ECCLR.bit.CTR_PRD = 1;
          ECap2Regs.ECCLR.bit.INT = 1;
    PieCtrlRegs.PIEACK.all = PIEACK_GROUP4; //re-enable the PIEACK bit
}

__interrupt void ecap3_isr(void)
{
        ECap3Regs.CAP4 = sine_table[index3]*6666;

                index3++; // Go to next sample in sin_table

                if (index3>samples)
                {
                        index3=0;
                }

          ECap3Regs.ECCLR.bit.CTR_PRD = 1;
          ECap3Regs.ECCLR.bit.INT = 1;
    PieCtrlRegs.PIEACK.all = PIEACK_GROUP4; //re-enable the PIEACK bit
}
```