DEVELOPING PROCEDURES TO ASSESS THE PERFORMANCE OF THE MUON BACKEND ELECTRONICS FOR THE HL-LHC UPGRADE AT CERN

An Undergraduate Research Scholars Thesis

by

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RESEARCH COMPLIANCE CERTIFICATION

Research activities involving the use of human subjects, vertebrate animals, and/or biohazards must be reviewed and approved by the appropriate Texas A&M University regulatory research committee (i.e., IRB, IACUC, IBC) before the activity can commence. This requirement applies to activities conducted at Texas A&M and to activities conducted at non-Texas A&M facilities or institutions. In both cases, students are responsible for working with the relevant Texas A&M research compliance program to ensure and document that all Texas A&M compliance obligations are met before the study begins.

I, Ghassan Ali Ahmad, certify that all research compliance requirements related to this Undergraduate Research Scholars thesis have been addressed with my Faculty Research Advisors prior to the collection of any data used in this final thesis submission.

This project did not require approval from the Texas A&M University Research Compliance & Biosafety office.

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ABSTRACT

Developing Procedures to Assess The Performance of The Muon Backend Electronics for The HL-LHC Upgrade at CERN

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In light of the ongoing and planned major upgrades to the Large Hadron Collider (LHC) at CERN, the experiments operating at the LHC will need to adapt to the environment with a much increased rate of interactions and detector occupancy. The Compact Muon Solenoid (CMS) experiment is expected to observe collisions at a significantly increased rate, and upgraded electronics must be implemented to handle the increased data rate as a result. In order to have confidence in the functionality of these optimized electronics, every hardware component must be validated with clearly defined specifications. The purpose of this paper is to design hardware diagnostics procedures to validate that the upgraded backend electronics boards (X2O) for the CMS muon trigger and subsystems at the Large Hadron Collider will meet the performance requirements. In essence, this paper can be utilized as a user manual for testing the operating conditions of the hardware components of the X2O and ensuring these conditions are within the required specifications. This user manual will clearly define the diagnostic tools and procedures for each test, along with providing the data collected from each respective test of the X2O board at the Texas A&M CMS electronics lab. Supplying these procedures is crucial for the long-term goal of equipping future research and development of the High-Luminosity LHC project, which will

produce more collisions and therefore more data to process and improve our knowledge of fundamental properties of matter and potentially yielding new discoveries.

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NOMENCLATURE

TAMU	Texas A&M University
LHC	Large Hadron Collider
HL-LHC	High Luminosity Large Hadron Collider
CMS	Compact Muon Solenoid
ATCA	Advanced Telecommunications Computing Architecture
FPGA	Field Programmable Gate Array
VUP13	Virtex™ UltraScale+ 13
CSC	Cathode Strip Chamber
PPM	Parts Per Million
QSFP	Quad Small Form Factor Pluggable

1. INTRODUCTION

1.1 The Large Hadron Collider at CERN

The Large Hadron Collider (LHC), the most powerful particle collider in the world, is located in Geneva, Switzerland. Built by the European Organization of Nuclear Research (CERN), it contains a large ring with a circumference of 27 kilometers and lies over 100 meters underground [1]. The ring consists of a beam pipe pumped down to a near-vacuum condition where proton bunches are accelerated to nearly the speed of light in opposing directions using strong electric fields and superconducting magnets [2]. There are 4 collision zones along the LHC ring with each having a unique experimental purpose. When the highly energetic particles collide, the conditions present one billionth of a second after the Big Bang can be recreated in this controlled environment [3]. Through observing these collisions, some of today's most pressing unresolved topics within physics can be explored, such as dark matter, dark energy, and supersymmetry.

1.2 The Compact Muon Solenoid Experiment

One of the four LHC collision zones holds the Compact Muon Solenoid (CMS), which is a particle experiment used for measuring the various products of the collisions. The system consists of multiple cylindrical layers, which work together to identify and measure properties of different particles produced in the collisions of high energy proton beams. A superconducting solenoid lies in its center and provides immense magnetic field of 3.8 Tesla, capable of bending the trajectories of the charged particles that pass through the detector [4]. The outermost layers contain the muon detector system, which is responsible for tracking the trajectories of the muons passing through. The momenta of the muons can be determined by measuring the bending angle induced by the magnet. Other detector layers of the CMS experiment observe different types of particles that are generated from the high energy proton-proton collisions.

1.3 The High-Luminosity LHC

At the current integrated luminosity, the LHC produces approximately one inelastic event every 25 nanoseconds (40 million collisions per second) [4]. The ongoing period of testing is known as Run-3. However, there is a major upgrade to the LHC in preparation that involves increasing the integrated luminosity. This project is known as the High Luminosity LHC (HL-LHC), and it will result in more energetic collisions, a higher rate of data, and ultimately more physics potential of CMS and the LHC as a whole [5]. As a result, the CMS in general and its muon system electronics and detectors in particular are in need of an upgrade to keep up with the increased volume of data produced by the HL-LHC.

1.4 Project Objective & Purpose

For the upcoming Long Shutdown 3 (LS3), major installations are planned for the CMS detectors and electronics to handle the increased data rate. Without the proper improvements to the data processing system, there will be losses in valuable data and errors in functionality. Of these upgrades is the X2O modular system in the backend hardware of the CMS detectors. In order to ensure the reliability of the new electronics, all components of this backend apparatus must be proven to exceed performance specifications and pass/fail thresholds must be set for measurements such as temperature or voltage. A set of procedures and diagnostics tests that certify the upgraded boards meet specifications will provide a reliable criteria to be established for quality control and future functionality testing of the CMS experiment backend system. This project aims to provide this for the installation, maintenance, and debugging of the X2O processor board. These will be accomplished through testing with the X2O prototype board and testing setup at the Texas A&M CMS lab using the 0xBEFE GitLab repository of python scripts. The results and analysis will be presented after the procedures have been clearly defined. This chapter outlines and contextualizes the project and its goals in order to explain its scientific purpose. Chapter 2 will provide a detailed procedural description of the methodologies employed in each of the hardware tests involved in this project to obtain scientifically valid results. Then, the actual results

obtained using these testing procedures will be presented in Chapter 3. Chapter 3 will also include in-depth analysis of the results of the tests. Finally, Chapter 4 will conclude the thesis and provide a summary of the objective of this project, the methods used to obtain the results, and the project as a whole.

1.5 X2O Board Overview

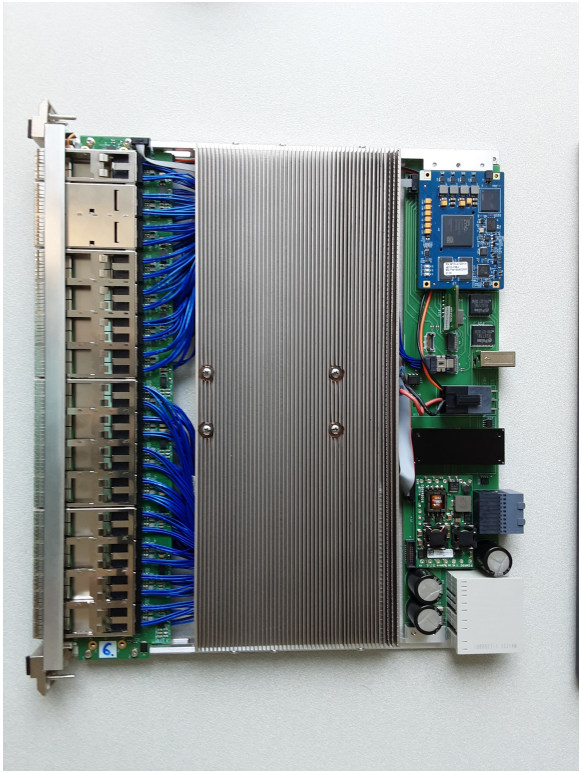

Figure 1: *Bottom view of the X2O board* [6]

The X2O board is a modular card compatible with Advanced Telecommunications Computing Architecture (ATCA) standard. It is a custom made circuit board specifically catered towards handling muon data. It's higher data processing speed and higher bandwidth provides a significant upgrade to the muon data handling system. The circuit board's control interface is based on ZYNQ system-on-chip manufactured by Xilinx. This is also employed as an IPMC host in addition to a control interface. [7]

The X2O board is composed of 3 modules, each of which serve unique purposes [7]. Firstly, the power module connects to the backplane of the ATCA crate and is responsible for providing power to the board. This module hosts the Xilinx Zynq CPU + Field-Programmable Gate Array (FPGA) chip and runs a Linux based operating system called CentOS. Secondly, the FPGA module is the host of the main processor chip, the Xilinx VU13P FPGA, with 1.7 million logic gates. This FPGA supports optical links with 140 megabytes of fast memory storage. Finally, the optical module located near the front panel of the boards. The optical module provides 30 optical transceiver ports, and 120 optical links. Each optical link is capable of up to 25 gigabit per second processing speed, meaning the entire board is capable to up to 3 terabit per second data processing power [8]. Optical transceivers may be plugged into each of the optical module ports. Figure 2 displays the physical locations of the modules that have been discussed thus far [7].

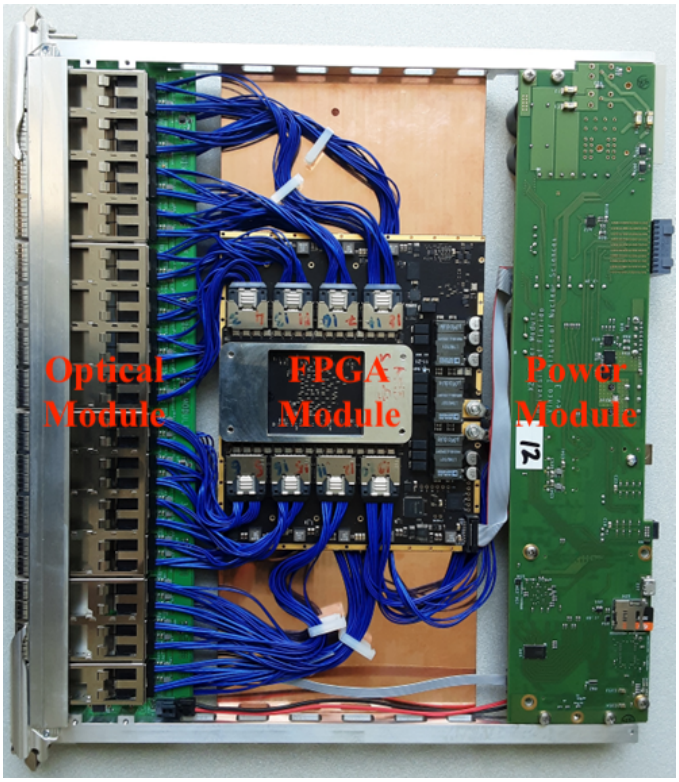

Figure 2: *Top view of the X2O board with module labels* [6]

X2O intermodule communication is achieved using various types of cable communications. The following block diagram illustrates these intermodule connections for convenient reference.

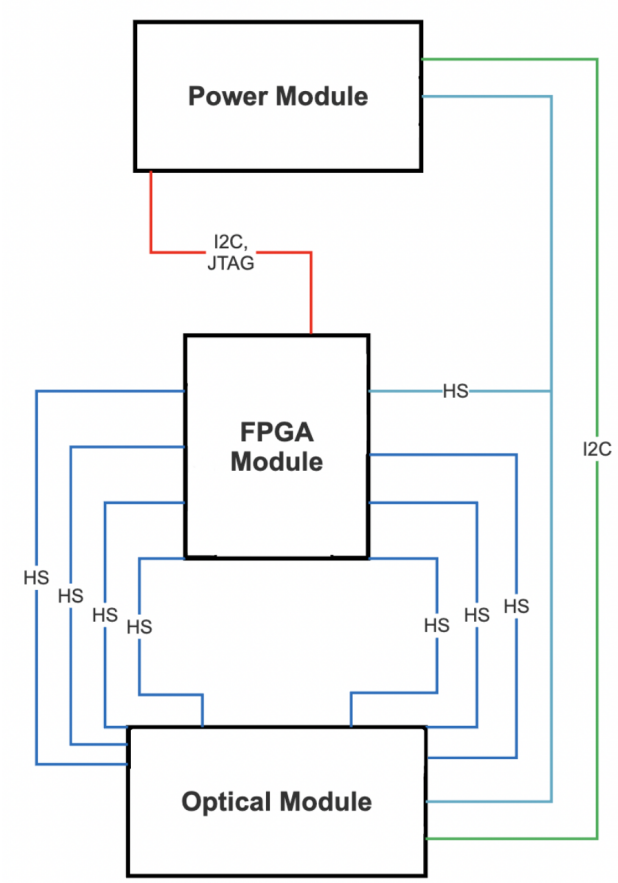

Figure 3: *X2O Intermodule Communication with HS representing High-Speed data, JTAG and I2C being used for control and monitoring.*

The optical and FPGA modules communicate via high speed HDR-225834 Samtec cables, which are represented by the blue lines in Figure 3. I^2C cables are used to communicate between the optical and power modules. These are depicted as the green lines shown in the block diagram. There is additional I^2C communication as well as JTAG cables that compose the connection between the power and FPGA modules, which is communication represented by the red connection of the diagram. Finally, there is one high speed HDR-225833 cable that connects the

FPGA to both the optical and power modules, which is displayed as a light-blue connection in Figure 3. All these cables are custom designed specifically for the purpose of intermodule communication of the X2O board.

The board subject to the testing that is outlined in this project is not a complete X2O board. The X2O board at Texas A&M is merely a prototype board that existing in the testing environment specifically for the purpose of testing particular components, systems, and configurations. As a result, some components are missing on this prototype that are present in the complete and functioning X2O board that will be produced and installed into the CMS electronics system.

2. METHODS

2.1 Principal Testing Conditions

Before the procedures are described in detail, the exact testing environment will be outlined and displayed for reference. Certain testing conditions may vary between the tests that will be defined later. However, the common and fundamental conditions that are present for every test is the topic of this section. As previously mentioned, the X2O board is compatible with Advanced Telecommunication Computing Architecture. The TAMU lab features an ATCA crate along with other components that provides a valid testing setup. This testing setup is intended to represent an X2O operational environment that would be implemented as major upgrades are completed at the muon data processing system at the Compact Muon Solenoid experiment. The intricate details of how the ATCA crate functions and its capabilities will not be discussed in this paper. However, its connectivity and its role in the testing environment are more relevant for the intents and purposes of this project and are worth noting. The ATCA crate of the CMS type provides 14 full width slots and 1 half width slot. Processor cards, such as the X2O, may be inserted into the full width slots. The crate used in this project has a network switch installed in slot 1 and an X2O board installed in slot 8. The ATCA crate provides cooling fans that are programmable to different speeds, which is crucial to the testing conduced in this project. The following image displays how the ATCA crate plays its role in the testing framework, along with how the X2O board was plugged into it.

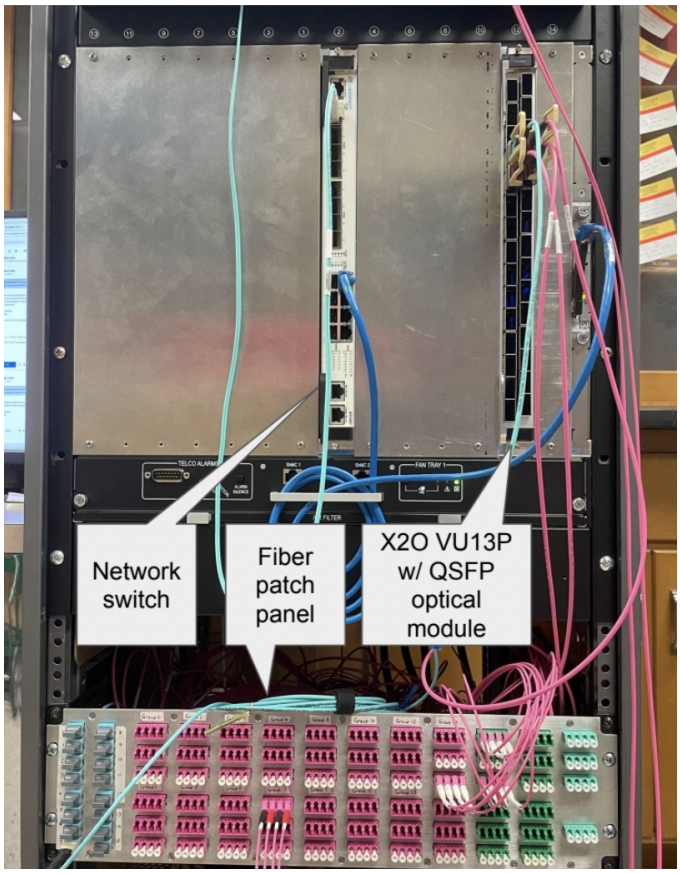

Figure 4: *ATCA Crate at TAMU* [9]

The labels on the image indicate what major components are involved in the ATCA crate testing setup. The X2O board is displayed on the right, and the optical module ports are visible. The fiber patch panel is displayed on the bottom, and the network switch is shown in slot 1 of the crate to the left of the X2O board.

2.2 Common Procedure & Standardized Testing Conditions

There are underlying procedures that must be carried out before any of the testing outlined in this chapter is executed. Now that the testing environment at use has been clearly defined we may move forward with these procedures. The testing setup for the purposes of this project consisted of a control PC connected to the ATCA crate and a fiber optic switch box controlled by a Raspberry Pi with a monitor at the Texas A&M CMS lab. The X2O board has many electronic

devices that are extremely sensitive to static discharge. When handling and inspecting the board, it is crucial to ground oneself beforehand. Depending on external conditions, it may be necessary to discharge multiple times in the process of handling the board or any components involving it.

Now, the common procedure for the testing involved in this project is as follows. Firstly, the X2O board must be installed into the ATCA crate. As previously mentioned, the board used in this project was plugged into slot number 8. Once the board was installed, the power was turned on. At this point, the control PC was capable of signaling to the X2O interface on the network using the ping command. The X2O interface may require a few minutes to appear on the network. This process is essentially logging into the X2O CPU. This step is crucial for any of the hardware tests because it ensures that the board is on and reachable by the control PC through the network. The ping command can also be used to troubleshoot issues with connectivity.

From this point, the X2O was properly installed and reachable by the control PC. The software used to conduct the tests in the project all reside in the 0xBEFE CERN GitLab repository (Project ID: 107761). This repository must be imported and installed onto the control PC to run any of the tests in this project. Once it is ensured that the 0xBEFE software is installed, it is required to conduct a safety check on the physical conditions of the board. Before anything is run, however, it is required to maintain a sufficiently high fan level. For the purposes of this project, a fan level of 5 was required. The following displays the command to obtain a fan level of 5 in the command-line interface of the control PC.

```
./fan_level_5.sh
```

The process of the fan speed reaching the commanded level may take a few moments. At this point, the prerequisite conditions for all the operational tests in this project are satisfied. The safety check on the physical conditions of the hardware devices can be executed now. This is accomplished by using the monitor.py python script in the 0xBEFE repository. The following displays the command that executes this safety check using the monitor.py python script.

```
python3 boards/x2o/monitor.py
```

The active values for the critical measurable conditions of the hardware components are shown in the interface after running this command. The purpose of the safety check is to ensure that the voltage and temperature levels of the X2O card are not exceeding the absolute specifications and to prevent damaging the board's components. The absolute specifications that the board must not exceed are established in the results section of the voltage, current, and temperature tests.

As previously mentioned, it is crucial for a standardized testing environment to be established. In particular, the fan speed, number of optical transceivers, and the number of neighboring boards must be controlled across tests and between trials to ensure consistent testing results. This project works with only one prototype X2O board with no neighboring boards. Furthermore, the standardized fan speed is level 5, and the initial tests were conducted with no optical transceivers in the optical module of the X2O. Separate tests were also conducted with the maximum number of optical transceivers plugged into the optical module (30), which impact the temperatures of board components. The fan speed, however, may be raised to combat the increase in temperature, for example. Raising the fan speed to a higher level such as 6 would maintain the comfortable temperatures for the hardware devices that are investigated in this paper. These parameters are important to keep in mind when referring to the results of this project, because deviations from them have significant effects on the conditions of the hardware devices.

2.3 Voltage, Current, & Temperature Tests

The voltage, current, and temperature tests are intended to be a useful method of measuring the physical status of the certain hardware components of the board. Specifically, they serve the purpose of measuring the physical conditions of FPGA and non-FPGA related power rails. The methods of this section will commence at the point of the conclusion of the common procedure. Assuming the safety check has been completed and displays safe levels of temperatures, voltages, and current, the following procedure composes the physical tests of the X2O board. Firstly, from the home directory in the command-line interface, the CentOS linux running on the X2O Zynq processor must be accessed. This is accomplished by logging into the X2O from the

control PC:

```
ssh root@x2o
```

At this point, all commands are directed to the Linux operating system on the X2O card. The portion of the procedure following this point requires access to the 0xBEFE GitLab repository referred to in the common procedure. The directories in the repository may not coincide with the directories names referred to in the following steps to conduct the tests. The steps will proceed as they were completed to conduct the test at the time of writing. While there may be asymmetries between the procedure at outlined in this project and later in time as the repository get refined and updated, the conceptual systematic process is expected to remain the same.

After connecting to the X2O card, it is necessary to change to the directory where the initial 0xBEFE software are located by typing this on the command line.

```
cd ~/gem/0xbefe_test_refclks/scripts
```

Following this step, the environment variable needs to be established. The source environment that best configures the software for the purpose of this test is the CSC X2O environment. The in-line command to set this environment up is as follows.

```
source env.sh csc x2o 0
```

The FPGA programming may commence after this step. The purpose of the programming the FPGA is to load a specific firmware onto the main FPGA. The command to program the FPGA in the manner that is best suited for this test is the following.

```
python3 boards/x2o/program_fpga.py
```

A possible error that may occur after running this command is regarding the PC being unable to detect the FPGA and will appear as "ERROR: could not detect VU13P FPGA." This indicates that the FPGA is powered off. In the event that this error occurs, the following command powers up the FPGA.

```
python3 boards/x2o/power_up.py
```

The software should indicate whether the FPGA is now powered on or not. After powering on the FPGA, the previous command to program the FPGA must be repeated. Then, the next command is as follows.

```
python3 csc/init.py
```

There may be an error that follows this command that indicates a frontend missing bitfile. This error is not detrimental to the operation of this testing procedure and may be ignored. At this point, it is wise to check the condition of the X2O power rail components once again. This can be accomplished using the monitor.py python script referred to previously in the safety check portion of the common procedure. The command to accomplish this is:

```
python3 boards/x2o/monitor.py
```

The active monitoring measurements for key hardware components should be displayed. It is recommended to observe whether the measurements are nonsensical or extremely high to avoid danger to the condition of the board. After this is ensured, the X2O directory is accessed by running the following:

```
cd ~/jessica/0xbefe/scripts/boards/x2o
```

The physical test is then run with the following command.

```
python3 physical_test.py csc
```

This test displays the voltages, temperatures, and currents of both FPGA and non-FPGA power rails. This test was repeated multiple times over several days at different times of day in order to minimize environmental influence and other external factors to the state of the hardware components. Embedded in the script is code that automatically saves the exact measurements in a CSV data file.

The physical_test.py program does not display the temperatures of any optical transceivers. As previously mentioned, the voltage, current, and temperature tests explained thus far were conducted with no optical transceivers plugged into the optical module. However, tests were also conducted with 30 individual QSFP+ optical transceivers installed into the X2O board to emulate a more realistic power load. Before executing this test, however, the fan speed must be raised. A fan level of 6 was used for the testing involving 30 QSFPs. The fan speed is changed using the same command explained in the common procedure.

```
./fan_level_6.sh
```

The program that displays the active physical measurements for the QSFPs exists in the same directory as the physical_test.py program, and the command to execute this test is as follows.

```
python3 optics.py
```

The physical conditions of the QSFPs should be displayed after executing this program. The test was repeated several times in 5 minute increments until stable temperature measurements were observed. The measurements were recorded for each channel, and monitor.py was run once the stable temperature was reached to observe the internal temperatures of the power supplying devices.

2.4 FPGA Programmability Tests

The function of the FPGA is dependent on its ability to be programmed with certain firmware. The purpose of this test is to validate that the FPGA is programmed through the means of verifying slow control communication with the Zynq CPU. The links used in this communication are depicted by the JTAG communication path in Figure 3 in the X2O board overview section of the introduction. To ensure this communication is validated, the program that is employed in these tests programs the VU13P FPGA with CSC firmware and transmits a bitstream to it. The FPGA then executes a checksum function to ensure that the received bitstream has no errors. In

the event that errors in the bitstream are found, meaning the data integrity is unreliable, the FPGA will not start up. Each test executes this process 10 times.

The procedure to conduct this test will now be explained. As previously mentioned, the procedure begins at the point where the common procedure concludes, working from the scripts directory and using the same environment that was set up previously with the "source" function.

The testing indicated that the CSC environment displays the most compatibility with the goals of this project, however it is not a necessity as various environments may be sourced to conduct the testing that this project involves. With the FPGA powered on, the program that repeatedly programs the FPGA and verifies that it is programmed successfully is executed by using the following command.

```
python3 x2o_utils/fpga_short.py <insert path to bitfile>
```

The part of the command that says "<insert path to bitfile>" must be replaced with the desired bitfile path. The fpga_short.py script repeatedly programs the VU13P FPGA with CSC firmware, and commands it to analyze the checksum of the received bit-stream. Each checksum iteration of the bit-streams that is incorrect will result in the FPGA not starting up. This program takes approximately 2 minutes to complete, and it was run 500 times overnight across multiple days to minimize external factors and maximize the validity of the collected data.

2.5 Oscillator Clock Tests

Within the X2O board, there are normally 32 reference crystal oscillator clock chips (SG3225VEN - DDGA) and one clock synthesizer chip. However, the prototype here at TAMU was designed to function with only 30 oscillator reference clocks. The functionality of the oscillator chips are crucial to any testing involving the X2O and the capabilities of the board as whole. For the purposes of the X2O, these oscillators are employed as reference clocks that aid in high speed optical communication. Without properly functioning reference clocks, the optical links would fail to provide reliable communication and there would be inconsistent time resolution for the detector data to corresponding collisions. As a result, it is paramount that these clocks reliably run at a consistent frequency.

The X2O board contains two types of clocks. These are referred to as synchronous and asynchronous clocks. The asynchronous clocks are the crystal oscillators that were referenced previously. The synchronous clocks are provided by the synthesizer chip. It is important to note that the synthesizer chip that provides the synchronous clocks is not present in the prototype X2O board that is subject to the testing outlined in this paper. Therefore, the clocks that are being tested will exclusively consist of the asynchronous clocks. Following this point, "clocks" will refer to strictly the asynchronous clocks.

The goal of the clock tests is to ensure the functionality of the oscillators by the method of measuring their frequencies. The software that accomplishes this conducts 100 reads of the frequencies for each clock every time the program is run. The procedure for using this program and collecting the necessary data begins with the preparation steps outlined in the common procedure to source the environment and power up the FPGA to ensure the X2O is ready for this test.

The software measures the nominal frequencies of the clocks with the following command from the scripts directory.

```
python3 boards/x2o/x2o_utils/refclk_freq_monitor.py
```

As previously mentioned, the purpose of this test is to measure the frequencies at which these clocks oscillate. The program conducts 100 reads of the frequencies for each iteration. The expected value for the frequency of these clocks is 156.25 MHz, and the specification for the frequency tolerance is within ± 25 parts per million (PPM) error from that expected value [10]. In general, the results of these tests should be analyzed against the expected value and the tolerance to validate the functionality of the oscillators.

2.6 High-Speed Communication Tests

The high-speed communication tests involves validating that communication between the high-speed optical links of the board are functional. The test conducted to validate this communication involves ensuring the link connectivity and that the bit error rate is sufficiently low. Before beginning the high-speed communication testing procedure, the optical module of the X2O board

must be completely filled with QSFPs installed into each port and all the link channels must be disabled. The model used for these tests is the 40G QSFP+ model.

The link connectivity is tested with the following procedure. Continuing from the X2O directory, the following command runs the program that performs a loop-back test between the installed QSFPs.

```
python3 boards/x2o/x2o_utils/optic_test.py
```

After running this test, rows of 3 numbers separated by commas are displayed. The first number represents the cage number, the second is the channel mask, and the third is the optical link number. The software indicates two things; the first is whether the internal communication through the high-speed cables is successfully achieved, and the second is the bit error rate of this communication. The program sets the links into a random bit sequence mode that generates 10^{12} bits through the link. The established confidence level for this test is no greater than 1 bit error per 10^{12} bits.

3. RESULTS & ANALYSIS

3.1 Voltage, Current, & Temperature Tests Results & Analysis

Before proceeding to present the results of the physical tests that were conducted, the absolute specifications of the hardware components of the X2O must be understood. These conditions are defined by the manufacturers of the devices involved, and are cited to be the minimum and maximum values of voltage, current, and temperature that damage the components. These parts typically have built-in safety mechanisms that prevent them from reaching these conditions. However, the results of the physical tests should not approach near these values. Table 1 presents these absolute specifications for the allowed voltage and temperature limits for the safe and reliable operation of the FPGA.

Table 1: *Absolute specifications of the FPGA allowed temperatures and power rail voltages in the X2O board.*

Power Rail	Regulator	Max. Temperature (°C)	Max. Supply Current (A)	Min. Voltage (V)	Max. Voltage (V)
FPGA VCCINT	LTM4700 (x3)	100	100	0.825	0.876
MGTAVCC North	LTM4626 (x2)	100	12	0.873	0.927
MGTAVCC South	LTM4626 (x2)	100	12	0.873	0.927
MGTAVTT North	LTM4626 (x2)	100	12	1.164	1.236
MGTAVTT South	LTM4626 (x2)	100	12	1.164	1.236
VCCAUX	MAX8556	100	4	1.746	1.854
MGTVCCAUX North	TPS7A92	100	2	1.746	1.854
MGTVCCAUX South	TPS7A93	100	2	1.746	1.854
Intermediate Rail	LTM4626	100	12	-	-

It is required that the regulator chips of the FPGA power rails do not violate these voltage limits. This is what is tested in the physical tests of this project. The non-FPGA related power rails also have unique absolute specifications, and Table 2 displays the minimum and maximum allowed voltage and temperature limits for the safe and reliable operation of the non-FPGA devices.

Table 2: *Absolute specifications of the non-FPGA allowed temperatures and power rail voltages in the X2O board.*

Power Rail	Regulator	Destination Chip	Max. Temperature (°C)	Min. Voltage (V)	Max. Voltage (V)
Oscillators Northeast	TPS7A92	SG3225VEN	85	2.375	2.625
Oscillators Northwest	TPS7A92	SG3225VEN	85	2.375	2.625
Oscillators Southeast	TPS7A92	SG3225VEN	85	2.375	2.625
Oscillators Southwest	TPS7A92	SG3225VEN	85	2.375	2.625

The data collected from the physical tests were completely within the absolute specifications, with none of the devices approaching near any dangerous conditions. However, these specifications in and of itself are not purposeful regarding the objectives of this project. The data was analyzed in order to establish typical or expected values and define normal operating conditions that represent the minimum and maximum values of the typical results of the physical tests. Before further analysis of the data is shown, two general categories of hardware devices will be distinguished.

3.1.1 Power Supplying Devices

On the side of power supply, the critical measurable conditions are typically temperature and current. The regulator chips associated with each power rail can only withstand providing up to a certain current. Similarly, the internal and external operating temperatures should not exceed specific values in order to proceed with any X2O testing.

All the results of the physical test on the critical power supplying variables were well within absolute specifications. Furthermore, consistent results over multiple trials were observed. The testing conditions listed in the methods section of a consistent level 5 fan speed as well as 0 optical transceivers were maintained. From the data, the expected or normal operating conditions are defined in the following manner. The plots in Figure 5 display the internal temperatures of the regulators of the MGTAVCC South power rail and the MGTAVTT North power rail over several trials.

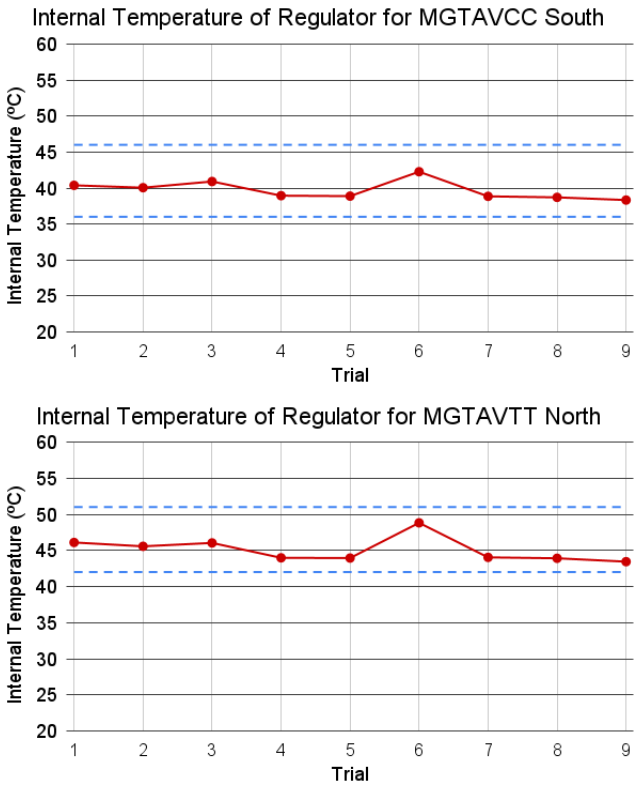

Figure 5: *Plots of internal temperatures of the MGTAVCC South and MGTAVTT North power regulators with no optical transceivers installed into the X2O.*

As the data suggests, it is evident that the temperature fluctuation is minimal. The normal operating conditions are defined to be within approximately 10% of the average temperature values for each. These values are represented by the blue lines shown in Figure 5. The normal operating conditions for the regulator chip of the MGTAVTT N are defined to be between 42ºC and 51ºC. Similarly, the MGTAVCC S regulator normal operating temperatures are defined to be between 36ºC and 46ºC. These ranges should be seen as the expected ranges of measurements achieved by running the physical tests on the X2O board. Results that are found to be outside of these ranges would indicate that there is something out of the ordinary within the conditions of the X2O. In that case, there should be some investigation into finding the cause of this deviation from expectation. This process is repeated for each of the categories listed in Table 1 and Table 2.

3.1.2 *Power Destination Devices*

The devices that are receiving the power provided by the voltage regulators are generally concerned with the voltage values. This is the critical measurement because out of range values may result in a systematic hardware failure. In Table 2, the oscillator power rails consist of (for the purposes of this explanation) regulator chips that are responsible for providing the power, and destination chips that receive this power. The following subsection will display the analysis of the data keeping in mind the critical measurements for both the power supplying and power using devices.

3.1.3 *Normal Operating Conditions*

After analysis of the data, it was evident that the measurable values were overall consistent. Table 3 displays the normal operating conditions that were established after the analysis of the voltage, current. and temperature data of the FPGA related devices and power rail voltages.

Table 3: *Normal operating conditions of the FPGA temperatures and power rail voltages in the X2O board.*

Power Rail	Regulator	Min. Temperature (°C)	Max. Temperature (°C)	Supply Current (A)	Min. Voltage (V)	Typical Voltage (V)	Max. Voltage (V)
FPGA VCCINT	LTM4700 (x3)	-	-	-	-	-	-
MGTAVCC North	LTM4626 (x2)	-	-	0.152	0.89	0.895	0.9
MGTAVCC South	LTM4626 (x2)	36	46	0.155	0.89	0.898	0.91
MGTAVTT North	LTM4626 (x2)	42	51	0.364	1.1942	1.1943	1.1944
MGTAVTT South	LTM4626 (x2)	35	46	0.374	1.196	1.197	1.198
VCCAUX	MAX8556	-	-	1.273	1.796	1.797	1.799
MGTVCCAUX North	TPS7A92	-	-	-	1.8138	1.8142	1.8144
MGTVCCAUX South	TPS7A93	-	-	-	1.817	1.8188	1.8194
Intermediate Rail	LTM4626	53	63	0.55	-	2.634	-

Table 3 is analogous to Table 1, however it displays the expected normal operating values of FPGA related regulator chips after analyzing the trends in the collected data rather than the absolute failure specifications. Table 4 displays the normal operating conditions determined after analysis of the physical data for the non-FPGA related power rail chips.

Table 4: *Normal operating conditions of the non-FPGA temperatures and power rail voltages in the X2O board.*

Power Rail	Regulator	Destination Chip	Max. Temperature (°C)	Min. Voltage (V)	Typical Voltage (V)	Max. Voltage (V)
Oscillators Northeast	TPS7A92	SG3225VEN	-	2.504	2.505	2.506
Oscillators Northwest	TPS7A92	SG3225VEN	-	2.5162	2.5163	2.5164
Oscillators Southeast	TPS7A92	SG3225VEN	-	-	-	-
Oscillators Southwest	TPS7A92	SG3225VEN	-	2.512	2.513	2.514

There are some missing values in Figures 7 and 8. This is due to the physical test program not being comprehensive and certain devices are not read by the physical test program. For example, the VCCINT power supplying regulators were found to have nonsensical values for their temperatures. The temperatures were measured to be above 90,000ºC. Due to this program related misreading, the test simply displayed no values for the these qualities. Also, it is important to emphasize that the results displayed are for an incomplete prototype of the X2O board. As a result, there were a few power rail voltages that are not present on the board. Due to this, the script was written to exclude these measurements. Furthermore, no temperatures were displayed for the oscillator chips. The oscillator chips typically do not get too hot, and there are no built-in temperature sensors. Not every voltage has an associated temperature. Despite these errors, the temperature, current, and voltage data that actually were collected were all found to be consistent for both the power supplying and power consuming devices.

The testing of this prototype with 0 optical transceivers and a fan speed set to level 5 provided data that suggested these operating conditions should be expected. However, the results of actual testing of complete X2O boards under different conditions would not fall under these expectations. As mentioned previously, the number of optical transceivers and X2O boards plugged into the ATCA crate will raise the temperatures that the devices are running at.

The data collected from the testing involving 30 QSFP+ optical transceivers and a fan speed level of 6 will be presented now.

Figure 6 plots the optical transceiver temperature measurements collected for each channel as a function of time at a fan speed of 6. The time represents the number of minutes passed

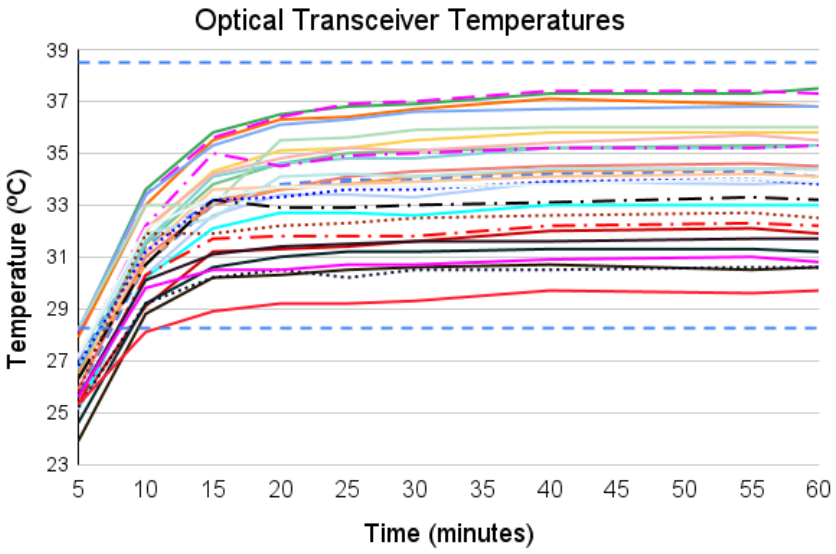

Figure 6: *Temperature (ºC) of each optical transceiver as a function of time in terms of minutes after the main FPGA is powered on with 30 QSFPs installed into the X2O.*

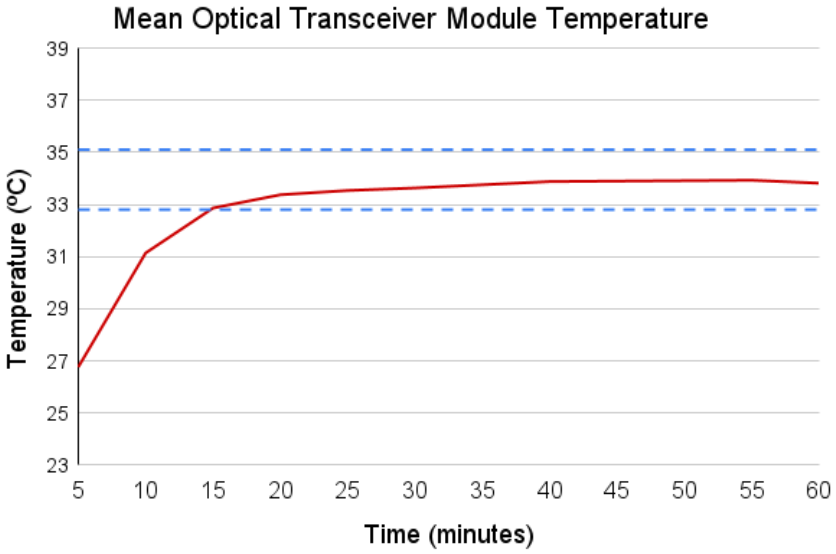

Figure 7: *Mean temperature (ºC) of optical transceiver module as a function of time in terms of minutes after the main FPGA is powered on with 30 QSFPs installed in the X2O.*

after the FPGA was powered on and is included to display the temperature increase and stabilization period. The blue dashed lines in Figure 6 represent the minimum and maximum temperatures that define the normal operating conditions for any given channel at the stable temperatures.

The conditions are the minimum temperature at 28.25ºC and the maximum at 38.5ºC. Figure 7 plots the average QSFP temperatures across all channels from the data displayed in Figure 6 over the same time period. The normal operating condition for the mean QSFP temperature at the stable temperatures is defined as 32.8ºC at a minimum and 35.1ºC at a maximum. These limits are represented as the blue dashed lines in Figure 7.

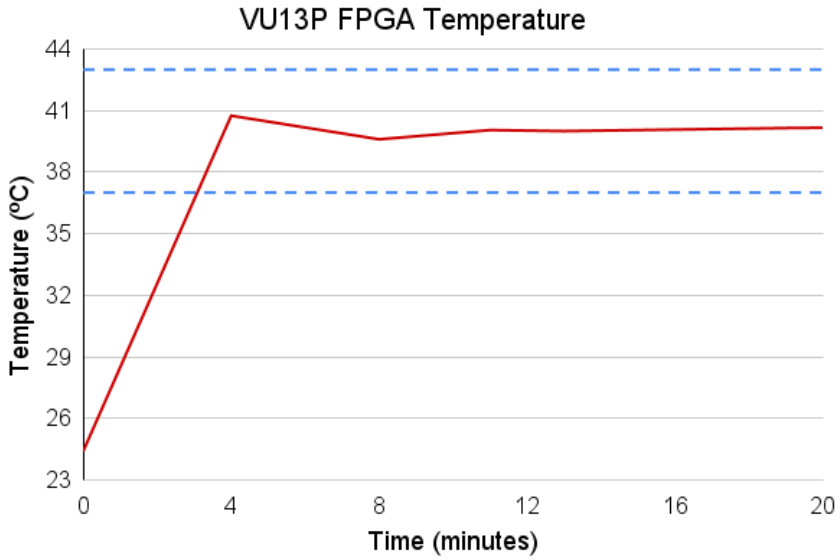

Figure 8: *Temperature (ºC) of the main FPGA as a function of time in terms of minutes after the main FPGA is powered on with 30 QSFPs installed in the X2O.*

The main FPGA temperature measurements are presented in Figure 8. Through analysis of the stabilized temperature, it was determined that the normal operating temperature range for the main FPGA is 37ºC to 43ºC with 30 QSFP+ optical transceivers at a fan level of 6.

The intermediate rail in the X2O board is typically the hottest rail. Figure 9 displays the temperature observed for this component as time passes after the FPGA was powered on.

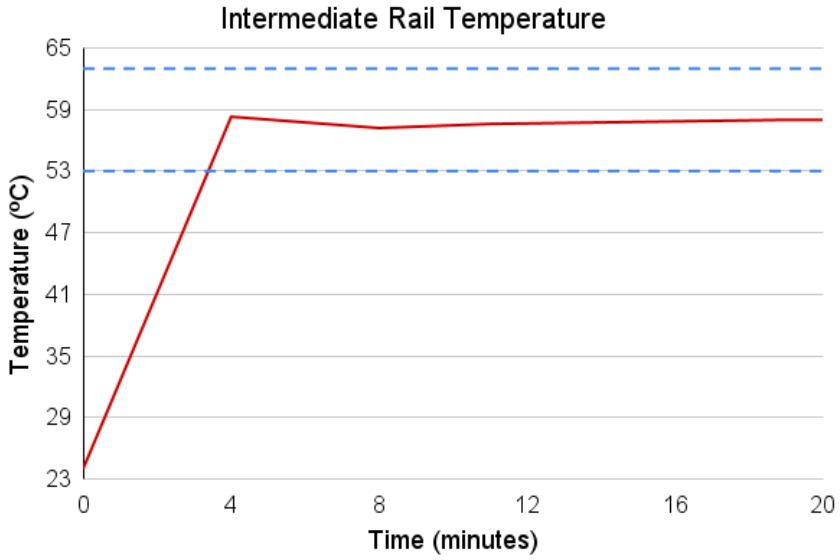

Figure 9: *Temperature (ºC) of the intermediate rail as a function of time in terms of minutes after the main FPGA is powered on with 30 QSFPs installed into the X2O.*

Through analysis of the stabilized temperature in Figure 9, it was determined that the normal operating temperature range for the intermediate rail is 53ºC to 63ºC with 30 QSFP+ optical transceivers at a fan level of 6.

For comparison, temperature data from the MGTAVTT N and MGTAVCC S power regulators with 30 QSFPs installed into the X2O board and a fan level of 6 was collected.

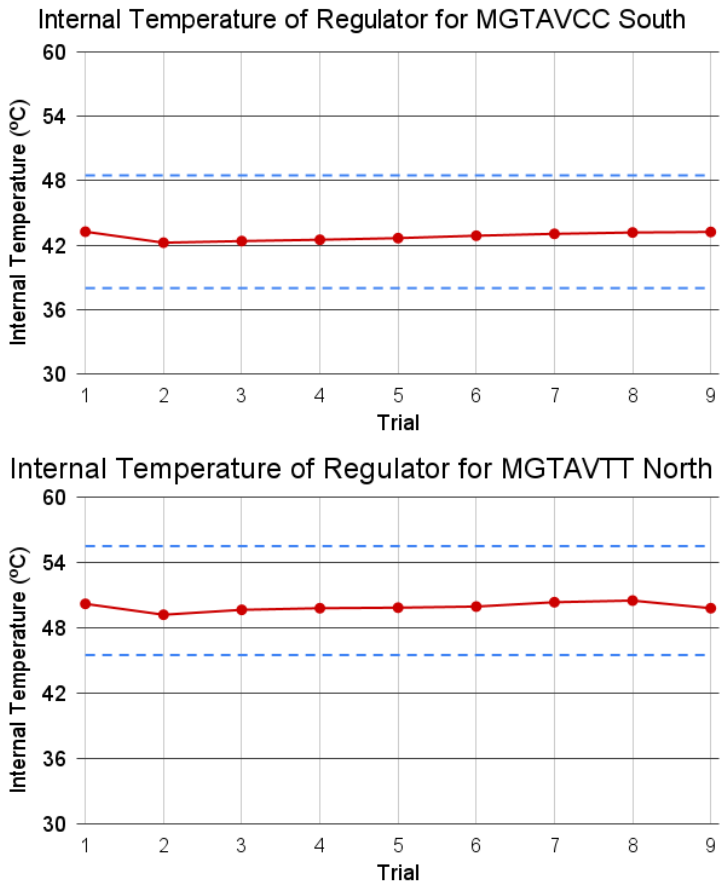

Figure 10: *Plots of internal temperatures of the MGTAVCC South and MGTAVTT North power regulators with 30 optical transceivers installed into the X2O.*

The normal operating conditions are represented by the dashed blue lines shown in Figure 10. With 30 QSFPs installed and a fan level of 6, the normal operating conditions for the regulator chip of the MGTAVTT N are defined to be between 45.5ºC and 55.5ºC. Similarly, the MGTAVCC S regulator normal operating temperatures are defined to be between 38ºC and 48.5ºC. As expected, these ranges are shifted a few degrees higher relative to the previous results for these regulators due to the optical transceivers drawing power and heating up the board.

3.2 FPGA Programmability Tests Results & Analysis

The methods chapter in the FPGA programmability section explained that the testing consisted of multiple runs of using the program 500 times. It is also important to keep in mind that

the result of this test is simply the number of times the communication has passed, as well as displaying the number of cycles executed for comparison. The procedure explained previously refers to using CSC firmware, however this is not a necessity; any firmware may be used. The programmability testing that was conducted used various firmware configurations to observe variations in the results across firmware.

Extremely consistent results were observed from these tests. The program tests the chip to chip connectivity. As explained previously, the test executes this communication validation 10 times, and this test was run 500 times. Of all of these runs, none of the tests resulted in an FPGA programmability failure. Similarly, there were no significant failures in the same tests due to varying the firmware, which further validates the results.

3.3 Clock Tests Results & Analysis

The reference clock tests displayed very consistent results. The frequency measurements for the 30 oscillators were collected and expressed in parts per million relative to the expected value of 156.25 MHz. As mentioned previously, the frequency tolerance for the clocks is ± 25 parts per million. The following histogram plots the PPM occurrence distribution of frequency measurements for the oscillators on this prototype X2O board.

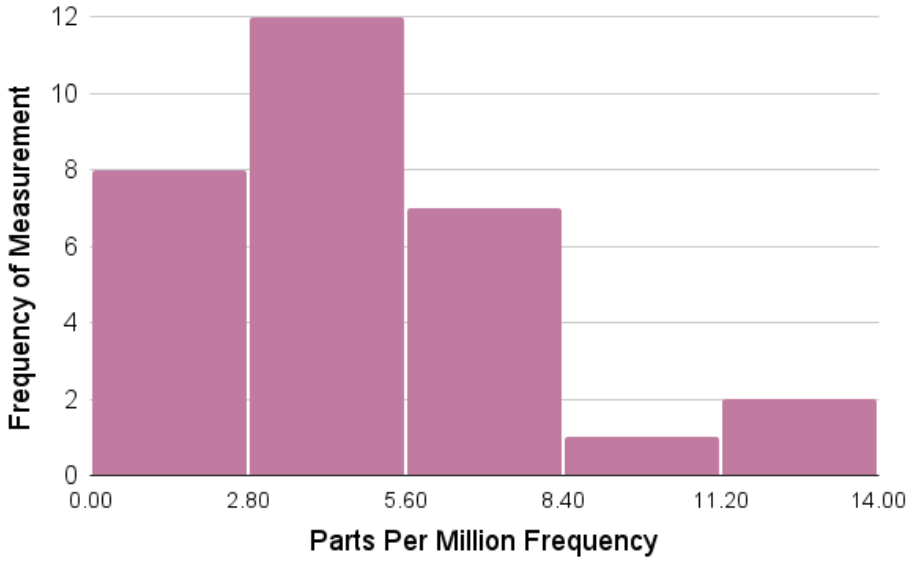

Figure 11: *Histogram of the occurrence of measured clock frequencies in part per million.*

As Figure 11 displays, all the frequency measurements were well within the 25 PPM tolerance given by the manufacturer. Furthermore, the majority of the frequency measurements were within 10 PPM. The results indicate that by using the standardized testing conditions explained previously, future testing results for complete X2O boards should emulate the 10 PPM expectation for the frequencies of the clocks on this X2O prototype.

3.4 High-Speed Communication Tests Results & Analysis

The results of the high-speed communication tests were consistent. All the links passed the bit error tests as they all produced less than 2 errors. Furthermore, the results of the link connectivity part of the test displayed that almost all the links were functional. The channels were put in loop-back mode by the software. The links between two channels were tested individually, then the test was repeated for the next two channels until all the links are tested. There were issues with the link between cages 2 and 3. This is because cage 3 on the X2O is faulty. This along with the bit error results mean high-speed communication is functional between all but cages 2 and 3. The functionality of cage 3 will be explored further in future projects.

4. CONCLUSION

The upgrades to the backend electronics system with the X2O for the CMS muon trigger at the Large Hadron Collider is critical to the future successes of high energy physics research. The LHC is expected to observe collisions at a significantly increased rate due to the coming upgrades of the High-luminosity LHC. Handling the increased data rate resulting from the higher energy collisions is paramount for making full use of the LHC data. The data collected from testing of the prototype X2O board at the Texas A&M CMS electronics lab using these newly created procedures are presented in detail in this paper. The hardware diagnostics procedures outlined in this paper provide a user manual for testing the operating conditions of the hardware components of newly produced X2O boards and ensuring these conditions meet the required specifications. It is also a useful reference for expected results of the tests outlined in this paper. It is essential to have confidence in the functionality of the optimized electronics boards that will be produced in the future. The diagnostic tools and procedures presented in this paper also provides confidence in any future testing with such boards through comparison with the normal operating conditions determined by the analysis of the results displayed in this project.

4.1 Future Research

This paper contributes to the field of particle physics by providing detailed hardware diagnostics procedures for validating the performance of the upgraded electronics and ensuring they meet the required specifications. The data collected from the X2O board at the Texas A&M CMS electronics lab provides valuable insights into the functionality and quality control testing of the upgraded electronics, which can be used to inform future research and development efforts. Overall, this paper is an essential resource for researchers and engineers working on the CMS muon trigger at the Large Hadron Collider, providing a roadmap for testing and validating the performance of the upgraded backend electronics board.

The tests used in this project is by no means comprehensive for the X2O board, and the

complexities of the hardware can be tested to immense detail. However, more general testing can and will be accomplished using this prototype X2O board here at TAMU. The existing testing setup has great potential to harbor additional research that can be very useful.

In summary, this project's contribution to the CMS muon system is its provision of clear and well-defined hardware diagnostics procedures that can be used to validate the performance of the upgraded backend electronics board (X2O) for the CMS muon trigger at the LHC. The diagnostic procedures presented in this paper will provide a crucial framework for future research and development of the High-Luminosity LHC project and will help ensure the continued success of the world's largest particle accelerator.

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