DESIGN TECHNIQUES FOR HIGH-SPEED MULTI-CARRIER WIRELINE

RECEIVERS

A Dissertation

by

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ABSTRACT

The explosion in network traffic driven by cloud computing and wireless data usage necessitates serial I/O operate at higher data rates. The per-channel I/O data rate is projected over 100Gb/s due to packaging technology allowing only modest increases in I/O channel number. As the high-speed data symbol times shrink, this results in an increased amount of inter symbol interference (ISI) for transmission over both severe low-pass electrical channels and dispersive optical channels. This necessitates increased equalization complexity, consideration of more bandwidth-efficient modulation schemes, such as baseband PAM4 and coherent QAM, and the use of forward error correction. Serial links that utilize an analog-to-digital converter (ADC) receiver front-end offer a potential solution, as they enable more powerful and flexible digital signal processing (DSP) for equalization and symbol detection and can easily support advanced modulation schemes. Moreover, the DSP back-end provides robustness to process, voltage, and temperature variations, and benefits from improved area and power with CMOS technology scaling. However, with the data-rate increasing to 100+ GS/s, the front-end ADC for PAM 4 modulation requires 50G+ GS/s sample rate, and high input bandwidth is essential for less induced ISI. Power consumption of such high-speed ADC is a major problem. This motivates the exploration of energy-efficient high-speed and high-bandwidth time-interleaved ADC design. In addition to this, sampling clock jitter places fundamental performance limitations on common time-interleaved ADC architectures,

necessitating clock generation and distribution circuitry that achieve rms jitter of a few hundred of femtoseconds.

This dissertation presents three researches. The first work presents a 1.5GS/s 8-bit unit pipeline-SAR ADC on 14nm with output level shifting techniques that significantly reduce the unit-ADC power and maintain the high-speed. The unit-ADC operates with a 0.8V supply, consumes 2.4mW power, and achieves16.7fJ/conv.-step FOM at Nyquist. The second research presents a high-speed time-interleaved ADC, proposed a speed-enhanced bootstrapped switch that enable a low-power and high bandwidth interleaver. A 7-bit 38GS/s ADC 22nm prototype achieves 41.9fj/conv.-step at low frequency, 64.1fj/conv.-step at Nyquist, and has a 20GHz 3dB bandwidth. The third research is a novel frequency domain multi-carrier ADC-based receiver front-end. The multi-carrier technique significantly improves jitter robustness and reduce the conversion speed of front-end ADC as well as the DSP complexity. A 40Gb/s receiver frontend 22nm prototype can operate with the highest 1.6psrms jitter and achieves 3.05pJ/bit power efficiency

DEDICATION

For the memory of my father

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CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supervised by dissertation committee consisting of Professor Samuel Palermo [advisor], Professor Sebastian Hoyos [co-advisor] and Professor Jun Zou of the Department of electrical and computer engineering and Professor Duncan M. (Hank) Walker of the Department of computer science and engineering.

The multi-carrier techniques depicted in Chapter 2.2 was provided by Professor Sebastian Hoyos.

All other work conducted for the dissertation was completed by the student independently.

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1. INTRODUCTION

The explosion in cloud computing application, IOT, and wireless data usage has created dramatic growth in data center traffic. This motivates the serial links that perform the communication between ICs in these systems must operate at higher speed. In order to alleviate the significant frequency dependent attenuation encountered on these legacy channels, PAM-4 signaling is a common choice of modulation format because of the PAM-4 Nyquist frequency is just half of PAM-2. Many designs [1-5] employ ADC based receiver architectures for PAM-4 links to take advantage of process scaling and process, voltage and temperature (PVT) robustness of the CMOS process in the DSP. The more powerful equalization techniques that lend themselves to easier digital implementations extend the amount of insertion loss that the receiver can handle in comparison to mixed signal implementations. Despite these advantages, ADC-based serial links are generally more complex and consume more power than mixed signal serial links due to the conventional SAR-based time-interleaved ADC and DSP that employs large amount taps of FFE and DFE.

The converters that utilized in the ADC-based front-end employ a large amount of time-interleaved unit-ADC channels to achieve the required high effective sampling rates. Sampling in these ADCs is typically performed in several ranks with multiple clock phases per rank and generating these clocks with the required accuracy and jitter performance is a major challenge. Another major issue is maintaining the required signal bandwidth as the interleaving factor is increased. This motivates the development of high-speed low-

power unit ADCs that can reduce the interleaving factor for a given effective sampling rate, resulting in smaller area and an overall simpler design.

In ADC-based links, most of the front-end time-interleaved ADCs were not intended for achieving analog 3dB bandwidth up to Nyquist [12]. The analog bandwidth is less relevant than SNDR at high frequencies in previous researches, the FIR filter is utilized to equalize amplitude degradation. However extra FIR taps for the ADC bandwidth equalization requires more DSP power, this motivates the innovations for low-power and high-bandwidth ADC interleaver design.

Moreover, as the wireline communication data rates climb over 100Gb/s, the bit period shrinks to dozens of picoseconds and the high-speed time-interleaved ADC performance is limited by the jitter barrier. This necessitates that clock generation and distribution circuitry that achieve rms jitter of a few hundred femtoseconds. Despite there are some researches regarding over 100Gb/s baseband PAM-4 ADC-based receiver, their jitter tolerance are limited to around one hundred femtosecond and a power-hungry low jitter clock circuitry are necessary. This motivates the innovations on the ADC-based receiver architecture for jitter robustness.

In order to address the previous mention challenges in ADC-based receiver design, this dissertation is organized as follows:

Chapter 2 introduces the background material of the high-speed wireline link technique, including the ADC-based receiver architecture, high-speed time-interleaved ADC architecture, and the challenges for the 100+GS/s receiver design. It also presents multi-carrier technique and a frequency-domain ADC-based receiver architecture. And

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the digital equalization techniques for the frequency-domain ADC-based receiver are briefly described.

Chapter 3 presents a single channel 1.5GS/s 8-bit pipelined-SAR ADC that utilizes a novel output level shifting (OLS) settling technique to enable low-voltage operation of the dynamic residue amplifier with low hardware overhead. A detailed discussion of the proposed OLS settling technique that allows for an inter-stage gain of ~4 with a settling time that is only 28% of a conventional CML amplifier is introduced. Implementation details asynchronous ADC architecture and key circuit blocks as well as experiment results are covered.

Chapter 4 presents a 7-bit, 38 GS/s, 32-way Time-Interleaved ADC, which utilizes a high-bandwidth 8-way interleaver architecture based on a proposed speed enhanced bootstrapped switch, which shows higher operation speed and better EBON with high frequency input. Design details of the 38GS/s ADC and the innovative speed-enhanced bootstrapped for high-bandwidth are covered and measurement results of both ADC SNDR and bandwidth are shown to verify the effectiveness of the proposed time-interleaved ADC architecture

Chapter 5 presents a novel jitter-robust 40Gb/s wireline ADC-based receiver front-end (RXFE) architecture that supports multicarrier signaling to provide a ~3X relaxation in clock jitter requirements. The multicarrier signal is formed by three bands to support a total 40Gb/s data rate. This includes baseband (BB) PAM4 operating at 4GS/s and mid-band (MB) and high-band (HB) that both carry 4GS/s QAM16 on 4GHz and 8GHz orthogonal carriers, respectively. System level simulation, receiver architecture, analog

front-end circuit, clock generation with jitter injection and time-interleaved ADC design, along with the experiment results are presented.

Chapter 5 summarize the three works and concludes the dissertation. In addition, this chapter recommends a time domain ADC architecture for further improve the high-speed ADC design. It also presents a frequency domain multi-carrier TX architecture that can work with the proposed muti-carried RX front-end.

2. BACKGROUND[*]

This chapter briefly introduces the background of the high-speed wireline link technique, including the ADC-based receiver architecture, high-speed time-interleaved ADC architecture, and the challenges for the 100+GS/s receiver design. Then the multi-carrier technique and a frequency-domain ADC-based receiver architecture are present in detail, mainly focus on the jitter tolerance performance advantage compare with the traditional base-band ADC-based receiver. Finally, the digital equalization techniques for the frequency-domain ADC-based receiver are briefly described.

2.1. High-speed wireline link

The bandwidth of wireline link is limited by high-frequency loss of electrical traces, reflection from impedance discontinuity and crosstalk between adjacent channels. Fig. 2.1 shows a typical backplane example, which contains IC package, connector, vias and the backplane traces. All the components introduce dispersion and reflection which causes symbols transmitted in different time interval with each other. This is known as inter-symbol interference (ISI) and leads to a big challenge of transmitting high data rates over a bandwidth limited channel.
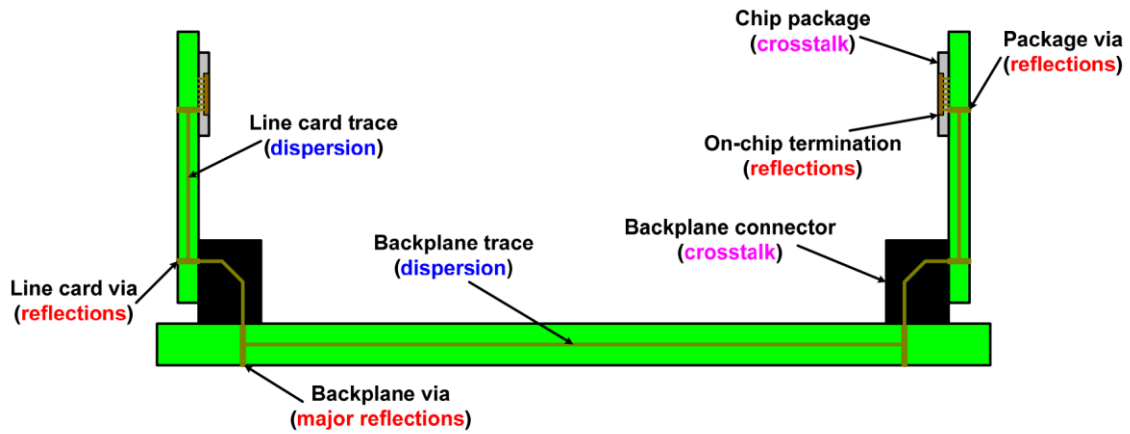
Figure. 2.1: Electrical Backplane channel cross section.
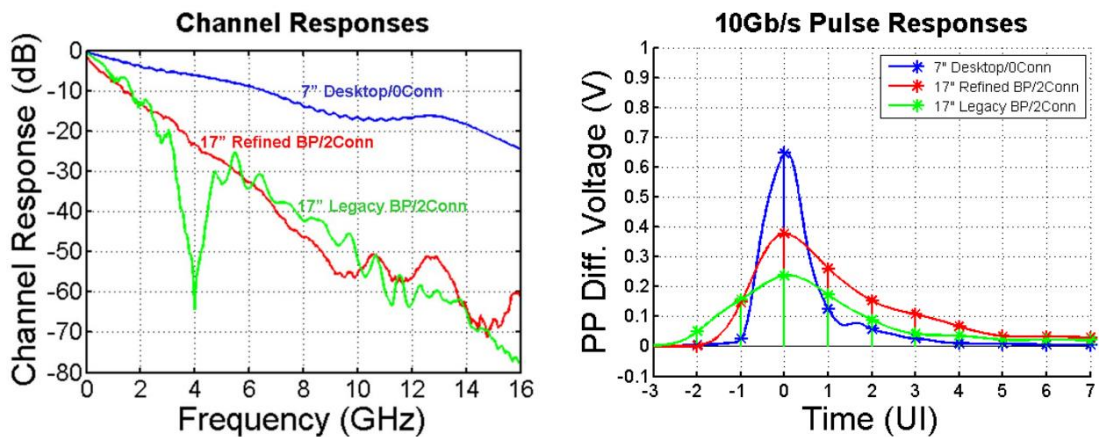
Figure. 2.2: Frequency response and pulse response of three channels.

Fig. 2.2 shows how these frequency-dependent loss terms result in low-pass channels where the attenuation increases with distance. The high-frequency content of pulses sent across these channels is filtered, resulting in an attenuated received pulse with energy that has been dispersed over several bit periods, three example channels with different profiles are present. When transmitting data across the channel, energy from individual bits will now interfere with adjacent bits and make them more difficult to detect. The ISI increases with channel loss and can completely close the received data eye

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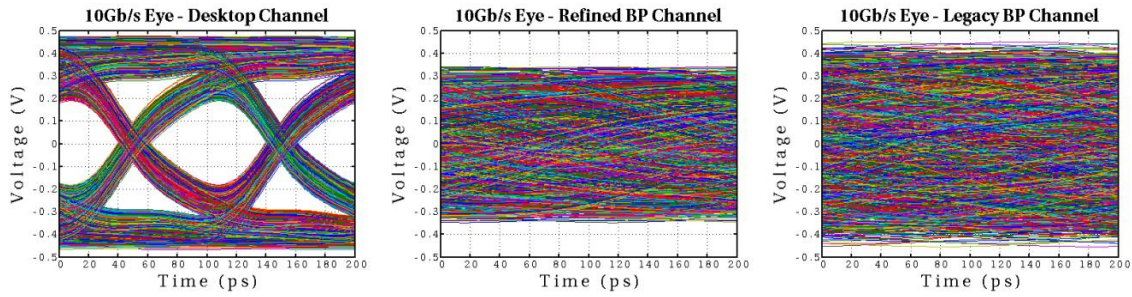
Figure. 2.3: Eye diagrams after channels without eqalization.

diagram, as shown in Fig. 2.3. While the eye is fairly open for the short desktop channel, and a slicer (comparator) with threshold level at zero can detect the received '0' and '1' signals reliably, the eye is completely closed for longer backplane (BP) channels, which causes errors in the detected signal.

2.1.1. Baseband ADC-based receiver architecture

As previously introduced, ISI is the main problem in the wireline communication system to reliable symbol detection at receiver. In order to extend the bandwidth of a given channel, signal equalization techniques are employed to cancel the ISI. The equalization can be implemented on both transmitter side and receiver side. Depending on system data rate requirements relative to channel bandwidth and the severity of potential noise sources, different combinations of transmitter and/or receiver equalization are employed.

Transmit equalization, implemented with a finite impulse response (FIR) filter, is the most common technique used in high-speed links. This TX "pre-emphasis" (or "de-emphasis") filter attempts to invert the channel distortion that a data bit experiences by pre-distorting or shaping the pulse over several bit times. The main advantage of implementing the equalization at the transmitter is that it is generally easier to build high-speed digital-to-analog converters versus receive-side analog-to-digital converters.

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However, because the transmitter is limited in the amount of peak power that it can send across the channel due to driver voltage headroom constraints, the net result is that the low-frequency signal content has been attenuated down to the high-frequency level.

Receiver side equalization can be classified as mixed-signal architectures and ADC-based architectures. Both mixed-signal receivers and ADC-based receivers employ equalization that can be broadly divided into linear equalization and non-linear equalization. Examples of linear equalization are continuous time linear equalizers (CTLE) and discrete time finite impulse response (FIR) equalizers. Examples of non-linear equalizers are decision feedback equalizers (DFE) and maximum-likelihood sequence estimation (MLSE). While mixed-signal receivers mainly employ CTLE and DFE (both FIR and IIR feedback), ADC-based receivers generally employ some analog equalization before the ADC in the form of a CTLE and followed by a powerful linear feedforward equalizer (FFE) and DFE in the digital domain in the DSP.

As the ever-increasing demanding for the I/O data rate climes to 56 Gb/s and scaling beyond 100 Gb/s in the future. The large amount of frequency-dependent loss present in conventional electrical channels makes the use of common two-level pulse amplitude modulation (PAM-2) challenging without significant infrastructure upgrades. This motivates the use of the more spectrally efficient four-level PAM (PAM-4). While PAM-4 has a Nyquist frequency half of PAM-2, it is more sensitive to residual ISI. Thus, mix-signal receiver front ends often employ large tap-count feedforward equalizers (FFEs) that are difficult to robustly implement in the analog domain due to process, voltage, and temperature variations. Fig. 2.4 shows a serial link receiver front end that employs an
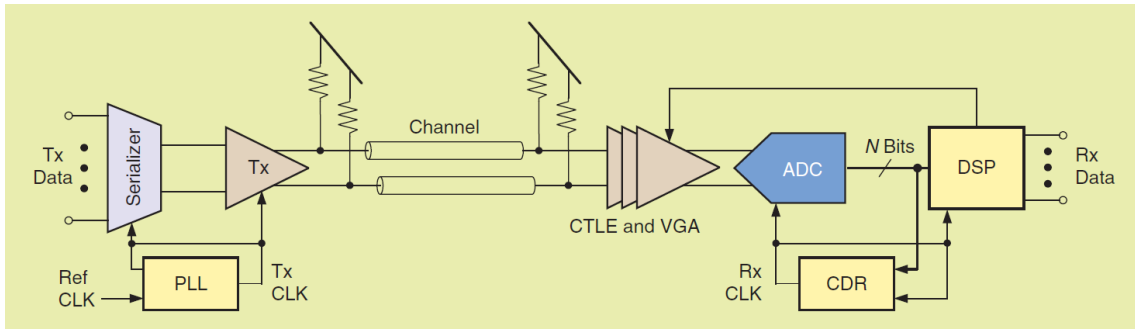
Figure. 2.4: ADC-based receiver architecture.
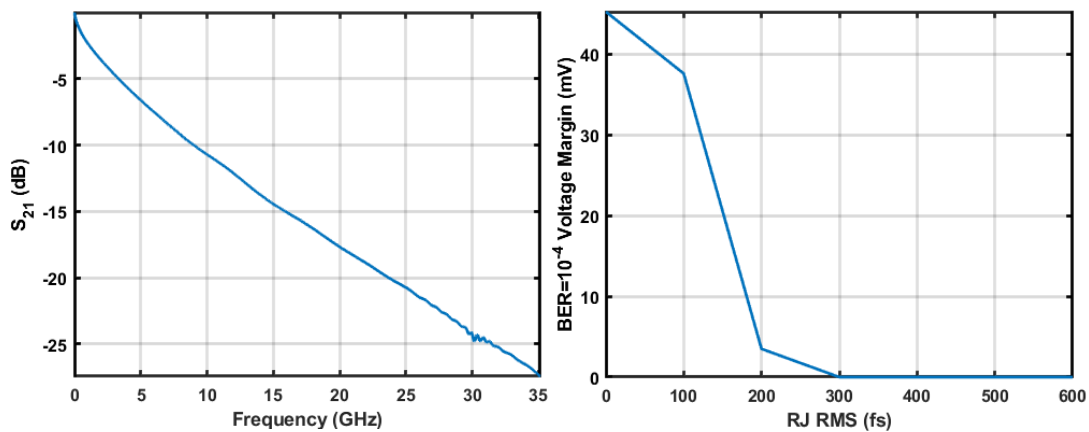
Figure. 2.5: 128 Gb/s ADC-based receiver modeling. Channel, BER vs. Jitter

analog-to-digital converter (ADC) followed by digital signal processing (DSP) to perform ISI cancellation and symbol detection in the digital domain. This ADC-based receiver is well suited for more spectrally efficient modulation schemes, such as PAM-4, and benefits from the improved area and power offered from CMOS scaling.

Unfortunately, sampling clock jitter places fundamental performance limitations on common time-interleaved ADC architectures, necessitating clock generation and distribution circuitry that achieve rms jitter of a few hundred femtoseconds. As shown in Fig. 2.5, for 128Gb/s communication over the channel, the clock needs less than 300fs total rms jitter to achieve acceptable BER assuming forward error correction in the system.
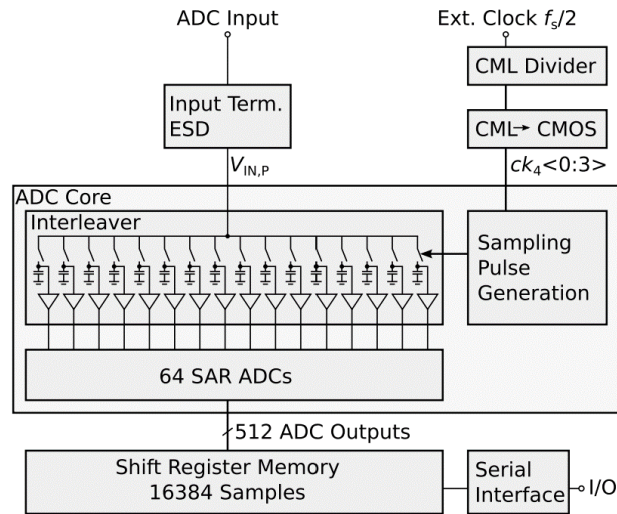
Figure. 2.6: A 64-way time-interleaved ADC example

2.1.2. High-speed ADC architecture and calibration

For the over 20GS/s ADC design, time-interleaved architecture is commonly employed, it combines N-way unit-ADCs that working in a time interleaving manner to achieve N x fs conversion speed. Fig 2.6 show a 64-way time-interleaved ADC example [12]. Most of the time-interleaved ADC designs are intended to have good SNDR at Nyquist instead of achieving 3dB input bandwidth up to Nyquist, since the FIR filter could equalize the high-frequency amplitude degradation. The ADC input connects to 16 parallel sampling switches that sample the input onto sampling capacitors. The sampled voltages are then buffered and forwarded to four sub-ADCs. SAR ADCs are chosen to convert the samples, as their mostly digital architecture is highly suitable for FinFET technologies at low supply voltages, and SAR ADCs have been proven to be power efficient and small in area while operating at more than 1 GS/s [16]. The digital output of the SAR ADCs is connected to a large shift-register-based memory that stores 16384 samples.
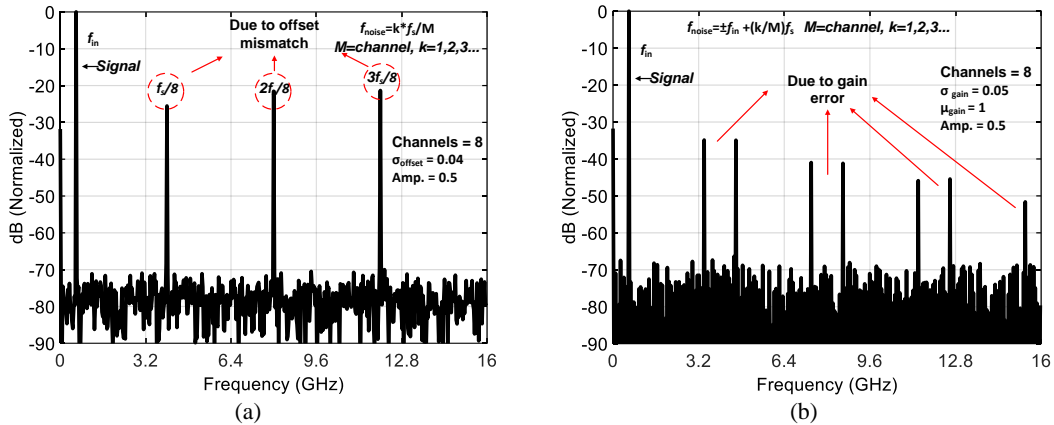
Figure. 2.7: Impact of offset (a) and gain (b) error on ADC output spectrum

While time interleaving enables extremely high sample rate converters, conversion errors occur due to mismatches between the parallel sub-ADCs. These errors appear as spurious peaks in the ADC output spectrum and can significantly degrade SNDR. The magnitude and position of these tones depend on the type of the mismatch, which can be classified as either offset, gain, and timing skew errors. Calibration techniques, both in the analog and digital domains, are employed to correct for these time interleaving errors and achieve acceptable performance.

Channel offset errors occur due to device mismatches in the time-interleaved T/Hs, reference generation circuitry, and comparators. Fig. 2.7(a) shows the impact of offset error on ADC output spectrum for an 8-way TI-ADC model with a $1V_{ppd}$ FSR and offset standard variation of 40mV. Analog domain channel offset calibration could be costly, whereas the offset of each channel could be easily subtracted in digital domain which is more common nowadays. The mismatches can also result in gain errors between each channel. Fig. 2.8 shows the impact of gain errors on ADC output spectrum for an 8-way TI-ADC model with a $1V_{ppd}$ FSR and gain standard variation of 5%. Same as the offset

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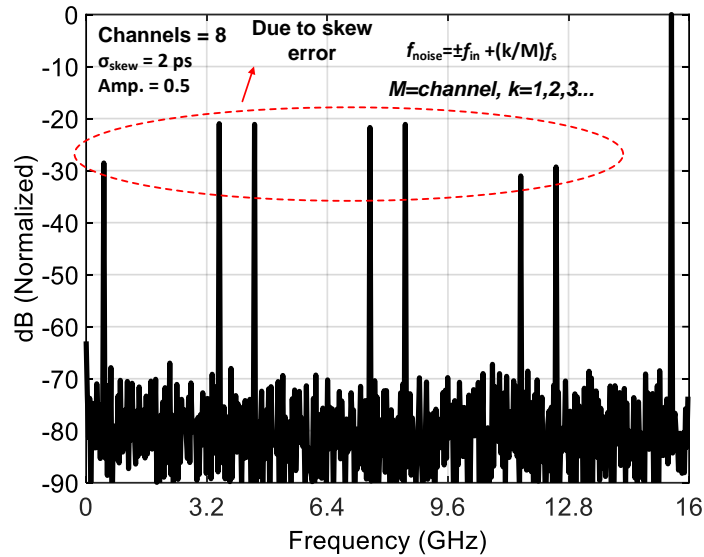
Figure. 2.8: Impact of skew error on ADC output spectrum

error, the gain error is signal independent static error, it could be easily calibrated in digital

domain by multiplying a correction factor with the output of each channel.

Skew errors result from device mismatches and layout asymmetries in the multi-phase clock generation and distribution to the input track-and-holds. Fig. 2.8 shows the impact of gain errors on ADC output spectrum for an 8-way TI-ADC model with a $1V_{ppd}$ FSR and skew standard variation of 2ps. These are most often calibrated with per-phase digitally-adjustable delay cells in the clock distribution buffers [13, 14, 15, 19] or phase interpolators with independent phase offset codes. Skew errors will cause each sub-ADC to generate a pulse response with a slightly different ISI characteristic. Thus, an efficient approach to detect skew errors is to monitor the differences in the converged tap coefficients of a per-slice adaptive equalizer. The delay cell or phase interpolator control can be adjusted to minimize the coefficient differences and calibrate the skew to within the resolution of the correction circuitry. Independent equalizer tap control allows for further fine compensation of residual skew and bandwidth errors.

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2.2. Muti-carrier techniques

Multicarrier communication systems [30] offer several key advantages over single carrier systems including reduced inter-symbol interference because of the narrowband nature of each carrier and much simpler frequency domain equalization consisting of just complex value scaling of the carrier's amplitude and phase estimates. One of the most successful realizations of multicarrier communications systems is orthogonal frequency division multiplexing (OFDM) where the transmitter uses an inverse DFT to transform the frequency block of information bits to the time domain for transmission, and the receiver uses a DFT to estimate the carrier's information. This digital implementation has taken advantage of technology scaling and the advances in low power DAC and ADC needed at the interfaces.

From legacy DSL operating at few Mb/s to WiFi operating at 56Mb/s and most recently serial links operating at 56Gb/s [8] have relied on this technology. While the wireless standards require up-conversion of a complex baseband signal to the allocated frequency band with in-phase and quadrature components simultaneously transmitted, the wireline counterparts do not require up-conversion and therefore realize the transmission of a baseband real-valued signal in which the constellation is mapped. This baseband realization is called discrete multi-tone (DMT). The sampling of multicarrier signals can be accomplished in time-domain at Nyquist rate for a full digital implementation or in a symbol rate fully analog implementation if a correlator bank is used. More interesting, it can be implemented in the frequency domain if filters banks are used. As illustrated in Fig. 2.9 and investigated in [30], sampling multicarrier signals of total duration T in the
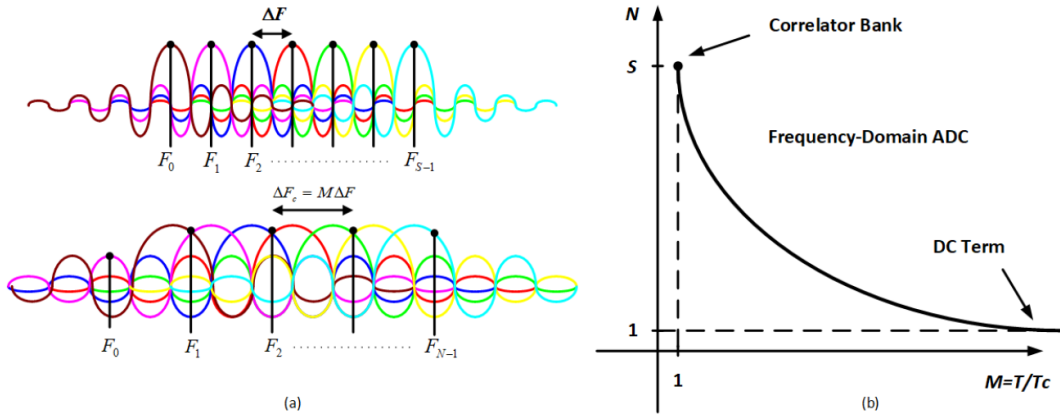
Figure. 2.9: Characteristics of A/D conversion of multicarrier signals in the frequency domain. (a) Effect of time segmentation in the bandwidth of the multicarrier signal and in the samples frequency spacing ΔFc (b) Number of coefficients N versus the symbol-period to segmentation-time ratio ($M = T/Tc$) .

frequency domain introduces a fundamental constraint in the total number of frequency samples (N) versus the number of processing windows (M) and number of carriers (S) given by $N=S/M$. Such constraint produces carrier expansion when the window processing time (Tc) shortens, requiring an adaptive digital baseband that adjusts for changing conditions in the design

2.2.1. Frequency-domain ADC-based receiver

In order to break the jitter barrier that existed in the traditional ADC-based receiver. Fig. 2.10 shows a frequency-domain ADC-based receiver [31]. The input CTLE drives the front-end channels that have a mixer for down-conversion, a Bessel low-pass filter, and an ADC for sampling and digitization. These digitized samples are then processed by the FIR filters in the DSP and their outputs are combined to either perform symbol estimation in PAM-4 baseband mode or to perform both inter-channel interference (ICI) and ISI cancellation in multi-tone mode. This architecture provides several benefits. First,

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Reconfigurable Frequency Domain ADC-Based Receiver
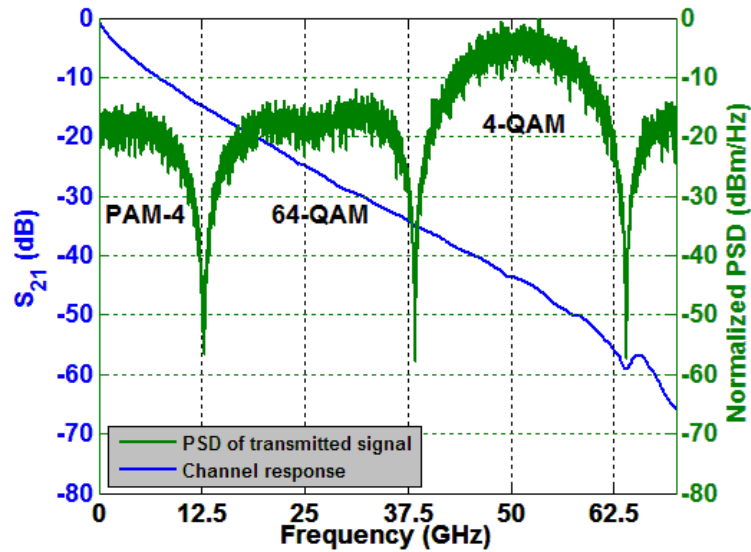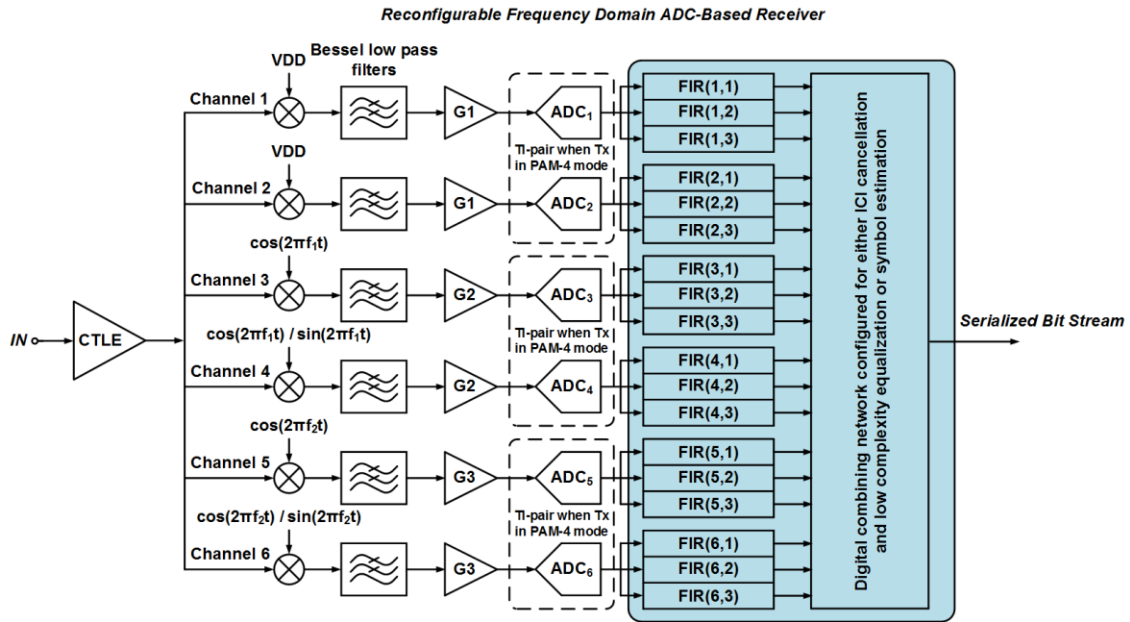
Figure. 2.10: 128 Gb/s ADC-based receiver modeling. Channel, BER vs. Jitter

the mixers perform self-equalization [32] and provide some channel loss compensation, allowing for a reduction in digital equalization complexity. Second, high-frequency noise introduced by the mixers and CTLE is attenuated by the channel filters. Finally, the inclusion of digital receive-side ICI cancellation filters in the 128Gb/s system allows for

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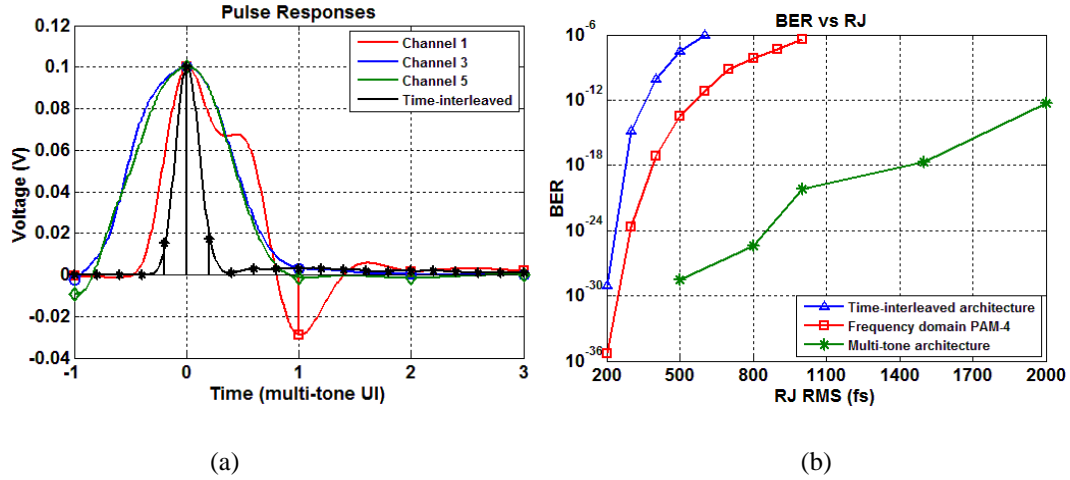
Figure. 2.11: (a) 128Gb/s system pulse responses from a time-interleaved 64GS/s PAM4 system and the proposed frequency-domain receiver in multi-tone mode with the responses from the baseband and I-phase channels shown. (b) BER vs RJ for a time-interleaved receiver and the frequency-domain receiver operating in baseband PAM4 and multi-tone mode.

a 50% improvement in relative channel spacing when compared against a previous 10Gb/s mixed-signal implementation [32].

The receiver channels are configured differently in order to support conventional baseband (PAM2-8) or multi-tone signaling. Assuming a 128Gb/s data rate achieved with baseband 64GS/s PAM4, the receiver is configured as having 3 effective channels with pairs of channels utilizing the same mixer LO frequency. System simulations indicate that a near optimum partitioning has the first effective channel (1/2) processing the low-frequency portion of the signal with a dummy mixer, the second channel (2/4) utilizing a single-phase 1/3-baudrate LO (21.33GHz), and the third channel (5/6) utilizing a single-phase 1/2-baudrate LO (32GHz). The pair of ADCs in each effective channel operates as a 21.33GS/s time-interleaved converter.

An intuitive visualization of the relative jitter robustness of the proposed architecture is shown in the Fig. 2.11(a) pulse responses from a conventional time-interleaved system and the proposed frequency-domain architecture operating in multi-tone mode over a channel with over 30dB loss at 32GHz. Even with an optimized CTLE, the narrow 64GS/s PAM4 pulse response has significant ISI and is more sensitive to timing jitter than the wider 12.8GS/s pulse responses that also experience mixer self-equalization. This is reflected in the BER versus random jitter plot of Fig. 2.11(b). Assuming an equal amount of RJ on both the ADC samplers and the mixer LO clocks, the multi-tone architecture is able to achieve a BER=10-12 with an RJ near 2psrms. This is over 5X the jitter required by the time-interleaved system. In a more conventional PAM4 mode, the frequency-domain receiver still provides a 60% improvement in jitter tolerance.

2.3. Digital equalization techniques for the frequency-domain ADC-based receiver

Operating in a frequency-channelized manner offers the key advantage of processing a longer symbol time, which translates into reduced clock rates for the digital filters. For example, a time-interleaved receiver implementation requires 16 FFE taps and 2 DFE taps effectively operating at the full baud rate in order to support 128Gb/s operation over the channel in Fig. 2.10 with baseband PAM4. Reception of the same baseband PAM4 signal with the frequency-domain receiver offers the advantages of mixer self-equalization and a longer effective symbol time out of the ADC front-end. This allows removal of the DFE taps and the utilization of a digital equalizer with only 16FFE taps that effectively operate at one-third the baud rate.

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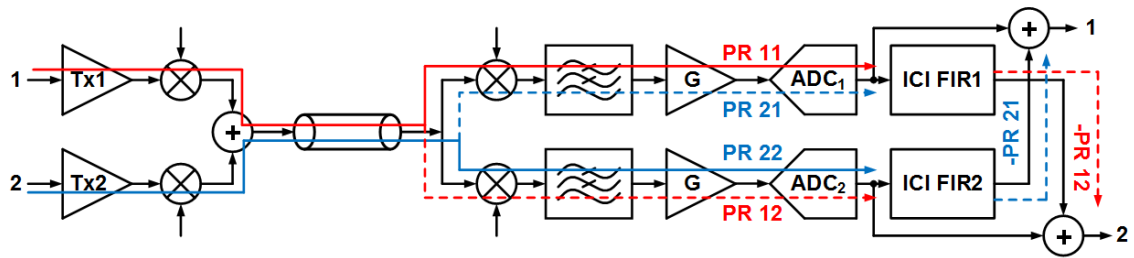
Figure. 2.12: ICI cancellation with digital FIR filters.

Further digital complexity savings are achieved with operation in the 5-channel multi-tone mode, with only 3 FIR taps that effectively operate at one-fifth a comparable PAM4 baud rate required for ISI cancellation. However, in the absence of sharp roll-off filters on the transmitter side, signal energy from one channel will spill over into the adjacent channel and cause inter channel interference in the multi-tone implementation. While ICI can be reduced to an insignificant level by increasing the spacing between the data channels [32], this will cause the highest frequency QAM channel to experience significant attenuation when it passes through the communication channel. As this interference is well modelled as linear time-invariant, the FIR filters are utilized to remove ICI in a manner similar to the ISI cancellation filters.

Fig. 2.12 shows a 2-channel example with the desired channel pulse responses, PR11 and PR22, and the ICI pulse responses, PR12 and PR21. The received signal from the aggressor channel is passed through an ICI FIR filter to produce an interference estimate that is subtracted from the victim channel. In the proposed multi-tone implementation, a total of 8 4-tap ICI FIR filters are necessary to remove adjacent channel interference. Comparing against a time-interleaved PAM4 implementation at the same

effective data rate, and considering both the 3-tap ISI and 4-tap ICI FIR filters, the multi-

tone digital complexity is only 59% of the TI system.

3. A 1.5GS/S 8B PIPELINED-SAR ADC WITH OUTPUT LEVEL SHIFTING SETTLING TECHNIQUE IN 14NM CMOS[*]

This chapter presents a single channel 1.5GS/s 8-bit pipelined-SAR ADC utilizes a novel output level shifting (OLS) settling technique to reduce the power and enable low-voltage operation of the dynamic residue amplifier. The ADC consists of a 4-bit first stage and a 5-bit second stage, with 1-bit redundancy to relax the offset, gain, and settling requirements of the first stage. Employing the OLS technique allows for an inter-stage gain of ~4 from the dynamic residue amplifier with a settling time that is only 28% of a conventional CML amplifier. The ADC's conversion speed is further improved with the use of parallel comparators in the two asynchronous stages. Fabricated in a 14nm FinFET technology, the ADC occupies $0.0013mm^2$ core area and operates with a 0.8V supply. 6.6-bit ENOB is achieved at Nyquist while consuming 2.4mW, resulting in an FOM of 16.7fJ/conv.-step.

3.1. Introduction

As wireline communication data rates climb about 100Gb/s, there is an increased number of receiver front-ends utilizing high-speed analog-to-digital converters (ADCs) that allow for subsequent powerful digital equalization and symbol detection techniques [6]. These converters employ a large amount of time-interleaved unit-ADC channels to

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*Part of this chapter is reprinted with permission from "Y. Zhu et al., "A 1.5GS/s 8b Pipelined-SAR ADC with Output Level Shifting Settling Technique in 14nm CMOS," 2020 IEEE Custom Integrated Circuits Conference (CICC), 2020, pp. 1-4, doi: 10.1109/CICC48029.2020.9075942."

achieve the required high effective sampling rates. Sampling in these ADCs is typically performed in several ranks with multiple clock phases per rank and generating these clocks with the required accuracy and jitter performance is a major challenge. Another major issue is maintaining the required signal bandwidth as the interleaving factor is increased. This motivates the development of high-speed low-power unit ADCs that can reduce the interleaving factor for a given effective sampling rate, resulting in smaller area and an overall simpler design.

Successive-approximation-register (SAR) ADC architectures are popular due to their low comparator count and simple digital logic content, making them suitable for compact and power-efficient mid-resolution time-interleaved ADCs [33]. However, the conversion speed is limited in the most common implementation of the successive approximation algorithm that performs sequential single-bit conversion cycles. As shown in Fig. 3.1, introducing pipelining in the SAR ADC provides improved speed by decreasing the number of conversion cycles per input sampling event. A critical block in this architecture is the amplifier that transfers the residue signal between the two pipeline stages. In high-speed converters, conventional opamp-based amplifiers are not suitable due to the excessive static power required to meet settling time requirements. An alternative approach is to use a dynamic residue amplifier that is only activated once over the entire conversion process [18].
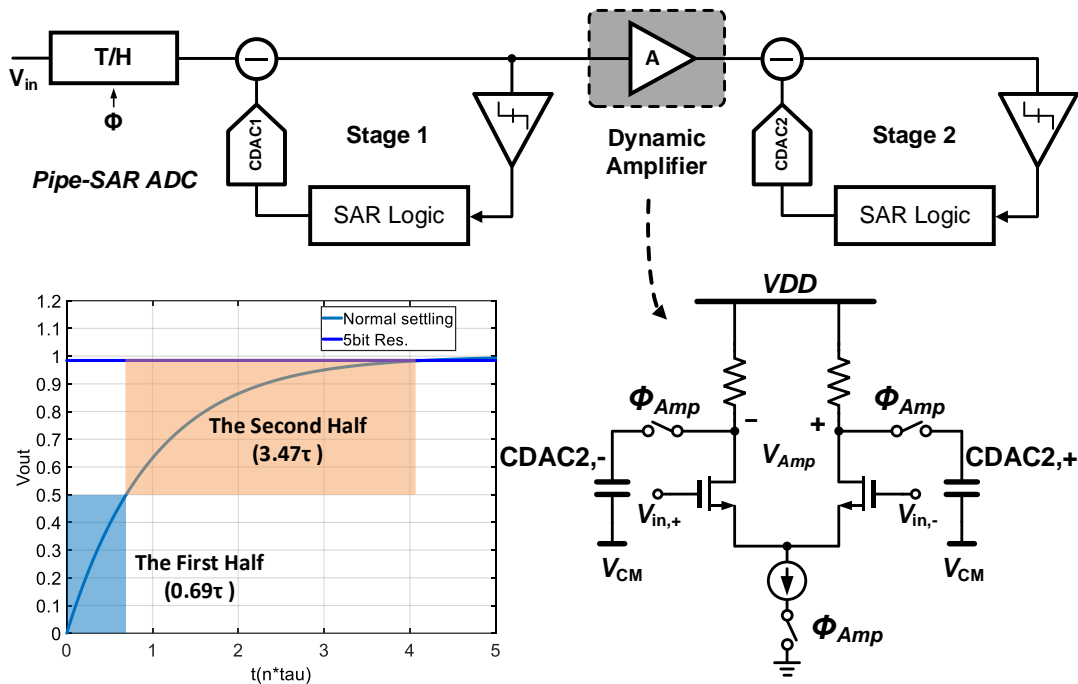
Figure 3.1: Pipeline SAR ADC with a dynamic amplifier.

While dynamic residue amplifiers have the potential to save power, these topologies require a small τ to achieve fast settling times. Satisfying this and maintaining a given gain can result in large dynamic tail current values and increased input transistors that load the first pipeline stage capacitive digital-to-analog converter (CDAC). Given that the smallest CDAC that satisfies the kT/C noise requirement is desired to reduce input buffer power, this loading can cause significant reference attenuation that must be compensated with an increased range reference buffer that is difficult to implement with low supply voltages. Another issue is kickback noise due to the coupling through the large dynamic amplifier input transistors.

This Chapter presents a single channel 1.5GS/s 8-bit pipelined-SAR ADC that utilizes a novel output level shifting (OLS) settling technique to enable low-voltage

operation of the dynamic residue amplifier with low hardware overhead. A detailed discussion of the proposed OLS settling technique that allows for an inter-stage gain of ~4 with a settling time that is only 28% of a conventional CML amplifier is given in Section 3.2. Section 3.3 provides an overview of the asynchronous ADC architecture and key circuit details. Measurement results from a 14nm CMOS FinFET prototype are presented in Section 3.4. Finally, Section 3.5 provides the conclusion.

3.2. Output Level Shifting Settling

While the pipeline-SAR ADC architecture reduces the required settling accuracy of the residue amplifier, it is still challenging to achieve this at high speeds. Upon activation, the Fig. 3.1 conventional dynamic amplifier output will settle as

$$V_{Amp} = A_{CML}V_{in}\left(1 - e^{-\frac{t}{\tau}}\right)$$

Where A_{CML} is the gain. This settles to 50% of the steady state value in a rapid 0.69τ, but requires an additional 3.47τ to settle to the 5-bit accuracy required in the second pipeline stage. The brute force method of reducing this settling time is to reduce the load resistor to decrease τ, but this leads to the aforementioned issues of increased tail current values and large input transistor sizes.

Previously, a OLS technique was developed to reduce errors in feedback amplifiers that occur from finite opamp gain [22]. In that work, an initial estimate of the desired output voltage is sampled on a level shifting capacitor and then this capacitor is switched in series with the opamp output and the feedback amplifier output to improve settling accuracy. This work modifies this technique to dramatically improve the settling time of the open-loop dynamic residue amplifier by utilizing the second pipeline stage CDAC2 as

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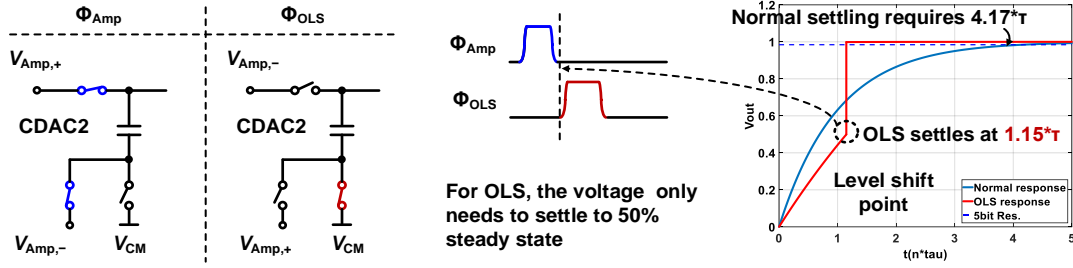
Figure 3.2: Output level shifting technique.

the level shifting capacitor. Fig. 3.2 gives an overview of the proposed OLS settling technique. When Φ_{Amp} is high and the amplifier is activated, the differential output voltage is stored on both sides of CDAC2 by connecting the nominal amplifier output to the top plate and the opposite output to the bottom plate. This Φ_{Amp} duration should nominally match the rapid 50% settling time. After this, Φ_{OLS} is enabled to switch the CDAC2 bottom plate to the common mode. Charge conservation during this phase produces a rapid doubling of the amplifier output signal. Thus, the amplifier output voltage only needs to initially settle to 50% of the steady-state value and the long second half settling is avoided. The significant speed-up offered by the OLS technique is achieved with the low hardware overhead of only one extra bottom-plate CDAC2 switch.

A simplified schematic of the OLS dynamic amplifier, which offers several improvements relative to a conventional CML dynamic amplifier, is shown in the Fig. 3.3. Instead of utilizing a simple resistive-loaded differential pair, this inverter-based amplifier structure provides both PMOS and NMOS transconductance to provide a higher gain of

$$A = (g_{mp} + g_{mn})(r_{on}//r_{op}) \approx 2A_{CML}$$

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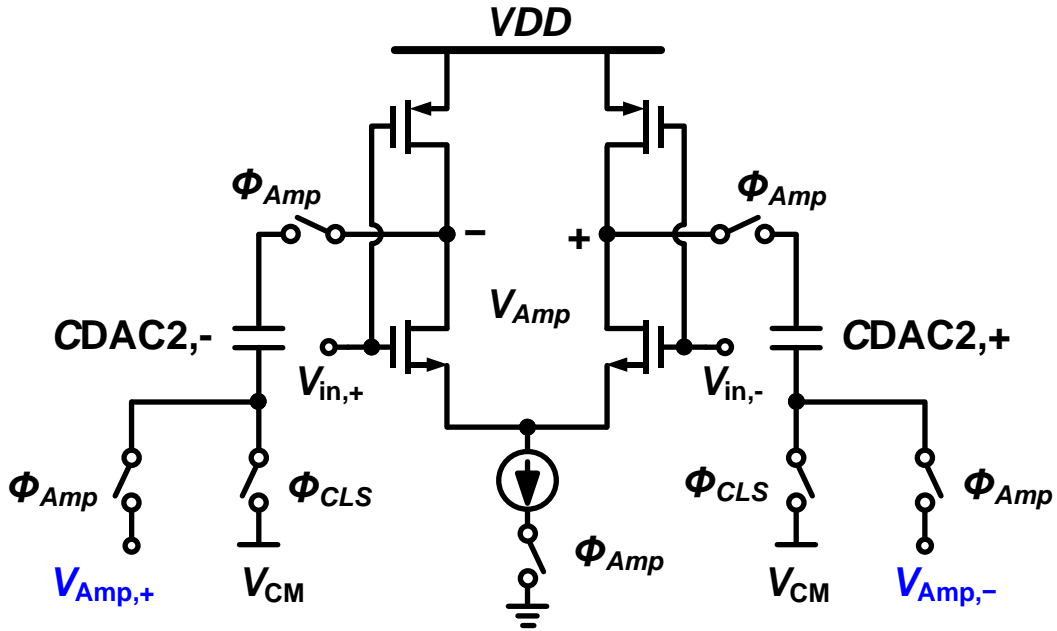
Figure 3.3: Simplified schematic of the OLS dynamic amplifier.

at lower supply voltages. While the amplifier has high impedance outputs, a stable

output common mode is achieved by resetting the CDAC2 top plate to the common mode

prior to activation. One downside of this OLS amplifier is that the equivalent capacitive

loading is 4X larger than the conventional CML amplifier due to both sides of CDAC2

being connected to each amplifier output and each capacitor experiencing Miller

multiplication. Considering this, the time for the OLS amplifier to achieve 50% settling

relative to the original CML amplifier is

$$Av_{in}\left(1 - e^{-\frac{t}{4*\tau}}\right) = 0.5A_{CML}v_{in}$$

$$t = 1.15\tau.$$

Due to the increased amplifier gain, this is only 28% of the 4.17τ required by the

conventional CML amplifier at 5-bit resolution. This also results in lower average power

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due to the dynamic amplifier's reduced activation time. Moreover, the required amplifier's linear output swing range is decreased by a factor of two.

One potential issue with the proposed amplifier is matching the duration of Φ_{Amp} with the 50% settling point. However, high precision is not necessary, as any inaccuracy simply results in a modified gain value that is easily compensated with adjustment of the second stage reference voltages.

The jitter of the Φ_{Amp} pulse is another issue need to be considered. As shown in the Fig. 3.4(a), the Φ_{Amp} jitter causes the timing variance of the level shifting point, and this time domain error further generates the voltage noise at the output. Intuitively, a small settling time constant τ gives very fast transition time which makes the output voltage more sensitive to the timing variance, and the rms value of the jitter determines how much timing error we have. Thus, the noise power is the function of the settling time constant τ and the rms jitter. Quantitatively, the jitter induced voltage noise power could be calculated through the following equation

$$\Delta V \cong \frac{dV}{dt} * \Delta t$$

$$E\{\Delta V^2\} = E\left\{\left(\frac{dV}{dt}\right)^2 * \Delta t^2\right\} = E\left\{\left(\frac{dV}{dt}\right)^2\right\} * E\{\Delta t^2\}$$

$$E\{\Delta V^2\} \cong \left(\frac{0.75}{2 * \tau}\right)^2 * \sigma_t^2$$

26
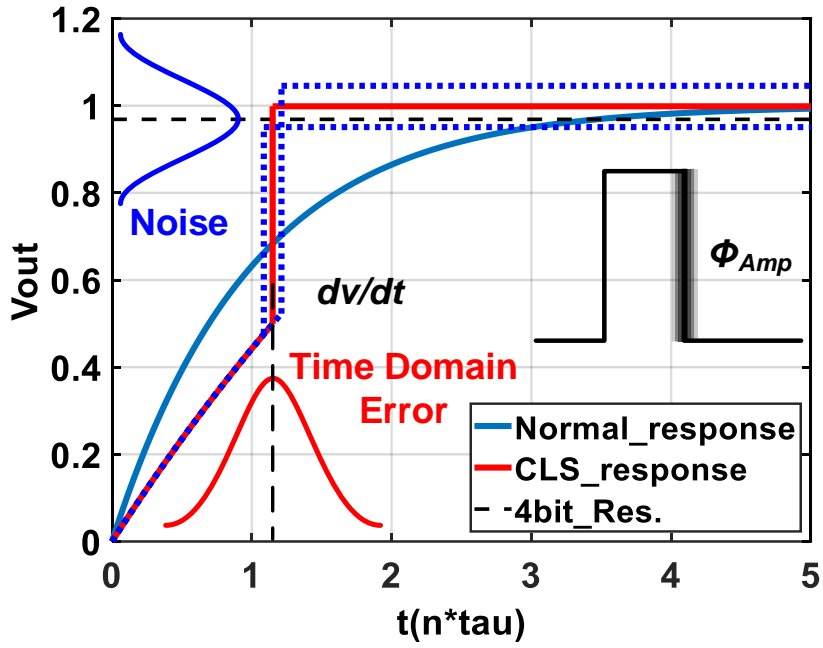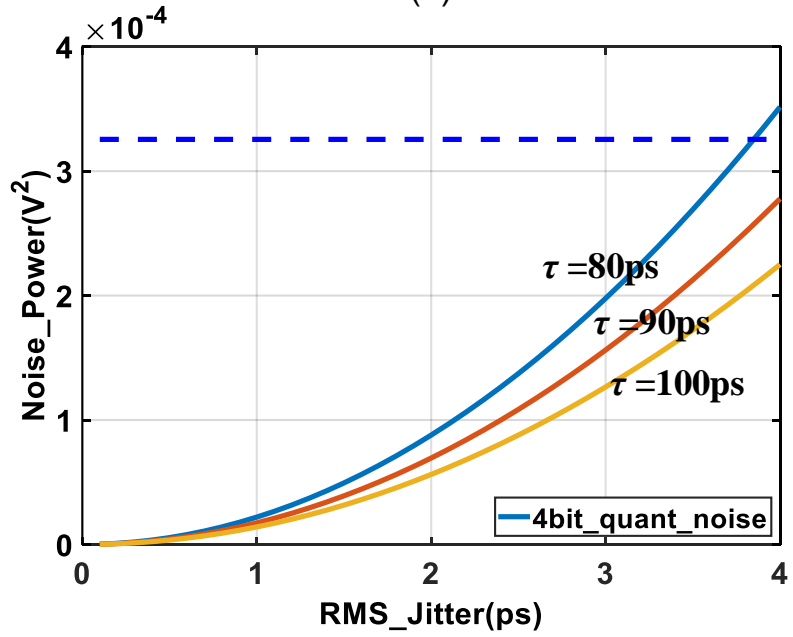
Figure 3.4: Clock jitter impact (a) transient waveforms (b) jitter induced noise power.

According to the previous equation, Fig. 3.4(b) plot the noise power Vs. jitter with
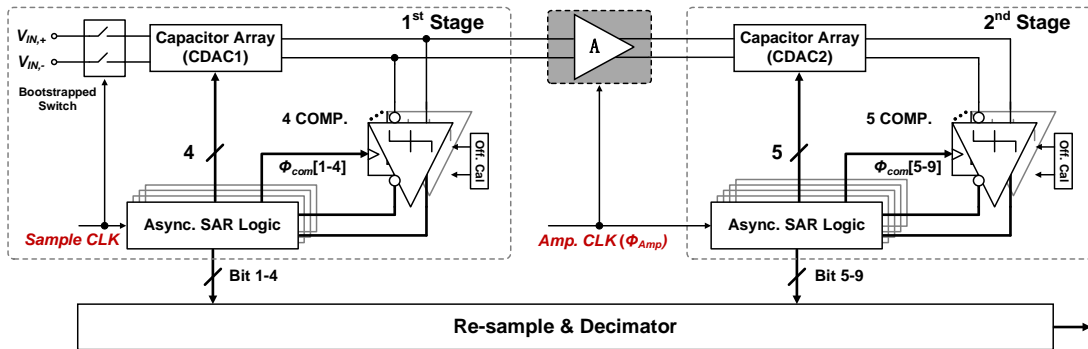
Figure 3.5: Pipeline SAR ADC with output level shifting residue amplifier.

different settling time constant. The jitter specifications on the Φ_{Amp} signal are also not prohibitive, as a relatively large 3.8ps rms jitter can be tolerated to achieve 4-bit accuracy with 80ps settling time constant.

3.3. ADC Architecture and Building Blocks

Fig. 3.5 shows the 8-bit pipelined-SAR ADC with the first pipeline stage converting 4-bits and the second stage converting 5-bits. This 1-bit redundancy between the two stages relaxes the gain, offset, and reference settling requirements of the first stage. The input signal is sampled with a boot-strapped switch that reduces the input sampling time constant and improves high-frequency linearity. kT/C noise requirements are satisfied with CDAC1 and CDAC2 set at 32fF and 16fF, respectively. Both stages employ parallel comparators that are asynchronously activated sequentially for each conversion step, eliminating the comparator reset delay and offering significant speed-up.

The ADC timing diagram is shown in Fig. 3.6. After input sampling, the first stage converts 4 bits and holds the residue voltage for partial amplification when Φ_{Amp} goes high.

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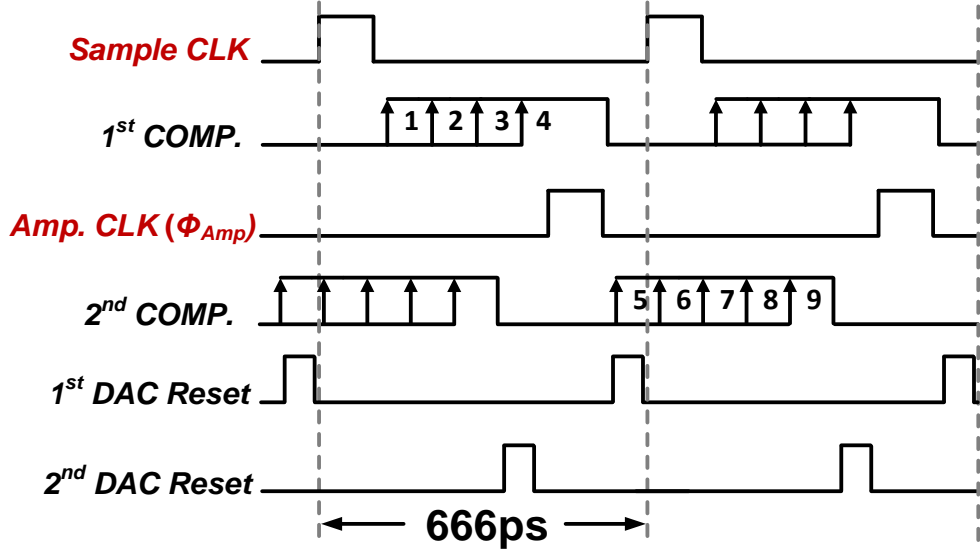
Figure 3.6: Unit Pipeline-SAR ADC timing diagram.

Φ_{Amp} then transitions low and the level-shifted gain is achieved when the Φ_{OLS} pulse is activated with minor modifications in the second stage reference switch logic. The second stage then converts the final 5 bits. Both stage CDACs are reset after their conversions are complete to avoid memory effect, with these reset signals internally generated by the comparator ready signal and input clocks. Independent flipped-voltage followers serve as buffers for the two sets of CDAC reference voltages that are locally decoupled with MOS capacitors. As previously mentioned in Section II, the second-stage reference voltage values are tuned to accommodate any static deviations in the dynamic amplifier gain due to the exact Φ_{Amp} pulse width.

3.3.1. Dynamic Amplifier and Comparator
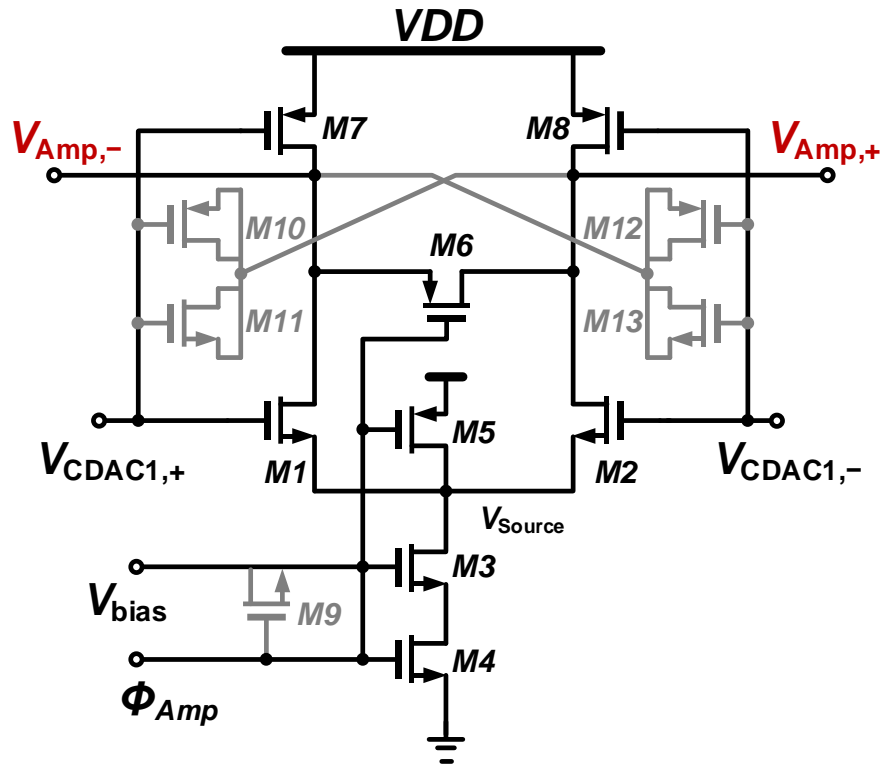
Figure 3.7: Inverter-based dynamic amplifier schematic

A clocked inverter-based buffer that achieves a gain of ~4 serves as the residue amplifier stage, shown in detail in Fig. 3.7. In addition to the main transconductance transistors M1/2 and M7/8, M3 acts as a current source that is switched on by M4 when Φ_{Amp} is activated. The gray transistors improve the dynamic performance, with M10-13 compensating kickback noise and M9 boosting the amplifier startup. When the amplifier is disabled transistors M5 and M6 reset V_{Source} to VDD and short the differential output, respectively. As shown in the Fig. 3.8 transient simulation results, resetting CDAC2 allows the amplifier output to start separating from the common mode and then experience an effective doubling after the level shifting.
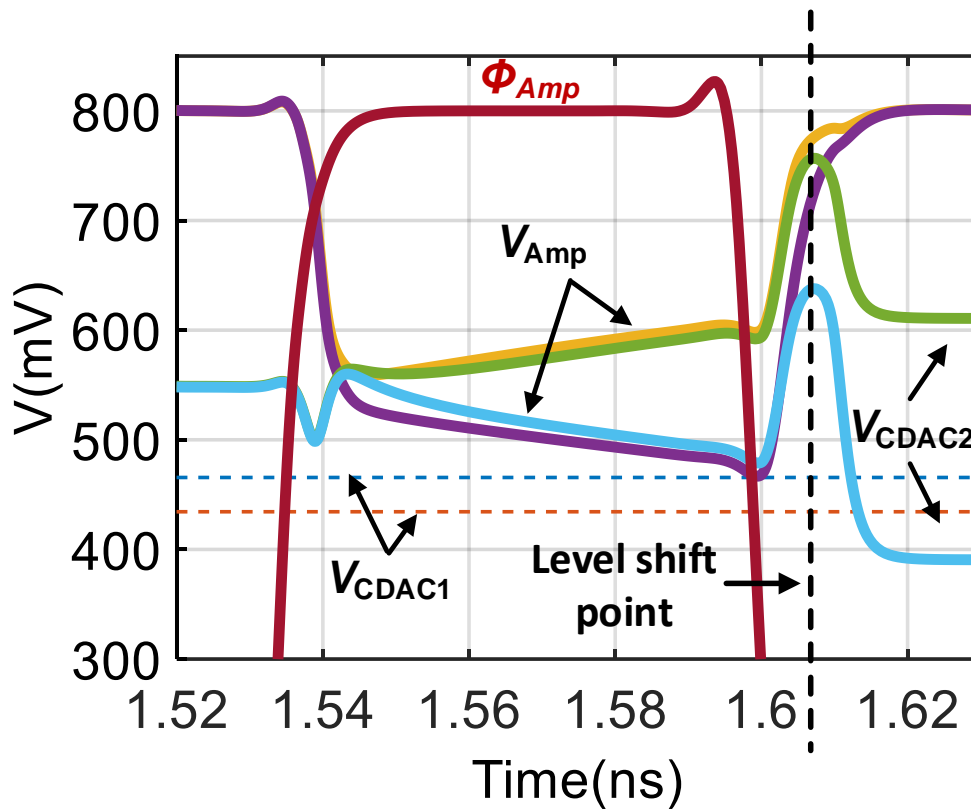
Figure 3.8: Inverter-based dynamic amplifier transient simulations

Dynamic two-stage comparators are used to allow for low-voltage operation in the two pipeline stages. These comparators are foreground offset-calibrated with current-mode DACs.

3.3.2. Second Stage Reference Switch with Embedded OLS

Fig. 3.9 illustrates how the OLS technique is included with minor logic changes in the reference switch control to allow both the CDAC2 bottom and top plate to connect to the amplifier output during the amplification phase. As shown in detail for the negative DAC MSB switches, there is an extra right-most switch that connects the bottom plate to the positive input signal when Φ_{Amp} is high. An AND gate then produces the Φ_{OLS} signal
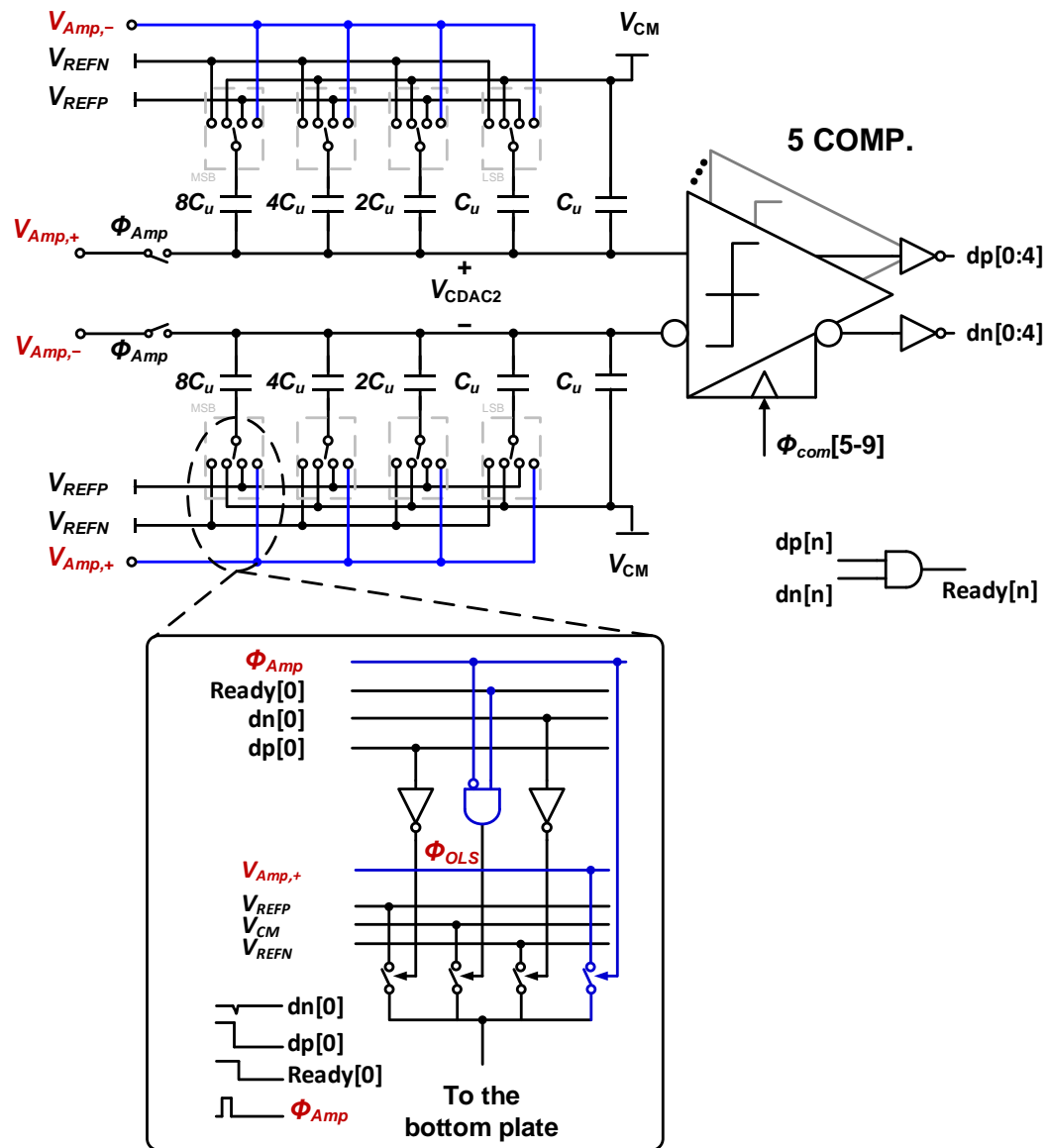
Figure 3.9: Second stage reference switch control with embedded OLS technique

to switch the bottom plate to the common mode when Φ_{Amp} goes low and the comparators'

ready signals are enabled. Since the extra switch is added to the CDAC bottom plate, there

are no speed penalty or reference attenuation issues.

3.4. Experimental Results
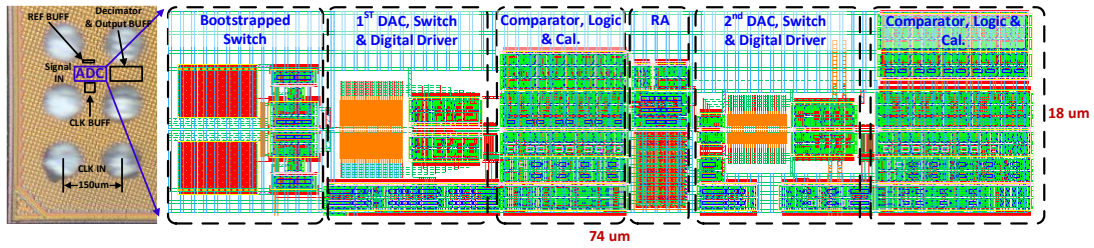
Figure 3.10: Unit-ADC chip micrograph and layout details
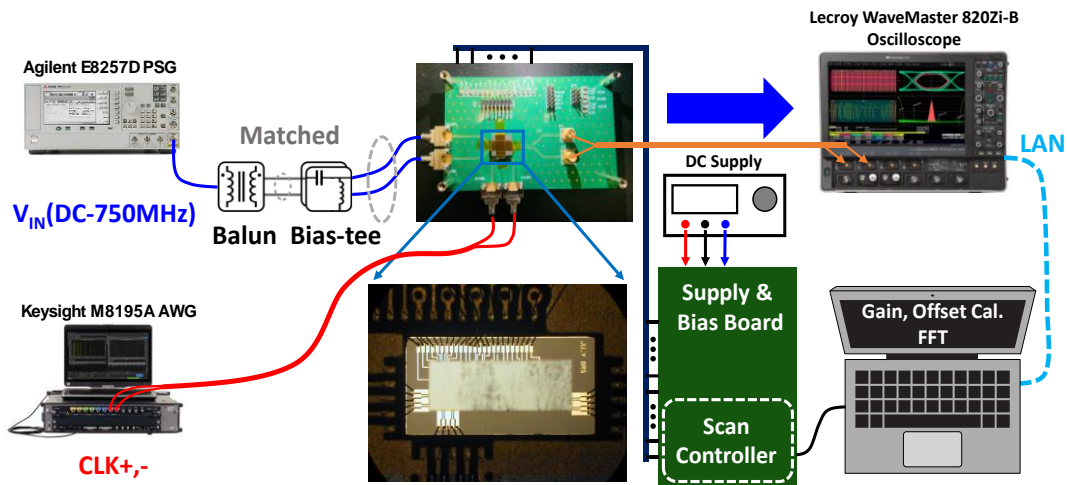
Figure 3.11: ADC characterization set-up.

Fig. 3.10 shows the chip micrograph of the pipelined-SAR ADC, which was fabricated in a 14nm CMOS FinFET process and occupies an active area of 0.0013mm^2. The ADC is powered from a 0.8V supply and has a 460mV$_{pp,diff}$ full-scale input range with a common mode of 500mV. Testing is performed with an initial foreground offset calibration for all comparators. Fig. 3.12 shows DFTs of the ADC output when operating at 1.5GS/s. The achieved SNDR is 43.5dB and 41.4dB for low frequency and close to Nyquist inputs, respectively, translating to 6.93 and 6.58 bits ENOB. Fig. 3.13 shows that

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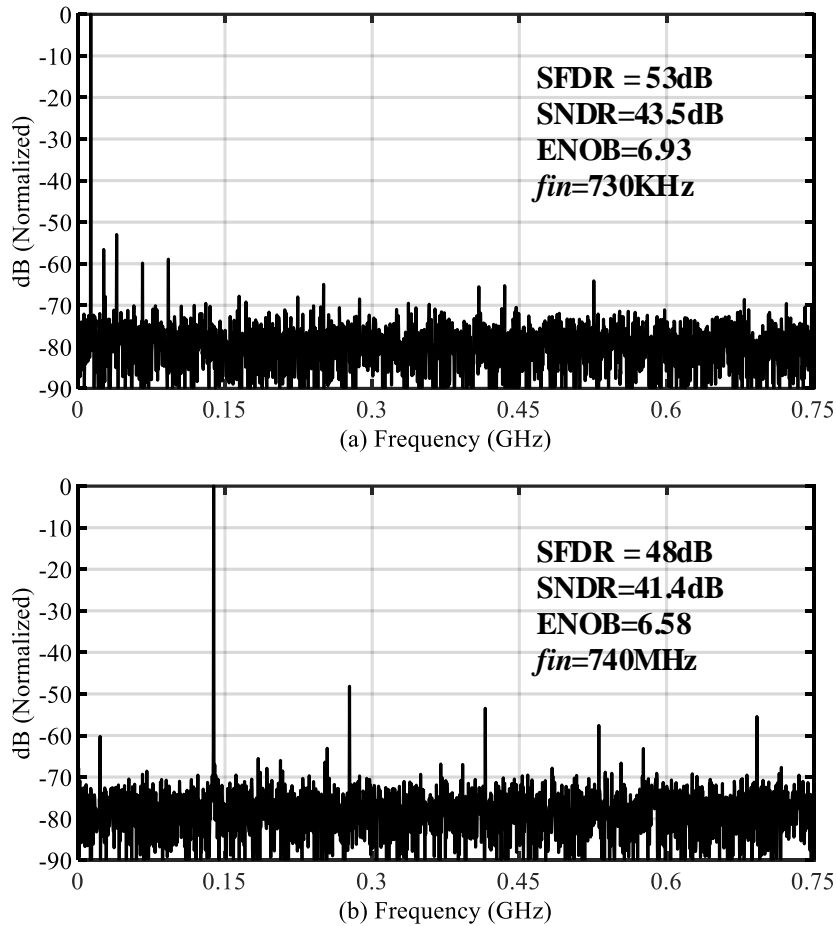
Figure 3.12: ADC DFT results with (a) low frequency input, (b) Nyquist input

the ADC maintains over 40dB SNDR and 45dB SFDR over frequency and Fig. 3.14 shows

the maximum DNL and INL are +0.93/-0.84 and +0.75/-1.02 LSB, respectively. Table I

summarizes the ADC performance and compares this work against previous medium

resolution ADCs

3.5. Conclusion

This chapter presented a single channel 8-bit pipelined-SAR ADC that utilizes a

novel low-overhead OLS settling technique in the dynamic residue amplifier. A low power
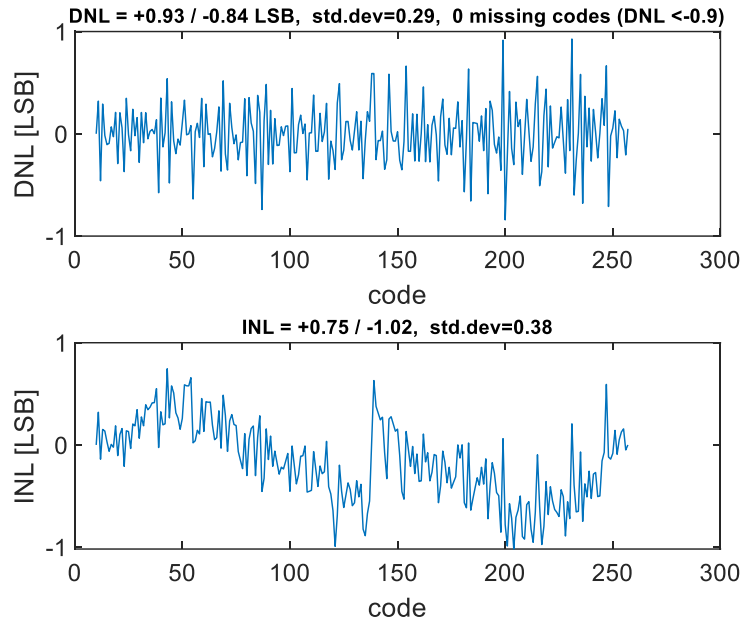
Figure 3.13: DNL and INL plots
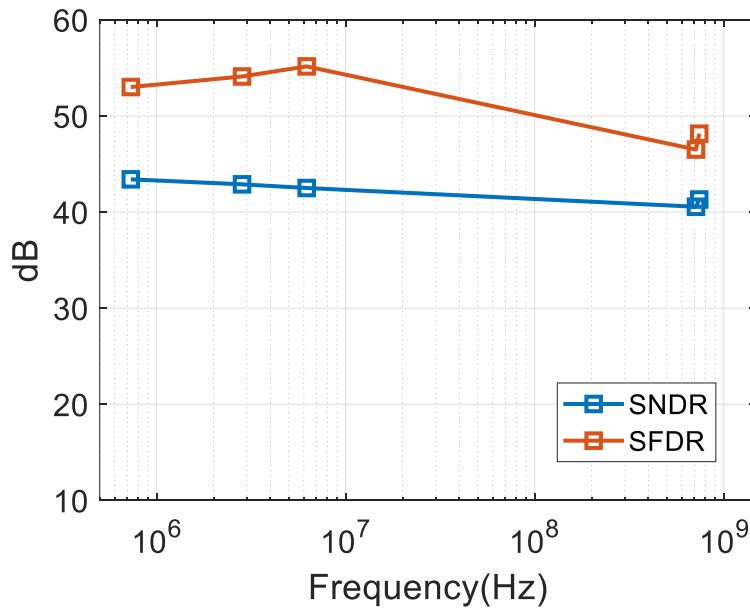
Figure 3.14: SNDR and SFDR Vs. input frequency

design is realized by combining this technique with the use of parallel comparators in the

Table 3.1 Unit-ADC Performance Summary.

References	VLSI'18 [34]	CICC'19 [35]	ISSCC'17 [36]	ISSCC'17 [18]	This Work
Technology (nm)	40	40	28	14	**14**
Supply (V)	1.2	1.1	0.9	0.95	**0.8**
Architecture	Two step SAR	2-3b SAR	1-2b SAR	Pipe-SAR	**Pipe-SAR**
Channels	1	1	2	1	**1**
Resolution (bits)	8	7	7	10	**8**
Sampling rate (GS/s)	1.1	0.9	2.4	1.5	**1.5**
ENOB @Nyquist	7.18	6.3	6.36	8	**6.58**
Area (mm^2)	0.00165	0.014	0.0043	0.00158	**0.0013**
Power (mW)	4	2.6	5	6.9	**2.4**
FOM (fj/conver-step)	25	36.6	25.3	17.7	**16.7**

two asynchronous pipeline stages to allow for 1.5GS/s operation with a low 0.8V supply

voltage.

4. A 38GS/S 7-BIT TIME-INTERLEAVED PIPELINED-SAR ADC WITH SPEED-ENHANCED BOOTSTRAPPED SWITCH[*]

This chapter presents a 7-bit, 38 GS/s, 32-way Time-Interleaved ADC, which utilizes a high-bandwidth 8-way interleaver architecture based on a proposed speed enhanced bootstrapped switch, which shows higher operation speed and better EBON with high frequency input. For the high-speed unit-ADC design, the pipeline structure of the 4-bit 1st stage and 4-bit 2nd stage is utilized for low power and high-speed design, and utilized output level shifting settling technique (OLS) allows for an inter-stage gain of ~ 4 with low power and achieves only 33% of a conventional CML amplifier based exponential settling. The unit ADC's conversion speed is further improved with the use of a parallel comparator in the two asynchronous stages. The ADC was fabricated in the Intel 22nm FinFET technology, at 38GS/s, the 7b ADC achieves 41.9fj/conv.-step at low frequency, 64.1fj/conv.-step at Nyquist, and has a 20GHz 3dB bandwidth.

4.1. Introduction

High-speed time-interleaved ADCs are becoming more common in wireline receiver front-ends due to the enabling of subsequent digital processing for equalization and easier support of higher-order modulation schemes [6]-[9]. Fig. 4.1 shows a common implementation of the high-speed time-interleaved ADC[10][11], which utilize two rank

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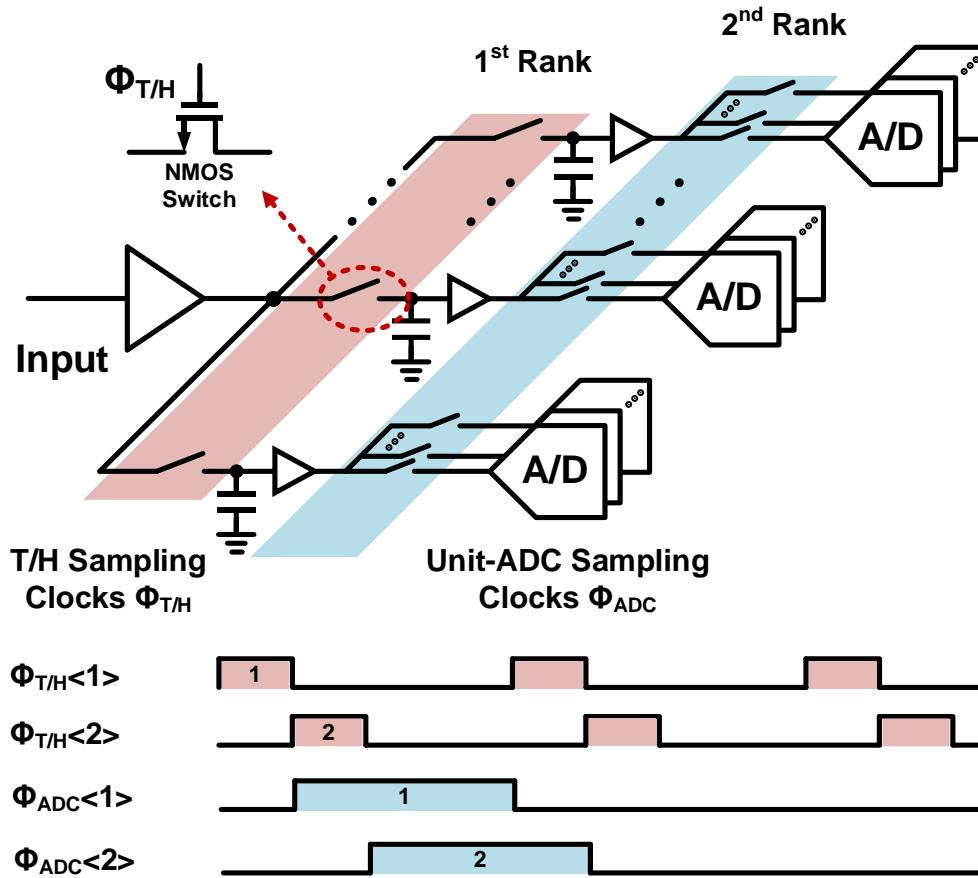
Figure 4.1: A common structure of the high-speed time-interleaved ADC

architecture. The first rank is high-speed tracking and hold circuit with less interleaving

factor, each tacking and hold channel followed by multiple unit-ADCs that performs

analog to digital conversion for the held volage from the first rank. Given that the high-

speed sample and hold is only utilized at the first rank, this architecture is able to

efficiently decreases the critical sampling clock phases for massive interleaving unit-ADC

channels. and alleviate the bandwidth mismatch between T/Hs.

However, the sampling of wideband analog signals associated with higher data

rates is a big challenge for conventional bootstrapped switch (BS) T/H circuits. one reason

for this is that the low-duty-cycle sampling clocks are utilized for avoiding sampling crosstalk between time-interleaved sub-ADCs, shorten the tracking time and requires improvements in T/H circuit startup time. The other reason is as technology nodes scale, ADCs based on the digital-intensive SAR architecture becomes faster, in order to keep the low interleaving factor for T/Hs, it requires the T/H circuits scales same in speed. This motivates the use of simple NMOS switches in high-speed ADCs [12]-[15]. However, even the input buffer is NMOS source follower, the common mode input of the sampling circuit is above the V_{DSAT} that results in medium conductance of the NMOS sampling switch. Therefore, with the nominal supply voltage, the NMOS switch requires quite large size transistors to satisfy the settling requirements. Significant size of the NMOS switch result in additional non-linear capacitance on the first rank and increase the loading of the input broadband buffer. Also, the NMOS switch negatively impact the high-speed linearity and ADC front-end bandwidth.

The other challenge is from the unit-ADCs [16][17]. In order to achieve high date rate wireline communication, the converters have to employ a large amount of time-interleaved unit-ADC. A high-speed low-power unit ADCs that can reduce the interleaving factor for a given effective sampling rate, resulting in smaller area and an overall simpler design.

To overcome these issues, this chapter presents a time-interleaved ADC that utilizes both a high-bandwidth interleaver architecture based on a proposed speed-enhanced bootstrapped switch [19] and a pipelined-SAR unit ADC that utilizes a novel

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output level shifting (OLS) [20] settling technique to enable low-voltage operation and low power consumption of the dynamic residue amplifier with low hardware overhead.

This chapter is organized as follows, Section II describes the ADC architecture including the interleaver structure with the proposed speed-enhanced bootstrapped switch. A detailed discussion of the unit pipeline-SAR ADC with OLS settling technique and some key circuit details are given in Section III. Measurement results from a 22nm CMOS FinFET prototype are presented in Section IV. Finally, Section V provides the paper conclusion.

4.2. Time-Interleaved ADC Architecture

A top-level overview of the 38GS/s time-interleaved ADC is shown in Fig. 4.2. The ADC core consists of an 8-way first-rank interleaver that samples and buffers the input signal, 32-way unit-ADCs, which performs the A-2-D conversion, and multi-phase clock Gen.

The ADC input is fully differential and terminated by a 100-ohm resistor. Both sides of the input are protected by the reduced electrostatic discharge diodes (ESD) for less input bandwidth impact. A T-Coil termination architecture is utilized to reduce the effective capacitance seen at the input of the ADC by tuning out the ESD capacitance [21]. The ADC input firstly connect to two parallel buffers which separately drive even and odd channels from the 8 parallel sampling switches that sample the input on the sampling capacitors. The sampled voltages are then buffered and forwarded to 4 sub-ADCs. Pipe-SAR ADCs are chosen to convert the samples, as SAR ADC are mostly digital architecture
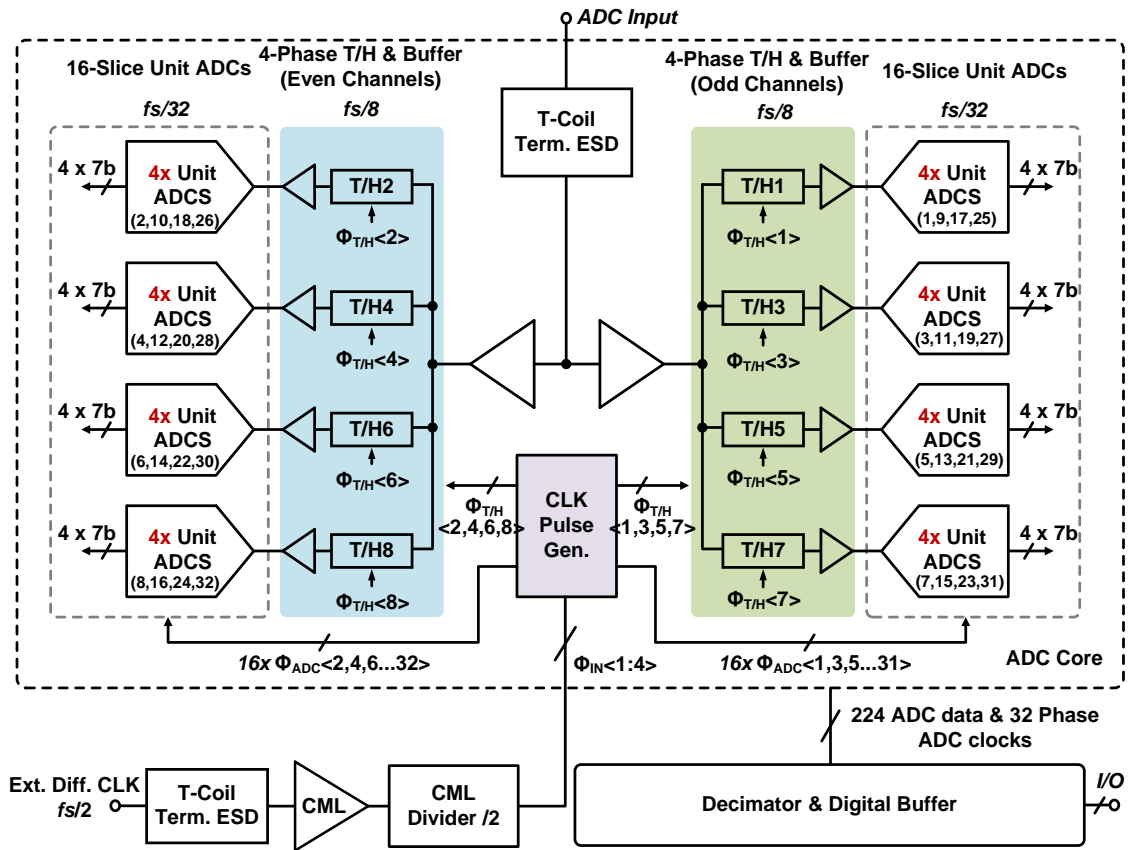
Fig. 4.2. An overview of the ADC, the ADC core consist of muti-phase clock gen, 32-channel unit-ADCs and 8-channel T/Hs

is highly suitable for advanced technologies at low supply voltages, and pipelining techniques have been proved to be both power efficient and high speed.

The 32 channel 7-bit digital output data and clock of each unit ADCs are captured by a synchronize block then connected to the decimator that down sample the output data rate to ~MHz for the measurement. A differential external clock is connected to an on-chip CML buffer then pass through the CML divider. The four phases of the CML divider output are converted to CMOS level then feed into the ADC core. The 8 clock phases of

T/Hs

Unit ADCs

$\Phi_{T/H}<1>$ C_S $\Phi_{ADC}<1>$ $C_{S\text{-}ADC}$

$\Phi_{T/H}<3>$ $\Phi_{ADC}<9>$

$\Phi_{T/H}<5>$ $\Phi_{ADC}<17>$

$\Phi_{T/H}<7>$ $\Phi_{ADC}<25>$

V_{in}

$\Phi_{T/H}<2>$ C_S $\Phi_{ADC}<2>$ $C_{S\text{-}ADC}$

$\Phi_{T/H}<4>$ $\Phi_{ADC}<10>$

$\Phi_{T/H}<6>$ $\Phi_{ADC}<18>$

$\Phi_{T/H}<8>$ $\Phi_{ADC}<26>$
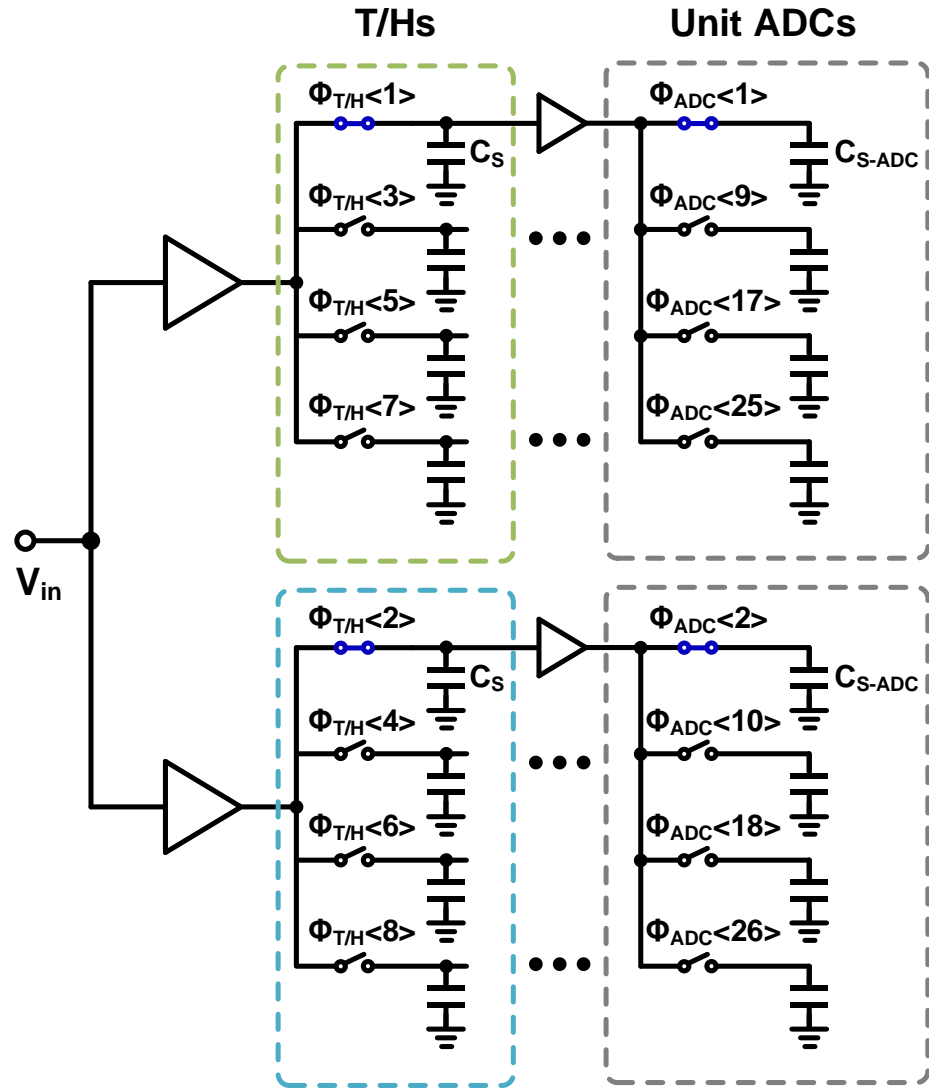
Fig. 4.3. Interleaver architecture

the Tracking and Hold (T/H) and the 32 clock phases of the unit ADC clock are derived

from the CLK pulse generation block which is the part of the ADC core.

4.2.1. ADC Timing Diagram
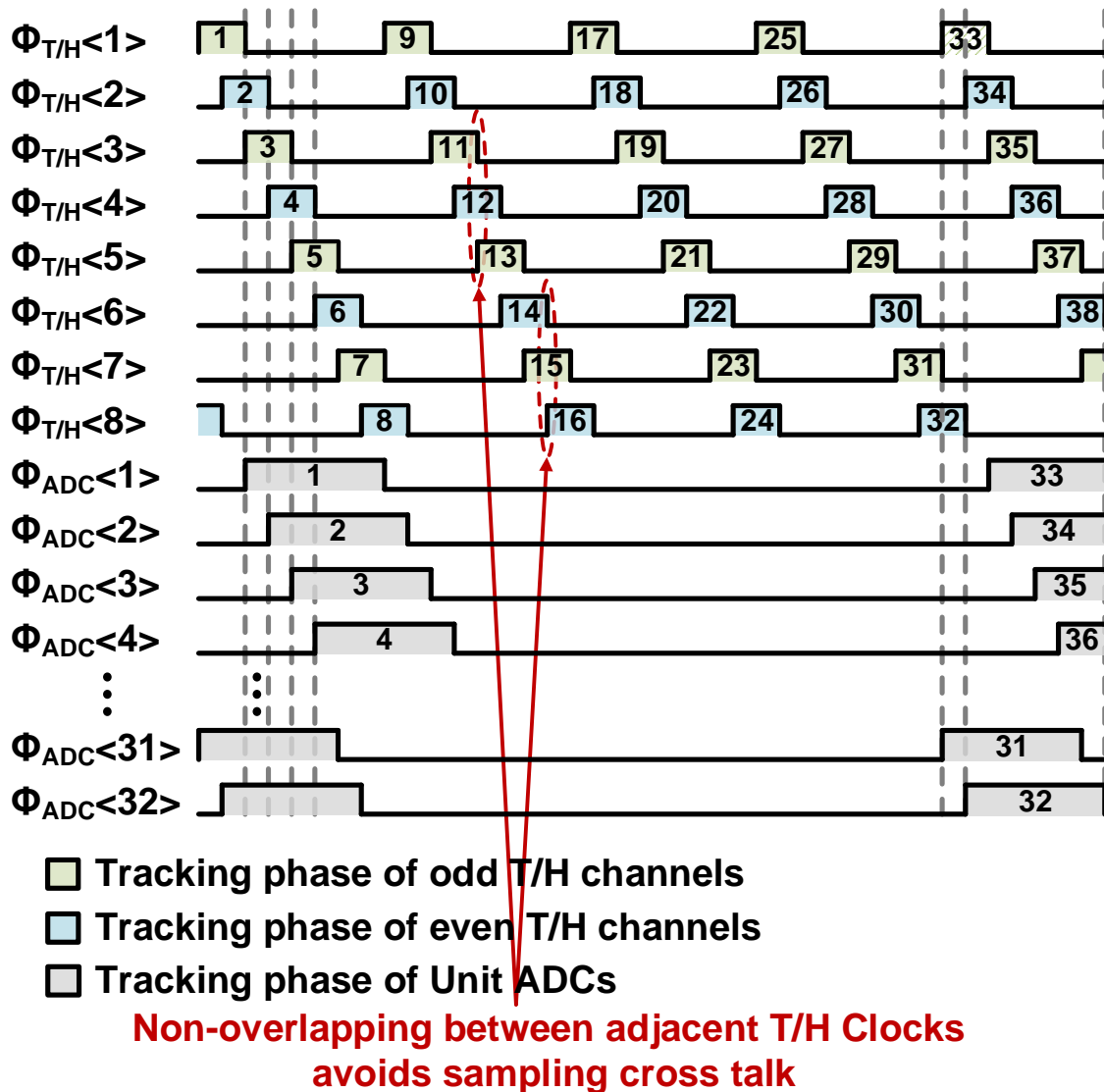
Fig. 4.4. Corresponding timing diagram of sampling clocks and unit-ADC clocks

Fig. 4.3 shows the interleaver architecture. There are two stages of the time-interleaving, The first rank is an 8-way T/Hs where the input is sampled and held by 8 phase clocks and two input buffers. Parallel even and odd input buffers drive half of the first-rank 8-way T/Hs. Fig. 4.4 shows corresponding timing diagram of sampling clocks and unit-ADC clocks, the T/H is clocked by fs/8 25% duty-cycle pulse, which avoid the
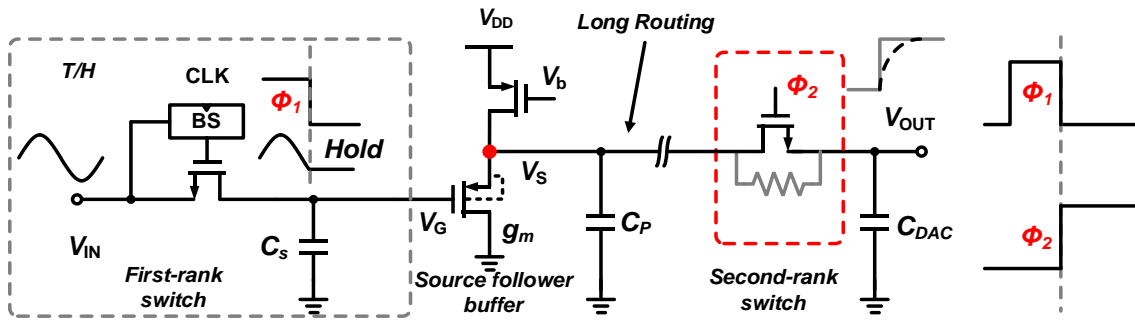
Fig. 4.5. Circuit detail of an interleaving channel
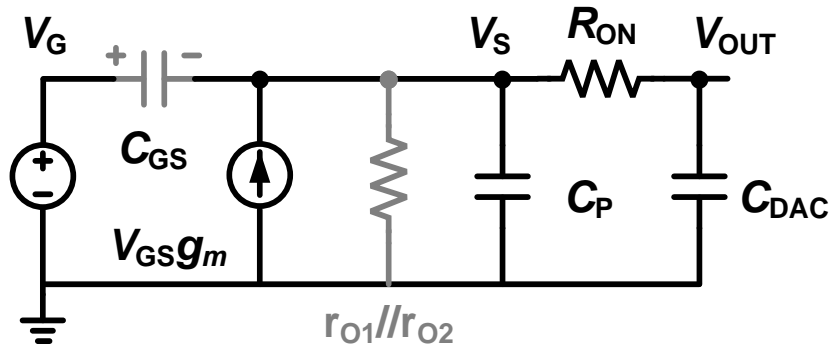
Fig. 4.6. Small signal model when the second-rank switch is 'ON'

sampling crosstalk in each 4 even and odd T/H channels, and since the even and odd channel is isolated by the parallel input buffers, there is no sampling crosstalk between all the T/H channels. The 2nd interleaving stage, realized through ADC buffer, drives 4 unit-ADCs slices but only one unit-ADC sampling switch is on at each time. The 32-phase unit-ADC sampling clock runs at fs/32 and each unit-ADC clock sampling phase overlaps with 1st stage holding phase.

4.2.2. Interleaver architecture and proposed speed-enhanced bootstrapped switch

In order to derive the efficient design technique for the high speed interleaver. This part first analysis the step response of the sample and hold process. Fig. 4.5 shows the

schematic of a sampling channel, the buffered input signal first sample and hold on the 1st rank sampling capacitor CS and connect to the gate V_G of a source follower which servers as 2nd rank buffer to drive the following unit-ADCs which contains second rank sample and hold circuit. The second rank switch is enabled while the first rank switch is in hold phase.

The significant layout size difference between the less interleaved and relatively small size T/Hs and massive slices unit-ADCs caused long routing from the buffer to unit-ADCs. Since each unit-ADC needs to see the full input bandwidth, the second rank buffers are the most power-hungry block of the interleaver. It is very challenging to design such a buffer that can drive the unit-ADCs through long routing with low power.

As V_S, output of the source follower, has an initial value when the 2nd rank switch is 'on', also VS is changing during the settling process due to the finite bandwidth of the 2nd rank buffer. It is not a simple RC settling process and the math results for the transient step response can be tricky.

Fig. 4.6 shows the small signal model when the 2nd rank switch is on. V_{OUT} is the voltage on the unit-ADC DAC. C_P consist of the self-capacitance loading of the buffer and the capacitance parasitic from routing, usually C_P is comparable to C_{DAC}, which is the capacitive DAC of the unit-ADC, due to the long routing from buffer to each unit-ADC. From the layout extraction, C_P/C_{DAC} is roughly 2 for this design. First, write the current equation for the V_S node using Kirchhoff's current law, and C_{GS} is neglected, because the gate voltage is already held

$$C_P \frac{dV_S}{dt} - g_m \cdot V_{gs} + \frac{V_S - V_{OUT}}{R_{ON}} = 0 \tag{4.1}$$

The voltage V_S is expressed by

$$V_S = R_{ON} \cdot C_{DAC} \cdot \frac{dV_{OUT}}{dt} + V_{OUT} \tag{4.2}$$

In the Eq. (4.1), assume the output impedance of the source follower ro1//ro2 is infinite, which lead to an ideal unit gain source follower. Since the gain of the source only impacts the steady-state and causes the static error, and it could be calibrated as channel gain error, therefore ignored in the dynamic settling error analysis.

Also given the worst case for the initial condition. The worst case happens when V_{OUT} settles from '0' to max amplitude with a Nyquist input which gives maximum difference between V_G and V_S

$$V_{OUT}(0) = 0, \ V_S(0) = 1 - \max(|V_G(t) - V_S(t)|) \tag{4.3}$$

And $\tau = R_{ON} \cdot C_{DAC}$, $GBW \cdot 2\pi = \frac{g_m}{C_P}$, the transient step response of the V_{OUT} is derived by solving the Eq.(4.1) and Eq.(4.2) with the initial condition Eq.(4.3). And the final results is a function with 2nd rank switch time constant τ, 2nd rank buffer GBW and hold time.
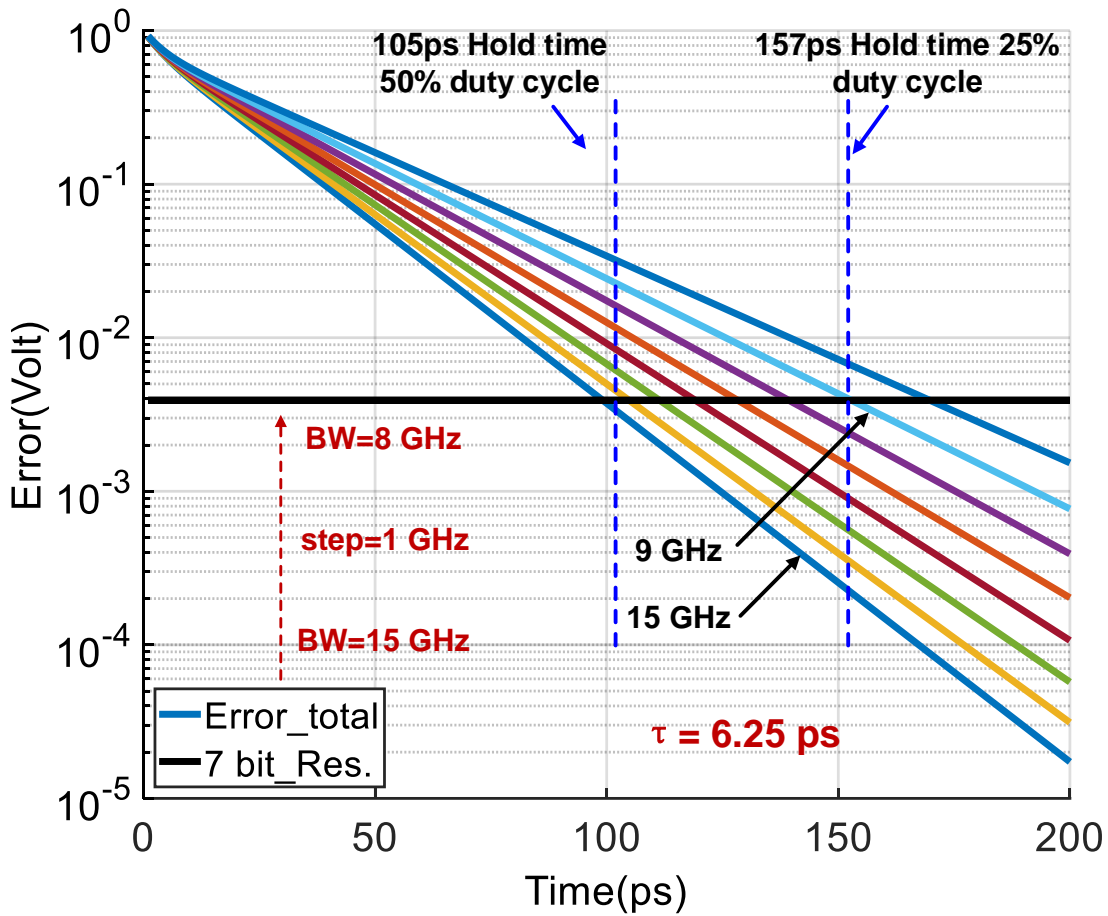
Fig. 4.7. Settling error vs. hold time with different 2ⁿᵈ rank buffer bandwidth

Since combine the eq. (4.1) and eq. (4.2) gives a non-homogeneous differential equation, it is solved by MATLAB. Based on the results of the transient response, Fig. 4.7 shows the modeling results of settling error vs. hold time with different 2ⁿᵈ rank buffer bandwidth. The required 2ⁿᵈ buffer bandwidth is just 9GHz with 25% duty-cycle compared to 15GHz with the 50% duty-cycle. The 25% low-duty-cycle sampling clock significantly relax the buffer bandwidth requirements by increase the holding time and therefore save the power.

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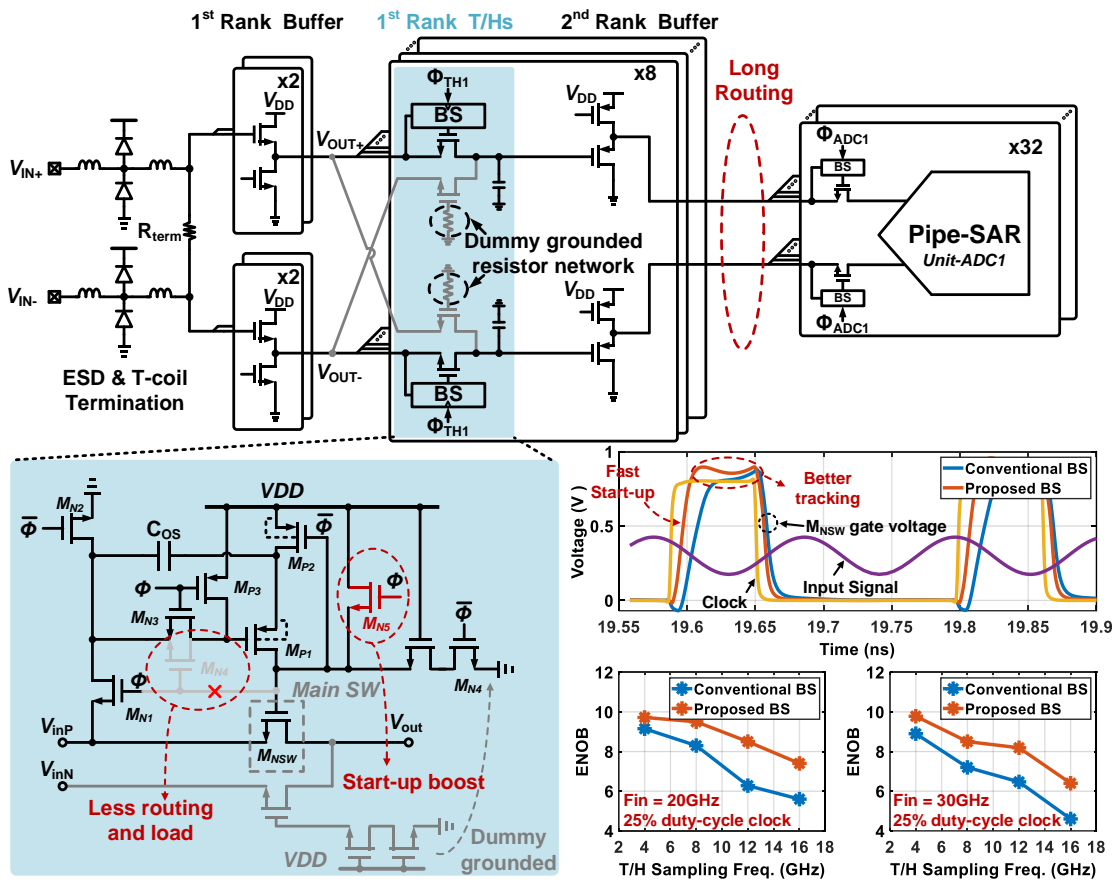
Fig. 4.8. Interleaver schematic, proposed speed-enhanced bootstrapped switch and T/H post-layout simulations

While the 25% duty cycle first-rank T/H clock reduce the buffer bandwidth requirements and sampling crosstalk, it does necessitate that the T/H have a fast start-up time. It is difficult because the T/H is load by the second-rank buffer that has to be sized sufficiently to drive long routing parasitics to the second- rank switches. The proposed BS topology, shown in Fig. 4.8, modifies the M_{N1} gate connection to come directly from Φ. As soon as the clock is enabled, M_{N1} turns on to transfer the boosted voltage to the M_{NSW} gate to reduce start-up time and offer better tracking of the high-speed input. M_{N5} is also added to rapidly pull up the M_{NSW} gate signal upon entering track mode to further improve the start-up time. Post-layout transient simulation waveforms show that the proposed

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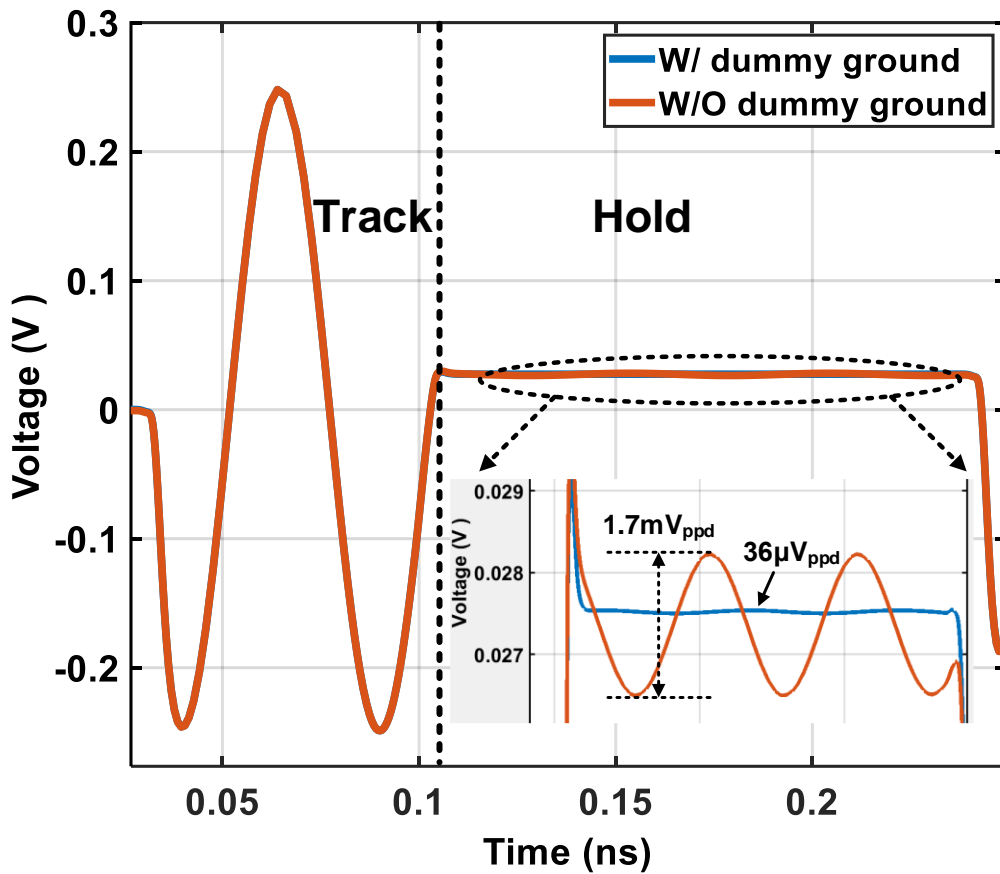
Fig. 4.9. Hold phase signal feedthrough impact

topology has a wider switch on pulse, faster start-up, and better tracking relative to a conventional bootstrapped switch. At the effective $f_s/8$ T/H frequency of 4.75GHz for 38GS/s operation, this results in 0.75b and 1.1b improvement in ENOB with 20GHz and 30GHz input signals. Projecting this bootstrapped switch operation in ADCs with higher speed 16GHz clocks shows further improvement of 1.8b with both 20GHz and 30GHz input signals.

A dummy ground network added to the gate of the dummy switch transistor which servers a signal feedthrough neutralized path. The dummy grounded network creates a
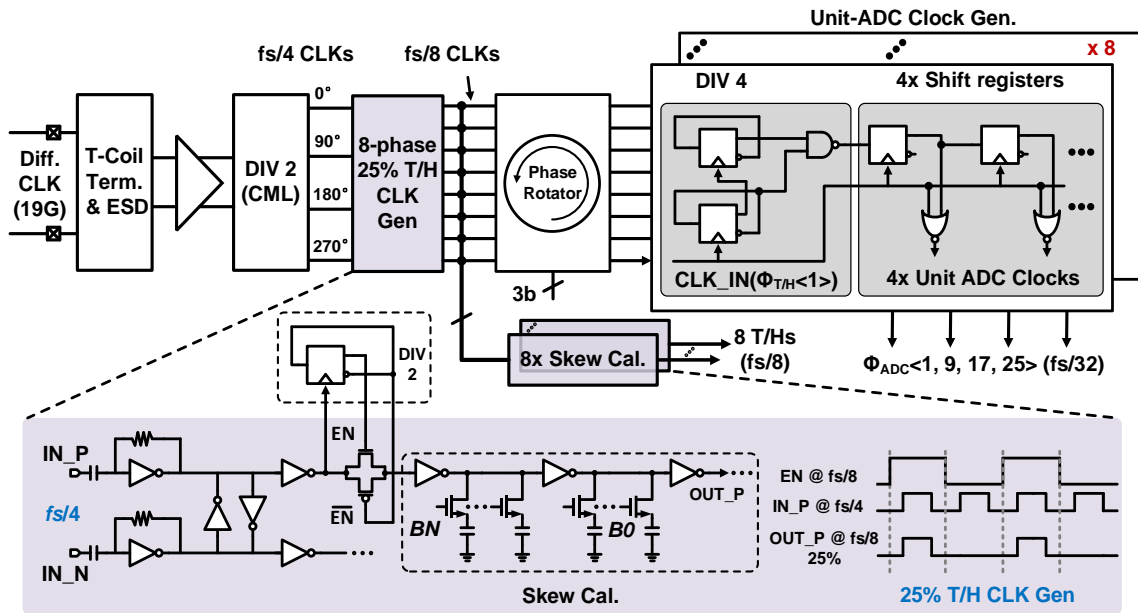
Fig. 4.10. Clock generation include high performance 25% duty cycle 8-phase T/H clock gen., skew calibration DAC, and 32-phase unit ADC clock gen.

copy of the gate loading of the main sampling switch M_{NSW} in the holding phase, therefore generates an accurate negative signal feedthrough. Fig. 4.9 shows the T/H simulation results with Nyquist input, with dummy grounded network, the peak-to-peak signal swing in the hold phase is only 36μV compared to 1.7mV that without dummy grounded network. Also, the FFT results shows 1-bit ENOB improvement at Nyquist.

PMOS source follower-based 2nd-rank buffer is utilized for generating a suitable around VDD/2 input common mode of the unit-ADC comparators for the high-speed operation, and the input 1st rank buffer is NMOS source follower which gives lower output common mode for the linear operation of the 2nd rank buffer.

4.2.3. Multi-Phase Clock Generator

Fig. 4.10 shows the schematic of the clock generator for 8 phases T/Hs 4.75GHz clocks and 32 phase 1.1875GHz unit-ADC clocks. The fs/2 external clock first pass
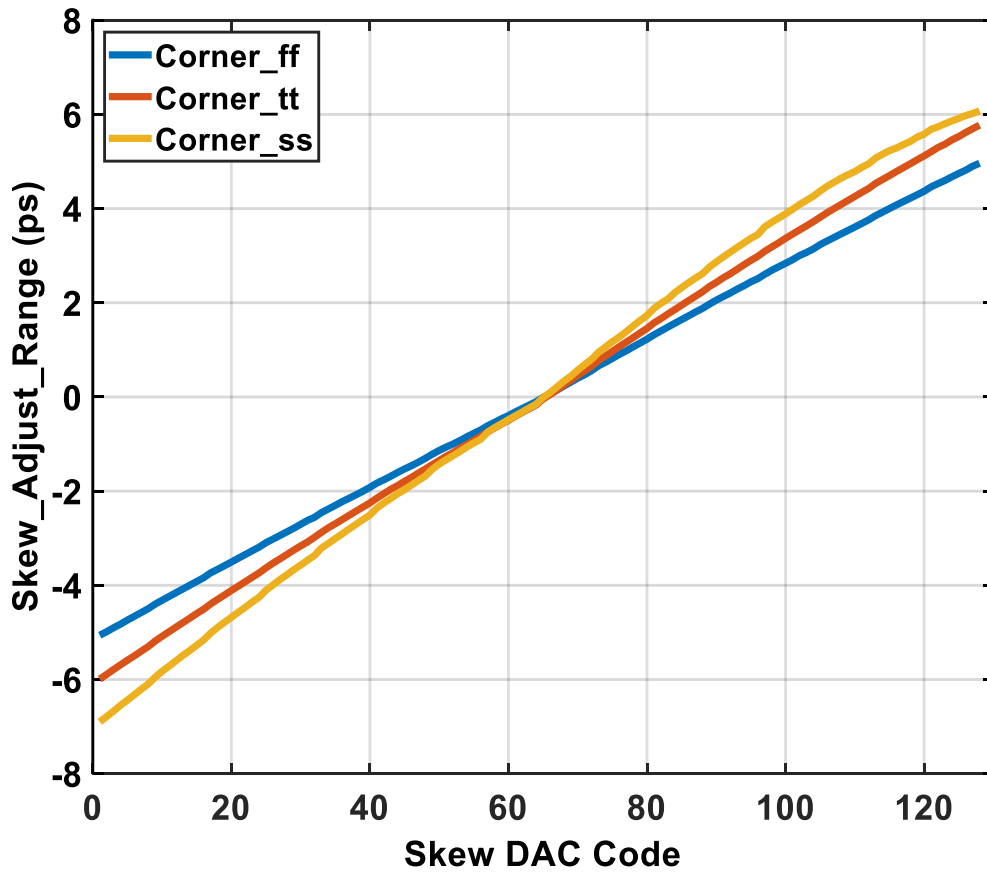
Fig. 4.11. Skew DAC simulation

through a CML divider /2 circuit, which generates 4 phase fs/4 clock with 90° phase space.

The 4 phase CML level clock signal are fed to a CML-to-CMOS circuit and then connect

to a CMOS divider /2 circuit that outputs 8 phase CMOS level fs/8 clock with 50% duty

cycle and 45° phase space.

     Meanwhile, the CMOS level fs/4 clocks connect to pass gate which is enabled by

the fs/8 clock. By properly align fs/8 and fs/4 clock, the 25% fs/8 sampling pulses is

selected from fs/4 clock. And all the 8 phase 25% sampling is derived by choosing the

different phase of fs/8 and fs/8 clocks.

Then 8 phases 25% sampling pulse connected to skew calibration capacitors and buffers to the sampling switches. The skew calibration has 7-bit resolution with ~95fs step, simulation results with different corner are shown in Fig. 4.11. Clock jitter is optimized by separately placing the programable capacitive loadings in several buffer stages to achieve steep rising and falling edges.

The unit-ADC clocks are derived from the T/H clocks. Each T/H clocks connects to a divide by 4 circuit and follows by 4 shift registers that generates 4 phase fs/32 clocks. Totally 32 phases unit-ADC clocks are divided from 8 phase T/H clocks, NAND and NOR logic gate shape the unit-ADC clock pulse width to set the ADC sampling pulse width equals to the hold width of the T/H clock pulse.

Also, a phase rotator is inserted between the T/H clocks and unit-ADC clock generator, the 360° phase rotation with 3-bit control is manually adjusted to align the sampling phase of the unit-ADC clock with the hold phase of the T/H clocks.

4.3. Unit Pipeline-SAR ADC Architecture

Fig. 4.12 shows the 7b unit pipelined-SAR ADC. Both pipeline stages convert 4-bits, with 1-bit redundancy between the stages to relax the first stage gain, offset, and reference settling requirements. The second-rank switch is the same proposed bootstrapped topology to reduce the input sampling time constant and improve linearity. kT/C noise requirements are satisfied with CDAC1 and CDAC2 set at 32fF and 16fF, respectively. Both stages employ parallel comparators that are asynchronously activated sequentially for each conversion step, eliminating the comparator reset delay and offering significant speed-up.
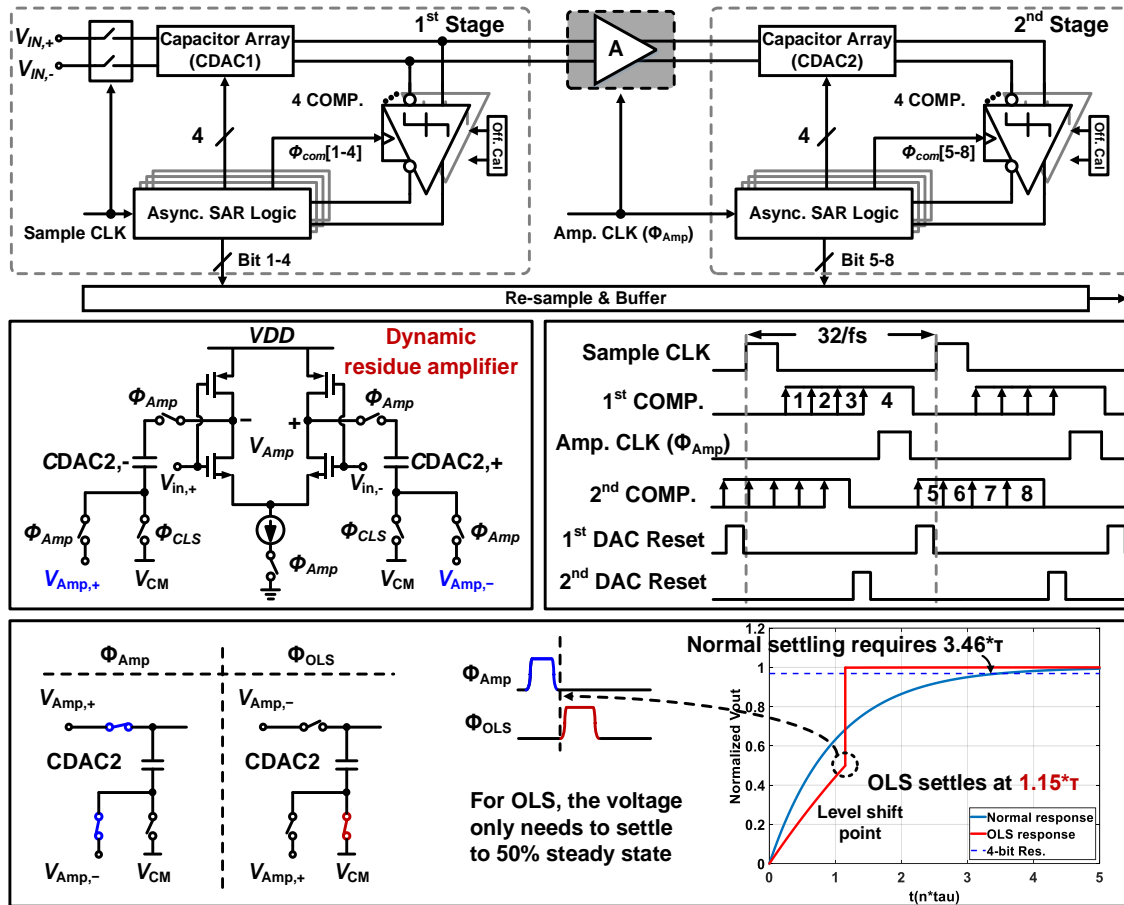
Fig. 4.12. Unit-ADC and building blocks

A clocked inverter-based buffer that achieves a gain of ~4 serves as the residue amplifier stage. An OLS technique [20] allows the residue amplifier output to only settle to 50% of the steady state value, which results in a 1.15τ settling time that is roughly 3X faster than a conventional CML amplifier's settling for 4-bit resolution. This allows for lower average power due to the dynamic amplifier's reduced activation time. Both the first and second pipeline stages have independent reference DACs and buffers, which avoids crosstalk and allows for inter-channel gain mismatch and inter-stage gain error calibration.
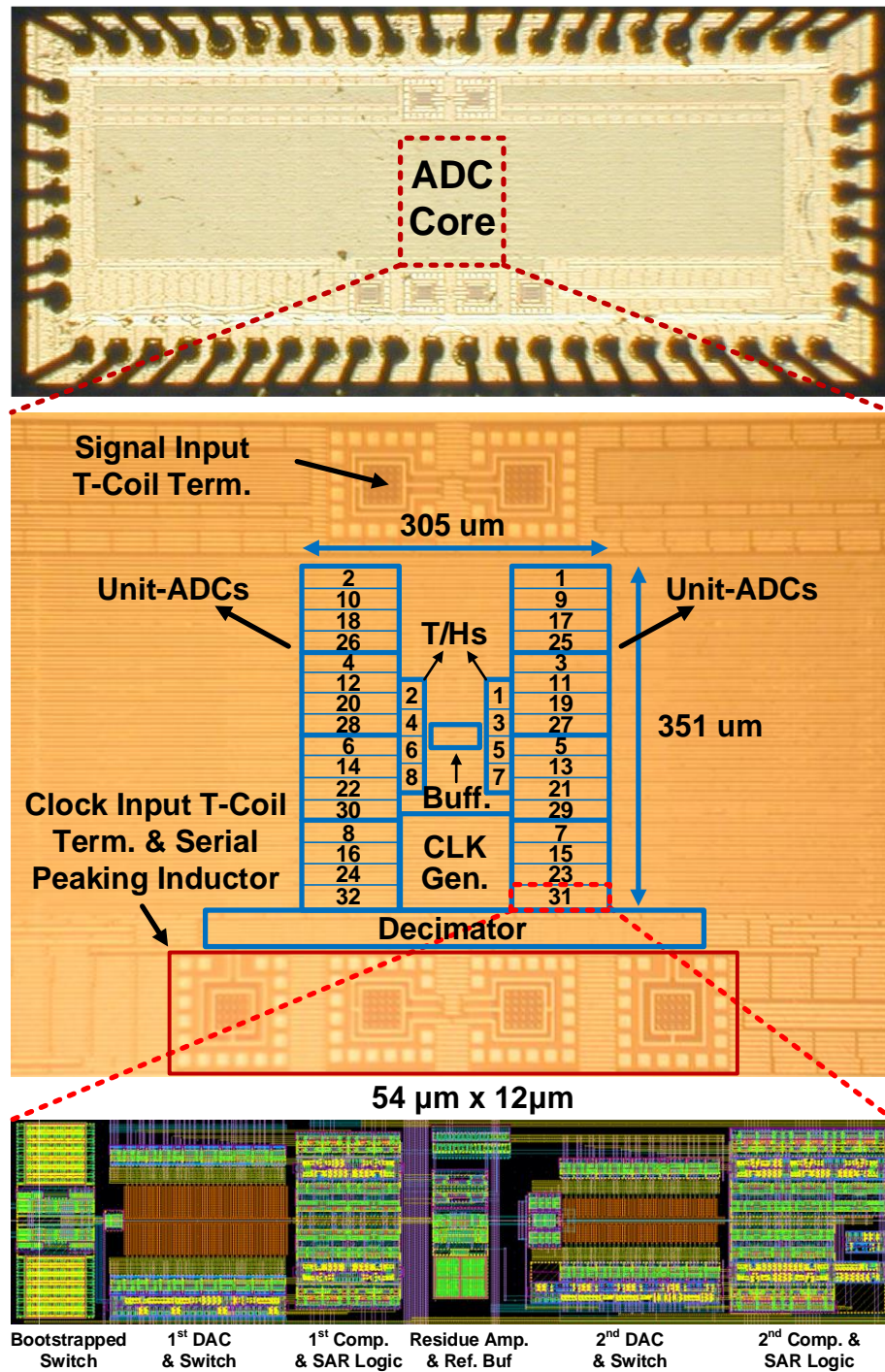
Fig. 4.13. TI-ADC Chip micrograph and layout details

Dynamic two-stage comparators [24] are used to allow for low-voltage operation

in the two pipeline stages. These comparators are foreground offset-calibrated with

54
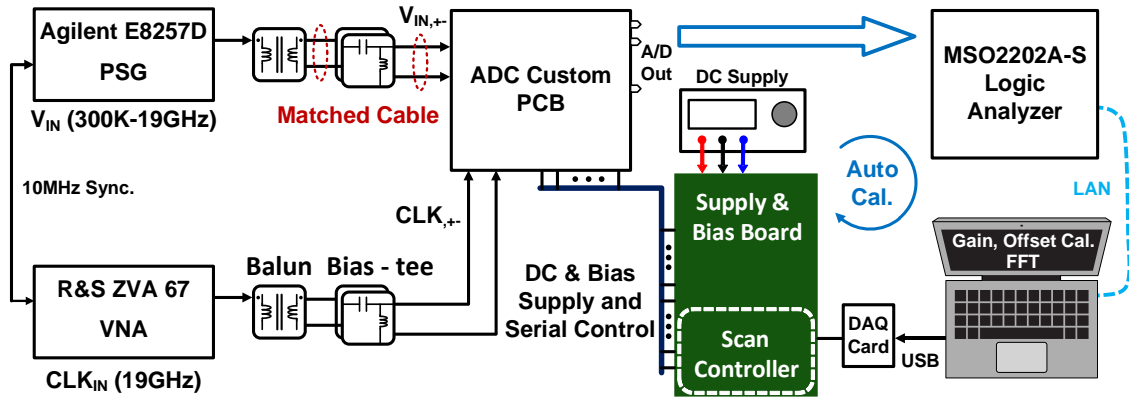
Fig. 4.14. Time-Interleaved ADC characterization and foreground auto calibration setup
current-mode DACs

4.4. Experimental Results

A chip microphotograph and layout floor plan of the prototype 7-bit 38GS/s ADC, which was fabricated in Intel 22nm CMOS process, is shown in Fig. 4.13. The core time-interleaved ADC, consisting of two input buffer, 8-way T/H, multi-phase clock generator and 32-way unit pipeline-SAR ADCs, occupies 0.107 mm^2. All the even and odd channels are split on the left and right side for symmetric routing and placing the front-end T/H close to the unit-ADCs minimized the high-speed signal routing from the 2nd rank buffer to each unit-ADCs. This maximum distance is about 160 um length, which adds a ~ 81fF capacitive loading due to routing. The critical 8 phase sampling clock routing is also reduced by placing the clock generator close together to the T/H circuits, and the number of the clock buffer chain is optimized for the best jitter performance. Also, one unit pipelined-SAR ADC core only occupies 54um x 12um, and for the unit-ADC layout, the bootstrapped switch, 1st SAR ADC, residue amplifier, 2nd SAR ADC are placed in

55
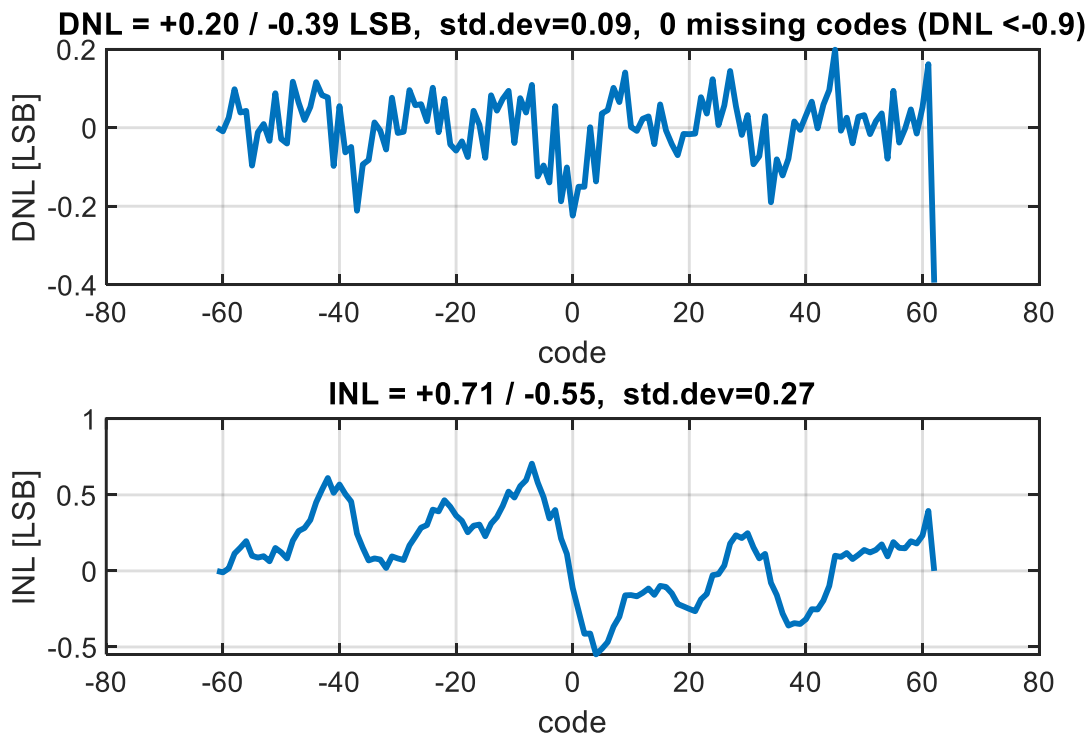
Fig. 4.15. Aggregated DNL and INL of the Time-Interleaved ADC

sequence, each unit-ADC has independent reference buffer for avoiding the reference coupling noise.

The measurement is performed with the wire-bonded chip-on-board test setup. Fig. 4.14 shows time-interleaved ADC characterization and auto calibration setup. The Comparator offset, channel mismatch/offset, and phase skew calibration are done in the foreground. The automatic measurement script running on PC captures the ADC output data from the logic analyzer, calculate the error and update the on-chip programable scall cells code, after several times iteration the calibration setting converges to optimum

56
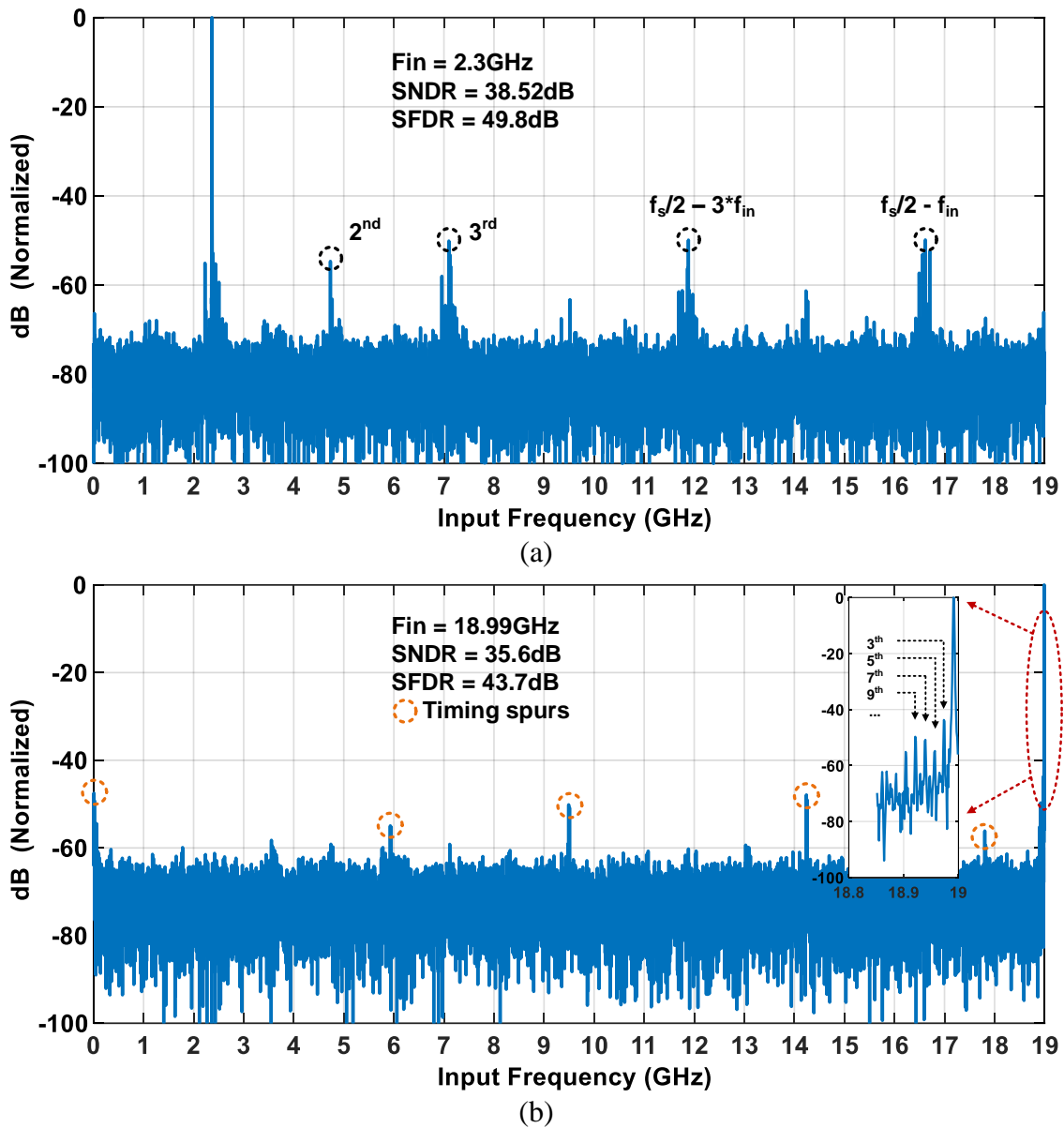
Fig. 4.16. ADC DFT results with (a) low frequency input, (b) Nyquist input

For the comparator calibration, the ADC input is set to the dc common mode, and each comparator is selected by MUXs and monitored from real-time scope. A comparator's output is averaged and the calibration DAC code is adjusted automatically until this average close to 0.5, which implies that the comparator is metastable. The
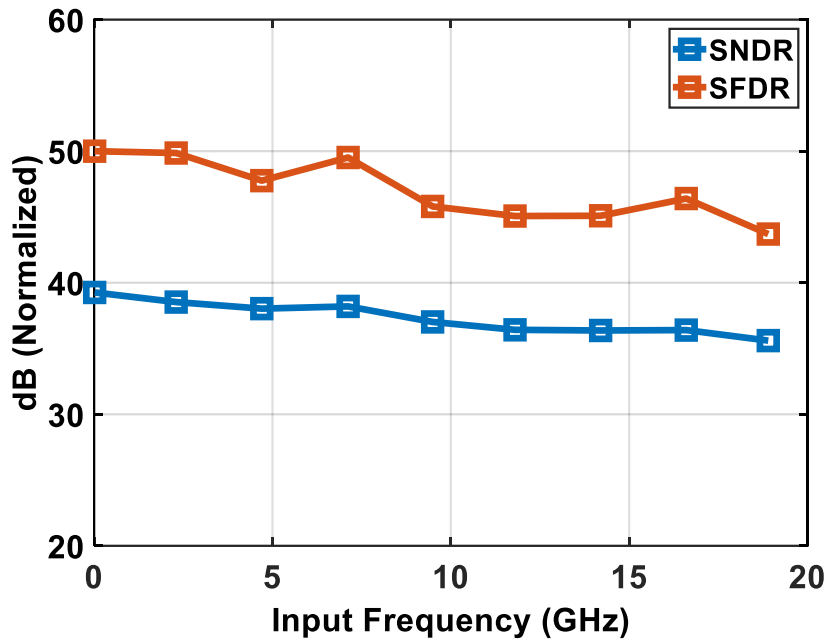
(a)
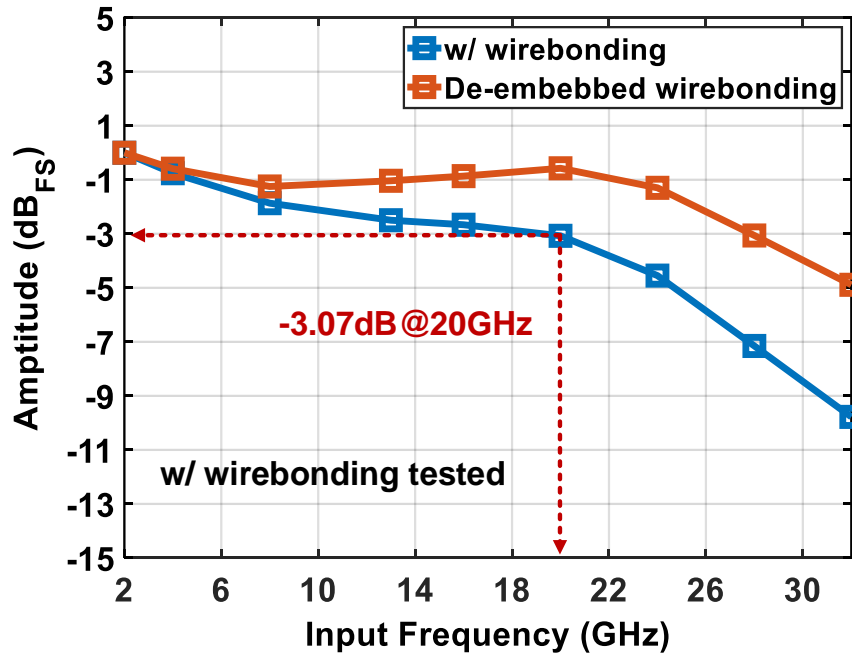
(b)

Fig. 4.17. (a) ADC SNDR and SFDR vs. input frequency, (b) ADC input frequency response

channel gain and skew calibration is performed thru sine fitting algorithm [], which

calculate the amplitude, offset, and phase of each unit-ADC output when the input is a

Table 4.5 Time-Interleaved ADC Performance Summary.

References	ISSCC'18 [12]	JSSC'18 [13]	CICC'17 [27]	ISSCC'19 [28]	JSSC'16 [29]	**This Work**
Technology (nm)	14	28	28	7	16	**22**
ADCs/Interleaver Supply (V)	0.8/0.9	0.95/±0.9	0.95/0.95	0.9/0.9	0.9/0.9	**0.85/0.9**
Sampling Rate (GS/s)	72	56	28	30	28	**38**
Channels	64	64	64	32	64	**32**
Architecture	8b -TI-SAR	8b -TI-SAR	8b -TI-SAR	7b-TI-SAR	8b-TI-SAR	**7b -TI-Pipe-SAR**
3 dB Bandwidth (GHz)	21***	31.5	NA	NA	NA	**20**
SNDR@$f_{in,low}$ (dB)	39.3	40.5	37	33*	40.9*	**39.26**
SNDR@$f_{in,Nyquist}$ (dB)	32.7 @27G	33	34	32* @14G	31.5*	**35.6**
Total/Interleaver Power (mW)	235/77	702/291	165/NA	79.65/NA	280/NA	**119.7/37.05**
FoM@ $f_{in,low}$ (fj/conv-step)	43	145	102	81.6**	110.4	**41.9**
FoM@ $f_{in,Nyquist}$ (fj/conv-step)	121	344	140	83.6**	325.7	**64.05**
Area (mm^2)	0.15	0.878	0.24	0.078	NA	**0.107**

* Measurements with CTLE front-end
** Added the clock generation power
*** Probe Testing

sinewave. Then the skew calibration DAC and on-chip reference DAC are adjusted automatically until each unit-ADC output has roughly same amplitude and equally spaced phase. And the offset of each unit-ADC channels is subtracted off-chip.

The unit-ADCs and the multi-phase clock generator are powered by 0.85V supply, consumes 82.65 mW. The interleaver which includes input 1st rank buffer, 1st rank T/H and 2nd rank buffer are powered by 0.9V supply, cosumes 37.05 mW.

A sinewave histogram technique [25] is utilized for ADC static characterization. Fig. 4.15 shows that the aggregated maximum DNL and INL after calibration are +0.2/-0.39 LSB and +0.71/-0.55 LSB, respectively.

Fig. 4.16 shows the 32768-points DFT of the decimated (1089X) ADC output after calibration when sampling low and Nyquist frequency sinusoidal input at 38GS/s. At low frequency, the time-interleaved ADC achieved SNDR and SFDR of 38.52 dB and 49.8dB, the performance main limited by the thermal noise, remaining gain mismatch spurs and the unit-ADC non-linearity due to the incomplete settling of the pipeline gain stage. The spur at $f_s/2\text{-}f_{in}$ and $f_s/2\text{-}3f_{in}$ caused by the aliasing and a relatively higher third harmonic distortion in one of the channels [26]. At Nyquist, the SNDR and SFDR are 35.6dB and 43.8dB, spurs coming from the remaining skew, bandwidth mismatch and non-linearity, as well as jitter limits the performance. The harmonics at the high frequency input are mainly caused by the interleaver sampling switch since the input signal tracking of the bootstrapped switch is less accurate at high frequency.

Fig. 4.17(a) shows the measured SNDR and SFDR with various input frequencies at 38GS/s, the SNDR and SFDR drops 3.7dB and 6.3dB at Nyquist, respectively. The measure 3dB bandwidth of the time-interleaved ADC is 20 GHz, as shown in Fig. 23(b), which includes insertion loss from wire-bonding, and de-embedding the wirebond parasitics show that 28GHz bandwidth is possible.

Table 4.1 summarizes the time-interleaved ADC and compares this work against previous 7-8b ADCs operating at ≥28GS/s. Total ADC power consumption is 119.7mW, with 82.65mW dissipated in the pipelined-SAR unit ADCs and clock generation circuitry operating on a 0.85V supply and 37.05mW from the 0.9V proposed interleaver, also achieving 64.05 fj/conv-step FoM at Nyquist input. The interleaver consums the least

power and achieves 20GHz 3-dB bandwidth with wirebonded chip-on-board testing. And the totally area is only 0.107 mm^2 with 22nm CMOS process.

4.5. Conclusion

This chapter has presented a 32-way 38 GS/s 7-bit time-interleaved ADC. A low power, high speed unit-ADC design is realized by combine several techniques, including a novel low-overhead OLS settling technique in the dynamic residue amplifier, pipelined-SAR architecture, parallel comparators, and asynchronous SAR. The proposed speed-enhanced bootstrapped switch with the lows-duty-cycle sampling clock significantly saves the interleaver power and achieves high 3-dB bandwidth without limiting the input common mode. Overall, the high input bandwidth and SNDR enabled by the proposed interleaver and pipelined-SAR unit ADC with OLS settling allows for significant improvement in the Nyquist rate FoM.

5. A JITTER-ROBUST 40GB/S ADC-BASED MULTICARRIER RECEIVER FRONT END IN 22NM FINFET[*]

Demand for increased data-rates in serial link transceivers calls for innovative architectures capable of overcoming communications impairments such as limited channel bandwidth and stringent jitter specifications. While mixed-signal and ADC-based receiver architectures that utilize simple pulse amplitude modulation (PAM) can take advantage of technology scaling, it is becoming increasingly difficult to deal with the extremely short baseband pulse widths. This chapter presents a wireline receiver front-end (RXFE) architecture that supports multicarrier signaling to provide a ~3X relaxation in clock jitter requirements.

5.1. Receiver front-end architecture

Fig. 5.1 shows the implemented RXFE architecture and the multicarrier signal power spectral density, where orthogonality is leveraged to allow for band overlapping and improved spectral efficiency. Assuming the channel bandwidth is occupied by N channels, $\Delta_f = \frac{W}{N}$, and the symbol rate $\frac{1}{T}$ in each subchannel is chosen as a multiple of the channel separation Δ_f, then, the subcarriers will be orthogonal over a symbol interval T, independent of the relative phase relationship between subcarriers (ϕ).
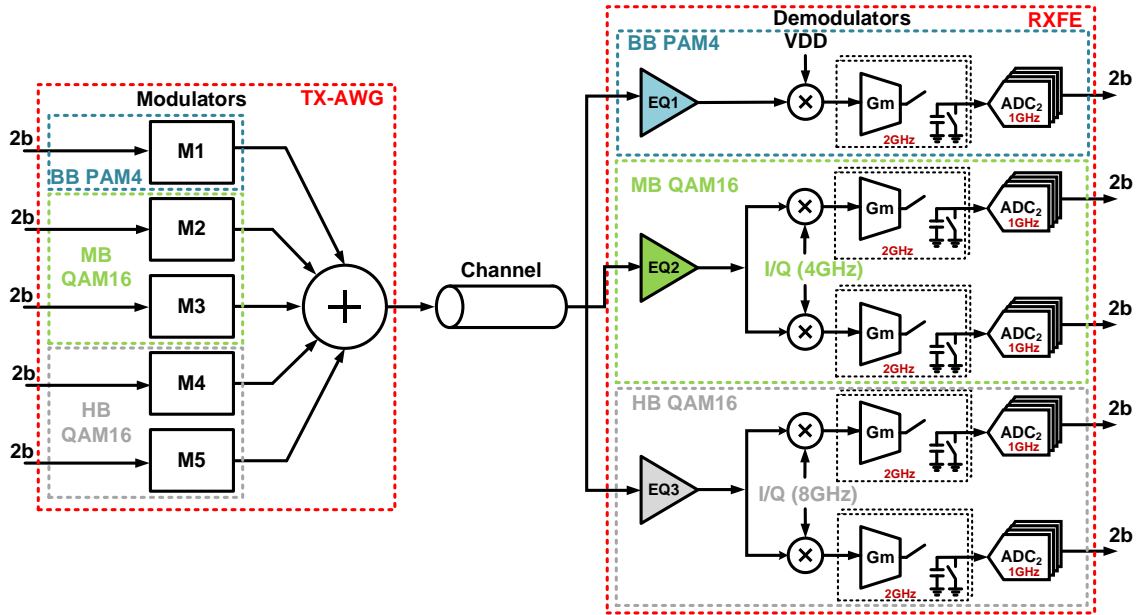
Fig. 5.1. Multicarrier RXFE architecture
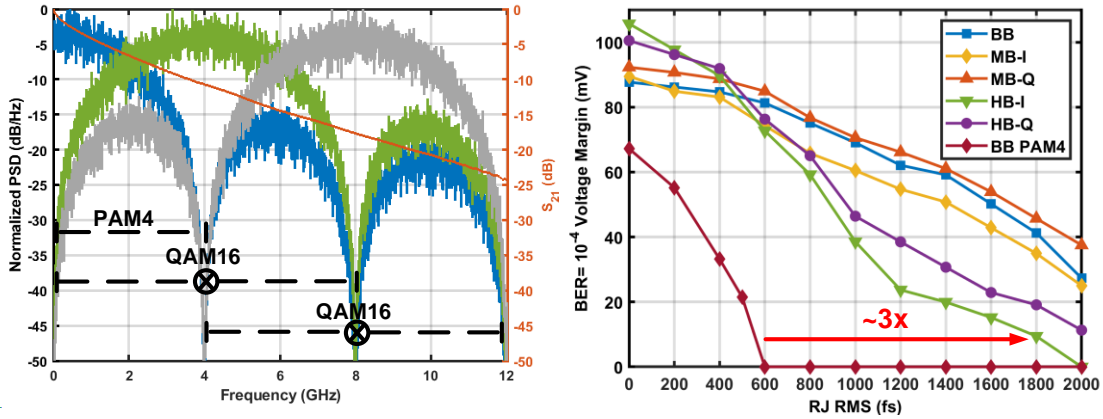
Fig. 5.2. Multicarrier RXFE modeling results

$$\int_0^T \cos\left(2\pi f_k t + \phi_k\right) \cos\left(2\pi f_j t + \phi_j\right) dt = 0$$

The multicarrier signal is formed by three bands to support a total 40Gb/s data rate. This includes baseband (BB) PAM4 operating at 4GS/s and mid-band (MB) and high-band (HB) that both carry 4GS/s QAM16 on 4GHz and 8GHz orthogonal carriers,

respectively. This 4GS/s rate has a symbol duration that is 5X longer than a conventional 20GS/s baseband PAM4 signal. Thus, the proposed architecture offers jitter robustness that has been evaluated through system-level simulations with different clock jitter amounts on both the receiver LO down-conversion and sampling clocks when operating over a channel with 20dB loss at 10GHz. The modeling results in Fig. 5.2 show that the proposed multicarrier system which can tolerate up to 1.6psrms jitter, whereas a BB PAM4 system cannot tolerate more than 600fsrms at a BER=10-4.

5.2. Schematic of the receiver front-end

As shown in Fig. 5.3, after the input T-coil termination the multiband signal passes through three parallel continuous-time linear equalizers (CTLEs) designed to optimally equalize each of the bands and relax RXFE linearity requirements. The BB CTLE drives a single segment consisting of a dummy mixer, integrating sinc filters, and 4-way time-interleaved ADC, while the MB and HB CTLE both drive two I/Q segments with the mixers switched with the 4GHz and 8GHz LO signals, respectively. Inverter-based CTLE structures with two signal paths are utilized [37], with the top branch low-pass response subtracted from the bottom path all-pass response to form a high-pass characteristic. The advantage of using this architecture lies on the ability to set equal transconductances for the top and bottom branches to significantly attenuate the low-frequency component of the multiband signal. This results in a more optimal AC response, improved linearity, and lower output-referred noise for the MB and HB segments. The RXFE sinc filters are implemented with resettable integrators built with dynamic amplifiers with common-restoration and programmable source degeneration resistances for gain control.
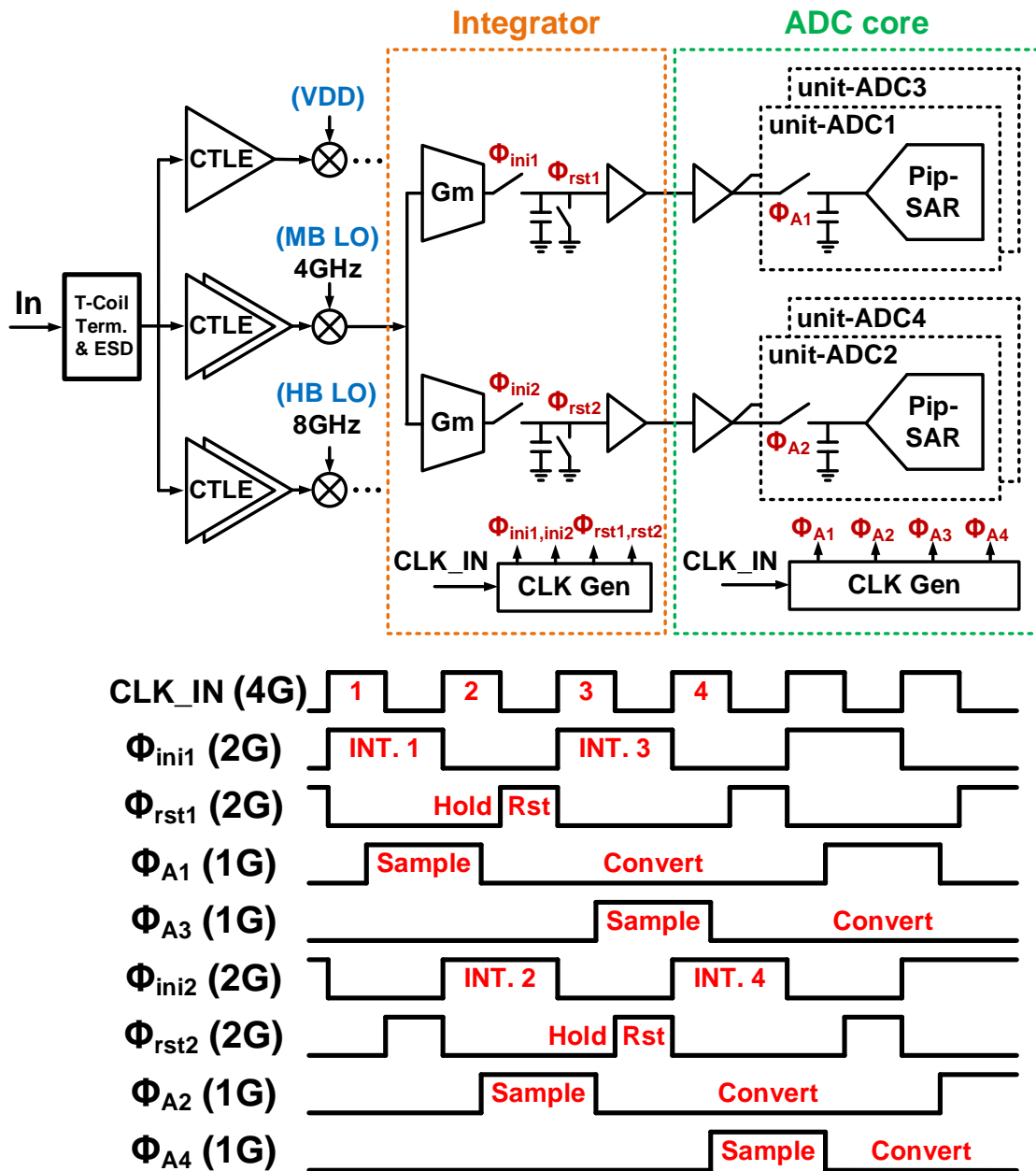
Fig. 5.3. RXFE schematic and timing diagram

The Fig. 5.3 timing diagram shows the integrator operation and interface with the 4-way time-interleaved ADC. The integrator in each segment operates in a 2-way time-interleaved manner to allow for an integrator reset cycle. In this case, ϕ_{ini1} going high marks the start of the integration period. The clock ϕ_{A1} will go high right after this to start
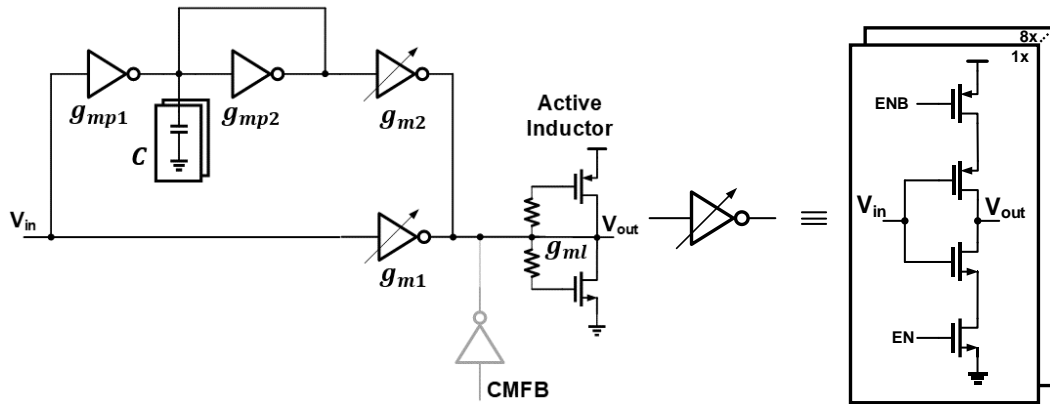
Fig. 5.4. Inverter-based CTLE and programmable inverter schematic

tracking the output and then perform sampling after ϕ_{ini1} goes low. The 25% percent duty

cycle ϕ_{rst1} creates an integrator hold phase that relaxes the timing requirement for this ADC

sample clock. The integrator capacitor is then reset when ϕ_{rst1} goes high. Each 7-bit 1GS/s

unit ADC is formed by a pipelined-SAR structure with an output level shifting (OLS)

settling technique [20] for low power and high-speed operation. 4-bits are converted in

both pipeline stages, with 1-bit redundancy between the two stages to relax the gain, offset,

and reference settling requirements. Both stages employ parallel comparators that are

asynchronously activated sequentially for each conversion step, eliminating the

comparator reset delay and offering significant speed-up.

5.2.1. Schematic of CTLE

As it can be seen in Fig. 5.4, an inverter-based structure is chosen for the CTLEs

[37], where the NMOS and PMOS transistors operate as transconductors driving active

inductors for bandwidth extension. In this structure there are two signal paths, the top-path

that consist of a Gm-C low-pass filter followed by a programmable transconductance that
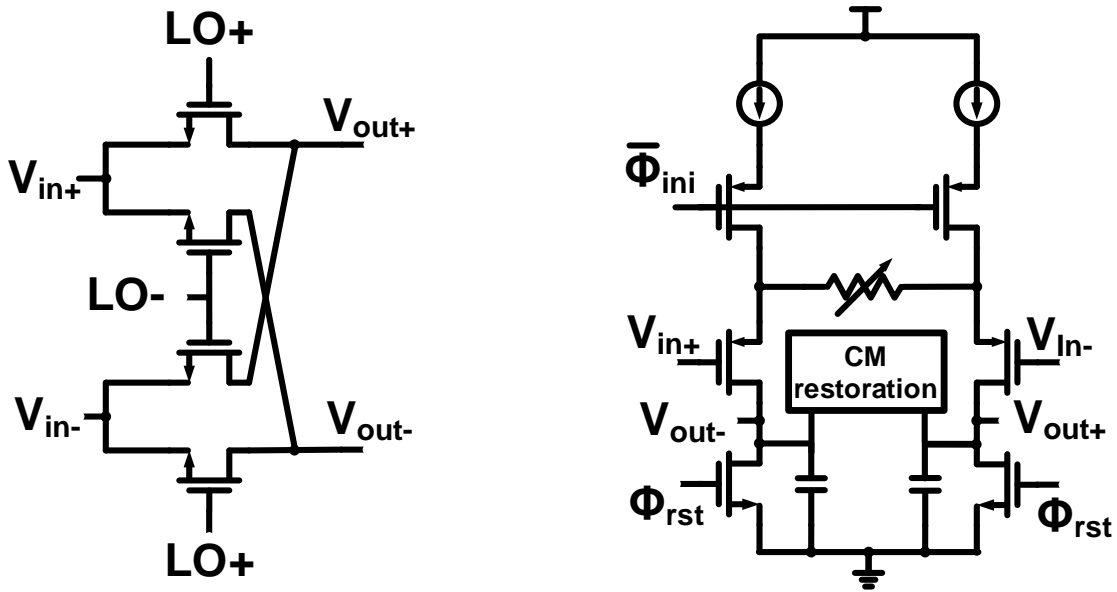
Fig. 5.5. Double-balanced passive mixer and resettable PMOS integrator schematic

would subtract from the all-pass bottom-path. The resulting high-pass filter transfer function of the CTLE is defined by the following equation:

$$-\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ml}} - \frac{gm_2}{g_{ml}}\frac{g_{mp2}}{g_{mp1}}\frac{1}{1 + \dfrac{SC}{g_{mp1}}}$$

The three CTLEs were designed by using a 1 V power supply and consume a total of 64 mW. For this front-end design, the LF, MF and HF CTLEs are peaking at 2, 6, and 10 GHz respectively. The LF CTLE uses one of these stages followed by a buffer, the MF and HF CTLE uses two of them cascaded, and a buffer.

5.2.2. Schematic of integrator and mixer

Given its low noise and high-linearity, passive double-balanced mixers are used. Thereafter, resettable PMOS integrators with degeneration resistor for gain programmability and enhanced linearity are used. The integration of the symbols on each channel is performed in a 2-way interleaved fashion, while one integrator is resetting, the
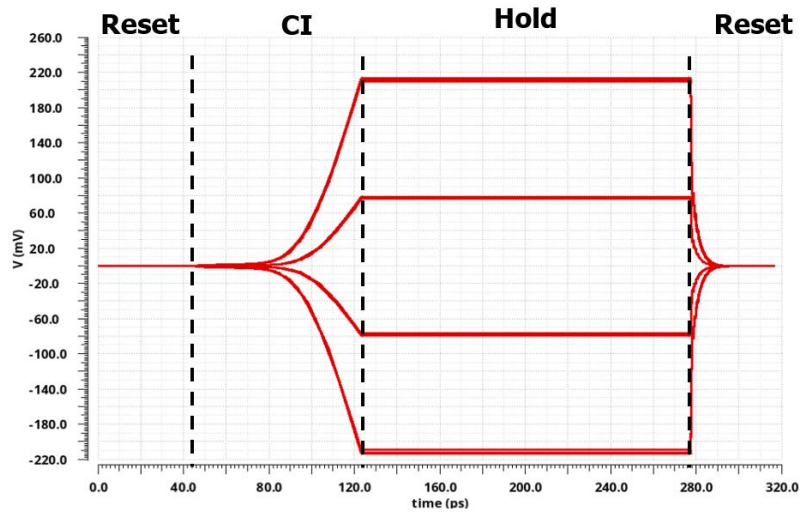
Fig. 5.6. Integrator output with PAM-4 signal input

other is integrating. Since the sub-channel ADC is also 2-way interleaved, each integrator

is connected to a sampler. The schematics of the mixer and integrator are shown below.

As it can be seen in the following figure, the designed analog front-end linearity is

evaluated. The left-hand side of the figure shows the 1dB compression point of the CTLE,

which occurs when the output signal is about 800 mVppd. On the right-hand side, the

PAM-4 eye diagram at the output of the second rank sampler of one of the channel's ADC

is shown in Fig. 5.6. This eye-diagram has a ratio-level-mismatch (RLM) higher than 90%.

5.2.3. 4-way time interleaved ADC design

For a 40 Gb/s 5-channel system, the ADC sampling rate is 4 GS/s. The 7-bit 4GS/s

ADC is based on 4-way time-interleaving of a Pipe-SAR ADC with output-level-shifting

(OLS) technique [20] for enhanced residue amplifier settling. Fig. 5.7 shows the block

diagram of the interleaving architecture. There are two stages of the time-interleaving. The

first stage is a two-way time interleaved T/H, where the input signal is tracked and held

by two phases of 2 GHz clock. The second stage is a 4-way time interleaved 1GHz unit-

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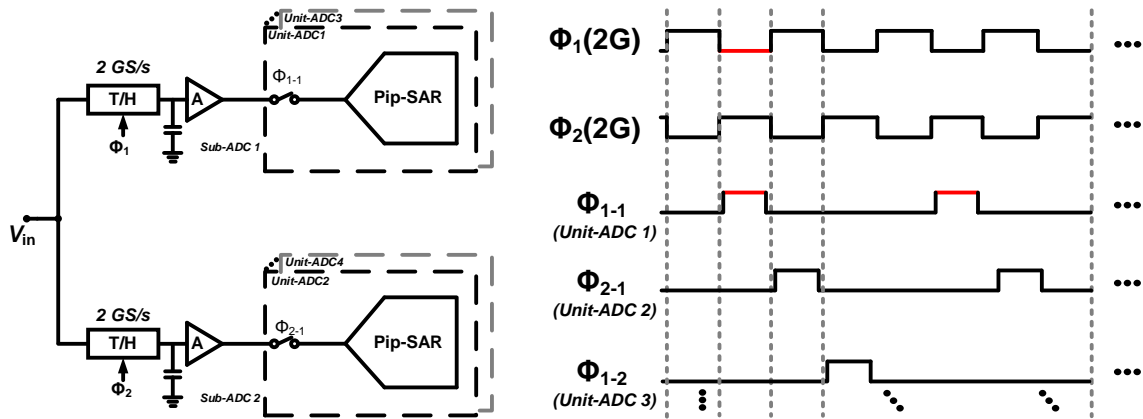
Fig. 5.7. Architecture and timing diagram of the 4 GS/s time-interleaved ADC

ADC, where the held signal from the first stage is further sampled on the CDAC and converted into digital code. A unit gain buffer is placed at the output of each T/H to sequentially drive parallel unit-ADCs.

5.3. Multi-Phase Clock generator

Fig. 5.8 shows the RXFE clock generation circuitry that generates the HB and MB LOs and the 10 input clocks for the integrators and ADC local clock generation blocks in each segment. A 16GHz differential clock input passes through a CML divider and CML-to-CMOS converters to generate 4-phase 8GHz clock signals for the HB LO signals. A subsequent CMOS divider generates 8-phase 4GHz clock signals, with four of these phases used for the MB LO signals. Additionally, these eight 4GHz clocks signals are provided to 10 6b phase interpolators to generate the clocks for the integrators and ADCs with independent sampling phase control. Phase mismatches between I and Q LO signals are compensated with skew calibration blocks consisting of distribution buffers that have digitally controlled capacitive loading. To verify the proposed RXFE jitter robustness, the distribution buffers of the LO and integrator/ADC clocks operate on a power domain with

69
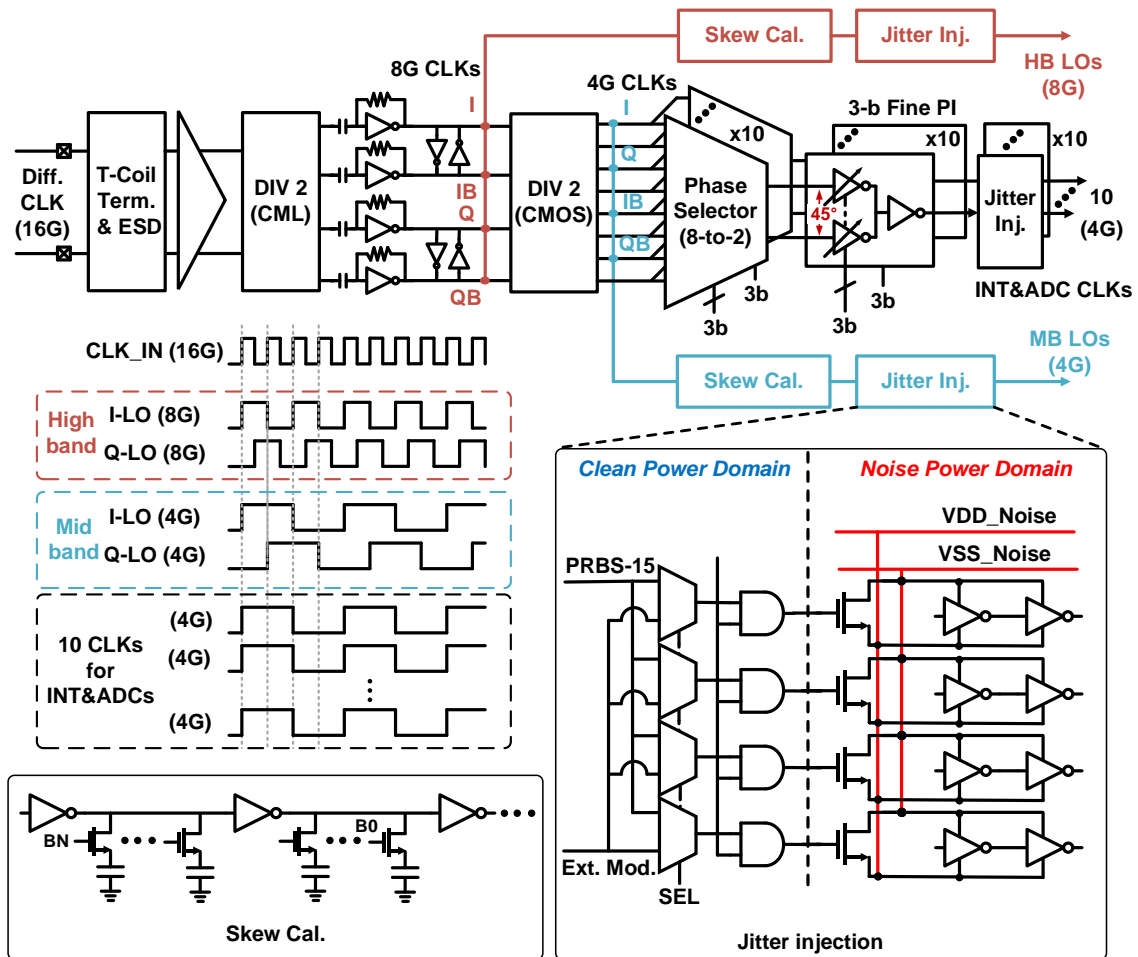
Fig. 5.8. RXFE clock generation

programmable noise injection. Large shunting NMOS transistors are driven by either an internal PRBS generator or an external signal to provide jitter with varying frequency content.

5.4. Experiment Results

The 22nm FinFET die micrograph is shown in Fig. 5.9, the entire RXFE occupies 0.84mm2 when the input T-coil and clock buffer inductors are included. The CTLE, mixers, and integrators occupy 102um X 225um of this area, while the ADCs consume 150um X 441um. Fig. 5.10 shows the DFT from one of the decimated (621x) 4-way time
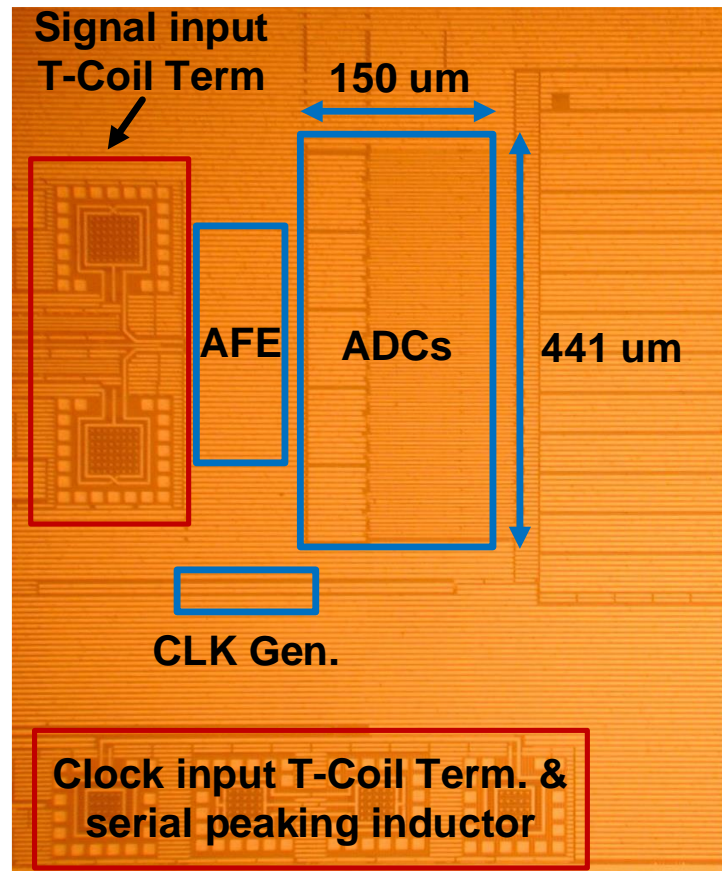
Fig. 5.9. RXFE Chip micrograph

interleaved ADC outputs when sampling a low-frequency input at 4GS/s, with an achieved

SNDR and SFDR of 33.7dB and 42 dB, respectively. The ADC Nyquist rate ENOB

through the entire RXFE is 4.2b and 4.53b when the RXFE is de-embedded. The

frequency response of the CTLEs are measured from the ADC output using single-tone

inputs, with the BB, MB, and HB CTLEs achieving a highest normalized peaking of 8dB,

7dB, and 3dB, respectively. Fig. 5.11 show RXFE measurement results with a 40Gb/s

multiband input signal with independent PRBS15 patterns in the bands generated with a

Keysight M8195A AWG with an 800mVppd total swing. This is passed through a channel

with 20dB insertion loss at 10GHz (conventional baseband PAM4 Nyquist) and data is
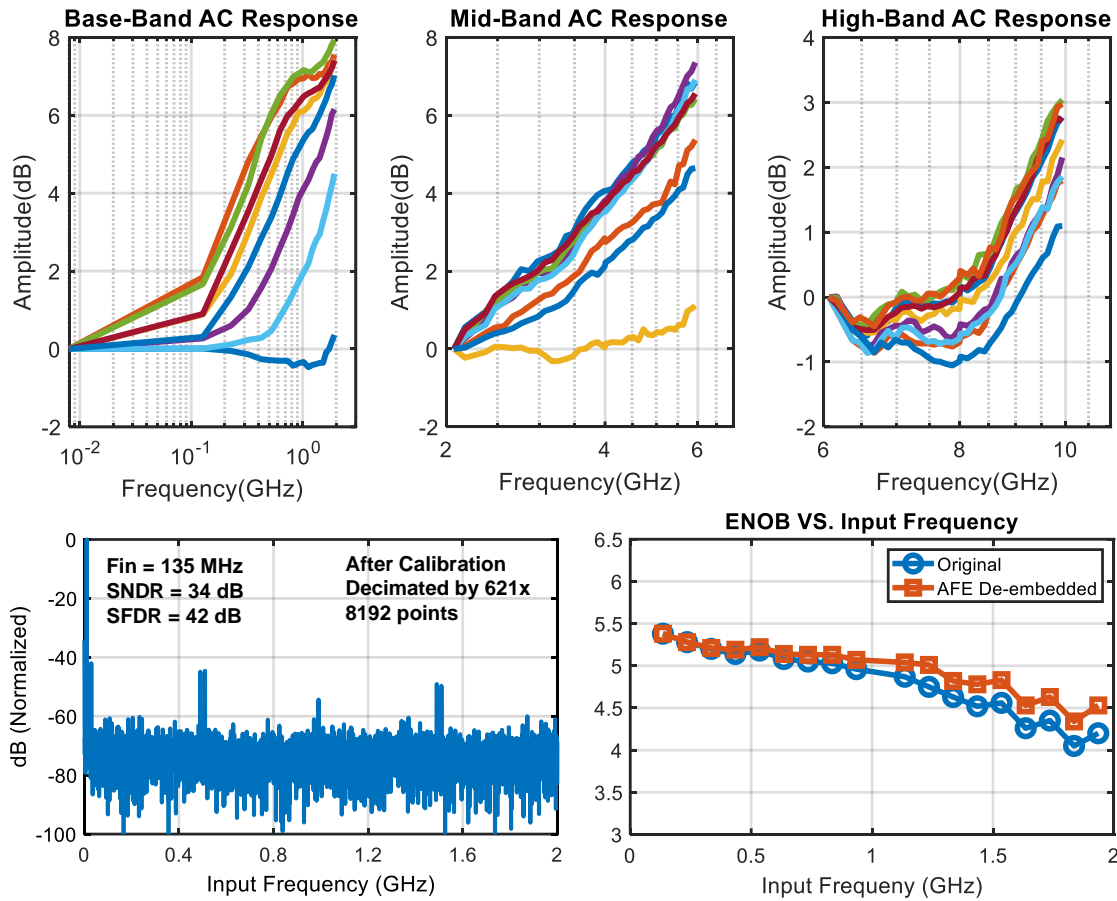
Fig. 5.10. CTLE response of each band, ADC spectrum with a low frequency input, and ENOB vs. input frequency

collected with and without jitter added. For the maximum 1.6psrms jitter injection, the BB channel has an average voltage margin of 24 ADC codes at a BER=10^{-5} and the MB and HB constellations have a respective EVM of 20.4dB and 18.8dB that translates to BERs of 10^{-6} and 3.5×10^{-5}. These constellations suffered a respective EVM degradation of 0.5dB and 0.8dB with respect to the no jitter added case.

5.5. Conclusion

This chapter has presented a jitter robust multi-carrier 40Gb/s receiver front-end. Table 5.1 compares this RXFE with other ADC-based wireline RXFE that utilize

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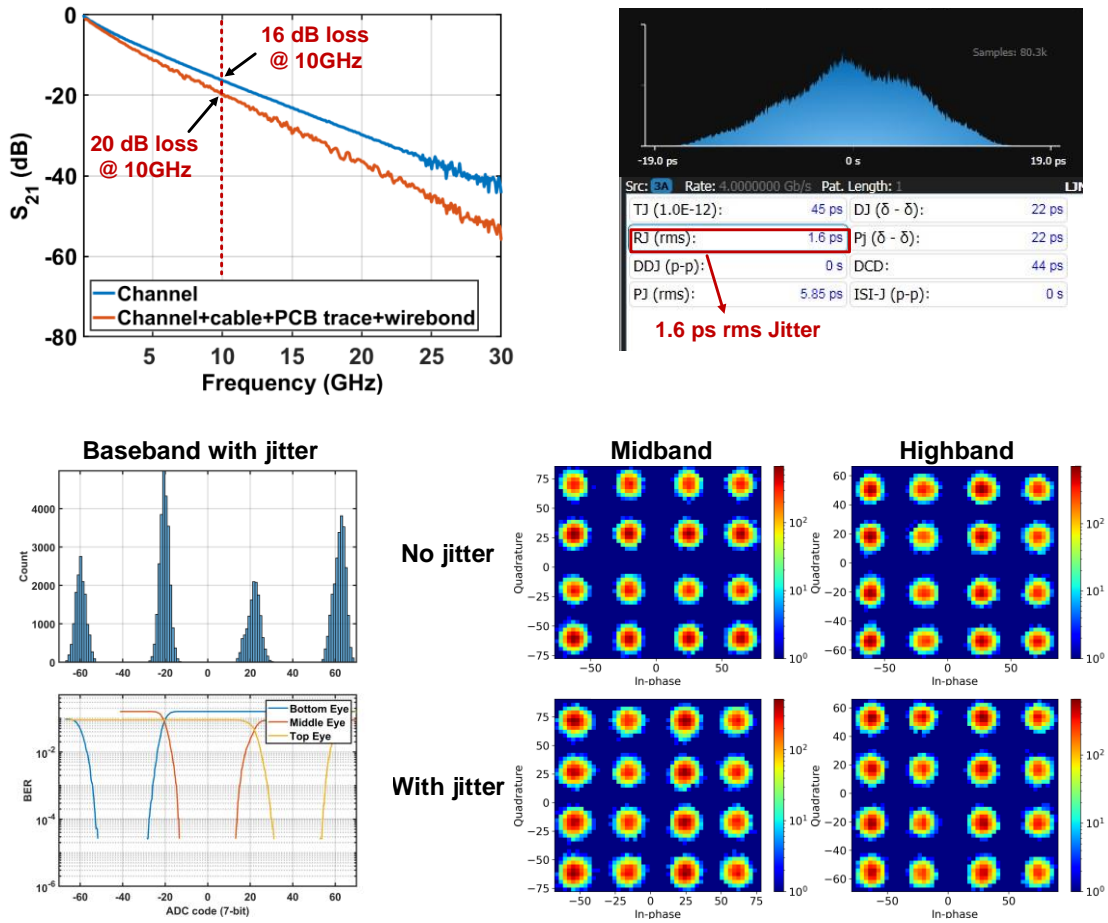
Fig. 5.11. Channel insertion loss, jitter measurement, and measured PAM4 and QAM16 constellations.

conventional PAM4 and multi-tone signaling. The proposed multicarrier RXFE can

operate with the highest 1.6psrms jitter and achieves 3.05pJ/bit power efficiency.

Table 5.1 RXFE Performance Summary.

Specification	LaCroix ISSCC 2019	Ali ISSCC 2019	Kim ISSCC 2019	Upadhaya ISSCC 2018	Wang ISSCC 2018	This Work
Technology	7 nm FinFET	7 nm FinFET	14 nm FinFET	16 nm FinFET	16 nm FinFET	**22 nm FinFET**
Modulation	PAM-4	PAM-4	64-QAM DMT	PAM-4	PAM-4	**Multicarrier**
Power Supply (V)	0.75, 0.8, 1.2	0.8, 1	0.7, 0.75, 0.8	0.85, 0.9, 1.2, and 1.8	0.9, 1.2	**0.85, 0.95, 1.2**
Data Rate	60 Gb/s	56 Gb/s	56 Gb/s	56 Gb/s	64.375 Gb/s	**40 Gb/s**
Fs (GS/s)	30	28	22.4	28	32	**5 x 4**
ADC Structure	TI-SAR	TI-SAR	TI-Pipe-SAR	TI-SAR	TI-Folding Flash	**TI- Pipe-SAR**
Pre-Equalization	CTLE	CTLE	No	CTLE	CTLE	**CTLE**
ENOB @ Nyquist	N/A	4.74 bits	N/A	4.43 bits	4.33 bits	**4.5 bits**
Area	0.84 mm^2	0.32 mm^2	0.26 mm^2	N/A	0.16 mm^2	**0.84 mm^2**
Max. Compensated Channel Loss	32 dB @ 14 GHz	40 dB @ 14 GHz	28 dB @ 14 GHz	32 dB @ 14 GHz	30 dB @ 16 GHz	**20 dB @ 10 GHz**
RMS Jitter	160 fs	225 fs	N/A	180 fs	162 fs	**1.6 ps**
BER	< 1e-6	< 1e-5	< 2e-4	< 1e-12	< 1e-4	**< 1e-4**
AFE + ADC Power	303 mW	180 mW	93.2 mW	N/A	283.9 mW	**122 mW**
Power Efficiency (pJ/bit) AFE + ADC	5.05	3.2	1.6	5.8	4.44	**3.05**

6. CONCLUSION AND FUTURE WORK

6.1. Conclusion

ADC-based receiver are becoming more common in wireline receivers due to the enabling of powerful and flexible digital processing for equalization and easier support of higher-order modulation schemes. However, the ADC-based receivers are usually more power hungry compare with mixed-signal receivers due to the conventional SAR-based high speed time-interleaved ADC front-end. Moreover, as the ever-increasing wireline communication data rates climbs 100+Gb/s, sampling clock jitter places fundamental performance limitations on common baseband PAM4 ADC-based receivers, necessitating clock generation and distribution circuitry that achieve rms jitter of a few hundred femtoseconds. And this jitter issue will become more severe for the future 200+Gb/s design. This dissertation presents three different works for addressing these challenges.

The first research focused on the low power and high-speed unit-ADC design that can reduce the interleaving factor for a given effective sampling rate, resulting in smaller area and an overall simpler time-interleaved ADC design. Presents a single channel 8-bit pipelined-SAR ADC that utilizes a novel low-overhead OLS settling technique in the dynamic residue amplifier. A low power design is realized by combining this technique with the use of parallel comparators in the two asynchronous pipeline stages to allow for 1.5GS/s operation with a low 0.8V supply voltage and achieves an FOM of 16.7fJ/conv.-step.

The second research focused on the implementation of a low power and high bandwidth time-interleaved ADC which avoid the extra amplitude equalization for the

ADC input bandwidth therefore save the following DSP power. The 38GS/s 7-bit time-interleaved ADC prototype utilizes previous mentioned unit-ADC and a high-bandwidth 8-way interleaver architecture based on a proposed speed enhanced bootstrapped switch. which shows higher operation speed and better EBON with high frequency input. The time-interleaved ADC achieves 41.9fj/conv.-step at low frequency, 64.1fj/conv.-step at Nyquist, and has a 20GHz 3dB bandwidth.

The last research focused on the jitter-robust ADC-base receiver design. Presents a novel frequency-domain wireline ADC-based receiver front-end (RXFE) that supports multicarrier signaling to provide a ~3X relaxation in clock jitter requirements. Also the previous mentioned pipeline-SAR unit-ADC and speed enhanced bootstrapped switch are utilized. A 40Gb/s RXFE prototype can operate with the highest 1.6psrms jitter and achieves 3.05pJ/bit power efficiency.

6.2. Time-domain high-speed ADC design

Recently time-domain ADCs have shown promising speeds for mid-resolution application, because the quantization is performed by the inside flash TDC. Fig. 6.1 shows an 8b time-domain ADC example [42], which consists of a S/H, a VTC, and a two-stage TDC. The S/H adopts bootstrapped switches with cross-coupled compensation for high linearity sampling on an input capacitance of only 45fF (single-ended). The dynamic VTC converts the sampled voltage into a time difference ($S_{P1}<0>$, $S_{N1}<0>$) through a pair of current sources and crossing detectors. The pseudo-differential and discharging features guarantee the high linearity of the VTC. The 8b TDC comprises a 4b pseudo-differential flash TDC (with 1b sign) as the coarse stage and a 5b single ended interpolation TDC
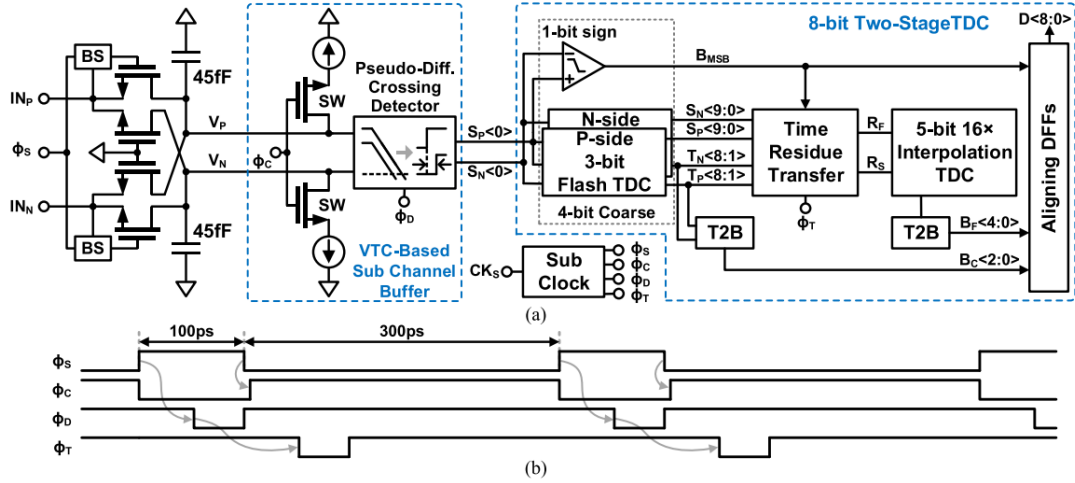
Fig. 6.1. (a) Block and (b) timing diagrams of the 8-bit 2.5GS/s time-domain ADC
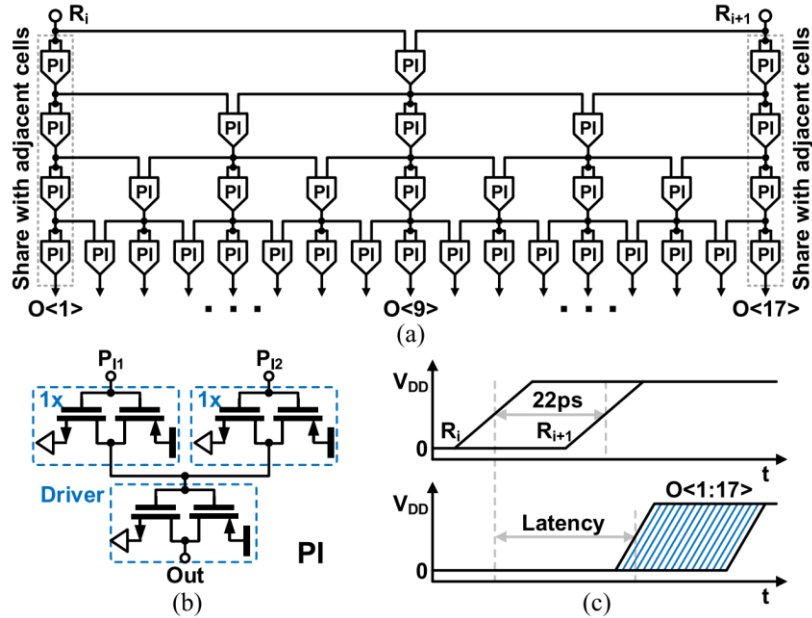
Fig. 6.2. (a) 4-layer 16x time interpolator (b) unit phase interpolator cell (c) Timing diagram of the 16x time interpolator

(with 1b redundancy) as the fine stage. This design successfully implements a 2.5GS/s 8-bit ADC on 65nm CMOS process, and calibration for the comparators is not needed, because the time comparator only needs to compare two signal levels which are VDD and VSS.

However, there is no gain stage between course TDC and fine TDC, the time step for the fine TDC is only 1.375ps. This design utilized a 16x time interpolator for generating the stringent fine time step. As shown in Fig. 6.2, 4 layers and 34 inverter-based phase interpolators (PI) are utilized for one cascade stage and there are two cascade stages in total. Moreover, dummy delay cells and interpolators are added both before and after the quantization cells to shield the terminal effect. Those are results in around 136 PI cells in total, which is power-hungry and could be susceptible to PVT variation on advanced technology. Also, the fine time step could cause comparator meta stabilities.
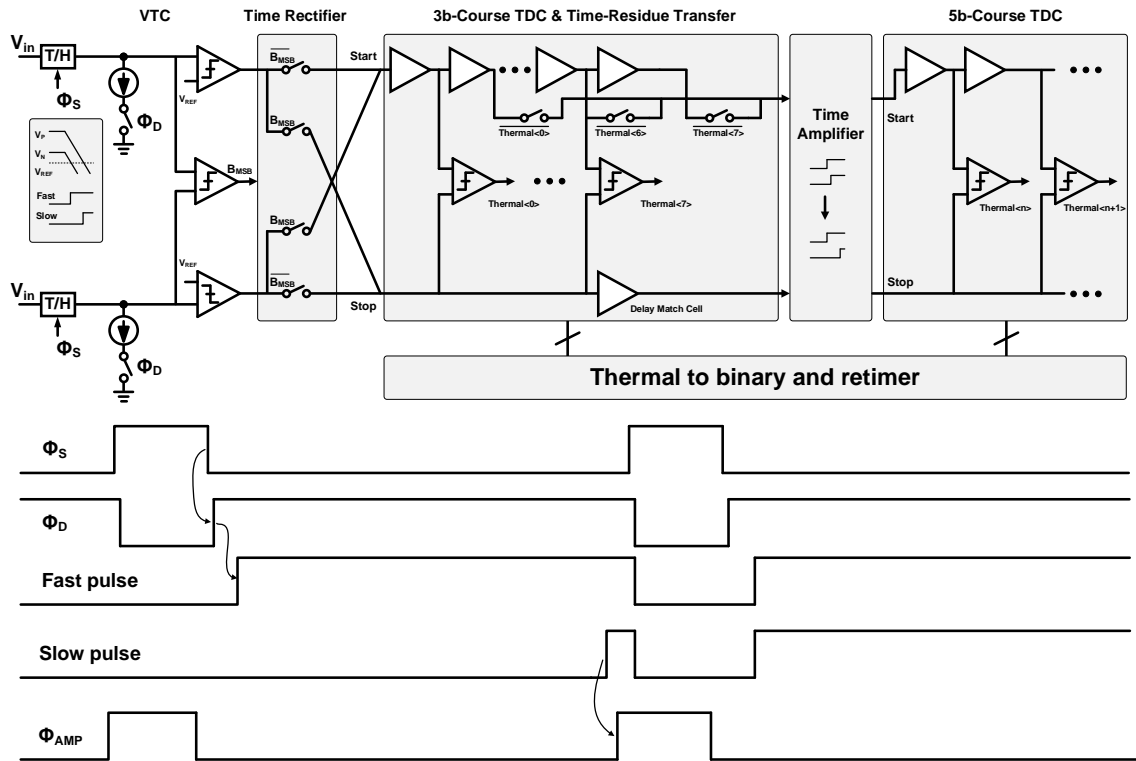
Fig. 6.3. A pipeline time-domain ADC with time amplifier, and timing diagram

Fig. 6.3 shows a proposed 8-bit pipeline time-domain ADC with time amplifier (TA) that amplifies the time residue from the 3-bit first stage flash TDC. The residue TA increases the second stage LSB step by a factor of residue gain, and therefore enables a

course 5-bit 2nd stage flash TDC which could be implemented by simple digital buffers. According to the timing diagram of Fig. 6.3, T/H is clocked by Φ_S, once the input voltage has been sampled by bootstrapped switch, Φ_D enables a pair of current sources which discharge the voltage on the sampling capacitors. Then the following crossing detector converts the voltage difference to time difference, which is the gap between fast and slow pulse. Also, a sign bit comparator is placed right after the T/Hs and triggered by Φ_D. The sign bit saves 1 bit resolution of the first stage TDC and controls the time rectifier that forces the fast pulse always connect to the delay line. The residue time amplifier is enabled by the Φ_{AMP} clock that is located after the slow pulse, and there is 1-bit redundance between two stages relax the gain and delay mismatch.

A low power TA with enough gain and linearity is essential for implementing the system. Fig. 6.4 shows a possible TA design [43] that achieves ~8x gain and 6-bit resolution. Two discharging phases of two capacitors C_X and C_Y (in differential configuration) take place in turn during the amplification. The first one is an early discharging phase between t_1 and t_2 with a large slew rate after the first rising edge of the inputs arrives. For example, if V_{INA}'s rising edge arrives first, it will discharge C_X through M_{1A} and M_{2A} while keeping V_Y at V_{DD}. Then, when the rising edge of V_{INB} arrives, both capacitors will discharge together at an equal but small slew rate through M_{3A}, M_{4A}, M_{3B} and M_{4B}. When the two voltages cross the threshold of two TCDs at t_3 and t_4, respectively, an amplified time difference is generated. The input and output time are

$$t_{in} = t_2 - t_1 = \frac{V_{DD} - V_1}{SR_1} = \frac{V_{DD} - V_1}{\frac{I_{D1}}{C_X}}$$

(a)

(b)
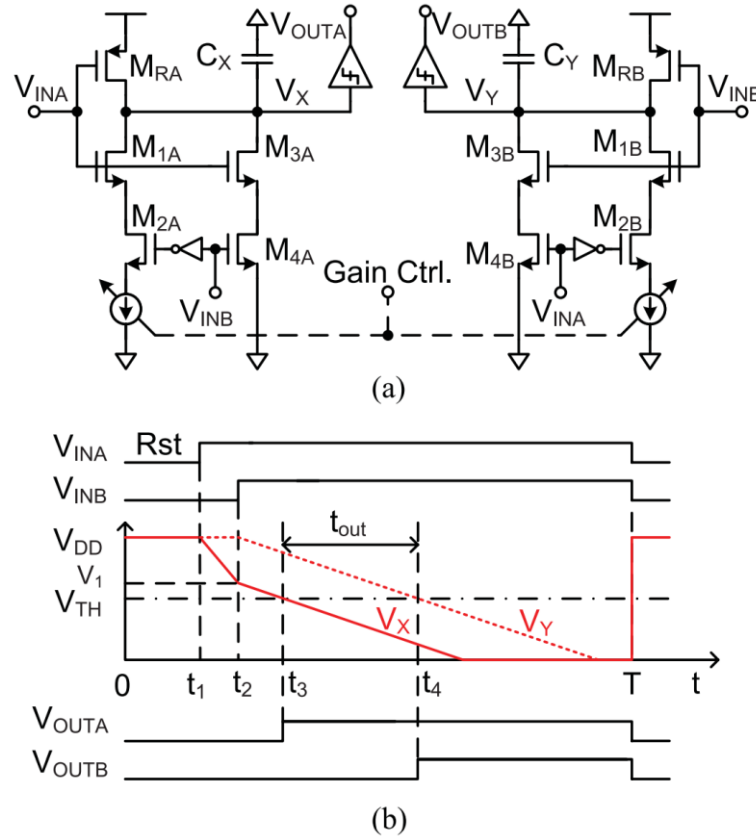
Fig. 6.4. **(a) circuit diagram and (b) timing diagram of the TA**

$$t_{out} = t_3 - t_4 = \frac{\frac{1}{2}V_{DD1}}{SR_2} - \frac{V_1 - \frac{1}{2}V_{DD1}}{SR_2} = \frac{V_{DD} - V_1}{SR_2} = \frac{V_{DD} - V_1}{\frac{I_{D2}}{C_X}}$$

where I_{D1} and I_{D2} are the discharging currents in two phases. So, the gain of the

TA is

$$A_t = \frac{t_{out}}{t_{in}} = \frac{SR_1}{SR_2} = \frac{I_{D1}}{I_{D2}}$$

In summary, the time domain ADC converts the voltage difference to time

difference that quantized by the flash TDC. Compare against the conventional SAR ADC,

it is faster and does not require large area capacitive DAC, reference buffer and comparator

calibration, has potential to realize a high-performance ADC with better energy efficiency.

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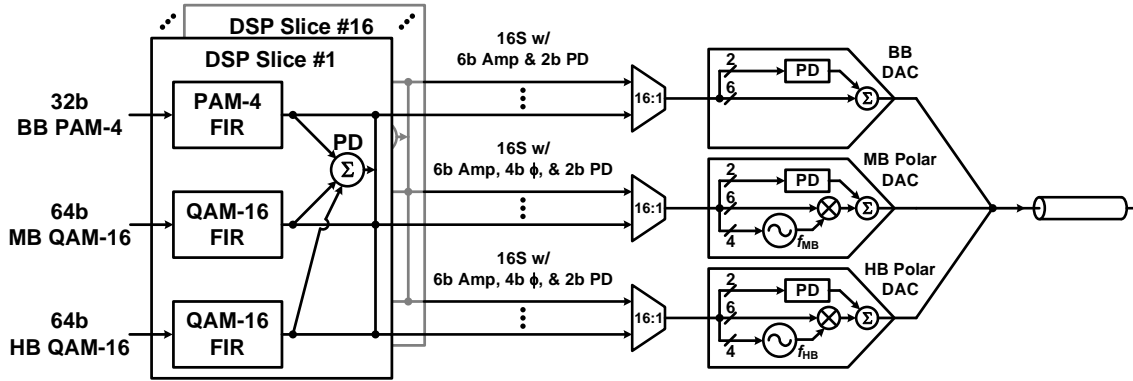
Fig. 6.5. Proposed multi-carrier DAC-based transmitter

6.3. Frequency domain multi-carrier transmitter

As the common PAM-4 transmitter does not support the proposed multi-carrier receiver. A DAC-based transmitter architecture is proposed for transmitting the multi-carrier signal also aims to significantly improve jitter robustness and reduce system equalization complexity. The proposed DAC-based transmitter supports advanced baseband and multi-carrier modulation schemes. The target performance is a low-power multi-carrier DAC-based serial I/O transmitter capable of operating at data rates >100Gb/s. With the inclusion of a multi-carrier receiver and the optimum modulation for a given channel, operation with channels that have more than 30dB loss at an equivalent Nyquist frequency is possible.

Fig. 6.5 shows the proposed multi-carrier DAC-based transmitter with baseband (BB) PAM-4, mid-frequency band (MB) QAM-16, and high-frequency band (HB) QAM-16 modulations. For 64Gb/s data transmission, 160 parallel bits at 400MHz drive the DSP and pass-through FIR filters that are programmable from 1-8 taps. In order to achieve sufficient output stage linearity, the outputs of these filters are summed to generate a parallel multi-bit predistortion code. The outputs of the 400MHz DSP are 3 parallel

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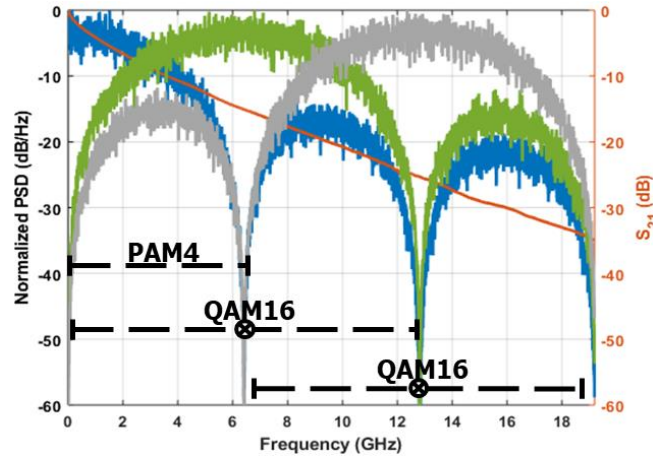
Fig. 6.6. Power spectral density of modulated signal in the proposed architecture and channel loss

streams of 16 symbols that are represented with a multi-bit code, which represents the level of the BB PAM-4 signal and the amplitude of the MB and HB QAM-16 signals, a multi-bit phase code for the MB and HB QAM-16 signals, and the predistortion code. 16:1 serialization is performed on these bits to generate 3 parallel 6.4GS/s codes that drive the polar transmitter output DACs whose outputs are combined in the analog domain for transmission. This architecture provides several benefits. First, each channel is operating at an effective 6.4GS/s sampling/serialization rate, which is significantly lower than the 64GS/s sampling rate required for conventional PAM4 modulation, allowing for close to a 6X improvement in simulated rms jitter tolerance. Second, the up-conversion performed in the MB and HB channels perform mixer-based self-equalization and provide some channel loss compensation, allowing for a reduction in digital equalization complexity. Finally, the polar transmitter output stages provide the ability to support multiple 16-point constellations, such as QAM-16 and APSK-4+12, that improve the back-off energy efficiency.

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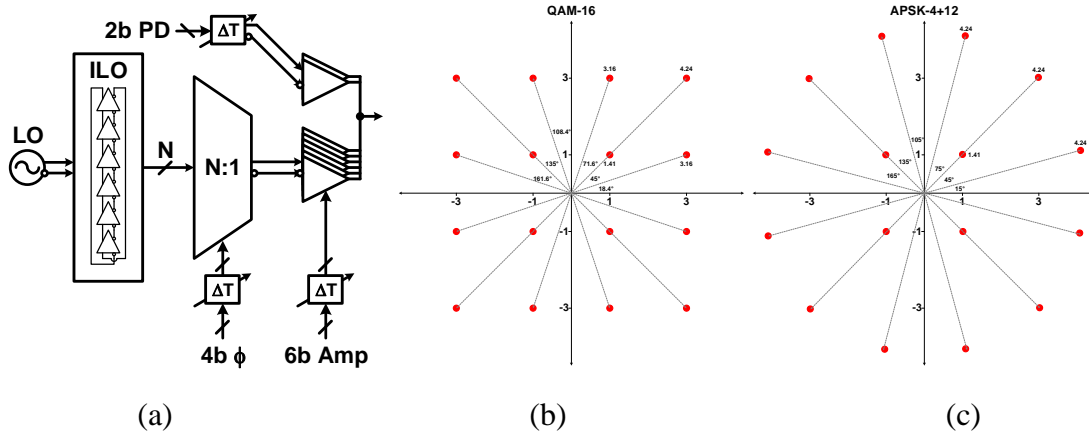
Fig. 6.7. (a) Digital polar output DAC. 16-point constellations: (b) QAM-16 and (c) APSK-4+12.

Fig. 6.6 shows the power spectral density of the modulated signal from a potential 64Gb/s multi-carrier implementation implemented with the BB PAM-4 channel, the MB QAM-16 channel centered at 6.4GHz, and the HB QAM-16 channel centered at 12.8GHz. Orthogonality of the multi-carrier channels is achieved by operating at harmonics of a 6.4GHz carrier.

A block diagram of the proposed digital polar transmitter output stage used in both the MB and HB channels is shown in Fig. 6.7. A given constellation point is realized by first using the digital phase code to generate the desired phase from the high-speed phase modulator. This output phase passes to the output driver where it is scaled by the multi-bit amplitude control to realize the desired constellation point magnitude. This decoupling of the output phase generation and amplitude control simplifies the control of the output magnitude relative to a conventional I/Q QAM modulator where the output phase generation and amplitude is realized by summing modulated I and Q carriers. The proposed polar architecture provides the flexibility to generate multiple 16-point constellations other than the conventional square QAM-16 constellation shown in Fig. 6.7,

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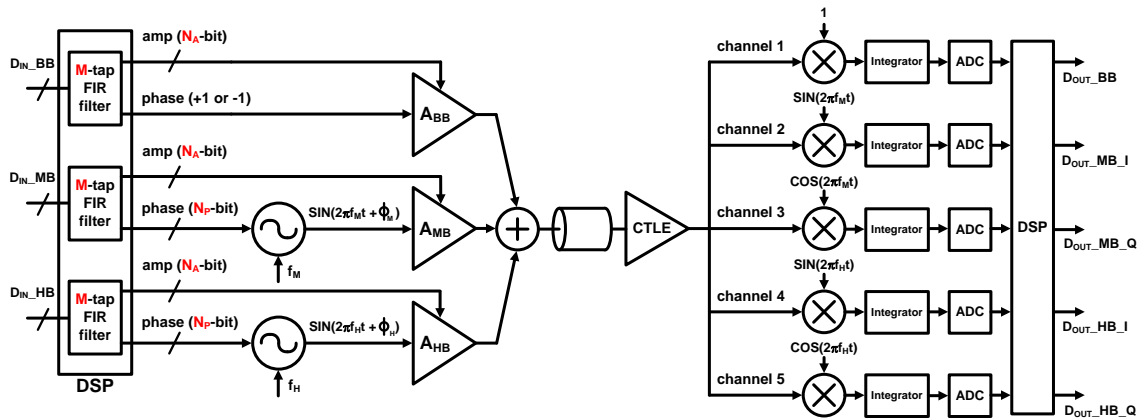
Fig. 6.8. System-level model for multicarrier TX and RX

which has three different output magnitudes. For example, the APSK-4+12 constellation allows all the outer 12 points to have the same maximum magnitude. This lower peak-to-average power ratio allows for relaxed output driver non-linearity and operation at a smaller back-off with reduced spectral regrowing.

The high-speed phase modulator utilizes an injection-locked oscillator (ILO) locked to the desired carrier frequency to generate N multiple clock phases that are selected by a phase mux with the digital phase code. This produces the differential carrier signal at the output driver with the appropriate phase for the desired constellation point.

For transmitter equalization, a segmented lookup table (LUP) approach is planned for the FIR filter implementation in the DSP [44] as shown in Fig. 6.5. An 8-b LUP is used for each tap, with the BB PAM-4 channel having 4 entries per LUP and the MB and HB QAM-16 channels having 16. These tap outputs are summed and quantized for the output stage at each channel. This LUP-based approach will allow the efficient implementation of an FIR filter with a programmable range from 1 to 8 taps.

Table 6.1 Summary of System-Level Design Parameter for 64Gb/s DAC-based Tx.

Data rate	64 Gb/s
Channel loss	> 30 dB at 16 GHz
Jitter requirement	< 1500 fs$_{rms}$
The number of taps (M)	8 taps
Bit resolution of output DAC (N_A)	7 bits
Bit resolution of phase modulator (N_P)	7 bits (>96 phases)

The proposed transmitter (Tx) is verified by using system-level models to verify its operation and to optimize its design parameters. The system-level models implemented by using MATLAB consist of a polar Tx model, a channel model, and a receiver (Rx) model based on a I/Q demodulator using integrators and ADCs (Fig. 6.8). As the channel model, two kinds of channels (30- and 40-dB loss at 16 GHz) are considered. For Rx equalization, a CTLE and a 5-tap adaptive MIMO equalizer in the DSP are used. In the Tx model, the number (M) and the coefficients of FFE taps, the bit resolution (N_A) of the output DAC, and the bit resolution (N_P) for the phase modulator are adjusted to maximize the voltage margin at the Rx output.

From the verification using system-level models, the key design parameters to achieve the target performance in silicon implementation are summarized in Table 6.1. To operate properly with a channel having near 40dB loss at an equivalent Nyquist frequency, at least 8 taps should be considered for the Tx equalization. The required bit resolutions (N_A and N_P in Fig 6.8) for the output DACs and the phase modulator to achieve almost the same performance with the infinite resolution cases are 7 bits, respectively.

(a)

(b)

(c)   (d)
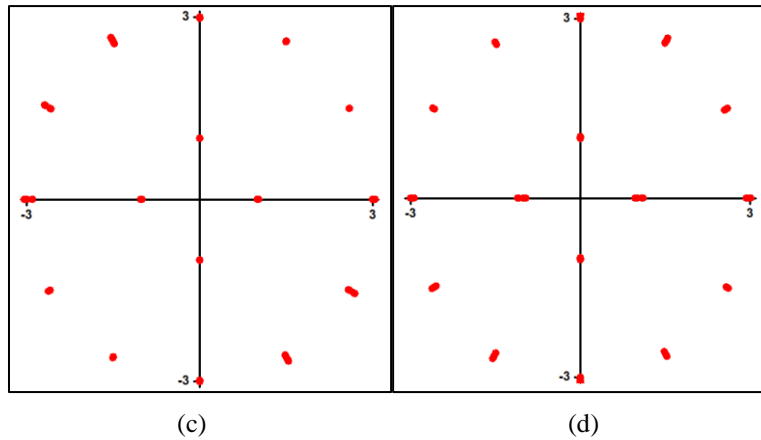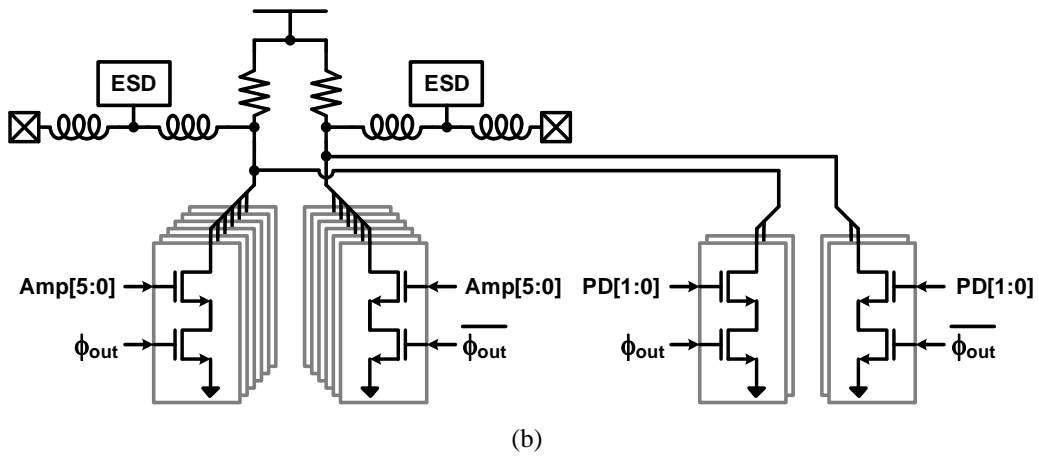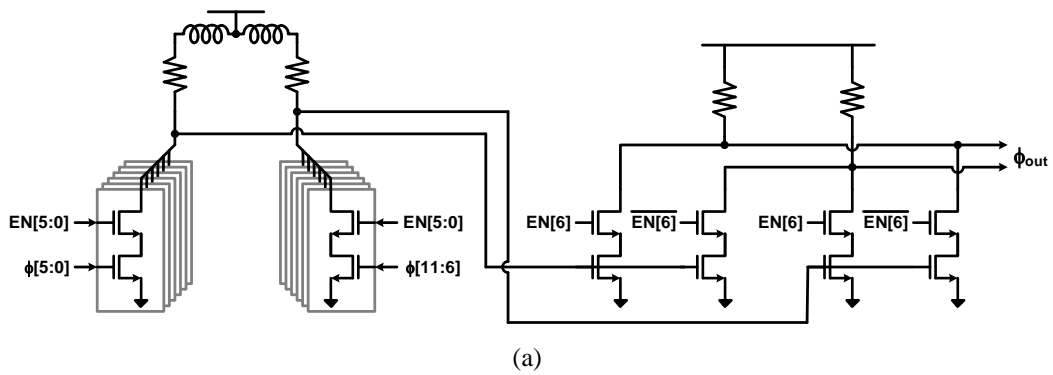
Fig. 6.9. Digital polar output DAC schematics: (a) phase mux and (b) segmented output driver. Simulated APSK-4+12 constellations with (c) 12.8GHz and (d) 25.6GHz carriers.

Fig. 6.9(a) shows an example where N=12 to generate either the QAM-16 or

APSK-4+12 constellations. An initial pseudo-differential CML 6:1 phase mux, which

utilizes shunt peaking for bandwidth extension allows generation of 0° to 150°. This is followed by a 2:1 mux that can invert the differential output to span the required 360°.

Fig. 6.9(b) shows the DAC output driver that is segmented with 6b (4b binary and 2b thermometer) amplitude control and parallel 2b predistortion cells. The selected phase signal differentially drives the bottom transistor in each output driver segment, while common amplitude control of the top transistors realizes the desired constellation point magnitude with also the FIR filter response computed by the DSP. The 22nm simulation results of Fig. 6.9(c) and (d) show that the APSK-4+12 constellation is generated with low EVM for both the 12.8 and 25.6GHz carriers.

In conclusion, a DAC-based transmitter architecture is proposed for 100+Gb/s serial links. To improve jitter robustness and reduce system equalization complexity, the proposed DAC-based transmitter supports advanced baseband and multi-carrier modulation schemes. Before implementing the transmitter in silicon, it is verified by using MATLAB system-level models to verify its operation and to optimize its design parameters. From the results of system-level verification, the performance requirements of Tx block circuits are specified. A phase modulator circuit is one of key blocks in the proposed Tx because its phase change must be large, accurate, and fast. It also presents an initial design for the phase modulator and output driver with amplitude modulation.

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