HIGH LINEARITY TECHNIQUES FOR ANALOG FILTERS, BUILT-IN TESTING AND IMPEDANCE SPECTROSCOPY IN SCALED CMOS TECHNOLOGIES

A Dissertation

by

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ABSTRACT

With the advances in CMOS technology, the minimum feature sizes and the threshold voltage of the transistors are continuing to scale down. This scaling down allows an increasing count of transistors per unit area, increasing device speed, and lowering power consumption. This technological trend has fueled enormous advancement in the development of low-cost and feature-rich system-on-chip (SoC) products. Today's SoCs often integrate a complete electronic system in a single CMOS platform, including highly-complex digital circuits, high-fidelity analog peripherals, radio-frequency (RF) circuits, and power management circuits. Advancement in SoC enabled new technologies such as smart homes, smart cities, and wearable medical devices. However, the increasing number of integrated analog parts that coexist with digital circuits brings several challenges, such as the aggressive reduction in supply voltage and increased susceptibility to the process, voltage, and temperature (PVT) variations. These challenges motivated exploring alternative forms of analog signal representation, such as the time/phase domain and created new topologies of analog circuits that take advantage of CMOS technology scaling. Moreover, analog built-in-self-test (BIST) is becoming inevitable with the increased number of analog components per integrated circuit (IC) and increased intra-die and inter-die process variability. Furthermore, SoC technologies have enabled advancement in hand-held medical devices, which is becoming an essential driver for the future consumer electronics market. In this dissertation, challenges and solutions for these research topics are explored.

First, a new class of phase-mode ring oscillator (RO)-based filters that address linearity and process variance limitation of existing RO-based filters is presented. A highly-linear process-tolerant RO filter topology is achieved by imitating the widely known active-RC topology in the phase domain. We propose utilizing a set of frequency detectors (FDs) and

phase detectors (PDs) to extract both the frequency and phase information of an inverter-based RO to synthesize active filters in a way similar to integrator-based active-RC filters, which are synthesized using a set of capacitors and resistors, respectively. A zero-compensation technique is proposed to extend the achievable bandwidth of the proposed topology. Also, a delay-locked loop (DLL)-based tuning scheme is introduced to achieve resilience over PVT variations. A prototype 5th-order, 2–22 MHz continuous-time Butterworth filter is presented in 130 nm CMOS technology to demonstrate the proposed topology. The filter consumes 6.2–8.9 mA from a 1 V supply and achieves 26.2 dB in-band IIP3. The filter achieves bandwidth variation less than $\pm 3.5\%$ over a temperature range of -40 °C to 85 °C and supply voltage range of 0.9–1.2 V.

Second, a harmonic-canceling sinewave generator for analog BIST applications. An architectural solution to implement the irrational coefficient of the sampled half-sine harmonic-canceling filter (HCF) is presented. The proposed technique relaxes the trade-off between output linearity and coefficients mismatch. The cascade of HCFs allows to filter out up to the 47^{th} harmonic of an input square-wave. Additionally, the system is fully reconfigurable to implement different order HCFs and can be configured to enhance either the fundamental harmonic or the 5^{th} harmonic of an input square wave, which extends the output frequency range. The system is fabricated in 180nm CMOS technology. Measurement results show a maximum of 66 dBc spurious-free dynamic range (SFDR) and output frequencies ranging from 0.8 MHz to 100 MHz.

Finally, an impedance analyzer with an on-chip stimulus generator (SG) for bioimpedance spectroscopy applications is presented. The system provides sub-GΩ impedance measurement with less than 1.2% error over the frequency range of 0.01–100 kHz. The impedance analyzer system prototype is implemented in 180-nm CMOS technology, the SG and the impedance read-out (IRO) circuits consume 0.64 mW and 0.32 mW respectively from a 1.8V supply.

DEDICATION

To my parents, brothers, my wife, and beloved daughter, Jasmine.

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All other work conducted for the dissertation was completed by the student independently.

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1. INTRODUCTION

The CMOS integrated circuit (IC) industry has vastly evolved over the past decades in terms of increased chip speed and functionality density along with decreased power dissipation and cost, as Moore's law had projected [3]. The feature size of semiconductor devices has been continuously shrinking over time, reaching deeply into the nanoscale. This technological trend fueled enormous advancement in the development of low-cost and feature-rich system-on-chip (SoC) products. Today's SoCs often integrate a complete electronic system into a single CMOS platform, including highly-complex digital circuits, high-fidelity analog peripherals, radio-frequency (RF) circuits, and power management circuits. Advancement in SoC has enabled new technologies such as smart homes, smart cities, and wearable medical devices. However, the increasing number of integrated analog parts that coexist with digital circuits brings several challenges. First, technology scaling, which is mainly driven by digital circuits, results in an aggressive reduction in the supply voltage. This trend adds a burden to the traditional voltage-mode analog circuitry operating on the same supply. Moreover, in some applications, digital circuits could benefit from supply-voltage scaling that dynamically adjusts performance according to different energy modes [4]. Therefore, it is desirable to develop digital-friendly analog circuits that use nontraditional forms of signal representation, such as the time/phase-mode circuits, which can operate with flexible supply voltages and takes advantage of technology scaling.

The second challenge that faces modern SoCs with an increased number of integrated analog parts is the increased testing time and cost. The increasing number of analog parts in modern ICs results in an increasing amount of test data that needs to be processed in real-time to determine the quality of the parts. The automatic test equipment (ATE) has to process a massive amount of parallel data from multiple interfaces connected to various parts of a

device under test (DUT) in real-time to maintain high test throughput [5]. Although built-in self-test (BIST) and design-for-testability (DFT) are well established for digital circuitry [6], the research in analog DFT and BIST techniques are lagging [5]. Analog BIST can enable the reduction of test instrument complexity or elimination of the need for external test instruments altogether [5].

As previously mentioned, modern SoCs have enabled advancement in wearable medical devices, which is becoming an essential driver for the future consumer electronics market. They are expected to exceed $7.9 Billion in sales in 2021 [7]. Much research is being conducted to develop compact, versatile, and low-cost medical sensor technologies, which enables better health monitoring. One of the most promising technologies is bio-impedance sensors technology, which is becoming the basis of novel noninvasive medical diagnostics.

1.1 Time/Phase-Mode Analog Circuits

Although the semiconductor technology scaling has resulted in a phenomenal performance improvement of digital circuits, this trend has been a mixed blessing for analog circuits [8]. Fig. 1.1 summarizes transistor performance metrics that the International Technology Roadmap for Semiconductor (ITRS) report projected [9]. With the aggressive reduction of transistors gate length, the intrinsic device speed, i.e. transistor f_T, has improved but the intrinsic gain of the devices has reduced. Moreover, the lowered supply voltage introduces a voltage headroom limitation that makes the representation of analog signals in voltage domain with a high signal-to-noise ratio (SNR) significantly harder. For these reasons, alternative domains of analog signal representation are needed that are more suitable for scaled CMOS technologies. A strong candidate is to represent analog information in time or phase domain, where the analog signal is represented as a time difference or a phase shift between two rising and/or falling edges [10]. Fig. 1.2 shows the analog signal representation in both voltage and time/phase domain. It is worth noting that time/phase mode analog circuits ben-

efit from technology scaling as opposed to the traditional voltage-mode circuits thanks to the improved time resolution of nanoscale technologies.

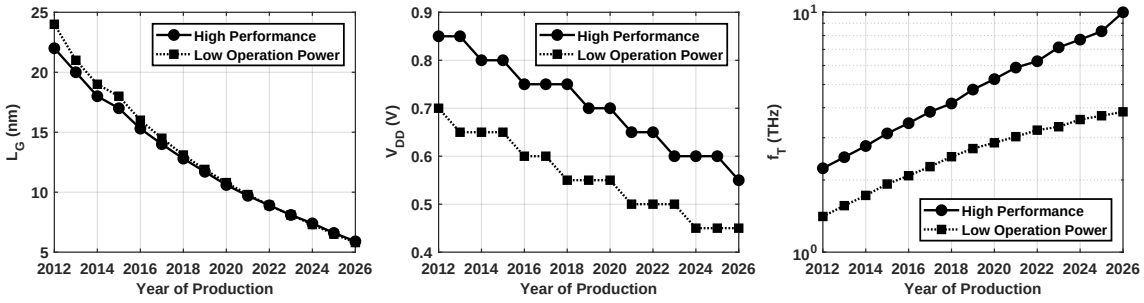


Figure 1.1: Summary of gate length, supply voltage, and intrinsic frequency of transistors for high performance and low power technologies from 2012 to 2026 by ITRS.

Several phase-mode circuits are found in the literature, including digital-to-analog converters (ADCs) [11, 12] and analog filters [13–15], that use ring-oscillators (ROs) as frequency/phase quantizers, or as voltage/current-to-phase integrators, respectively. The phase-mode ADCs have gained vast popularity in the past decade because of their ability to achieve less power and higher resolution compared to the voltage-mode ADCs [16]. On the contrary, phase-mode analog filters, i.e., RO-based filters, did not gain the same popularity, because of their inability to achieve competitive linearity performance when compared to traditional

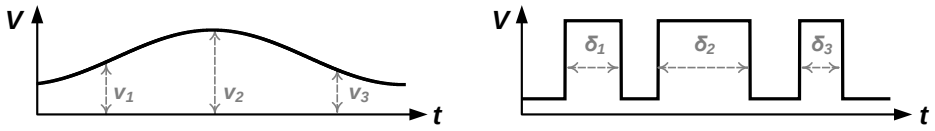


Figure 1.2: Analog signal representation in different domain: (a) voltage domain, and (b) time/phase domain.

voltage-mode analog filters. This dissertation studies the limitations of the existing RO-based filters in terms of linearity and process, voltage, and temperature (PVT) variations. Then, this study proposed a new class of RO-based filter that addresses these limitations.

1.2 Analog Built-in Self-Test

Testing procedures are a vital part of the product fabrication cycle and sometimes consume as much as 55% of the total production cost [17]. In this context, BIST solutions have been proposed as an appealing approach to reduce the testing cost. The concept is to embed self-testing capabilities to the integrated circuits, such as a stimulus generator and an output response analysis. A block diagram of a complete BIST and optimization system was proposed in [1, 2] and is shown in Fig. 1.3. This system consists of an analog self-test path and a digital optimization engine. The analog self-test path consists of a stimulus generator and an output response analyzer. Multiple stimuli can be implemented to capture various characteristics of the DUT. For example, dc characteristics, transient waveform ($h(t)$), transfer function ($H(j\omega)$, linearity and noise can be measured as shown in Fig. 1.3. Researchers have attempted to implement numerous stimuli such as single-tone generators [18–31], and two-tone generators [30, 32]. Moreover, research on output response analyzers, such as on-chip spectrum analyzers [33–38], on-chip oscilloscopes for supply noise measurements [39–42], and on-chip linearity measurement [43–45] have been also reported in the literature.

This dissertation also focuses on the on-chip stimulus generators for BIST, particularly harmonic-canceling single-tone synthesizers. Section 3 presents a modular approach to implement harmonic-canceling synthesizer of any order, that can enhance either fundamental harmonic or any individual higher harmonic. A prototype of an on-chip fully-reconfigurable high-quality sine-wave synthesizer is also presented to prove the proposed concept. The same concept can be extended to implement multi-tone signal generators for further BIST capabilities.

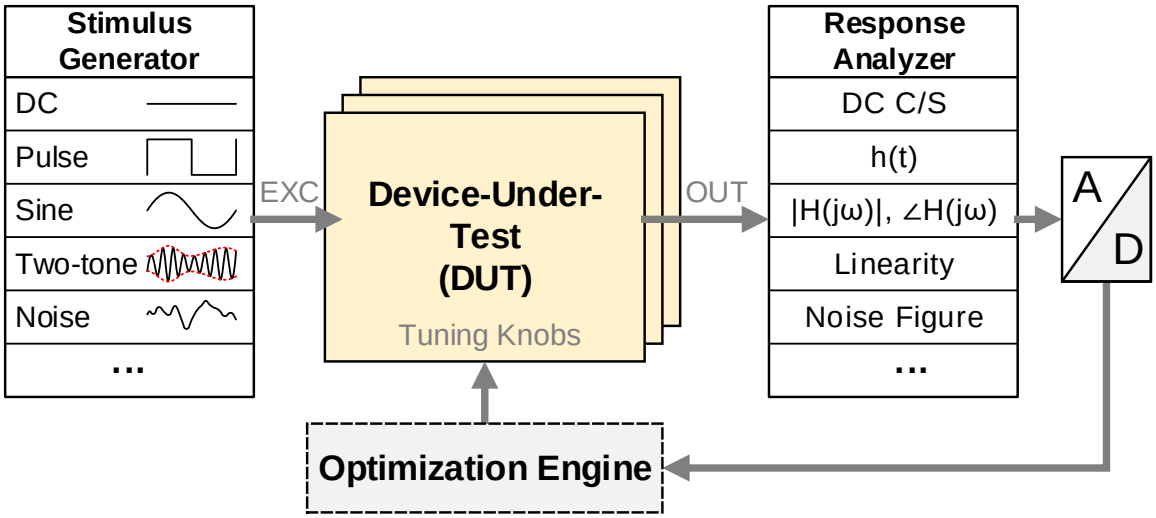


Figure 1.3: Fully-integrated built-in self-test and optimization system [1, 2].

1.3 Fully-Integrated Impedance Analyzer

Impedance analyzers are used to measure complex electrical impedance over a range of test frequencies. Impedance analysis is a powerful tool to characterize materials in numerous applications such as biomedical devices, agriculture, food production, and environment monitoring. Characterization is based on the knowledge of the relationship between the measured electrical impedance and specific physical properties of the material under test. In biomedical applications, impedance measurements have been used as a noninvasive method for several clinical applications such as monitoring heart failures [46], hydration, body composition [46], and blood pressure [47]. Bio-impedance measurement can be done in a clinical setup or in a portable wearable device [47–49].

Furthermore, impedance analyzers can be used with electrochemical impedance spectroscopy (EIS)-based sensors. EIS-based sensors are widely used for precise and rapid disease diagnosis [50, 51]. Miniaturized impedance analyzers enable EIS systems to integrate with a small form factor that can be used for wearable and point-of-care devices. Ac-

cordingly, Section 4 of this dissertation focuses on the implementation of a fully-integrated highly-accurate impedance analyzer for EIS applications.

1.4 Organization

The dissertation contains five sections. Following the introduction, Section 2 presents a new class of RO-based filters that address linearity and process variance limitation of existing RO-based filters. In Section 3, a harmonic canceling sinewave synthesizer for analog BIST application is presented. Section 4 extends the concept of the harmonic canceling synthesizer to implement a harmonic canceling impedance analyzer with an on-chip stimulus generator for EIS applications. Finally, Section 5 concludes the dissertation and explores areas of future work.

2. A PVT-RESILIENT, HIGHLY-LINEAR FIFTH-ORDER RING-OSCILLATOR-BASED FILTER [1]

2.1 Introduction

Analog filters are used for a wide range of applications such as baseband channel select filters in wireless receivers, or for signal conditioning and anti-aliasing filters preceding analog-to-digital converters in sensor applications. Analog filters are basically built of integrators, as integrators are used to form complex poles required in the synthesis of high-order filters. Commonly used integrator topologies use operational transconductance amplifiers (OTA) with different requirements on the unity-gain bandwidth (UGB) of the utilized OTAs. Named after the topology of the integrator, commonly used analog filter implementations are: OTA-C, active-RC, and active-UGB-RC filters (Fig. 2.1 left). In OTA-C topology, an OTA loaded by a capacitor, C, forms an integrator [52], which can build high bandwidth filters [53] with low power consumption because the UGB of the OTA is in the same order as the filter's corner frequency. However, OTA-C integrators suffer from poor linearity because OTAs are working in an open loop, and they have to be accompanied by linearization techniques [54]. On the other hand, active-RC filters offer better linearity at the cost of lower signal bandwidth, because the OTAs work in a feedback configuration [55, 56]. However, active-RC filters suffer from higher noise compared to OTA-C, because of the thermal noise of the resistors. Active-UGB-RC topology [57] provides a compromise between the OTA-C and active-RC filters. Active-UGB-RC filters are built in a way similar to active-RC; however, the UGB of the OTAs are used to double the order of the filter [57]. The main drawbacks of the active-UGB-RC topology are that it also suffers from high noise because of the

[1] This section is reprinted with permission from H. Osman and E. Sánchez-Sinencio, "A PVT-Resilient, Highly-Linear Fifth-Order Ring-Oscillator-Based Filter," in IEEE Transactions on Circuits and Systems I: Regular Papers. ©2020 IEEE.

resistors and linearity degradation close to the filter's corner frequency. All these topologies require OTAs with very high, ideally infinite, dc gain. However, OTA design becomes even more challenging in nanoscale CMOS technologies because of the reduced intrinsic gain of the devices and the limited voltage headroom [58].

As a solution to the challenging nature of OTA-based integrators in nanoscale CMOS technologies, an inverter-based ring-oscillator (RO) is utilized in [13, 14, 59] to implement an integrator with infinite dc gain. A current-controlled oscillator (CCO) is used in [13, 14] to convert the input current into oscillations with an instantaneous frequency that is a function of the input current. Since the instantaneous phase of the CCO is the integral of its instantaneous frequency, then the CCO works as a current-to-phase (I-to-Φ) integrator. A phase detector (PD) measures the phase difference between the CCO phase and a reference phase to produce pulse-width modulated (PWM) representation of the CCO phase [60]. A charge pump (CP) is then used to convert this PWM signal into a current. This way, the CCO-PD-CP combination works as a current in–current out (I to I) RO-based integrator (ROI) that can be utilized to build continuous-time (CT) filters [13, 14]. However, the ROI architecture resembles the classical open-loop OTA-C topology, as shown in Fig. 2.1; hence, it inherits its linearity limitations. Moreover, the corner frequency of the filter is proportional to the CCO gain, k_{CCO}, which is susceptible to PVT variations [14].

To overcome the nonlinearity of the ROI, a ring-oscillator based amplifier (ROA) is proposed in [15]. The ROA intrinsically has an infinite dc gain. Therefore, it can be used as a substitute for OTAs in active-RC or active-UGB-RC filter architectures. A zero-compensation technique is utilized in [15] to enable the ROA to drive large load capacitances required by active-UGB-RC topology. Only two ROAs were used to build a fourth-order active-UGB-RC filter. This architecture suffers from the following drawbacks: 1) the filter's poles are sensitive to the UGB of the ROA, which in turns is proportional to the process-dependent gain of the VCO, k_{VCO}, used to build the ROA, and 2) the output of the charge-

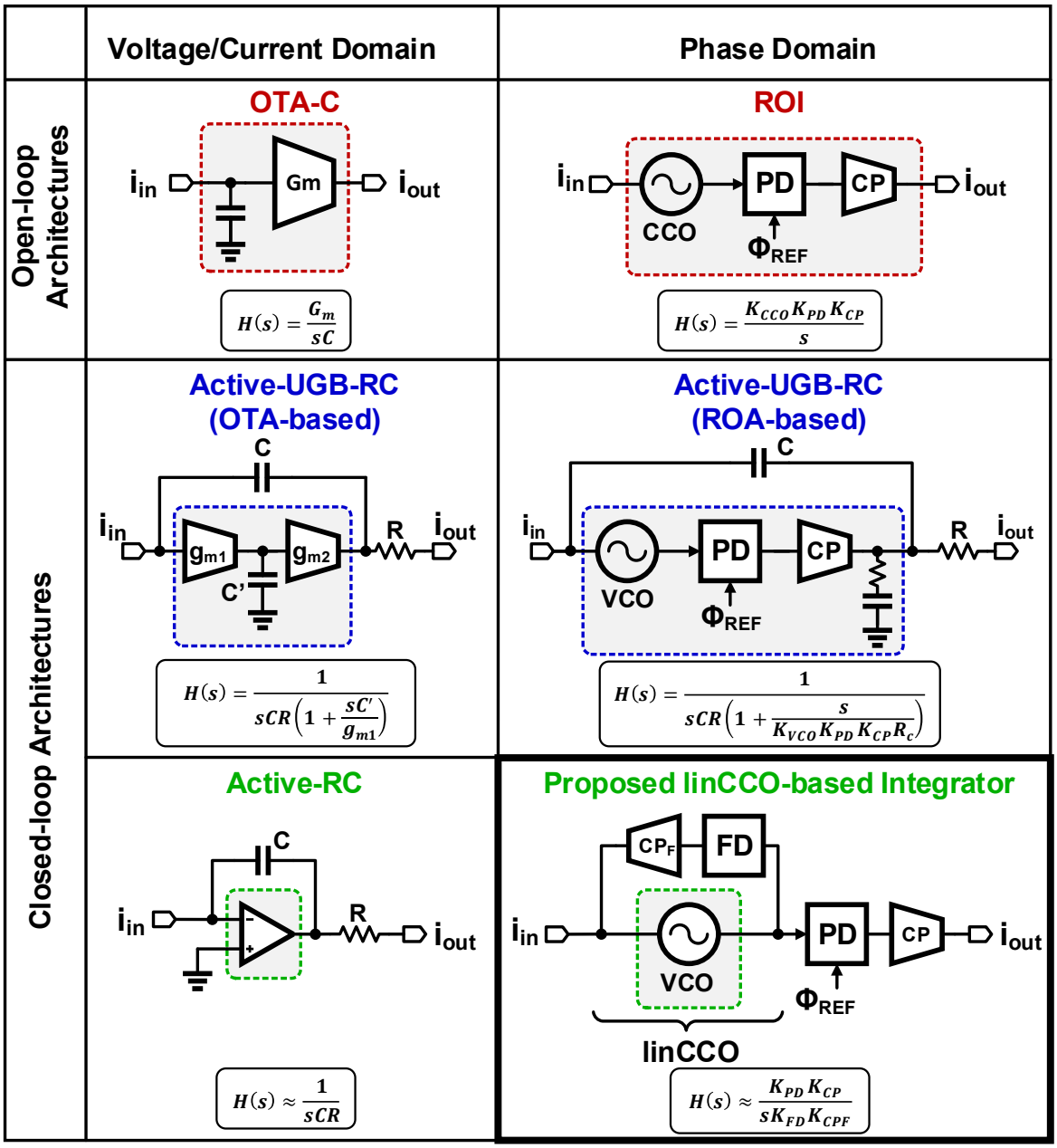


Figure 2.1: Open-loop and closed-loop integrator architectures in the voltage/current-domain and equivalent implementations in the phase domain.

pump is in voltage domain similar to OTA-based structures, which makes this topology unsuitable for low-voltage applications. Fig. 2.1 summarizes the integrator architectures of the

continuous-time RO filters found in the literature along with their OTA-based counterparts.

In this section, a highly linear RO-based filter topology (Fig. 2.1 bottom right) is introduced that mimics the well-known active-RC filter topology. The proposed topology leverages both phase and frequency information of the RO to create proportional and derivative feedback paths around the RO, corresponding to the resistive and capacitive paths in active-RC topology, respectively. The linearity of the RO improved because of the closed-loop operation. A frequency compensation scheme is also introduced to allow the proposed filter topology to achieve higher bandwidth. A DLL-based frequency tuning scheme is also reported that goes along with the proposed filter topology to achieve PVT resilience.

The rest of the section is organized as follows: Section 2.2 analyzes the linearity of the RO-based filters and outlines how the nonlinear transfer characteristics of the RO results in degradation of both in-band and out-of-band linearity performance. In this respect, a highly linear oscillator is inevitable for improved linearity performance. Section 2.3 introduces a closed-loop linearization technique for RO's transfer characteristics resulting in a new circuit that we refer to as a linearized current-controlled oscillator (linCCO), and outlines the resemblance between the proposed linCCO-based integrator and active-RC integrator. Section 2.4 discusses filter architecture using the proposed linCCO, the frequency tuning scheme, and the prototype filter implementation. Circuit design of the important building blocks is presented in Section 2.5. The measurement results of the prototype filter are presented in Section 2.6, followed by conclusions in Section 2.7.

2.2 Linearity Analysis of RO-based Filters

In this section, we analyze the linearity of conventional RO-based filter architecture implemented in [13, 14]. This topology uses a pseudo-differential integrator as shown in Fig. 2.2a to obviate even-order harmonic distortion caused by the nonlinear I-to-F characteristics of the CCO. The pseudo-differential integrator consists of two identical CCOs driven by

differential input currents. However, odd-order harmonic distortion is still present, which limits the linearity performance of this topology. We first study the equivalence between the CCO-PD structure employed in RO-based filters and naturally-sampled pulse width modulation (NSPWM) modulators. Then, a simplified model for nonlinear distortion components caused by nonlinear I-to-F characteristics of the CCO, and the NSPWM aliasing distortion is discussed.

2.2.1 Equivalence between CCO-PD Structure and NSPWM Modulator

Fig. 2.2a shows a pseudo-differential first-order RO filter similar to the one used in [13, 14]. When a zero differential input current is applied, the two CCOs become locked to each other with a zero frequency difference and a phase difference $\Delta\Phi_0 = \pi$. Therefore, the free-running instantaneous phases of the two oscillators are $\Phi_0 \pm \pi/2$, where $\Phi_0 = 2\pi f_0 t$.

When differential ac input current, $\Delta i_i = i_i^+ - i_i^-$, is applied, the oscillators' instantaneous phases change accordingly and become $\Phi_0 \pm (\pi/2 + \Delta\phi/2)$, where $\Delta\phi$ is the integral of the differential control ac current, $\Delta i_c = i_c^+ - i_c^-$, and is expressed as:

$$\Delta\phi(t) = 2\pi k_{CCO} \int_0^t \Delta i_c d\tau. \tag{2.1}$$

From Fig. 2.2c, it is noted that the rising and falling edges of the PD output correspond to the time instants when $\Phi_0 \pm (\pi/2 + \Delta\phi(t)/2) = 0$, respectively. Therefore, PD outputs can be thought of as the difference between a leading-edge NSPWM signal resulting from comparing $\pi/2 + \Delta\phi(t)/2$ with the wrapped phase $-\Phi_0$, and a trailing edge NSPWM resulting from comparing $\pi/2 + \Delta\phi(t)/2$ with the wrapped phase Φ_0. The result is a double edge NSPWM signal, $d_o(t)$, that can be modeled as an output of a comparator comparing a modulating signal $x(t) = \Delta\phi(t)/\pi$ with a triangular carrier as shown in Fig. 2.2b. The NSPWM signal, $d_o(t)$, consists of a baseband signal, $\langle d_o(t) \rangle = x(t)$, along with a high-frequency ripple signal, $r(t)$, which is $x(t)$ phase-modulated onto each carrier harmonic [61].

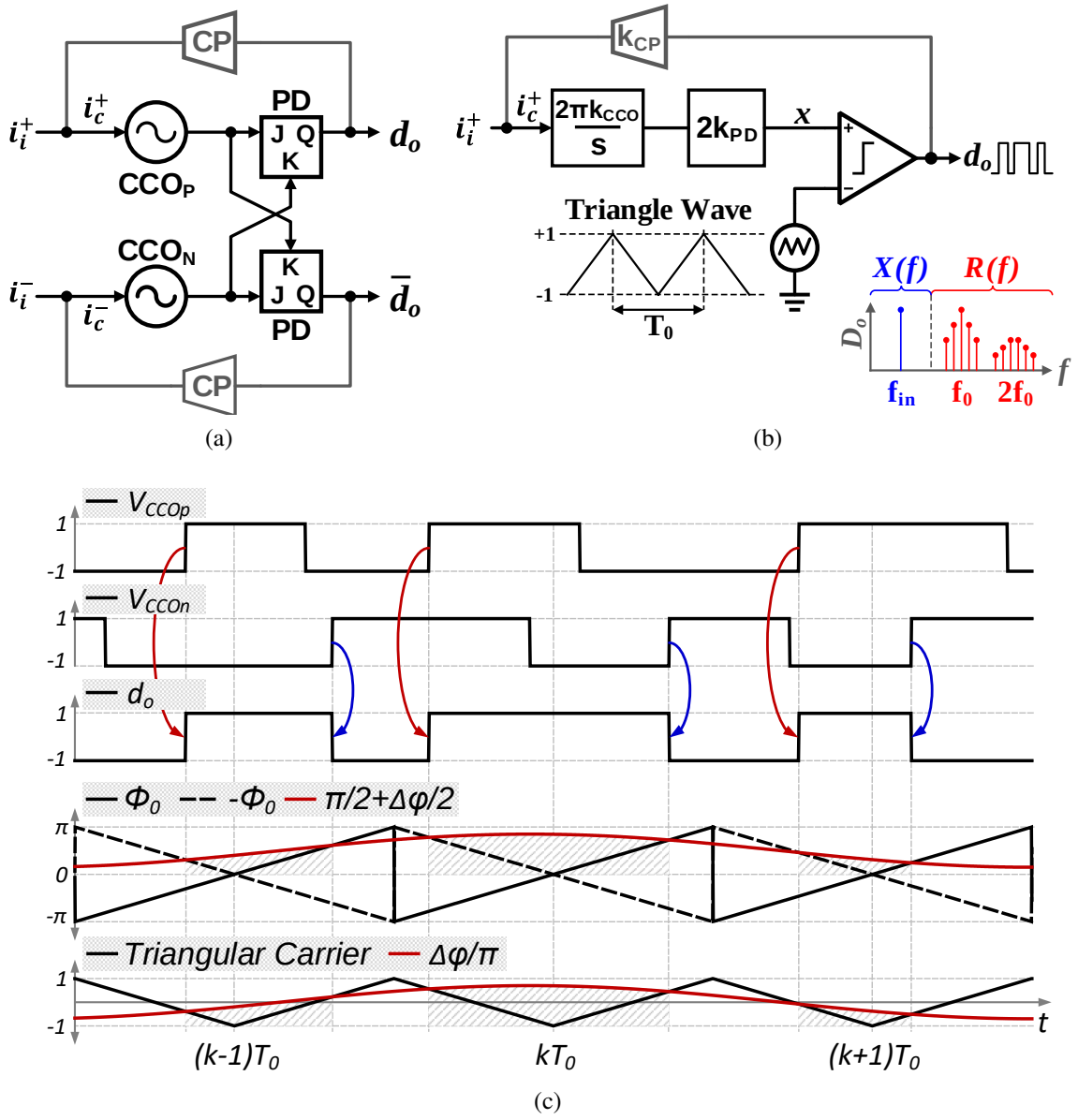


Figure 2.2: Equivalence between CCO-PD structure in RO-based filters and dual-edge NSPWM modulators; (a) 1st-order RO filter, (b) equivalent model using NSPWM modulator, and (c) timing diagram.

2.2.2 Effect of CCO Nonlinear Characteristics

The first contributor to the filter's nonlinearity is the nonlinear I-to-F characteristics of the CCO. In [14], the suppression of the CCO nonlinearity is attributed to its placement in a feedback loop. However, this assumption is not completely true at the whole frequency range because the loop gain drops at frequencies higher than the filter's cut-off frequency. This causes high nonlinear distortion for out-of-band signals, which we will illustrate herein. Moreover, the nonlinearity caused by the self-mixing of the phase-modulated NSPWM ripple signal as it passes through the CCO nonlinearity was not taken into account. A divide-and-conquer technique is used here to study the nonlinear behavior of the RO-based filter without loss of generality. On the one hand, it is noted that the transfer function from the input current to the CCO control current, namely the error transfer function (ETF), has a high-pass response. Thus, the magnitude of the CCO control current becomes relatively large in the filter's stopband, which produces nonlinear distortion components when applied to the CCO. On the other hand, the transfer function from the input current to the NSPWM modulating signal $x(t)$, namely the signal transfer function (STF), has a low-pass response. Therefore, the nonlinear distortion components produced from the downconversion of the phase-modulated ripple signal, $r(t)$, can only become dominant in the filter's passband. The ETF and STF are expressed as:

$$ETF = \frac{i_c(s)}{i_i(s)} = \frac{1}{1+T(s)}, \tag{2.2}$$

$$STF = \frac{x(s)}{i_i(s)} = \frac{1}{k_{CP}} \frac{T(s)}{1+T(s)}, \tag{2.3}$$

where $T(j\omega) = \frac{\omega_c}{s}$ is the open-loop transfer function, and $\omega_c = 2\pi f_c = 4\pi k_{CCO} k_{CP} k_{PD}$ is the bandwidth of the first-order filter.

The frequency-domain nonlinearity analysis method presented in [62, 63] is used here

to study the frequency behavior of the harmonic distortion of RO filters. We start with the weakly nonlinear open-loop I-to-F characteristic of the CCO, i.e., the characteristics only exhibit gradual slope changes but are not hard-limited or saturated. The harmonic distortion can be calculated from the series expansion of the I-to-F nonlinear characteristics:

$$f = k_{CCO}\left(1 + k_{3N} i_c^2\right) i_c, \tag{2.4}$$

where i_c is the CCO input control current, f is the CCO frequency shift from its free-running frequency, k_{CCO} is the CCO gain in Hz/A, and k_{3N} is the third-order nonlinear coefficient normalized to the linear gain k_{CCO}. Only the third-order nonlinear coefficient is considered because it is the dominant distortion contributor.

2.2.2.1 Stopband Harmonic Distortion

Based on the aforementioned divide-and-conquer technique, the ripple signal is nearly signal-independent in the stopband. For that reason, it is omitted in this frequency range. By considering a pure input sinusoidal tone at the input of the first-order filter shown in Fig. 2.2a, i.e. $i_i(t) = I_i cos(\omega t)$, the amplitude of the CCO control current becomes $I_c = I_i \times |ETF\,(j\omega)|$. By substitution into (2.4), the CCO's frequency shift exhibits a nontrivial harmonic distortion

$$f(t) \approx k_{CCO} I_c \left[\cos(\omega t) + \frac{k_{3N}}{4} I_c^2 \cos(3\omega t)\right], \tag{2.5}$$

where the effect of gain compression has been neglected for simplicity. The amplitude of the third-order distortion component equals $(k_{CCO}k_{3N}/4) \times I_i^3 \times |ETF\,(j\omega)|^3$, which can be viewed as a spurious signal injected at the output of the I-to-F converter. That spurious distortion signal is subsequently processed by the feedback loop and appears at the output scaled by its corresponding transfer function evaluated at the harmonic frequency, i.e., at

3ω [62]. Therefore, the harmonic distortion at the output of the lossy integrator can be calculated as:

$$\mathrm{HD}_{3\mathrm{f}}^{\mathrm{CCO,SB}}(\omega) = \frac{k_{CP}^2 k_{3N}}{12} \cdot \frac{1}{|1+T(j\omega)|^2 |1+T(j3\omega)|} \left(\frac{I_i}{k_{CP}}\right)^2, \tag{2.6}$$

2.2.2.2 Passband Harmonic Distortion

Because of the high-pass ETF, the baseband component of the CCO control current is almost zero, and it can be assumed that the CCO control current is only the high-frequency ripple signal scaled by the CP gain, i.e., $i_c(t) \approx k_{CP} r(t)$. When this phase-modulated signal is applied to the nonlinear CCO with the characteristics described in (2.4), some of the phase-modulated carrier harmonics are down converted to the baseband frequency. Without loss of generality, it is assumed that the input signal is at a much lower frequency, nearly at dc, with respect to the free-running frequency of the CCO. Therefore, we can study the nonlinear distortion produced by this phenomenon by deriving the dc transfer characteristics of the mean cube ripple, $\langle r^3(t) \rangle$, versus the modulating signal, x, that is for an M-phase NSPWM is given as:

$$\left\langle r^3(t) \right\rangle = 16 \left(D - \frac{2m+1}{2M}\right) \left(\left(D - \frac{2m+1}{2M}\right)^2 - \frac{1}{4M^2} \right), \tag{2.7}$$

where $D = \frac{x+1}{2}$ is the duty-ratio of the PWM signal, $m = \mathrm{floor}\,(M \times D)$ is the maximum integer that does not exceed $M \times D$, and $\langle \cdot \rangle$ is the mean operator. Equation (2.7) is derived in a similar way to the mean square ripple of multiphase PWM-based buck converters [64]. Fig. 2.3 plots $\langle r^3(t) \rangle$ versus the modulating signal, x, for single-phase and some multi-phase PWM modulators. It is worth noting from Fig. 2.3 that although $\langle r^3(t) \rangle$ is a continuous function, it is not infinitely differentiable at $x = \frac{2m}{M} - 1$. Hence, the filter will introduce severe small-signal nonlinearity if biased around any of these points. An optimal bias point

is chosen to improve the nonlinearity of the RO filter, which is $x_0 = 0$ for odd M or around $x_0 = 1/M$ for even M. In the vicinity of the bias point x_0, (2.7) can be described with the power series:

$$\left\langle r^3(t) \right\rangle = 2\left(x - x_0\right)\left(\left(x - x_0\right)^2 - \frac{1}{M^2}\right), |x - x_0| < \frac{1}{M} \tag{2.8}$$

where

$$x_0 = \begin{cases} 0 & Odd\, M \\ 1/M & Even\, M \end{cases} \tag{2.9}$$

Equation (2.8) can be used to estimate the filter's passband HD_3. For an input current $i_i(t) = I_i cos(\omega t)$, a third-order distortion component is generated at the output of the nonlinear I-F characteristics of the CCO (as shown in Fig. 2.4) with an amplitude $2k_{CCO}k_{3N}k_{CP}^3\frac{X^3}{4} = (k_{CCO}k_{3N}k_{CP}^3/2) \times I_i^3 \left|STF\left(j\omega\right)\right|^3$. Therefore, the passband harmonic distortion at the output of the lossy integrator can be expressed as:

$$\mathrm{HD}_{3\mathrm{f}}^{\mathrm{CCO,PB}}\left(\omega\right) = \frac{k_{CP}^2 k_{3N}}{2} \cdot \left|\frac{T\left(j\omega\right)}{1 + T\left(j\omega\right)}\right|^2 \left|\frac{T\left(j3\omega\right)}{1 + T\left(j3\omega\right)}\right| \left(\frac{I_i}{k_{CP}}\right)^2, \tag{2.10}$$

2.2.3 Aliasing Distortion in the NSPWM Modulator

A linearized model for the NSPWM modulator is often used as a gain of one for transfer function calculations. However, it was shown in [65] that an NSPWM modulator embedded in a closed-loop system with an open-loop transfer function, $T(j\omega)$, exhibits distortion even with perfectly linear components. Intuitively, this distortion was attributed to the ripple feedback signal, $r(t)$, that is filtered by $T(j\omega)$ and is effectively superimposed to the perfectly linear triangle carrier in Fig. 2.2b. This effect was studied in [65] for the low-frequency modulating signal $x(t)$ applied to an NSPWM modulator and was modeled as a signal-dependent offset $G(x)$, and a signal-dependent aperture delay $t_d(x)$ added to the tri-

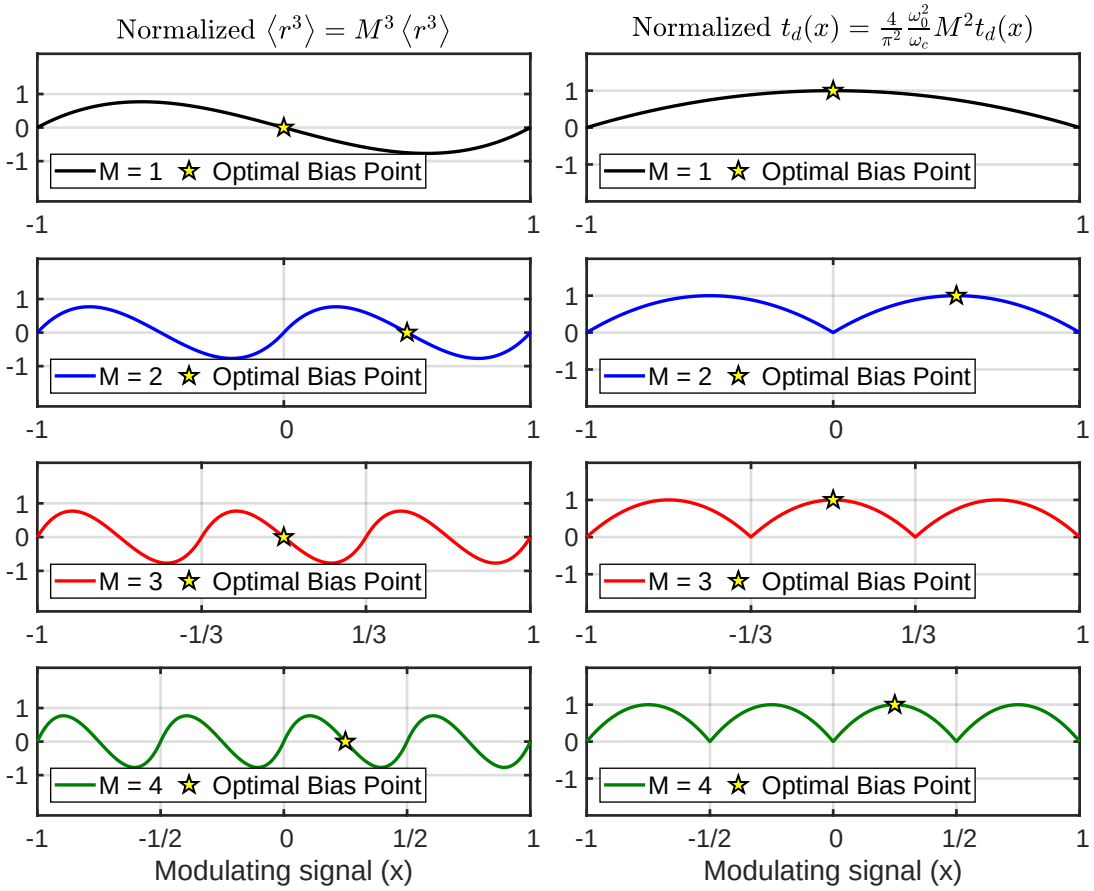


Figure 2.3: Normalized mean cube ripple $\langle r^3 \rangle$ and normalized signal-dependent aperture delay $t_d(x)$ versus modulating signal, x, for different values of M (M=1 represents a single-phase 1st-order RO filter, and $M > 1$ represents multi-phase filters).

angle carrier. Therefore, an improved model for the NSPWM modulator was derived with the following input-output relationship:

$$\langle d_o \rangle = x + G(x) + x' t_d(x), \tag{2.11}$$

where

$$G(x) = \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{(-1)^{n+1} \sin(n\pi x)}{n} \mathbb{R}\mathrm{e}\left\{T(jn\omega_0)\right\}, \tag{2.12}$$

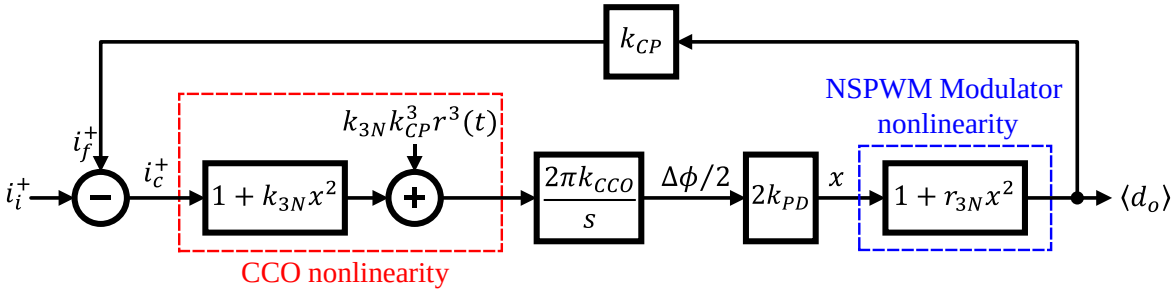


Figure 2.4: Model of a 1st-order RO filter with both nonlinear I-to-F CCO characteristics and ripple feedback nonlinearity.

and

$$t_d(x) = \frac{1}{2\pi f_0} \sum_{n=1}^{\infty} \frac{\cos\left(n\pi\left(x+1\right)\right)-1}{n} \mathbb{I}\mathrm{m}\left\{T(jn\omega_0)\right\}, \tag{2.13}$$

where $\omega_0 = 2\pi f_0$ is the carrier frequency, i.e. CCO's free-running frequency in rad/sec. For the first order RO filter shown in Fig. 2.2a, $T(j\omega)$ is a lossless integrator with gain ω_c. Hence, $G(x) = 0$, and the aperture delay can be derived for the general case of M-phase NSPWM modulator (see Appendix A) as:

$$t_d(x) = \frac{\pi^2}{4}\frac{\omega_c}{\omega_0^2}\left(\frac{1}{M^2} - \left(x+1-\frac{2m+1}{M}\right)^2\right), \tag{2.14}$$

where $m = \mathrm{floor}\left(M \times D\right)$ is the maximum integer that does not exceed $M \times D$, and $D = \frac{x+1}{2}$ is the duty-ratio of the PWM signal. Fig. 2.3 plots $t_d(x)$ versus the modulating signal, x, for single-phase and some multi-phase PWM modulators. Similar to what was observed for $\langle r^3(t)\rangle$, $t_d(x)$ is severely nonlinear around $x = \frac{2m}{M} - 1$. Hence, the optimal bias point discussed in Section 2.2.2 is crucial to improve the nonlinearity of the RO filter, which is $x_0 = 0$ for odd M, or $x_0 = 1/M$ for even M. In the vicinity of the bias point x_0, (2.14) can

be described with the power series:

$$t_d(x) = \frac{\pi^2}{4}\frac{\omega_c}{\omega_0^2}\left(\frac{1}{M^2} - (x - x_0)^2\right), |x - x_0| < \frac{1}{M} \tag{2.15}$$

Using (2.11) and (2.15), the RO lossy integrator exhibits a third-order harmonic distortion even if a linear CCO was used. By using (2.15) to substitute $t_d(x)$ in (2.11), we obtain the following nonlinear input-output relation:

$$\langle d_o \rangle \cong x + r_{3N}(j\omega)\, x^3, \tag{2.16}$$

where $r_{3N}(j\omega) = -j\omega\frac{\pi^2}{4}\left(\omega_c/\omega_0^2\right)$ is a frequency-dependent third-order nonlinear coefficient. Thus, the harmonic distortion at the output of the lossy integrator can be derived using the same nonlinearity analysis used in Section 2.2.2:

$$\mathrm{HD}_{3\mathrm{f}}^{\mathrm{NSPWM}}(\omega) = \frac{\pi^2}{16}\left(\frac{\omega_c}{\omega_0}\right)^2 \frac{\omega_c}{\omega} \cdot \frac{1}{|1 + T(j\omega)|^2 |1 + T(j3\omega)|}\left(\frac{I_i}{k_{CP}}\right)^2, \tag{2.17}$$

The results obtained from (2.6), (2.10), and (2.17) are validated with simulation results of a first-order RO filter with different number of phases $M = 1, 2, 4$ and biased at the optimal bias condition as shown in Fig. 2.5. The simulation results show a very good agreement with the theoretical findings. It is worth noting that harmonic distortion is present even when a perfectly linear CCO model is used, which was predicted by (2.17). Therefore, (2.17) can serve as a lower limit for achieved HD_3 of a first-order filter with a certain f_c and f_0.

The effectiveness of the optimal bias condition is validated with the simulation of a 4-phase first order RO filter with and without applying the optimal biasing condition as shown in Fig. 2.6. The filter shows a normal behavior of HD_3 versus input power with slope $2\,dB/dB$ when optimal bias is used, because $t_d(x)$ and $\langle r^3(t) \rangle$ can be described as a finite polynomial function of x around $x = x_0$. On the other hand, when the filter is biased

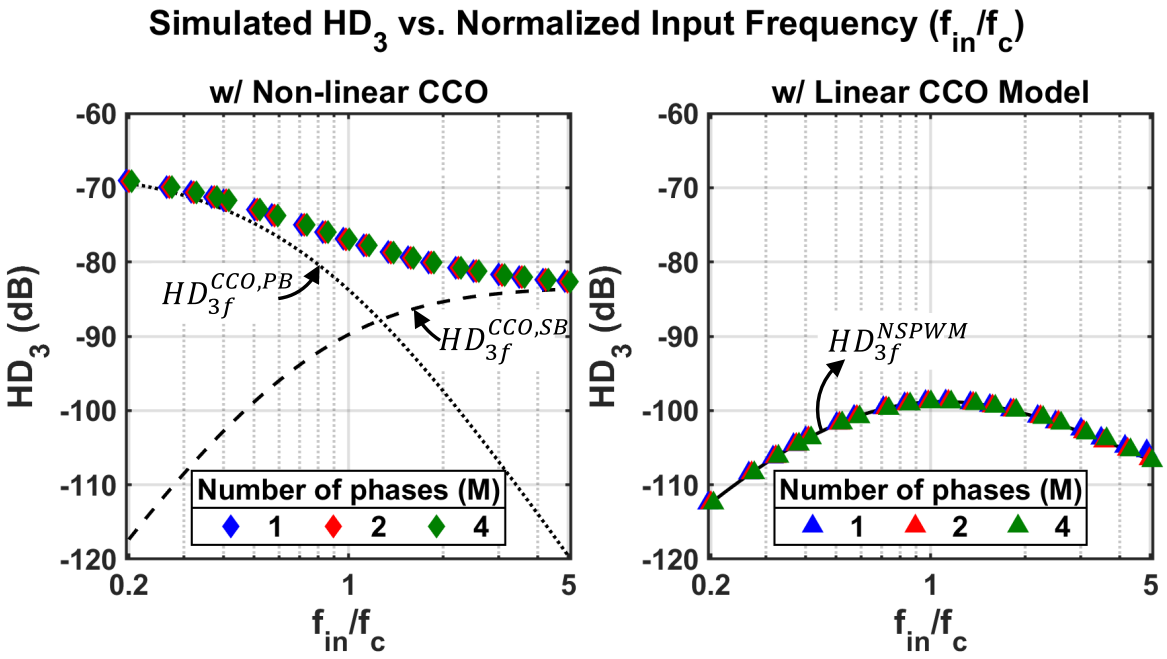


Figure 2.5: Simulated HD_3 versus frequency for single-phase and multi-phase 1st order RO filter with $f_c = 5$ MHz, $f_0 = 200$ MHz and ${}^{I_{in}}/_{K_{CP}=0.25}$. Continuous lines are calculated values, and marked points are simulated values.

around $x = 0$, the aperature delay, $t_d(x)$, and $\langle r^3(t)\rangle$ are functions of $|x|$, which result in the abnormal behavior of HD_3 versus input power with the $1\,dB/dB$ slope resulting in a worse small-signal nonlinearity.

The aforementioned analysis suggests that in the absence of ripple cancellation techniques, a highly linear CCO is inevitable for wide-band linearity for the RO-based filters. Therefore, we herein propose a linearized CCO that, together with the optimal biasing, can achieve a highly linear filter.

2.3 Proposed Linearized CCO

In this work, a linear RO-based integrator that mimics the linear active-RC integrator is proposed. The basic structure of an active-RC integrator is shown in Fig. 2.7a; the feedback capacitor works as a voltage-to-current (V-I) differentiator as shown in Fig. 2.7b. Hence,

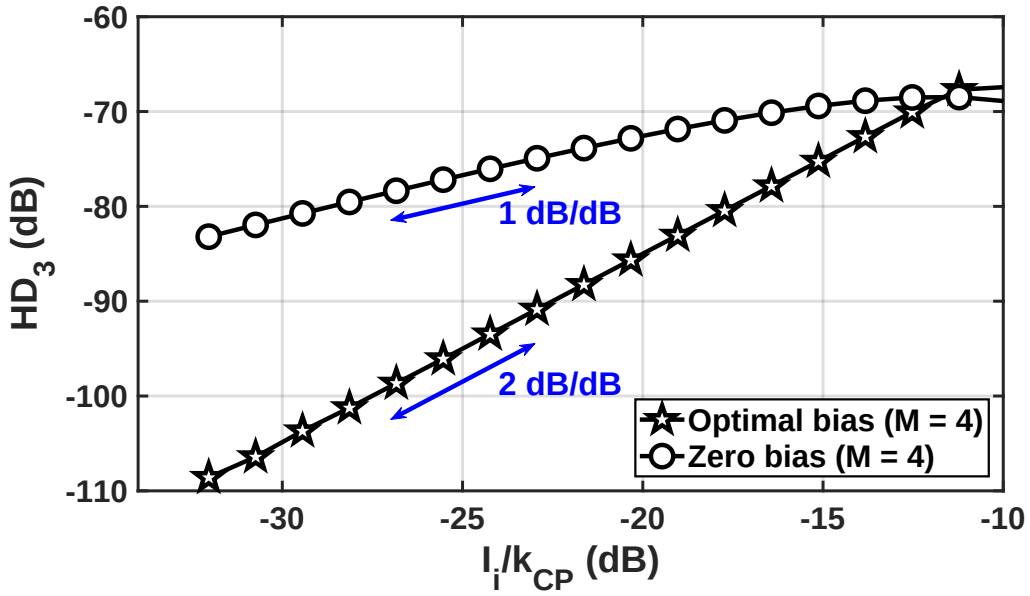
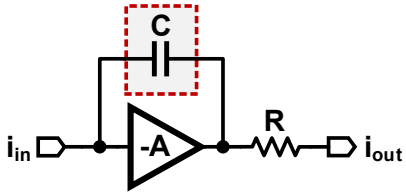


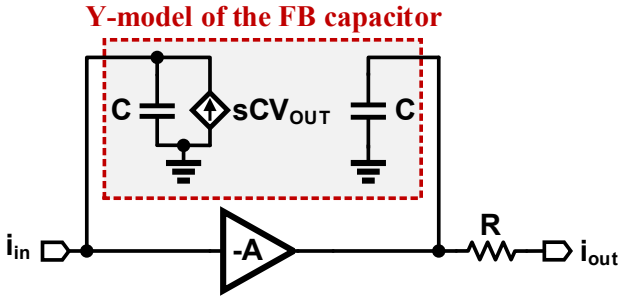
Figure 2.6: Simulated HD_3 versus input current for a four-phase 1st-order RO filter with $f_c = 5$ MHz, and $f_0 = 200$ MHz showing linearity improvement when biased at the optimal bias point .

because the capacitor is used in feedback with a high-gain operational amplifier (opamp), the overall transfer function of the opamp with the capacitive feedback becomes an I-V integrator. A set of resistors is used to convert the amplifier's output voltage into current that is supplied to other integrators, or to the same integrator to implement a lossy active-RC integrator. The nonlinearity of the opamp is suppressed because it is employed in a feedback configuration. The proposed integrator, shown in Fig. 2.7c, mimics the same concept. A frequency detector (FD) is used to extract the instantaneous frequency of a VCO. The instantaneous frequency is the derivative of the VCO phase. Hence, the FD works as a feedback differentiator playing the role of the capacitor in active-RC topology. A charge pump is then used to convert the output of the FD into current to be subtracted from the input current of the integrator. Here, the nonlinearity of the VCO is also substantially reduced because of the feedback configuration. The proposed VCO-FD-CP configuration, shown in Fig. 2.7c, can be treated as a linearized CCO (linCCO). A PD followed by a CP is then

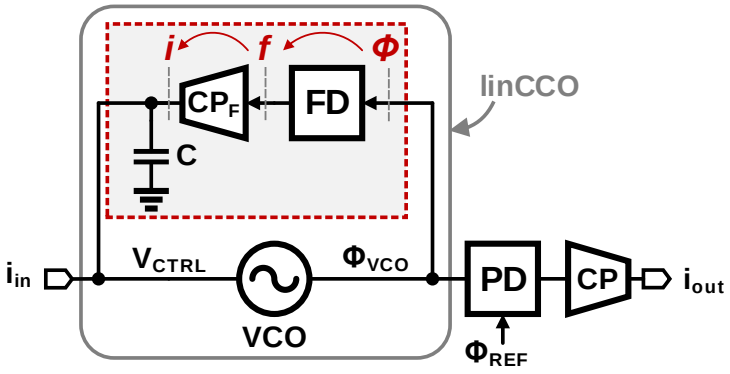
used to convert the linCCO phase into current [14] resulting in a linear I-to-I integrator homologous to the active-RC integrator, shown in Fig. 2.7a.



(a)



(b)



(c)

Figure 2.7: (a) Active-RC integrator employing voltage-current feedback, (b) active-RC integrator with feedback capacitor replaced with its Y-model, and (c) proposed linCCO-based integrator.

The concept of the proposed linearization technique is close to that presented in [66]; however, the FD used here is based on the one-shot generator shown in Fig. 2.8a instead of the switched-capacitor circuit used in [66]. The input-output characteristics of the FD, shown in Fig. 2.8a, is expressed as:

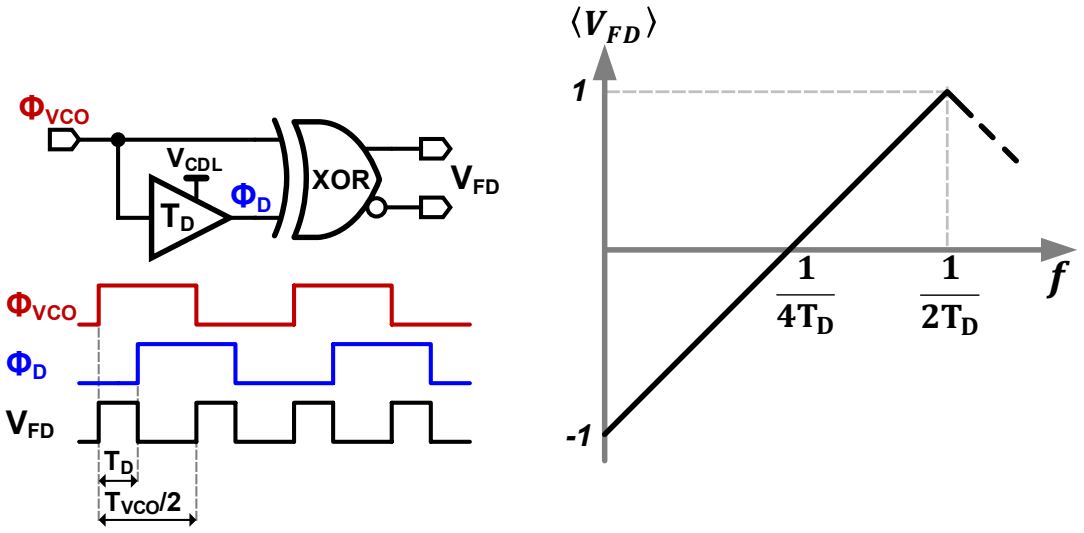
$$\langle V_{FD} \rangle = 4T_D f - 1 \tag{2.18}$$

The linear range of the FD is $1/2T_D$ and centered around $1/4T_D$, as illustrated in Fig. 2.8b. Therefore, for $i_{in} = 0$ the frequency of the linCCO is locked to $1/4T_D$. Moreover, for small-signal ac current, i_{in}(s), the transfer function of the linCCO employing the one-shot FD can be derived as:

$$H_{linCCO}(s) = \frac{\phi_o(s)}{i_{in}(s)} = \frac{2\pi k_{linCCO}}{s} \times \overbrace{\frac{1}{1 + sC\frac{k_{linCCO}}{k_{VCO}}}}^{Non-dominant\,pole}, \tag{2.19}$$

where $k_{linCCO} = {}^{1}/_{(4T_D k_{CPF})}$, which is the gain of the linCCO in Hz/A. A voltage controlled delay line (VCDL) is utilized in the FD to work as a tuning knob for the integrator gain. This tuning knob allows continuous frequency tunability for the proposed linCCO-based filters (to be discussed in Section 2.4.3). The proposed integrator has a high-frequency nondominant pole caused by finite k_{VCO}, which is analogous to the nondominant pole caused by the amplifier's finite UGB in active-RC topology. The nondominant pole must be placed at least tenfold of the corner frequency of filters built using this integrator to avoid Q-enhancement and passband peaking [67]. The frequency of the nondominant pole can be increased by increasing k_{VCO}/C. However, this results in a trade-off between the nondominant pole frequency and the amplitude of the ripples caused by the pulse-frequency modulated (PFM) signal coming from the FD. On the one hand, a large capacitor is needed to filter the PFM signal produced by the FD resulting in a small peak-to-peak triangular ripple voltage at the

input of the linCCO. This relaxes the linearity requirements of the linCCO's feedback CP, as well as other charge pumps that are connected to this node. On the other hand, a larger capacitor pushes the integrator's non-dominant pole to lower frequencies which may limit the highest achievable bandwidth of the proposed topology.

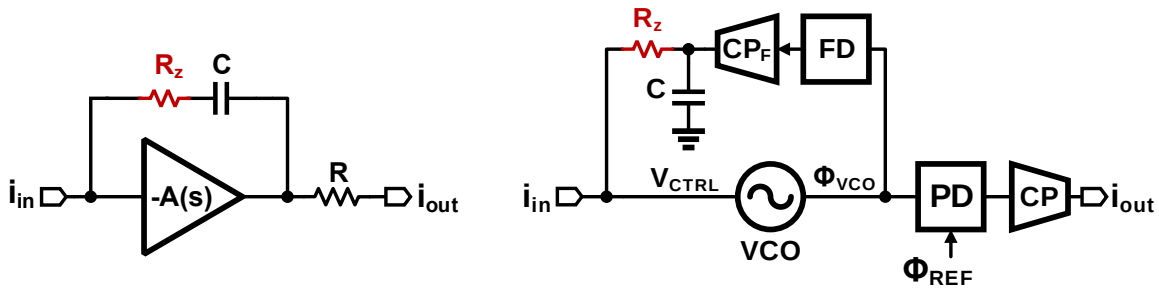


(a) (b)

Figure 2.8: Frequency detector: (a) simplified schematic and timing diagram, and (b) input-output characteristics.

2.3.1 Integrator Frequency Compensation

To resolve the trade-off between the nondominant pole frequency and the amplitude of the PFM ripple signal coming from the FD, an integrator frequency compensation (IFC) technique is used that is analogous to the R_z compensation scheme used in active-RC filters [68, 69]. The compensation scheme for active-RC integrators, employing an amplifier with finite unity gain bandwidth (UGB), ω_u, utilizes a series resistor in series with the in-



(a) (b)

Figure 2.9: R_z compensation in (a) active-RC integrators, and (b) the proposed linCCO-based integrator.

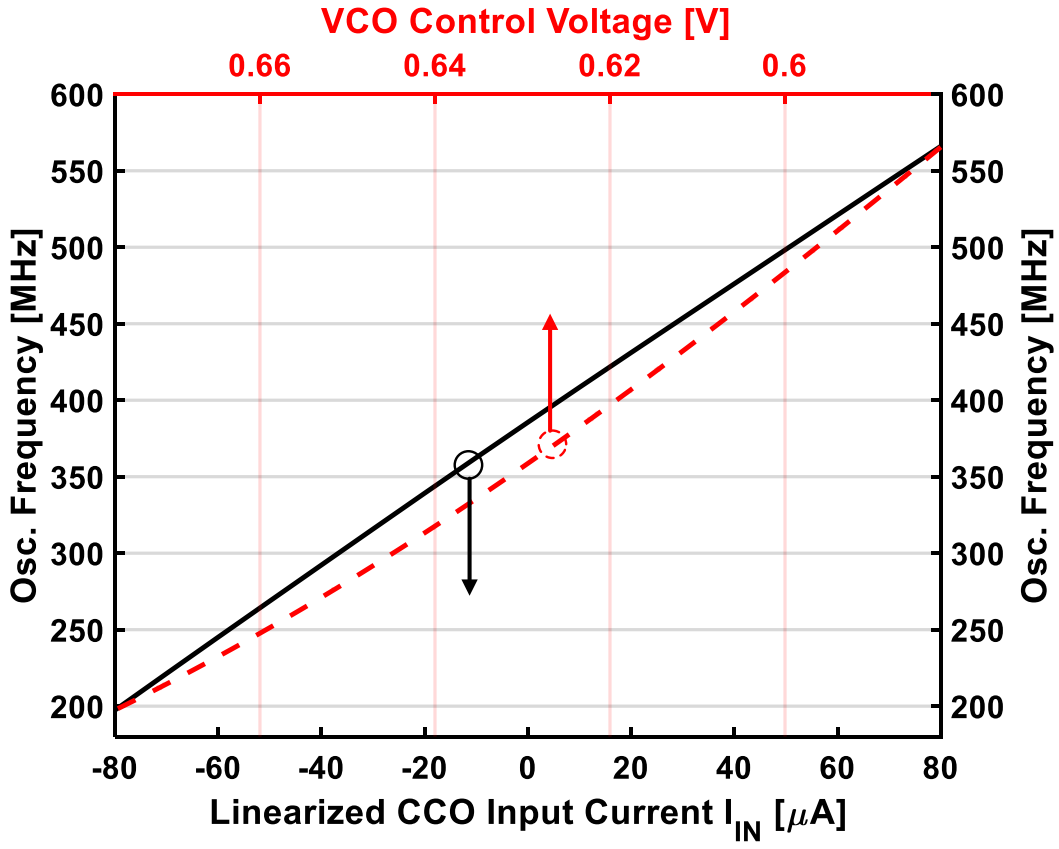


Figure 2.10: Comparison between the simulated tuning curve of the open-loop VCO employed in the linCCO (red dashed line) and the closed-loop linCCO (solid black line).

Table 2.1: Comparison between the simulated relative nonlinearity of the open-loop VCO employed in the linCCO, and the closed-loop linCCO

	Relative Nonlinearity	
	Single-ended	**Pseudo-differential**
Open-loop VCO employed in linCCO	4.46%	0.62%
Closed-loop Linearized CCO	0.65%	0.05%

tegrating capacitor, as shown in Fig. 2.9a. The added resistor creates an extra zero in the transfer function, which cancels the nondominant pole when $\omega_u = 1/R_zC$ [68]. A similar compensation scheme can be utilized in the proposed integrator topology, as shown in Fig. 2.9b. The additional series resistor, R_z, adds a zero to the transfer function of the linCCO to become:

$$H_{linCCO}(s) = \frac{2\pi k_{linCCO}}{s} \times \frac{1 + sCR_z}{1 + sC\frac{k_{linCCO}}{k_{VCO}}} \tag{2.20}$$

The additional zero can compensate for phase lag caused by the nondominant pole if $R_z = k_{linCCO}/k_{VCO}$. Hence, a bigger capacitor can be used, which helps to filter out the high-frequency ripple signal of the FD while preserving the accuracy of pass-band and stop-band responses of filters employing the proposed linCCO integrator.

The simulated I-to-F conversion curve of the proposed linCCO, and the V-to-F conversion curve of the open-loop VCO employed inside linCCO are shown in Fig. 2.10 for the same output frequency. The I-to-F conversion curve of the linCCO is visually more linear. The worst-case deviation of these tuning curves from the best fit lines, i.e., relative nonlinearity, are reported in Table 2.1 which shows $\sim 6.9\times$ improvement for single-ended linCCO implementation and $\sim 12.4\times$ improvement for the pseudo-differential linCCO implementation.

2.3.2 Noise Analysis

The noise of the proposed linCCO-based integrator can be evaluated using the noise model that is illustrated in Fig. 2.11. The primary noise contributors are the VCO, the delay line, and the charge pumps. The power spectral density (PSD) of the phase fluctuations of the VCO and delay line are denoted by $S_{\Phi,VCO}$ and $S_{\Phi,DL}$, respectively. The PSD of the output-referred noise currents produced by the charge pumps are denoted by $S_{i,CPF}$ and $S_{i,CP}$ for the feedback and output charge pumps, respectively. The phase detector and the XOR gate of the FD contribute negligible noise and thereby they are excluded from this analysis. The compensation resistor, R_z, is effective at high frequency to cancel the non-dominant pole, hence its in-band noise contribution is also negligible. The PSD of the input-referred noise current of the linCCO-based integrator, S_i, can be expressed as:

$$S_i = \frac{S_{\Phi,linCCO}}{\left|H_{linCCO}(s)\right|^2} + \frac{S_{i,CP}}{\left|H_{linCCO}(s)k_{PD}k_{CP}\right|^2} \tag{2.21}$$

where $S_{\Phi,linCCO}$ is the PSD of the phase fluctuations of the linCCO, that is given by:

$$S_{\Phi,linCCO} = \left|H_{linCCO}(s)\right|^2 \left(S_{\Phi,DL}k_{XOR}^2k_{CPF}^2 + S_{i,CPF} + S_{\Phi,VCO}\left|\frac{s^2C}{2\pi k_{VCO}}\right|^2 \right), \tag{2.22}$$

From (2.22), it is worth noting that the phase noise of the VCO is high-pass filtered when employed in the linCCO configuration. However, the phase noise of both the delay line and the feedback CP are integrated. Hence, the low-frequency noise is dominated by the delay line and the feedback CP used for linearization, whereas the phase noise of the VCO adds up only at higher frequency offset [70]. Fig. 2.11 illustrates the effect of different noise contributors to the phase noise of the linCCO, $S_{\Phi,linCCO}$, while taking into account only thermal noise for simplicity. The phase noise of the linCCO has two regions of 20 dB/decade roll-off with an intermediate plateau. It is worth noting that the proposed integrator trades off

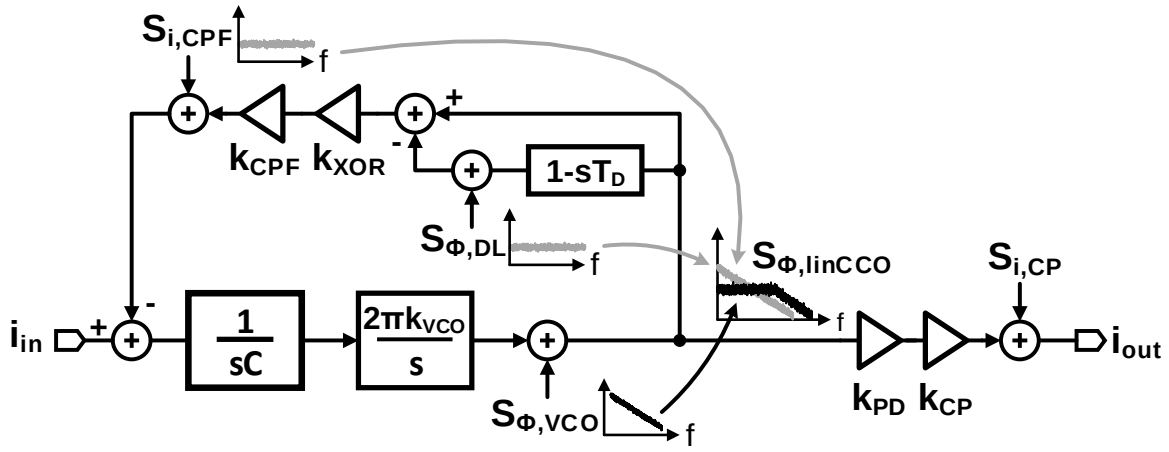


Figure 2.11: Noise model of linCCO-based integrator.

the noise for linearity since the linCCO has more noise contributors compared to an open-loop CCO such as the one that was used in [14]. Moreover, when comparing the proposed integrator with the active-RC topology, the feedback differentiator of the linCCO is noisy compared to the noiseless feedback capacitor of active-RC topology.

2.4 Filter Architecture using linCCO-based Integrator

2.4.1 First-Order Section

The simplified block diagram of a first-order low pass filter using the proposed linearized CCO is depicted in Fig. 2.12a. In analogy to active-RC architecture, FD-CP and PD-CP structures are analogous to the feedback capacitor and resistor in a first-order active-RC filter, respectively. In the proposed topology, a single-phase high-frequency VCO is used so that only single FD and CP are used in linCCO implementation. The linCCO is followed by a multi-phase generator, basically a frequency divider, that is used to generate M phases in order to produce an M-phase PWM signal at the output of the phase detector to suppress the PWM spurious tones by a factor of M. The transfer function of the low-pass filter is given

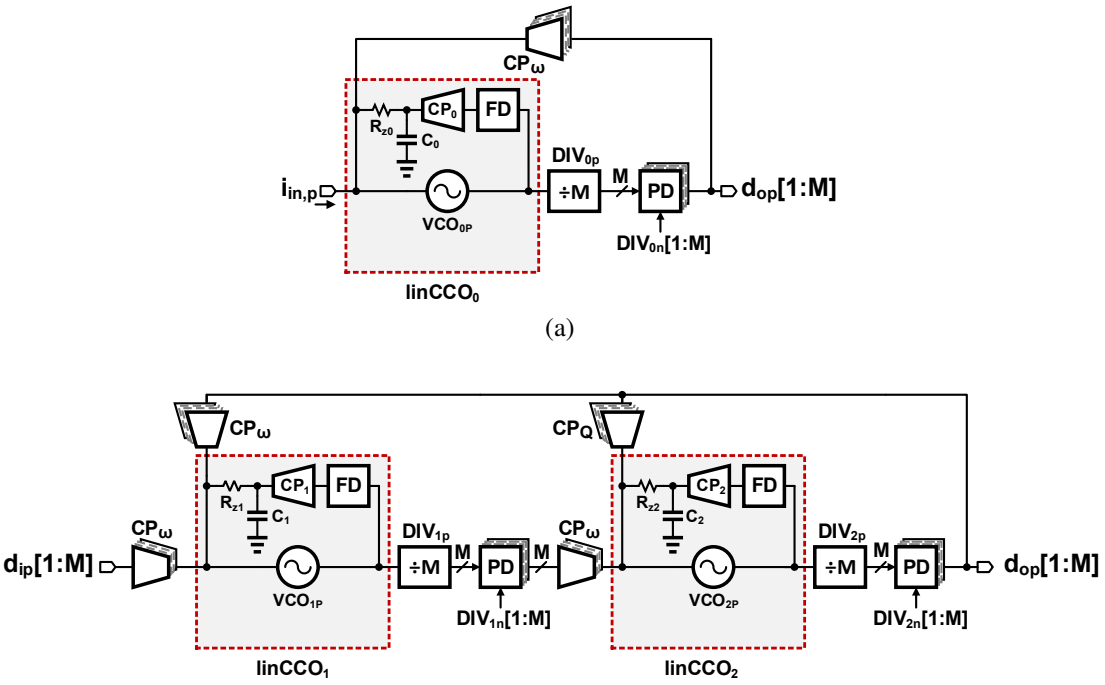


Figure 2.12: Filter design using linCCO integrator (only half circuit is shown for simplicity): (a) first-order section and (b) Tow-Thomas biquad.

by:

$$H_{LPF1}(s) = \frac{1}{k_{CP\omega}} \times \frac{1}{1 + \frac{s}{4\pi k_{linCCO} k_{DIV} k_{PD} k_{CP\omega}}} \tag{2.23}$$

where k_{linCCO}, k_{DIV}, k_{PD}, and $k_{CP\omega}$ denote the gain of the linearized-CCO, M-phase generator, phase detector, and feedback charge pump, respectively. Since $k_{linCCO} = 1/\left(4T_D k_{CP0}\right)$, the -3 dB bandwidth is given by:

$$f_{3dB} = \frac{k_{DIV} k_{PD}}{2T_D} \left(\frac{k_{CP\omega}}{k_{CP0}}\right) \tag{2.24}$$

It is worth noting from (2.24) that the ratio $k_{CP\omega}/k_{CP0}$ is maintained across PVT variations because it is a ratio between the switched current sources used to build the charge pumps. Hence, the filter's bandwidth is inversely proportional to T_D, or subsequently di-

rectly proportional to the free-running frequency of the linearized CCO, $f_{linCCO} = 1/4T_D$. Therefore, the filter's bandwidth can be well-controlled across PVT variation by controlling T_D or f_{linCCO}. This can be accomplished by using a delay-locked loop (DLL) or by a phase-locked loop (PLL) that locks a replica delay line or a replica linearized CCO, respectively, to a reference clock. This property is similar, to some extent, to switched-capacitor (SC) filters where the filters' critical frequencies are a function of the capacitor ratio and clock frequency. Needless to say that the switched-current ratio in the proposed filter is not as well-controlled as the capacitor ratio in SC filters. However, the accuracy of the proposed filter can be improved across PVT variations if the area and speed are traded off.

2.4.2 Biquadratic Section

The simplified block diagram of a Tow-Thomas biquad using the proposed linCCO integrator is shown in Fig. 2.12b. The architecture is homologous to active-RC topology, where each resistor is replaced by a PD-CP structure, each capacitor is replaced by a FD-CP, and each opamp is replaced with a VCO. Therefore, the design methodology is similar to conventional active-RC filters. The transfer function of the proposed Tow-Thomas biquad is given by:

$$H_{LPF2}(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{2.25}$$

where $\omega_0 = 2\pi f_0$ and Q are the biquad's natural frequency and quality factor, respectively, and are given by:

$$f_0 = \frac{k_{DIV}k_{PD}}{2T_D}\left(\frac{k_{CP\omega}}{\sqrt{k_{CP1}k_{CP2}}}\right) \tag{2.26}$$

$$Q = \frac{k_{CP\omega}}{k_{CPQ}}\sqrt{\frac{k_{CP1}}{k_{CP2}}} \tag{2.27}$$

Similar to the first-order filter, the biquad's natural frequency is a function of the ratio of current sources, and T_D. It is also worth noting that the biquad's quality factor is a ratio between two current sources that can be controlled over PVT variations.

2.4.3 DLL-based Frequency Tuning

The proposed linCCO-based filter is tuned using a master-slave tuning scheme shown in Fig. 2.13a. The slave is the proposed linCCO-based filter. The master contains a scaled replica delay line similar to that used in the linCCO FD. A feedback loop, created using a DLL, adjusts the delay of the replica delay line of the master to equal one period of the accurate reference clock Φ_{ref}. Because the same control voltage is also applied to the delay lines inside the FDs of the proposed linCCO-based filter, the filter will have time constants proportional to T_{ref}.

Two-hundred runs of Monte-Carlo simulation (process+mismatch) are carried out to validate the effectiveness of the proposed frequency tuning scheme, as depicted in Fig. 2.13b and 2.13c, for the high-Q biquad of a 5th-order Butterworth filter ($f_0 = 20$ MHz and $Q = 1.62$). In Fig. 2.13b, white bars and black bars show the simulated percentage of deviation from the expected ω_0 ($\Delta\omega_0/\omega_0 \cdot 100\%$) without tuning and with tuning enabled, respectively. The statistical data are fitted to the Gaussian distribution, and the standard deviation ($\sigma_{\Delta\omega_0/\omega_0}$) is obtained, which is reduced by $\sim 7.2\times$ when the frequency tuning is enabled. Fig. 2.13c depicts the effect of the frequency tuning scheme on the percent deviation of the quality factor ($\Delta Q/Q \cdot 100\%$), which shows $\sim 2\times$ reduction in the simulated $\sigma_{\Delta Q/Q}$. Although the frequency tuning scheme does not directly affect the quality factor, as in (2.27), it lowers the variations of the integrators' nondominant pole (2.20). Hence, it reduces the relative error between the nondominant pole and compensation zero, and indirectly attributes to lower Q variations.

2.4.4 Fifth-Order Butterworth Filter Prototype

An 8-phase fifth-order prototype filter was implemented to prove the proposed concept. The block diagram of the filter prototype is shown in Fig. 2.14. It comprises a cascade of one first-order stage followed by two Tow-Thomas biquad stages. The cascaded stages are

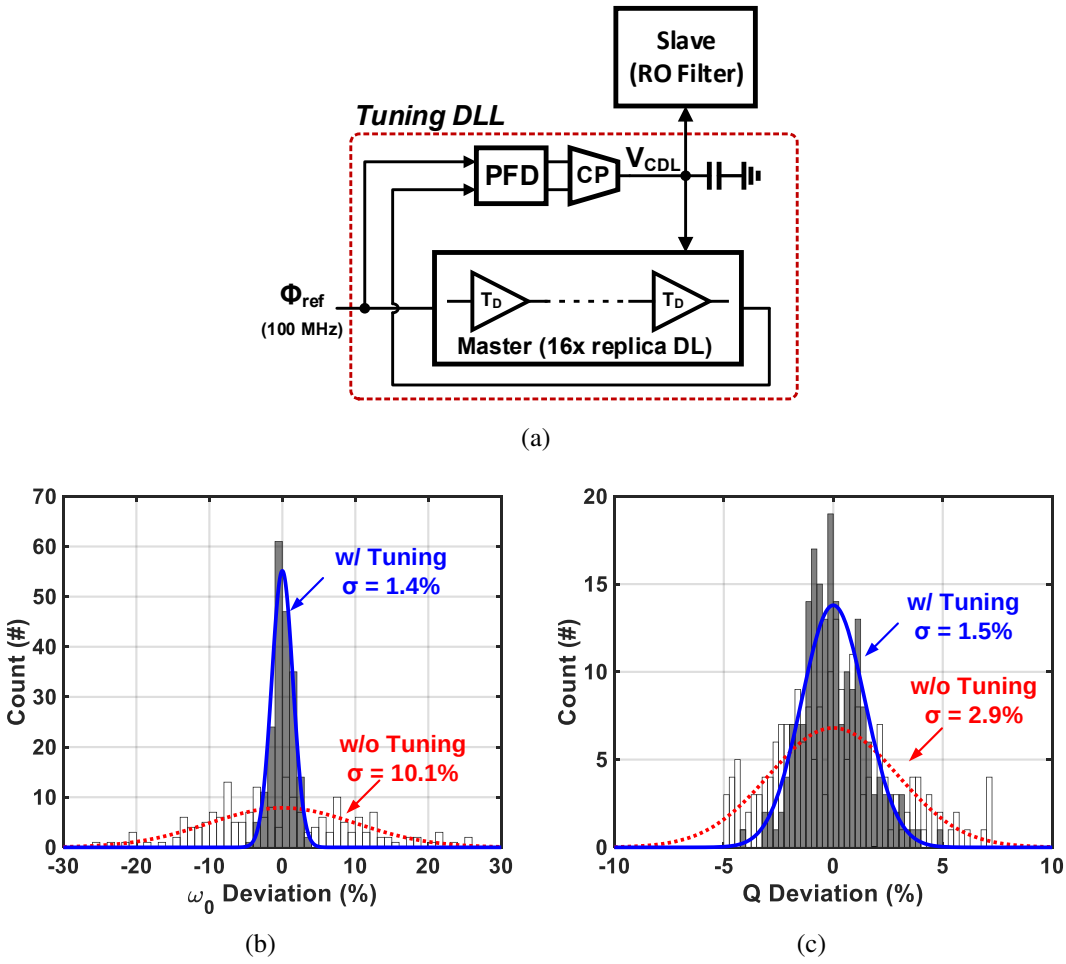


Figure 2.13: DLL-based master-slave frequency tuning scheme for the linCCO-based filter, and 200-run Monte-Carlo simulation results (process+mismatch) of a biquad ($f_0 = 20MHz$ and $Q = 1.62$): (a) block diagram of the tuning scheme, (b) biquad's ω_0 deviation, and (c) biquad's Q deviation.

ordered from low-Q to high-Q to prevent overloading intermediate stages, which yields better linearity [71]. A digitally-controlled resistor R_{IN} is used as a voltage-to-current converter at the input. The 8-phase PWM output of each stage is converted to current through charge pumps and is supplied to the following stage. The 8-phase PWM output of the last stage is converted to a voltage by a resistive adder [14]. A digitally controlled master bias block sources the current to the filter's stages to set the bandwidth and quality factor of each stage.

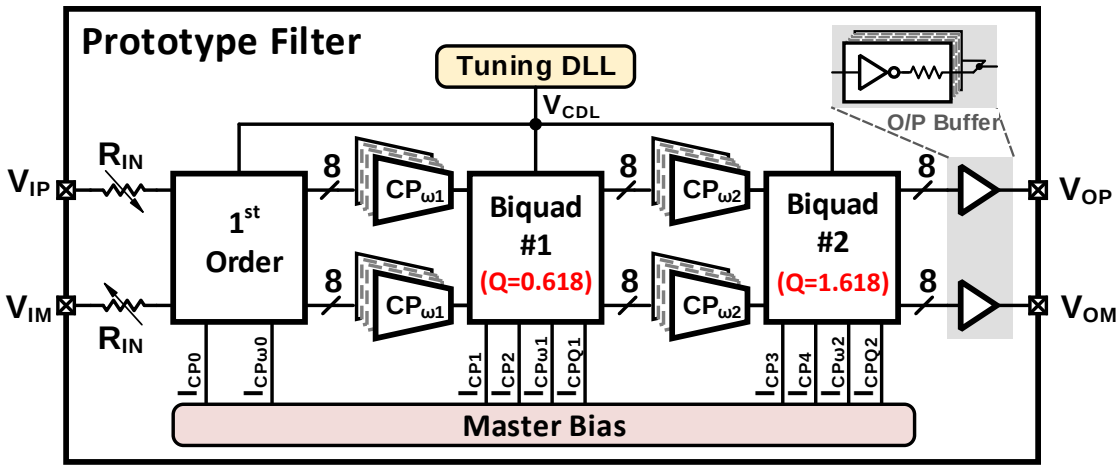


Figure 2.14: Fifth-order Butterworth filter prototype.

The tuning DLL supplies the control voltage (V_{CDL}) of the delay lines inside the FDs of the linCCOs.

2.5 Circuit-Level Implementation

2.5.1 Ring Oscillator

The circuit diagram of the ring oscillator is shown in Fig. 2.15. It consists of 12 pseudo-differential delay stages, each implemented by using two current starved inverters with two cross-coupled feedforward resistors implemented using CMOS transmission gates. The feedforward resistors are used to attenuate the common-mode (CM) signals while differentially coupling the two output clocks together. The aforementioned technique is favored over the latch-based delay cell where two weak inverters are connected back-to-back between the differential outputs of each delay cell because feedforward topology has superior noise performance [72]. The 12-stage RO is biased by a weak PMOS transistor that sets the minimum frequency of oscillation, and a control PMOS transistor, M_C, that is driven by the control voltage V_{CTRL}. Minimum length devices are used in the RO delay stages because the oscillator's flicker noise is highpass filtered as a byproduct of the proposed linearization

technique, and the width is optimized to satisfy the required noise performance without burning unnecessary power. An AC-coupled inverter with resistive feedback is used to amplify the limited-swing outputs of the RO to rail-to-rail, and the cross-coupled inverters are used to ensure the outputs are complimentary with minimum duty cycle distortion.

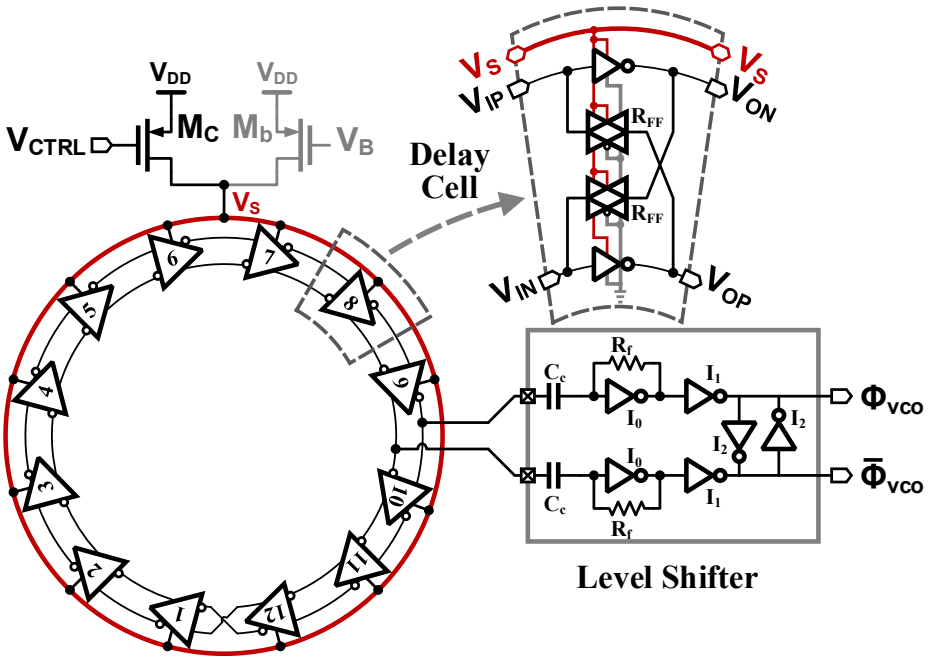


Figure 2.15: Pseudo-differential 12-stage ring oscillator and the delay cell.

2.5.2 Delay Line

The delay-line (DL) of the FD is implemented using six supply-regulated pseudo-differential delay stages, as shown in Fig. 2.16. Each delay stage is composed of two CMOS inverters with two weaker cross-coupled inverters at the output to ensure the differential operation of the delay-line. The output of the delay-line is not full-swing; hence a level shifter is used to amplify the DL output to rail-to-rail.

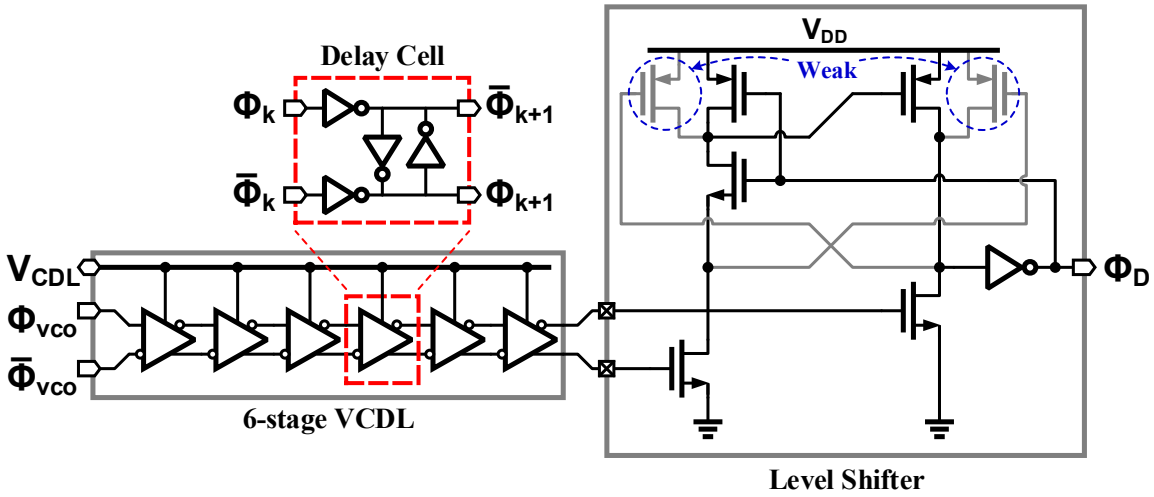


Figure 2.16: FD's 6-stage VCDL, the delay cell, and a level shifter to convert VCDL output to a rail-to-rail signal.

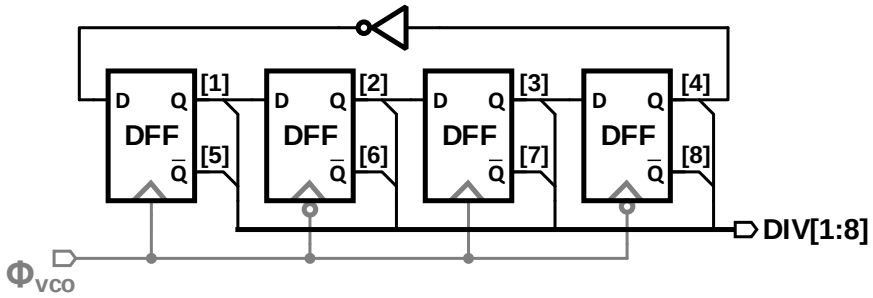
2.5.3 Multi-Phase PWM Generator

The outputs of the linCCO integrators are applied to the multi-phase PWM generator to generate M-phase PWM signals with precisely matched duty cycles. In this prototype, $M = 8$ was chosen as a trade-off between performance and complexity, resulting in 18 dB attenuation in the PWM spurious tones. The 8-phase PWM generator is implemented in two stages; the first stage is a divide-by-4 circuit using a dual-edge triggered ring counter in which the output of a 4-bit shift register is inverted and fed-back into its input as shown in Fig. 2.17a. The divide-by-4 circuit is built of standard CMOS DFFs as unit building blocks. The linCCO followed by the divide-by-4 block can be thought of as an 8-phase linCCO running at $f_{CCO}/4$. Therefore, the subsequent blocks can operate at a lower frequency, which reduces their design complexity and lowers their dynamic power consumption. This solution was chosen over implementing an 8-phase linCCO running at $f_{CCO}/4$, because an 8-phase linCCO will require the linearization technique to be replicated for each phase, which adds design complexity.

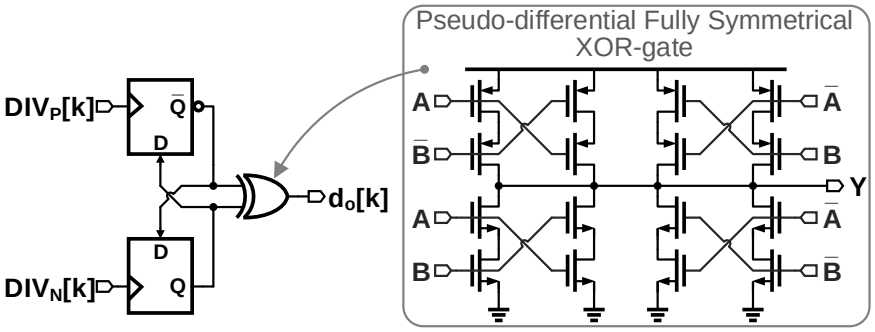
The second stage of the 8-phase PWM generator is eight 2-state phase detectors shown in Fig. 2.17b. The 2-state PD has a 2π linear range; thus, the phase difference between the two linCCOs, i.e., before the divider, can vary from 0 to 8π without the output being heavily distorted. The 2-state PD is based on a JK flip-flop that can be built symmetrically using two DFFs and an XOR gate. A pseudo-differential fully symmetrical XOR gate is utilized, as shown in Fig. 2.17b, to minimize output duty cycle distortion. The timing diagram of the proposed 8-phase PWM generator is illustrated in Fig. 2.17c.

2.5.4 Charge Pump

The schematic of the charge pump is shown in Fig. 2.18 [73]. A single-ended source-switched topology is used because of its fast switching and lower charge injection compared to drain-switched charge pumps. Transistors M_{CN} and M_{CP} are the current source devices, while switches M_{SN} and M_{SP} control the direction of the current flow to the charge pump output. The helper transistors M_{HN} and M_{HP} are used to ensure fast turn-off of current source devices.



(a)



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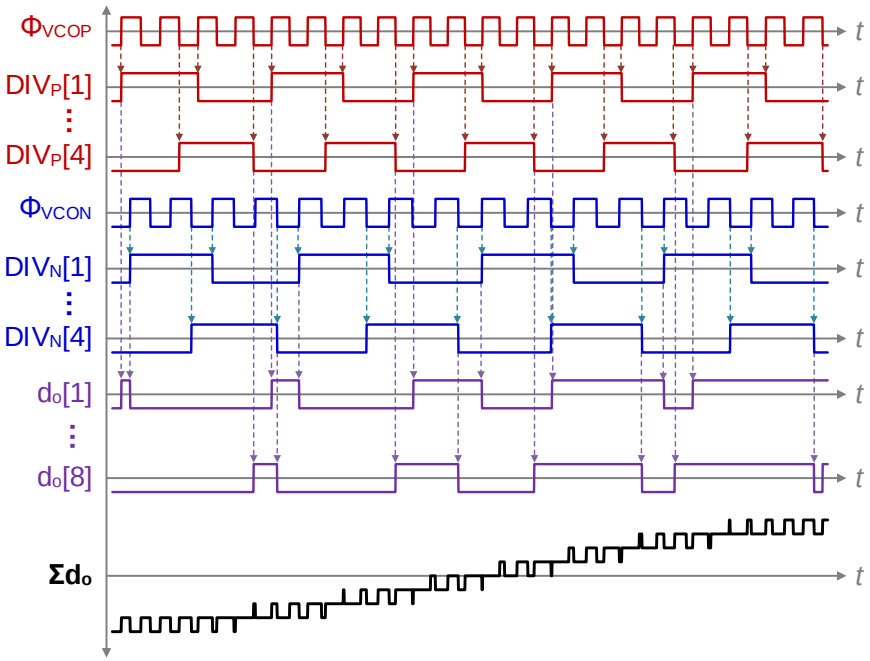


(c)

Figure 2.17: 8-phase PWM generator: (a) divide-by-4 circuit, (b) two-state phase detector with pseudo-differential fully-symmetric XOR gate, and (c) timing diagram.

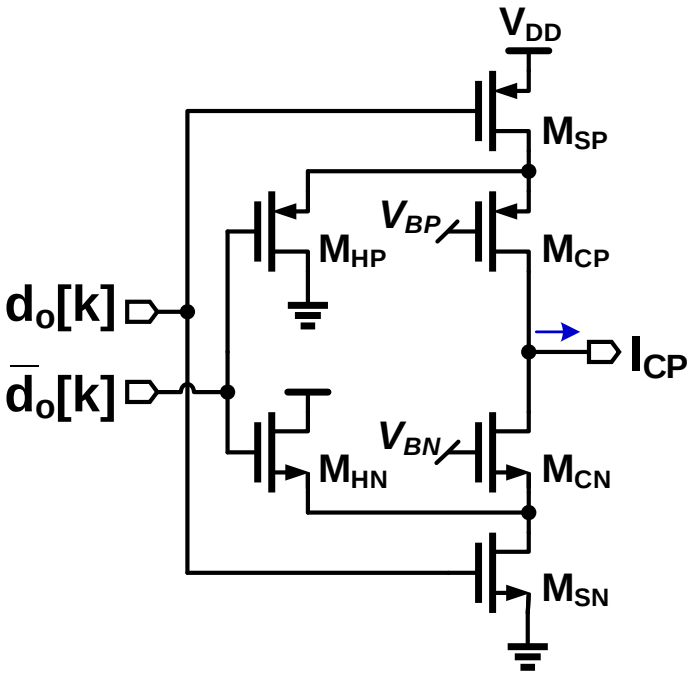


Figure 2.18: Source-switched charge pump.

2.6 Experimental Results

The fifth-order prototype filter is implemented in a 130 nm CMOS process. A die micrograph of the chip is shown in Fig. 2.19. The total die area is 1 mm^2 and the effective filter's area is 0.39 mm^2. The filter's chip is packaged in QFN44 and mounted on a PCB, where all the connectors and power supply filters for low noise requirements are placed. All digital controls are generated by a DAQ card and applied to the prototype chip using an on-chip scan chain. Fig. 2.20 describes the complete test setup that is used for the frequency response, noise, and linearity characterization.

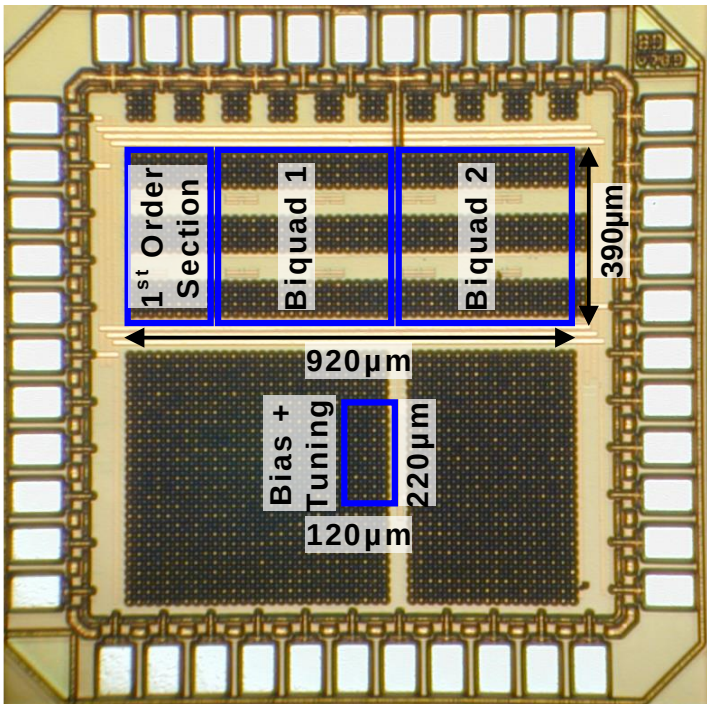


Figure 2.19: Die micrograph of the prototype filter.

Fig. 2.21 shows the measured filter transfer function and the ideal fifth-order Butterworth filter response for each bandwidth setting, which shows the frequency response closely

matching the ideal Butterworth response for bandwidth settings up to $22.5\,MHz$. A small peaking ($< 0.6dB$) is observed at the maximum bandwidth setting because of parasitic poles in the feedback loop. The bandwidth was adjusted through digitally controlled bias currents sourced to the charge pumps.

The process resilience achieved by the proposed frequency tuning scheme was verified through temperature and voltage sweeps, as shown in Fig. 2.22. The 3dB-bandwidth variation versus temperature is shown in Fig. 2.22a with and without the frequency tuning scheme. The temperature sweep shows at least a $2.5\times$ reduction in bandwidth variation when the frequency tuning scheme is enabled. The worst-case temperature variation is $\pm 3.5\%$ over the temperature range -40 °C to 85 °C for the 20-MHz bandwidth setting. It should be noted that lower bandwidth settings achieve much lower variations because at smaller bandwidth settings, the filter becomes less susceptible to the nondominant pole variations caused by k_{VCO}. Fig. 2.22b shows the 3dB-bandwidth variation versus supply voltage; it also shows worst case variation of $\pm 0.5\%$ over the supply-voltage range from 0.9 V to 1.2 V, which is 22.5 times better than the untuned case.

The linearity performance of the proposed filter prototype is validated through the two-tone test of the 10-MHz filter bandwidth setting and is depicted in Fig. 2.23a. The in-band IIP3 (IB-IIP3) is measured by applying two tones at 1.95 MHz and 2.05 MHz, yielding a measured IB-IIP3 of 26.2 dBm. The out-of-band IIP3 (OB-IIP3) is characterized by applying two tones at 20 MHz and 38 MHz, yielding a measured OB-IIP3 of 33.8 dBm as shown in Fig. 2.23a. The measured filter output spectrum with full-scale input of +2 dBm or 796 mV_{ppd} is shown in Fig. 2.24a. This is $\sim 40\%$ of the 1 V supply. The spurious-free dynamic range (SFDR) is 60.8 dB. Although the third-order nonlinearity is improved over RO filter in [13], our prototype's even-order linearity performance was limited by an underestimated mismatch in the pseudo-differential implementation. The wideband spectrum is shown in Fig. 2.24b, which reveals the remaining PWM tones because of the underestimated

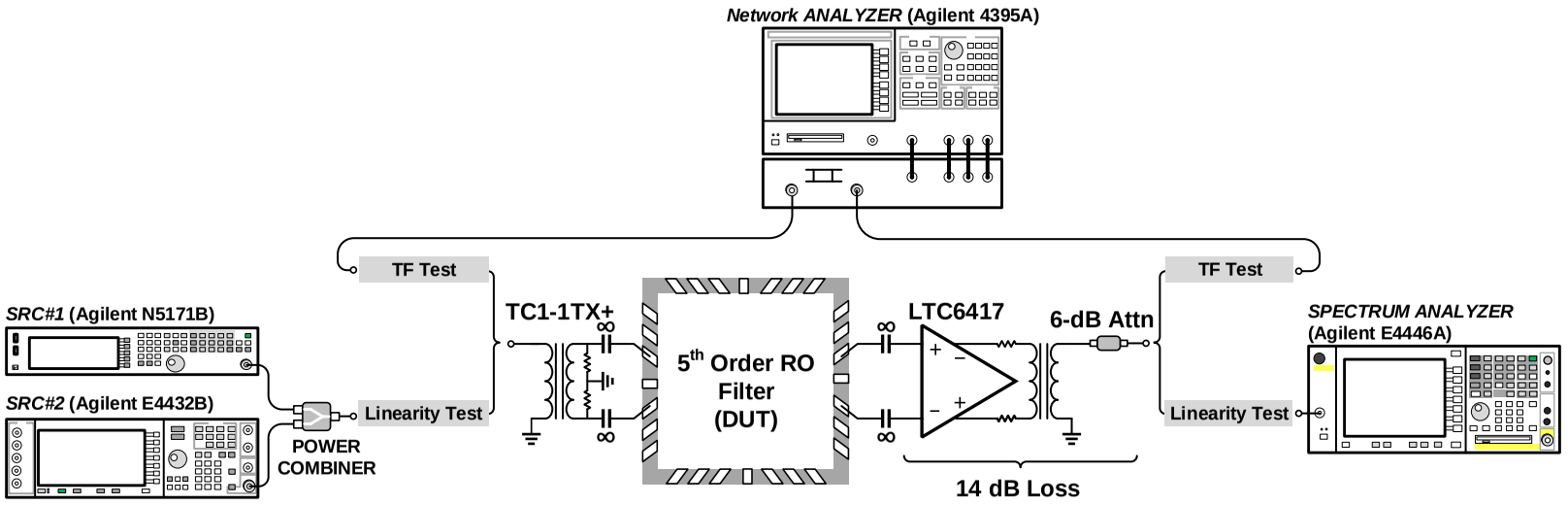


Figure 2.20: Lab measurement setup.

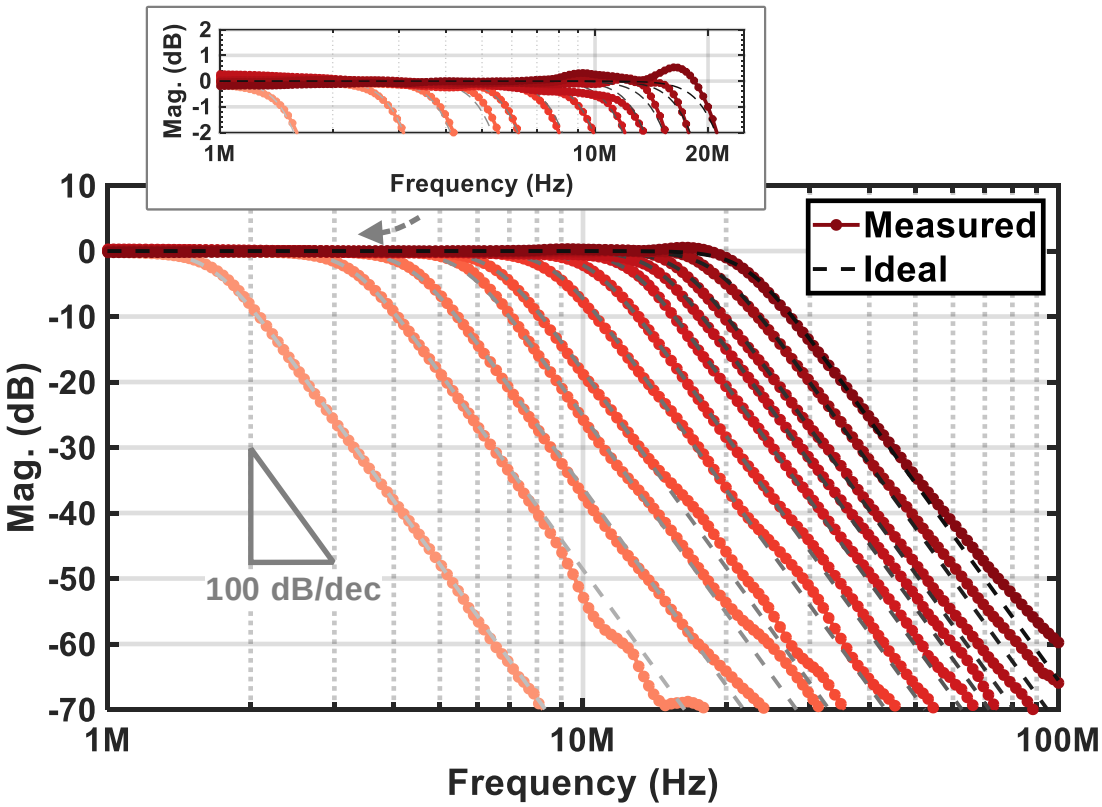
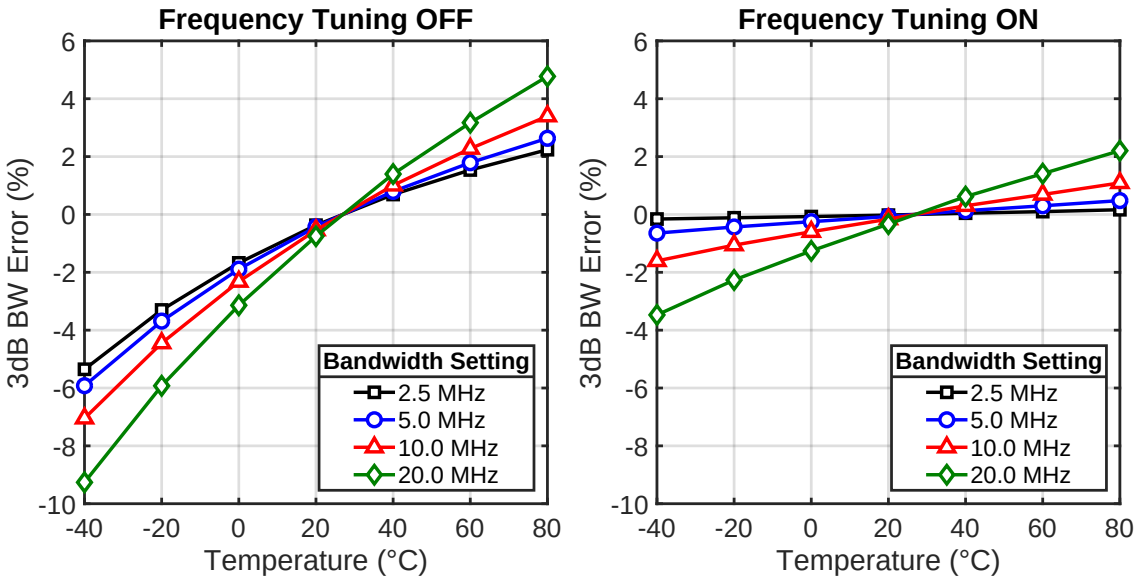


Figure 2.21: Measured filter transfer function (solid lines) for different settings (BW = 1.5–22.5 MHz) and superimposed ideal fifth-order Butterworth transfer functions (dashed lines) for comparison.

mismatch.

Table 2.2 shows a comparison of this filter prototype performance against state-of-the-art RO filters [13, 15, 74], a switched-mode opamp-RC (PWM-based) filter [58], and some state-of-the-art voltage-mode filters that uses conventional topologies such as OTA-C [54,75] and active-RC [56, 76]. The proposed filter achieves a competitive IIP3 among state-of-the-art RO filters and is very close to the opamp-based active-RC filter [56]. The noise performance is higher than [13]; however, this is attributed to the extra charge pump and frequency detector used in the linCCO, as discussed in Section 2.3.2, and because the filter is



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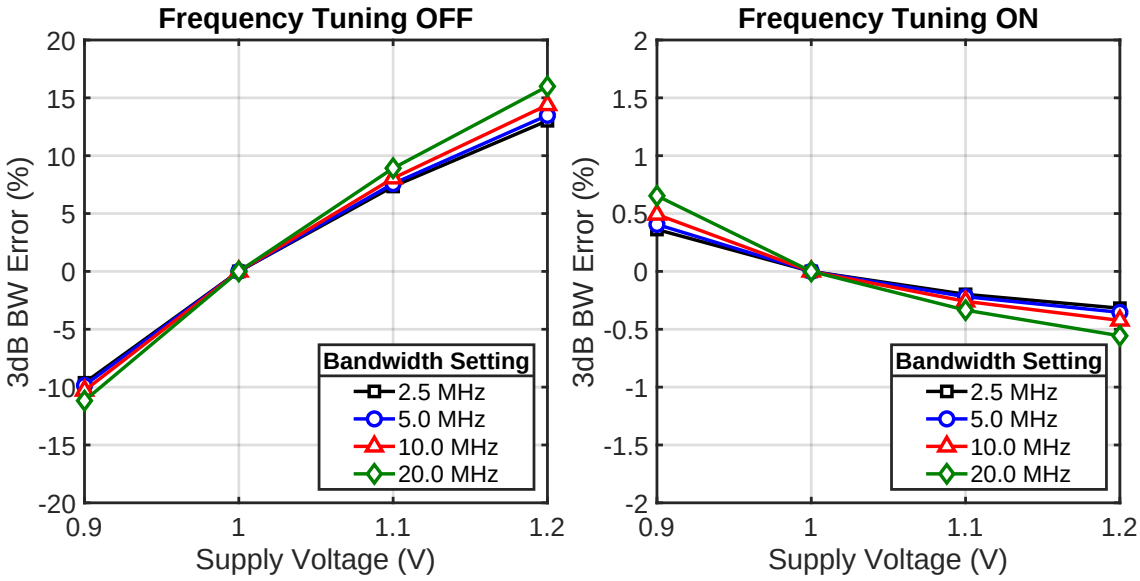
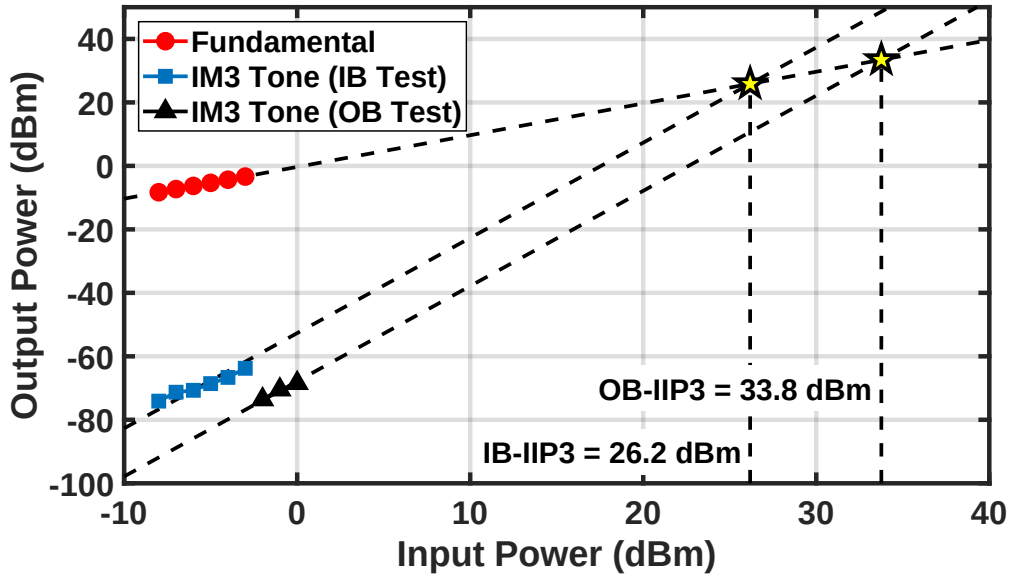


(b)

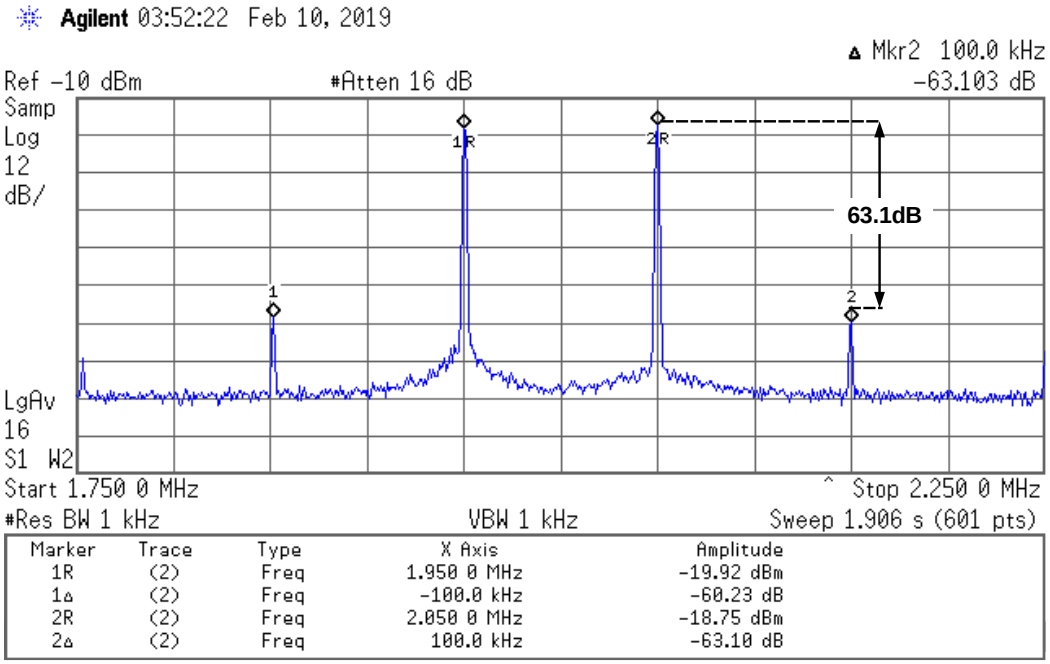
Figure 2.22: Measured filter's 3dB-bandwidth error versus temperature and supply voltage with and without tuning: (a) temperature sweep and (b) supply voltage sweep.

of a higher order (hence more noise). The proposed topology can lend itself to high-linearity applications, whereas [13] can be utilized in low-noise high-frequency applications. This

is analogous to opamp-based counterparts, whereas OTA-C topology is more suitable for low-noise high-frequency applications, while active-RC topology is more suitable for high-linearity applications. Additionally, the proposed linCCO-based filter topology enables the use of a simple but effective DLL-based frequency tuning scheme, which achieves a worst-case 3-dB bandwidth variation of $\pm 3.5\%$ over the -40 °C to 85 °C temperature range and a supply voltage range from 0.9 to 1.2 V. Two figure-of-merits (FoM) are used for a fair comparison with prior work to account for key performance metrics such as power, noise (P_N), linearity (IIP_3), order (N), and bandwidth (f_{BW}), as shown in Table 2.2. FoM_2 [76, 77] normalizes FoM_1 [78] by the ratio between the lower third-order inter-modulation tone $f_{IM3,Low}$ and the poles frequency f_{Poles} as discussed in [77]. The proposed topology achieves an excellent FoM_2 among recently published switched-mode and RO-based filters and is competitive with voltage-mode active-RC and OTA-C filters. It should be noted the proposed prototype is in an older technology node compared to other switched-mode and RO-based filters. In summary, this work provides a high linearity performance, wide-range tunability, and the best process resilience compared to the recently published switched-mode and RO-based filters.

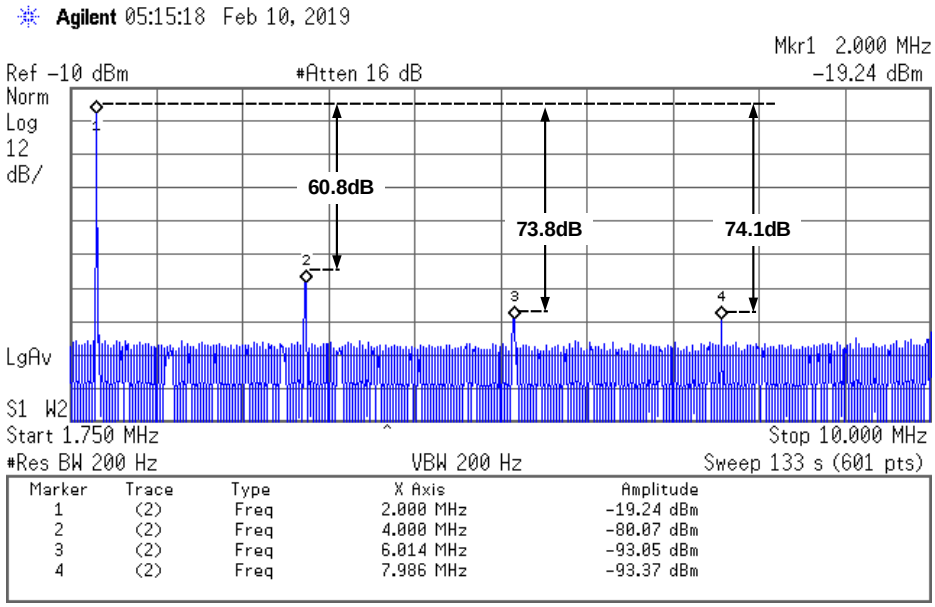


(a)

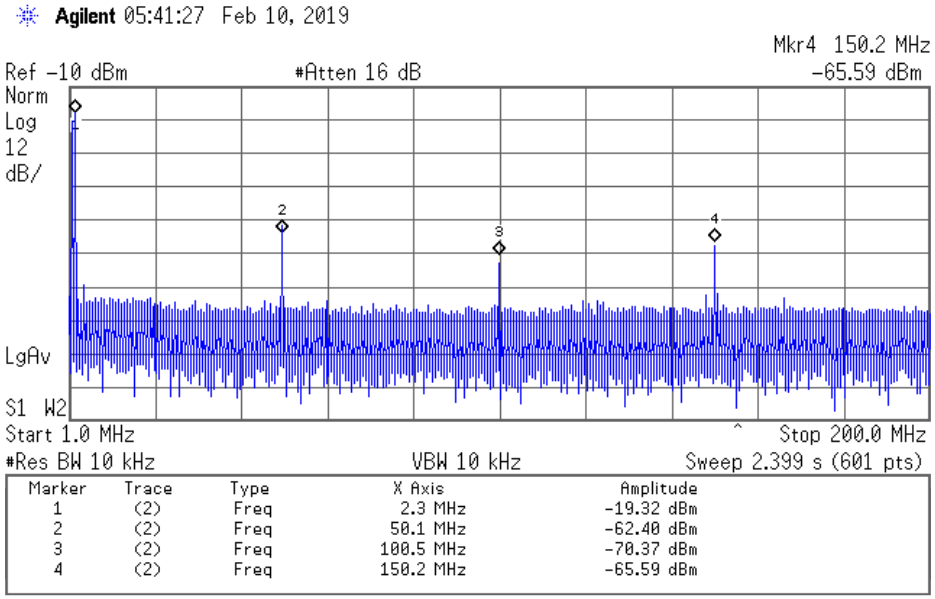


(b)

Figure 2.23: Two-tone linearity measurements: (a) input power (P_{in}) sweep with two-tone frequencies $f_{1,2} = 1.95$ MHz and 2.05 MHz for the IB-IIP3 test and $f_{1,2} = 20$ MHz and 38 MHz for the OB-IIP3 test, and (b) output spectrum for $P_{in} = -4$ dBm, $f_{1,2} = 1.95$ MHz and 2.05 MHz.



(a)



(b)

Figure 2.24: Measured filter's output spectrum for a 2 MHz input signal at a full scale of 2 dBm : (a) close-up (0–10 MHz) showing an in-band spurious-free dynamic range (SFDR) of 60.8 dB and (b) the complete spectrum (0–200 MHz) showing an incomplete cancellation of the ring oscillator (RO) spurs.

Table 2.2: Performance Summary and Comparison with the State-of-the-Art Filter Implementations

	Phase/Time-Mode					Voltage/Current-Mode			
	This Work	**ISSCC '12** [13]	**ESSCIRC '14 [15]**	**TCAS-II '20 [74]**	**JSSC '14 [58]**	**JSSC '09 [56]**	**JSSC '17 [76]**	**JSSC '11 [75]**	**JSSC '10 [54]**
CMOS Technology [nm]	130	90	55	65	65	130	180	90	130
Filter Topology	RO Integrator using linCCO	RO Integrator	ROA-UGB-RC	ROA-RC	SMOA-RC†	Active-RC	Active-RC & Active-gm-RC	OTA-C	OTA-C
Filter Order	5^{th}	4^{th}	4^{th}	4^{th}	4^{th}	5^{th}	4^{th}	6^{th}	2^{nd}
Supply Voltage [V]	1.0	0.55 0.9	1.2	0.9	0.6	1.0	1.8	1.0	1.2
Bandwidth [MHz]	1.5–22.5	7 30	40	25	70	1–20	22.5	8.1–13.5	200
Power [mW]	6.2–8.9	2.9 19.1	7.8	8.2	26.2	3–7.5	12.6	4.35	20.8
IB-IIP3 [dBm]	26.2	N/A 16.7	27.3	22.6	36[c]	26–31.3	21.5	22.1	14
OB-IIP3 [dBm]	33.8	N/A N/A	22.5	13.9	N/A	8–52.8	N/A	17.5–18.9	12.4
IR Noise [nV/$\sqrt{Hz}$]	112.8	23.7 32.8	96	25.15[a]	43.6	52–85	18.34	75	35.4
Area [mm^2]	0.39	0.29	0.07	0.11	0.38	1.53	0.35	0.24	0.5
Frequency Tuning	✓	✗	✗	✗	✗	✓	✗	✗	✗
Bandwidth VT Variations	±3.5%	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
FoM$_1$ [dB(j^{-1})]	153.4	150.4	155.5	159.3	161.5	158.4–158.7	158.3	156.2	147.5
FoM$_2$ [dB(j^{-1})]	146.4	138.6	142.5	N/A[b]	145.7	151.8–153	150.6	144.9	146.3

†SMOA: Switched-mode Operational Amplifier (PWM-based)

[a] Calculated from SNR plot

$$\text{FoM} = \frac{Power/_N}{f_{BW}\left(\frac{IIP_3}{P_N}\right)^{2/3}} \text{ [j/pole]}$$

[b] Two-tone test frequencies not reported

$$\text{FoM}_1 = 10 \cdot \log_{10}\left(\frac{1}{\text{FoM}}\right) \text{ [dB(j}^{-1}\text{)] [78]}$$

[c] Calculated from reported FoM

$$\text{FoM}_2 = 10 \cdot \log_{10}\left(\frac{1}{\text{FoM}} \cdot \frac{f_{IM3,Low}}{f_{BW}}\right) \text{ [dB(j}^{-1}\text{)] [76, 77]}$$

2.7 Conclusions

This section has introduced a highly linear process-resilient RO-based filter. A linearized CCO (linCCO) has been proposed that mimics the operation of the active-RC filter topology in the phase-domain to achieve state-of-the-art linearity. Furthermore, a zero compensation technique has been presented to extend the achievable bandwidth of the proposed topology. Also, a DLL-based frequency tuning scheme was introduced to achieve PVT resilience for the proposed linCCO-based filter topology. As a proof of concept, we demonstrated and verified a continuous-time fifth-order filter prototype with a cut-off frequency that is tunable from 1.5 MHz to 22 MHz and achieves state-of-the-art linearity at 1 V. The proposed filter was implemented in a 130 nm CMOS technology. It consumes 6.2–8.9 mW and achieves a 26.2 dB in-band IIP3. Thanks to the DLL-based tuning scheme, the filter achieves a bandwidth variation of less than $\pm 3.5\%$ over a temperature range of -40 °C to 85 °C and a supply voltage range of 0.9 to 1.2V.

3. A HARMONIC-CANCELING SYNTHESIZER USING SKEW-CIRCULANT-MATRIX-BASED COEFFICIENT GENERATOR [1]

3.1 Introduction

Testing procedures are a vital part of the product fabrication cycle and sometimes consume as much as 55% of the total production cost [17]. In this context, built-in self-test (BIST) solutions have been proposed as an appealing approach to reduce the testing cost. The concept is to embed self-testing capabilities to the device under test (DUT), such as stimulus generation and response analysis. Particularly, several highly linear tone generators have been proposed [18–31].

One of the first attempts to synthesize a low-distortion stimulus signal was by means of the band-pass-filter-based oscillator [18–20]. The main drawbacks of this approach are the trade-off between total harmonic distortion (THD) and limiter block circuit complexity along with high power consumption dominated by the filter and limited tuning frequency range. Other solutions are based on direct digital frequency synthesizer (DDFS) [21–24]. Typically, these systems use a phase accumulator, a phase-to-amplitude mapping (P2AM) block, and a digital-to-analog converter (DAC). The main drawback of DDFS is the high power consumption mainly due to the complex and power-hungry P2AM block because it is usually based on a read-only memory (ROM). On the other hand, harmonic-canceling (HC) synthesizers are presented as low-cost, highly-linear tone generators [25–31]. This technique is based on the summation of phase-shifted square-waves, which are weighted with irrational coefficients. It requires a phase generator, a coefficient generator (CG) and a combiner. Previous works on HC synthesizers have implemented such irrational coefficients based on

[1] Parts of this section is reprinted with permission from G. G. Garayar-Leyva, H. Osman, J. J. Estrada-López and E. Sánchez-Sinencio, "A Harmonic-Canceling Synthesizer Using Skew-Circulant-Matrix-Based Coefficient Generator," in 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 2020, pp. 1-5. ©2020 IEEE.

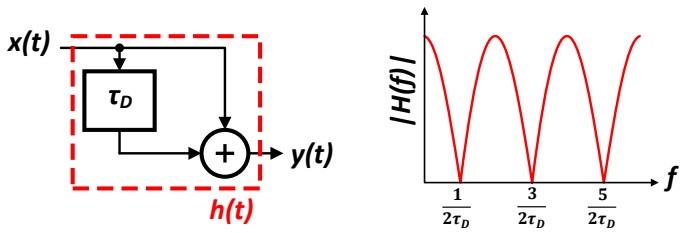
ratios of integer numbers [26–31] and their linearity is mainly limited by mismatch and process variations, requiring calibration schemes that add to the design cost and complexity.

This work presents an HC synthesizer with a skew-circulant-matrix-based CG that implements the required irrational tap coefficients by using integer numbers in a recursive approach without the need for calibration. This CG relaxes the trade-off between output linearity and coefficient mismatch.

This section is organized as follows: Section 3.2 reviews existing harmonic canceling techniques and outlines the limitations of these techniques as they either require impractically small time-step resolution or irrational coefficients. In this respect, this work proposes the skew-circulant-matrix (SCM) based integer-coefficient HC filter in Section 3.3. Section 3.4 discusses an optimized implementation of the SCM-based coefficient generator. The implementation of a prototype synthesizer using the proposed technique is illustrated in Section 3.5. The measurement results of the prototype synthesizer are presented in Section 3.6, followed by conclusions in Section 3.7.

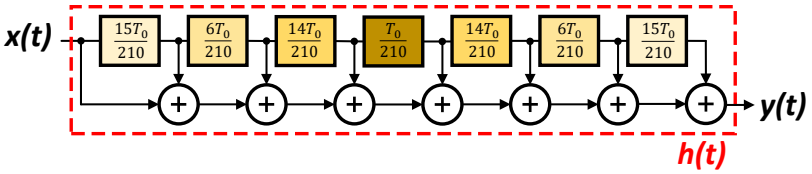
3.2 FIR-based Harmonic Canceling Techniques

3.2.1 Constant-Amplitude Harmonic Canceling FIR Filter

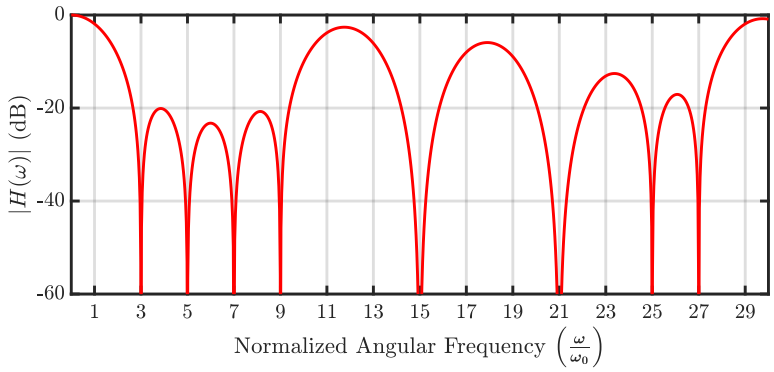


(a) (b)

Figure 3.1: Basic concept of time-mode harmonic-canceling filter: (a) block diagram and (b) transfer function.



(a)



(b)

Figure 3.2: Constant-amplitude (time-mode) harmonic canceling filter that cancels the 3rd, 5th and 7th harmonics and all their odd multiples: (a) block diagram and (b) transfer function.

The key idea behind this technique is to use a finite impulse response (FIR) harmonic canceling filter with equal gain coefficients. This technique is also referred to as time-mode harmonic canceling technique [25] because its only degree of freedom is to add square-wave signals of the same frequency and amplitude, but with different time shifts. The basic concept can be illustrated, as shown in Fig. 3.1 for two square waves that are spaced by a time delay, τ_D. The output is a three-level rectangular waveform, that is the input square wave, $x(t)$, filtered by an FIR filter whose transfer function is expressed as:

$$|H(f)| = 2\left|\cos\left(\pi f \tau_D\right)\right|, \tag{3.1}$$

where f is the frequency in Hz. The filter's transfer function has nulls at odd multiples of $\frac{1}{2\tau_D}$. Hence the time delay can be adjusted to suppress a specific harmonic and all its

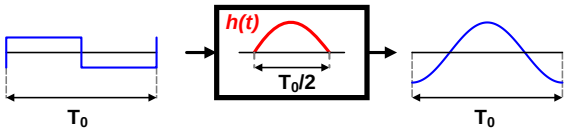
odd multiples. For example, by using $\tau_D = {}^{T_0}/_{2k}$, the k-th harmonic of the output signal is completely suppressed. The complete cancellation of multiple harmonics is feasible by synthesizing an FIR filter that has a transfer function equals to the product of different instances of the transfer function, which is described in (3.1). For instance, to suppress the 3rd, 5th and 7th harmonics, and all their odd multiples, the following harmonic-canceling filter can be used:

$$\begin{aligned} |H(f)| &= \left| \prod_{k=3,5,7} \cos\left(\pi f \frac{T_0}{2k}\right) \right| \\ &= \frac{1}{4} \left| \cos\left(\pi f \frac{T_0}{210}\right) + \cos\left(\pi f \frac{29T_0}{210}\right) + \cos\left(\pi f \frac{41T_0}{210}\right) + \cos\left(\pi f \frac{71T_0}{210}\right) \right|, \end{aligned} \quad (3.2)$$

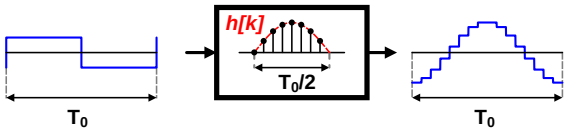
where T_0 is the period of the input square wave. Fig. 3.2 shows a block diagram of this time-mode harmonic canceling filter along with its transfer function, which shows the cancellation of the targeted harmonics. It is worth noting that a small time-step resolution ($\frac{T_0}{210}$) is needed to suppress the 3rd, 5th and 7th harmonics. To suppress more harmonics, the time-step resolution can be impractically small, which limits the efficacy of this technique. The authors in [25] proposed a solution that combines the time-mode harmonic-canceling FIR filter with a third-order passive filter to achieve a total harmonic distortion of less than -70 dB. They also proposed a heuristic algorithm to optimize the time-step resolution, number of square-wave phases, and time shifts such that the time-mode harmonic-canceling FIR, along with the passive filter, provides the lowest THD [25].

3.2.2 Sampled Half-sine Harmonic Canceling FIR Filter

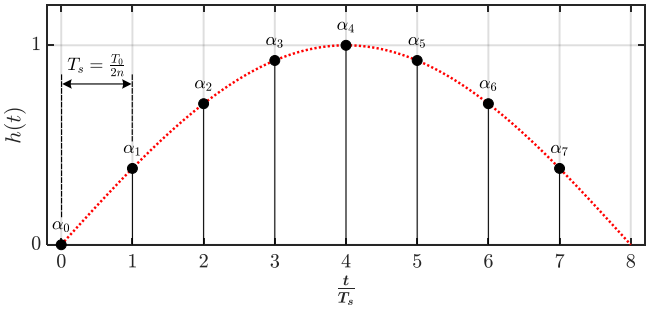
The concept of harmonic cancellation using a sampled half-sine filter was first introduced in [79] for low-frequency sine wave generation, and then it was revived in recent publications [28, 29]. The basic concept can be illustrated as shown in Fig. 3.3a where a symmetric square wave of period T_0 is applied to a filter that has an impulse response of a half-sine.



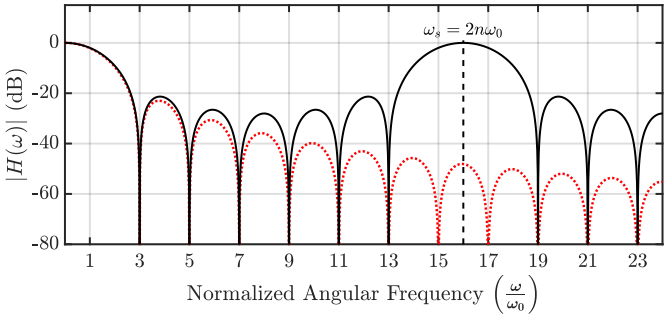
(a)



(b)



(c)



(d)

Figure 3.3: Half-sine harmonic canceling FIR filter: (a) continuous-time filter, (b) discrete-time (sampled) implementation, (c) impulse response of the continuous-time (dashed red) and the sampled 8-tap HC filters (solid black), and (d) frequency response of the continuous-time (dashed red) and the sampled 8-tap HC filters (solid black).

The transfer function of the continuous-time half-sine (CTHS) filter can be derived using the Fourier transform as [28]:

$$H_{CTHS}(\omega) = \frac{2}{\omega_0} \frac{\cos\left(\frac{\pi}{2}\frac{\omega}{\omega_0}\right)}{1-\left(\frac{\omega}{\omega_0}\right)^2}, \tag{3.3}$$

where $\omega_0 = {}^{2\pi}/_{T_0}$ is the angular frequency of the input square wave. The magnitude response of the CTHS is depicted in Fig. 3.3d, the transfer function has nulls at all harmonic frequencies except the fundamental frequency ($\omega = \omega_0$). Therefore, the output of the CTHS filter is a pure sinusoidal-wave with no spurious harmonics. However, the implementation of the perfect CTHS filter is impractical and, to the best of our knowledge, is not found in the literature.

A practical implementation for the CTHS filter is by using an n-tap FIR filter whose tap coefficients (α_k) are the half-sine impulse response sampled at $T_s = {}^{T_0}/_{2n}$ [28, 29], or

$$\alpha_k = h\,[k] = \sin\left(\frac{k\pi}{n}\right), k = 0, 1, \ldots, n-1, \tag{3.4}$$

A basic block diagram for the n-tap FIR harmonic canceling filter is shown in Fig. 3.3b, where the output is a staircase approximation of a sine-wave. The transfer function of the sampled n-tap FIR filter described by (3.4) can be derived as:

$$|H_{FIR,n}(\omega)| = \frac{\cos\left(\frac{\pi}{2}\frac{\omega}{\omega_0}\right)\sin\left(\frac{\pi}{n}\right)}{\cos\left(\frac{\pi}{n}\frac{\omega}{\omega_0}\right)-\cos\left(\frac{\pi}{n}\right)}, \tag{3.5}$$

The magnitude response of the n-tap FIR filter is demonstrated in Fig. 3.3d for $n = 8$. Notably, the frequency response of the FIR filter $|H_{FIR,n}(\omega)|$ is periodic with a period of $2n\omega_0$. Therefore, it has nulls at all harmonic frequencies except the fundamental and $2nl \pm 1$ for $l = 1, 2, \ldots, etc.$ The problem of the non-canceled harmonics can be mitigated by increasing the number of FIR taps to push the non-canceled harmonics to very high frequencies where a simple passive filter can provide sufficient attenuation to the non-canceled harmonics. Table 3.1 shows the tap coefficients for several n-tap FIR harmonic canceling filters for

Table 3.1: Tap coefficients for several sampled half-sine n-tap FIR harmonic canceling filters

n	α_0	α_1	α_2	α_3	α_4	α_5	α_6	α_7	1st noncancelable harmonic
4	0	0.7071	1	0.7071					$7\omega_0$
6	0	0.5	0.866	1	0.866	0.5			$11\omega_0$
8	0	0.3827	0.7071	0.9239	1	0.9239	0.7071	0.3827	$15\omega_0$

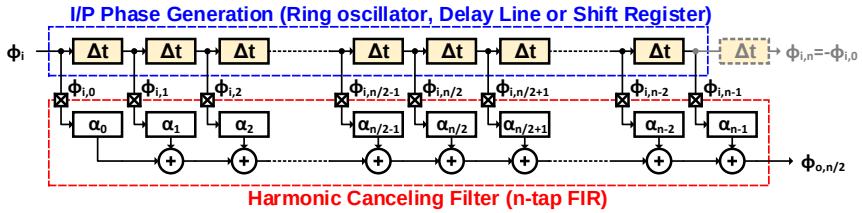
several values of n; only even values of n are presented because they will be the focus of the rest of this section.

Notably, the sampled half-sine FIR filters have more degrees of freedom (time step and tap coefficients) compared to the constant-amplitude harmonic canceling FIR filters. For instance, on the one hand, a constant-amplitude harmonic canceling FIR filter needs a time step of $\frac{T_0}{30}$ to suppress the 3rd and 5th harmonics. A sampled half-sine 4-tap FIR filter, on the other hand, needs a time step of $\frac{T_0}{8}$ and the tap coefficients that are provided in Table 3.1 to cancel the same harmonics. Hence, a sampled half-sine FIR filter can achieve similar harmonic cancelation with a larger time step resolution at the expense of utilizing irrational tap coefficients.

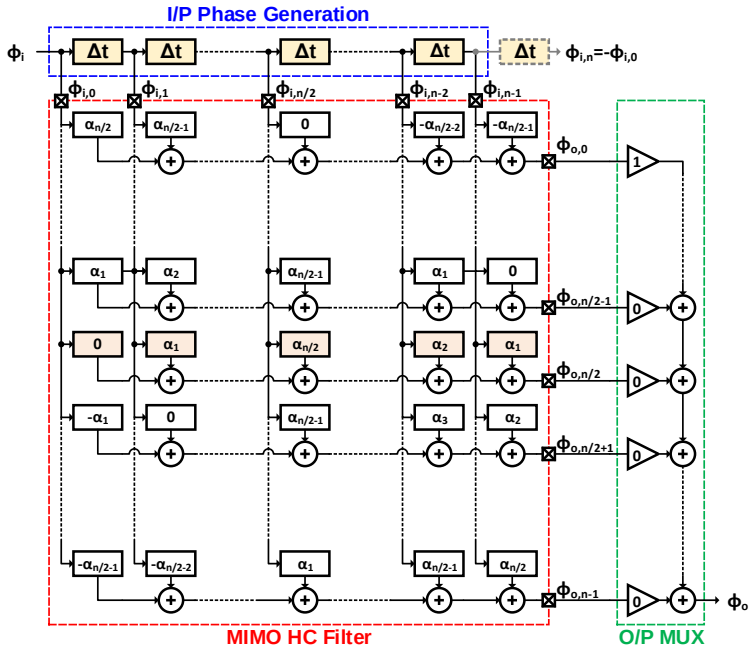
3.3 Proposed Harmonic Canceling Technique

3.3.1 Matrix Representation of the HC Filter

In this section, a systematic and a modular way to implement the sampled half-sine FIR harmonic-canceling filters is presented, which is referred to as a harmonic-canceling filter (HCF). This starts from the block diagram implementation of an HCF like that was presented in [28, 29] as shown in Fig. 3.4a. The input to the n-tap HCF filter is a symmetric square-wave $\phi_i(t)$ that is applied to $(n-1)$ delay elements each having a delay of $T_s = {}^{T_0}/_{2n}$, hence providing the input phases $\phi_{i,k} = \phi_i(t - kT_s)$. The input phases are scaled by the tap coefficients, α_k, that were given by (3.4). For an even n, it is true that $\alpha_0 = 0$, $\alpha_{n/2} = 1$ and $\alpha_k = \alpha_{n-k}$ which means that the HCF is a linear-phase FIR filter. Hence, the HCF provides



(a)



(b)

Figure 3.4: General form of the n-tap harmonic cancelling filter (HCF): (a) HCF block diagram implementation for generating a single output phase, and (b) HCF block diagram for generating multiple output phases .

a constant input-output group delay of $\frac{n}{2}T_s$ [80]. For that reason, the output of the HCF is annotated as $\phi_{o,n/2}$ to indicate the input-output delay of the HCF filter. The input-output relationship of the HCF filter, that is shown in Fig. 3.4a, is given by:

$$\phi_{o,n/2} = \sum_{k=0}^{n-1} \phi_{i,k}\alpha_k \tag{3.6}$$

The block diagram, that is depicted in Fig. 3.4a, can be generalized as illustrated in

Fig. 3.4b, where multiple output phases $\phi_{o,k}$ can be generated from the available input phases $\phi_{i,k}$ for $k = 0, 1, \ldots, n-1$ provided that the inputs are periodic and odd symmetric, i.e. $\phi_{i,k+2n} = \phi_{i,k}$ and $\phi_{i,k+n} = -\phi_{i,k}$. The multiple-input and multiple-output (MIMO) HCF shown in Fig. 3.4b is useful because of its ability to generate all the output phases. Hence, it allows cascading multiple imperfect HCFs to improve the total harmonic rejection, as further illustrated. The HCF shown in Fig. 3.4b can be represented by the following matrix equation:

$$\boldsymbol{\Phi_o} = \boldsymbol{A_i}\boldsymbol{\Phi_i} \tag{3.7}$$

where $\boldsymbol{\Phi_i} = (\phi_{i,0}, \phi_{i,1}, \cdots, \phi_{i,n-1})^T$ is the input phases vector, $\boldsymbol{\Phi_o} = (\phi_{o,0}, \phi_{o,1}, \cdots, \phi_{o,n-1})^T$ is the output phases vector, and A_i is the coefficients matrix which is given by (3.8). It is worth noting that A_i is a symmetric skew-circulant matrix (SCM) where every row is the right cyclic shift of the row above it, and the change of sign in the sub-diagonal entries [81].

$$\boldsymbol{A_i} = \begin{bmatrix} 1 & \alpha_{n/2-1} & \cdots & 0 & \cdots & -\alpha_{n/2-2} & -\alpha_{n/2-1} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \alpha_1 & \alpha_2 & \cdots & \alpha_{n/2-1} & \cdots & \alpha_1 & 0 \\ 0 & \alpha_1 & \cdots & 1 & \cdots & \alpha_2 & \alpha_1 \\ -\alpha_1 & 0 & \cdots & \alpha_{n/2-1} & \cdots & \alpha_3 & \alpha_2 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ -\alpha_{n/2-1} & -\alpha_{n/2-2} & \cdots & \alpha_1 & \cdots & \alpha_{n/2-1} & 1 \end{bmatrix} \tag{3.8}$$

A skew-circulant matrix can be completely defined by the elements of its first row, hence we will use the notation $\boldsymbol{A_i} = \mathrm{scirc}\left(1, \alpha_{\mathrm{n}/2-1}, \cdots, 0, \cdots, -\alpha_{\mathrm{n}/2-2}, -\alpha_{\mathrm{n}/2-1}\right)$ to represent the ideal irrational coefficients matrix.

It is worth noting that because of the symmetry of A_i, the MIMO HCF illustrated in Fig. 3.4b can be rearranged as shown in Fig. 3.5. The rearranged implementation shown in Fig. 3.5 is composed of an FIR coefficient generator that carries only dc signals, and an

output combiner that combines the input phases scaled by the corresponding coefficients. This implementation is favored over the straightforward implementation shown in Fig. 3.4b because the input phases have faster paths to the output. Thus, the system will introduce less phase variations resulting in a better harmonic rejection performance [30].

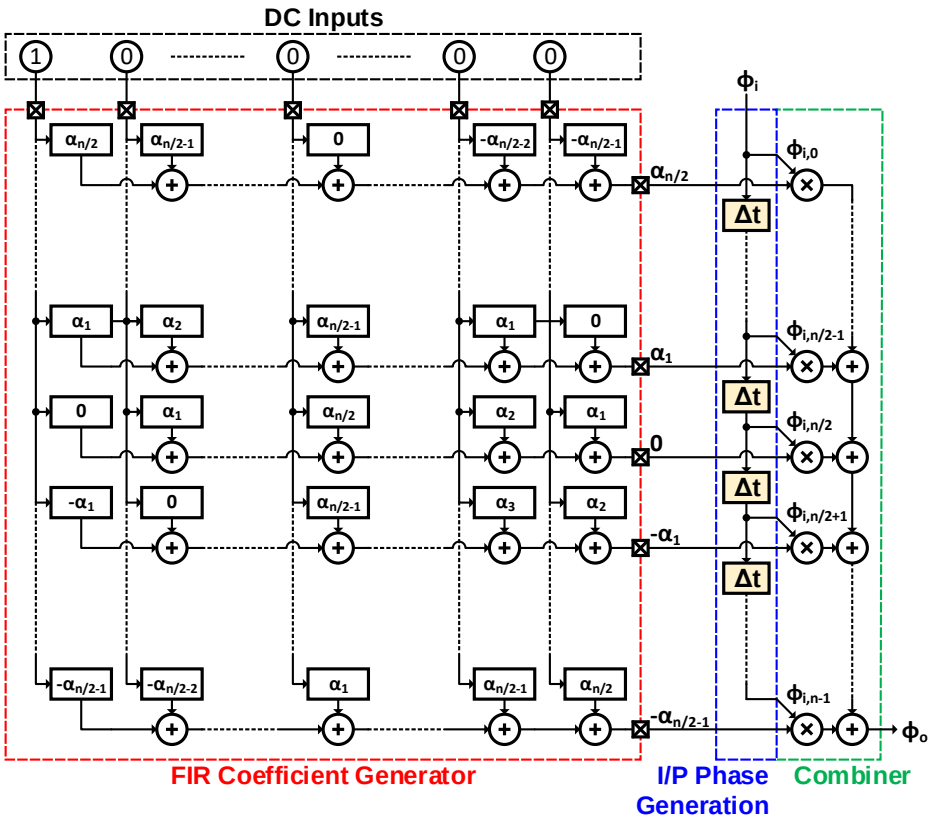


Figure 3.5: Proposed n-tap HC filter implementation using an FIR coefficient generator and an output phase combiner.

3.3.2 Properties of the Skew-Circulant Matrices

A skew-circulant matrix (SCM) $\boldsymbol{S_n} = \mathrm{scirc}(s_o, s_1, \ldots, s_{n-1})$ of order n has eigenvectors that are defined as

$$y_m = \begin{pmatrix} 1 & , e^{\frac{j\pi(1+2m)}{n}} & , \dots & , e^{\frac{j\pi(1+2m)(n-1)}{n}} \end{pmatrix}^T, m = 0, 1, \dots, n-1 \tag{3.9}$$

where j is the unitary imaginary number and the T is the matrix transpose. It is worth noting that the eigenvectors are independent on the elements of the SCM, hence they are similar for all SCMs with the same order n. The corresponding eigenvalues of $\boldsymbol{S_n}$ are given by [81]:

$$\lambda_m = \sum_{k=0}^{n-1} s_k e^{\frac{j\pi(1+2m)}{n}}, m = 0, 1, \dots, n-1 \tag{3.10}$$

Matrix $\boldsymbol{S_n}$ can be expressed by its eigen decomposition $\boldsymbol{S_n} = \boldsymbol{U\Lambda U^*}$, where matrix $\boldsymbol{U} = [y_0|y_1|\cdots|y_{n-1}]$, $\boldsymbol{\Lambda} = diag(\lambda_0, \lambda_1, ..., \lambda_{n-1})$ and $\boldsymbol{U^*}$ is the conjugate transpose of $\boldsymbol{U}$. From (3.9), all SCMs of the same order n share the same eigenvectors; hence, the same matrix $\boldsymbol{U}$.

3.3.3 Proposed Skew-Circulant-Matrix based, Integer-Coefficient HC Filter

Note that from (3.8), $\boldsymbol{A_i} = \text{scirc}(s_0, s_1, \dots, s_{n-1})$, where $s_k = \cos(k\pi/n)$. Consider a system defined by a normalized, even-order, SCM $[\boldsymbol{A_i}]$, with inputs $\phi_{i,k}$ and outputs $\phi_{o,k}$, for $k = 0, 1, \dots, n-1$. Its eigen decomposition is given by

$$[\boldsymbol{A_i}] = \frac{\boldsymbol{A_i}}{\|A_i\|} = \boldsymbol{U\Lambda_i U^*} \tag{3.11}$$

where $\|A_i\|$ is the Euclidean norm of $\boldsymbol{A_i}$ and, from (3.10), $\boldsymbol{\Lambda_i} = diag(1, 0, \dots, 0, 1)$ (see Appendix B.1). Let $\boldsymbol{A} = \text{scirc}(s'_0, s'_1, \dots, s'_{n-1})$ be an even-order SCM such that $s'_k = \text{sgn}(s_k)$, where $\text{sgn}(\cdot)$ is the sign function, i.e. it is an integer-coefficient SCM. It is derived in Appendix B.2 that the eigenvalues of $\boldsymbol{A}$ are given by

$$\lambda'_m = (-1)^m \cot\left(\frac{\pi(1+2m)}{2n}\right), m = 0, 1, \dots, n-1 \tag{3.12}$$

Let $[\boldsymbol{A}]$ be the normalized version of $\boldsymbol{A}$ such that $[\boldsymbol{A}] = \boldsymbol{A}/\|A\| = \boldsymbol{U}\boldsymbol{\Lambda}\boldsymbol{U}^*$, where $\boldsymbol{\Lambda} = diag(1, \epsilon_1, \ldots, \epsilon_{n-2}, 1)$ and $\epsilon_m = \lambda'_m / \max(|\lambda'_m|) < 1$. Fig. 3.6 presents the eigenvalues of some normalized, integer-coefficient SCMs.

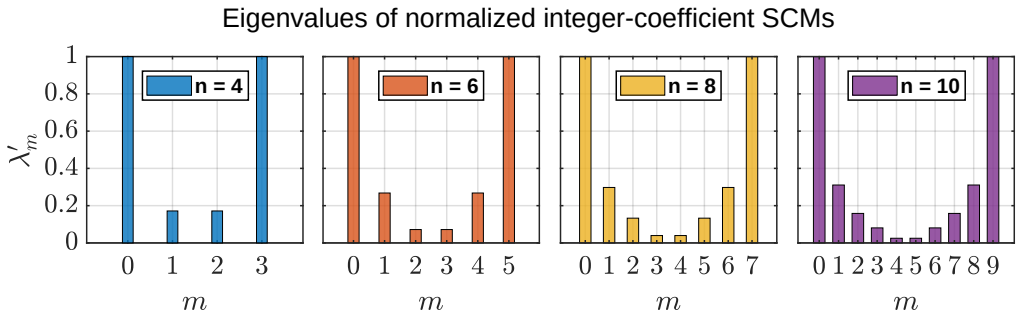


Figure 3.6: Eigenvalues of some normalized integer-coefficient SCMs of even order n.

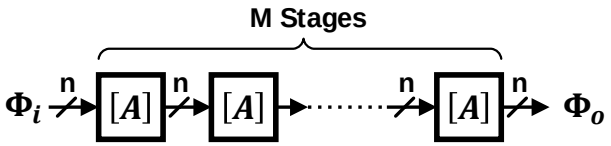
As previously stated, SCMs of the same order n share the same eigenvectors. Based on this property, if M replicas of $[\boldsymbol{A}]$ are cascaded, then

$$[\boldsymbol{A}]^M = \left(\frac{\boldsymbol{A}}{\|A\|}\right)^M = \boldsymbol{U}\boldsymbol{\Lambda}^M\boldsymbol{U}^* \tag{3.13}$$

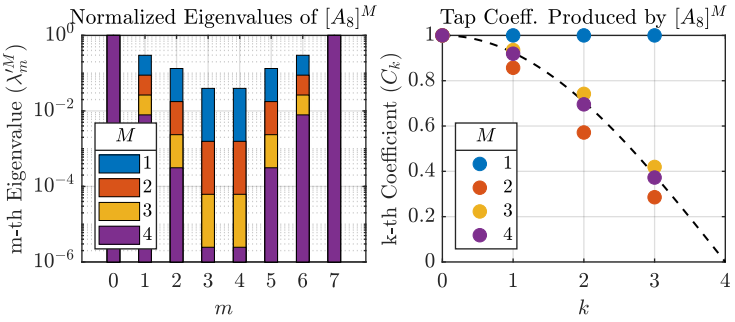
where $\boldsymbol{\Lambda}^M = \text{diag}(1, \epsilon_1^M, \ldots, \epsilon_{n-2}^M, 1)$. Then

$$\lim_{M\to\infty} [\boldsymbol{A}]^M = \boldsymbol{U}\boldsymbol{\Lambda}_{\boldsymbol{i}}\boldsymbol{U}^* = [\boldsymbol{A}_{\boldsymbol{i}}] \tag{3.14}$$

This result implies that an ideal n-tap HCF with the irrational coefficients, that were described in (3.4), can be implemented with a cascade of M normalized, even-order, integer-coefficient SCMs as shown in Fig. 3.7.



(a)



(b)

Figure 3.7: Proposed skew-circulant-matrix based, integer-coefficient HC filter: (a) block diagram using cascade of M identical stages of integer-coefficient SCM $[A]$, and (b) normalized eigenvalues and tap coefficients of $[A]^M$ showing its convergence to the ideal $[A_i]$ for greater M.

3.3.4 Cascade of Different Order HC Filters

The cascade of more than one HC filter of different order, n, enables the cancellation of more harmonics than only one HC filter can do. A system with a cascade of two 4-tap and 6-tap FIR harmonic canceling filters was presented in [30] to cancel square-wave harmonics up to the 21st. This section presents a generalized form for cascading arbitrary HC filters and derives the conditions required to cancel as many harmonics as possible. Without loss of generality, we assume two HC filters with sizes n_1 and n_2 , namely HC_{n_1} and HC_{n_2}, are cascaded. From section 3.3.1, HC_{n_1} and HC_{n_2} requires clock phases that are equally spaced by π/n_1 and π/n_2, respectively. To provide the clock phases required by the two HC filters, a clock generator with a π/n phase granularity is needed, where n is the least common multiple of n_1 and n_2, or

$$n = \mathrm{lcm}\,(n_1, n_2) = \frac{n_1 n_2}{\gcd\,(n_1, n_2)}, \tag{3.15}$$

where $\mathrm{lcm}\,(\cdot)$ and $\gcd\,(\cdot)$ are the least common multiple and the greatest common divisor operators, respectively. The first HC stage (HC_{n_1}) works on n_1 input phases equally separated by π/n_1 . Therefore, n/n_1 parallel filters are needed for proper harmonic cancellation for the n input phases. A perfect shuffle permutation $P_{n_1}^{n/n_1}$ is needed at the input of this stage to reorder input phases such that each HC_{n_1} filter gets n_1 equally-separated phases. The perfect shuffle permutation $P_{n_1}^{n/n_1}$ is done simply by grouping the n inputs into n_1 groups each of size n/n_1, and then the vector is reordered by taking one element of each group in turn until the whole vector is reassembled [82]. Another perfect shuffle $P_{n/n_1}^{n_1}$ is needed at the output to rearrange output phases back to their original order. A similar arrangement is made for the second stage (HC_{n_2}) where n/n_2 parallel filters are needed for proper harmonic cancellation of the n phases along with the input and output perfect shuffle matrices. The aforementioned configuration is illustrated in Fig. 3.8 for $n_1 = 4$ and $n_2 = 6$.

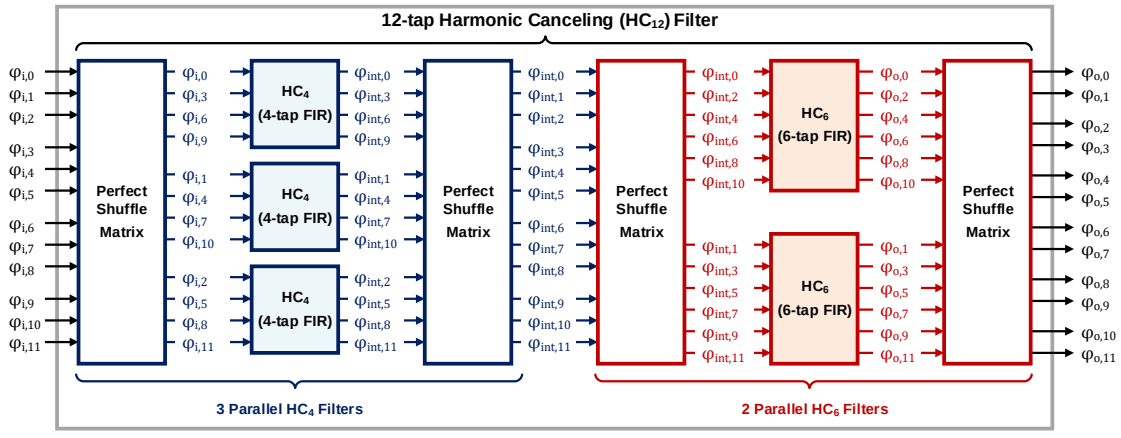


Figure 3.8: Cascade of HC_4 and HC_6 filters forming an effective 12-tap harmonic cancelling (HC_{12}) filter.

This system can be described mathematically as:

$$\begin{aligned} \boldsymbol{\Phi_o} &= \boldsymbol{P_{n/n_2}^{n_2}} \left(\boldsymbol{I_{n/n_2}} \otimes \boldsymbol{A_{n_2 \times n_2}} \right) \boldsymbol{P_{n_2}^{n/n_2}} \boldsymbol{\Phi_{o1}} \\ \boldsymbol{\Phi_{o_1}} &= \boldsymbol{P_{n/n_1}^{n_1}} \left(\boldsymbol{I_{n/n_1}} \otimes \boldsymbol{A_{n_1 \times n_1}} \right) \boldsymbol{P_{n_1}^{n/n_1}} \boldsymbol{\Phi_i} \end{aligned}, \tag{3.16}$$

where $\otimes$ is the Kronecker product operator, and for $n = s \times r$, the perfect shuffle matrix P_r^s is constructed by taking slices of the $n \times n$ identity matrix I_n as:

$$\boldsymbol{P_r^s} = \begin{bmatrix} I_n\left(1:s:n,:\right) \\ I_n\left(2:s:n,:\right) \\ \vdots \\ I_n\left(s:s:n,:\right) \end{bmatrix} \tag{3.17}$$

where the well-known colon notation used in MATLAB to designate submatrices is used here [83]. Recall the definition of the Kronecker product of two matrices $X = (x_{ij})_{i=1,\ldots,m;j=1,\ldots,n} \in M_{m\times n}(\mathbb{R})$ and $Y = (y_{hk})_{h=1,\ldots,p;k=1,\ldots,q} \in M_{p\times q}(\mathbb{R})$ to be the $mp \times nq$ matrix [82]:

$$\boldsymbol{X} \otimes \boldsymbol{Y} = \begin{bmatrix} x_{11}\boldsymbol{Y} & \cdots & x_{1n}\boldsymbol{Y} \\ \vdots & \ddots & \vdots \\ x_{m1}\boldsymbol{Y} & \cdots & x_{mn}\boldsymbol{Y} \end{bmatrix} \tag{3.18}$$

By using properties of Kronecker product [82], (3.16) can be simplified to:

$$\boldsymbol{\Phi_o} = \left(\boldsymbol{A_{n_2 \times n_2}} \otimes \boldsymbol{I_{n/n_2}} \right) \left(\boldsymbol{A_{n_1 \times n_1}} \otimes \boldsymbol{I_{n/n_1}} \right) \boldsymbol{\Phi_i} \tag{3.19}$$

To visualize the result obtained from (3.19), it follows that for the cascaded system shown in Fig. 3.8 if ideal HC filters are used, the resulting Kronecker products of (3.19) are given by:

$$\begin{aligned} \boldsymbol{A_{6\times 6}} \otimes \boldsymbol{I_2} &= \text{scirc}\left(1, 0, \frac{\sqrt{3}}{2}, 0, \frac{1}{2}, 0, 0, 0, -\frac{1}{2}, 0, -\frac{\sqrt{3}}{2}, 0\right) \\ \boldsymbol{A_{4\times 4}} \otimes \boldsymbol{I_3} &= \text{scirc}\left(1, 0, 0, \frac{1}{\sqrt{2}}, 0, 0, 0, 0, 0, -\frac{1}{\sqrt{2}}, 0, 0\right) \end{aligned} \tag{3.20}$$

It is derived in Appendix B.3 that the matrix product $\left(\boldsymbol{A_{n_2\times n_2}} \otimes \boldsymbol{I_{n/n_2}}\right)\left(\boldsymbol{A_{n_1\times n_1}} \otimes \boldsymbol{I_{n/n_1}}\right)$ is simply a scaled version of $A_{n\times n}$ if and only if $\gcd(n_1, n_2) > 1$, or

$$\boldsymbol{A_{n\times n}} = \frac{2}{\gcd\left(n_1, n_2\right)}\left(\boldsymbol{A_{n_2\times n_2}} \otimes \boldsymbol{I_{n/n_2}}\right)\left(\boldsymbol{A_{n_1\times n_1}} \otimes \boldsymbol{I_{n/n_1}}\right), \tag{3.21}$$

Hence, a cascade of two HC filters, HC_{n1} and HC_{n2}, is equivalent to an HC filter of size $n = \text{lcm}\left(n_1, n_2\right)$ if and only if n_1 and n_2 have a common factor, i.e., $\gcd\left(n_1, n_2\right) > 1$. It is intuitive to choose $\gcd\left(n_1, n_2\right) = 2$ to maximize the order of the resulting HC filter. This property can be utilized to decompose any HC filters into a cascade of smaller HC filters, which eases the system implementation. The same criteria can be applied recursively to more than two cascaded stages. For example, a 60-tap HC filter that can cancel up to the 117$^{\text{th}}$ harmonic can be decomposed into a cascade of 4-tap, 6-tap, and 10-tap HC filters.

3.3.5 Bandpass HC Filter

In the harmonic cancelling filter system described in section 3.3.3, the input fundamental frequency is of interest. However, it is relevant to point out that higher-order harmonics can be selected, i.e., a bandpass HC filter can be implemented. The impulse response of the HC filter used to select the m-th harmonic $h_m(t)$ can be generalized as follows:

$$h_m\left(t\right) = \sin\left(\frac{2\pi m}{T}t\right), \tag{3.22}$$

where m is the main harmonic of interest. Fig. 3.9 shows various harmonic-canceling filters selecting either the fundamental, 3$^{\text{rd}}$ or 5$^{\text{th}}$ harmonics. It follows that, to obtain the FIR tap-coefficients, we sample $h_m(t)$ with sample intervals equal to $T_s = {}^{T_0}/_{2n}$, considering $n > m$

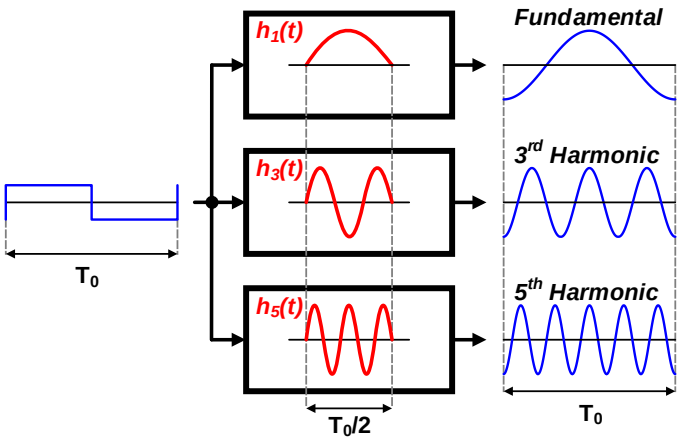


Figure 3.9: The impulse response of various harmonic-canceling filters selecting different harmonics.

to satisfy the Nyquist sampling theorem.

It is worth noting that the sampled impulse response, $h_m[k] = \sin(mk\pi/n)$, is symmetric around the center, i.e., at $k = n/2$. Moreover, the sampled values $h_m[0], h_m[1], \ldots, h_m[n/2-1]$ are all different if m and $2n$ are relatively prime, i.e., their greatest common divisor is 1 [84].

Following the case for $n = 8$, we want to extract the fundamental, 3rd and the 5th harmonic. From (3.22), $h_1[k] = sin(\pi k/8)$, $h_3[k] = sin(3\pi k/8)$ and $h_5[k] = sin(5\pi k/8)$ where $k = 1, 2, \ldots, 7$. Fig. 3.10 shows the sampled impulse response of $h_1[k]$, $h_3[k]$ and $h_5[k]$. Notably, the tap coefficients absolute values are similar, but they have a different order and sign. Hence, assuming the tap coefficients are available, it is possible to implement different filters, each of them enhancing different harmonics just by rearranging the order and signs of the tap coefficients.

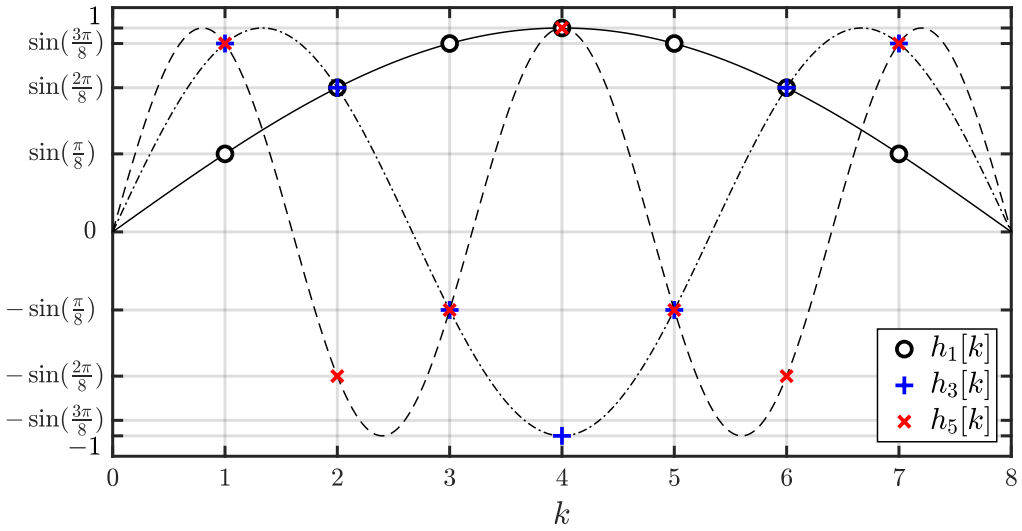
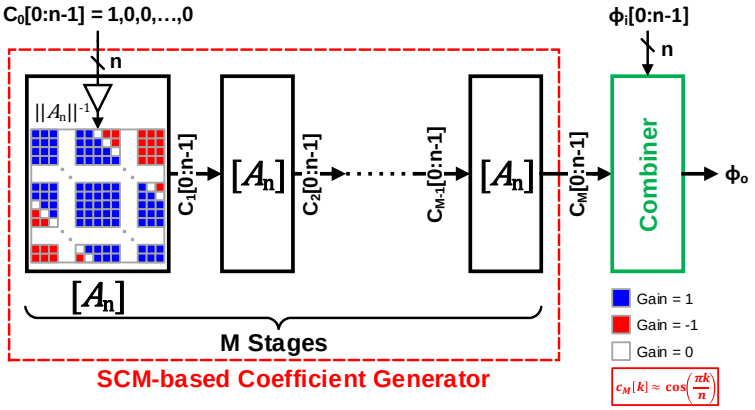


Figure 3.10: Impulse responses of an 8-tap lowpass harmonic-canceling filter ($h_1[k]$) and 8-tap bandpass harmonic-canceling filters ($h_3[k]$ and $h_5[k]$).

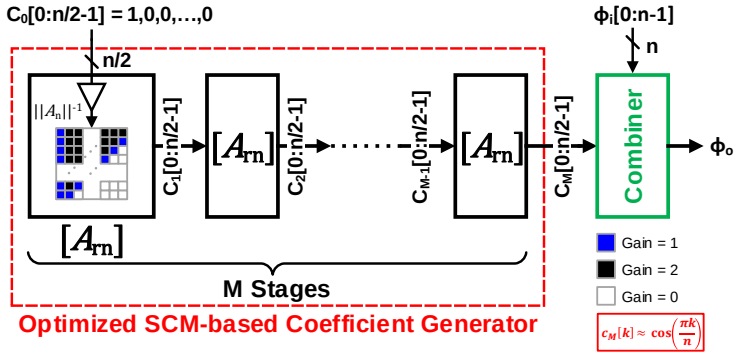
3.4 Skew-Circulant-Matrix based Coefficient Generator

3.4.1 Multistage Open-Loop Coefficient Generator

In this section, the system-level implementation of the coefficient generator (CG), that is shown in Fig. 3.5, is illustrated using the proposed skew-circulant-matrix (SCM) based approach. Fig. 3.11a shows the straightforward implementation of the CG for an n-tap HC filter using a cascade of M identical integer-coefficient SCMs, $[\boldsymbol{A_n}]^M$. According to (3.14), $[\boldsymbol{A_n}]^M$ will converge to the ideal $[\boldsymbol{A_{n,i}}]$ for large M. Therefore, for $C_0\,[0:n-1] = (1, 0, \cdots, 0)$, the output of the M-th stage is the first column of the ideal $[\boldsymbol{A_{n,i}}]$, i.e., $C_M\,[k] \propto \cos(k\pi/n)$ for $k = 0, 1, \cdots, n-1$. The quarter-wave symmetry of the cosine function can be utilized to reduce the implementation complexity of the coefficient generator as shown in Fig. 3.11b, where only the first $n/2$ coefficients are calculated as they represent a full quadrant of the cosine function. Therefore, the $n \times n$ integer-coefficient SCM, $[\boldsymbol{A_n}]$, can be reduced to an $n/2 \times n/2$ matrix, $[\boldsymbol{A_{rn}}]$ where:



(a)



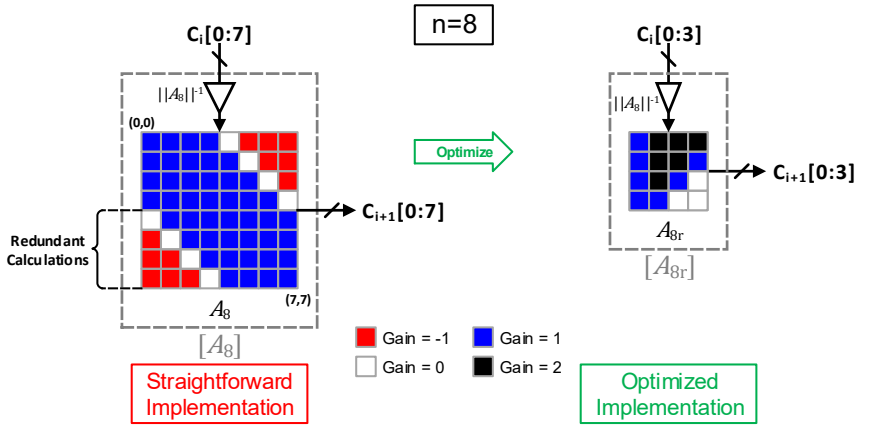
(b)

Figure 3.11: System level implementation of the coefficient generator of an n-tap HC FIR filter: (a) straightforward implementation, and (b) reduced implementation.

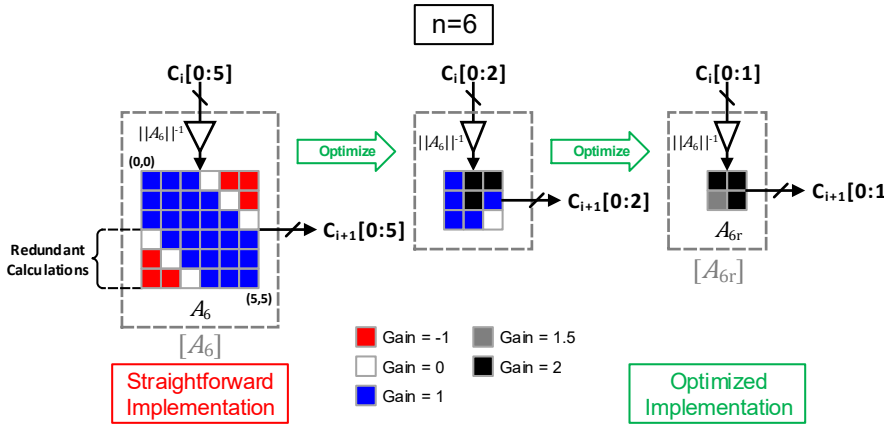
$$[\boldsymbol{A_{rn}}] = \|A_n\|^{-1} \begin{bmatrix} 1 & 2 & 2 & \cdots & 2 & 2 \\ 1 & 2 & 2 & \cdots & 2 & 1 \\ \vdots & \vdots & \ddots & \ddots & \ddots & 0 \\ 1 & 2 & 2 & 1 & \ddots & \vdots \\ 1 & 2 & 1 & 0 & \cdots & 0 \\ 1 & 1 & 0 & 0 & \cdots & 0 \end{bmatrix} \tag{3.23}$$

Fig. 3.12 shows examples of the reduced implementation for $n = 8$ and $n = 6$. For the case $n = 8$, the quadrant symmetry is exploited to obtain $[\boldsymbol{A_{r8}}]$ as shown in Fig. 3.12a.

For the case $n = 6$, $[\boldsymbol{A_{rn}}]$ can be further optimized by noting that ideally $C_i\,[2] = {}^{C_i[0]}/_{2}$; therefore, only the first two coefficients are calculated, as shown in Fig. 3.12b, and the third coefficient is simply half of the first coefficient.



(a)



(b)

Figure 3.12: System level implementation of the coefficient generator: (a) 8-tap FIR coefficient generator, and (b) 6-tap FIR coefficient generator.

3.4.2 Closed-loop Coefficient Generator

First, consider the outputs of each stage of an M-stage open loop SCM-based coefficient generator, that is shown in Fig. 3.11b. It is noted that the output coefficients of each stage

asymptotically approaches the ideal tap coefficients as they progress through the chain of the cascaded open-loop stages. Therefore, the inputs and outputs of the last stage are exactly the same, as M approaches infinity. This can be implemented at a low complexity by using the closed-loop coefficient generator shown in Fig. 3.13, where the output of a single stage is fed-back and applied to its input. At steady-state the inputs and outputs of $[\boldsymbol{A_{rn}}]$ are exactly the same and equals the ideal tap coefficients, or $C_{CL}\,[k] = \cos(k\pi/n)$ for $k = 0, 1, \cdots, {}^{n}/_{2}-1$. It should be noted that this intuition is correct if the normalizing gain equals

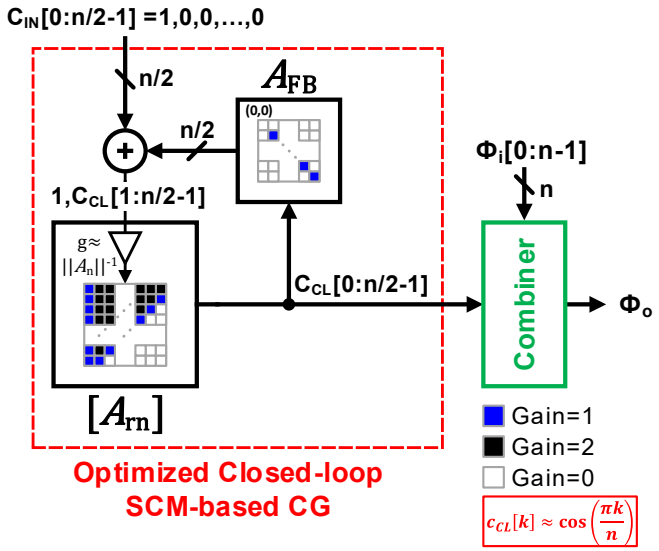


Figure 3.13: Block diagram of the closed-loop skew-circulant-matrix based coefficient generator for an n-tap HC filter.

its ideal value, i.e., $g_n = \|A_n\|^{-1} = \tan\left(\frac{\pi}{2n}\right)$. For ease of implementation, the normalizing gain is approximated to a rational number, e.g., $g_n = \frac{8}{5n} \approx \|A_n\|^{-1}$, that affects the accuracy of the generated coefficients. The output of the closed-loop coefficient generator is expressed as:

$$\boldsymbol{C_{CL}} = (\boldsymbol{I} - [\boldsymbol{A_{rn}}]\,\boldsymbol{A_{FB}})^{-1}\,[\boldsymbol{A_{rn}}]\,\boldsymbol{C_{IN}}, \tag{3.24}$$

where $[\boldsymbol{A_{FB}}] = \text{diag}\,(0, 1, 1, \cdots, 1)$, $\boldsymbol{C_{IN}} = (1, 0, \cdots, 0)^T$. To validate the proposed concept, system-level simulations for various n-tap HC filters employing several M-stage open-loop coefficient generators and the proposed closed-loop coefficient generator are shown in Fig. 3.14. The total harmonic distortion (THD) is calculated by taking into account all harmonics up to the Nyquist frequency, i.e., nf_0 where f_0 is the frequency of the output sinusoid. Following the case of $n = 8$, it is noted from Fig. 3.14 that each open-loop CG stage results in a 10dB improvement in the output THD, whereas a closed-loop CG with $g_n = \frac{8}{5n}$ is capable of producing a sinuosoid with a THD of $-66dB$. The closed-loop coefficient generator is capable of achieving the same THD as a 5-stage open-loop CG, as depicted in Fig. 3.14, for $n > 6$; therefore, replacing the first stage of an M-stage open-loop CG with a closed-loop CG results in a lower implementation complexity. For example, a 7-stage open-loop CG, or a cascade of a closed-loop CG followed by a 2-stage open-loop CG are needed to obtain a THD better than $-80dB$.

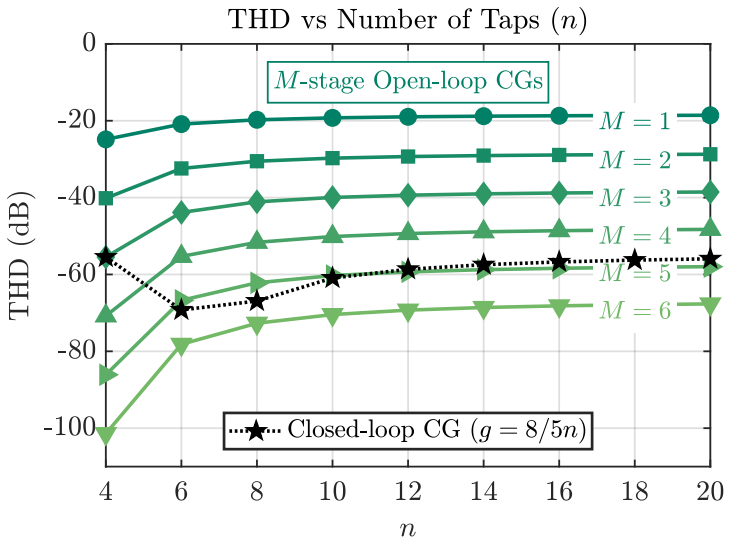


Figure 3.14: Simulated THD versus number of taps for various n-tap HC filters employing several M-stage open-loop coefficient generators (solid lines), and the closed-loop coefficient generator (dotted line).

3.5 Circuit Implementation of the Synthesizer Prototype

This section presents the circuit-level implementation of a reconfigurable n-th order harmonic canceling synthesizer prototype that employs the proposed skew-circulant matrix-based coefficient generator concept. The order of the harmonic canceling filter (HCF) can be configured to either one of three predefined settings, $n \in \{6, 12, 24\}$. First, the system architecture of the proposed synthesizer is discussed. Then, the circuit-level implementation of the individual building blocks is presented.

3.5.1 System Architecture

The principle idea of the reconfigurable harmonic canceling filter is illustrated in Fig. 3.15, where the number of the HCF tap coefficients is kept constant for all different configurations. The typical configuration ($n = 24$) is depicted in Fig. 3.15a, where 24 equally-spaced phases of an input square wave are weighted by the HC_{24} tap coefficients, $c_k = \cos(\frac{\pi k}{24})$. The weighted square waves are summed to produce a stepwise-approximated sine-wave that has the 47$^{\text{th}}$ harmonic as its first non-cancelable harmonic. In the proposed architecture, the square-wave phases are produced by a frequency divider that is driven by an input clock at a frequency of $f_{CLK} = 48f_0$, where $f_0 = 1/T_0$ is the frequency of the output sine-wave. Therefore, the maximum frequency of the output sine-wave is bounded to $f_0 = \max(f_{CLK})/48$. To extend the frequency range of the harmonic canceling synthesizer, the order of the HCF can be lowered. To double the maximum frequency of the output sine-wave while maintaining the same peak-to-peak amplitude, the HCF can be reconfigured to $n = 12$ as shown in Fig. 3.15b, where every two consecutive coefficients of HC_{24} are summed together; hence it is equivalent to two HC_{12} that are connected in parallel to produce the same output power of the HC_{24} configuration. Fig. 3.15c shows the HC_6 configuration that extends the maximum frequency of the output sine-wave to $f_0 = \max(f_{CLK})/12$.

Fig. 3.16 shows the system-level implementation of the proposed reconfigurable har-

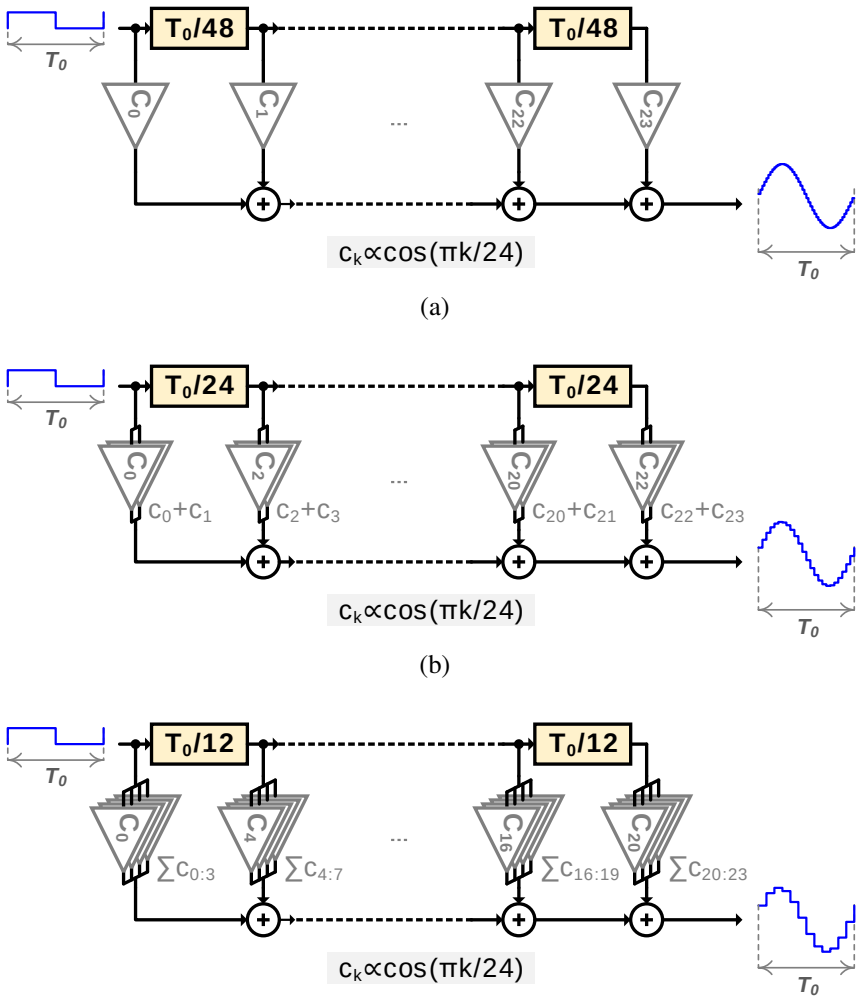


Figure 3.15: Conceptual block diagram of the reconfigurable harmonic canceling filter; (a) 24-tap HCF, (b) 12-tap HCF where every two consecutive coefficients of HC_{24} are summed together, and (c) 6-tap HCF where every four consecutive coefficients of HC_{24} are summed together.

monic canceling filter. It consists of an HC_{24} coefficient generator (CG), a current combiner, and a phase generator. The reconfigurability is implemented in the phase generator block, where the divide ratio of the clock divider is programmed and the square-wave phases are arranged as illustrated in Fig. 3.15. The proposed harmonic canceling synthesizer also allows either selecting the fundamental or the 5$^{\text{th}}$ harmonic. The bandpass harmonic canceling filter,

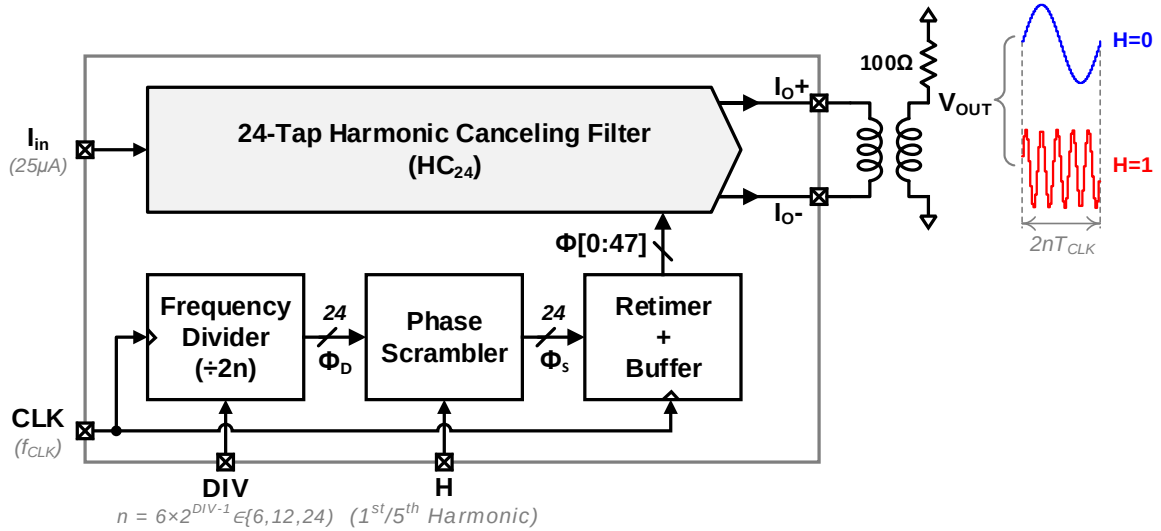
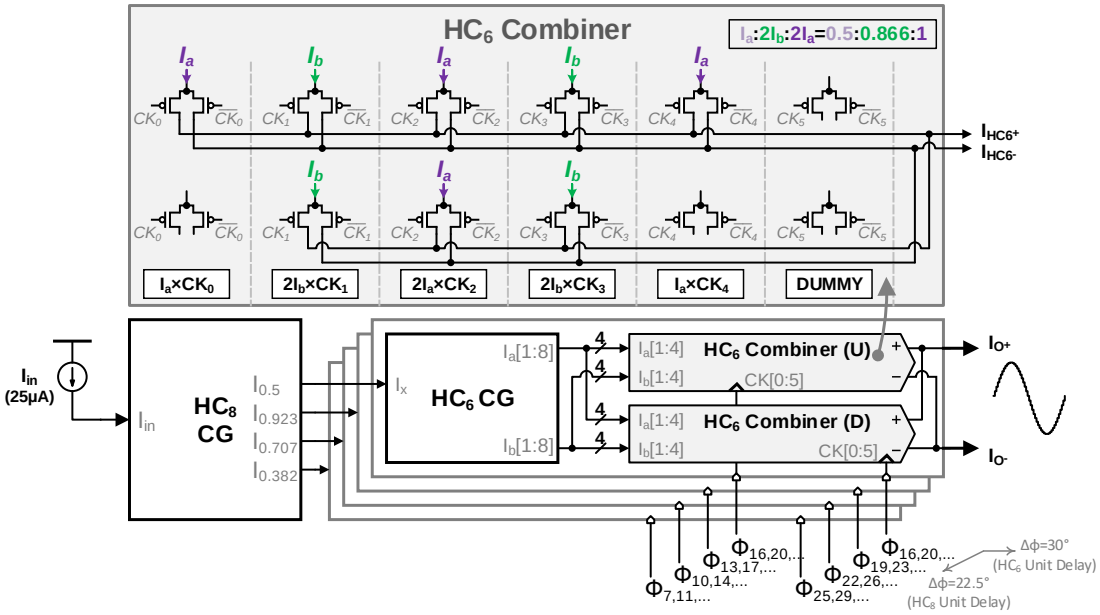


Figure 3.16: System-level implementation of the reconfigurable harmonic-canceling filter prototype.

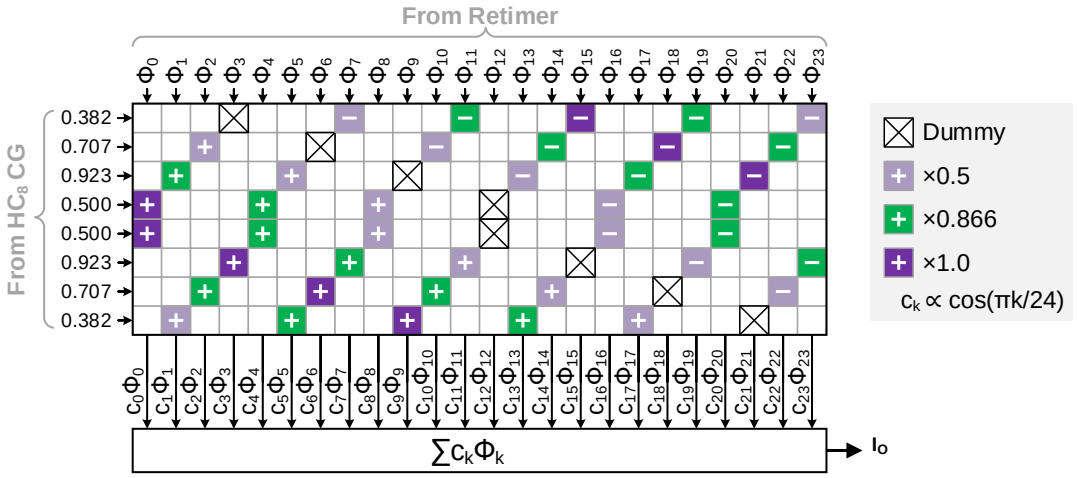
that is capable of selecting the 5th harmonic, is achieved by reordering of the square-wave phases as suggested in section 3.3.5. The phase re-arrangement is managed by the phase scrambler (PS) block, that is further discussed in section 3.5.3.

3.5.2 Coefficient Generator and Current Combiner for HC_{24} Tap Coefficients

The block diagram of the 24-tap harmonic canceling filter is shown in Fig. 3.17a. The 24-tap HCF is built of a cascade of an 8-tap HCF and a 6-tap HCF, as discussed in section 3.3.4. A single HC_6 CG followed by one HC_6 combiner forms one 6-tap HCF. The tap coefficients of a 6-tap HCF are known to be $(0.5, 0.866, 1, 0.866, 0.5, 0)$. The reduced implementation of the skew-circulant-matrix based 6-tap CG, that was illustrated in Fig. 3.12b, is utilized to generate the distinctive tap coefficients of the 6-tap HCF, i.e. $(1, 0.866)$. The generated coefficients are dc currents thanks to the current-mirror-based CG topology, which is further illustrated herein. The 6-tap CG is driven by an input current I_x and generates output currents $I_a = I_x$ and $I_b = 0.866 \times I_x$. Multiple copies of the output currents, I_a and I_b, are generated by having multiple output branches of the current-mirror-based CG. The



(a)



(b)

Figure 3.17: The 24-tap HCF topology as a cascade of 8-tap and 6-tap HCF sub-blocks; (a) block diagram of the proposed topology, and (b) the combination pattern of the clock phases and the tap coefficients where each row represents a 6-tap HCF, the color coding represents the absolute value of the tap coefficient, and the sign represents the polarity of the tap coefficient.

notation $I_a[1:8]$, for instance, represents a signal bus with eight copies of I_a. The 6-tap combiner is based on the current-steering topology that was discussed in [30]. The 6-tap

current combiner is shown in Fig. 3.17a, where six equally-spaced square waves, $CK_{0:5}$, are scaled by $(I_a, 2I_b, 2I_a, 2I_b, I_a, 0)$, which are proportional to the 6-tap HCF tap coefficients. The cascaded HCF topology is attained by instantiating eight 6-tap HCFs each biased by one of the HC_8 coefficients and clocked by a group of square-wave phases, where the groups are phase-shifted by $\pi/8$ with respect to each other, as shown in Fig. 3.17a. The reduced implementation of the skew-circulant-matrix based 8-tap CG, which was illustrated in Fig. 3.12a, is utilized to generate the distinctive tap coefficients of the 8-tap HCF, i.e. $(1, 0.923, 0.707, 0.382)$ that are supplied to the HC_6 instances.

The detailed combination pattern of the clock phases and the tap coefficients is depicted in Fig. 3.17b. Each row in Fig. 3.17b represents a 6-tap HCF; the color coding represents the absolute value of the tap coefficient, whereas the sign represents its polarity. The rows are scaled by the HC_8 tap coefficients annotated on the left side of each row. The sum of each column provides the tap coefficients of the 24-tap HCF and is effectively multiplied by the corresponding square-wave phase annotated at the top of each column. The time delay between two consecutive combiner subcells of each row is $\frac{4T_0}{48} = \frac{T_0}{12}$ that is the unit delay of the 6-tap HCF, whereas the time delay between each row and the one below it, is $\frac{3T_0}{48} = \frac{T_0}{16}$ which is the unit delay of the 8-tap HCF. The illustrated connection pattern guarantees a balanced load for all the square-wave phases, as shown in Fig. 3.17b, which reduces the systematic phase mismatch that limits the achievable harmonic rejection [30].

The circuit-level implementation of the coefficient generators is shown in Fig. 3.18. The 8-tap coefficient generator (CG_8) is depicted in Fig. 3.18a; the first stage is a closed-loop CG, which is a straightforward implementation of the block diagram shown in Fig. 3.13. The closed-loop CG_8 stage is followed by two open-loop CG_8 stages to achieve a THD better than 80 dB according to Fig. 3.14. A similar topology is used for the 6-tap coefficient (CG_6) as shown in Fig. 3.18b.

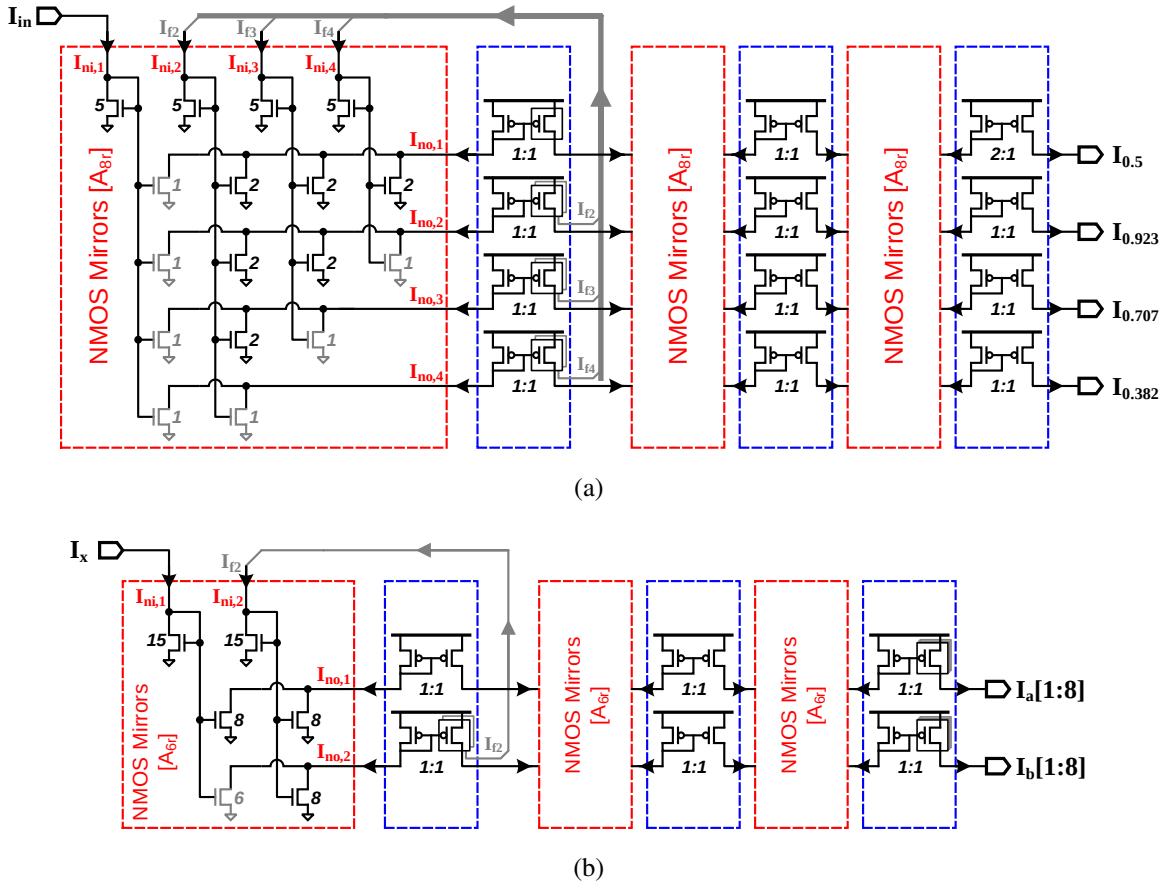
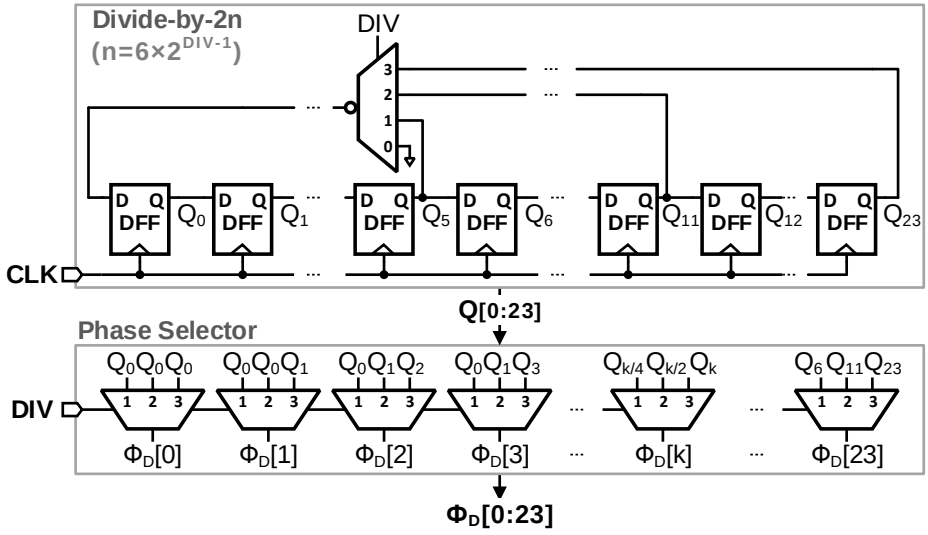


Figure 3.18: Circuit implementation of the coefficient generators: (a) 8-tap HCF coefficient generator, and (b) 6-tap HCF coefficient generator.

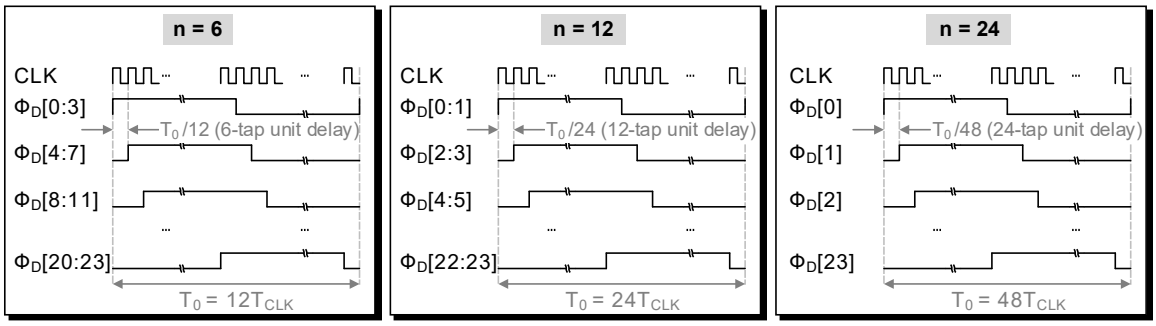
3.5.3 Phase Generator for HCF Tap Delays

3.5.3.1 Programmable Frequency Divider for HCF Order Reconfigurability

The reconfiguration of the proposed harmonic-canceling filter is implemented in the phase generator block. The conceptual architecture, which was discussed in Fig. 3.15, is achieved by the programmable clock divider shown in Fig. 3.19. The programmable clock divider is a variable-length ring counter, as shown in Fig. 3.19a, where an inverting feedback multiplexer (MUX) is used to select between the output of the 6^{th}, 12^{th}, or 24^{th} flip-flops to obtain clock division ratio of 12, 24, or 48, respectively. The outputs of the clock divider



(a)



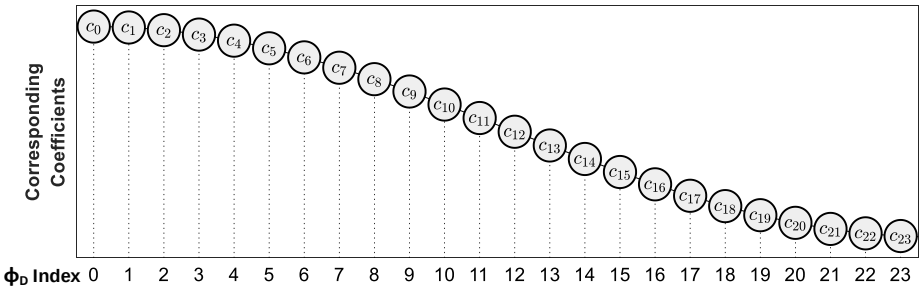
(b)

Figure 3.19: The programmable frequency divider required for HCF order reconfigurability; (a) schematic of the divide-by-n block, and (b) the timing diagram of output waveforms

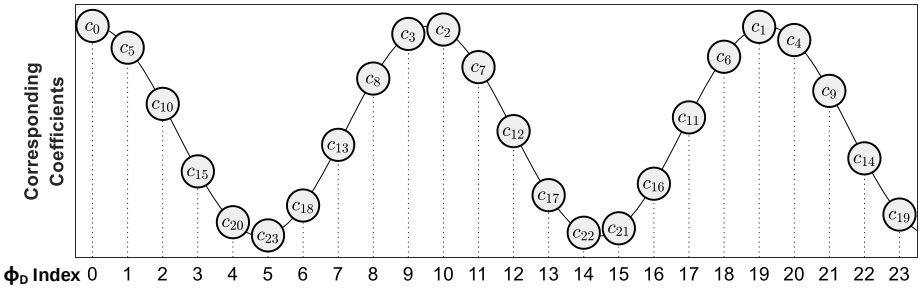
are applied to a phase selector block that implements the connection pattern, which was illustrated in Fig. 3.15. For instance, following the case of $n = 6$, a divide-by-12 block is needed, and every four consecutive coefficients of HC_{24} are connected in parallel. Hence, the output ports of the divide-by-12 block $Q\,[0:5]$ are connected to the output ports of the phase selector in the following pattern: $\phi_D\,[0:3] = Q\,[0]\,, \cdots\,, \phi_D\,[20:23] = Q\,[5]$. A similar phase selection pattern is implemented for the 12-tap configuration. The timing diagram of the proposed reconfigurable phase generator block is shown in Fig. 3.19 for various HCF

order settings, $n \in \{6, 12, 24\}$.

3.5.3.2 Phase Scrambler for Lowpass/Bandpass HCF Reconfigurability



(a)



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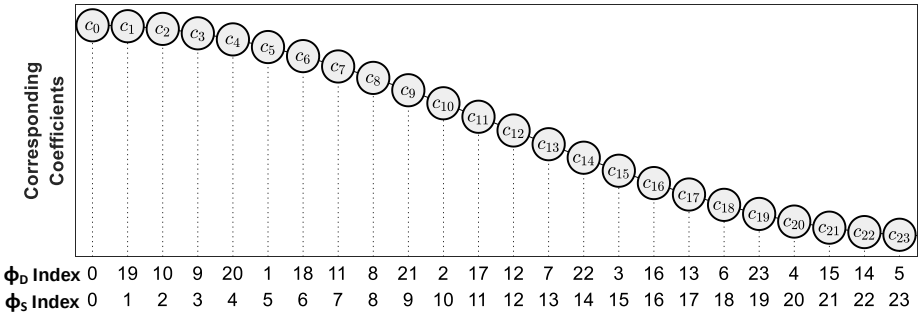


(c)

Figure 3.20: Phase scrambling concept: (a) square-wave phases $\phi_D[k]$ and corresponding tap coefficients to select the fundamental harmonic ($H = 0$), (b) $\phi_D[k]$ and corresponding tap coefficients to select the 5-th harmonic ($H = 1$), and (c) scrambling $\phi_D[k]$ for ($H = 1$) to maintain the order of tap coefficients.

The proposed harmonic-canceling filter can be configured to the bandpass HCF mode, where it enhances the 5th harmonic and cancels the fundamental harmonic. The enhanced harmonic number, $m = 5$, is coprime with $2n$ for all different HCF order settings. Therefore, the tap coefficients for the bandpass HCF, that equal the sampled impulse response $h_5[k] = \cos(5k\pi/n)$, can be obtained by reordering the tap coefficients of the lowpass HCF, $c_k = h_1[k] = \cos(k\pi/n)$, as suggested in section 3.3.5. This concept is illustrated in Fig. 3.20 for the 24-tap HCF. The typical lowpass HCF configuration is depicted in Fig. 3.20a, where $\phi_D[k]$ is multiplied by $c_k = \cos(k\pi/n)$. For the bandpass HCF configuration, the k-th square-wave phase, $\phi_D[k]$, should be multiplied by $h_5[k] = \cos(5k\pi/n)$, as shown in Fig. 3.20b. This can be implemented by either rearranging the HCF tap coefficients while maintaining the order of the square-wave phases or by simply rearranging the square-wave phases $\phi_D[k]$ while maintaining the order of the HCF tap coefficients. The later solution is adopted because of its lower implementation complexity by using digital multiplexers. Fig. 3.20c shows the mapping between clock divider's output phases, $\phi_D[0:23]$, to the scrambled phases, $\phi_S[0:23]$, that are required to enhance the 5th harmonic. The lowpass/bandpass HCF reconfigurability is implemented by a MUX-based phase scrambler (PS), that uses a control bit, H, to connect either $\phi_D[0:23]$ or $\phi_S[0:23]$ to the 24-tap HCF block.

3.5.3.3 Retimers

The output of the phase scrambler is sampled at the rising edge of the input clock, CLK, by a set of D flip-flops. This retiming technique [85] is utilized to reduce the phase errors that are induced by routing, the phase selection MUXs, and MUX-based phase scrambler.

Fig. 3.21 shows the simulated output waveforms and spectra for different HCF order settings, $n \in \{6, 12, 24\}$. All HCF order settings can be reconfigured to either select the fundamental harmonic ($H = 0$) as shown in Fig. 3.21a, or the 5th harmonic ($H = 1$) as

shown in Fig. 3.21b.

3.6 Experimental Results

The harmonic-canceling synthesizer is fabricated in a 180 nm CMOS technology. It occupies an active area of 0.51 mm^2. Fig. 3.22 shows the die micrograph of the system. The CLK signal is provided by an Agilent E8267D Vector Signal Generator. The differential output current is converted to a single-ended voltage by means of a 100 Ω resistive load and a balun. It is measured with an Agilent DSA91304A Infiniium Digital Signal Analyzer.

The prototype can be configured to one of the three HCF order settings, $n \in \{6, 12, 24\}$, each of them with a programmable band-pass feature. The performance of each of the six operation modes is characterized by its power consumption, SFDR, and output frequency range f_o. Fig. 3.23 shows the measured power and SFDR versus output frequency, f_o, of the 24-tap HCF when the fundamental harmonic is of interest ($H = 0$).

The CG and Combiner blocks consumes dc current, therefore their power consumption is independent of frequency. In addition, SFDR decreases with frequency due to the increasing phase error from the phase generator block. Fig. 3.24 presents the measured output power spectral density (PSD) of the 24-tap HCF. For $H = 0$, the main harmonic (MH) is the fundamental one, and the first non-cancellable harmonic is the 47$^{\text{th}}$ harmonic. For $H = 1$, the main harmonic is the 5$^{\text{th}}$ harmonic, and the first non-cancellable harmonic is the 43$^{\text{rd}}$.

Table 3.2 summarizes the performance of each operation mode and compares it with previous work. This work presents the highest number of operation modes and the highest-order HCF, i.e. the highest first non-cancellable harmonic. Also, it offers the first band-pass HCF implementation. The modular SCM-based CG provides comparable SFDR values with respect to previous works that use calibration schemes.

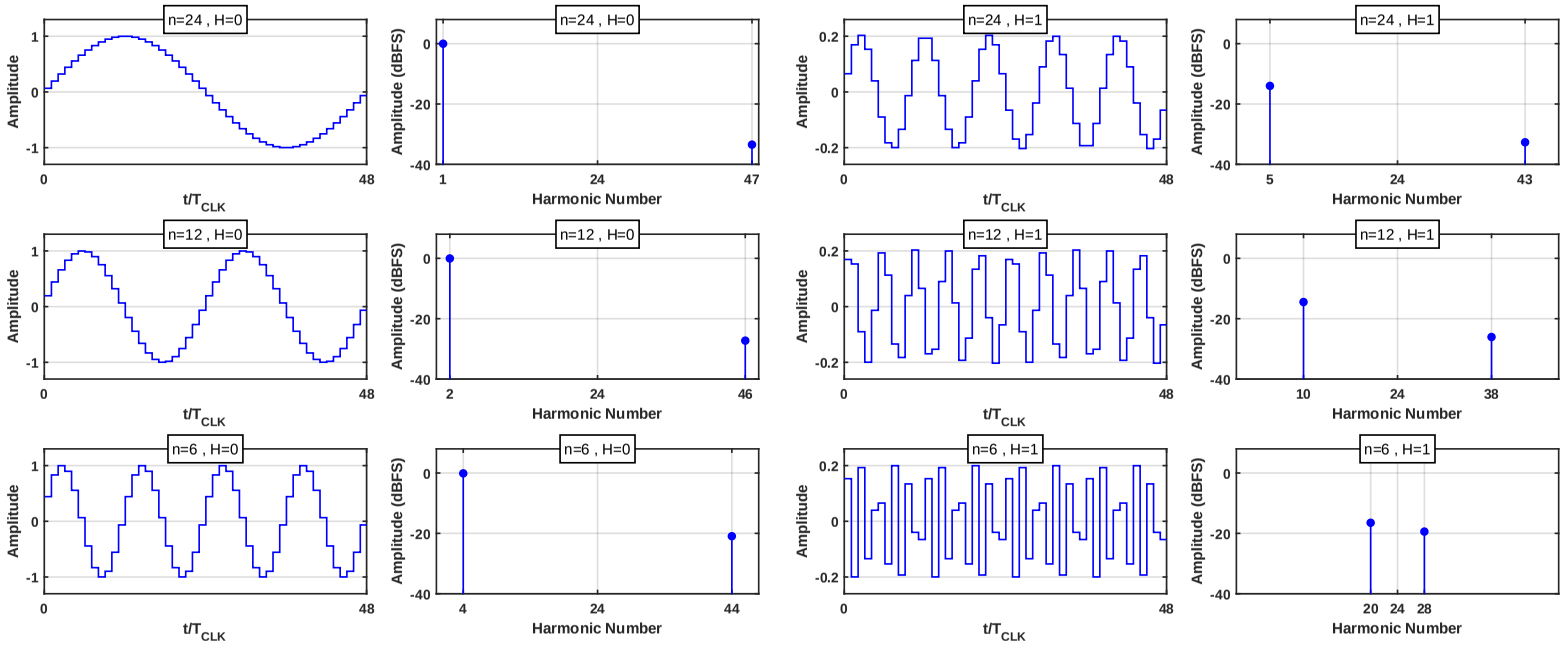


Figure 3.21: Simulated output waveforms and spectra for different settings of HCF order ($n = \{24, 12, 6\}$): (a) selecting the fundamental harmonic ($H = 0$), and (b) selecting the 5$^{\text{th}}$ harmonic ($H = 1$).

Table 3.2: Performance Summary and Comparison with the State-of-the-Art Single-tone Synthesizers

	FIR HCF	**MH**	**f_o (MHz)**	**SFDR (dBc) @ f_o (MHz)**	**Power (mW) @ f_o (MHz)**	**Area (mm^2)**	**Tech.**	**Coefficient Generator**
This work	**5-tap**	**1st**	**0.8-60**	**66.4 @ 0.8 52.9 @ 60**	**6.8 @ 0.8 19.1 @ 60**	**0.51**	**180nm CMOS**	**SCM-based**
		5th	**33-100**	**46.5 @ 33 38.4 @ 100**	**6.1 @ 33 8.7 @ 100**			
	11-tap	**1st**	**0.8-32**	**64 @ 0.8 53 @ 32**	**6.8 @ 0.8 15.3 @ 32**			
		5th	**8.3-75**	**43.7 @ 8.3 38.8 @ 75**	**5.3 @ 8.3 8.7 @ 75**			
	23-tap	**1st**	**0.8-12.5**	**63.7 @ 0.8 54.6 @ 12.5**	**6.9 @ 0.8 13.3 @ 12.5**			
		5th	**2-50**	**53.6 @ 2 46.2 @ 50**	**5.1 @ 2 10.2 @ 50**			
[31]	5-tap	1st	1.67-333	45† @ 166 60‡ @ 166	NR	0.011	28nm FDSOI	VCCS + calibration
[30]	11-tap	1st	0.01-1	NR	4	0.056	130nm CMOS	Current Mirrors
[29]	4-tap	1st	1-10	68.7† @ 1 71.6‡ @ 1	0.9 @ 1 1.2 @ 10	0.066	130nm CMOS	Unit-current switches+DEM
[28]	5-tap	1st	150-850	50.5† @ 150 60.3‡ @ 150 47† @ 750 70‡ @ 750	9.1 @ 150 57.2 @ 850	0.08	180nm CMOS	Resistor-ratios + calibration
[27]	7-tap	1st	1.11	77* @ 1.11	3.24	0.04	180nm CMOS	Capacitor Ratios
[26]	7-tap	1st	20-220	45 @ 100	NR	0.045	90nm CMOS	Current Mirrors

NR: Not reported, †: without calibration or DEM, ‡: with calibration or DEM, *:-THD
VCCS: Voltage-controlled current source, DEM: Dynamic element matching

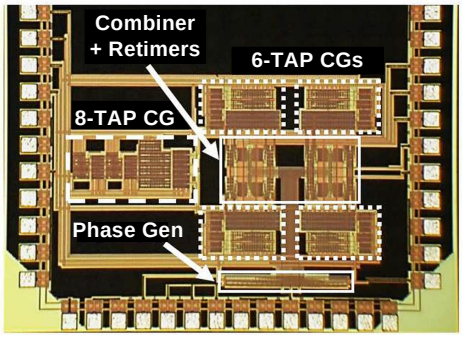


Figure 3.22: Die micrograph of the harmonic-canceling synthesizer prototype.

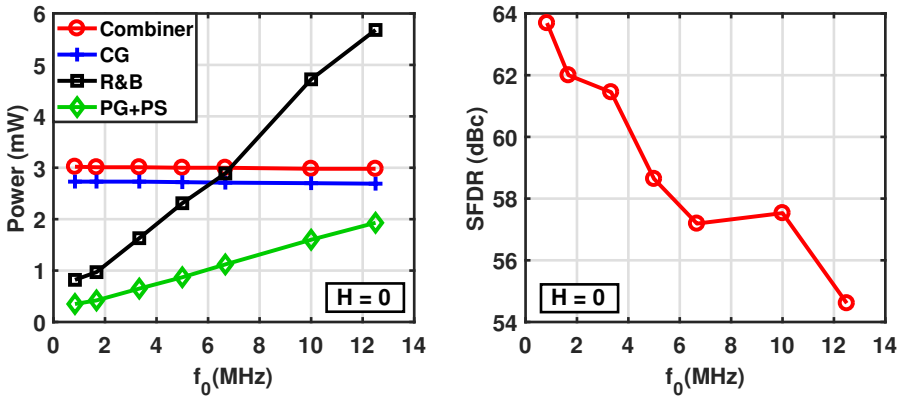


Figure 3.23: Measured power and SFDR versus output clock frequency for the 24-tap HCF setting.

3.7 Conclusion

In this work, a harmonic-canceling single-tone synthesizer that uses an SCM-based coefficient generator for BIST applications is proposed. This coefficient generator generates irrational coefficients from integer numbers in a recursive approach with no calibration scheme, relaxing the trade-off between output linearity and coefficient mismatch. The selectable 24-tap, 12-tap and 6-tap HCFs are implemented along with their band-pass versions. They cover a frequency range from 0.8 MHz to 100 MHz and provide the highest number of operation modes and the highest first non-cancellable harmonic reported. Measured SFDR values

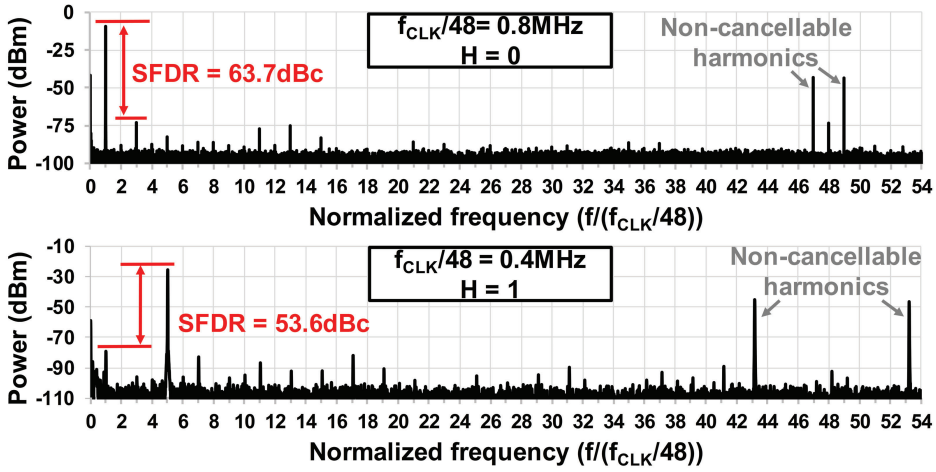


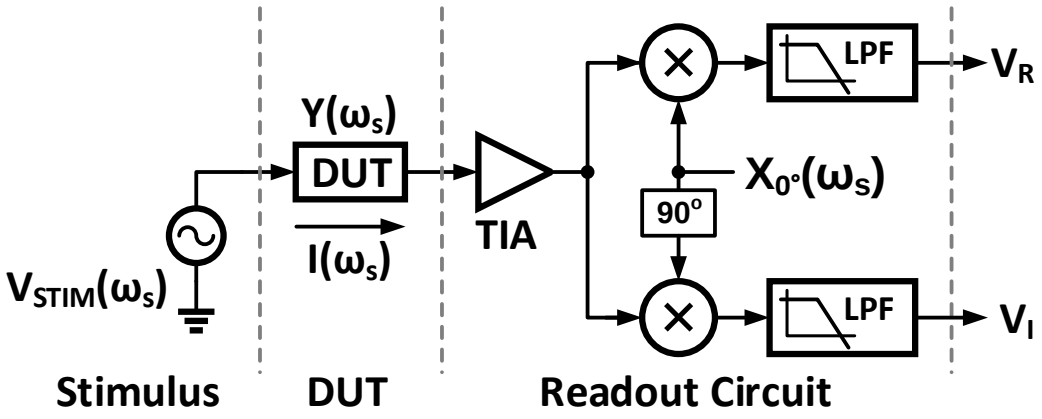
Figure 3.24: Measured output spectra for both lowpass (H=0), and bandpass (H=1) 24-tap HCF configurations.

prove the effectiveness of the proposed SCM-based coefficient generator architecture.

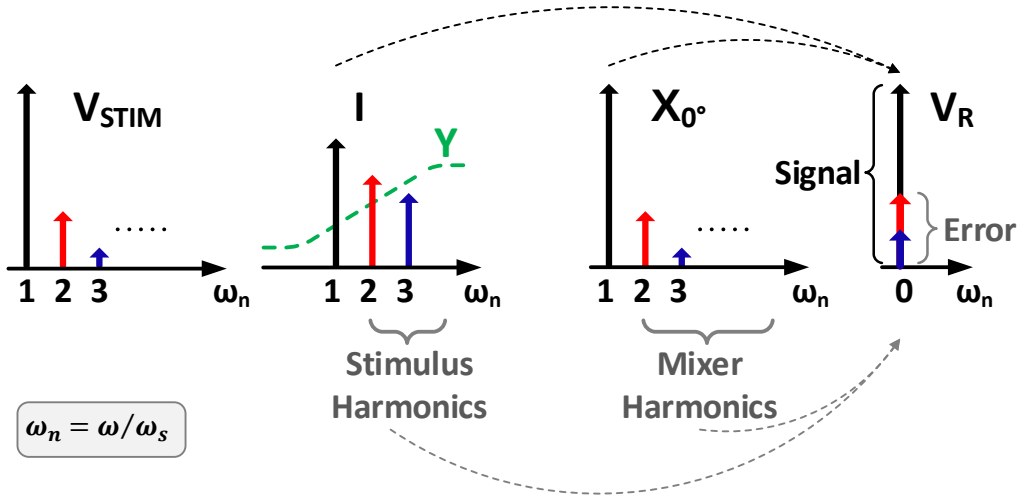
4. AN IMPEDANCE ANALYZER WITH ON-CHIP STIMULUS GENERATOR FOR ELECTROCHEMICAL IMPEDANCE SPECTROSCOPY APPLICATIONS

4.1 Introduction

Compared to optical, calorimetric, and piezoelectric sensors, electrochemical impedance spectroscopy (EIS) sensors offer a low-cost, simple, highly sensitive, and easy-to-miniaturize tool for characterizing biomolecular interactions to capture and detect specific analytes (e.g., DNA and proteins) on a surface [86] . The coherent detection technique, shown in Fig. 4.1a, is well known in high precision EIS systems [86–90]. It uses a sinusoidal signal at a particular frequency to stimulate the device under test (DUT). Then, the current flowing in the DUT is amplified by a transimpedance amplifier (TIA). Quadrature mixers followed by low-pass filter (LPF) are then used to extract the magnitude and phase of the admittance of the DUT. However, the vast majority of these EIS systems employ impedance analyzers that rely on highly-linear external sinusoidal stimulus sources [86, 87, 89], which impede miniaturization to the scale required for hand-held or point-of-care (PoC) devices. Notably, the measurement accuracy of EIS systems strongly depends on the accuracy of the stimulus sine-wave and the demodulating sine-wave used in the quadrature mixers. Fig. 4.1b shows the effect of non-zero harmonic content of the stimulus and demodulating sine-waves on the impedance measurement accuracy [91, 92]. Two approaches have been previously proposed for miniaturized sine-wave stimulus generators: 1) on-chip generation of staircase approximation of a sine-wave [88]; 2) a high-accuracy $\Sigma\Delta$ representation of a sine-wave stored in a read-only-memory (ROM) embedded in an external field-programmable gate array (FPGA), which is fed into an on-chip voltage-to-current converter, and then filtered out by an off-chip low-pass filter (LPF) to reduce high-frequency quantization noise [90]. Thus, either the measurement accuracy or system miniaturization is compromised.



(a)



(b)

Figure 4.1: a) Coherent detection technique for impedance measurement, and b) effect of stimulus's harmonics on the measurements' accuracy.

This work proposes a distributed harmonic canceling technique that allows the implementation of a fully-integrated impedance analyzer capable of providing high-precision impedance measurements with less than 1.2% error over the 0.01–100 kHz range. Following the introduction section, the proposed system architecture is illustrated in Section 4.2. Section 4.3 discusses the circuit-level implementation of the stimulus generator and impedance readout circuit. The experimental results are presented in Section 4.4, followed by conclusions in Section 4.5.

4.2 System Architecture

The conceptual block diagram of the system is shown in Fig. 4.2. Instead of using a sine-wave stimulus, a slew-rate controlled three-level stimulus voltage (V_{STIM}) is used to interrogate the device under test (DUT). Harmonic filtering techniques are utilized on the stimulus generator to generate V_{STIM} from a digitally-friendly square-wave clock, and on the impedance readout (IRO) circuit to eliminate the errors induced by the spurious harmonics of V_{STIM}. On the stimulus generator side, two phases of a square-wave clock, at sensing frequency (f_s) and shifted by $60°$ ($T_s/6$) with respect to each other, are applied to two slew-rate-control (SRC) blocks to set their rise and fall times to $T_s/7$. From the frequency domain perspective, this corresponds to filtering each clock by a sinc filter, H_{sinc}, which has nulls at integer multiples of $7 \cdot f_s$. The filtered clocks are summed with equal weights to generate the output stimulus voltage, V_{STIM}, which can be thought of as the output of a 2-tap finite-impulse-response (FIR) filter [28]. The FIR filter, $H_{FIR,1}$, places notches at odd multiples of $3 \cdot f_s$, therefore the resulting spectral content of V_{STIM} will be as shown in Fig. 4.2. The DUT is interrogated by V_{STIM}, resulting in a current, I_{DUT}, that carries both wanted information about DUT admittance at sensing frequency, $Y(j\omega s)$, and unwanted information about DUT admittance at the remaining harmonics' frequencies.

On IRO circuit side, I_{DUT} is converted to a voltage by a low-noise transimpedance am-

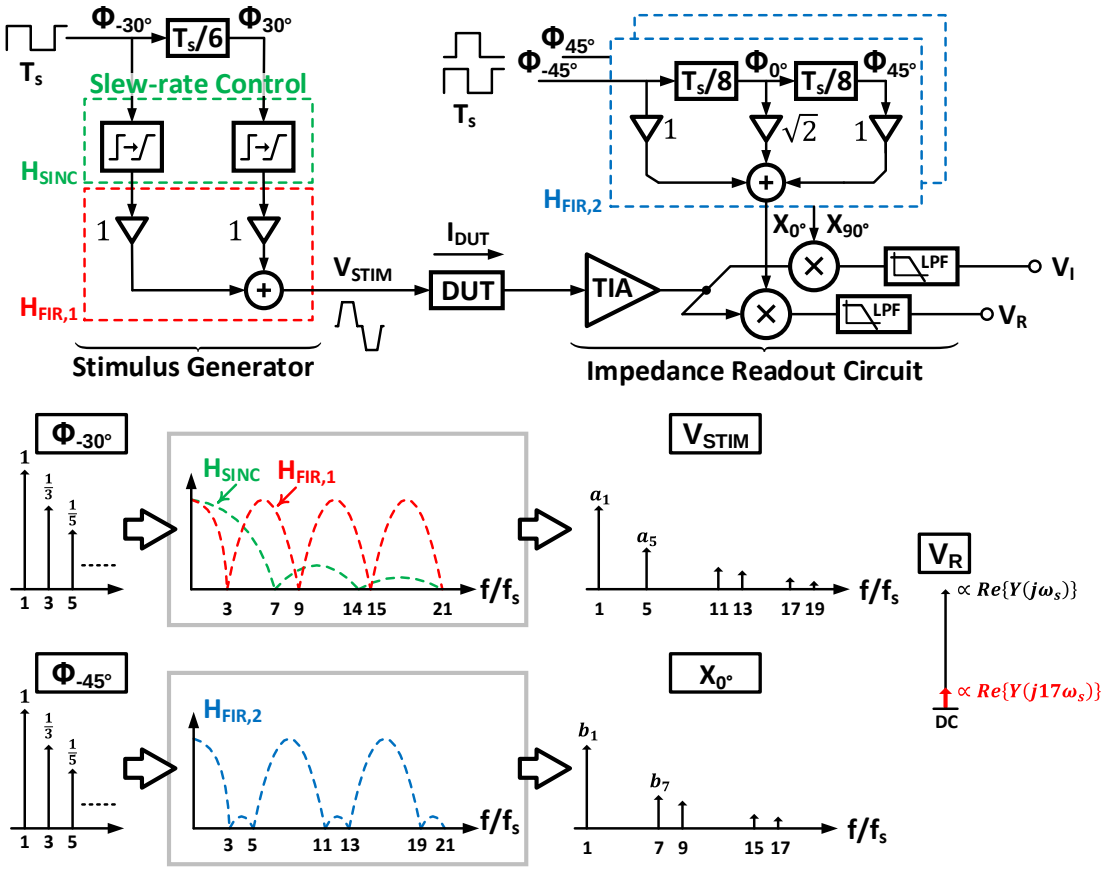


Figure 4.2: Conceptual block diagram of the proposed impedance analyzer based on harmonic cancellation techniques in stimulus generator and impedance readout circuit.

plifier (TIA). Then, it should be ideally multiplied by in-phase and quadrature-phase sine waves (X_{0° and X_{90°) of frequency f_s, and low-pass filtered to provide two DC outputs V_R and V_I that are respectively proportional to the real and imaginary parts of $Y(j\omega s)$. In our proposed topology, a 3-tap FIR filter, $H_{FIR,2}$, is designed to cancel the spurious harmonics of the multiplying square-wave clocks that coincide with the remaining harmonics of V_{STIM} as shown in Fig. 4.2. The 17$^{\text{th}}$ harmonic is the first non-canceled harmonic in both V_{STIM} and X_{0° (X_{90°); therefore, it causes error in DUT impedance measurement. However, this error is below 1% due to the natural attenuation of the 17$^{\text{th}}$ harmonic with respect to the fundamental component in the square wave spectrum and the additional attenuation caused by H_{sinc}. A proximate accuracy may be attained with a sine-wave stimulus generator using the FIR filter approach [28] without further harmonic cancellation on the IRO side. However, a complete cancellation of all square-wave spurious harmonics up to the 17$^{\text{th}}$ in the stimulus generator side requires a 9-tap FIR filter with irrational tap coefficients, which is more complicated compared to the proposed topology.

4.3 Circuit Implementation

Fig. 4.3 shows the schematic of the stimulus generator. A frequency divider module divides a master clock, $MCLK$, by 12, generating the different phases of the sensing clock (f_s) used by both the stimulus generator and the IRO circuits. A switched-C current source, clocked by two non-overlapping phases of $MCLK$, Φ_1 and Φ_2 , are used to generate a reference current, I_{REF}, proportional to f_s. The reference current is mirrored by a ratio K to two current starved inverters that are clocked by two phases (30° and 330°) of f_s and loaded by two active-C integrators. The output of each integrator is a square wave with rising and fall times set by the ratio between the integrator's feedback capacitance, C_4, and I_{REF}. This ratio is designed to be a constant fraction of T_s over the entire frequency range as shown in Fig. 4.3. The outputs of the integrators are summed by a resistive network and attenuated by

a digitally-programmable-attenuator (DPA) to vary the amplitude of V_{STIM} over the range 4.7–600 mV_{pp}.

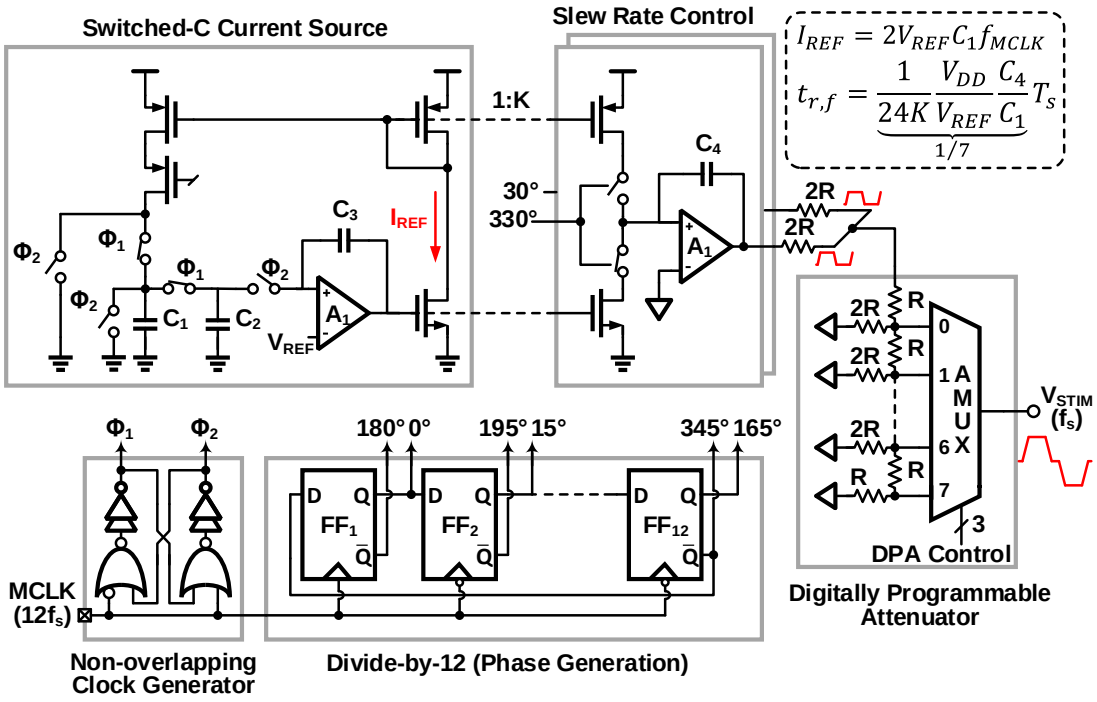


Figure 4.3: Schematic of the stimulus generator.

The circuit-level implementation of the IRO circuit is shown in Fig. 4.4. The G_m-boosted common-gate TIA architecture lowers the input impedance of the TIA [28, 89]. The stimulus voltage is applied to the reference terminal of the G_m-boosting OTA (A_2); hence, it does not drive the DUT directly. Therefore, no output buffer is needed in the stimulus generator, which decreases its power consumption. A replica TIA is added that plays two roles: 1) It lowers the dc mismatch at the input of the following mixers [86], and 2) it partially cancels the effect of the parasitic capacitance (C_p) of the I/O pad and the circuit board as its admittance, $Y_p(j\omega s)$, appears as a common-mode signal at the output of the TIA. The output

of the TIA is fed to fully balanced Gilbert-cell quadrature mixers. The 3-tap FIR filter $H_{FIR,2}$ is implemented within each mixer; the active part of the mixer is split into three parts with transconductances weighted according to the tap coefficients (1,$\sqrt{2}$ and 1) and clocked by sensing clock phases ($-45°$, $0°$, $45°$) respectively.

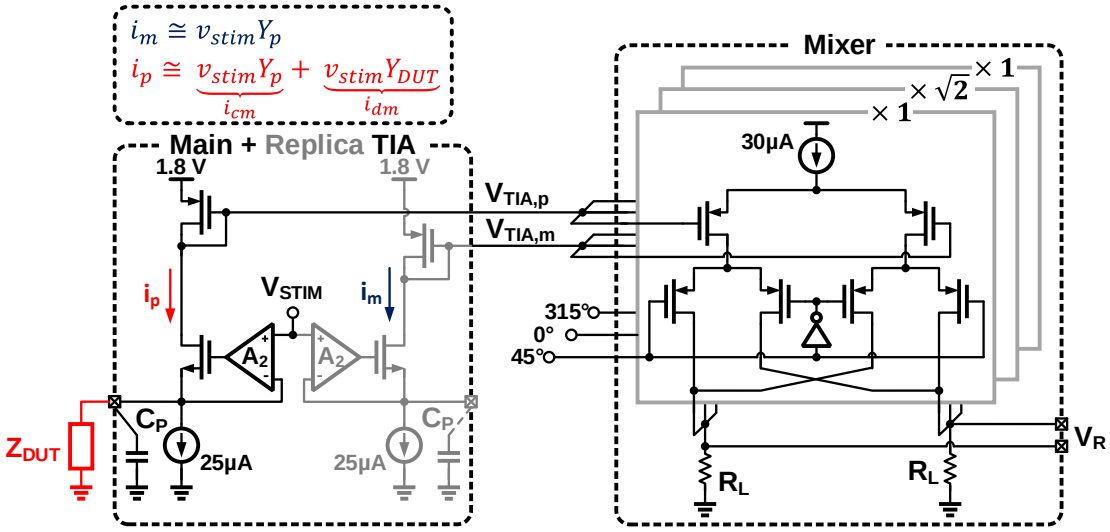


Figure 4.4: Circuit-level implementation of the impedance readout circuit.

4.4 Experimental Results

The impedance spectroscopy system is implemented in a 180 nm CMOS technology. A die micrograph of the chip is shown in Fig. 4.5. The stimulus generator and the IRO circuits occupy 0.19 mm^2 and 0.055 mm^2 , and consume 640 μW and 324 μW from a 1.8 V supply at $f_s = 100$ kHz, respectively. The chip is packaged in a QFN48 package and mounted on a PCB, where all the connectors and power supply filters for low noise requirements are placed.

Fig. 4.6a shows the output waveform of the stimulus generator for $f_s = 1$ kHz, that is a slew-rate-controlled 3-level signal. The rising and falling times are $T_s/7$ which result in

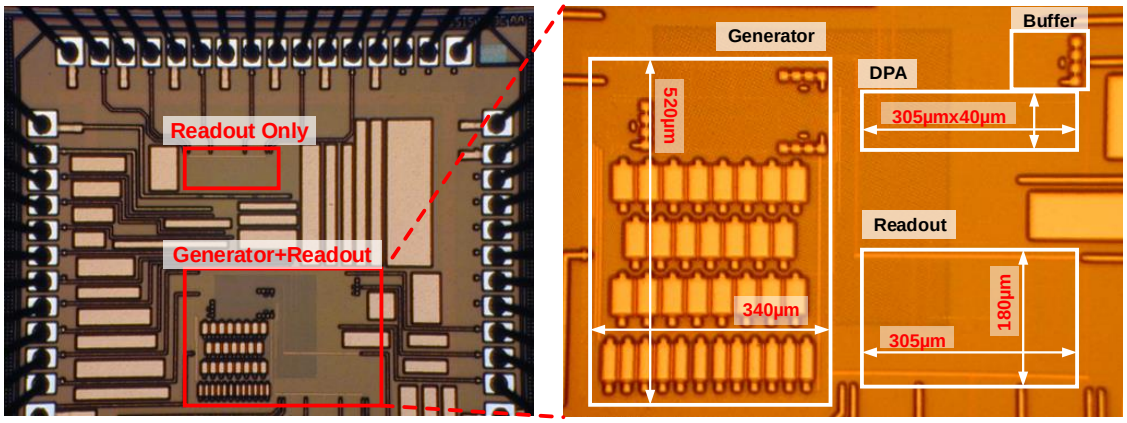
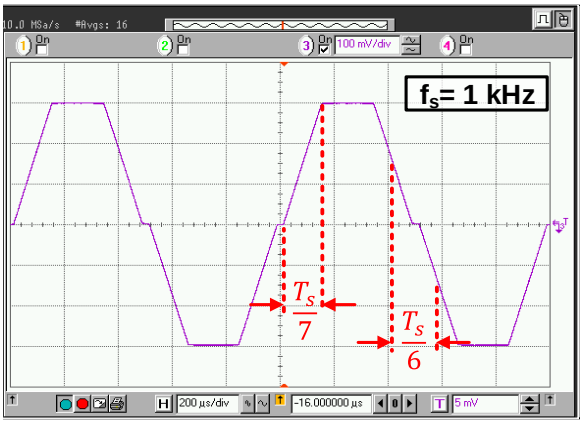


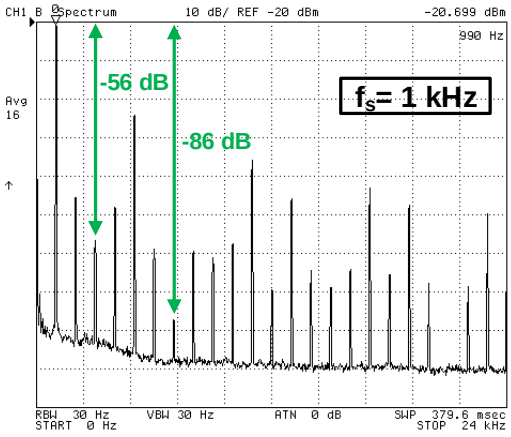
Figure 4.5: Chip micrograph.

suppression of the 7th harmonic. The frequency spectrum of V_{STIM} is shown in Fig. 4.6b for $f_s = 1$ kHz showing the attenuation of the 3rd and the 7th harmonics and all their odd multiples. Fig. 4.6c shows the effectiveness of the stimulus generator's proposed harmonic filtering techniques over the whole sensing frequency range. $H_{FIR,1}$ achieves more than 40 dB attenuation for the 3rd harmonic and improves at higher order harmonics, while H_{sinc} achieves more than 60 dB attenuation for the 7th harmonic over the whole frequency range as depicted in Fig. 4.6c.

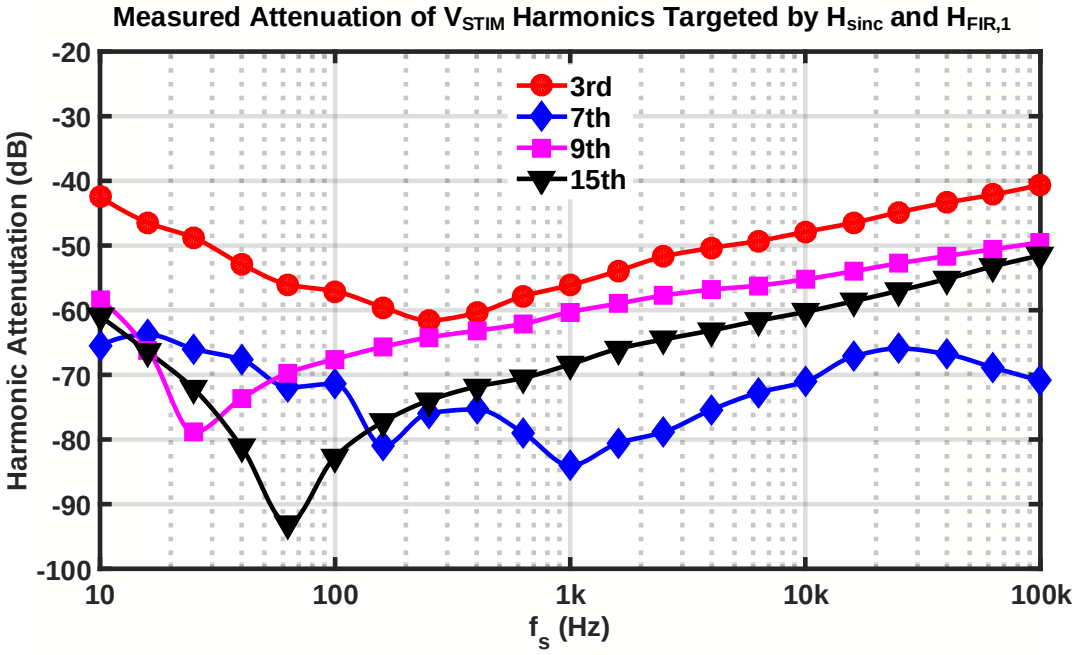
The measurement results of the impedance readout circuit are shown in Fig. 4.7. The total gain is 88 dB and the 1-dB compression point is at 40 μA_{pp}, as depicted in Fig. 4.7a, which sets a lower bound of 120 Ω to DUT impedance for $V_{STIM} = 4.7$ mV_{pp}. To validate the effectiveness of the harmonic cancellation technique of the IRO, the attenuation of the spurious harmonics targeted by the nulls of $H_{FIR,2}$ is depicted in Fig. 4.7b, which shows more than 40 dB attenuation over the whole range of f_s (0.01–100 kHz). The total integrated noise of the impedance readout circuit is 103 pA_{rms} over a 10-Hz bandwidth. Therefore, the upper bound of the detectable DUT impedance is 1 GΩ for $V_{STIM} = 300$ mV_{pp}. Fig. 4.8 depicts the minimum and maximum detectable DUT impedance at each attenuation setting of the DPA showing a 103 dB dynamic range.



(a)

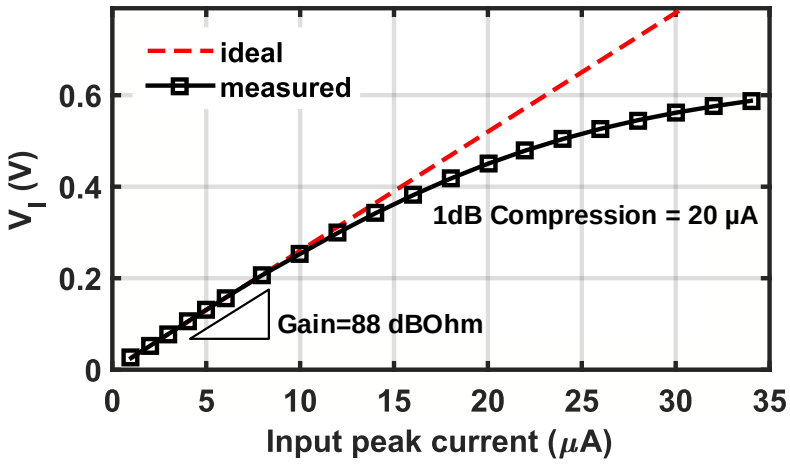


(b)

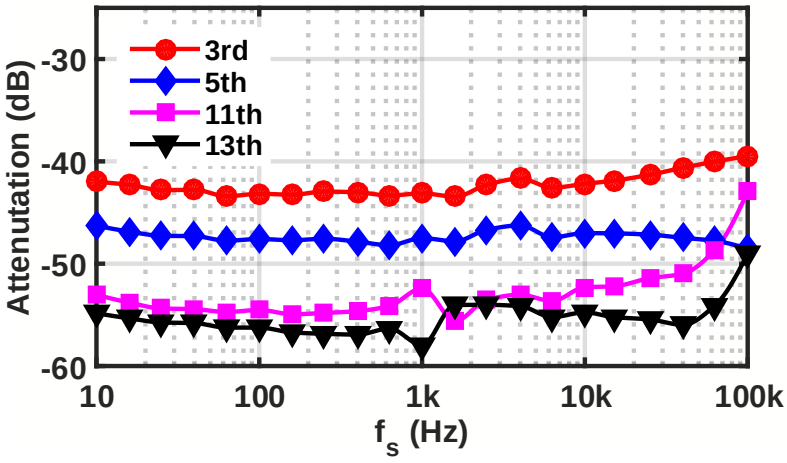


(c)

Figure 4.6: Stimulus generator's measurement results: a) output waveform for f_s=1 kHz, b) spectrum for f_s= 1 kHz, and c) measured harmonic attenuation of V_{STIM} harmonics targeted by H_{sinc} and $H_{FIR,1}$ versus sensing frequency, f_s.



(a)



(b)

Figure 4.7: Measurement results for the IRO; a) input/output linearity, and b) the measured harmonic attenuation versus sensing frequency, f_s.

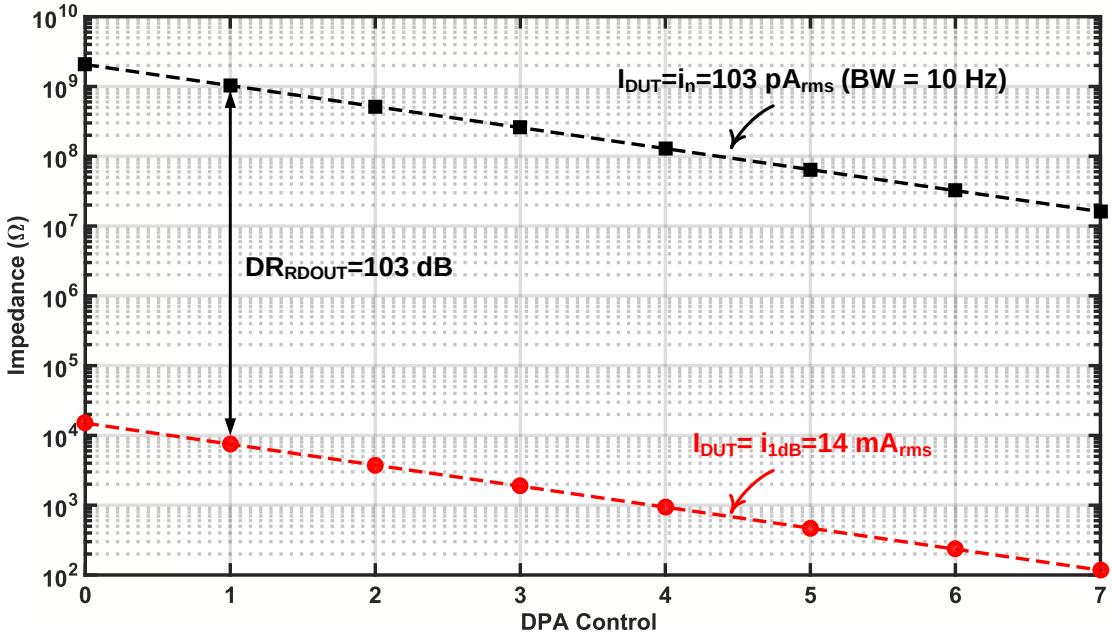


Figure 4.8: Range of detectable DUT impedance defined by the impedance readout circuit's 1-dB compression point, total integrated input referred noise, and the amplitude of V_{STIM} ($^{600}/_{2^{DPA}}$ mVpp).

Fig. 4.9 shows the sum of the measured harmonic attenuation (in dB) of both the stimulus generator and the impedance readout circuit showing the efficacy of the utilized harmonic cancellation technique for all spurious harmonics up to the 17th. The achieved harmonic attenuation results in an impedance measurement accuracy like that achieved with a sinusoidal source with total harmonic distortion (THD) of more than 65 dB. It is worth noting that the harmonics attenuation listed above are attained without employing any kind of phase, amplitude or mismatch calibration.

Fig. 4.10 shows the magnitude and phase spectra of a known impedance structure which mimics the impedance of an EIS biosensor. The continuous red lines are the analytically expected curves and the squares are the experimental values extracted from the dc outputs V_R and V_I over the sensing frequency range of 0.01-100 kHz. It shows the efficacy of the proposed system to measure the impedance with less than 1.2% error. Table 4.1 compares

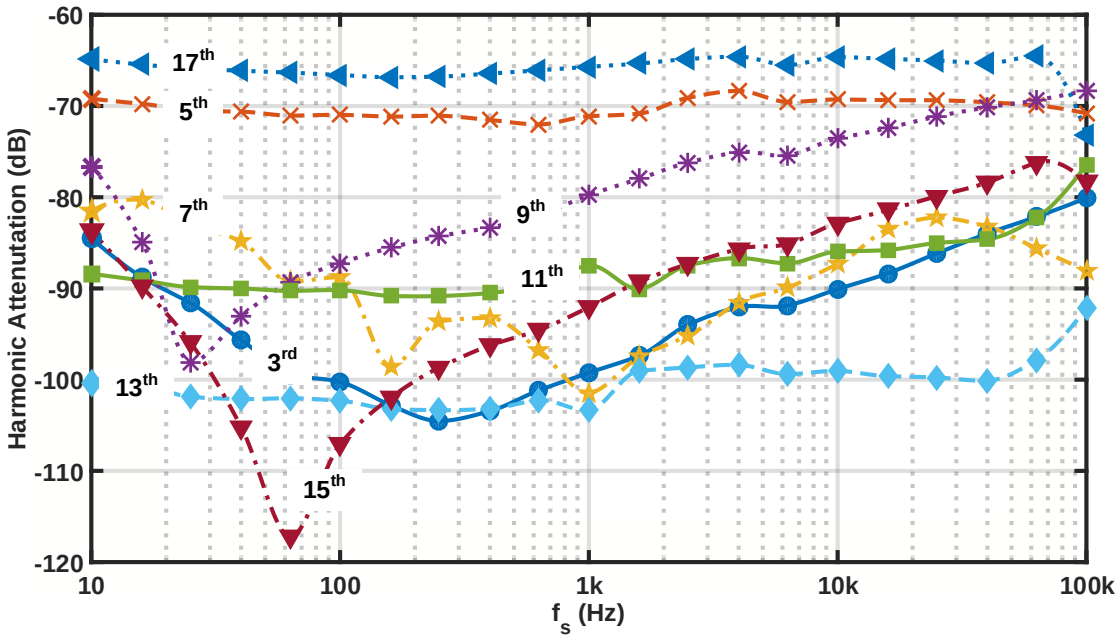


Figure 4.9: The sum of measured harmonic attenuation (in dB) of both the stimulus generator and the impedance readout circuit showing the effectiveness of the utilized harmonic cancellation techniques for all spurious harmonics up to the 17^{th}.

the measured performance of the proposed impedance analyzer against the state-of-the-art impedance analyzers. To the best of our knowledge, the proposed system achieves the highest level of integration with an on-chip stimulus generator that achieves the best power performance while maintaining high precision impedance measurements.

4.5 Conclusion

In this work, an impedance analyzer with an on-chip stimulus generator for electrochemical impedance spectroscopy applications was introduced. The study demonstrated and verified that the system provides sub-GΩ impedance measurement with less than 1.2% error over the sensing frequency range of 0.01–100 kHz thanks to the proposed harmonic canceling scheme. The impedance analyzer system prototype was implemented in a 180 nm CMOS technology, the stimulus generator and the impedance read-out circuits consume 0.64 mW and 0.32 mW, respectively, from a 1.8 V supply.

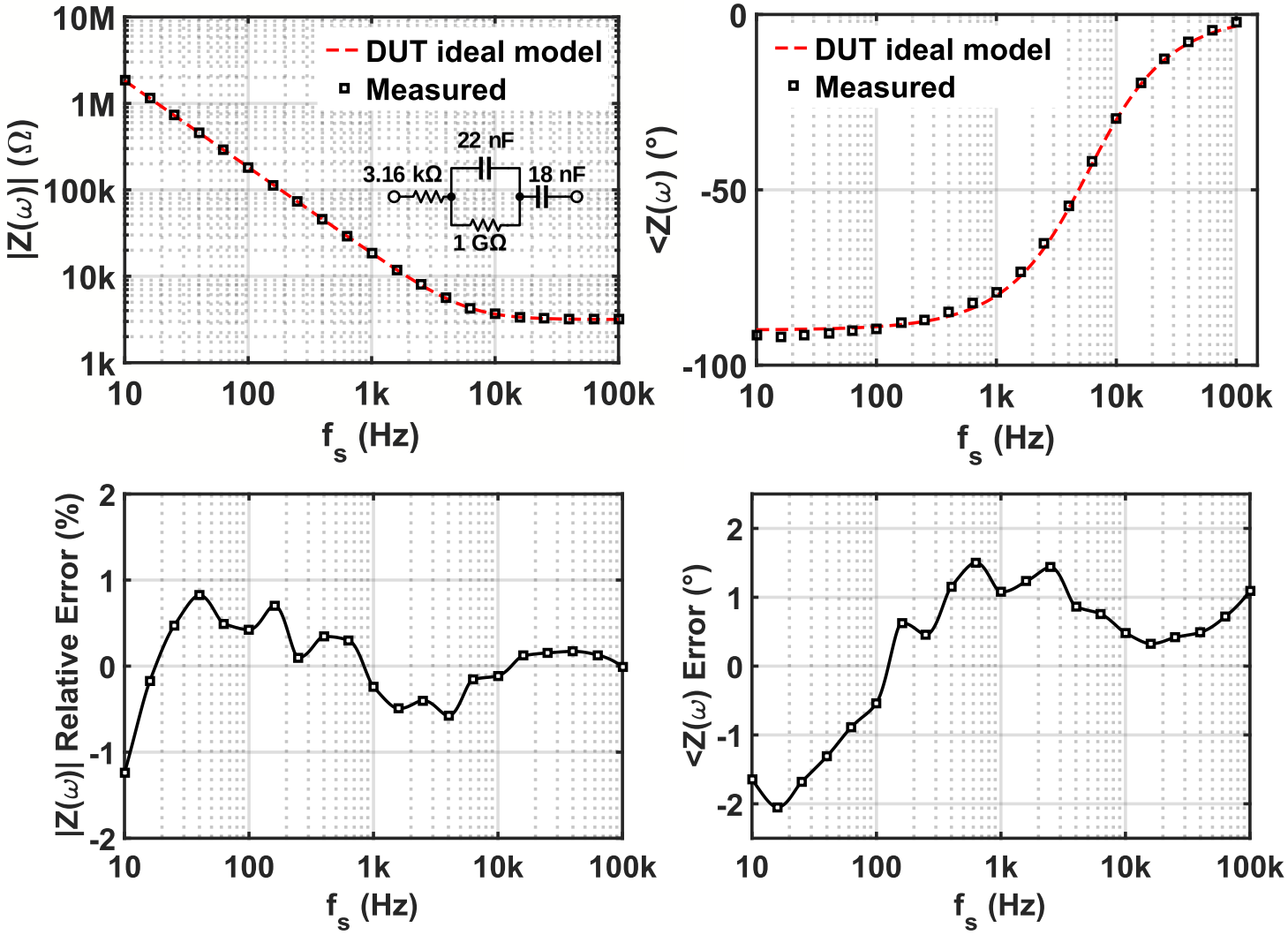


Figure 4.10: Measured impedance magnitude and phase spectra of a known DUT, and the measurement error.

Table 4.1: Performance Summary and Comparison with the Prior Art

	[86]	[87]	[88]	[90]	[89]	This Work
Technology (μm)	0.35	0.5	0.13	0.35	0.18	0.18
Supply Voltage (V)	3.3	3	1.2	N/A	1.8	1.8
Impedance Readout Circuit (per channel)						
Power (μW)	840 (w/o ADC)	6 (w/ ADC)	42 (w/ ADC)	1650 (w/ ADC)	144 (w/ ADC)	324 (w/o ADC)
Area (mm^2)	0.01	0.06	0.06	2.25	0.48	0.055
Dynamic Range (dB)	97	50	140	86–96	152	103
Noise (pA$_{rms}$)[BW=10 Hz]	330	N/A	0.32	N/A	0.163	103
Frequency Range	10 Hz–50 MHz	10 kHz	0.1 Hz–10 kHz	16 kHz	10 Hz–100 kHz	10 Hz–100 kHz
Stimulus Generator						
Type	-	-	8-bit Stepwise Approximation	$\Sigma\Delta$ + LPF†	-	FIR+Sinc Filtering
Frequency	-	-	0.1 Hz–10 kHz	1, 2, 4, 8, 16 kHz	-	10 Hz–100 kHz
Area (mm^2)	-	-	0.04	N/A	-	0.19
Power (mW)	-	-	1.1	N/A	-	0.5–0.64
Impedance Measurement Error	-	-	$<$8.4%	$<$0.02%	-	$<$1.2%

† External FPGA and passive LPF are used

5. CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

This dissertation proposed concepts that achieve high-linearity and process resilience for analog filters, analog BIST, and impedance spectroscopy applications in scaled CMOS technologies.

Section 2 has introduced a highly linear process-resilient RO-based filter. A linearized CCO (linCCO) has been proposed that mimics the operation of the active-RC filter topology in the phase-domain to achieve state-of-the-art linearity. Furthermore, a zero compensation technique has been presented to extend the achievable bandwidth of the proposed topology. Also, a DLL-based frequency tuning scheme was introduced to achieve PVT resilience for the proposed linCCO-based filter topology. As a proof of concept, we demonstrated and verified a continuous-time fifth-order filter prototype with a cut-off frequency that is tunable from 1.5 MHz to 22 MHz and achieves state-of-the-art linearity at 1 V. The proposed filter was implemented in a 130 nm CMOS technology. It consumes 6.2–8.9 mW and achieves a 26.2 dBm in-band IIP3. Thanks to the DLL-based tuning scheme, the filter achieves a bandwidth variation of less than $\pm 3.5\%$ over a temperature range of -40 °C to 85 °C and a supply voltage range of 0.9 to 1.2V.

Section 3 has proposed a harmonic-canceling sinewave synthesizer for analog BIST applications that uses a skew-circulant-matrix (SCM)-based coefficient generator. This coefficient generator generates irrational coefficients from integer numbers in a recursive approach with no calibration scheme, relaxing the trade-off between output linearity and coefficient mismatch. The selectable 24-tap, 12-tap, and 6-tap harmonic-canceling filters are implemented along with their band-pass versions. They cover a frequency range from 0.8MHz to 100MHz and provide the highest number of operation modes and the highest first non-

cancellable harmonic reported. Measured SFDR values prove the effectiveness of the proposed SCM-based coefficient generator architecture.

Section 4 extends the concept of harmonic-canceling sinewave synthesizer to implement an impedance analyzer for electrochemical impedance spectroscopy applications. We demonstrated and verified that the proposed impedance analyzer provides sub-GΩ impedance measurement with less than 1.2% error over the frequency range 0.01–100 kHz thanks to the proposed harmonic canceling scheme. The impedance analyzer system prototype was implemented in a 180 nm CMOS technology, the stimulus generator and the impedance read-out circuits consume 0.64 mW and 0.32 mW, respectively, from a 1.8 V supply.

5.2 Future Work

Future efforts to follow up on the research conducted in this dissertation are recommended as follows:

- In Section 2, future work can be done by investigating an improved control scheme for the oscillators. The purpose is to enhance the even-order distortion which was the bottleneck in the proposed linCCO-based integrator topology. The author would recommend using a fully differential control scheme for the two VCOs, such as the one used in [93], instead of the pseudo-differential control scheme that was used in Section 2.

- The work in Section 3 tackles the irrational tap coefficient of harmonic-canceling sinewave synthesizers in a systematic way. Future work may leverage the proposed technique along with dynamic-element matching (DEM) to drastically reduce random mismatches in the coefficient generator, which may result in a better SFDR [30]. Moreover, a better approximation for the normalizing gain of the closed-loop CG, that is discussed in Section 3.4.2, is advised which will enable achieving better SFDR with a fewer number of CG stages.

- The switched-capacitor based Sinc-filtering technique that was proposed in Section 4 may be utilized with the harmonic-canceling synthesizer of Section 3 to improve the achievable SFDR of the synthesizer. The additional Sinc-filtering stage could track the synthesizer's output frequency thanks to the switched-C implementation, which was discussed in Section 4.3, resulting in an improved SFDR over a wide frequency range. A possible implementation of such a system is illustrated in Fig. 5.1.

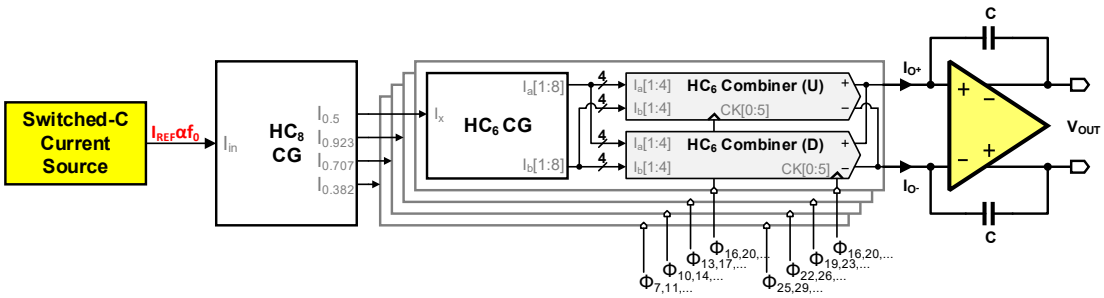


Figure 5.1: An improved 24-tap harmonic-canceling synthesizer topology as a cascade of a 6-tap HCF, an 8-tap HCF and an additional switched-C based filtering stage.

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APPENDIX A

NSPWM APERTURE DELAY DERIVATION

We start from the general expression of aperture delay in (2.13) [65]. For an M-phase RO-based filter, the NSPWM carrier harmonics are all suppressed except those at integer multiples of Mf_0. Therefore, for $T(s) = {}^{\omega_c}/_{s}$, (2.13) can be rewritten as a function of the PWM duty ratio $D = {}^{x+1}/_{2}$ as

$$t_d(D) = \frac{\omega_c}{\omega_0^2} \sum_{k=1}^{\infty} \frac{1 - \cos(2\pi k M D)}{k^2 M^2}, \tag{A.1}$$

Equation (A.1) represents a periodic function in D with period ${}^{1}/_{M}$. It was noted that $t_d(D)$ is the Fourier series expansion of the integral of a reverse sawtooth function with the same period. Hence, $t_d(D)$ is the biquadratic periodic function

$$t_d(D) = \pi^2 \frac{\omega_c}{\omega_0^2} \left[\frac{1}{4M^2} - \left(\left(D \bmod \frac{1}{M} \right) - \frac{1}{2M} \right)^2 \right], \tag{A.2}$$

where $\bmod$ is the modular division operator, i.e., $D \bmod \frac{1}{M} = D - \frac{m}{M}$, and m is the maximum integer that does not exceed $M \times D$, i.e., $m = \text{floor}\,(M \times D)$. Therefore, by direct substitution (A.2) reduces to (2.14).

APPENDIX B

ANALYSIS OF THE SKEW-CIRCULANT MATRIX-BASED HARMONIC CANCELING SYNTHESIZER

B.1 Eigenvalues of the Even-Order Skew-Circulant Matrix with Ideal HCF Coefficients

Consider the skew-circulant matrix, that represents the ideal harmonic-canceling and was described by (3.8), $\boldsymbol{A_i} = \text{scirc}(s_0, s_1, \ldots, s_{n-1})$, where $s_k = \cos(k\pi/n)$ for $k = 0, 1, \ldots, n-1$. Based on (3.10), the eigenvalues of a skew-circulant matrix are

$$\lambda_m = \sum_{k=0}^{n-1} s_k e^{\frac{j\pi k(1+2m)}{n}}, m = 0, 1, \ldots, n-1 \tag{B.1}$$

Then:

$$\lambda_m = \sum_{k=0}^{n-1} \cos\left(\frac{\pi k}{n}\right) e^{\frac{j\pi k(1+2m)}{n}} = \sum_{k=0}^{n-1} \left(\frac{e^{\frac{j\pi k}{n}} + e^{\frac{-j\pi k}{n}}}{2}\right) e^{\frac{j\pi k(1+2m)}{n}} \tag{B.2}$$

Closed-form solutions for the summations of the geometric sequences in (B.2) are given by:

$$\sum_{k=0}^{n-1} e^{\frac{j2\pi km}{n}} = \frac{1 - e^{j2\pi m}}{1 - e^{\frac{j2\pi m}{n}}} = \begin{cases} n & , m = 0, \pm n, \pm 2n, \ldots \\ 0 & , otherwise \end{cases} \tag{B.3}$$

$$\sum_{k=0}^{n-1} e^{\frac{j2\pi k(m+1)}{n}} = \frac{1 - e^{j2\pi(m+1)}}{1 - e^{\frac{j2\pi(m+1)}{n}}} = \begin{cases} n & , m = -1, \pm(n-1), \pm 2(n-1), \ldots \\ 0 & , otherwise \end{cases} \tag{B.4}$$

Therefore, for $m = 0, 1, \ldots, n-1$, the eigenvalues of the skew-circulant matrix $\boldsymbol{A_i}$ is expressed as:

$$\lambda_m = \begin{cases} \dfrac{n}{2} & , m = 0, n-1 \\ 0 & , otherwise \end{cases} \tag{B.5}$$

B.2 Eigenvalues of the Integer-Coefficient Skew-Circulant Matrix for an Even-Order HCF

Consider the integer-coefficient skew-circulant matrix described in section 3.3.3, $\boldsymbol{A} = \mathrm{scirc}(s'_0, s'_1, \ldots, s'_{n-1})$ such that $s'_k = \mathrm{sgn}\,(s_k)$, where $\mathrm{sgnsgn}\,(\cdot)$ is the sign function and $s_k = \cos(k\pi/n)$ for $k = 0, 1, \ldots, n-1$. According to (3.10), the eigenvalues of $\boldsymbol{A}$ are given by:

$$\begin{aligned} \lambda'_m &= \sum_{k=0}^{n-1} \mathrm{sgn}\left(\cos\left(\frac{\pi k}{n}\right)\right) e^{\frac{j\pi k(1+2m)}{n}} \\ &= \sum_{k=0}^{\frac{n}{2}-1} e^{\frac{j\pi k(1+2m)}{n}} - \sum_{k=\frac{n}{2}+1}^{n-1} e^{\frac{j\pi k(1+2m)}{n}}, m = 0, 1, \ldots, n-1 \end{aligned} \tag{B.6}$$

Eq. (B.6) can be simplified by using the sum of geometric sequence formula, or:

$$\begin{aligned} \lambda'_m &= \frac{1 - e^{\frac{j\pi(1+2m)}{n}\left(\frac{n}{2}\right)}}{1 - e^{\frac{j\pi(1+2m)}{n}}} - e^{\frac{j\pi(1+2m)}{n}\left(\frac{n}{2}+1\right)} \left[\frac{1 - e^{\frac{j\pi(1+2m)}{n}\left(\frac{n}{2}-1\right)}}{1 - e^{\frac{j\pi(1+2m)}{n}}}\right] \\ &= \frac{1 - e^{\frac{j\pi(1+2m)}{2}} - e^{\frac{j\pi(1+2m)}{n}\left(\frac{n}{2}+1\right)} + e^{j\pi(1+2m)}}{1 - e^{\frac{j\pi(1+2m)}{n}}} \\ &= e^{\frac{j\pi(1+2m)}{2}} \left[\frac{e^{\frac{j\pi(1+2m)}{n}} + 1}{e^{\frac{j\pi(1+2m)}{n}} - 1}\right] \end{aligned} \tag{B.7}$$

Therefore,

$$\lambda'_m = (-1)^m \cot\left(\frac{\pi\,(1+2m)}{n}\right), m = 0, 1, \ldots, n-1 \tag{B.8}$$

B.3 Equivalence between a Cascade of Lower Order Harmonic Canceling Filters and a Higher Order Harmonic Canceling Filter

We start from (3.19) that describes a system of cascaded harmonic-canceling filters of order n_1 and n_2, respectively. It is noted that $A_{n_1\times n_1} \otimes I_{n/n_1}$ is also a skew-circulant matrix with a first row equal to the first row of $A_{n_1\times n_1}$ upsampled by n/n_1 , and similarly for $A_{n_2\times n_2} \otimes I_{n/n_2}$. The Eigenvalues of these matrices are given by (Appendix B.1)

$$\begin{aligned} \lambda[A_{n_1\times n_1} \otimes I_{n/n_1}] &= \{\lambda_0, \lambda_1, \ldots, \lambda_{n-1}\} \\ \lambda[A_{n_2\times n_2} \otimes I_{n/n_2}] &= \{\mu_0, \mu_1, \ldots, \mu_{n-1}\} \end{aligned}, \tag{B.9}$$

where

$$\lambda_m = \begin{cases} \frac{n_1}{2} & \text{, if } m \in S_{11} \qquad\quad \text{, } S_{11} = \left\{kn_1 : k \in \mathbb{Z}, 0 \le k \le \frac{n}{n_1} - 1\right\} \\ \frac{n_1}{2} & \text{, if } m \in S_{12} \quad \text{, } S_{12} = \left\{kn_1 + (n_1 - 1) : k \in \mathbb{Z}, 0 \le k \le \frac{n}{n_1} - 1\right\} \\ 0 & \text{, otherwise} \end{cases}$$

$$\mu_m = \begin{cases} \frac{n_2}{2} & \text{, if } m \in S_{21} \qquad\quad \text{, } S_{21} = \left\{kn_2 : k \in \mathbb{Z}, 0 \le k \le \frac{n}{n_2} - 1\right\} \\ \frac{n_2}{2} & \text{, if } m \in S_{22} \quad \text{, } S_{22} = \left\{kn_2 + (n_2 - 1) : k \in \mathbb{Z}, 0 \le k \le \frac{n}{n_2} - 1\right\} \\ 0 & \text{, otherwise} \end{cases}, \tag{B.10}$$

The product of these two skew-circulant matrices of the same size is also skew-circulant matrix, and they all have the same Eigenvectors. Therefore, the Eigenvalues of the product is $\{\lambda_0\mu_0, \lambda_1\mu_1, \ldots, \lambda_{n-1}\mu_{n-1}\}$, where

$$\lambda_m \mu_m = \begin{cases} \frac{n_1 n_2}{4} & \text{, if } m \in S_{11} \bigcap S_{21} \\ \frac{n_1 n_2}{4} & \text{, if } m \in S_{12} \bigcap S_{22} \\ \frac{n_1 n_2}{4} & \text{, if } m \in S_{11} \bigcap S_{22} \\ \frac{n_1 n_2}{4} & \text{, if } m \in S_{12} \bigcap S_{21} \\ 0 & \text{, } otherwise \end{cases}, \tag{B.11}$$

It can be shown that $S_{11} \bigcap S_{21} = \{0\}$ and $S_{12} \bigcap S_{22} = \{n-1\}$, while $S_{11} \bigcap S_{22} = S_{12} \bigcap S_{21} = \varnothing$ if and only if $\gcd(n_1, n_2) > 1$. That is:

$$\lambda \left[\left(A_{n_2 \times n_2} \otimes I_{n/n_2} \right) \left(A_{n_1 \times n_1} \otimes I_{n/n_1} \right) \right] = \begin{cases} \frac{n_1 n_2}{4} & \text{, if } m = 0, n-1 \\ 0 & \text{, } otherwise \end{cases}, \tag{B.12}$$

where

$$n = \operatorname{lcm}(n_1, n_2) \text{ and } \gcd(n_1, n_2) > 1, \tag{B.13}$$

It is observed that a skew-circulant matrix with that set of eigenvalues is simply a scaled version of $A_{n \times n}$, therefore:

$$A_n = \frac{2n}{n_1 n_2} \left(A_{n_2 \times n_2} \otimes I_{n/n_2} \right) \left(A_{n_1 \times n_1} \otimes I_{n/n_1} \right), \tag{B.14}$$