DEEP REACTIVE-ION ETCHING PROCESS DEVELOPMENT AND MASK SELECTION

An Undergraduate Research Scholars Thesis

by

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ABSTRACT

Deep Reactive-Ion Etching Process Development and Mask Selection

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Deep reactive-ion etching is an important process in the fabrication of microelectromechanical system devices, through-silicon vias, and dynamic random-access memory capacitors, among other devices and components. High-quality etching is a crucial step in device fabrication, where the etch quality is determined by three properties: aspect ratio (ratio of depth of etched feature to width of etched feature), selectivity (ratio of desired material's etch rate to etch mask material's etch rate), and sidewall profile (angle relative to feature bottom and sidewall roughness).

A cryogenic-temperature deep reactive-ion etching process is developed to obtain 90°, smooth sidewalls and maximize the selectivity and aspect ratio through the optimization of oxygen gas flow rate, radio frequency power, and inductively-coupled plasma power on a (111) silicon substrate. The aspect-ratio-dependent etching effect and its impact on etch rate is also examined.

Additionally, etch mask behaviors of selectivity and tendency to crack are characterized for 100 nm electron-beam evaporated chromium, 500 nm thermally-grown silicon dioxide, and 1.45 µm post-develop-baked AZ 5214 E-IR photoresist.

The experimental results provide insight on how to adjust the etching process according to the specific device application and which material and film thickness is best to use as an etch mask.

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Finally, thanks to my mother and father for their unconditional support of my education.

NOMENCLATURE

Al	Aluminum
ARDE	Aspect-ratio-dependent etching
BOE	Buffered oxide etchant
Cr	Chromium
C_4F_8	Octofluorocyclobutane
DI	Deionized
DRIE	Deep reactive-ion etching
EBE	Electron-beam evaporation
F	Fluorine
HF	Hydrofluoric acid
H_2O	Water
H_2O_2	Hydrogen peroxide
H_2SO_4	Sulfuric acid
ICP	Inductively-coupled plasma
ICPP	Inductively-coupled plasma power
IPA	Isopropyl alcohol
MIF	Metal ion free
NH_4F	Ammonium fluoride
O_2	Oxygen
PVD	Physical vapor deposition
RF	Radio frequency

RFP	Radio frequency power
RIE	Reactive-ion etching
RPM	Revolutions per minute
SEM	Scanning electron microscope
SF_6	Sulfur hexafluoride
Si	Silicon
SiF_4	Silicone tetrafluoride
SiO_xF_y	Silicon oxyfluoride
SiO_2	Silicon dioxide
Si_3N_4	Silicon nitride

CHAPTER I

INTRODUCTION

Wet and Dry Etching

Etching is the process by which specific areas of a substrate are removed through physical bombardment, chemical reactions, or both. The areas that are not removed are protected by a film referred to as the etch mask, which is formed using the photolithography process. Common etch mask materials include silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and metals, such as aluminum (Al) or chromium (Cr). Poor etch masks will break down and cause undesired areas to be etched, ruining the sidewall profile and aspect ratio.

Wet etching uses chemicals to remove the specific areas. Common wet etchants are hydrofluoric acid (HF) and nitric acid (HNO_3) (combined to form silicon (Si) etchant) and HF and ammonium fluoride (NH_4F) (combined to form SiO_2 etchant). Chemical reactions between the etchant and substrate create soluble byproducts that are then removed (etched). Wet etching is generally highly selective and isotropic, that is etching occurs evenly in all directions.

Dry etching has two primary variations: plasma etching and reactive-ion etching (RIE). Both variations occur at low pressures and tend to have vertically-anisotropic profiles, i.e. etching occurs significantly more in the vertical direction. Plasma etching uses ions from a plasma to physically bombard the substrate. By applying a bias to the plasma using a 13.56 MHz radio frequency (RF) electromagnetic field, ions are accelerated towards the substrate, which etches the exposed regions. The resulting fragments are removed via the vacuum pump connected to the chamber in which the process is occurring. Reactive-ion etching also uses ion bombardment, but has the added effect of radical-substrate reactions. When a radical (an atom,

molecule, or ion with at least one unpaired valence electron) bonds with the substrate, a reaction occurs, forming a compound. For example, the monatomic fluorine (F) radical and silicon (Si) react to form silicon tetrafluoride, SiF_4. Assuming both the process chamber pressure and temperature are low enough, the SiF_4 will be volatile upon formation and is easily removed by the vacuum pump. Some RIE systems include a 13.56 MHz inductively-coupled plasma (ICP) source, which increases plasma density (number of ions present in the plasma). However, ICP RIE decreases the vertical anisotropy due to more radical-substrate reactions taking place, which occur in both the horizontal and vertical direction [1].

Etching Characteristics

Important characteristics of etching include selectivity, aspect ratio, sidewall profile, and etch rate.

Selectivity is the ratio of the substrate etch rate to the mask etch rate. If selectivity is low, the etch mask can be completely etched, exposing the originally-protected regions of the substrate to the plasma. RIE generally has high selectivity due to the chemical reactions performing a majority of the etching. In regards to etching Si, metal and non-Si-based dielectric etch masks have much higher selectivity due to there being no chemical reactions between the material and the plasma's radicals. Si-based dielectrics (SiO_2, Si_3N_4) and organic materials (photoresist) generally exhibit moderate and poor selectivity, respectively.

Aspect ratio is the ratio of the etch depth to width. High aspect ratio structures are created using a specific type of RIE, called deep reactive-ion etching (DRIE), and are used in through-silicon vias (TSV) [2] and sensor technologies [3].

Sidewall profile of the etch includes the feature sidewall and bottom roughness and angle of the sidewall relative to the bottom. Applications such as optical waveguides and microfluidics

rely on smooth sidewalls to prevent optical losses [4] or flow obstruction [5]. Black Si is the formation of Si micropillars on the feature bottom. It is commonly used in the photovoltaics industry for solar cells due to its high absorption and low reflectivity of light, which creates high-efficiency cells [6]. The micropillars are created through the resputtering of the etch product and the condensation of silicon oxyfluoride (SiO_xF_y) films that serve as micromasks on the feature's bottom [7].

Etch rate is the speed at which the substrate is etched and increases with ICP power (ICPP), RF power (RFP), and etch gas flow rates. Larger ICP powers and gas flow rates generate more radicals, causing more numerous radical-substrate chemical reactions. Larger RF powers accelerate ions towards the substrate with more force and cause a large number of substrate atoms to be removed per single ion.

Deep Reactive-Ion Etching

There are two variations of DRIE: the Bosch process and cryogenic DRIE. The Bosch process is composed of two steps that repeat over many cycles, depending on etch depth. The first step is a standard reactive-ion etch. The second step is the deposition of an inert passivation layer on the recently-etched trench's sidewalls and bottom. Octafluorocyclobutane (C_4F_8) gas is generally used to form the passivation layer [8] [9]. After the passivation layer deposition is complete, the reactive-ion etch is repeated. The bombardment of the ions etches the trench bottom's passivation layer, but not the sidewall layers. This exposes the underlying substrate and allows for deeper vertical etching to occur with minimal horizontal etching. Each step lasts only a few seconds. Longer steps allow higher etch rates due to more protection, while shorter steps result in smoother sidewalls, due there being less time for isotropic etching to take place.

Cryogenic DRIE cools the process chamber and sample down to -100 °C or below, which slows the chemical etch rate according to the Arrhenius Equation [10] and allows ion bombardment to etch vertically. If both sulfur hexafluoride (SF_6) and oxygen (O_2) are used as the etching gases when etching Si, a SiO_xF_y passivation layer can form via condensation [11], allowing cryogenic DRIE to act similarly to the Bosch process's passivation step, without the need for an independent deposition step. The cryogenic temperature can cause cracking of etch masks, especially photoresists, so metal etch masks are generally used for cryogenic DRIE.

Using the Bosch process with SF_6 as the etching gas and C_4F_8 as the passivation layer, an aspect ratio of 107 (0.374 μm wide and 40.1 μm deep) has been achieved at 20 °C [12]. The sidewall angle is controllable as a function of the percent of O_2 in the total gas flow [13]. Cryogenic etching has achieved Si:SiO_2 selectivity of 150:1 and Al_2O_3 selectivity of 66000:1 [14] and aspect ratio of over 47 [15].

CHAPTER II

METHODS

Photomask Design

A dark-field photomask (Table 1) was designed to create 6000 µm long DRIE arrays (Figure 1) for characterization. The arrays are of variable width and spacing. Beginning with five lines each of width W, feature width is kept constant while spacing between features varies between 3W, 2W, and 1W, resulting in three 5x1 line arrays for each width, or 30 total arrays, each with 50 µm between them. Array feature widths are 10 µm, 9 µm, 8 µm, 7 µm, 6 µm, 5 µm, 4 µm, 3 µm, 2 µm, and 1 µm. All features were combined into a single "unit" square, then made into a truncated array of 3-5-5-5-3 unit squares across the mask (Figure 2), allowing five unit squares to fit on a single 2 in. Si wafer.

Table 1. Photomask characteristics

Parameter	Value
Dimensions	5x5x0.090 in.
Substrate materials	2 µm flat amorphous fused-silica (quartz)
Mask material	Chromium
Critical dimension	1 µm (DRIE feature)
Manufacturing grid	25 nm
Fabrication method	Direct laser write

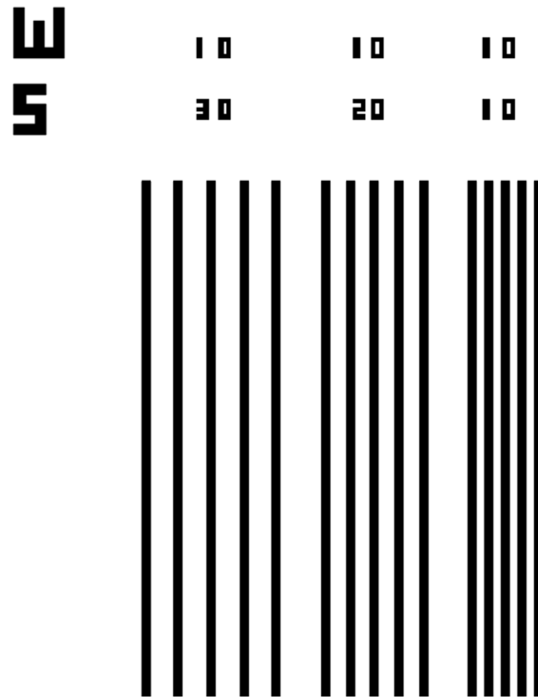

Figure 1. DRIE arrays with 10 µm feature width and 30 µm, 20 µm, 10 µm spacing

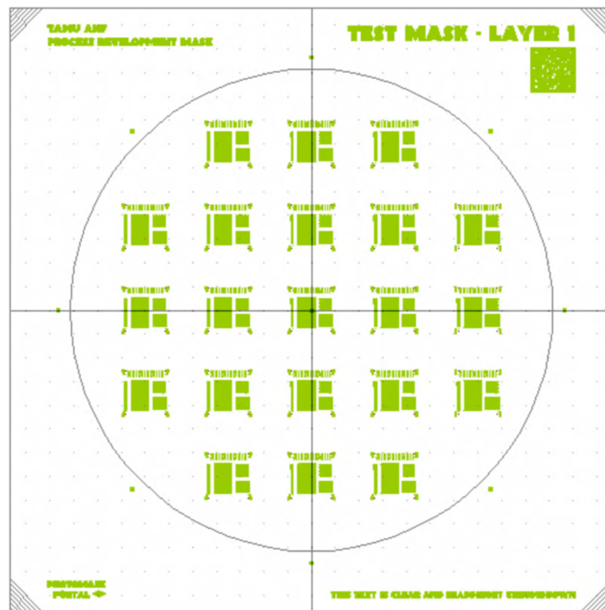

Figure 2. Photomask layout with 3-5-5-5-3 truncated array of unit squares

Aspect-ratio-dependent etching (ARDE) can be observed from the arrays by comparing the etch rate of a larger feature to a smaller feature. In ARDE, the etch rate decreases with feature size due to lack of etching species delivery capabilities [16].

Substrate Preparation

Substrates used were single-side polished silicon (Si) wafers (Table 2) with a single primary flat.

Table 2. Substrate characteristics

Parameter	**Value**
Diameter	50.8 mm
Orientation	(111)
Thickness	279 ± 20 µm
Doping	n-type (P)
Resistivity	1-5 Ω-cm

Pre-Deposition

Wafers were cleaned for 10:00 min using three parts 96% sulfuric acid (H_2SO_4) and one part 30% hydrogen peroxide (H_2O_2) piranha solution followed by a 10:00 min warm (hot plate set at 200 °C) deionized (DI) water bath rinse, a 5:00 min room-temperature DI water bath rinse, and N_2 drying. The piranha solution clean ensures a clean Si-Cr/Si-SiO_2/Si-photoresist interface and allows better adhesion between the film and wafer.

To minimize contamination and native oxidation after cleaning, wafers were taken directly to the electron-beam evaporation system for Cr deposition, the oxidation furnaces for SiO_2 growth, or to pre-photolithography cleaning.

Pre-Photolithography

Wafers were cleaned using 99.5% acetone, 99.5% isopropyl alcohol, DI water, then dried using N_2. After N_2 drying, wafers were placed into a 90 °C oven for 10:00 min to evaporate any residual solvents remaining on the wafer. Wafers were then passively cooled for 10:00 min at room temperature.

Thin-Film Deposition

Electron-beam Evaporation (EBE)

100 nm 99.95% Cr was deposited using a Kurt J. Lesker PVD 75 Electron-Beam Evaporation system (Table 3). The wafer was placed in the middle of the substrate holder and rotated at 20 revolutions per minute (RPM) during deposition to promote film thickness uniformity across the wafer.

Table 3. Cr EBE characteristics

Parameter	Value
Deposition pressure	5×10^{-6} Torr
Deposition rate	0.1 nm/s
Accelerating voltage	10 kV
Crystal thickness monitor life	>90%
Substrate rotation speed	20 RPM

Thermal Oxidation

500 nm SiO_2 was grown using a Minibrute oxidation furnace and steam. A bubbler was filled with DI water and turned on for 1:00 hour prior to the oxidation to ensure an adequate amount of steam was being generated. The quartz tube was heated to 1100 °C while 99.999%-

pure N_2 was flowing throughout. Wafers were loaded onto a quartz boat with all wafer flats aligned on top. A single guard wafer was placed at either end to ensure the process wafers experienced the same steam conditions. The boat was loaded into the front of the 1100 °C tube for 5:00 min to allow heat acclimation and prevent thermal shock. After 5:00 min, the boat was pushed into the center of the tube. The N_2 supply was turned off and the bubbler connected to the tube, allowing steam to flow in. The tube cap was placed back on.

The total growth time of 500 nm steam-based (wet) SiO_2 on (111) Si at 1100 °C is 34:29 min. After this time was finished, the bubbler was disconnected and N_2 turned back on to prevent further oxide from growing. The boat was slowly pulled out and left to cool at room temperature for 15:00 min.

Cr thicknesses were measured after the Cr mask patterning using a Bruker DektakXT profilometer. SiO_2 thicknesses were measured directly after the growth using an Ocean Optics NanoCalc spectrometer. A step height standard with thermally-grown SiO_2 was used to calibrate the measurement, then the samples themselves were measured.

Photolithography

After the pre-photolithography cleaning procedure, AZ 5214 E-IR positive photoresist was immediately applied to the wafer using a BIDTEC SP100 Spin Coater. The experimentally-determined spin coat recipe (Table 4) results in 1.45-1.48 µm of resist and was verified using a Bruker DektakXT profilometer. The wafer was soft-baked at 120 °C for 2:00 min on a hot plate. An EVG 610 Double-Sided Mask Aligner with 365 nm (i-line) UV light was used to expose the photoresist. Soft contact between the wafer and mask was used during the exposure. The UV light source's intensity profile was measured with an OAI Model 308 UV Light Meter with 365 nm probe before each exposure to ensure proper dosage was applied.

Table 4. Spin coat recipe

Parameter	Value
Speed 1	500 rpm
Time from 0 rpm to Speed 1	10 s
Time at Speed 1	10 s
Speed 2	4000 rpm
Time from Speed 1 to Speed 2	5 s
Time at Speed 2	40 s
Time from Speed 2 to 0 rpm	3 s

AZ® 726 metal-ion free (MIF) developer was used for developing the exposed regions of photoresist. Development time averaged 35 s and was followed by two separate room temperature DI water baths and N_2 drying. The photoresist was inspected using a Nikon Eclipse LV150N optical microscope to check for development quality and completeness. If the photoresist was underdeveloped, the wafer was placed back into the AZ® 726 MIF for 1-5 seconds, then rinsed in the DI water baths. If the photoresist was overdeveloped, the photoresist was removed using 85 °C AZ® 400T Photoresist Stripper and the entire photolithography process, including the pre-cleaning, started over.

After development, the wafer was placed into an oven at 135 °C for 10:00 min for post-develop baking, making it resistant to the etchant used for the etch mask patterning. When the post-develop baking finished, the wafers were passively cooled for 10:00 min at room temperature.

After post-develop baking the AZ 5124 E-IR thickness was measured using a Bruker DektakXT profilometer.

Etch Mask Patterning

In order to expose the Si underneath the etch mask material, the etch mask itself must be etched completely down to the mask-Si interface using an etchant entering through the developed regions of photoresist.

To etch Cr, Alfa Aesar® Cr etchant (79 parts H_2O, 16 parts cerium (IV) ammonium nitrate, 5 parts nitric acid) was placed on a 60 °C hot plate for 5:00 min. The wafer was submerged into the Cr etchant for 35 s to ensure all the Cr covering Si was removing. The wafer was then immediately rinsed in two consecutive room temperature DI water baths and dried using N_2.

To etch SiO_2, the wafer was submerged into J.T. Baker® buffered oxide etchant (BOE) (7 parts 6% hydrofluoric acid (HF), 1 part ammonium fluoride (NH_4F)) for 7:30 min. An overetch factor of 20% was included in the etch time to ensure no SiO_2 remained over Si regions. The wafer was then immediately rinsed in two consecutive room temperature DI water baths and dried using N_2.

To remove the remaining photoresist, AZ® 400T Photoresist Stripper was placed onto a 150 °C hot plate for 10:00 min. The wafer was then submerged in solution for 15:00 min and agitated throughout.

Wafer Dicing

The wafer was diced into five individual samples using a Micro Automation M1100 Dicing Saw with a 0.008 ± 0.0003 in. wide diamond blade at a cut speed of 2.0 mm/s and spindle speed of 24000 rpm. The mechanical damage caused by the dicing is irrelevant because the

DRIE features are in the middle of the die and not cut by the blade. DI water cooling was applied during dicing to ensure the wafer did not overheat and remove the slurry created by the cutting process.

Deep Reactive-Ion Etching

All etching was performed using an Oxford Instruments Plasmalab 100 ICP-RIE system. The tool is outfitted specifically for 100 mm wafers, so a “carrier” wafer must be used when etching samples smaller than 100 mm. Because the DRIE process etches Si, 500 nm Al was deposited using electron-beam evaporation onto a bare 100 mm Si wafer to serve as the carrier wafer. Al is not etched by SF_6 or O_2, so it will not be affected by the plasma and can be used over many etching processes without breaking. To improve the thermal conduction between the sample and carrier wafer, COOL-GREASE ZXM, a zinc oxide-filled thermally conductive grease with approximate thermal conductivity of 20 ± 10% W/m-°C, was used. A thin layer was applied to the sample’s backside before being placed onto the carrier wafer. A single piece of Kapton® tape was applied to either side of the sample to adhere it securely and flush to the carrier wafer.

A 15:00 min O_2-based plasma chamber clean (Table 5) was performed prior to etching to remove possible contaminants from the process chamber.

Table 5. O_2 plasma chamber clean recipe parameters

Parameter	**Value**
Pressure (mTorr)	20
ICP power (W)	1000
RF power (W)	100
O_2 gas flow rate (SCCM)	60
Chamber temperature (°C)	25
Helium backside cooling pressure (mTorr)	0
Helium backside cooling gas flow rate (SCCM)	0

The process chamber's temperature was decreased to -100 °C using liquid nitrogen. The Al carrier wafer with attached die was finally placed into the process chamber to begin the etching process.

All recipes (Table 6) began by decreasing the process chamber's pressure to 0.1 mTorr (minimum reading of pressure gauge) for 1:00 min to minimize possible chamber contaminants. The next step began flowing 60 SCCM O_2 for 30 s at a chamber pressure of 30 mTorr, then striking and stabilizing an O_2-based plasma for 10 s. The SF_6 flow rate was progressively increased from 0 SCCM while the O_2 gas flow rate progressively decreased until each gas's flow rates were at their final values. Each step was held for 5 s to allow the plasma to stabilize. ICPP, backside He cooling, and chamber temperature remained constant throughout the entire recipe. RFP and chamber pressure both progressively decreased with each step until their final values. An automated impedance matching unit minimized reflected power on both the RF and ICP generators. The Cr etch experiments were performed for 20:00 min, the SiO_2 for 3:00 min, and

AZ 5214 E-IR for 2:00 min. The SiO_2 and AZ 5214 E-IR experiments were performed for a shorter time than Cr to ensure there was still a thin film left to measure for selectivity.

Table 6. Example recipe steps

Step	Pressure (mTorr)	RFP (W)	SF_6 Flow (SCCM)	O_2 Flow (SCCM)
1	30	0	0	60
2	30	100	0	60
3	27	85	1	55
4	24	70	5	50
5	21	55	10	45
6	18	40	20	40
7	15	30	40	35
8	15	20	90	30

Three parameters and their effects on the final etch result were examined: ICPP, RFP, and O_2 gas flow rate (Table 7). All other variables were held constant (Table 8).

Table 7. Variable parameters and values

Parameter	Value
ICPP (W)	600/800/1000/1200
RFP (W)	10/20/40
O_2 gas flow rate (SCCM)	20/30/40

Table 8. Constant parameters and values

Parameter	Value
Chamber temperature (°C)	-100
Chamber pressure (mTorr)	15
Helium backside cooling pressure (mTorr)	10
Helium backside cooling gas flow rate (SCCM)	38
SF_6 gas flow rate (SCCM)	90

Characterization

Scanning Electron Microscopy

In order to view the cross-section of the sample, the sample was cleaved using a Ted-Pella® diamond scribe.

The cleaved sample was adhered to carbon tape and mounted on a stage such that the features were perpendicular to the electron beam's column. The stage was then placed into the scanning electron microscope (SEM) chamber and the chamber vacuumed down to 9×10^{-2} Pa. The stage was rotated and tilted to view the features upright and directly, respectively.

A TESCAN MIRA3 SEM with secondary electron detector was used for analysis. Accelerating voltage varied between 10-30 kV and beam emission current was 280 μA. Working distance varied between 7-16 mm. Gun pressure was 10^{-8} Pa, column pressure was less than 5×10^{-3} Pa, and chamber pressure was 9×10^{-2} Pa. Chamber degaussing was performed prior to each image to improve resolution and ensure accurate measurements. Stigmation and beam wobble were adjusted during imaging to improve resolution.

Feature depth, feature width, sidewall angle, and remaining Cr and AZ 5214 E-IR etch mask thicknesses were all measured using TESCAN's built-in software measurement tools for distances and angles.

Spectrometry

An Ocean Optics NanoCalc spectrometer was used to measure the remaining thickness of SiO_2 after etching. A step height standard with thermally-grown SiO_2 was used to calibrate the tool, then the etched samples were placed underneath to be measured.

CHAPTER III

RESULTS

Thin-Film Deposition

Cr, SiO_2, and AZ 5214 E-IR Thicknesses

The average etch mask thicknesses (Table 9) were calculated for each material. The refractive index of the SiO_2 was found to be 1.4571, compared to an ideal value of $n_{SiO2} = 1.4585$ [17].

Table 9. Average etch mask thicknesses

Material	Average Thickness (nm)
Cr	101.52
SiO_2	578.2
AZ 5214 E-IR	1482

The Cr etch time remained constant at 35 s, but the SiO_2 BOE etch time was increased to 9:00 min to accommodate for the additional oxide thickness. The additional oxide thickness can be attributed to poorly-calibrated thermocouples and extra growth from residual steam after the bubbler connection to the tube was removed.

Aspect Ratio

Effect of RF Power on Aspect Ratio

Increasing RFP increases vertical physical etching due to stronger ion bombardments. Because the electrodes are set up parallel to the sample (the positive electrode is closest to the sample), whenever the RF field pulses, both the F^- and O^{2-} ions are accelerated orthogonally

towards the sample/positive electrode, etching primarily in the vertical direction. Horizontal etching can occur if the ion is deflected and collides with the sidewall.

Because plasmas contain species with such high energies, plasma temperatures are much greater than -100 °C [18], the chamber temperature used in these experiments. Increasing RF power then substantially increases sample temperature due to higher energy collisions, especially at the surface, where the plasma is concentrated. This temperature increase is minimized to an extent through the use of the thermal grease, helium backside cooling, and low chamber temperature, but will ultimately increase horizontal etching, worsening the aspect ratio. In extreme cases, the individual array features can merge together, resulting in one large trench (Figure 3).

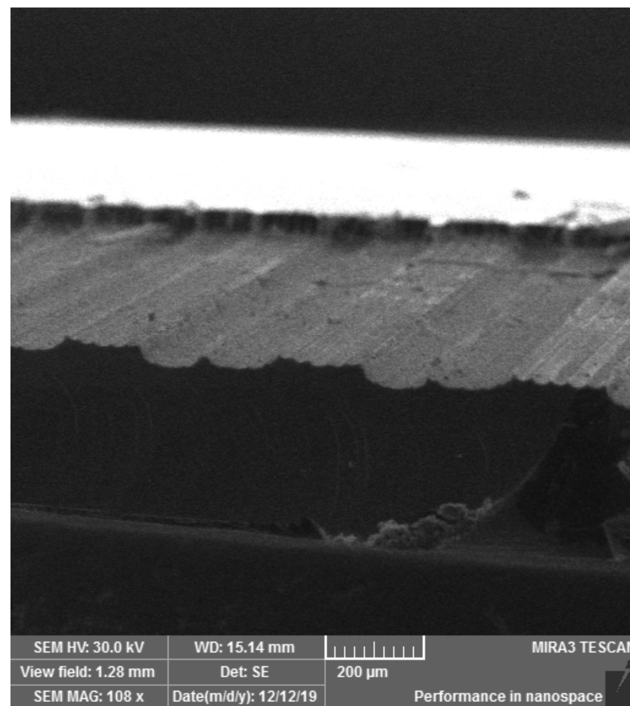

Figure 3. Array feature merging due to high temperature

Aspect ratio was found to increase with RFP (Figure 4) due to a larger vertical etch rate.

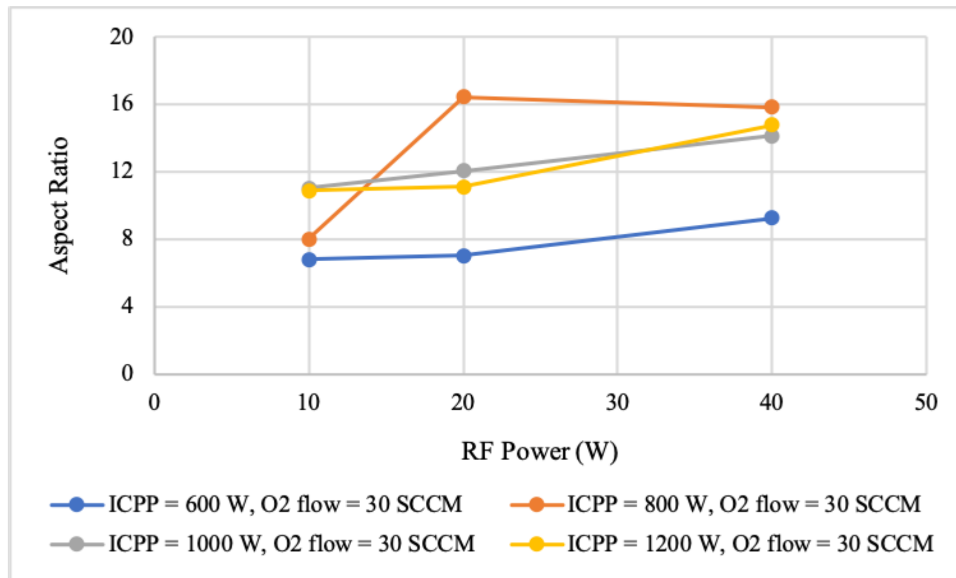

Figure 4. Aspect ratio vs. RFP

Effect of ICP Power on Aspect Ratio

Because ICPP increases the concentration of etchant species within the plasma, as the plasma engulfs the sample, more F radicals react with the Si on both the feature's sidewalls and bottom. This decreases the aspect ratio due to the increased horizontal etching rate on both sidewalls.

It was found that the aspect ratio as a function of ICPP follows an inverse parabolic trend (Figure 5). At a certain concentration, the vertical etch rate saturates, causing excess F radicals to move away from the feature bottom and towards the sidewalls. This increases the horizontal etching rate, decreasing aspect ratio.

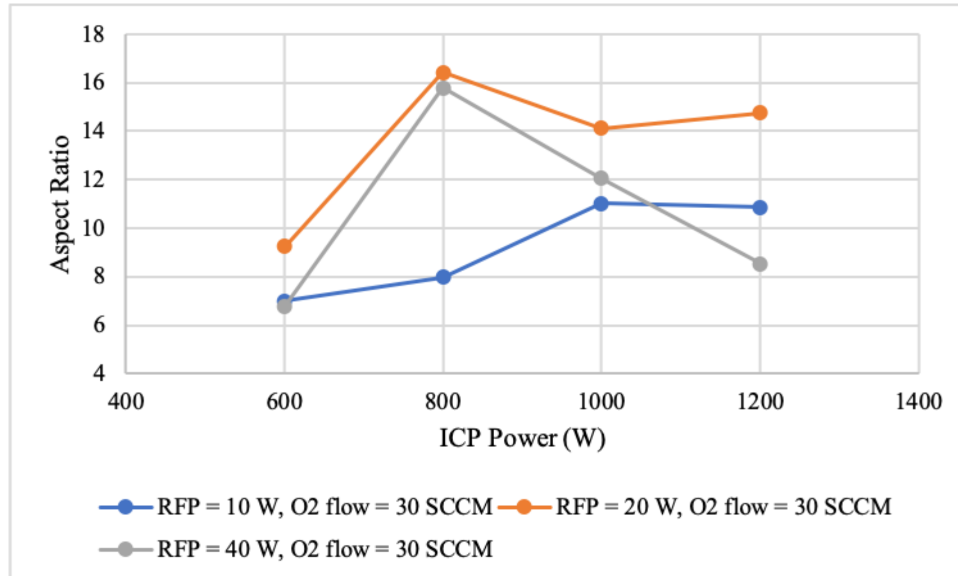

Figure 5. Aspect ratio vs ICPP

Effect of O_2 Gas Flow Rate on Aspect Ratio

O_2 condenses with both Si and F atoms to form an inert, non-continuous passivation layer of SiO_xF_y on the feature sidewalls and bottom. This phenomenon is similar to the Bosch process, but without the continuity of the passivation layer. Using RFP, the bottom layer will be etched significantly faster than the sidewalls due to ion bombardment, allowing for deep vertical etching and minimal horizontal etching while the sidewalls are protected. However, too much O_2 flow creates two issues. First, O_2 within the plasma impedes the delivery of F radicals to the feature bottom, decreasing the vertical etch rate while maintaining the horizontal etch rate near the top of the feature, decreasing the aspect ratio. Second, excess O_2 forms a thick passivation layer throughout the feature, further restricting the flow of F radicals to the trench bottom.

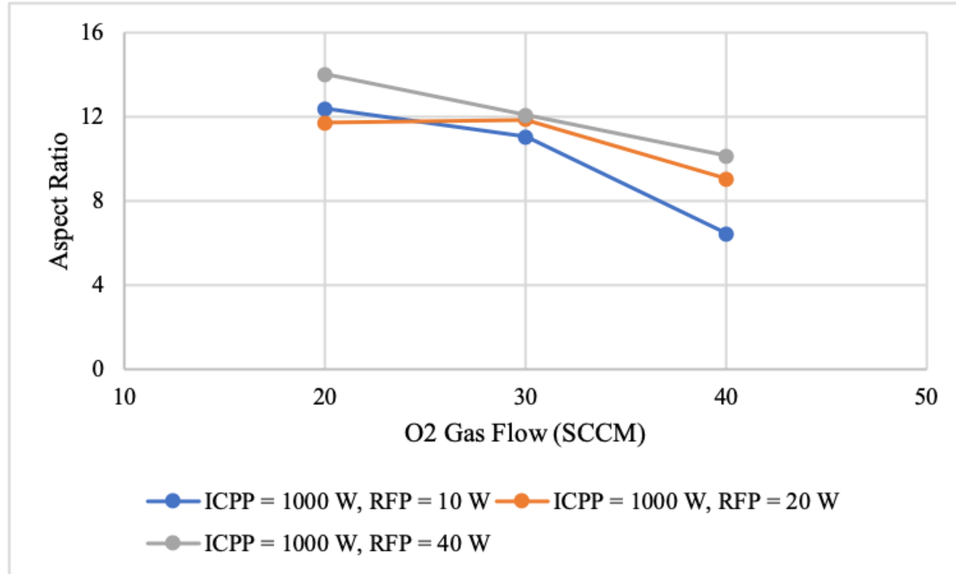

Figure 6. Aspect ratio vs. O_2 gas flow rate

Aspect-Ratio-Dependent Etching

Aspect-ratio-dependent etching (ARDE) can be seen by the difference in etch rates and aspect ratios between the three feature arrays examined after etching. Across all recipe combinations for all mask materials, the etch rate of array one was significantly higher than for array two and three (Figure 7). F radical delivery to the feature bottom is much more likely when the feature opening is larger.

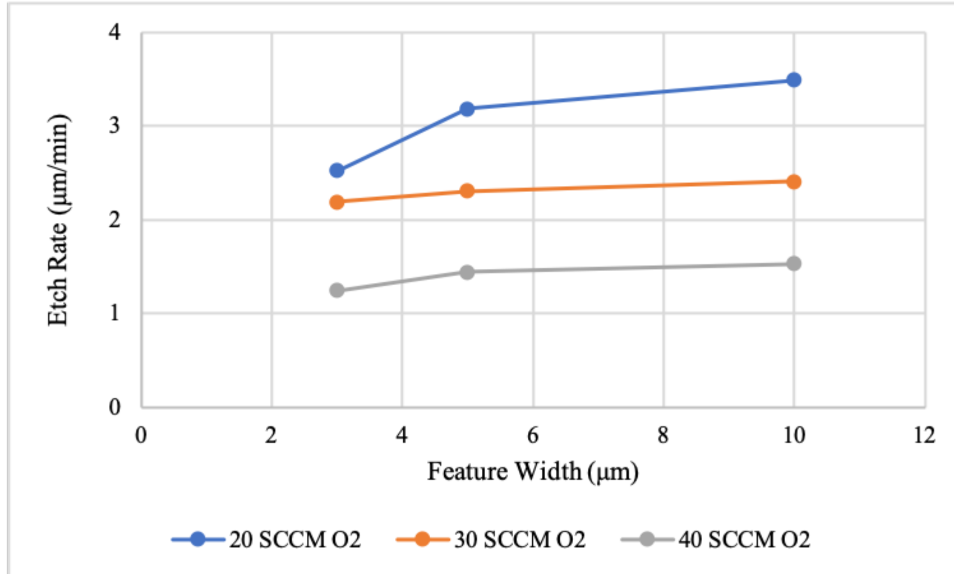

Figure 7. Etch rate as a function of feature width with ICPP = 1000 W, RFP = 10 W

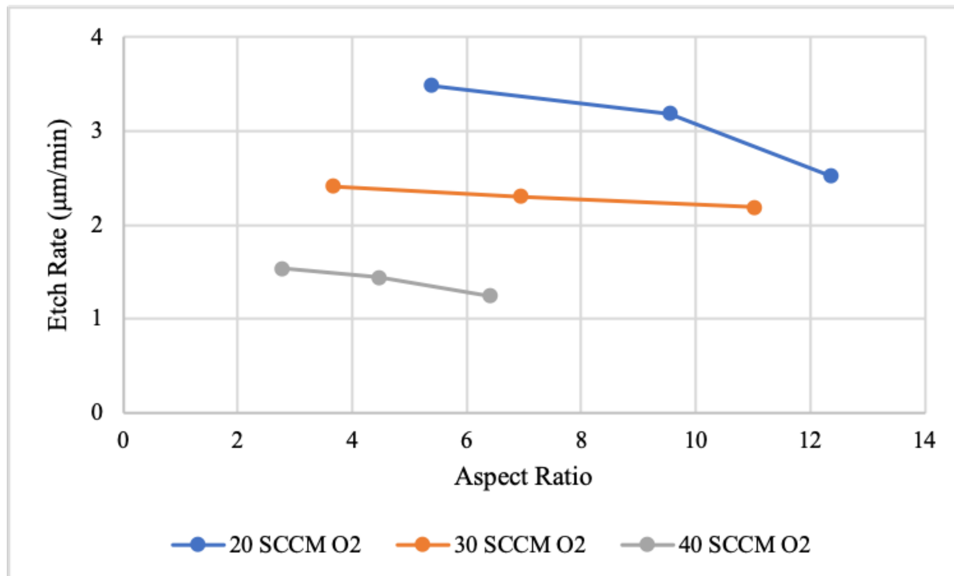

Figure 8. Etch rate as function of array three aspect ratios with ICPP = 1000 W, RFP = 10 W

Selectivity

Effect of RF Power on Selectivity

Etch mask selectivity decreases with RFP for all materials (Figure 9). As RFP increases, both the F^- and O^{2-} ion bombardment strength increases, etching both the mask and substrate faster. As etch depth increases, ions and radicals are less likely to reach the bottom, decreasing the substrate etch rate over time. The ions remain constantly etching the mask on the substrate's surface, maintaining the mask etch rate.

Heat also contributes to the selectivity. Because most of the RFP-generated heat is above the substrate or at its surface, the top of the sample will have a higher temperature then the bottom of the feature, causing that area's etch rate (which includes the mask, but not the feature bottom) to increase.

Surprisingly, the AZ 5214 E-IR did not crack throughout the process. Cracking has been shown to occur when He backside cooling is applied [14]. The ion bombardment strength was expected to damage the resist, but evidently did not (Figure 10).

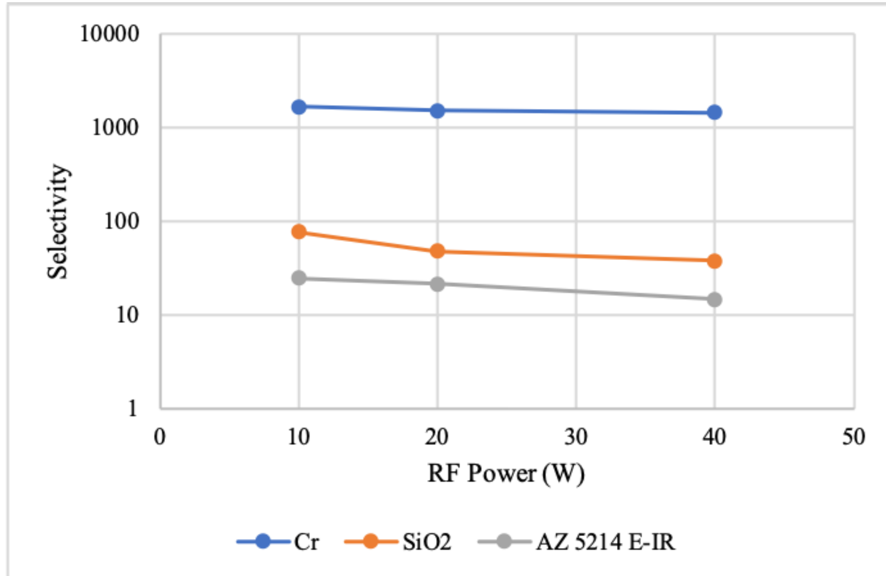

Figure 9. Selectivity vs. RFP with ICPP = 1000 W, O_2 gas flow rate = 30 SCCM

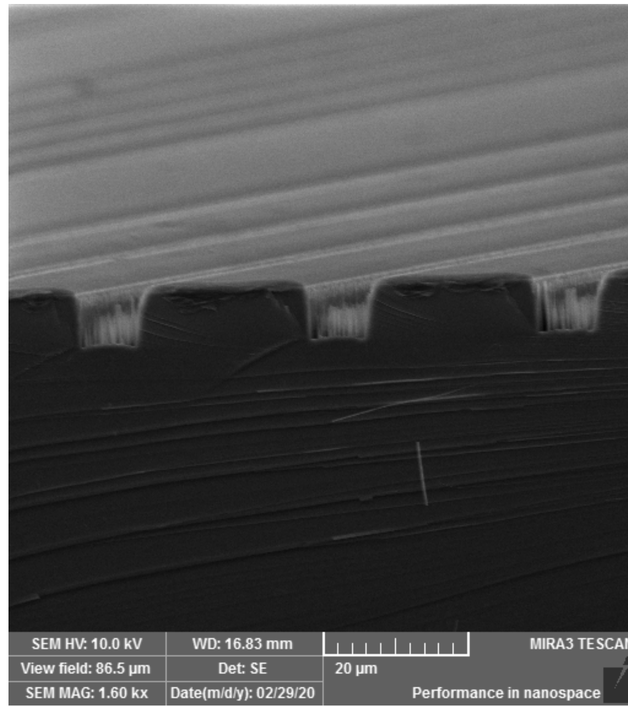

Figure 10. SEM cross-section showing lack of AZ 5214 E-IR damage

Effect of ICP Power on Selectivity

For both Cr and SiO_2, increasing ICPP increases selectivity due to the formation of more F radicals and O^{2-} and F^- ions that reactively and physically etch Si, respectively. While the concentration increase of both species will increase the etch rate of Cr and SiO_2, the etch rate of Si will increase more.

For AZ 5214 E-IR, increasing ICPP approximately maintains selectivity due to the formation of more O_2 radicals and O_2 and F ions that increase the AZ 5214 E-IR etch rate.

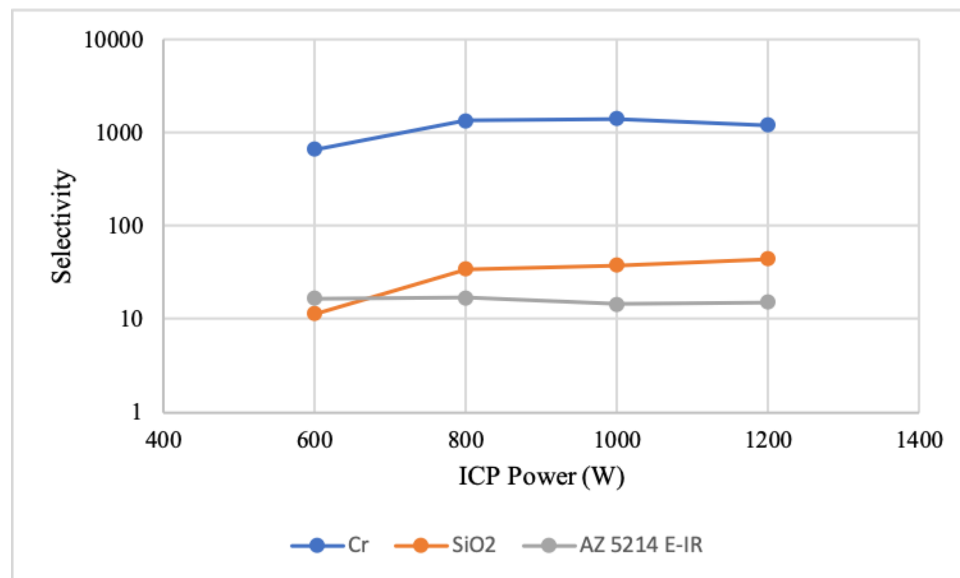

Figure 11. Selectivity vs. ICPP with RFP = 40 W, O_2 gas flow rate = 30 SCCM

Effect of O_2 Gas Flow Rate on Selectivity

Larger O_2 gas flow rates decrease selectivity Cr, SiO_2, and AZ 5214 E-IR (Figure 12). More O_2 species impede the flow of F radicals into the feature, decreasing the Si etch rate for all materials. This is the primary reason for decreased Cr and SiO_2 selectivity. Physical etching of the mask also increases due to the larger concentration of various species within the plasma. AZ

5214 E-IR is highly reactive with O_2 radicals, causing the etch rate to increase substantially as more O_2 is applied to the system (Figure 13).

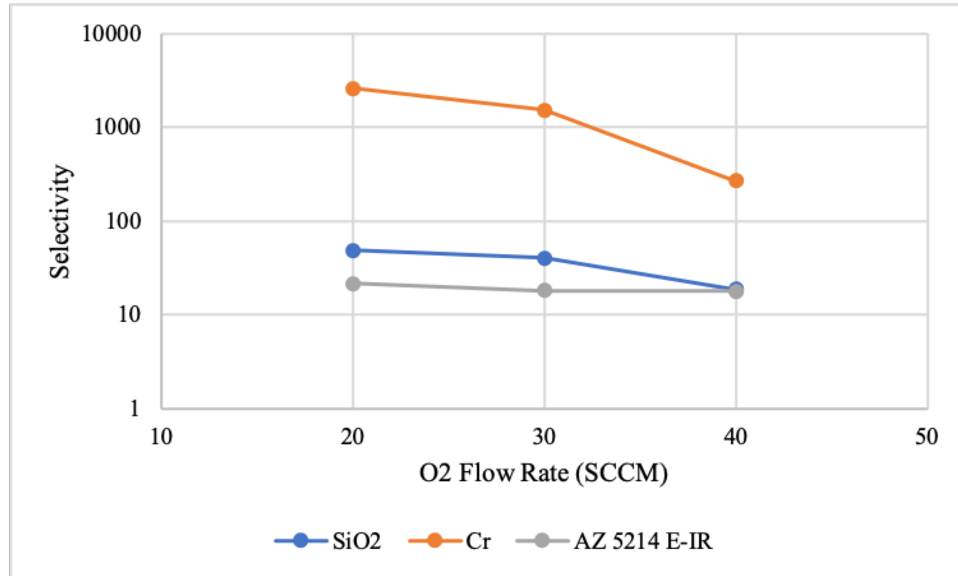

Figure 12. Selectivity vs. O_2 gas flow rate with ICPP = 1000 W, RFP = 20 W

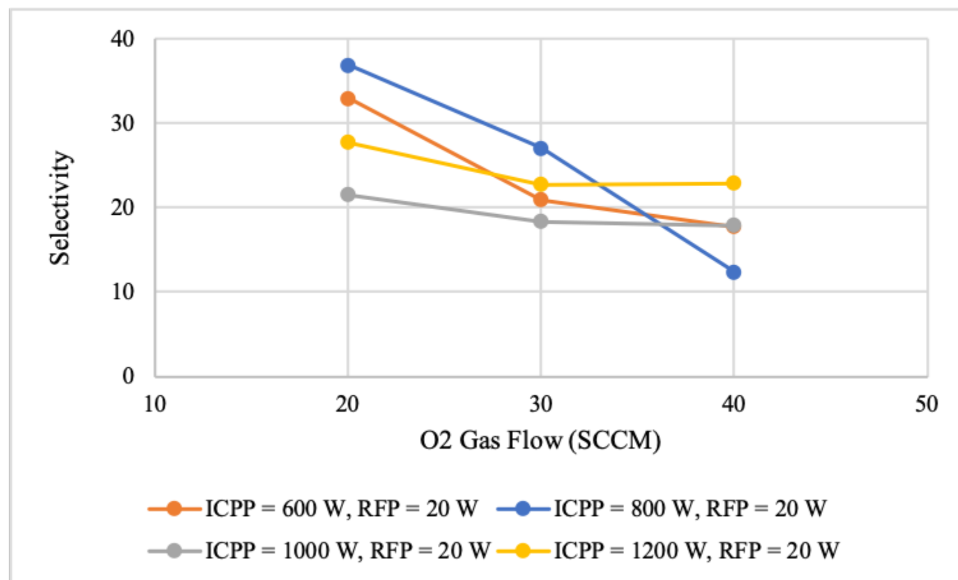

Figure 13. AZ 5214 E-IR selectivity vs. O_2 gas flow rate

Sidewall Profile

Effect of RF Power on Sidewall Profile

RFP was found to not have a significant effect on the sidewall angle nor roughness. Recipes with 10 W RFP (Figure 14) gave similar results as recipes with 40 W RFP (Figure 15).

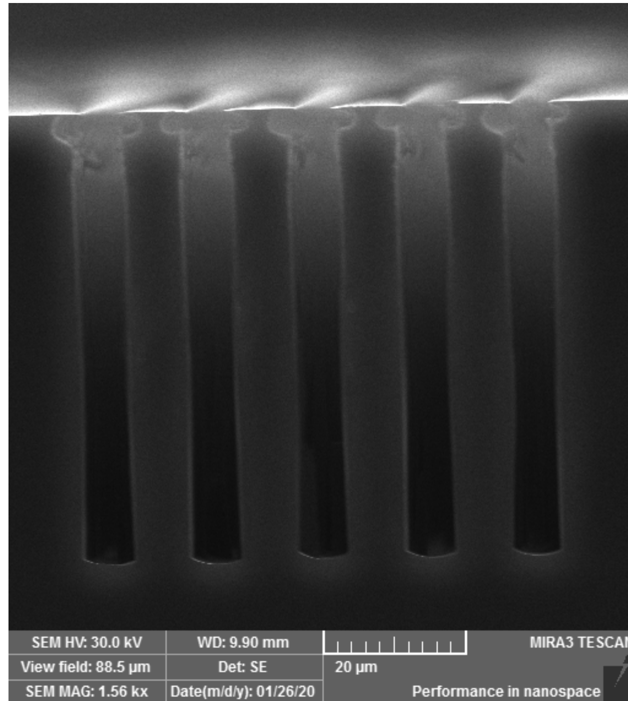

Figure 14. Smooth 90° sidewall profile using ICPP = 1000 W, RFP = 10 W, O_2 flow = 20 SCCM

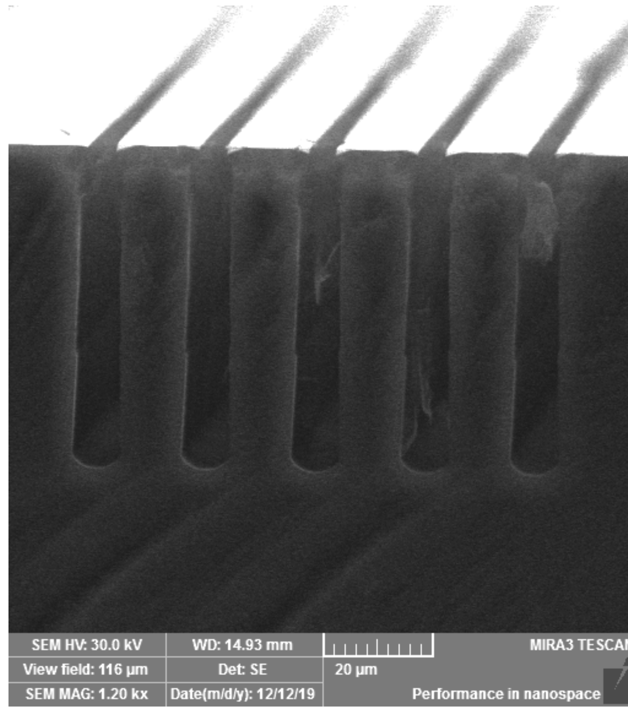

Figure 15. Smooth 90° sidewall profile using ICPP = 1000 W, RFP = 40 W, O_2 flow = 20 SCCM

Effect of ICP Power on Sidewall Profile

Increasing ICPP allows more uniform etching to occur both on the feature bottom and sidewalls. This improves the sidewall smoothness. Recipes with lower ICPP (Figure 16) gave rougher sidewalls than similar recipes with higher ICPP (Figure 17).

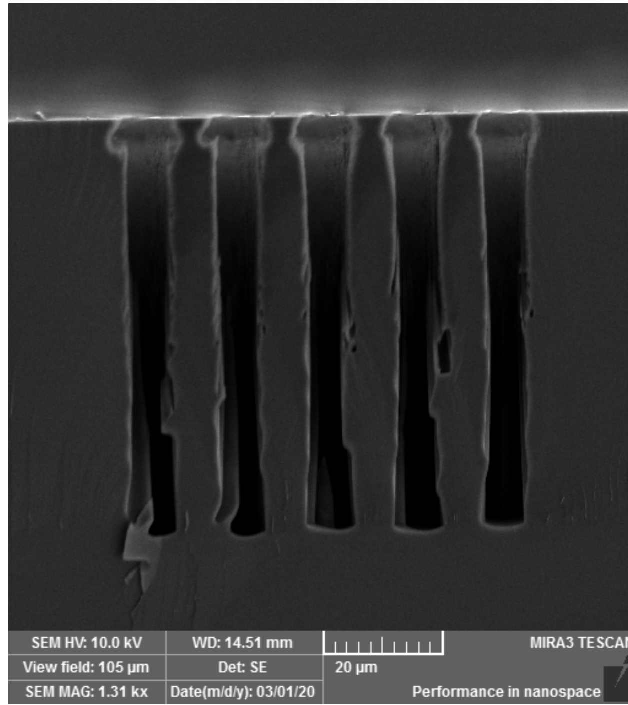

Figure 16. Rough sidewalls using ICPP = 800 W, RFP = 10 W, O_2 flow = 20 SCCM

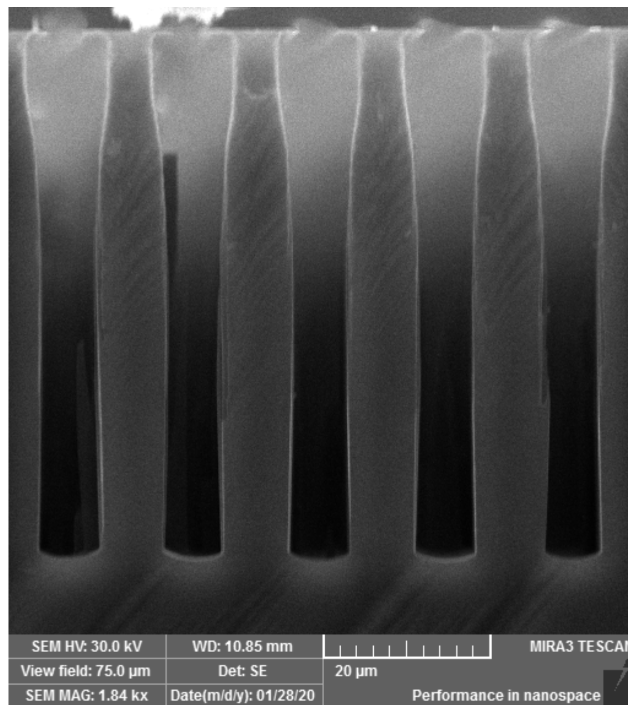

Figure 17. Smooth sidewalls using ICPP = 1200 W, RFP = 10 W, O_2 flow = 20 SCCM

Effect of O_2 Gas Flow Rate on Sidewall Profile

Larger O_2 gas flow rates form black Si more easily. More O_2 present forms both more numerous and thick SiO_xF_y films across the sidewalls and feature bottom, effectively creating a secondary mask within the feature. The places where this film is formed is largely random, causing non-uniform Si etch rates. This etch rate variation is what creates the needle-like structures on the feature bottom (Figure 18), where the tip of the "needle" is the SiO_xF_y mask. Needles of similar height to the feature depth were also seen for AZ 5214 E-IR recipes (Figure 19).

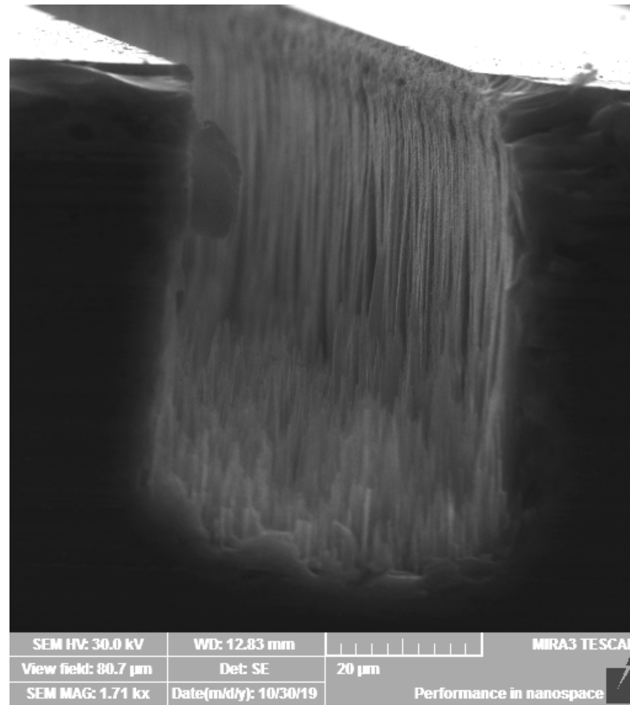

Figure 18. Black Si formed in the bottom of a 40 µm wide feature

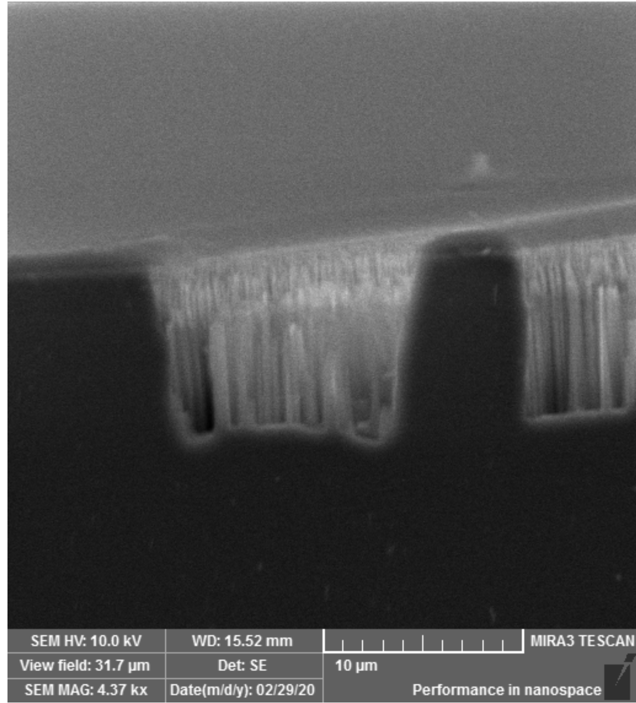

Figure 19. Black Si needles of similar height as feature depth

CHAPTER IV

CONCLUSION

While the Bosch process is the preferred deep reactive-ion etching method due to its ability to create a continuous sidewall passivation layer, the cryogenic method presented in this thesis is an acceptable alternative when the Bosch process is not available.

Three variables – radio frequency power, inductively-coupled plasma power, and O_2 gas flow rate – were tested with the goal of achieving high aspect ratio structures, high etch mask selectivity, and smooth, 90° sidewall profiles.

Higher RFP increased the aspect ratio due to larger vertical etch rates, decreased selectivity due to higher heat and more energetic bombardment, and had no effect on sidewall profile or angle.

Higher ICPP decreased the aspect ratio due to larger horizontal etch rates, increased selectivity for Cr and SiO_2 due to larger Si etch rates, maintained selectivity for AZ 5214 E-IR due to an increased Si and photoresist etch rate, and improved sidewall profile due to more uniform etch rates throughout the feature.

Higher O_2 gas flow rates decreased aspect ratio due to the restriction of F radicals to the feature bottom, decreased selectivity, and worsened sidewall profile due to the formation of more SiO_xF_y micromasks within the feature.

With the data these experiments produced, future researchers can design device processes appropriately according to the results presented.

The material, thickness, and deposition method of the etch mask can be chosen to maximize selectivity and prevent damage or cracking under the etch conditions. Sidewall angle

and smoothness can be controlled through the use of O_2 gas flow rate and ICPP, depending on whether smooth or rough sidewalls are desired. Black Si may also be easily formed. Expected aspect ratio values can be integrated into the device design.

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