CMOS INTEGRATION OF A SELF-POWERED RECTIFIER

An Undergraduate Research Scholars Thesis

by

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ABSTRACT

CMOS Integration of a Self-Powered Structural Health Monitoring Sensor System

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Literature Review

The structural health monitoring device proposed by Jason Lee Wardlaw in [1] has been shown to have individual circuit blocks that operate at the technology used, which is an ON Semiconductor 0.5µm Complementary Metal Oxide Semiconductor (CMOS) process. To advance this research, an IBM 0.13µm CMOS process will be used to replicate the operability of the circuitry and obtain an overall system integration onto a single semiconductor chip.

Thesis Statement

The use of the IBM 0.13µm CMOS process will be explored in its ability to replicate the system operability of that proposed in [1]. It will also allow for a higher density of transistors to fit in a single area (allocating less space for each system block to fit on a single chip) and a lowered overall power consumption, making it a suitable sensor for monitoring structural devices that surpass a lifetime comparable to that of civil infrastructures.

Theoretical Framework

Different CMOS technologies exist in order to build semiconductor chips. TSMC (Taiwan Semiconductor Manufacturing Company), GlobalFoundries, ON Semiconductor, AMS (Austria Mikro Systeme) AG, and AIM (American Institute for Manufacturing) Photonics are among a few of the many companies that supply these technologies. Each of these companies have different CMOS processes; however, for building analog components, not all of them are suitable due to the fact that there are certain transistor properties that need to be manipulated which can only be done at a certain transistor size. For compliance reasons, an IBM (International Business Machines) 0.13µm CMOS process will be used in this research as it is already accessible to the Electrical and Computer Engineering Department at Texas A&M University.

Project Description

The structural health monitoring device is set to operate under the conditions set forth by the structure being analyzed. The device proposed in [1] places an emphasis on bridges, but similar methods can be applied to any civil structure that exhibits vibrations which can be converted into usable energy. The operating frequency is expected to be around ~20Hz and voltage amplitude acquired by the memory-shape alloy is predicted to be around 1V. Both of these operating conditions were taken into account when building the circuitry that will monitor the health of the civil structure which then set the necessary certain circuit component to build the sensor.

This system will contain a component for harvesting vibrational energy, power-conditioning circuitry to supply power to all other blocks of the system, a sensor, a low-power analog-to-digital convertor, and a low-power radio-transmitter to send the data to a central processing location. All system blocks operate under the CMOS process used in [1] but in order

to make the system a more robust one, a different technology will be explored which will both reduce the amount of power consumption as well as increase the amount of circuit components which can fit onto a single semiconductor chip. The technology used in research is an IBM 0.13µm CMOS process which greatly reduces the amount of area used by a single transistor and requires less energy to operate in its saturated region.

Due to the time constraints of this project, it was only possible to focus on one of the blocks in this system. Although it can be argued that the ADC or the transmitter are vital parts of this sensor, none of the circuity would be functional if a power source were not present, therefore, the extension of this work will devote constructing and optimizing the power harvesting block. In the future, the rest of the blocks will be designed and integrated using the IBM 0.13µm CMOS process as well.

After focusing all efforts on the self-powered rectifier, it was found that the same functionality could be obtained from the circuit presented in [1] using a smaller technology. However, some changes are presented in this work that were made in order to optimize the circuit. The details of the changes are presented in the later chapters of this work but in the grand scale, the breakdown voltage of the technology (1.2V) for a single active device was achieved in 3 stages of rectification, the output of the rectifier was shown to have an equivalent output impedance of 17kΩ, and it is possible of supplying a maximum load of around 70µA to external circuitry, which is expected to be enough for the blocks it is supporting.

INTRODUCTION

Civil infrastructures are some of the most depended-on structures for society to function, therefore, it is sensible that a lot attention be placed in analyzing the health of said structures. Roads, highways, and bridges are amongst the most important since they are the means in which people commute from place to place. Efforts have been placed in non-destructive evaluation [2-3] of bridges and roads, where the impedance-based monitoring has been used in order to detect crack as well as the use of eddy currents in corrosion detection, but due to cost and functionality, other methods must be explored.

Jason Wardlaw has proposed a system in [1] that detects the relative stress and strain of a bridge as a vehicle passes above it by sensing the vibrations experienced by the bridge itself. The sensing system consists of a vibrational energy harvesting component, power conditioning circuitry, a sensor, a low-power circuit to convert the sensor information into an electrically digital signal, and a low-power transmitter to send the data to a central data processing location via-wirelessly. In his system, Wardlaw's circuit blocks were constructed using a 0.6µ-ON Semiconductor Complementary Metal Oxide Semiconductor (CMOS) process which allows for the smallest transistor to be 600nm in length and 800nm in width.

As electrical technology advances one would expect for the speed of their electronics to reduce in size, become faster, more reliable, etc. as is the case for the proposed system mentioned above. The technology used in order to produce the equivalent architecture of [1] will be a 0.13µ-IBM CMOS technology which allow for smaller transistors of area 180nm in width and 120nm in length. However, an effort must still be made to fully understand the components that make up the sensor system to assure that the functionality remains the same. Given that by changing CMOS

process technologies is more than just scaling transistors by a given constant, this makes this feat more challenging.

This sensor system is composed of various parts. An external coil which after experiencing vibrations will pass an electric current to the charge pump that will be used as the power rectifier. A Wheatstone Bridge circuit to sense the change in the bridge's stress and strain which will then be changed from referencing itself into a reference to ground (Differential to single-ended conversion). From there, the analog signal will be converted into a digitalized signal using a converting block and then sent through a radio transmitting circuit in order to send the recorded signal to a central processing location. This system is shown in Fig. 1.

However, due to time constraints, this system will take too long to optimize if done in a single year since as stated above. The integrity of the system relies on the proper scaling and understanding of minute detail in each individual component exercised in [1]. Therefore, it is important to focus on the most vital part of the overall circuitry which is the power-harvesting block because without power, all other components it supplies will be rendered useless.

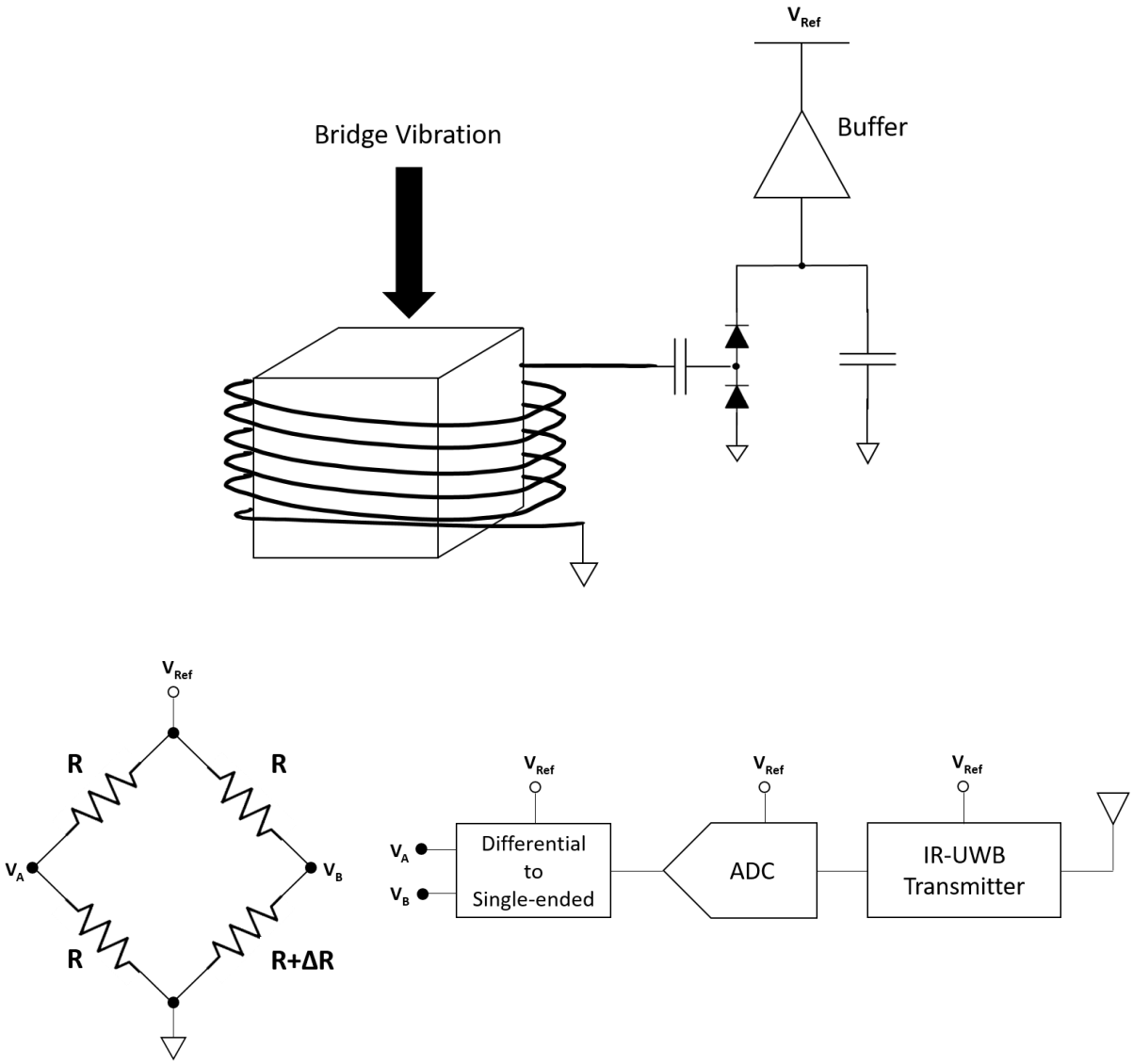


Figure 1. Generalized structure of the sensing system.

CHAPTER I

POWER TRANSFER

An electrical rectifier refers to electrical devices that transform electric current operating in a time-varying fashion into a direct and constant supply, or with engineering terminology, converting a signal from alternating current (AC) to direct current (DC). Rectification can meet a variety of needs such as radio applications, the transfer of power, and in this application, energy-harvesting. However, to produce a constant source of electrical current, there must first be a source of usable energy.

This work focuses on converting vibrational energy into a usable source of power. In [1], Wardlaw uses a mechanical-to-electrical converter composed of an alloy that could shift shape which would be wrapped around a metal coil so that when the coil experiences vibrations, electric current would be induced. This current is induced because of electromagnetic principles: a change in the magnetic flux (magnitude of magnetic flux links in a given volume) of a metal with a physically closed loop, induces an electric field within the metal itself to oppose the changing flux, which in essence, pushes free electrons in the metal from one side to the other, creating an electrical potential difference from one end of the metal to the other. Because this coil vibrates back and forth, the electrical potential difference alternates its high and low potentials between the two ends of the metal, creating a time-varying signal. This vibration is independent of the size of vehicle driving on it. Instead, this vibration depends on the natural frequency of the bridge which is typically known to range from 2 to 20Hz.

Knowing the frequency of operation is vital since it directly affects the type of rectifying equipment to be used. From [1], the coil was also devised to give around $1V_{0\text{-}pk}$ amplitude of the

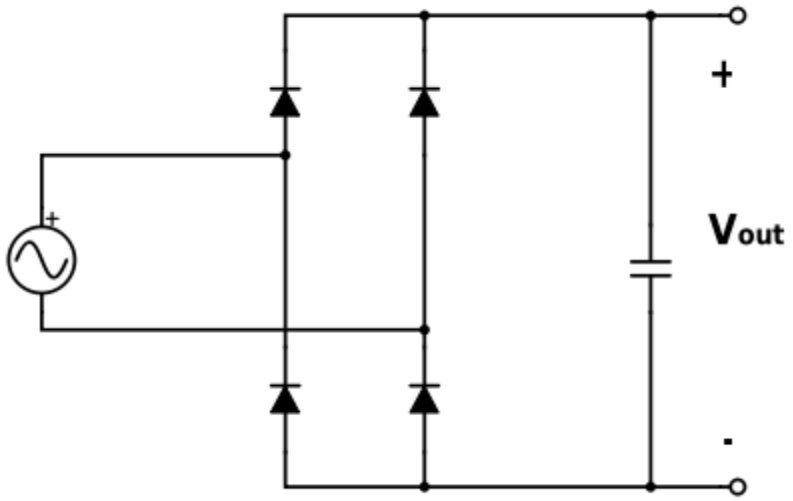


Figure 2. Full-wave rectifier.

given signal by changing the amount of turns on the coil and setting the vibrational frequency to 20Hz, making the signal perpetuated to the rectifier possible to be modeled as a sinusoidal waveform. Although for the sake of simulation, any periodic signal will work if it has a frequency of 20Hz. To decide what type of rectifying equipment to use, first we look at the common rectifiers at disposition.

A. Basic Rectifier

One of the most basic rectifiers known to exist is referred to as a full-wave rectifier [4]. This type of rectifier converts a time-variant signal into a DC-signal by using two key components, diodes and a capacitor. Shown in Fig. 2 is the most common topology of the full-wave rectifier. The capacitance at the output node is used to smooth out the output voltage to a constant output with the ripple dependent on the size of the capacitor.

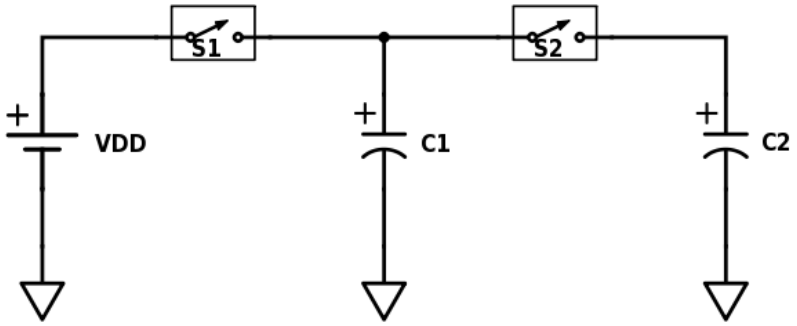


Figure 3. Common DC charge pump structure.

Although this is a very common structure, its efficiency is degraded by the fact that each diode has a turn-on voltage which the source must overcome before any current can be conducted to the output node. Moreover, most CMOS processes do not even have the option to create the junctions necessary to construct diodes on silicon dies. The latter constraint pushes this work to focus on a certain type of rectification common in CMOS processes referred to as charge pumps.

B. Switched-Capacitance Charge Pumps

In CMOS processes, a common power-sharing structure consists of a capacitive-switch network is used to generate DC outputs from either time-variant or constant-power supplies. A one-stage charge-pump system consists of a source, an input and output capacitance, and two switches. Ordinarily, the output capacitor is much larger than the input capacitor for dominance in equivalent output resistance, however, choosing too large of a value will directly impact the amount of time needed to saturate the output to its steady state so care must be taken in choosing components. A system as such can be modeled very simply as is shown in Fig. 3, using a constant voltage supply as the source. This, however, can be extended to time-variant sources without much operational difference.

Both switches work opposite of each other with only one of them closed at any instant. During start-up, the first switch is responsible for supplying the first capacitor with a net charge equivalent to the capacitive-voltage product from

$$Q_1 = V_{DD} \times C_1 \tag{1}$$

while the secondary switch is responsible of sharing the charge with the output capacitor per

$$Q_2 = V_{out} \times (C_1 + C_2). \tag{2}$$

Once the output capacitor has acquired some charge, the past switching stages play a role in the total output voltage as expressed in

$$Q_{SW\ 1\ CLSD} = V_{dd} \times C_1 + V_{out}(t_0^+) \times C_2 \tag{3}$$

and

$$Q_{SW\ 2\ CLSD} = V_{out}(t) \times (C_1 + C_2). \tag{4}$$

If designed correctly, with negligible switch resistance and switching time, the output voltage should be equivalent to that of the source in the DC-case after a certain amount of switching stages proportional to the output capacitance. This DC-DC pump operation can easily be translated over to an AC-DC converter by a simple change mentioned in the next chapter without much difference in the stated equations. The DC-DC charge pump was analyzed in this case because it is much easier to comprehend compared to its AC-equivalent.

CHAPTER II

CHARGE PUMPS

Different topologies of AC charge pumps will be explored in this chapter. An idealized topology for AC charge pumps is shown in Fig. 4 and it has the same overall functionality as the DC-case in chapter one. Switch one turns on during the negative half-cycle of the source's input while the second switch turns on during the positive half-cycle of the input. A constant-current source is connected on the output in order to model a load at the output of the rectifier since after all, this charge pump is responsible for powering all external circuitry.

Under ideal conditions, the loaded charge pump can be modelled by a few equations that will help characterize it under different loading conditions. While the overall operation is almost identical to that of a constant-source charge pump, the main difference is that for the time-variant system, the frequency of the source now dominates the characterization of the system and the control mechanism for the switches must be worked around it. The output of the charge pump is the main focus of the device so extensive characterization is important.

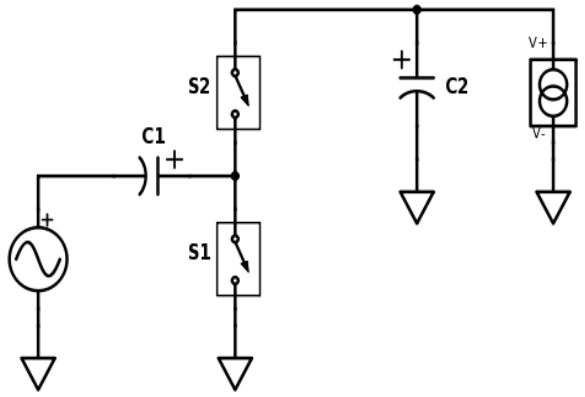


Figure 4. Common AC charge pump structure.

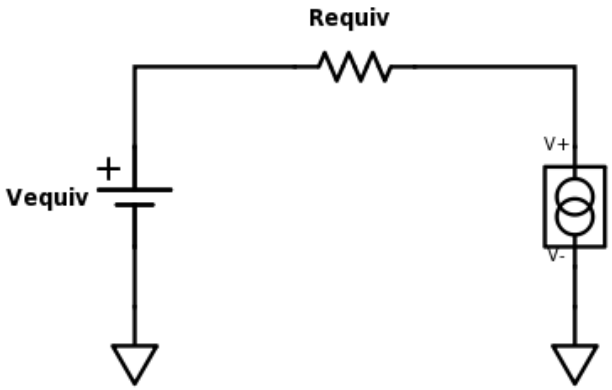


Figure 5. Equivalent charge-pump circuit with constant load.

In this case, the equivalent output voltage able to be delivered will be twice the amplitude of the AC-source per $V_{equiv} = 2\hat{V}_{in}$ while the impedance of the system at the output will be dependent on both capacitances is determined by $R_{equiv} = \frac{1}{2f}(\frac{2C_2+C_1}{C_1C_2}) \cong \frac{1}{fC_1}$. As mentioned before, the larger the output capacitance is compared to the input capacitance, the less the equivalent resistance depends on the former of the two. From these two common derivations, it is now possible to characterize this system as a series of a source and a resistance as shown in Fig. 5, to which a constant-current output can be applied to. This, again, represents a constant load being fed by the rectifying system, modelled by $V_{out} = V_{equiv} - R_{equiv}I_{out}$ to understand the system dependence on the output voltage and inner components. The output voltage ripple due to the current-load is of that shown by $\Delta V_{out} = \frac{I_{out}}{2fC_2} = \frac{V_{equiv}}{2fC_2R_{Load}}$ and while it may seem that the larger the value of the output capacitance brings overall better system characteristics, it is worthy to reiterate that the settle-time for the circuit is also directly proportional to that capacitor's size. Too large of a capacitor and the system takes too long to reach its final value, too small and the system starts to depend on the input capacitor.

Now that the ideal system is characterized, the dependence of vital variables on device parameters is concretely understood and the limitations of the system is as well. From here, non-ideal component-impact can be predicted. With respect to the switches, there is no CMOS transistor nor capacitor that will have negligible equivalent series resistance (ESR) so this will cause a time-dependency in the ideal equations mentioned above. Adding on, these switches must be controlled either internally or externally. If the sensor is to be sustained for the lifespan of a bridge, there is no lithium-ion technology to date that will have that lifetime so they can not feasibly be controlled externally, therefore, other control options must be explored.

A. CMOS Rectifiers

Charge pumps are composed of a combination of switches. The choice of rectifier in this work is a Cockroft-Walton type with the rudimentary topology shown in Fig. 6, which uses serial stages of diodes, or switches, and capacitors to generate a large DC output voltage from a time-variant source at the input. This system is commonly known as a rectifier multiplier and is one of the most used topologies for integrated circuits in terms of rectification, however, the diodes are replaced by transistors acting as switches.

The network of the rectifier has similar operation to the charge pump explained before. Unfortunately, the diodes acting as switches causes the overall system to degrade. The turn-on voltage required of the diode to activate and allow current to flow, V_D, will affect the charge flow in both the half-cycles of the AC source. Taking this turn-on voltage into account, the output can be modelled as

$$V_{out} = 2 \times \left(\hat{V}_{in} - V_D\right). \tag{5}$$

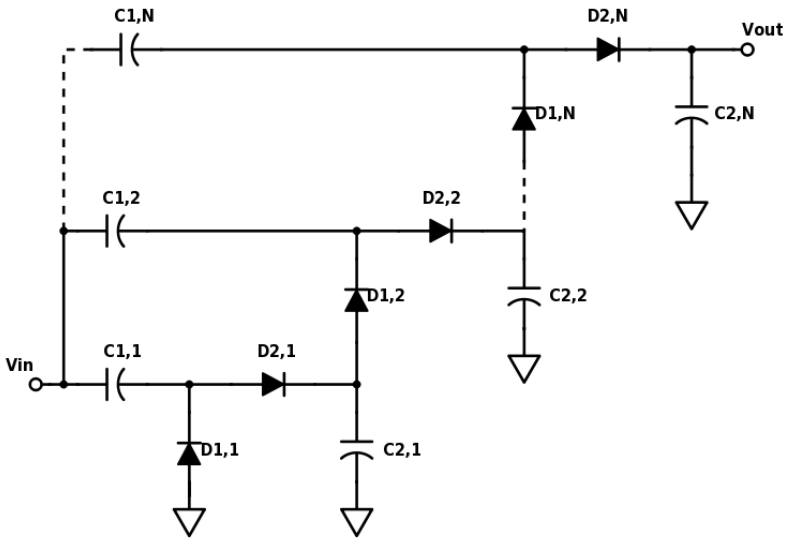


Figure 6. Cockroft-Walton Rectifier Multiplier

These loses happen regardless of the device used to allow the flow of current. To account for losses in turn-on voltage that even happen in CMOS-based switches, the system is cascaded using identical stages and techniques focusing on turn-on voltage cancellation will be applied to increase the output DC level. In many cases, increasing the input amplitude would fix the issues caused from these losses, as seen from (5), but this method is chosen since increasing the input voltage amplitude is not feasible in most applications.

As mentioned above, diodes (even low-turn-on voltage diodes, Schottky Diodes) are not made available in most CMOS processes and must therefore be replaced by transistors. Transistors can be used for a multitude of things in analog applications, including voltage-controlled switches. Shown in Fig. 7 are several possible topologies for using transistors as switches, however, some are more efficient than others due to the required turn-on voltage at their gate terminal with respect to their source terminal. All rectifiers will be assuming an input of $V_{in} = \hat{V}_{in} \times \cos(2\pi f t)$.

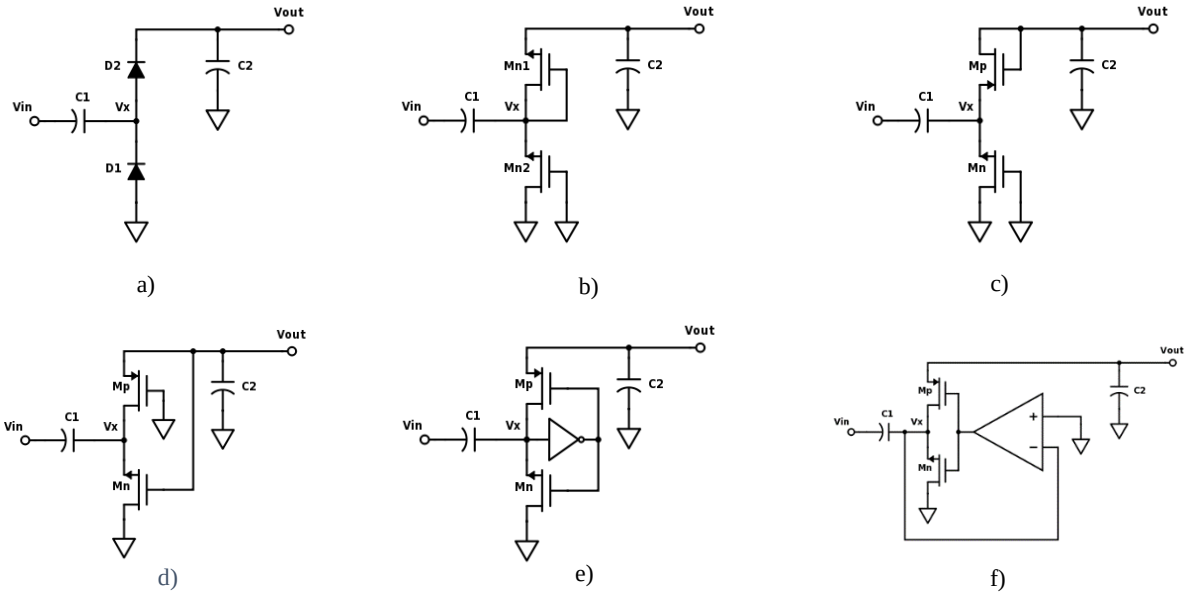


Figure 7. Possible rectifier - a) Diode-based, b) NMOS-based, c) CMOS-based, d) SVC-based, e) Inverter-based, f) Comparator- based

The rectifier in Fig. 7(a) shows the Cockroft-Walton RM. During start-up, the input waveform is seen at node V_X, so at the negative-half cycle of the input, the voltage level must surpass the required 600-700mV turn-on voltage of the diode to conduct a charge on C_1. Once surpassed, a maximum charge equal to $C_1(V_{in,max} - V_{turn-on})$ is stored on C_1. During the positive half-cycle of the input, the second diode conducts and not the charge stored on C_1 is shared with C_2. This operation has already been proven to work, however, the output DC-level is degraded because of the turn-on voltage required of the diodes. Applying Schottky diodes may appease this issue but this does not appease the issue that diodes are not available in most CMOS processes.

The rectifier in Fig. 7(b) shows an NMOS structure for both switches. Both transistors are in a diode-connected configuration and would therefore only need the switch's threshold voltage-difference from their source and gate terminals to activate. In this case, however, the top NMOS

transistor would suffer from the body effect and therefore a larger threshold voltage must be applied for it to turn on. The total output voltage level is shown in

$$V_{out} = 2\hat{V}_{in} - V_{tn,0} - V_{tn,Body}. \quad (6)$$

A Zero-V_{th} component would be ideal in this application but that would require additional masks and area [5] in the circuit layout, generating more costs. Fig. 7(c) aims to appease this issue by replacing the top NMOS transistor with a PMOS type. Due to the mobility of holes being significantly slower than electrons, the PMOS switch must be made much larger to conduct an equivalent amount of current. Doing this, however, increases the parasitic capacitance, C_p, at that node, given that parasitics scale by component size. If a PMOS transistor is to be used as one of the switches, regardless of the gate-connection, care must be taken to assure that the voltage level at *X* is not severely affected by these parasitic capacitances since the output level heavily depends on the voltage swing at that node. V_X can thus be characterized by $\hat{V}_x = \hat{V}_{in}\frac{C_1}{C_1+C_p}$, where C_p corresponds to the total parasitic capacitances at that node.

Fig. 7(d) shows a topology commonly referred to as Self-V_{th} Cancellation (SVC) and is proven to work for rectification purposes as explained in [6]. The use of this architecture allows for the transistors to act as switches rather than diodes because of their gate-connections. The output level is only deteriorated by the drain-to-source voltage differences of the transistors and can thus be characterized by

$$V_{out} = 2\hat{V}_{in} - V_{DSN,Sat} - |V_{DSP,Sat}| \quad (7)$$

Considering their operation at steady-state, the superposition of the voltage level at node *X* and the AC-input cause a change in the drain terminals of the transistors which autonomously decides which switch operates in its saturation region. During positive half-cycles of the input, the drain-to-source voltage of the PMOS reaches a level above $V_{DSP,Sat}$ necessary to conduct and similarly

with the NMOS transistor during the negative half-cycles. However, this architecture is victim to degradation after it is cascaded into multiple stages since the voltages at the gate-terminals cannot be controlled.

Fig. 7(e) is an inverter-based rectifier which, by the name, suggests that the input signal is inverted and applied to both gate terminals of the switches simultaneously. The inverter applies a voltage level to the gates that will effectively decide which transistor to activate [7]. Inspecting this architecture as a digital circuit, a high input (the positive half-cycle of the input) will be inverted to a low output and would effectively turn on the PMOS gate. The inverse happens when a low input (negative half-cycle) is inserted and the NMOS gate is then allowed to conduct. The effective output level will be the same as in the SVC-structure and characterized by (7) as well. However, the input signal is not a digital signal and an effective 1 or 0 may not always be the case. The gain of the inverter is actually what "inverts" the input by causing a 180^{o} phase shift once the AC-portion of it passes through the PMOS or NMOS devices within the gate. The efficiency of this circuit is degraded due a series of problems: the maximum gain that the inverter can achieve is limited by device size and branch current, the amount of time it takes for the signal to shift 180^{o} in phase and conduct the respective gate, and because the inverter solely determines which gate conducts based on the voltage level at node X without consideration of the output level. The latter problem comes into effect after considering the following scenario. In steady-state, after the voltage level at node X has raised just enough to be inverted, the PMOS gate-terminal is effectively connected to ground and a path has been created from node X to the output. However, the voltage level at X could be lower than the output level for a period of time and some charge is used up because of the reverse conduction.

To appease all problems presented by the inverter-based rectifier, a comparator-based rectifier is proposed as shown in Fig. 7(f) and presented in [8]. The authors from the work specify that the comparator used be dynamic in order to actively compare the value of node *X* and its relative value to a reference voltage. The reference in this case would be ground, so as to know when the input changes from positive to negative and vice-versa. This comparator rids the problem of reverse conduction, however it does raise the design issue of creating a comparator that will not constantly dissipate power. A current mirror was used in [8] to maintain all transistors in their active region, however, this generates the issue of static-power dissipation, one that would be preferably avoided since added loading will deteriorate the output level.

If the comparator-based design were to be a clocked device, one that would only dissipate current as a decision was being made, the device would be ultimately the best design choice. For his work in [1], Wardlaw decided that this was the type of architecture he would follow, the only problem now is understanding the internal components of the comparator and how they affect the overall system efficiency in order to optimize and scale it with another CMOS technology process.

CHAPTER III

COMPARATOR-BASED RECTIFIER

Power harvesting has been the focus of this work with an emphasis placed on a rectifier that is both self-powered and consumes a low amount of energy. Due to the nature of the input conditions to the rectifying circuitry, there are certain specifications that cannot be altered such as peak input-voltage (~1V) and operating frequency (~20Hz in this case). All of these mentioned criteria are some of the design considerations that are taken into account in constructing this circuitry.

The rectifier of choice, mentioned in the previous chapter, uses a comparator to accurately decide when to turn on the respective switches in the charge pump. The comparator is able to make this decision based on the relative voltages at node *X*, Ground, and the output voltage level and is powered by the output of the single stage. This method of rectification is not one that utilizes V_{th} cancellation techniques, mainly due to the reverse conduction the circuit would experience once node *X* causes the drain and source to change places in the PMOS transistor as seen with other architectures. And although the comparator-based rectifier proposed in [8] is not entirely applicable in this case due to the static consumption of power, it still shines light onto the benefits of using this topology to select which of the two switches can conduct. Under conditions that require low power consumption and low operating frequencies, it is common practice among the analog and digital realms to use switched-capacitor systems. This method allows the circuit to be selective in when and where current is conducted and is the operational foundation of charge pumps mentioned in previous chapters. Inverters are also a great method for amplifying the comparator's output signal during comparison due to their low-headroom requirements for the

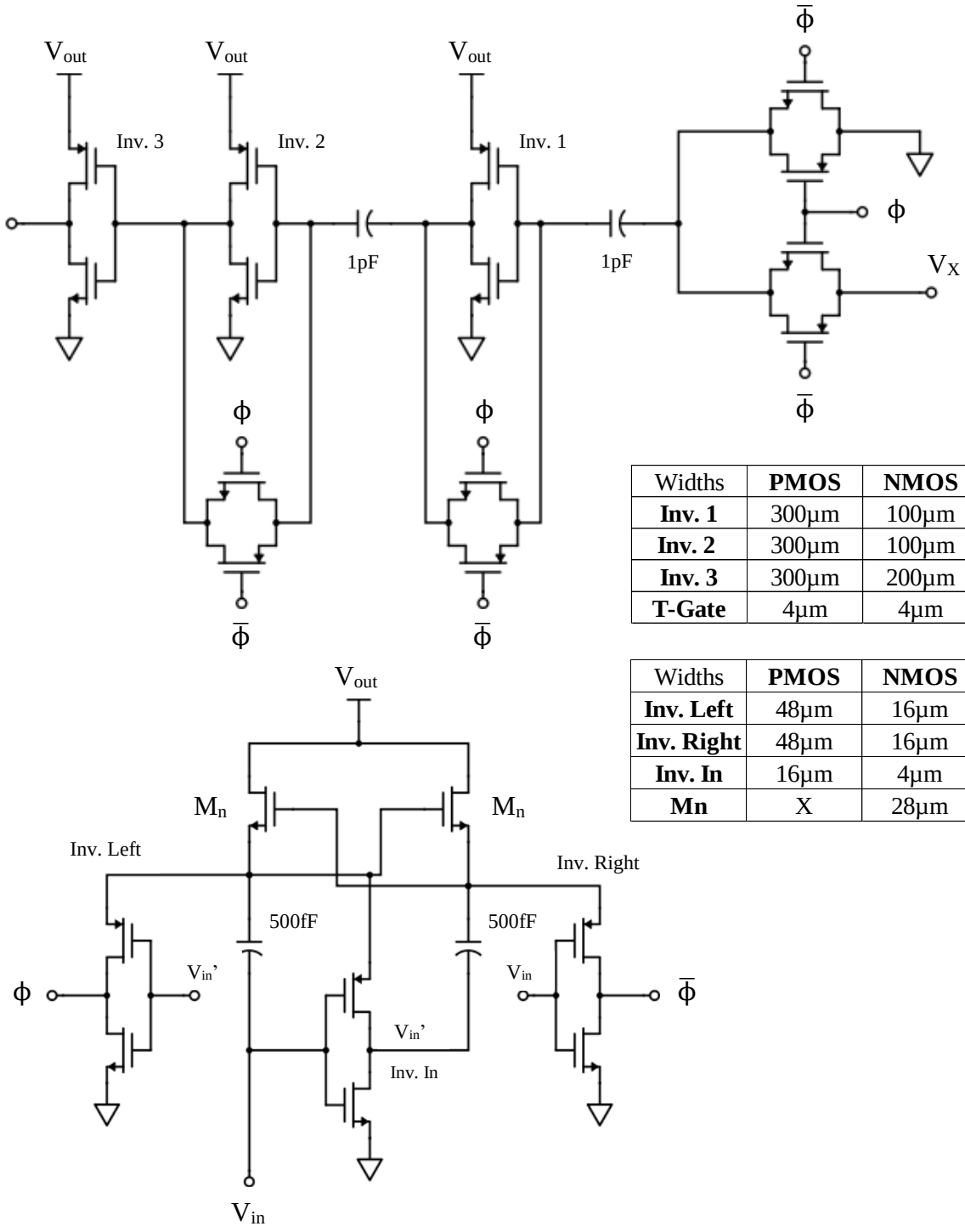
gain they attain. A combination of these two methods is what will make up the internal structure of the comparator used in this work.

The comparator's architecture is shown in Fig. 8 along with a clock-doubling circuitry to allow for the system to drive the transmission gates used as switches. This comparator is composed of a series combination of three inverters for maximum gain. The transmission gates are used to bias the inverters to their toggle positions for optimal gain and capacitors to store the charge due to voltage difference before being amplified. A supplemental circuit is added to this comparator to generate a differential clock signal to be fed into the transmission gates. The differential clock signals feed into the NMOS and PMOS transistors simultaneously through their gate terminals to reduce the amount of on-resistance and expedite the internal comparison [9]. The overall rectifier is wired as shown in Fig. 9.

A. Internal Operation

The comparator used in this work is a low-powered, clocked comparator, that only dissipates energy once the transmission gates conduct and a comparison is being made. The clock doubler complements the comparator in this low-energy effort by providing the driving signals for the transmission gates. The ports ϕ and $\overline{\phi}$ are 180º offset of each other and are aimed to reduce the ON-resistance of the gates.

There is a certain operation that is expected of the comparator during different input cycles. Whenever the voltage level at node *X* is larger than Ground, the positive half cycle of the wave, a low output is expected to drive the external PMOS device. The NMOS will still conduct a small amount of current given by $I_{leakage} = I_0(1 - e^{-\frac{V_x}{\phi_t}})$, where I_0 is a process-dependent variable that



Widths	**PMOS**	**NMOS**
Inv. 1	300µm	100µm
Inv. 2	300µm	100µm
Inv. 3	300µm	200µm
T-Gate	4µm	4µm

Widths	**PMOS**	**NMOS**
Inv. Left	48µm	16µm
Inv. Right	48µm	16µm
Inv. In	16µm	4µm
Mn	X	28µm

Figure 8. Comparator architecture (top) with supporting clock-doubling circuitry (bottom). Devices all have lengths of 0.12µm and use multiple fingers not shown here to achieve large width sizes.

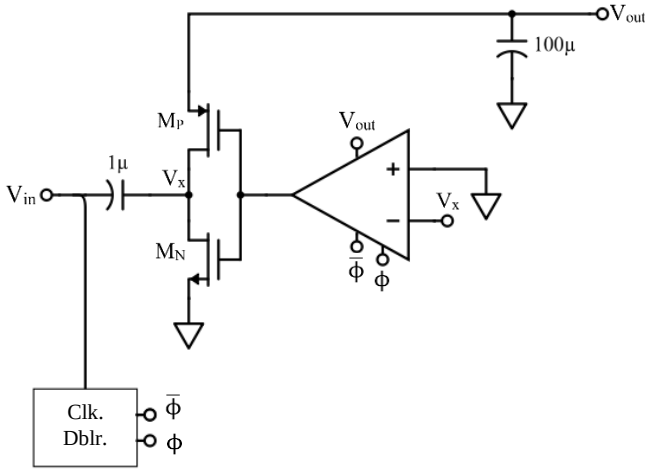


Figure 9. Rectifier architecture with comparator and clock doubler.
W_{NMOS} = 48µm. W_{PMOS} = 155µm. All Lengths are 0.12µm.

is process dependent and proportional to device proportions. Similarly, whenever the voltage level at node *X* is lower than Ground, the negative half cycle of the wave, a high output is expected to drive the external NMOS device and the PMOS device to conduct the leakage current.

Internally, the comparator is hard-wired to compare the voltage level of *X* against the value of Ground (0V) during the phase that ϕ is a low value and $\overline{\phi}$ is a high value. However, the clock-doubler will only produce such output when the input is at its negative half-cycle. In the positive half-cycle the transmission gate-driving signals change polarity, this is known as the sampling period of the comparator. During this sampling period, the voltage level at node *X* is higher than Ground automatically, so the output of the comparator must be as low as possible during this period. However, while sampling, the first two inverters in the chain are being placed at their toggle points and to prevent oscillation or ringing that will dissipate power, these two first inverters must be un-skewed. To ensure an output as low as possible and as much conduction from the PMOS device, the last inverter in the chain is skewed towards Ground but care must be taken so as not to harm the amplification of the last stage while in comparing periods. During the negative half-cycle of the input, node *X* is higher than Ground and the comparator is making a comparison.

The output of the comparator is as high as possible due to the structure of the comparator and the NMOS device now conducts current.

B. Clock Doubler

The main parameter to consider in designing the clock-doubling circuitry is the amount of current it is going to demand from the overall system since it directly correlates with the power dissipated. Since it is also powered by the single-stage output of the rectifier, care must be taken so that the amount of current it drains does not harm the overall efficiency of the system.

The clock doubler allows for the voltage level at the source terminals of the top, cross-coupled, NMOS devices to be nearly double of that of the source-voltage powering the device as shown in [10]. However, this operation is largely applicable for high operating frequencies with feasible on-chip capacitors provided by the CMOS technology process. For a frequency range near 20Hz, a high capacitance is in order. This would increase the time-constant of the circuit and not allow the stored energy in the capacitors to leak out before the voltage is essentially doubled at the source-terminals of the cross-coupled NMOS devices. However, due to the area restrictions of capacitors in CMOS processes and the costs that they generate, a smaller capacitance should be used and a voltage lower than double that of the source-voltage must be acceptable. To understand what voltage level is deemed as acceptable, what the signal drives must be known. The inverters that generate the clock signals have an output voltage given by

$$V_{clk} = V_{Src,NMOS}\left(\frac{C_2}{C_{gate}+C_2+C_{parasitic}}\right) \tag{8}$$

and, as shown, depend heavily on the gate-capacitances of the transmission gates they drive and the parasitics at the driving nodes. Thus, the transmission gates were designed with low parasitic capacitances to where the voltage driving their gates were enough to conduct with the clock

voltages and still be able bias the inverters to their toggle points with a low serial resistance given by

$$R_{T-Gate} \cong \frac{1}{\mu_N C_{ox}\frac{W_N}{L_N}(V_{GS,N}-V_{t,N})} \,||\, \frac{1}{\mu_P C_{ox}\frac{W_P}{L_P}(V_{GS,P}-|V_{t,P}|)}. \quad (9)$$

This equivalent resistance is applicable when the transmission gate is in saturation mode and is inversely proportional to the gate-voltage of each of the transistors. However, the gate-resistance, even when not in saturation-mode, decreases significantly with an increasing gate-voltage.

The authors in [9] and [1] wire the clock doubler such that the inverter used to generate the differential input signal is powered by the output of the rectifier. Since this inverter is being used as a static device, it will demand a constant supply of current. To appease this issue, the inverter at the input stage of the clock doubler is supplied by one of the gate voltages of the NMOS transistors. In this case, the rail that supplies the ϕ clock-signal is chosen. The clock doubler already dissipates low amount of energy due to the drain of the cross-coupled NMOS transistors connected through their drains to the source-voltage, but this assures that even the inverter responsible for creating a differential drive absorbs the least amount of current from the output. The amount of current drawn from the clock doubler with a voltage source of 1.2V is shown in Fig. 10.

C. Operation with Overall System

Now that the clock doubler is designed to meet the specifications of the transmission gates, there are some other design parameters to consider when designing the comparator to operate with the overall system. The capacitors were chosen so that the time-constant created with their value in combination of the on-resistance of the transmission gates is not small enough to where the stored charge in the capacitors dissipates before a comparison can be made. As mentioned before,

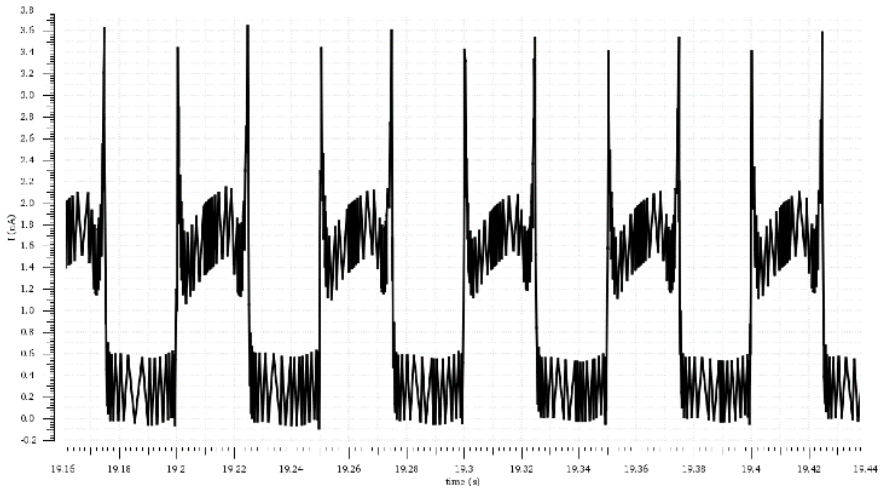


Figure 10. Clock doubler current absorption from a 1.2V source.
Peak current is seen as high as 3.6nA.

the inverters must be un-skewed for the first two stages to not allow unnecessary power dissipation through the PMOS and NMOS devices but must be designed such that they allow large amplification as given by

$$A_{inv} = (g_{mn} + g_{mp})(R_{dsn}||R_{dsp}). \tag{10}$$

The last inverting stage is purposely skewed towards Ground but not so much that the transistors are taken out of saturation and the entire amplification is harmed when making a comparison is being made. In a single stage, the comparator-based rectifier is able to generate a voltage level around 280mV as shown in Fig. 11. However, in most cases, this output level is not sufficient, therefore the output level must be increased by adding additional stages. In the IBM 0.13-micron CMOS process, the largest voltage that a single transistor can withstand from its drain-to-source or source-to-drain terminals is 1.2V. There are transistors that can withstand up to 3.3V in this technology, but they do require additional masks and take up more area. These are usually used for large power applications which is not the intention of this work. In order to supply the 1.2V, a cascade of two SVC-based rectifiers are applied to the output of the comparator-based single stage as shown in Fig. 12. The M_N and M_P are 48µm and 156µm respectively. Capacitor selection was

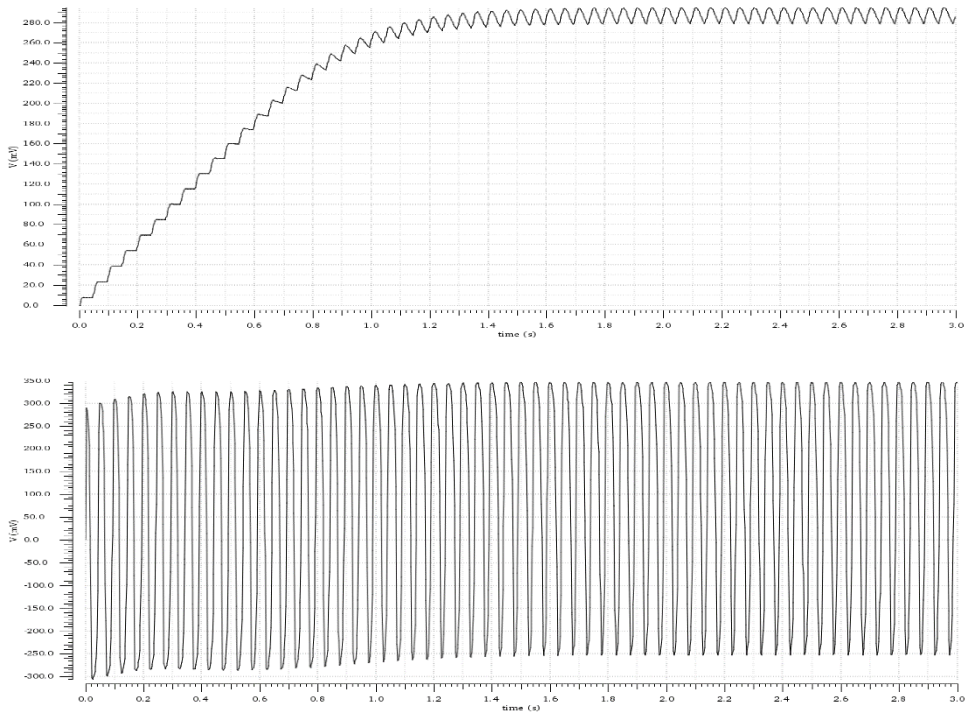


Figure 11. Output of single-stage rectifier (top) and voltage level of node *X* (bottom).

made using the initial design-protocol for charge pumps, making the output capacitance much larger than the input capacitance to reduce voltage ripple, however both large enough to neglect parasitic capacitance effects of MOS devices.

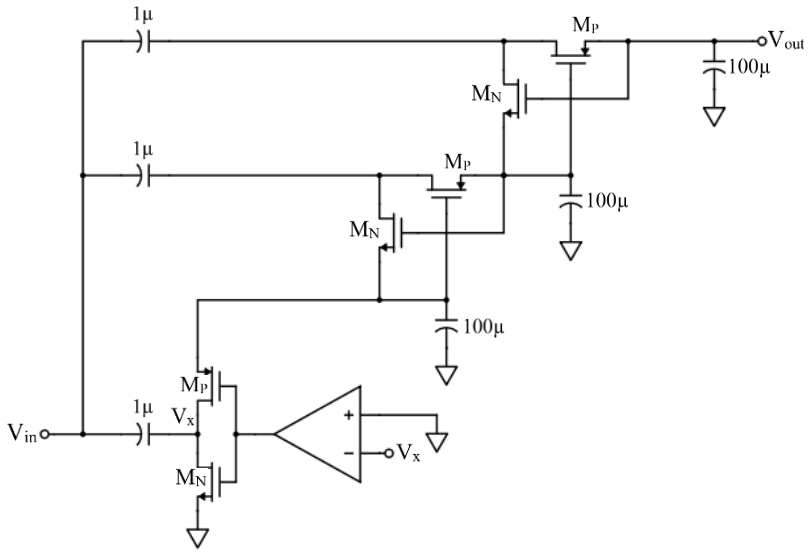


Figure 12. Overall rectifier with comparator-based rectifier followed by SVC-structures.

D. Design and Simulation

To justify the use of a comparator-based rectifier as the initial stage of the power harvester, it was first compared to a cascade of three SVC-based stages. The comparison was done with this structure of rectifier because it was shown before to be the next best architecture for rectification. The sizes of the NMOS and PMOS devices are the same as those in the comparator-based architecture. The results shown in Fig. 13 prove that the output of the rectifier containing the comparator generates a larger output than the pure SVC-based architecture by 100mV. Putting it into perspective, that is near 10% of the total possible voltage level. Although a comparator-based, single stage rectifier can only produce about 280mV when isolated, once combined with the complementary SVC-based structures, it generates ~467mV in its single stage. The reason for this increase in efficiency is due to the clock doubler. Since the clock doubler is powered by the overall output of the circuit, the higher the output DC-level, the larger the clock signals it can use to drive the transmission gates within the comparator. Therefore, as the output of the rectifier increases, the more the efficiency of the comparator-based stage increases, and therefore the efficiency of the rest of the system increases.

Since it has been proven through simulation that the comparator-based architecture works best, the next step was to layout the pre-silicon design of it on the IC-design toolkit, Cadence. The transmission gates were built first, then followed the comparator. The clock doubler was built with supporting “dummy” transistor and finger-splitting matching techniques to better assure that the differential circuit was equivalent on each branch [11]. The switches were added once all other

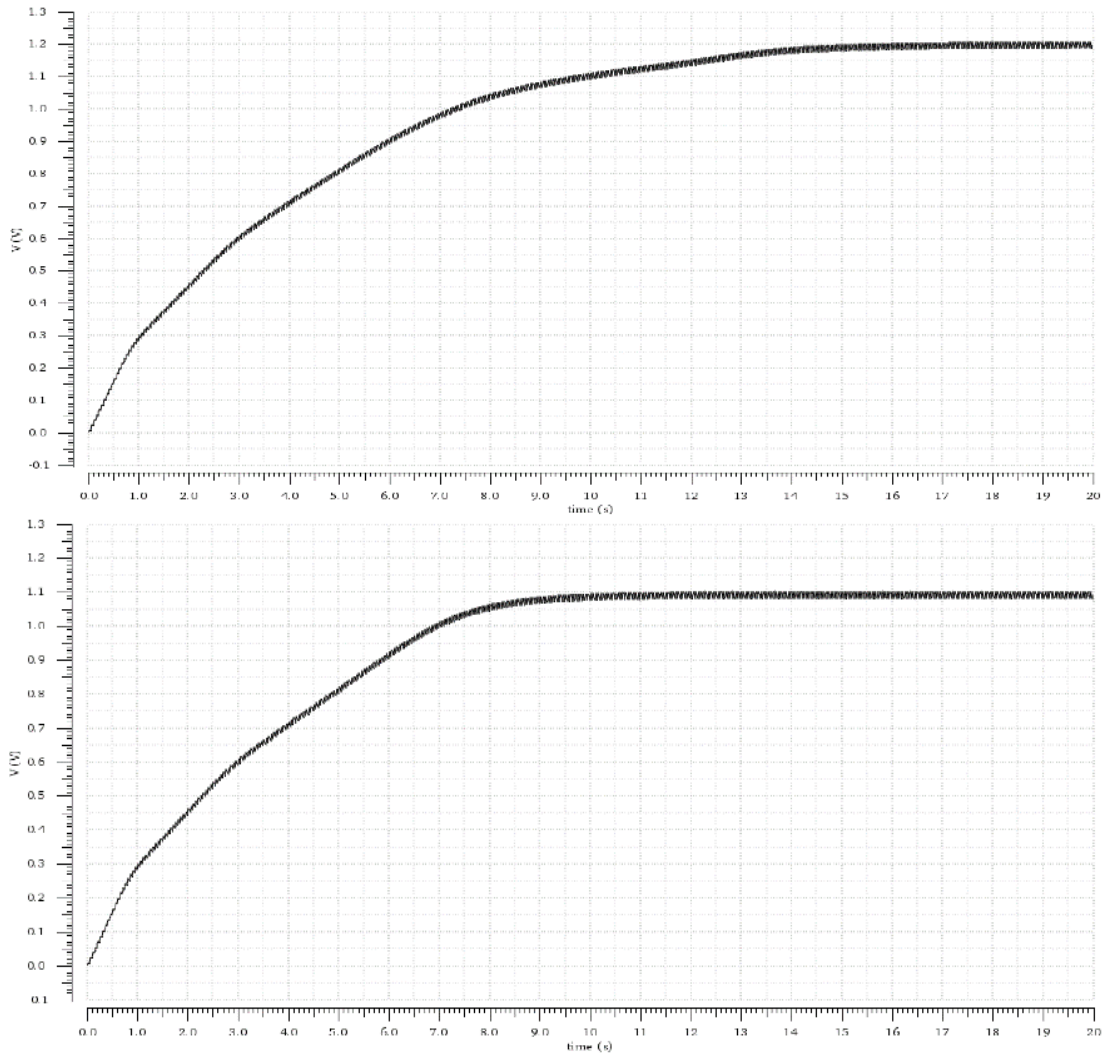


Figure 13. Comparison of output voltage using different architectures.
With comparator (top, $1.2V_o$) and pure SVC-based (bottom, $1.1V_o$).

blocks were created and their Layout vs. Schematic (LVS) was proven to be equal along with the Parasitic Extraction (PEX) of each block.

The layout of the entire three-stage rectifier is shown in Fig. 14. The block uses much smaller components than that shown in [1] due to the smaller CMOS process and the small discrepancies, such as skewing the last inverter in the comparator and wiring the source of the input inverter of the clock doubler to the gate of one of the cross-coupled NMOS devices, have optimized this

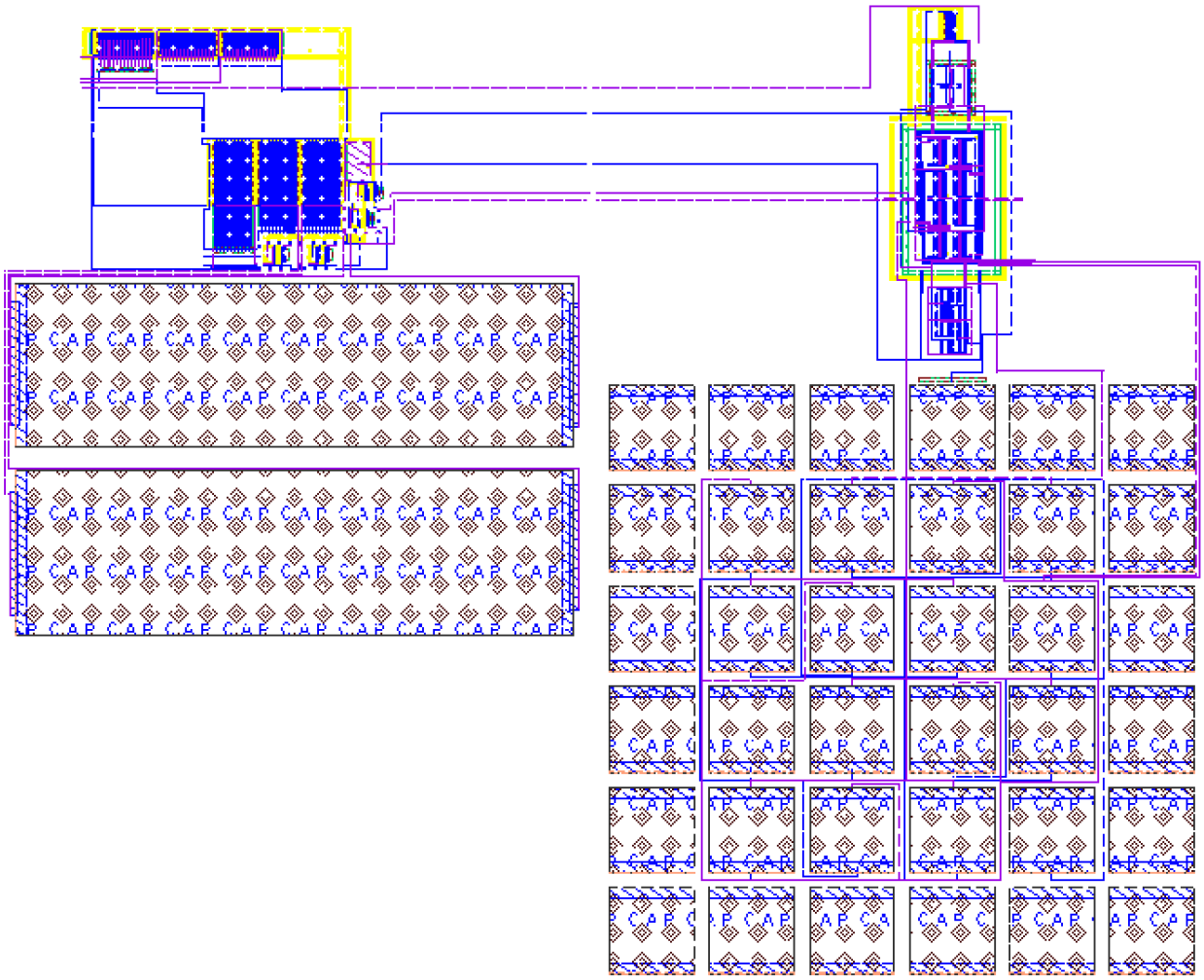


Figure 14. Layout of entire rectifier with all blocks combined.
Clock doubler(right), comparator (bottom-left), and switches (very-top-left)

circuit from its original predecessor. Moreover, this circuit only uses three stages to reach its final value as opposed to the four needed in [1], decreasing the cost (area, masks, money, etc.) and parasitics compared to the original architecture.

The results shown in Fig. 15 show that the average unloaded output level is around 1.2V but once the output is loaded with a current demand greater than a couple of micro-Amperes, the voltage level will drop due to the fundamental reasons stated in Chapter 2 of this work. In order to characterize the output impedance and the equivalent circuit of this rectifier, a parametric analysis

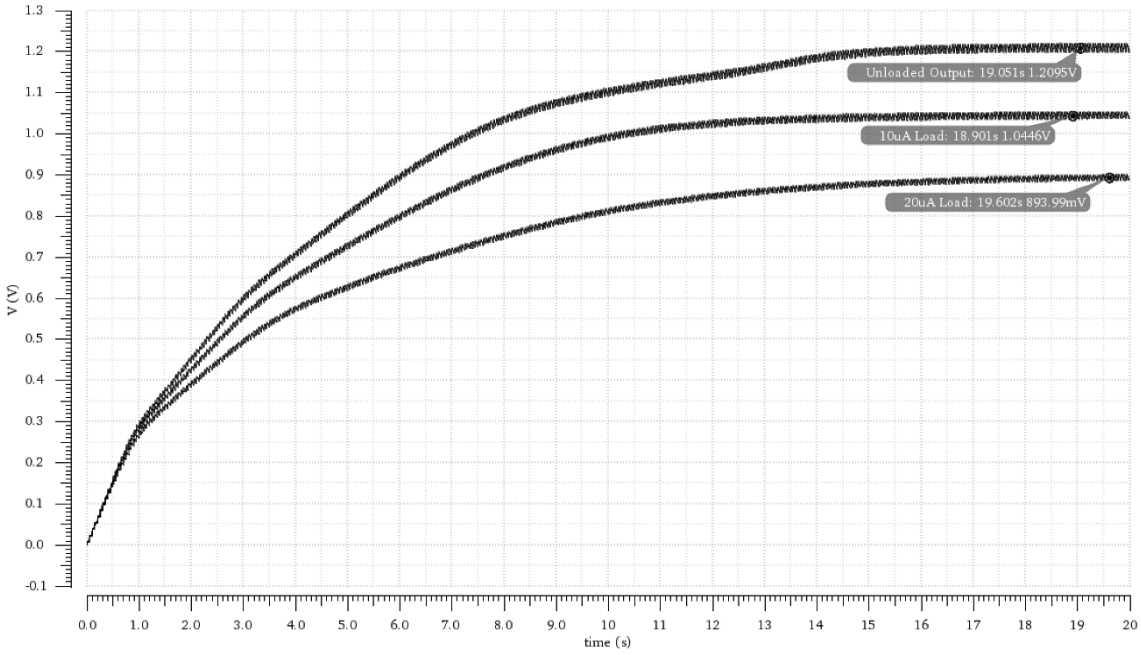


Figure 15. Post-layout simulation of rectifier output.
Equivalent output impedance ~17kΩ.

of the load current was done on this system. Fig. 15 shows the waveforms of three responses to the system. One with no load, one with a 10µA load current, and another with a 20µA load current. As seen in the figure, the differences in the loading conditions cause a drop in the output voltage level around ~165.6mV, corresponding to an output impedance of ~17kΩ (in the equivalent circuit from Fig. 5). Loading this circuit is then made possible so long as the current demand of the system is lower than a couple orders of micro-Amperes with a maximum of about 70µA. According to some of the work done in analog-to-digital converters, it is possible to create successive approximation register analog-to-digital converters (SAR ADCs) on the orders of micro-watts [12], even nano-watts [13]. The power consumption of the transmitter used in [1] could also be scaled down in power consumption to compensate for the supply in this effort. However small, the self-powered rectifier does have some capability to power external circuitry.

CONCLUSION

The work shown in [1] was proven to work on a 0.5µm ON Semiconductor CMOS Process. The rectifier utilized four stages of amplification in order to ramp up the output voltage level that would power the other blocks of the sensor presented in that work. The same was attempted here on a different technology process that changes the shortens the length of the smallest device from 0.6µm to 0.13µm. This change in length is accounted for by simply scaling each of the components by a constant factor. The mobility of holes and electrons is different, the capacitive per oxide area is different, the channel-width modulation of devices in each technology is different. There are very little similarities in device parameters between the 0.5µm process and the 0.18µm process, therefore complete understanding of each passive and active device in the rectifier of [1] is vital.

A re-design of the circuit in [1] was in order to replicate the work in a smaller technology. The smaller technology was able to deliver the maximum DC-voltage allowed by the process in three stages as was proven by the post-layout simulation. The circuit was shown to be able to supply around 70µA, enough to power external circuitry. Along with these simulations, the remaining parts of the sensor system must still be designed in the same CMOS process used in this work. However, power harvesting is the most vital part of the sensor system since without it, none of the other parts can even be used, and it was successfully given priority over the other parts of the SHM.

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