MICROWAVE CHARACTERIZATION OF GAN-ON-SI HETEROSTRUCTURE LOSS AND 2DEG AS A CONDUCTOR

A Dissertation

by

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ABSTRACT

GaN devices have been dubbed ‘the future of high frequency, high power applications’ due to the material properties of GaN that promises a clear advantage over competing technologies. Heteroepitaxial growth of AlGaN/GaN on Si has gained popularity in the recent years due to cost considerations and opportunity of on-chip integration of GaN and Si based devices. This work investigates the microwave properties of the GaN-on-Si substrate and the 2DEG in order to establish their limitations and advantages to set a framework for epitaxial growth and RF design efforts.

In this study the broadband characterization of GaN-on-Si is realized for 6 – 20 GHz frequency range. Dielectric loss of epi-layers is extracted through a differential study of CPWs on different thicknesses of GaN, AlGaN and AlN grown via metalorganic chemical vapor phase deposition (MOCVD) on Si. Changes in effective loss tangent, conductivity and dielectric loss tangent are reported. Where prior reports place the majority of dielectric loss at the Si/AlN interface, it is found that the top GaN layer has a bigger impact on the polarization losses, whereas the AlN is a stronger contributor to the overall conduction losses.

2DEG transmission properties over the 6 - 20 GHz range are also investigated and reported for the first time. Loss of 2DEG as a transmission line is found to be decreasing with frequency. The possible reasons for this loss behavior are examined. 2DEG ohmic contact geometry and its parasitics are also investigated to provide important design parameters for RF device design.

DEDICATION

To my mother, Hafize Berber, the rock of my life, my role model...

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1. INTRODUCTION

1.1. Motivation

GaN devices are overtaking other technologies in many application areas in the last decade since they have been commercially available in 2005. One application area GaN has proven advantageous is efficient optoelectronics. GaN devices have also been dubbed 'the future of high frequency, high power applications' and are preferred over other technologies in this area as illustrated in Figure 1-1. Global GaN RF devices market was valued at $295.6 million in 2015 and is expected to reach $703.4 million by 2020 [1].

Even though the technology is still at its initial development stages with the on-going research focusing on reliable substrate and basic device fabrication and modeling, GaN has already become the preferred technology for high power-high frequency applications, taking over GaAs. GaN HEMT devices can deliver up to 10X power density compared to GaAs PHEMTs, in the range of 10-12 W/mm of gate periphery compared to 1-1.5 W/mm. It has a much larger breakdown voltage of over 100 V compared to 7-20 V achievable by GaAs and higher RF and DC currents due to five times larger sheet charge density. Another advantage over GaAs is its ability to operate over 200 °C channel temperature compared to the 150 °C limit for GaAs.

GaN is already competing with SiC below 2 GHz for base station applications. A recent application area is low noise amplifiers (LNAs). As higher power GaN LNAs can be realized, the front-end circuitry including limiters can be dismissed, improving the achievable noise figure. Broadband amplifiers, high power switches and high power limiters are the other application areas that GaN is gaining popularity in. Advanced R&D

efforts, in terms of application, are focused on higher power, higher efficiency devices, and broadband and high frequency operation at sub-THz frequency range. The advantage of GaN over competing technologies in many application areas comes from its unique material properties.

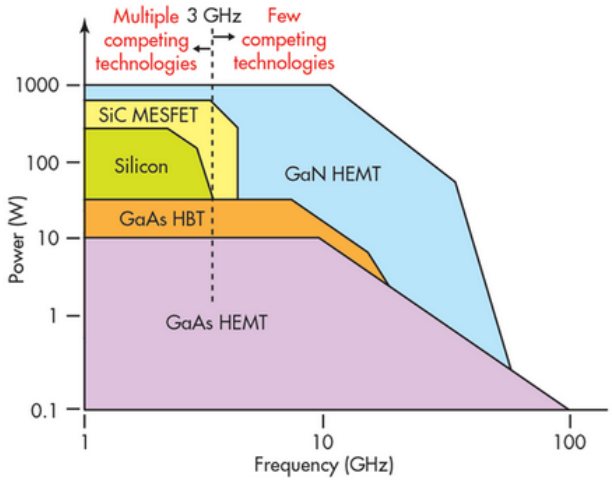


Figure 1-1 Competing technologies for high power – high frequency applications (Courtesy of RFMD)

Main reason for GaN's superiority over competing semiconductor technologies is its wide, direct bandgap. GaN is a wide-bandgap (E_g) material which results in a high critical electric field (E_c) and enables high breakdown voltages. Upper temperature limit of a semiconductor material is theoretically determined by its bandgap, with a rule-of-thumb for maximum temperature in K being equal to 500 times the bandgap energy in eV. Even though other factors such as the material decomposition and technology will affect the device operating temperature, GaN can theoretically operate at higher temperatures than competing semiconductors, improving system efficiency. Combined with high carrier

sheet densities achievable in devices fabricated using nitride heterostructures, GaN devices are able to deliver higher power compared to other technologies. Another advantage of GaN is its lower dielectric constant (ε_r) which enhances the achievable power densities and power added efficiencies of GaN power amplifiers. Its saturation velocity, considerably higher than Si and GaAs, combined with high mobility (μ) also enables higher frequency operation.

Its direct band gap, like the other III-V semiconductors such as InP and GaAs, results in more efficient absorption and emission of light and hence more favorable optoelectronic properties compared to indirect bandgap semiconductors such as Si. GaN is also insensitive to ionizing radiation, like the other wide direct bandgap materials, which makes it suitable for spacecraft solar panels and outer space electronics.

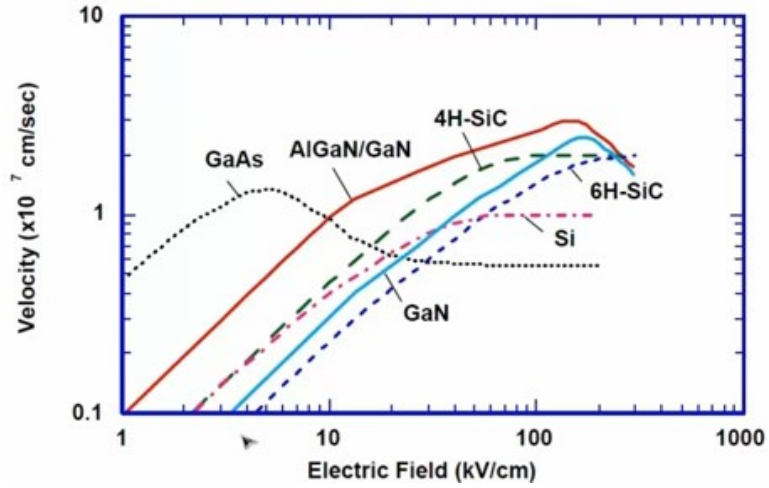
Table 1-1 Material properties of GaN and selected microwave substrates

Material	μ ($cm^2/V \cdot s$)	v_{sat} (10^7 cm/s)	ε_r	E_g (eV)	Bandgap Type	E_c (10^6 V/cm)	K (W/°K·cm)
Si	1350 [2]	1 [2]	11.9 [3]	1.1 [2]	indirect	0.2 [4]	1.5 [2]
GaAs	8500 [2]	2 [2]	12.9 [5]	1.42 [6]	direct	0.4 [4]	0.5 [2]
InP	≤5400 [5]	2.7 [7]	12.5 [5]	1.35 [6]	direct	0.5 [5]	0.68 [5]
3C-SiC	900 [2]	2 [2]	9.6 [2]	2.2 [2]	Indirect	1.2 [2]	4.5 [2]
4H-SiC	≤720 [2]	2 [2]	10 [2]	3.26 [2]	Indirect	2 [2]	4.5 [2]
6H-SiC	≤370 [2]	2 [2]	9.7 [2]	**3.0** [2]	Indirect	2.4 [2]	4.5 [2]
GaN	≥900[1] [2, 4]	2.5 [2, 8]	9.5	3.44 [6]	Direct	3 [4]	1.3[2] [9]
	1700[4] [4]	3.1 [8]					2.2[3] [10]
Diamond	1900 [2]	2.7 [2]	5.5 [2]	5.45 [2]	Indirect	5.6 [2]	20 [2]

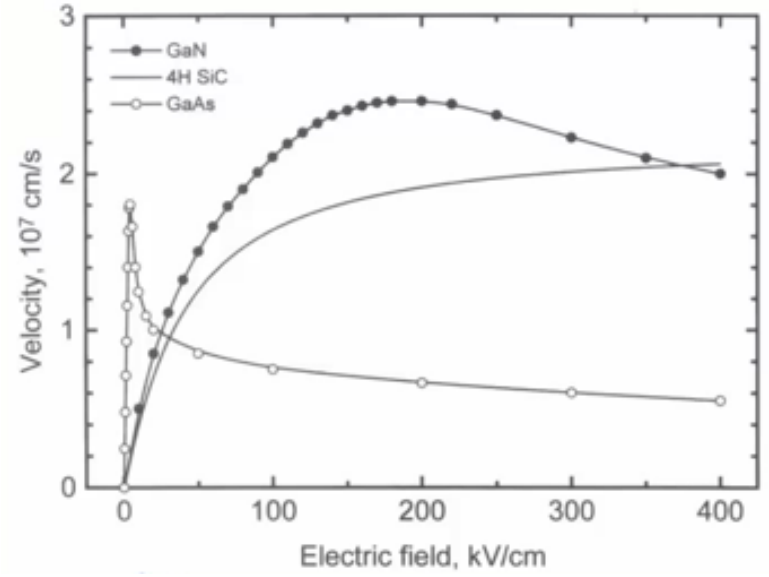
[1] Experimental value for GaN epilayers; theoretical value is higher.
[2] Early model value for bulk GaN
[3] Experimental value for GaN epilayers
[4] AlGaN/GaN heterostructure

Material properties of GaN and some of the competing semiconductors are listed in Table 1-1 for comparison. Electron velocity- electric field characteristics of some of these semiconductors are depicted in Figure 1-2. InP, GaAs and GaN are all III-V compound semiconductors - with elements indium and gallium from group III and phosphorus, arsenic and nitrogen from group V - whereas Si, SiC and diamond are group IV. Diamond has excellent thermal conductivity, superior mechanical and optical properties, and is a good electrical insulator. However, its high cost and scarcity limits its use as the ultimate semiconductor. Si, on the other hand, is the major substrate material due to its low cost and despite its mediocre material properties. Tradeoff between cost and performance has led to GaAs, InP and SiC being used instead of Si for high-power and/or high-frequency applications. Both GaAs and InP have very high electron mobilities compared to other materials which enables high-frequency operation. However, their narrow bandgap limits their critical electric fields and operating temperatures, eliminating their use for high-power applications. Their low thermal conductivity, K, is also a limitation for such applications. SiC with its wider bandgap is a more suitable candidate for such applications but its lower mobility hinders its high frequency operation. SiC has different properties depending on its crystal structure. Among the three main structures listed in Table 1-1, 3C-SiC has the highest electron mobility and saturation velocity owing to its higher symmetry. 6H is most easily prepared and best studied SiC substrate, whereas 3C and 4H are attracting more attention due to their superior electronic properties. Among all these semiconductors except for diamond, GaN combines the most desirable material properties

for high-frequency, high-power applications due to its wider bandgap and moderately high electron mobility.



(a)



(b)

Figure 1-2 Electron velocity- electric field characteristics in (a) logarithmic and (b) linear scale for various substrates

In order to better demonstrate the GaN advantages over the other semiconductor materials, some commonly used figures of merit are presented in Table 1-2, all calculated using the parameters given in Table 1-1. Baliga's Figure of Merit (BFOM) is derived as a measure of power FET's power loss performance, taking into account the minimum resistive loss possible in the drift region of a power FET based on the properties of its substrate semiconductor [11]:

$$\boldsymbol{BFOM = \mu \cdot \varepsilon_r \cdot E_g^3} \tag{1-1}$$

Baliga's high frequency figure of merit (BHFFOM) compares the achievable high-frequency performance of power FETs, again based on their substrate parameters. This revised figure of merit takes into account not only the conduction losses due to the FET on resistance, but also the switching losses at high frequencies due to the charging and discharging of the FET input capacitance [12]:

$$\boldsymbol{BHFFOM = \mu \cdot E_c^2} \tag{1-2}$$

Table 1-2 BFOM and BHFFOM for GaN and selected microwave substrates

Material	Relative μ	Relative ε_r	Relative E_g	Relative E_c	BFOM	BHFFOM	JFOM (THz·V)
Si	1	1	1	1	1	1	0.32
GaAs	6.3	1.08	1.29	2	14.6	25.2	1.27
InP	≤ 4	1.05	1.23	2.5	≤ 7.8	≤ 25	2.15
3C-SiC	0.67	0.81	2	6	4.3	24.1	3.82
4H-SiC	≤ 0.53	0.85	2.96	10	≤ 11.7	≤ 53	6.37
6H-SiC	≤ 0.27	0.82	2.73	12	≤ 4.5	≤ 38.9	7.64
GaN (bulk)	≥ 0.67	0.80	3.13	15	≥16.4	≥150.8	11.94
AlGaN/GaN	≤ 1.26				≤30.9	≤283.5	14.80
Diamond	1.41	0.46	4.95	28	78.7	1105.4	24.06

Another very frequently cited performance metric is the Johnson's Figure of Merit (JFOM) which quantifies the ultimate limit for the amplification and frequency

performance of a transistor based on its semiconductor parameters. It is derived based on a simplified charge transmission model in which the maximum cutoff frequency is determined by the saturated drift velocity of the charge carrier and the minimum transmission distance, which in turn is limited by the dielectric breakdown field, *V/L*. The resulting tradeoff between the maximum allowable applied voltage and the cutoff frequency is given by JFOM, which also defines the maximum achievable values for both voltage and frequency [13]:

$$\boldsymbol{JFOM = V_{max} \cdot f_T = \frac{v_{sat} \cdot E_C}{2\pi}} \qquad (\boldsymbol{Hz \cdot V}) \tag{1-3}$$

Table 1-2 lists the figures of merit calculated according to (1-1) to (1-3). Accordingly, InP and GaAs are not the best technologies for high power applications but they are preferred for high frequency due to their high mobilities. Resistive and switching losses are potentially less with SiC or GaN devices, enabling more efficient power electronics. SiC is generally preferred for low frequency, high power applications due to its low electron mobility. GaN, on the other hand, outperforms all other semiconductors except for diamond according to the figures of merit. Taking into account the cost, GaN is the most promising semiconductor for high power and high frequency applications.

Figure 1-3 shows the Johnson's Figure of Merit for GaN, InP and Si, illustrating the theoretical limits for the breakdown voltage – cutoff frequency of these semiconductor materials. Same figure also includes the state-of-art devices currently realized using these three semiconductors as well as InAs, SiC, SiGe and GaAs. High power, low frequency devices are generally realized with SiC due to its wide bandgap but lower mobility whereas InP with narrower bandgap but high mobility is preferred for the higher frequency

lower power devices. GaN devices are able to achieve higher power performance at higher frequencies and have the highest theoretical limit compared to the other semiconductor technologies as can be observed in Figure 1-3.

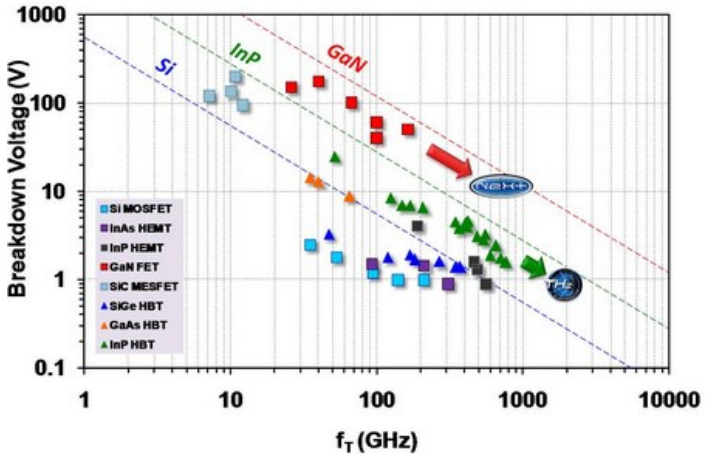


Figure 1-3 Johnson's Figure of Merit and current state of performance for GaN and competing technologies (Courtesy of DARPA NEXT).

Another advantage of GaN devices that is not captured in the figures of merit, is its high vertical and lateral scalability, again due to its material properties. GaN devices normally utilize 2-dimensional electron gas (2DEG), a thin sheet of electrons that spontaneously exists at nitride semiconductor interfaces due to polarization, as the device channel. Generally two nitride layers are interfaced in order to enhance the 2DEG, with the chemical composition and thickness of the layers determining the electron density. 2DEG is buried within the heterostructure at the nitride interface and is confined to a thickness of couple of nanometers, determined by its density. Example of such a heterostructure and the 2DEG formed at its interface are illustrated in Figure 1-4. The

device is formed around the already existing 2DEG channel / conductor area, by forming ohmic contacts to the 2DEG at the input and output terminals and isolating the device by destroying the 2DEG around it through either etching or implantation. The vertical device dimension is very well confined and in a few nanometer range due to the nature of 2DEG. The horizontal device dimensions are only limited by lithography and isolation process; nanometer wide 2DEG channels can be fabricated through electron beam (e-beam) lithography and reactive ion etching (RIE).

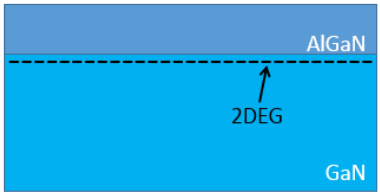


Figure 1-4 Illustration of a nitride heterostructure and the 2DEG formed at the heterostructure interface.

The GaN technology is still at its initial development stages with the on-going research focusing on reliable substrate and basic device fabrication and modeling. Unique devices that can be implemented utilizing the material properties have not yet been fully explored. The integration efforts have been around implementing previous technologies developed for GaAs, which are not suitable for frequencies over 100GHz - the frequency range GaN devices promise to operate at due to their material properties and scalability. One impeding issue, especially for the sub-THz operation range and broadband applications, is the availability of surrounding circuitry, most important of which is transmission lines, that can operate at these frequencies with sufficiently low attenuation and dispersion and also

can accommodate high power densities. In this research, 2DEG is investigated as a possible high-frequency interconnect and conductor material. Scalability and high mobility of 2DEG suggests that it can be employed as a transmission medium, circumventing some of the issues related to high frequency, high power operation of metals. 2DEG as transmission line in future GaN MMICs would also minimize the use of ohmic contacts, with a lot of reliability, repeatability and parasitics issues, in high-power, high-frequency circuitry.

GaN devices are generally fabricated using templates with heteroepitaxial growth due to the immaturity and high cost of device quality native substrates. Although early commercial epitaxial growth efforts used sapphire and SiC substrates, high quality GaN growth on high resistivity silicon (Si) substrates has become more proliferate in recent years. According to [1], GaN-on-SiC is currently used in over 95% of the commercially available GaN devices. GaN-on-SiC technology has developed much faster than GaN-on-Si and can provide high performance even if at a high cost. Si has gained popularity as a GaN substrate due to its low cost and opportunity of on-chip integration of GaN and Si based devices [14].

Even though many devices on GaN-on-Si templates with good performance and device reliability have been reported, including heterostructure field-effect transistors (HFETs) [15, 16] material quality is still known to limit high power and high frequency performance of Si-based GaN devices. Research efforts have focused on relating several performance degradations in GaN HFETs to threading dislocations (TD) in the epitaxial layers. Figure 1-5 shows the cross-sectional SEM image of a GaN HFET on Si substrate and also the

TEM image of the layers used to grow high quality GaN-on-Si. Dislocation density throughout various epi-layers, especially in the insulating AlN nucleation layer, is observed in the TEM image. Dislocations are reported to cause a decrease in free carrier concentration, transverse mobility degradation, and leakage currents [17-21], especially for TD densities approaching 10^9 cm^{-2}. One study based on current gain – frequency simulations for different TD densities suggests that frequency behavior of GaN HEMTs is more strongly affected by threading dislocations than its DC behavior [18].

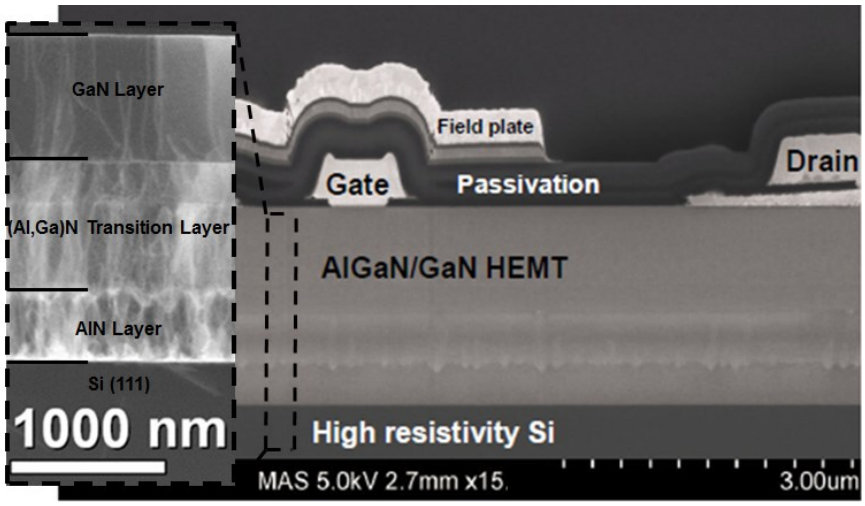


Figure 1-5 Cross sectional SEM image of a GaN HFET on Si substrate [22] and TEM image of a GaN-on-Si template.

Even though the effect of GaN-on-Si material quality, especially in terms of TD densities, on GaN device performance is well documented, there is insufficient data on material parameters that are required for circuit design of GaN-on-Si. Si substrate and the epi-layers are assumed to be insulating or semi-insulating for design purposes, leading to

subpar performance. One broadband characterization of CPWs on GaN-on-Si reports higher microwave losses than expected for the multilayer substrate with insulating/semi-insulating epi-layers on 10k Ω-cm Si [23]. This extra loss is attributed to a parasitic conductive layer inside silicon at the AlN/Si interface [24]. However, the AlN layer grown on Si (111) is highly defective and has the potential to provide significant scattering and trap centers that can lead to RF loss. In particular, the top GaN-on-Si epi-layer have the potential to more strongly contribute to the RF loss because of its close proximity to the device. A more thorough study of GaN-on-Si epilayers and their contribution to overall dielectric loss is needed given their observed TD densities, rather than lumping losses into a single effective layer in the substrate. In this study, we systematically examine the contribution of the Si substrate and the epi-layers to determine and quantify their individual contributions to microwave loss mechanisms.

1.2. Organization of This Dissertation

In order to highlight the issues concerning high-frequency operation and integration of GaN devices and to give a basic understanding of the proposed solution, first the basic device physics and the unique properties of the 2DEG will be explained. Current progress in terms of device performance and integration and the issues to be resolved will be summarized. The problems with current interconnect technologies at sub-THz and THz range will be explained in terms of limitations imposed by transmission line theory and thin film fabrication.

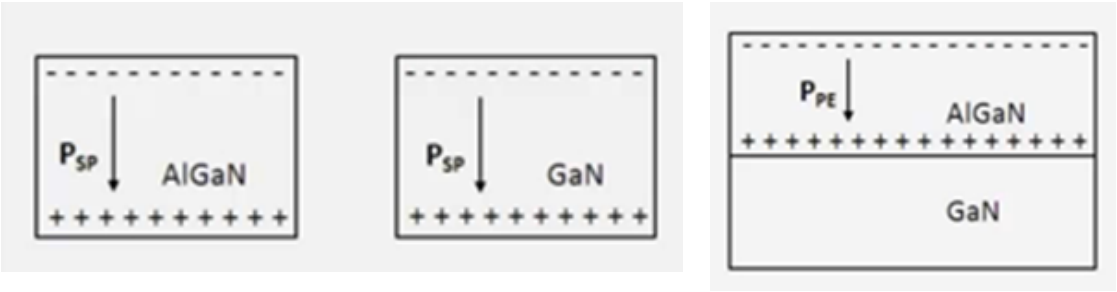
Test structures and masks created for RF characterization of GaN-on-Si substrates and 2DEG transmission lines are detailed next. Fabrication of the samples and development of electrically insulating SiN PECVD recipe are also explained. After RF Measurement setup and data extraction methodology is described, substrate and 2DEG RF measurement results are presented in the last two sections.

2. BACKGROUND

2.1. Fundamental GaN Physics

GaN-based devices rely on inherent polarization properties of III-Nitride material systems and the resulting formation of a well-confined high mobility, high carrier density carrier sheet named ***2-dimensional electron gas (2DEG)***.

Due to the asymmetric crystal structure and resulting dipole formation, III-Nitrides have an inherent spontaneous polarization field in an unstrained crystal as depicted in Figure 2-1 (a). When two III-Nitrides of different lattice constants are combined, the nitride films are strained, leading to the formation of an additional piezoelectric polarization field as shown in Figure 2-1 (b).



(a) (b)

Figure 2-1 (a) Spontaneous polarization (b) piezoelectric polarization

Total polarization field and additional heterostructure engineering result in the 2DEG charge sheet formation at the heterojunction. This well-confined sheet charge is used as the conduction channel in GaN-based devices. A basic high-electron mobility transistor (HEMT) structure and the 2DEG used as the transistor channel are depicted in Figure 2-2.

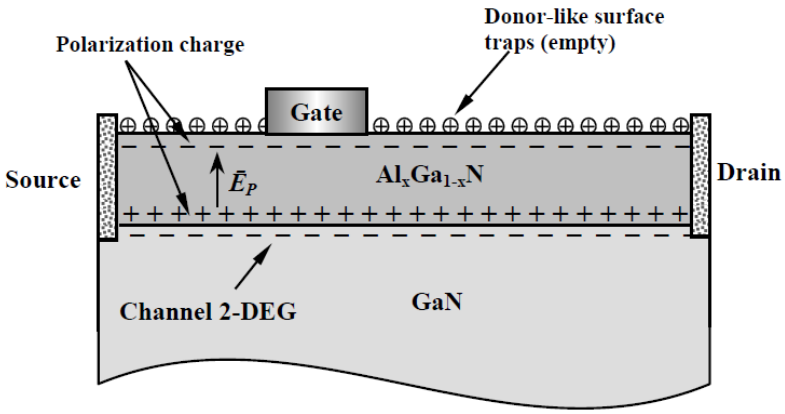


Figure 2-2 AlGaN/GaN HEMT Schematics

2DEG is a well-confined sheet of charge with high mobility and high carrier density. So far, the main focus and research on 2DEG has been in terms of utilizing it as a conduction channel in a transistor. This research focuses on investigating other implementation areas for this metal-like thin film while proposing solutions to some inherent problems with the GaN transistors and their integration, especially for high-frequency operation. First, known properties of 2DEG will be summarized and then the current situation of GaN systems and future challenges will be addressed.

2.2. 2DEG Properties

As mentioned previously, 2DEG has been mainly employed as a conduction channel in GaN-based transistors and majority of 2DEG-related data and analysis comes from characterization via such structures or optical measurements of un-patterned substrates.

Sheet carrier concentration, mobility and resistivity of 2DEG are generally estimated from the data compiled by Ambacher [25]. The parameter that can be engineered through

fabrication is the *sheet carrier concentration, n_s*. As depicted in Figure 2-3, n_s value depends on the thickness and composition of the top AlGaN layer. *Aluminum (Al) mole fraction x* of $Al_xGa_{x-1}N$ is the main factor in adjusting n_s. The AlGaN thickness also has an effect on the concentration, increasing n_s for thicker AlGaN layers.

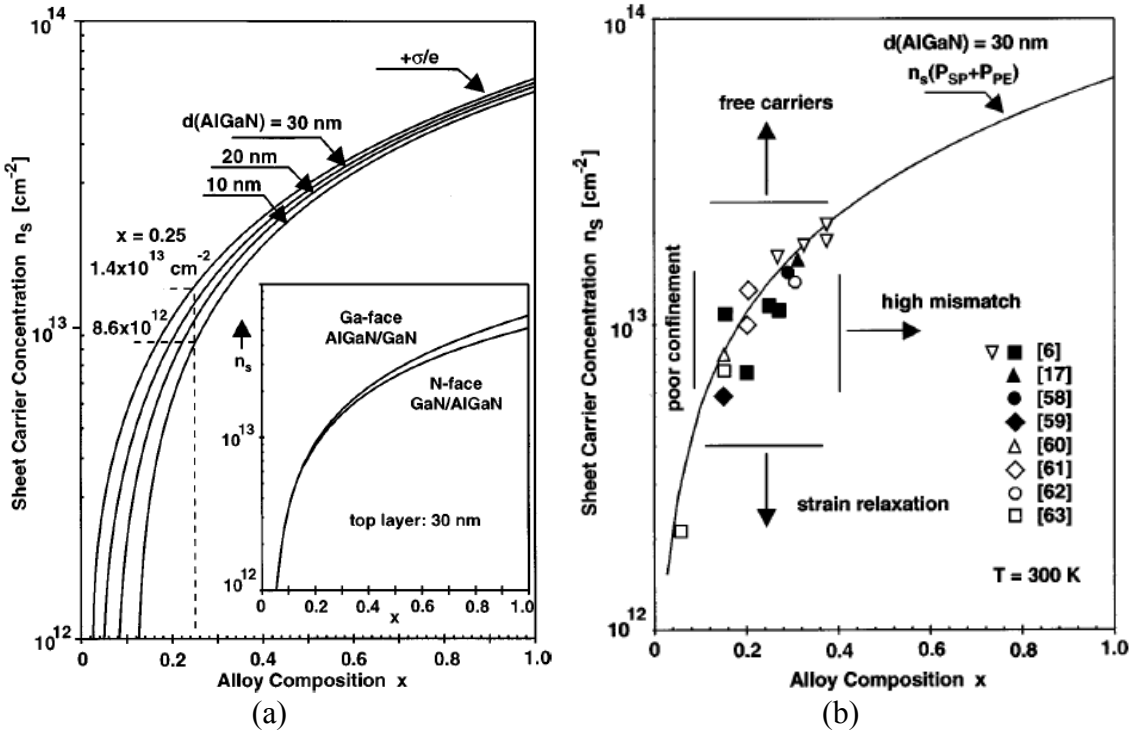
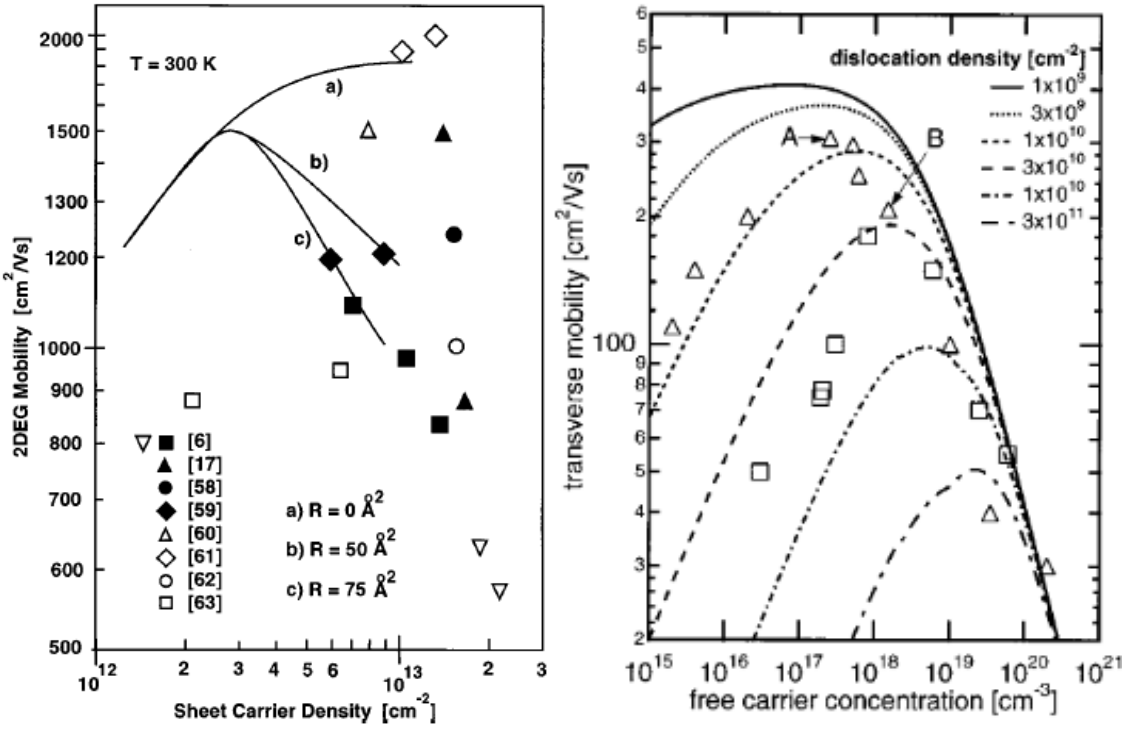


Figure 2-3 2DEG Sheet Carrier Concentration vs. Alloy composition (a) n_s at Ga-face (GaN/)AlGaN/GaN or N-face GaN/AlGaN(/GaN) interface for different AlGaN thicknesses, (b) Calculated and measured n_s vs. of the 30nm thick AlGaN [25]

The electron mobility of the 2DEG is mainly determined by its carrier concentration. Mobility as a function of n_s is plotted in Figure 2-4(a). The plot also shows the variation of mobility as a function of AlGaN/GaN interface roughness. The plotted mobility only takes into account the drift mobility of electrons which results in discrepancy between the

measured and calculated values, especially for high carrier densities. A supplemented mobility model including the effects of lattice scattering and Coulomb scattering at charged dislocation lines is shown in Figure 2-4(b).



(a) (b)

Figure 2-4 2DEG mobility vs. sheet carrier density (a) Calculated (drift mobility) and measured 2DEG mobility for AlGaN/GaN interface roughnesses [25] (b) Total mobility calculated including scattering mechanisms for dislocation densities [26].

The most important point from Figure 2-4(a) is the decrease in 2DEG mobility with increase in 2DEG carrier density, especially for high 2DEG carrier densities, which is explained by reduced channel dimensions (~2 nm) and increased scattering. There exists a limit for maximum achievable (μ_s x n_s) product for a given AlGaN composition. This also limits the minimum achievable *sheet resistance* R_s as depicted in Figure 2-5. The

calculated sheet resistivity using the drift mobility lies between 300 Ω and 190 Ω for Al contents between 0.2 and 0.3 but the lowest reported values are between 400 Ω and 200 Ω, respectively, due to interface roughness scattering and dislocation scattering [25].

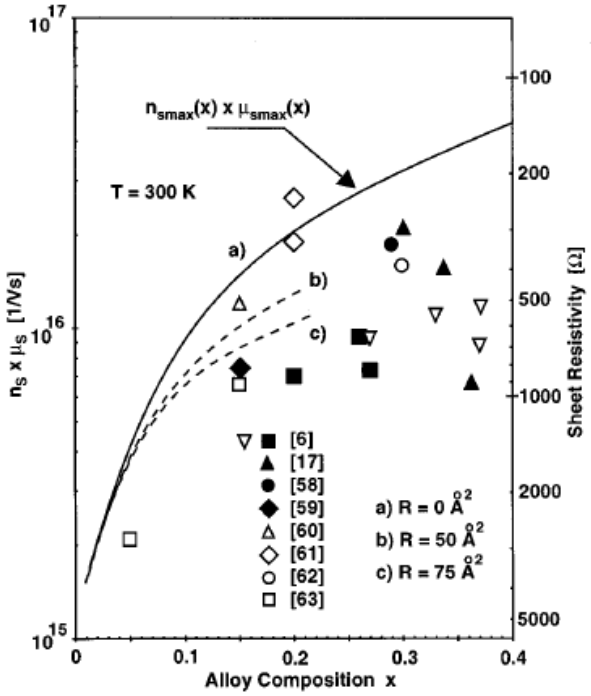


Figure 2-5 Calculated and measured 2DEG $\mu_s \times n_s$ products and sheet resistivities for different AlGaN/GaN interface roughnesses [25].

The equations and approximations for calculating the maximum sheet carrier concentration [25] for a given thickness and alloy composition and mobility [26] are not included here for the sake of brevity. It is important to note that:

- There is a trade-off between μ_s and n_s,
- μ_s x n_s product, hence, minimum R_s, is determined by the AlGaN layer,
- Reported R_s values lie between 400 Ω and 200 Ω due to scattering effects,

- Equations for 2DEG mobility including scattering effects have been developed,
- There is no known data or model on high-frequency behavior of 2DEG.

2.3. GaN Devices and MMICs: Achievements and Roadblocks

2DEG, whose properties are explained in the previous section, is one of the main reasons for the enhanced performance of GaN devices but it also poses one of the roadblocks. 2DEG is buried under a dielectric layer whose composition determines its main properties. Therefore, it has been proven difficult to engineer a well-defined, low resistance ohmic contact to 2DEG without altering the 2DEG itself.

The common practice for 2DEG ohmic contact fabrication is high temperature anneal of a metal stack consisting of Ti/Al/x/Au, where x can be Ti, Ni, Pt, Mo or Pd. The high temperature anneal (~850 C) results in 'low' contact resistance but causes the metals to diffuse into the channel area. The lack of a well-defined contact region is one of the main challenges to short-channel devices for high-frequency operation.

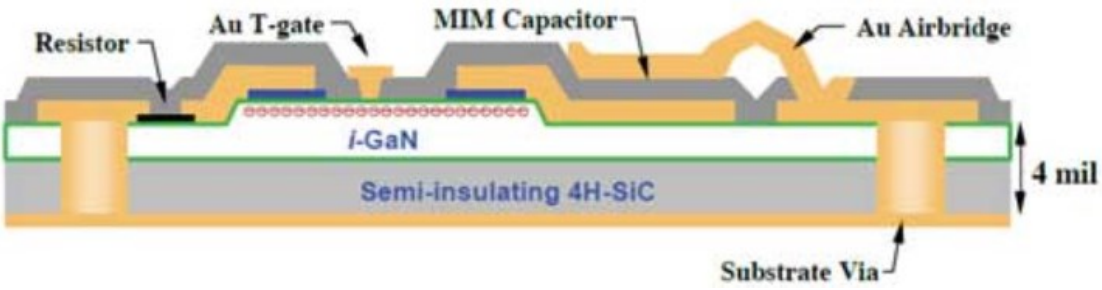
Another contact-related challenge is the high resistance of these contacts. An average contact resistance of 0.5 Ω-mm for common 2DEG ohmic contacts can contribute as much as 50% to the total on-resistance of the transistor. Table 2-1 shows the metal stacks and contact resistances for some commercial and research applications. Research efforts have been focused on achieving non-alloyed low resistance ohmic contacts, however, these approaches introduce further complications in terms of device performance and fabrication.

Table 2-1 Some ohmic contacts used in industry (IMEC, TriQuint) and research

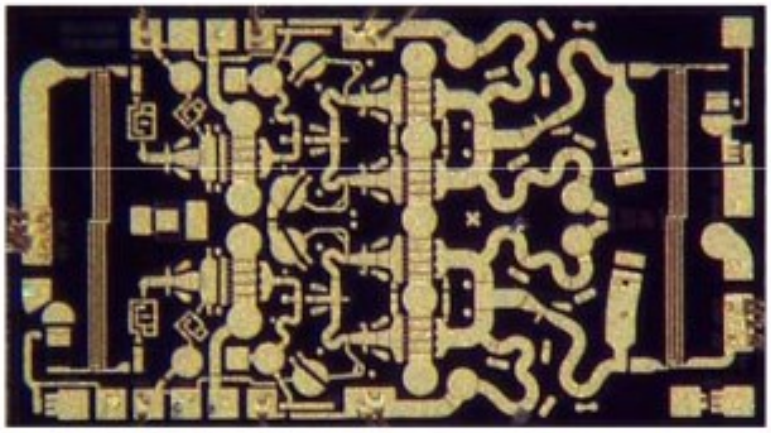
	IMEC	TriQuint	Chalmers T.U.	Our Group
Metal Stack	Ti/Al/Pt/Au	Ti/Al/Mo/Ti/Au	Ti/Al/Ni/Au	Ti/Al/Ni/Au
R_c [Ω-mm]	0.8	0.5	0.3 - 0.4	0.54

Commercial GaN products and state-of-art high power-high frequency devices available to date perform below the theoretical limits mainly due to device reliability and parasitics issues – one of which is the ohmic contact fabrication explained previously. Substrate and device reliability and parasitic reduction are some of the major research topics both in industry and in the academia. Concurrent with the on-going research to improve GaN performance, are the efforts for device integration. Using existing MMIC processes, GaN MMICs have been fabricated and are commercially available. A typical GaN MMIC cross-section and layout are depicted in Figure 2-6 (a) and (b), respectively.

GaN MMIC process employs typically two and maximum three metal layers for interconnects and passives. Dielectric layers such as SiN and BCB are used for passivation, capacitor dielectric, and encapsulation. Component connections and inductors are realized through air-bridges. In order to reduce parasitics, substrate-via technology and stripline transmission is used for the current operation frequencies up to 20 GHz.



(a)



(b)

Figure 2-6 (a) Typical GaN MMIC cross-section from Cree RF Products and (b) layout of a GaN power amplifier (TGA1135B) MMIC from TriQuint

The level of integration in GaN MMICs is limited not only due to cost, design difficulty and fabrication complexity but also due to reliability. Cumulative effect of process variation with each additional fabrication step is detrimental especially at high frequency operation where careful design and several design cycles are required for parasitic reduction and estimation, and where error margins are very tight. Reduction in required fabrication steps can provide invaluable improvement in terms of GaN MMIC performance and enable higher levels of integration. The GaN-based interconnects and other device possibilities proposed in this research could contribute to reduction in fabrication steps as these devices would be fabricated at the same step as the device channel.

As reliability and performance issues with GaN devices are resolved, the operation frequencies of GaN MMICs will move beyond the current value of 20 GHz. Stripline technology employed by current GaN MMICs will be replaced by coplanar waveguides

(CPW) at higher frequencies as they can provide superior attenuation and dispersion characteristics. GaN HEMTs can theoretically operate at sub-THz and THz frequencies given the estimated cut-off frequency – breakdown voltage product of 5 THz-V. The employment of planar transmission lines, including CPWs, will be problematic at these frequencies due to limitations which will be explained in the next two sections.

2.4. Interconnects and High Frequency-High Power MMICs

For high frequency applications up to 100 GHz range, coplanar waveguides (CPW) rather than stripline transmission lines are preferred due to their lower dispersion properties as mentioned in the previous section. However, at frequencies over 100 GHz, the dispersion and attenuation of even CPWs become too large to be effectively used in high performance MMICs.

One of the main problems with coplanar transmission lines at sub-THz range ($f > 300$ GHz) is loss due to radiation. Attenuation at these frequencies is mainly due to shock wave radiation into the substrate because of the permittivity mismatch between the substrate and the air resulting in a higher propagation speed on the line than the phase velocity in the substrate [27]. It has been demonstrated experimentally that the resulting radiation loss dominates the overall loss over 200 GHz compared to conductor and dielectric losses for coplanar transmission lines of 5 μm width [28].

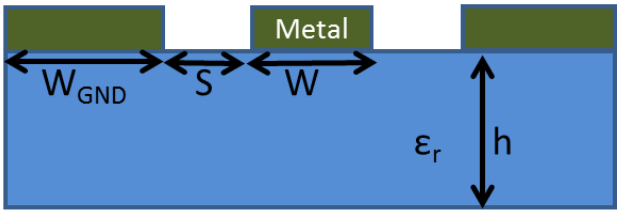


Figure 2-7 CPW cross-section on a substrate of height *h* and dielectric constant ε_r

The attenuation due to radiation loss of a CPW, including the effect of radiation angle and the frequency dependence of effective dielectric constant, is given as [29]:

$$\alpha_{radiation} = \left(\frac{\pi}{2}\right)^5 2 \left(\frac{\left(1 - \frac{\varepsilon_{eff}(f)}{\varepsilon_r}\right)^2}{\sqrt{\frac{\varepsilon_{eff}(f)}{\varepsilon_r}}} \right) \frac{(W + 2S)^2 \varepsilon_r^{3/2}}{c^3 K'(k) K(k)} f^3 \qquad (2\text{-}4)$$

where

$$\cos(\Psi) = \sqrt{\frac{\varepsilon_{eff}(f)}{\varepsilon_r}} \qquad (2\text{-}5)$$

shows the dependence of radiation angle Ψ, of the electromagnetic shock wave emitted into the substrate, on the mismatch between the effective permittivity of the coplanar structure, ε_{eff}, and the permittivity of the dielectric substrate, ε_r. $\alpha_{radiation}$ depends critically on the radiation angle as can be observed from (2-4). (1.1) is expected to be valid for geometries with $0.1 < W/S < 10$, $h > 2S$, and $\lambda > W + 2S$ [29].

The empirical formula used for the frequency-dependent effective permittivity of a CPW is:

$$\sqrt{\varepsilon_{eff}(f)} = \sqrt{\varepsilon_q} + \frac{\sqrt{\varepsilon_r} - \sqrt{\varepsilon_q}}{\left(1 + a\left(\frac{f}{f_{te}}\right)^{-b}\right)}, \tag{2-6}$$

where the quasi-static effective permittivity, ε_r, assuming equal distribution of fields in air and in the substrate is:

$$\varepsilon_q = \frac{\varepsilon_r + 1}{2}, \tag{2-7}$$

and the cutoff frequency for TE_1 mode, f_{re}, is:

$$f_{te} = \frac{c}{4h\sqrt{\varepsilon_r - 1}}. \tag{2-8}$$

The parameter b (≈1.8) is independent of geometry and a is related to geometry as:

$$\log(a) \approx u \log(W/S) + v, \tag{2-9}$$

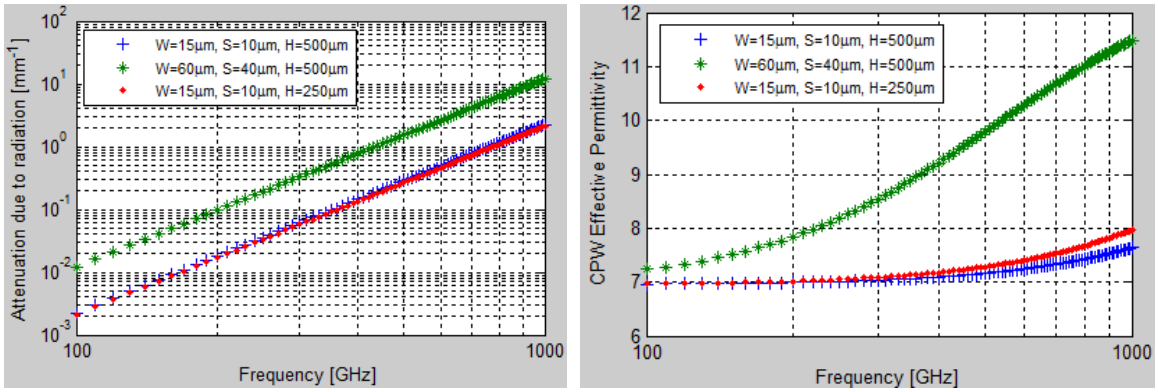
where

$$u \approx 0.54 - 0.64q + 0.015q^2,$$

$$v \approx 0.43 - 0.86q + 0.54q^2,$$

$$q = \log(W/h).$$

In these equations, W is the center conductor width, S is the separation between the center conductor and the ground conductors, h is the substrate height as depicted in Figure 2-7. $K(k)$ is the complete elliptic integral of the first kind with $k = W / (W + 2S)$, and $K'(k) = K(\sqrt{1-k^2})$. Frequency-dependent effective permittivity given by (2-6) is verified to be accurate within 5% for $0.1 < W/S < 5$, $0.1 < W/h < 5$, $1.5 < \varepsilon_r < 50$, and $0 < f/f_{te} < 10$ [30].



(a) (b)

Figure 2-8 (a) Radiation loss and (b) CPW effective permittivity variation with frequency for different S, W and H (ε_r = 12.9)

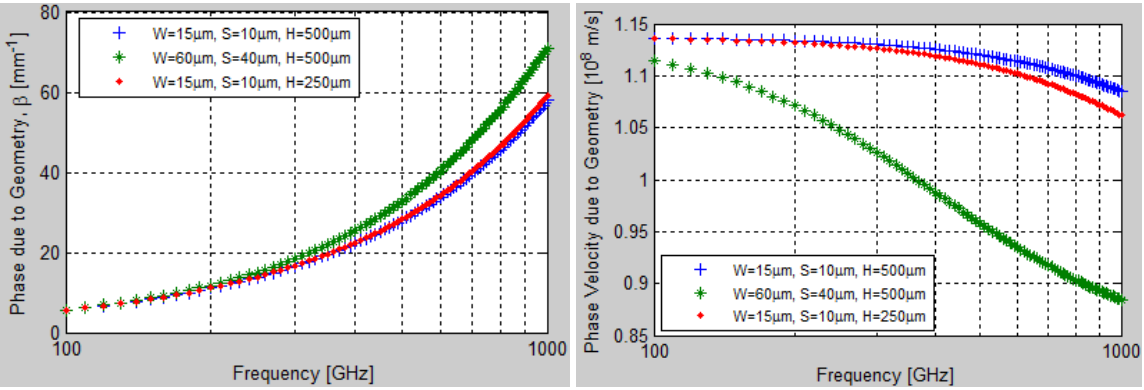
Radiation loss and CPW effective permittivity as given by (2-4) and (2-6) are plotted in Figure 2-8 (a) and (b), respectively, for different CPW dimensions and substrate thicknesses. The plot clearly indicates the need to reduce CPW dimensions in order to reduce radiation loss at high frequencies. The substrate thickness has a minimal effect on the $\alpha_{radiation}$ but does affect $\varepsilon_{eff}(f)$. According to Figure 2-8 (b), frequency variation of $\varepsilon_{eff}(f)$ is dramatically increased for larger CPWs.

One of the most important implications of effective permittivity variation with frequency is the pulse distortion due to dispersion, calculated from the Fourier transform of the time-domain waveform at a distance z:

$$\boldsymbol{V(f,z) = V(f,0)e^{-i\beta(f)z}} \qquad (2\text{-}10)$$

where the frequency dependent phase *β(f)* is given by [30]:

$$\boldsymbol{\beta(f) = 2\pi\frac{f}{c}\sqrt{\varepsilon_{eff}(f)}.} \qquad (2\text{-}11)$$



(a) (b)

Figure 2-9 (a) Phase and (b) Phase velocity variation with frequency for different S, W and H (ε_r = 12.9)

CPW phase and phase velocity, given by $v_{ph} = \omega/\beta(f)$, are plotted in Figure 2-9 (a) and (b), respectively. Increase in CPW $\varepsilon_{eff}(f)$ with frequency results in slower propagation of high frequency components of a broadband signal than the low frequency components, leading to dispersion. As apparent from the plots, large CPW dimensions not only increase attenuation but also dispersion with increasing frequency.

CPW characteristic impedance, given by (2-12) [31], is also a function of effective permittivity and becomes strongly frequency dependent for large CPW dimensions as depicted in Figure 2-10.

$$\boldsymbol{Z(f) = \frac{120\pi}{\sqrt{\varepsilon_{eff}(f)}} \frac{K'(k)}{4K(k)}.} \qquad (2\text{-}12)$$

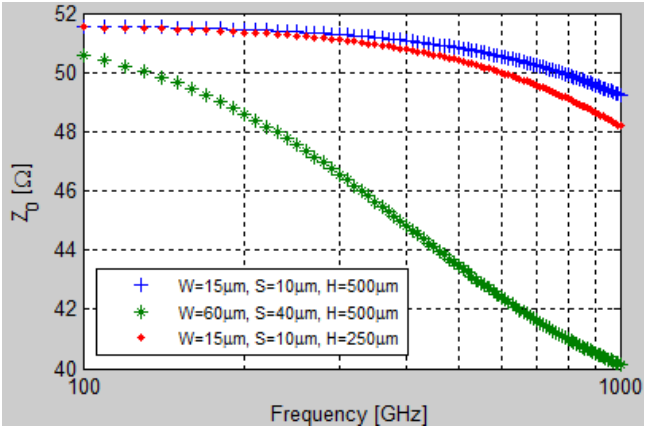


Figure 2-10 Characteristic Impedance variation with frequency for different S, W and H (ε_r = 12.9).

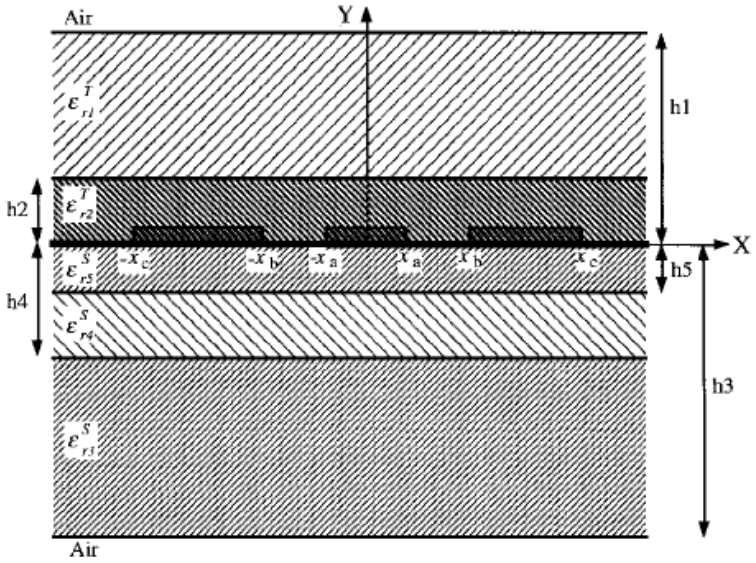


Figure 2-11 CPW structure for quasi-static effective permittivity (ε_q) calculation [31].

Note that (2-6) and the plots do not include the effect of finite CPW ground planes. Also, $\varepsilon_q = (\varepsilon_r + 1)/2$ is used for the CPW $\varepsilon_{eff}(f)$ calculation in (2-6), assuming equal field distribution in air and in the substrate. In MMICs, the CPW transmission lines are not in

direct contact with air but buried under layers of dielectric passivation/insulation layers and the substrates are not of single material. An improved analytical expression for ε_q, taking into account the multilayer structures and the finite dimensions of the dielectrics and ground planes as depicted in Figure 2-11, is given as [31]:

$$\boldsymbol{\varepsilon_{q,CPW} = \frac{C_{CPW}}{C_0} = \frac{C_0 + C_1 + C_2 + C_3 + C_4 + C_5}{C_0}} \tag{2-13}$$

where

$$\boldsymbol{C_0 = 4\varepsilon_0 \frac{K'(k)}{K(k)} \quad \text{and} \quad k = \frac{x_c}{x_b}\sqrt{\frac{x_b^2 - x_a^2}{x_c^2 - x_a^2}},} \tag{2-14}$$

$$\boldsymbol{C_i = 2\varepsilon_0\left(\varepsilon_{r_i} - \varepsilon_{r_{i-1}}\right)\frac{K'(k_i)}{K(k_i)} \quad \text{and}} \tag{2-15}$$

$$\boldsymbol{k_i = \frac{\sinh\left(\frac{\pi x_c}{2h_i}\right)}{\sinh\left(\frac{\pi x_b}{2h_i}\right)}\sqrt{\frac{\sinh^2\left(\frac{\pi x_b}{2h_i}\right) - \sinh^2\left(\frac{\pi x_a}{2h_i}\right)}{\sinh^2\left(\frac{\pi x_c}{2h_i}\right) - \sinh^2\left(\frac{\pi x_a}{2h_i}\right)}}.}$$

Note that for C_1 and C_3, the overlying dielectric is air and $\varepsilon_{r_{i-1}} = 1$. (2-13) takes into account the concentration of field lines in a dielectric of finite thickness relative to the surrounding dielectrics and enables more realistic assessment of $\varepsilon_{eff}(f)$.

$\varepsilon_{eff}(f)$ and $\alpha_{radiation}$ are plotted using ε_q and $\varepsilon_{q,cpw}$ for comparison in Figure 2-12 (a) and (b) for different SiN (ε_r = 7) thicknesses covering a CPW structure on a 500 μm thick substrate of ε_r = 12.9. Note that ε_q does not include the effect of this SiN layer. As shown in Figure 2-12, presence of such an SiN layer, which is typical in a GaN MMIC, increases $\varepsilon_{eff}(f)$, improves its variation with frequency, and as a result lowers the radiation loss.

Frequency dependence of characteristic impedance is also reduced as depicted in Figure 2-12(c).

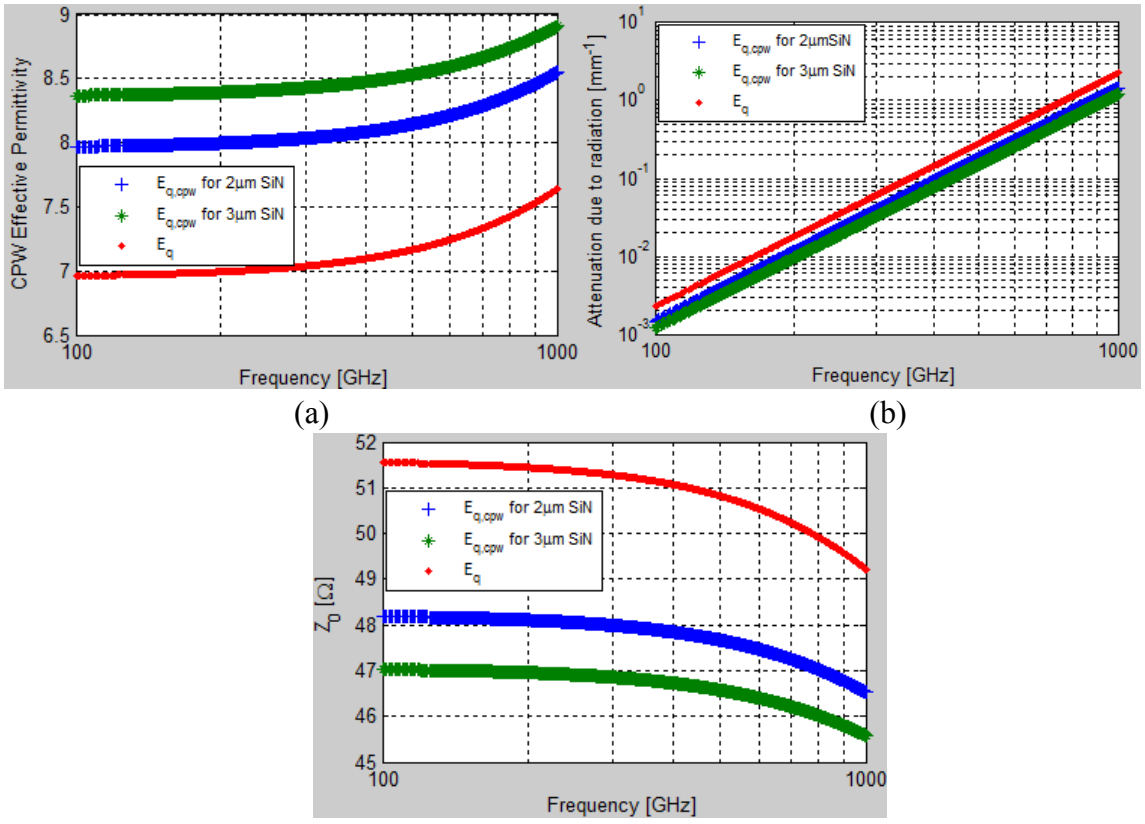


Figure 2-12 (a) $\varepsilon_{eff}(f)$, (b) Radiation loss and (c) characteristic impedance calculation using ε_q vs. $\varepsilon_{q,cpw}$ and the effect of dielectric over CPW ($\varepsilon_r = 12.9$, $W = 15$ µm, $S = 10$ µm)

The equations and results presented so far suggest that there are two approaches to reducing the radiation loss and dispersion that dominate signal transmission at high frequencies: scaling down CPWs and/or minimizing dielectric mismatch $\varepsilon_{eff}(f)/\varepsilon_r$. Examples of the latter approach are presented below and the CPW miniaturization is discussed in the next section in terms of material and fabrication limitations.

In order to minimize dielectric mismatch, a NASA-led research [32] proposes coplanar striplines sandwiched between semi-insulating GaAs substrates as depicted in Figure 2-13. This structure aims confining the field lines in a homogenous dielectric medium in order suppress radiation loss and reduce the overall attenuation at high frequencies to that of skin effect. A bandwidth improvement of up to 110GHz instead of 20GHz is achieved with the GaAs 'superstrate'.

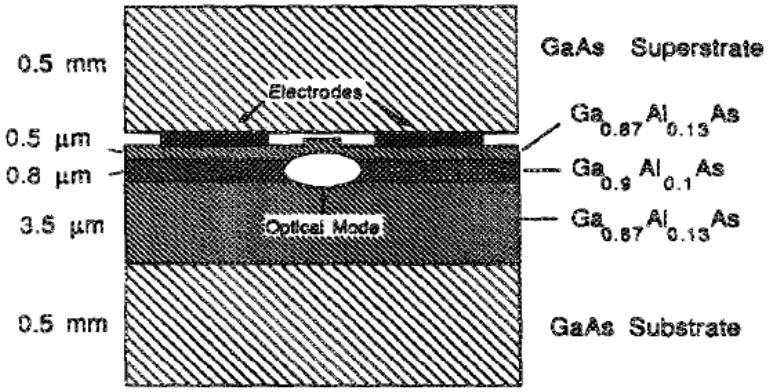
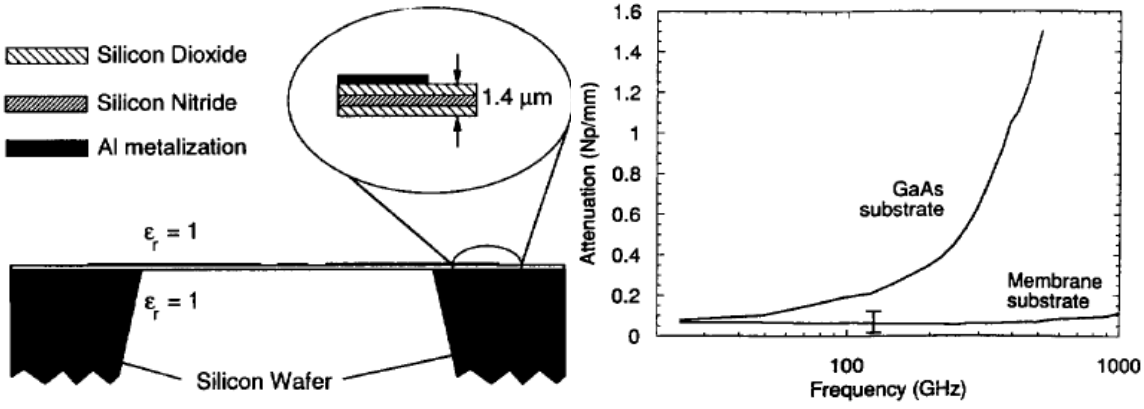


Figure 2-13 Velocity matched waveguide modulator with 100um wide coplanar striplines with S=20um sandwiched between GaAs substrates [32]

The main problem with this structure is the impossibility to obtain a perfect contact between the structures. In practice an air filled finite gap of width *d* will exist between the transmission line and the 'superstrate'. This gap is estimated to be up to 200 nm for the simple stripline geometry used in this work and would be expected to be higher for the non-planar MMICs. The decrease in effective dielectric constant due to the field lines tending to concentrate in this finite air gap is calculated in [33] for infinitely thin conductors as:

$$\varepsilon_{eff0} = \varepsilon_r - \frac{d(\varepsilon_r - 1)}{SK'(k)}\left[1 + \frac{\varepsilon_r(S + 2W)}{2WK(k)}\right] \qquad (2\text{-}16)$$

Another method employed to improve dielectric mismatch is reducing the substrate permittivity to close to that of air by utilizing micro-machined transmission lines as depicted in Figure 2-14(a). Transmission lines are fabricated over very thin layers of substrate [34, 35] or periodic support posts [36] where most of the substrate is etched. These structures enable low effective dielectric constant, reduced dielectric mismatch and reduced radiation loss. Fitted dielectric constant values of 2.0 and 5.2 are reported in [36] for coplanar striplines on 200nm thick SiO_2 cantilever support strips. Variation in measured dielectric constant is attributed to non-uniformity in SiO_2 etching. Despite the improved results of transmission lines on thin membranes as depicted in Figure 2-14(b), their complicated fabrication and mechanical robustness are issues to be considered.



(a) (b)

Figure 2-14 (a) Micromachined CPW structure (b) Attenuation of identical CPWs (W=40um & S=25um) on a thin membrane and on GaAs [34]

It has been demonstrated that at sub-THz and THz frequencies, frequency variation of $\varepsilon_{eff}(f)$ and phase velocity can be reduced and as a result radiation loss and dispersion can be minimized through:

- Scaling down CPW geometries
- Reducing the dielectric mismatch of materials surrounding the CPW.

Two approaches to realizing the latter method and their drawbacks have been presented. Next, the implications of scaling down CPW geometries will be discussed. Scaling down metals in horizontal direction also requires scaling in vertical direction due to fabrication limitations on realizable thin film aspect ratios. As a result, scaling down CPW geometries poses fabrication, material and reliability related problems which will be presented in the next section.

2.5. Metal Thin Film Limitations in High Frequency-High Power MMICs

Future of small-geometry metals as interconnects at THz frequencies is questionable as there are several adverse effects that impose limitations to shrinking metal conductor sizes and severely limit the electrical performance and reliability of thin films. Main issues that will be discussed in this section are:

- Resistivity increase in metal thin films
- Thermal-stress related limitations

2.5.1. Resistivity increase in metal thin films

Thin film metal resistivity defers from the bulk resistivity of the metal and is highly dependent on the metal thickness, deposition method and the underlying material. The classical expression for metal conductivity comes from the Drude model:

$$\sigma(\omega) = \frac{\sigma_o}{1 - i\omega\tau} \quad \text{and} \quad \sigma_o = \frac{ne^2\tau}{m} \tag{2-17}$$

where τ, scattering time, is the average time between collisions.

A main consideration, especially for thin films, is the scattering mechanisms which are not included in the Drude model. Scattering sites include defects, impurities, film surfaces/interfaces, and grain boundaries and significantly reduce the metal conductivity especially as the metal dimensions become comparable to electron mean free path. Taking into account all these scattering mechanisms, resistivity of a thin film is:

$$\rho(thin\ film) = \rho(thermal) + \rho(extrinsic) \tag{2-18}$$

$$\rho(extrinsic) = \rho(defect) + \rho(impurity) + \rho(grain\ boundary) + \rho(interface)$$

where $\rho(thermal)$ is the resistivity given by the Drude model.

As an example, consider the effect of surface scattering on resistivity [37]:

$$\frac{\rho_s}{\rho_o} = \frac{1}{1 - \frac{3(1-P)\lambda_{mfp}}{2d}\int_1^\infty \left(\frac{1}{x^3} - \frac{1}{x^5}\right)\frac{1 - e^{-kx}}{1 - Pe^{-kx}}dx} \tag{2-19}$$

where λ_{mfp} is the mean-free path of electrons, d is the film thickness and P is a parameter modeling elastic scattering (P = 1) that does not affect resistivity compared to diffuse scattering (P = 0) that increases it. Most interconnect metals used in ICs today exhibit P = 0.5 making them prone to increased resistivity due to surface scattering for small film

thicknesses compared to λ_{mfp}. High resistivity metals, such as copper, are affected more by surface scattering due to their large λ_{mfp}. Mean free paths for typical interconnect metals are summarized in Table 2-2.

Table 2-2 Mean free paths for metals used in interconnects [38]

Metal	Copper (Cu)	Aluminum (Al)	Tungsten (W)	Silver (Ag)	Gold (Au)
λ_{mfp}.[nm]	39.2	14.9	14.2	52.7	35.5

Figure 2-15 and Figure 2-16 depict the effect of thin film thickness on resistivity of Cu and Au, respectively. The deposition method dependency of metal resistivity can be observed from Figure 2-15 where minimum achievable Cu film thicknesses are 10 nm with CVD ($\rho \approx 30\rho_0$), 30 nm with electroplating ($\rho \approx 5\rho_0$) and 30nm with PVD ($\rho > 1000\rho_0$).

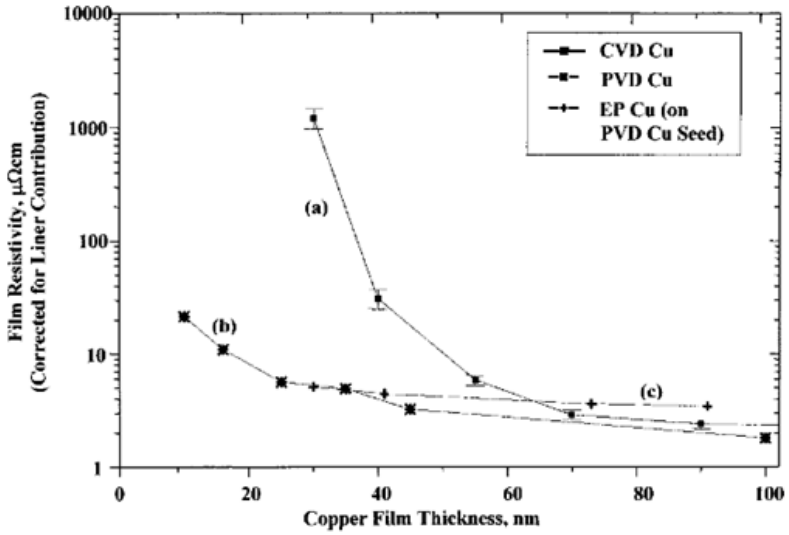


Figure 2-15 Copper resistivity as a function of thickness and deposition methods [38]

Figure 2-16 shows the resistivity dependence on underlying dielectric material, where Au on SiO_2 has much higher sheet resistance compared to Au on BCB or polymers. Sheet resistance of Au on SiO_2 is comparable to bulk value for t > 13 nm but increases drastically over 300 Ω/□ for thin films of t < 6 nm.

One important consideration not factored into the resistivities depicted in these plots is the barrier layer that is used to avoid the interaction of the metal with the underlying material. For example, in GaN MMICs, gold is deposited over a TiW barrier layer. Barrier layer increases thin film resistivity as [37]:

$$\frac{\rho_b}{\rho_o} = \frac{AR \times W^2}{AR \times W^2 - A_b} = \frac{1}{1 - A_b/(AR \times W^2)} \qquad (2\text{-}20)$$

where A_b is the area occupied by the barrier, AR is the aspect ratio of the thin film, and W is the width of the interconnect. (2-20) shows that for increasing aspect ratio and width, the effect of barrier layer on resistivity increases.

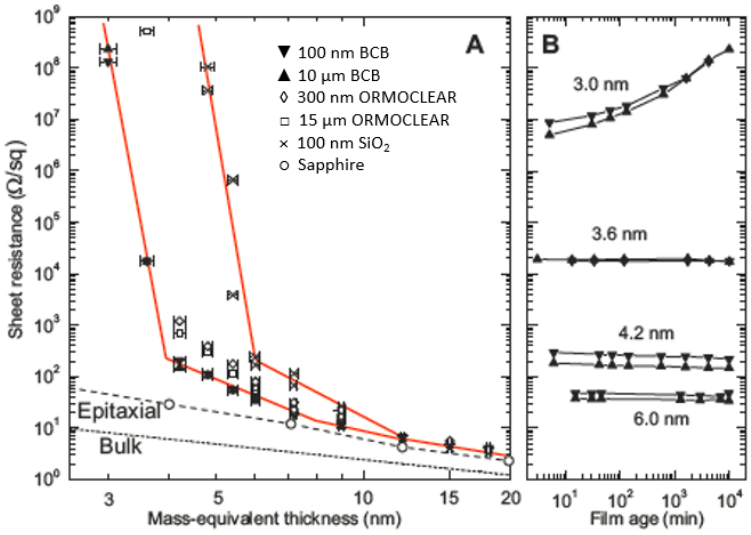


Figure 2-16 Au thin film resistivity as a function of thickness and time for films deposited on various dielectrics using conventional e-beam [39]

The resistivity expression including the scattering mechanisms as given by (2-17) shows excellent agreement with experimental values for thin films over some thickness but underestimates the resistivity for thinner films. The discrepancy arises from the assumption that surface roughness is smaller than the thin film thickness, which is not the case for ultrathin films. Surface roughness for e-beam deposited gold thin films of 3 nm to 7.3 nm thickness is depicted in

Figure 2-17. To minimize further increase in thin film resistivity due to surface roughness, research efforts are concentrated on improving the surface morphology of thin films via different deposition approaches, such as vacuum arc plasma process [40].

A study on conductivity of metals at THz frequencies also underlines the effect of thin film morphology and quality on the resistivity. In [41], it is reported that conductivity of Al and Cu drop at THz frequencies due to high carrier scattering by lattice defects within the 100nm THz skin depth. Considerably lower conductivity near the metal/air interface compared to conductivity near metal/polished Si interface is also reported. This variation is attributed to larger number of defects at the metal/air interface.

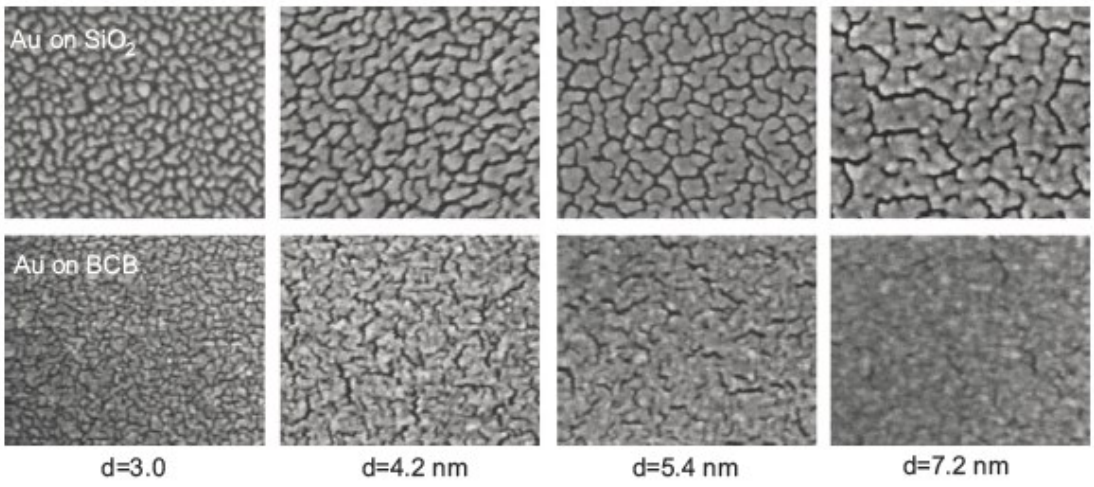


Figure 2-17 SEM images depicted the surface roughness of gold films on SiO2 and BCB polymer for different deposition thicknesses (images are 300nm across) [39]

The same authors investigate the THz conductivity of Al, Au and Ag thin films in [42]. As expected, the frequency independent conductivities of Al, Au and Ag thin films deposited via thermal evaporation are measured to be much lower than bulk conductivity, as shown in Table 2-3. This reduction is attributed mainly to scattering from grain boundaries. Two to four times reduced conductivity for Al and Au films at THz frequencies is also reported and again attributed to different conductivities at different interfaces of the metal film. Very large reflections at 0.5 – 3 THz range due to reduced conductivity near the interfaces are also reported.

Table 2-3 Thin film conductivities [$(\mu\Omega\text{-m})^{-1}$] and their percentages relative to bulk conductivities [42]

Metal	Thickness (nm)	σ at 295 K	σ at 77 K	Bulk σ_{dc} [a] at 295 K	Bulk σ_{dc} [a] at 80 K
	36	17 (45%)	25 (6%)		
	88	16 (42%)	26 (6%)		
Al	152	22 (58%)	51 (12%)	37.7	408
	85	15 (33%)	24 (12%)		
Au	150	31 (69%)	70 (34%)	45.2	208
Ag	86	46 (73%)	105 (30%)	63.0	346

The effects of reduced dimensions on thin film resistivity that have been presented so far are summarized below:

- Resistivity of thin film metals defer from the bulk value and depend on the fabrication method and the underlying,
- Barrier layers, used with Au in GaN MMICs, increase the overall resistivity,
- Resistivity increases due to scattering especially as metal dimensions are comparable to electron mean free paths for the metal,
- Further increase in resistivity is observed if surface roughness is in the order of metal dimensions,
- At THz frequencies, localized defects within the skin depth can reduce the resistivity more than anticipated by the skin effect.

2.5.2. Thermal-stress related limitations

Another important consideration for thin film interconnects for high frequency, high power applications is reliability, especially due to thermal effects. Interconnect

temperature may increase from Joule heating due to high current densities and poor heat conduction. Heating can place the metal under compression resulting in hillocks and cooling can place the metal under tension resulting in voids, leading to electrical shorts or opens, respectively. High current densities causing the movement of metal atoms in direction of current flow, i.e. electromigration (EM), can also result in void or hillock formation as depicted in Figure 2-18 and lead to interconnect failure. In order to avoid failure due to thermal effects, rms current density, average current density and short duration high peak currents on interconnects are limited in circuit design.

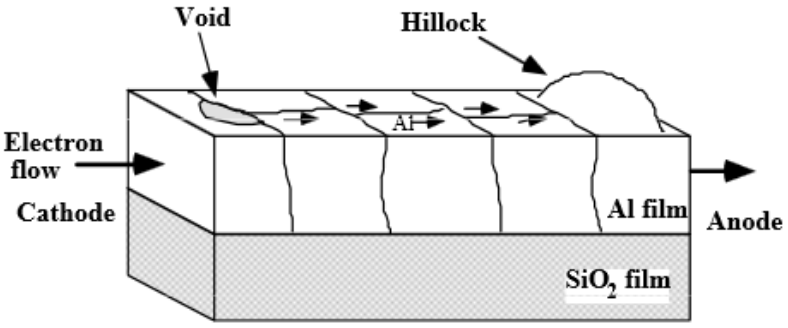


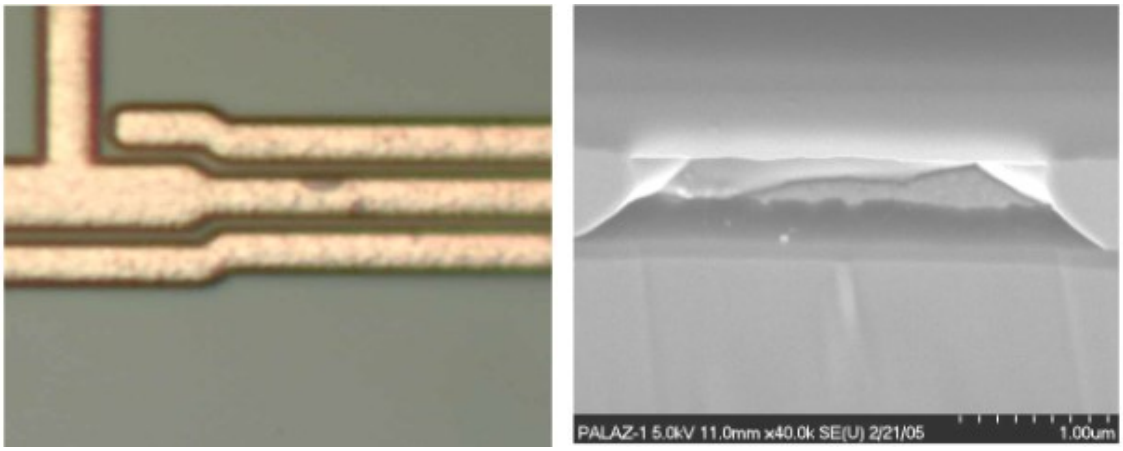
Figure 2-18 Void and hillock formation in thin films via electromigration

The median lifetime of an interconnect due to electromigration is given by:

$$t_{50\%} = \frac{A}{J^n} e^{\left(\frac{E_a}{kT}\right)} \qquad (2\text{-}21)$$

where A is a geometry-dependent material constant, E_a is the activation energy of the diffusion process (i.e. 0.6 eV for surface/interface diffusion for Au [43]) J is the current density, n is the current density exponent typically between 1-2, and T is the metal film

temperature. As observed from the equation, the increased current density and temperature -both of which are high for GaN MMICs- degrade the interconnect lifetime.



(a) (b)

Figure 2-19 (a) Optical micrograph of an electromigration void on a 1um thick Au interconnect, (b) SEM micrograph of a FIB cross-section of the void [43]

Figure 2-19 depicts a void on a gold interconnect caused by EM at $2x10^4$ A/mm^2 current density and 341°C operating temperature. The gold interconnect on GaAs substrate consists of a 100 nm TiW barrier layer, 30 nm sputtered Au seed layer and a 1 μm thick polycrystalline, electroplated Au film passivated with 0.8 μm nitride layer. In this Freescale Semiconductor-led study [43], it is found that the EM void is initiated at the TiW/Au seed layer interface and migrated upward, finally causing the bottom of Au line to completely migrate, leaving only a small portion of electroplated Au on the top back portion of the void as depicted in Figure 2-19(b).

Given the current densities reported by this study, 1 μm-thick Au interconnect can fail at maximum current density of 20 A/mm and 0.1 μm-thick Au interconnect only at 2

A/mm at operating temperatures of 341°C. If gold interconnect thickness is reduced to sub-micron range to minimize radiation loss, the maximum current density it can reliably support will reduce further. It would be a challenge to use such an interconnect in a high power GaN MMIC given that in a design maximum allowable current density on a metal line is around half of the failure value and that GaN HEMTs already report maximum drain currents over 1 A/mm and operating channel temperatures of 200-300°C.

Short duration-high peak current failure imposes stricter limitations to maximum currents and frequencies for a given metal thickness than the EM induced average current limitation discussed here. Metal interconnects will eventually impose the major trade-off between high power and high frequency designs as current densities and frequencies increase.

Another thermal-stress related reliability issue arises from the mismatch of thermal expansion coefficients of the substrate and the thin film, which results in mechanical stress, especially at high temperature operation. Thermal expansion coefficients for some GaN system materials are: 14 x 10^{-6} K^{-1} (Au), 3.17 - 5.6 x 10^{-6} K^{-1} (GaN), 3.2 x 10^{-6} C^{-1} (SiN). Deposition processes such as sputtering and low-temperature plating can cause an 'intrinsic' stress for the thin film. Stress due to difference in thermal expansion in addition to the intrinsic stress due to deposition can lead to cracking or interfacial failure of the thin film [44].

3. TEST STRUCTURES AND FABRICATION

In order to have broadband microwave characterization of the GaN-on-Si substrate as well as the 2DEG transmission properties, transmission lines were employed instead of resonant structures that are commonly used for material characterization. CPW transmission lines were preferred over microstrips to minimize dispersion, radiation losses, and parasitic surface wave and substrate modes. Similar structures are used for the characterization of both the substrate and the 2DEG transmission. Samples fabricated for the 2DEG characterization use extra masks in order to define the active areas, passivate the AlGaN/GaN top surface and enable fabrication of ohmic contacts to 2DEG.

In this section, first the design of CPWs used in the characterization is explained. Then the calibration structures included in the masks and their design is detailed. Next the fabrication flow and masks for the samples used in GaN-on-Si substrate loss and 2DEG transmission loss characterization are explained. Details of process steps and the problems encountered are also included. Finally the measurement setup is described.

3.1. First Design Cycle: GaN-on-Si Substrate Loss and 2DEG

The top and cross-sectional views of the CPW structures are depicted in Figure 3-1 (a) and (b), respectively. The design parameters for a CPW, on a substrate of height h and dielectric constant ε_r, are the signal (W) and ground conductor (W_{GND}) widths, the separation (S) between them and the CPW length (L) as well as the conductor metal and its thickness. First three parameters determine the characteristic impedance and the last two set the unit metal loss of the CPW.

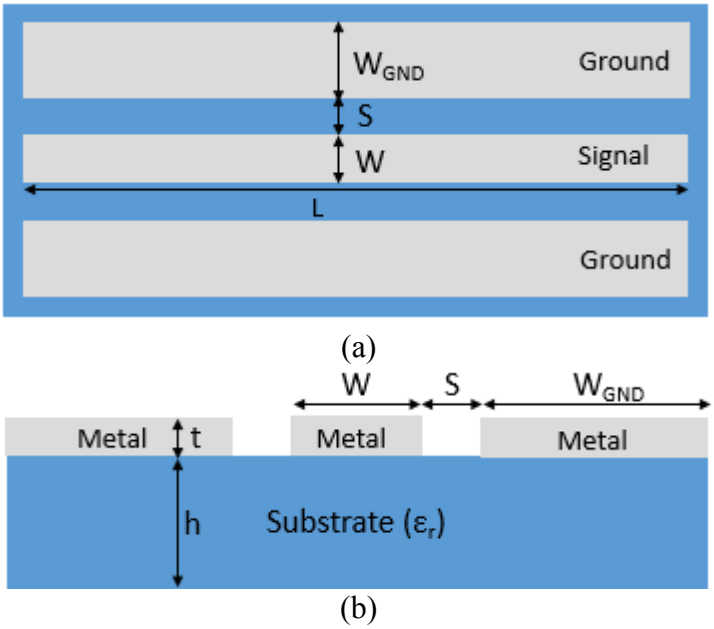
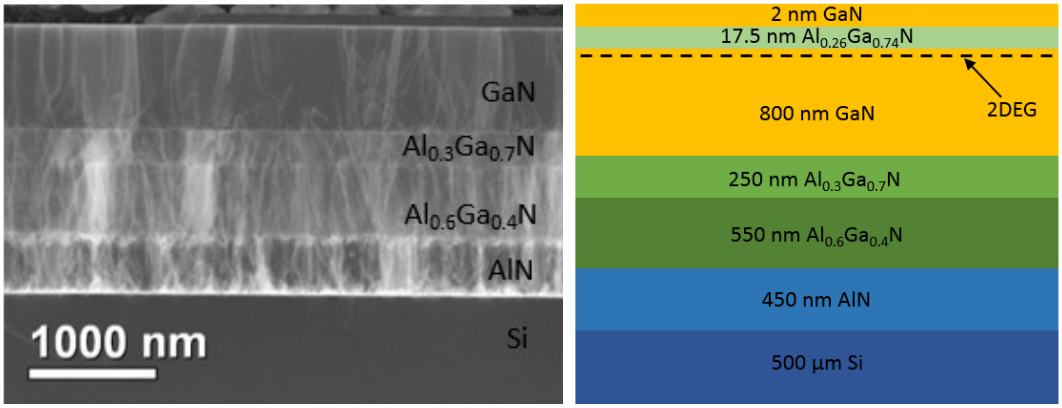


Figure 3-1 (a) top view and (b) cross-sectional view of a metal CPW

Characteristic impedance of the CPW needs to be 50 Ω in order to match the network analyzer input/output impedance. CPW Z_0 is given by (2-12) and W, S and W_{GND}, as well as substrate height and dielectric constant through $\varepsilon_{eff}(f)$. CPW samples were fabricated on different substrates for this study. High resistivity (Hi-R) Si substrate was used for control / reference samples. Nitronex AlGaN/GaN templates were used to prepare the substrates for the other CPW samples.

AlGaN/GaN heterostructure used in this study consist of various $Al_xGa_{1-x}N$ epi-layers on Hi-R Si substrate as depicted in Figure 3-2. In this notation, *x* indicates the Al mol fraction and determines the dielectric constant of the epi-layer as [45]:

$$\boldsymbol{\varepsilon_{r\,(Al_x\,Ga_{1-x}N)} = -1.2x + 9.7} \qquad (3\text{-}1)$$



(a) (b)

Figure 3-2 Cross-sectional (a) TEM image and (b) schematic of the AlGaN/GaN heterostructure used in this study.

Table 3-1 Dielectric constants of different epi-layers and epi-layer combinations

Layer (Bottom to Top)	**Thickness(µm)**	ε_r	$\varepsilon_{r,total}$	$\varepsilon_{r,total}$	$\varepsilon_{r,total}$
SiN	0.1	7			
GaN	0.002	9.7			
$Al_{0.26}Ga_{0.74}N$	0.0175	9.388			
GaN	0.8	9.7		11.8869	11.8861
$Al_{0.3}Ga_{0.7}N$	0.25	9.34			
$Al_{0.6}Ga_{0.4}N$	0.55	8.98			
AlN	0.45	8.5	11.8870		
Si	500	11.9			

In order to determine the CPW dimensions that will yield 50 Ω Z_0, first the total dielectric constant of multi-layer substrate needs to be determined. As shown in Table 3-1, the dielectric constants of the epi-layers, calculated using (3-1) vary between 8.5 and 9.7; a value much smaller than the Si dielectric constant of 11.9 [3]. The overall dielectric constant of substrates consisting of different epi-layers on Si is calculated through series capacitor approximation, assuming same area capacitance for the given thickness and dielectric constant of each layer. Dielectric constants for AlN-on-Si, full AlGaN/GaN

heterostructure and AlGaN/GaN with 100 nm SiN for passivation are tabulated in Table 3-1. The results show that the dielectric constant of 500 μm thick Si determines the overall value.

Table 3-2 Designed CPW dimensions for substrate characterization mask

CPW	W (μm)	W_{GND} (μm)	S (μm)	Z_0 (Ω)	ε_{eff}
1c	63.5	190.5	63.5	58.18	6.41
1b			50.8	54.52	6.42
1a			38.1	50.13	6.43
2c	76.2	228.6	63.5	55.22	6.41
2b			50.8	51.73	6.42
2a			38.1	47.57	6.42
3c	88.9	266.7	63.5	52.83	6.40
3b			50.8	49.49	6.41
3a			38.1	45.53	6.42
4c	101.6	304.8	63.5	50.85	6.4
4b			50.8	47.64	6.41
4a			38.1	43.85	6.41

First order design of CPW dimensions is obtained using $\varepsilon_r \approx 11.89$. Note that this assumes parallel-plate capacitance and uniform EM fields which is not accurate for the CPW structure. Sonnet simulations with multi-layer substrates using the tabulated dielectric constants and thicknesses for each layer were used to verify the Z_0. Note that the dielectric conductivity of each epi-layer will also alter the EM fields. The Si (111) substrate is highly resistive, with the specified resistivity of 10 kΩ-cm. The AlN and AlGaN T.L layers are labeled as 'highly resistive' and the GaN layer as 'semi-insulating'; however, their resistivities are unknown. In order to accommodate for Z_0 variations with substrate resistivities, CPWs with different dimensions are included in the first mask designed for substrate characterization. Dimensions for the CPW structures as well as their

characteristic impedance and effective permittivity, calculated assuming non-conductive substrate are given in Table 3-2.

CPW ground width is designed to be three times the signal conductor width in order to minimize the effects of finite W_{GND} [46, 47]. The effect of finite ground width on CPW attenuation is depicted in Figure 3-3. The attenuation increases with narrow ground conductors and the frequency dependence of attenuation for finite ground width, depicted in Figure 3-3, suggests that conductor losses dominate for narrow ($W_{GND} < 2W$) ground planes [46]. On the other hand, radiation loss increases with W_{GND} and a maximum ground conductor of $\lambda/8$ is recommended [48].

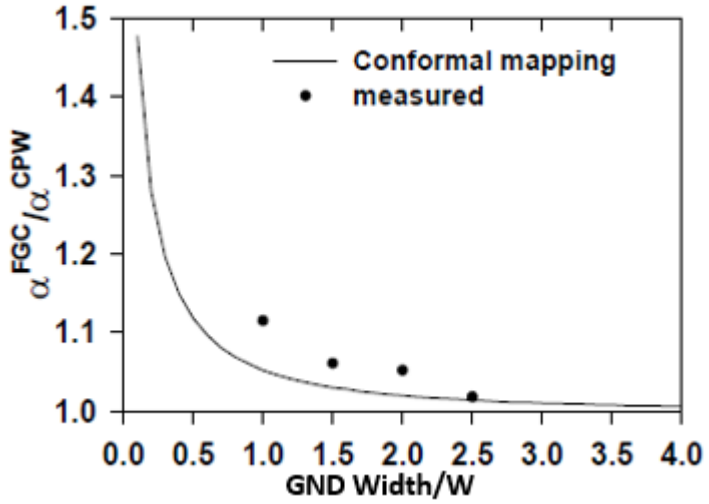


Figure 3-3 Effect of finite CPW ground width on attenuation: ratio of attenuation with finite W_{GND} (α_{FGC}) to infinite W_{GND} (α_{CPW}) [46].

Each CPW structure listed in Table 3-2 were included in the mask with four different lengths as well as open structures in order to enable on-wafer TRL calibration. These

CPWs of same geometry but different length –and die position- are also used for statistical purposes in characterization measurements with SOLT calibration.

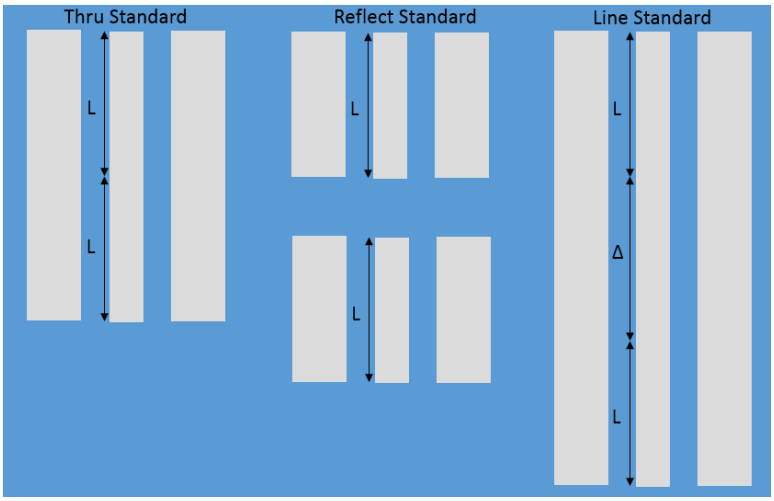


Figure 3-4 Schematic of TRL calibration standards.

For TRL calibration Thru, Reflect and at least one Line standard, as depicted in Figure 3-4, are needed. Reflect can be an open or a short; open structures are used in this mask as the same design is used for 2DEG CPWs for which short is difficult to implement. With TRL calibration, the reference plane is moved from the probe tips to a distance L for a Thru standard of length 2L. Reflect standards are fabricated with the same length L. The Line standard is of length 2L+Δ, where Δ determines the frequency range of calibration. Δ is designed to correspond to an electrical length of 90° ($\Delta = \lambda/4$) at the center frequency. Minimum and maximum measurement frequencies after the calibration should correspond to electrical lengths of 20° and 160°, respectively. For a frequency span of more than 8:1

(span:f_{min}), multiple Line standards are required. Meanwhile, Thru length is set to between λ/4 to λ/8. Note that the electrical length is:

$$\boldsymbol{\theta = 2\pi\left(\frac{l}{\lambda}\right)}, \tag{3-2}$$

where the wavelength λ is determined by the phase velocity v_p.

$$\boldsymbol{\lambda = \frac{v_p}{f}} \tag{3-3}$$

$$\boldsymbol{v_p = \frac{c}{\sqrt{\varepsilon_{eff}}}} \tag{3-4}$$

Assuming uniform field distribution in air and in the dielectric, ε_{eff} is calculated to be 6.445 and v_p as 1.181×10^8 m/s. CPW lengths used in this mask are given in Table 3-3. Lines 1, 2, and 3 can be used for TRL calibrations with different frequency spans. Their minimum and maximum frequencies that fulfill the electrical length requirement described above are also given in the same table. Mask 1 die layout with the CPW dimensions given in Table 3-2 and Table 3-3 is depicted in Figure 3-5. This mask is used for fabricating metal CPWs on various substrates for GaN-on-Si substrate characterization.

Table 3-3 CPW lengths and Line standard frequency spans for TRL calibration

	L (mm)	**f_{min} (GHz)**	**f_{max} (GHz)**
Thru	2.2	-	-
Open	1.1	-	-
Line 1	3.5	5	40
Line 2	2.85	10	80
Line 3	4.15	3.4	27

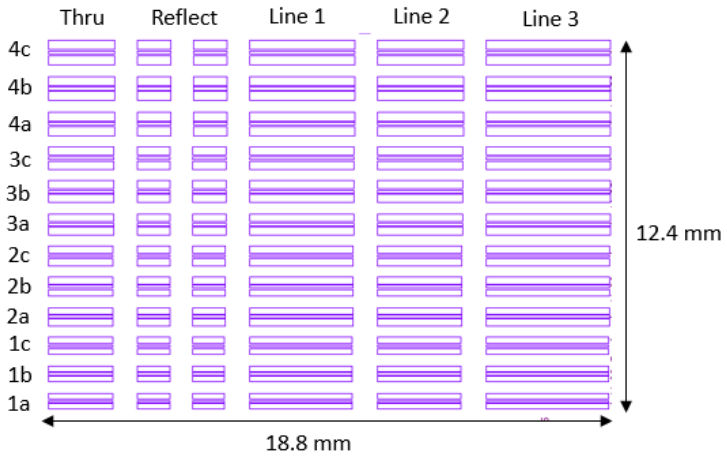


Figure 3-5 Metal CPW die layout (mask set 1)

Same die layout is also used to fabricate 2DEG CPWs, in which the metal signal and ground conductors are replaced by 2DEG. 2DEG is present everywhere in the original AlGaN/GaN heterostructure, buried ~20nm from the top surface. Recess etch is used to remove more than 20nm of the top surface, hence the 2DEG, from everywhere but the CPW conductor locations. After the sample is passivated with SiN, Ohmic contacts are formed at the ends of the CPWs in order to access the 2DEG conductors that are buried under the SiN and ~20nm AlGaN/GaN layers. 2DEG CPW top views depicting the ohmic contact locations on the 2DEG conductors and also the contact design are given in Figure 3-6 (a) and (b), respectively. The same figure (c) shows the cross-sectional schematic of the transmission path, showing a 2DEG conductor and the ohmic contacts on both ends. Figure 3-6(d) is another cross-sectional view depicting the ground-signal-ground lines of the 2DEG CPW and their ohmic contacts.

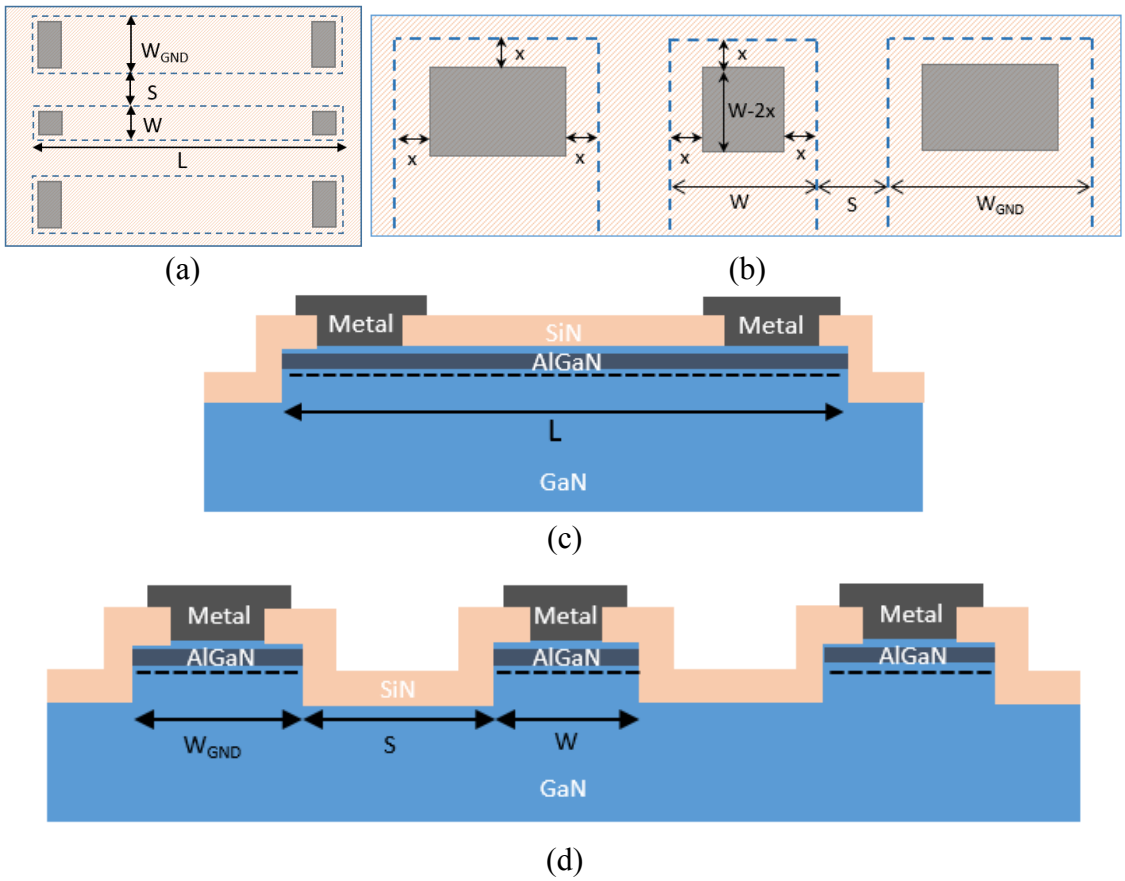


Figure 3-6 2DEG CPW top view schematics showing (a) the 2DEG CPWs and (b) contact design and cross-sectional schematics showing the (c) transmission path and (d) ground-signal-ground contacts.

Note that the contact opening in SiN is separated from the edges of the active area by a distance. This is to ensure contact metal is only over the active region and not in contact with the recessed GaN. Also, the ohmic contact metal overlaps the SiN around the contact opening in order to guarantee the active area is fully covered by the contact metal. Metal is also separated from the active area edges by a distance x in order to avoid overlap capacitors over the recessed GaN. These measures are taken against fabrication tolerances and mask misalignment failures. Another consideration while designing the contacts is the

GSG RF probe pitch – the contacts are designed to have less than 150 μm separation between them. Total of 4 masks are used for the 2DEG CPWs in order to accommodate the fabrication steps to recess etch AlGaN/GaN to define the 2DEG transmission lines and to create ohmic contacts. 2DEG CPW die layout with all 4 masks overlaid is depicted in Figure 3-18. The die is identical to that of the metal CPWs, except for the ohmic contacts at the CPW ends – visible (blue) in the figure for wider CPWs. 2DEG masks are given in Appendix A.1 - A.5 and the details are described in Section 3.3.

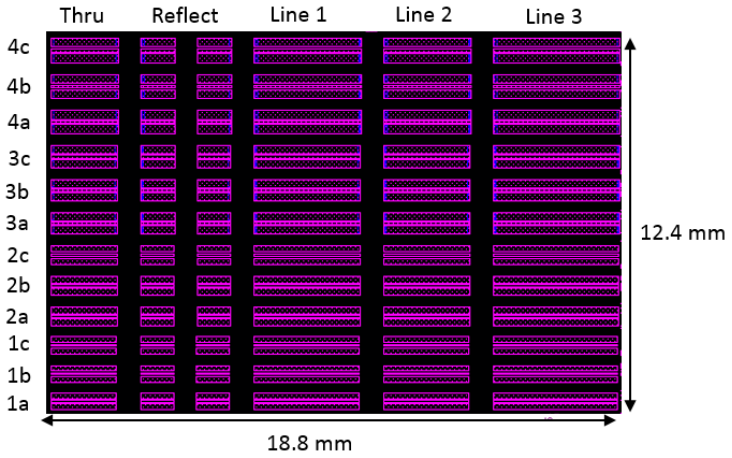


Figure 3-7 2DEG CPW die layout (mask set 1)

The masks were fabricated as photoplots by a commercial company and the photoplots were used to fabricate glass masks in-house. Especially due to the low resolution of the photoplots and the tolerances involved in Cr-on-glass mask fabrication, the final mask dimensions used in sample fabrication are different than the designed values. Final mask dimensions and corresponding characteristic impedance and effective permittivity values

are given in Table 3-4. Fabricated samples are within ±2 μm of the given dimensions due to photolithography tolerances.

Table 3-4 Fabricated CPW dimensions for substrate characterization

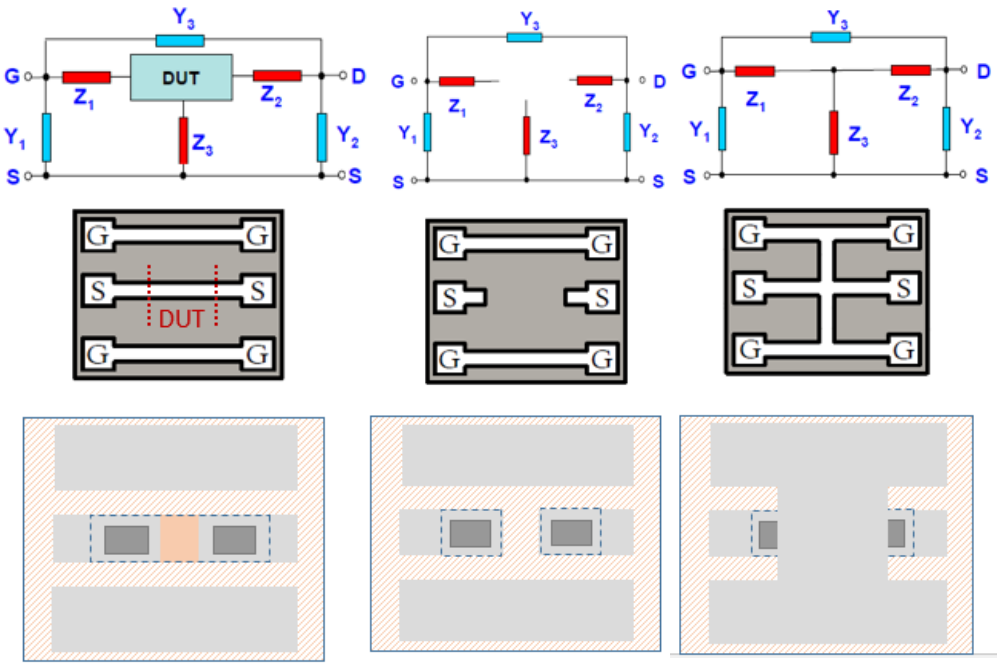
CPW	W (μm)	W_{GND} (μm)	S (μm)	Z_0 (Ω)	ε_{eff}
1c	74	190.5	53.5	52.96	6.42
1b			40.5	48.83	6.42
1a			27.5	43.68	6.43
2c	87	228.6	53.5	50.56	6.41
2b			40.5	46.62	6.42
2a			28	41.96	6.42
3c	99	276	53.5	48.72	6.40
3b			41	45.11	6.41
3a	104	271	28	39.95	6.42
4c	111.7	315	53	46.95	6.4
4b			40.5	43.45	6.41
4a			28	39.18	6.41

3.2. Second Design Cycle: 2DEG Transmission and Ohmic Contacts

3.2.1. 2DEG Transmission Line Characterization

Due to difficulties of obtaining reliable TRL calibration, a new mask set with de-embedding structures, rather than TRL kit is fabricated. Open-short de-embedding is used to extract the series and parallel parasitics due to device pads and ohmic contacts. Details of the open-short de-embedding algorithm is discussed in Section 4.5. De-embedding structures are designed as CPWs for probing with GSG configuration. The test and de-embedding structure schematics and the corresponding circuit elements are depicted in Figure 3-8. The 2DEG transmission line test structure with GSG pads is shown in Figure 3-8(a). Open de-embedding structure, Figure 3-8(b), is used to measure the parallel circuit

elements in the test structure whereas the short de-embedding structure given in Figure 3-8(c) is for series circuit element extraction. Note that the ohmic contacts are included in the open-short de-embedding structures and they will also be de-embedded, enabling the characterization of 2DEG transmission without the ohmic contact parasitics.



(a) (b) (c)

Figure 3-8 2DEG Transmission line test and de-embedding structures

The horizontal and vertical cross-sections of the de-embedding structures are depicted in Figure 3-9.

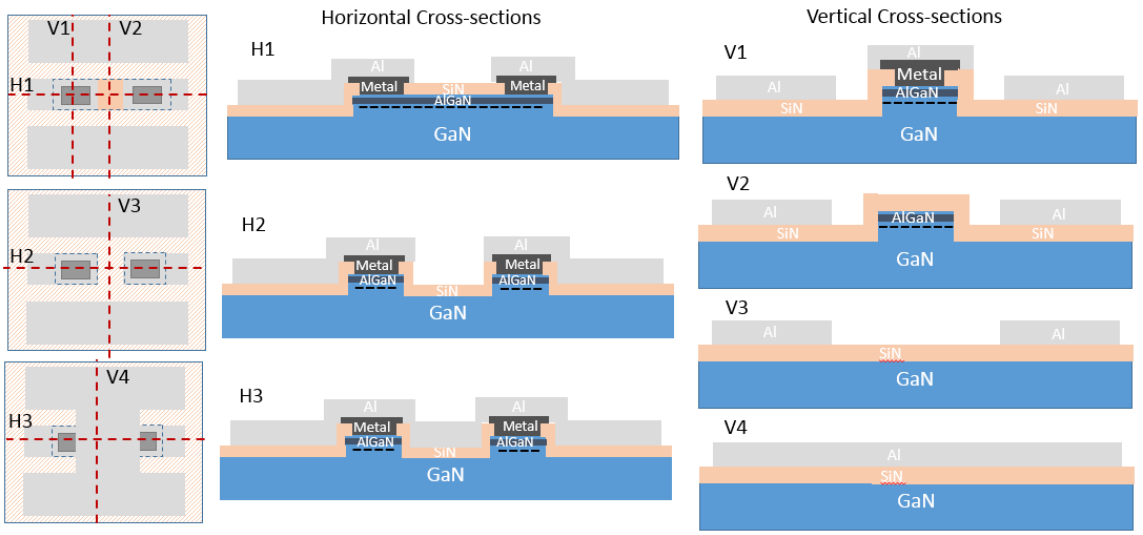


Figure 3-9 Horizontal and vertical cross-sections for the 2DEG Transmission line test and de-embedding structures

The CPW dimensions used for the pads are designed according to results obtained from the first Mask set metal CPW measurements. The CPW geometry that yielded characteristic impedance close to 50 Ω on GaN-on-Si substrate used for this mask. Accordingly, W = 97 µm and S = 57 µm and WGND= 300 µm for all the test structures in this mask. The DUT, which is the 2DEG transmission line, embedded in the CPW test structures is designed to have five different lengths of 8, 10, 12, 14, and 16 µm. Total CPW length is the same for all the structures but the length of signal pad is adjusted according to the DUT length. A schematic of the DUT with the CPW pads is depicted in Figure 3-10.

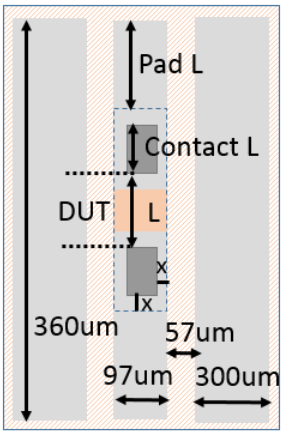


Figure 3-10 Schematic of 2DEG Transmission line test structure with CPW pads

For the 2DEG contact design, the width of the contact is maximized in order to minimize the 2DEG resistance. However, there are no guidelines in literature about the contact length or its tradeoffs. In order to observe the effects of 2DEG contact length on the ohmic contact and its parasitics, three different contact lengths of 11, 22, and 44 μm are used for contact width of 91 μm. Contact width is limited by the width of the CPW pad and the minimum required distance between the contact – active region edge, x, dictated by fabrication tolerances. The mask includes 2DEG transmission line test structure and open/short de-embedding structures for each contact length and 2DEG transmission length combination.

A set of same test and de-embedding structures with no 2DEG or ohmic contact but only Al pads, as depicted in Figure 3-11, is also included in the mask. They are included to provide a reference measurement and they can also be used to de-embed the ohmic contacts from the Al pads.

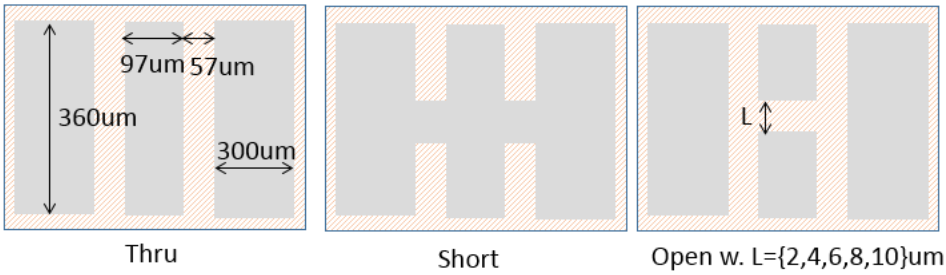


Figure 3-11 Al-only transmission line and open/short de-embedding structures

In addition to 2DEG transmission lines, 2DEG CPWs are also included in the mask to observe the variations if any due to 2DEG ground planes. 2DEG CPWs, depicted in Figure 3-12, are designed with 22 µm long contacts with all the other parameters the same as the 2DEG CPW test structures. The de-embedding structures are shown in the Figure 3-13.

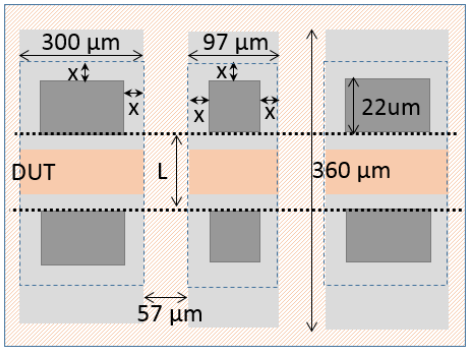


Figure 3-12 Schematic of 2DEG CPW test structure with CPW pads

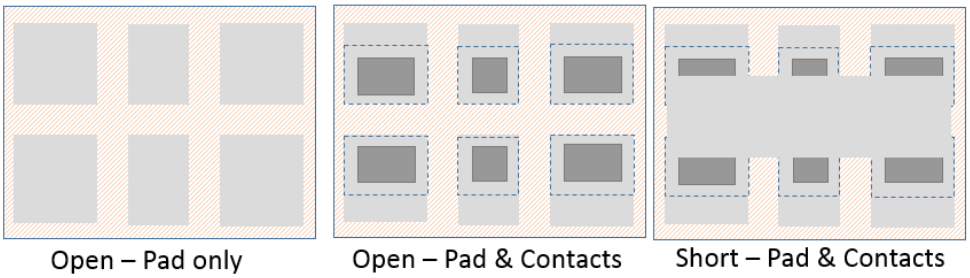
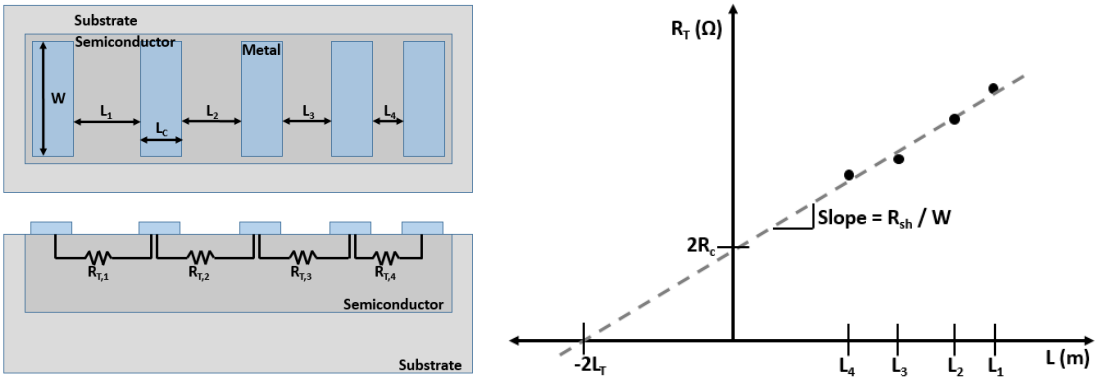


Figure 3-13 Schematic of de-embedding structures for 2DEG CPW

3.2.2. Ohmic Contact Characterization

In order to characterize the ohmic contacts to GaN transfer length method (TLM) test structure is used. TLM test structure, as depicted in Figure 3-14(a), consists of same dimension contacts separated by varying lengths of semiconductor / contacted material. From the resistance measurements between two adjacent contacts, the contact characteristics are derived as depicted in Figure 3-14(b). Sheet resistance, R_s, of the semiconductor is obtained from the slope of the linear fit to measured resistance vs. length, whereas its y- and x-intercepts yield the contact resistance, R_c, and the 'transfer length', L_T, respectively.



(a) (b)

Figure 3-14 (a) TLM test structure top and cross-sectional view (b) Contact parameters extraction using TLM data

Transfer length, L_T, is the effective contact length due to current crowding around the contact-semiconductor interface, illustrated in Figure 3-15. Given the exponential voltage drop with x, the distance at which there is the '1/e' voltage drop is defined as L_T and calculated as:

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{3-5}$$

where the specific contact resistivity, ρ_c ($\Omega \cdot cm^2$), is a parameter derived taking into account all the physical effects related to the contact and includes not only the contact-semiconductor interface but the regions around it. It is independent of contact area and, therefore, is a good metric for comparing contact quality.

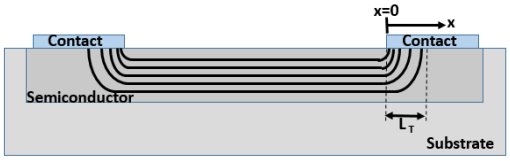


Figure 3-15 Cross-sectional schematic of a contact depicting the current crowding at the contact edges and the transfer length.

The relationship between the extracted parameters and the R-L data points, depicted in Figure 3-14(b) is derived under the assumption that the measured resistance is the series combination of two contact resistances and the resistance of the semiconductor in between:

$$R_T = 2R_c + R_s = 2R_c + \frac{R_{sh}}{W} L \tag{3-6}$$

where the contact resistance is calculated as specific contact resistivity, ρ_c, divided by effective contact area:

$$R_c = \frac{\rho_c}{L_T W} \tag{3-7}$$

(3-7) is valid for $L > 1.5\ L_T$; otherwise, L_T should be replaced by L for $L < 0.5\ L_T$ or by $L_T/\coth(L/L_T)$ for values in between. Combining (3-5) - (3-7), the TLM equation to determine L_T is obtained:

$$\boldsymbol{R_T = \frac{R_{sh}}{W} 2L_T + \frac{R_{sh}}{W} L} \tag{3-8}$$

As a final note, R_{sh}, L_T and ρ_c are the parameters that determine the quality of the contact and the resistance for a given area. Sometimes R_cW is product is reported as a metric as it is the ratio between the two of these parameters as shown in (3-7).

The TLM test structure designed for the ohmic contact characterization in this study is similar to that depicted in Figure 3-14(a), with the 2DEG as the semiconductor and the recessed GaN as the substrate. The distance L between the seven sets of ohmic contacts are 8, 10, 12, 14, 16, 18 and 20 μm.

The width of the contacts are the same as those of 2DEG transmission structures and are optimized for minimum 2DEG resistance. For the active 2DEG area of 97 μm width, using 3 μm separation from the active area edge on both sides to accommodate misalignment and fabrication tolerances, the contact with width is set to 91 μm.

While determining the length of the contact, the transfer length plays and important role. Current flows through only the transfer length portion of the contact, and therefore, contacts longer than L_T do not improve the R_C as shown by (3-7) and depicted in Figure 3-16 for different ρ_c values. The effective area, hence, the current density flowing across the contact, is also determined by L_T. Based on this, contact length should be minimized to a value of $L > 1.5\ L_T$ to obtain the smallest possible R_C and parasitics. However, the 2DEG ohmic contacts reported in literature are generally very large area structures and

there is no explanation for the need for large contact lengths. In order to observe effect of length on contact parameters, three different contact sets with L of 11, 22, and 44 μm were designed. Parallel combination of contacts, commonly used in Si IC design, was also tested with two more contact sets of five by one and five by two parallel contact vias.

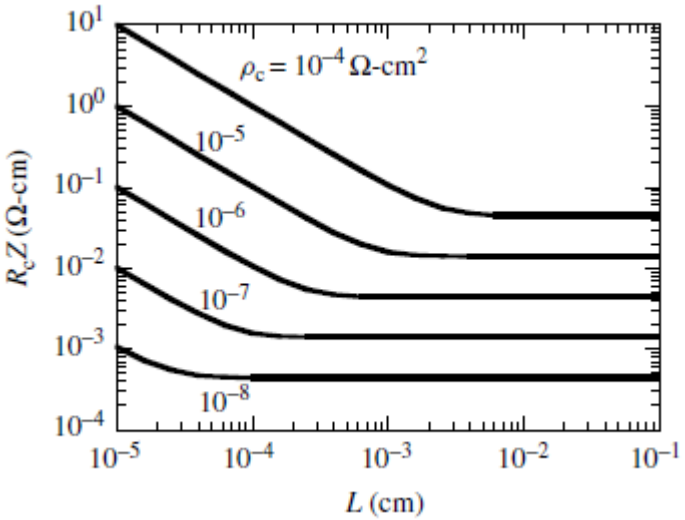


Figure 3-16 Variation of contact resistance – width product with contact length [49]

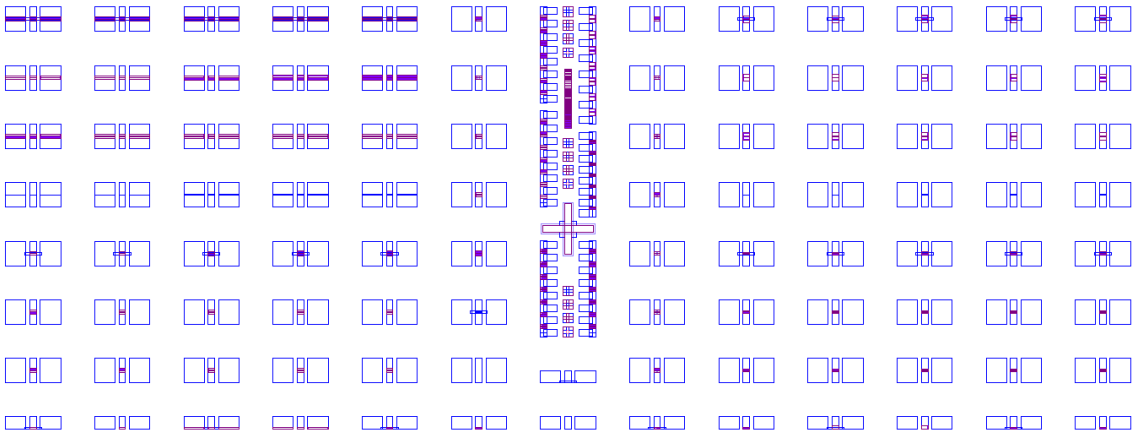


Figure 3-17 Mask Set 2 Die Layout

3.3. Sample Fabrication

Mask 1 of Mask Set I is used to fabricate metal CPWs on various substrates for the GaN-on-Si epi-layer loss characterization. Fabrication of metal CPWs and the preparation of the sample substrates are described in Section 3.3.1.

In order to characterize the 2DEG transmission, two different samples with different test structures have been fabricated using Mask Sets I and II. Even though the test structures differ in these samples, the fabrication steps for 2DEG transmission line is the same in terms of active area definition and ohmic contact formation. The only fabrication difference is that the second 2DEG sample, using Mask Set II, has an extra mask after ohmic contact formation in order to create Al interconnects and de-embedding structures. Mask Set II also contains TLM structures for 2DEG ohmic contact characterization. Even though the layout is different, the fabrication steps are the same as second 2DEG sample. In order to avoid repetition, the fabrication steps for all of these 2DEG devices are detailed in Section 3.3.2.

PECVD recipe for electrically insulating SiN was also developed during this study. Problems encountered with SiN quality and the insulating SiN design is explained in Section 3.3.3.

3.3.1. Metal CPW Fabrication

In order to investigate the loss contribution of epi-layers in AlGaN/GaN heterostructure five different samples were fabricated as depicted in Figure 3-18. The AlN and AlGaN/GaN templates are taken from the same GaN-on-Si fabrication process [50].

Figure 3-18(a) shows the control sample, used for reference, on 10 kΩ-cm Si (111) wafer, identical to the substrate of GaN-on-Si. Two samples shown in Figure 3-18(b) were fabricated on AlN-on-Si with AlN epi-thicknesses of 219 and 345 nm. The final two samples in Figure 3-18(c) were fabricated on GaN-on-Si of 595 and 795 nm GaN layers. Samples with different AlN and GaN layer thicknesses were achieved by reactive ion etching (RIE) of AlN-on-Si and GaN-on-Si, respectively.

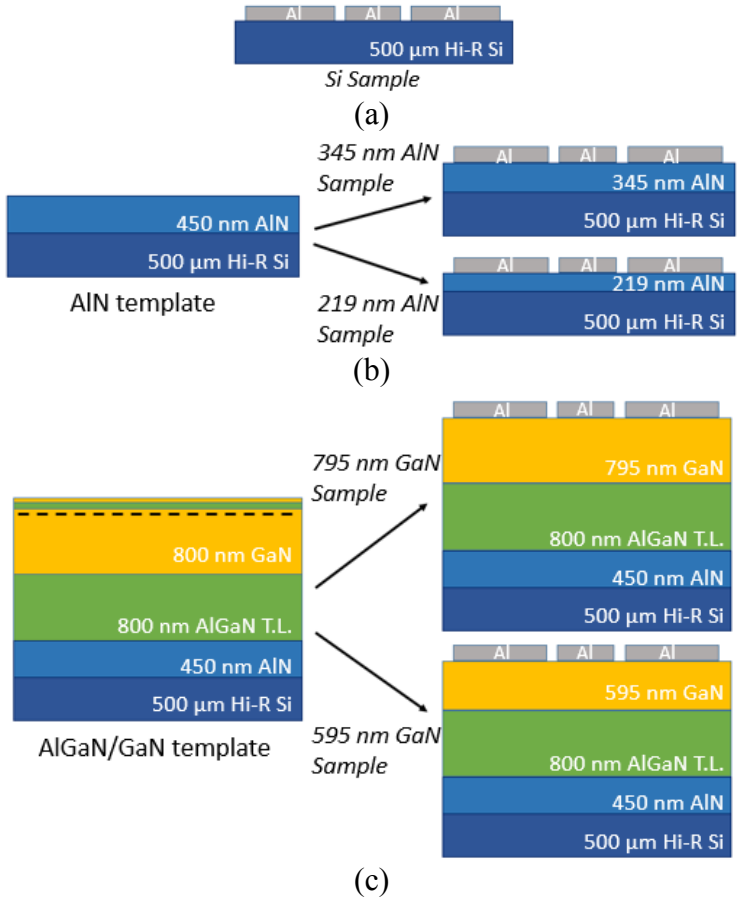


Figure 3-18 Cross-sectional representation of fabricated test samples (a) Si sample (b) AlN template and the two samples fabricated from it (c) AlGaN/GaN template and GaN-on-Si samples fabricated from it.

AlN-on-Si used for the sample fabrication consists of 450 nm AlN layer grown via MOCVD on high resistivity Si. Forming the 219 and 345 nm samples was completed by thinning the 450 nm thick AlN. Normally, the top surface of as-grown AlN is intentionally rough in order to trap threading dislocations and disperse mechanical stress that would follow for full HFET growth [51]. Therefore, a reactive ion etch (RIE) of was employed to not only planarize the surface but also target the thickness indicated in Figure 3-18(b). The AlN surface roughness is observed in the left side of the cross-sectional scanning electron microscope (SEM) image in Figure 3-19. An AlN etch rate of 7 nm/min was achieved with RIE using an SF_6 flow rate of 40 sccm and Ar flow rate of 10 sccm at 16°C with 44 mTorr chamber pressure, 200 W RF power and 400 W inductively coupled plasma (ICP) power. Planarization of the as-grown surface roughness after a 10-minute RIE etch using this RIE recipe is depicted in Figure 3-19. For the samples used in this study, the AlN was RIE-etched for 15 and 33 min in order to ensure minimal surface roughness and to obtain AlN layer thicknesses of 345 and 219 nm, respectively. Profilometer measurements of the AlN samples at the end of fabrication indicate surface roughness much less than 20 nm.

The AlGaN/GaN template, used for the fabrication of two samples depicted in Figure 3-18(c), start with 800 nm (*Al,Ga*)N transition layer followed by 800 nm GaN epi-layer, 17 nm AlGaN barrier and 2 nm GaN cap layer grown on the aforementioned AlN-on-Si structure again via MOCVD. 2-dimensional electron gas (2DEG) exists at the AlGaN – GaN interface of the GaN-on-Si template and it is confined in the GaN layer within approximately 2nm of the AlGaN-GaN interface for the given 2DEG concentrations [25].

It is essential to remove any traces of the 2DEG prior to CPW fabrication on GaN-on-Si as it would act as a conductive plane in close proximity to the transmission lines. 2DEG is removed from the GaN-on-Si template by etching the GaN cap, AlGaN barrier and a couple nanometers of the following GaN epi-layer via RIE. Using the same ICP-RIE recipe, GaN etch rate of 15 nm/min is obtained. 795 nm GaN sample was etched for only 1:40 min in order to obtain a GaN thickness close to the original value while ensuring all the 2DEG is removed. 15 min RIE etch was used to fabricate the final sample substrate of 595 nm GaN epi-layer.

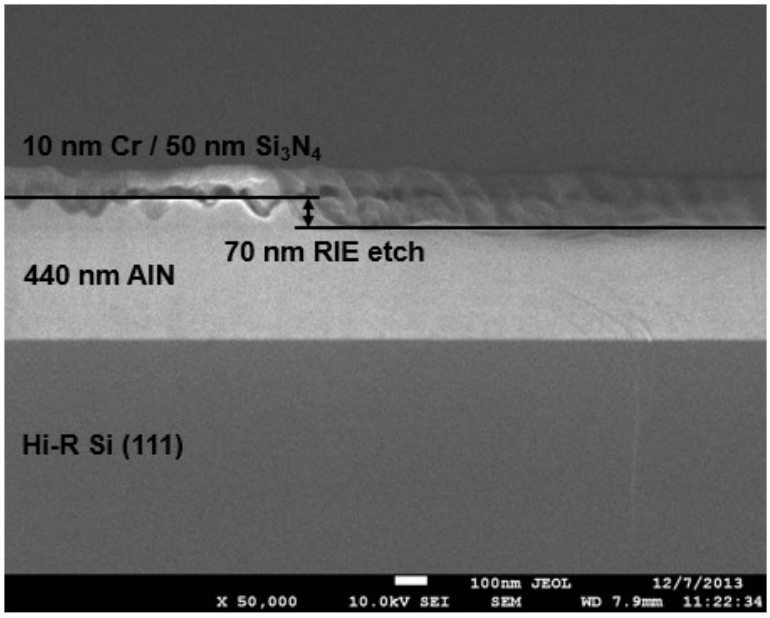


Figure 3-19 Cross-sectional SEM image of AlN-on-Si depicting the original surface roughness of the AlN layer and surface roughness after a 10-minute RIE etch.

After sample nitride etching and native oxide removal with buffered oxide etch (BOE) for Si, aluminum (Al) was deposited on all samples via electron beam evaporation. Al was

preferred over gold (Au) for the conductor metal due to cost and fabrication limitations. The only Au deposition method accessible was gold sputter which is limited in deposition thickness. Less than 100 nm thick Au can be deposited via sputtering, whereas the e-beam evaporator can easily go over 500 nm Al thickness. Despite having lower conductivity than Au, thick Al results in lower metal loss. Measured Al thickness for realized CPW structures is 680 nm on 800 nm GaN sample, 700 nm on 219 nm AlN sample and 780 nm on the other three samples. The variation in thickness is due to operation instability at such high deposition thicknesses. After Al deposition, CPWs were patterned using photolithography and Al wet etch. Show the top-view of a fabricated CPW.

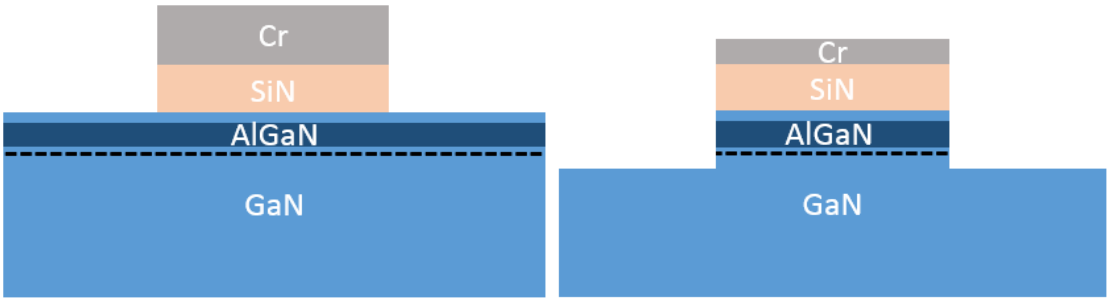
Figure 3-20 Picture of an Al CPW fabricated for GaN-on-Si substrate loss study.

3.3.2. 2DEG Device Fabrication

2DEG CPWs are fabricated using Nitronex AlGaN/GaN heterostructures. 2DEG exists throughout the whole wafer at a depth of ~20 nm, as depicted in Figure 3-18(c), as a conductive plane of approximately 2 nm thickness. In order to form 2DEG devices, the unwanted 2DEG portions need to be removed. 2DEG can be removed either by recess etch

or by isolation doping. Due to cost and ease of access, recess etch with RIE is preferred in this study.

In order to selectively RIE etch the 2DEG between the devices and keep it in the active areas, a mask that will withstand the plasma-etch process is needed. Cr with underlying SiN is deposited over the substrate and patterned as a hard mask for this purpose. The RIE recipe for GaN, detailed in Section 3.3.1, has an etch rate of 6 nm/min for Cr. In order to withstand up to 15 min RIE etch, 100 nm of Cr is deposited over the samples. 134 nm SiN deposition is realized with PECVD, whereas Cr is deposited via e-beam evaporation. After the deposition, Mask 1 of the first mask set is used to pattern both the Cr and the SiN. SiN and Cr are wet etched using BOE and Cr etchant, respectively, leaving both only in the areas where the 2DEG CPWs will be formed. After hard mask patterning, recess etch is realized via RIE for at least 1:40min, removing ~ 25 nm AlGaN/GaN, in order to ensure the removal of the 2DEG. 2DEG recess etch described so far is depicted in Figure 3-21 (a) and (b) showing the cross-sectional view before and after the RIE etch, respectively.



(a) (b)

Figure 3-21 Cross-sectional schematic of AlGaN/GaN recess etch (a) before and (b) after RIE etch.

Following the RIE etch, both Cr and SiN that served as the hard mask is removed, again via wet etch. As it is difficult to distinguish the edges of the patterned GaN, with or without the SiN, through the aligner microscope, some of the SiN/Cr stack is left behind as alignment markers. In order to achieve this, Mask 2 is used to pattern the photoresist to cover the SiN/Cr stack in alignment marker regions prior to wet etch. Once all the plasma damaged Cr/SiN stack, except for the alignment markers, is removed, new SiN is deposited via PECVD to provide passivation for the GaN and AlGaN/GaN surfaces.

Finally ohmic contacts are created using two masks, through the fabrication steps depicted in Figure 3-22. Mask 3 is first used to pattern the blanket SiN covering the sample and open the contact areas again using BOE wet etch as shown in Figure 3-22(a). Next, Mask 4 is used for liftoff photolithography, after which liftoff resist and photoresist is left in the areas from where the ohmic contact metal need to be removed. At the end of this step, all the sample surface, except for the contact regions, is covered with resist as depicted in Figure 3-22(b). Before contact metal deposition, the last step is to clean the active regions in the contact openings with HCl:DI (1:10) mixture. The samples are immediately placed in vacuum in the e-beam evaporator for the metal deposition after the HCl clean. 30 nm Ti, 180 nm Al and 40 nm Ni are deposited consecutively without breaking the vacuum in order to avoid oxidation between the metals in the ohmic metal stack. Final step of 50 nm gold (Au) deposition is realized with gold sputter and the time between e-beam and sputter depositions is minimized to avoid oxidation in between. Once the metal stack is deposited over the whole wafer, metal liftoff is realized by dipping the samples in AZ400T, which removes the remaining resist and any metal over it, as shown

in Figure 3-22 (c) and (d), respectively. In order for the AZ400T to reach the underlying resist and dissolve it, the total metal thickness needs to be less than 2/3 of the total resist thickness. The liftoff recipe used in this study, produces a PR/LOR total thickness of over 2 µm. Using rotation during the e-beam metal deposition enables uniform metal thickness over the sample but makes the liftoff process very difficult due to sidewall coverage.

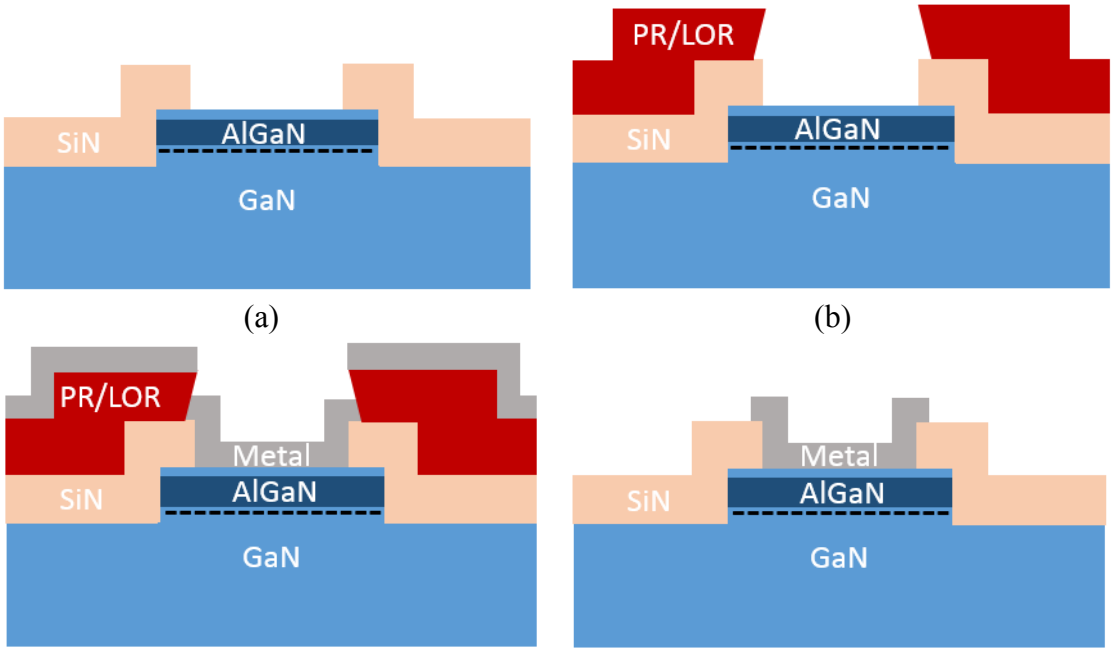


Figure 3-22 2DEG Ohmic contact fabrication flow: (a) contact opening (b) Lift-off photolithography (c) Ohmic contact metal deposition (d) Metal liftoff.

At this point the contact is not ohmic due to differences in metal-dielectric work functions. After the metal is placed over the contact regions, rapid thermal processing (RTP) is used to create ohmic contacts. Samples are RTP annealed in N_2 at 865°C for 30 sec. Ohmic contacts of the 2DEG CPW after RTP is depicted in Figure 3-23.

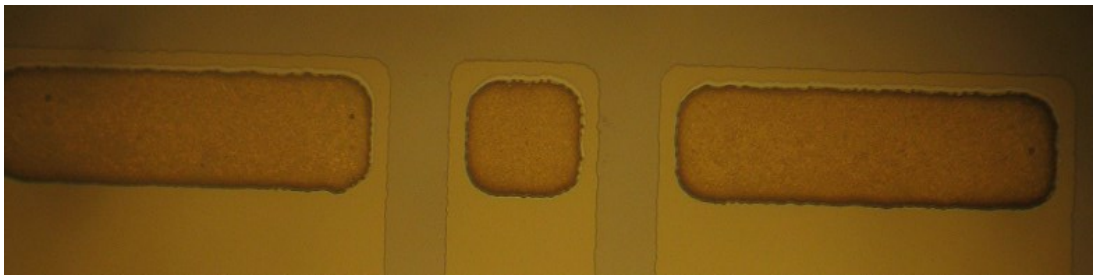


Figure 3-23 2DEG CPW and ohmic contacts after RTP

2DEG fabrication with Mask set 2 follows the exact steps as Mask set 1 until the end of ohmic contact formation. After ohmic contacts undergo RTP, Al is deposited over the sample and then a fifth mask is used to pattern the Al to fabricate the measurement pads and other interconnects. Figure 3-24 depicts an example of fabricated 2DEG transmission line test structure and its open / short de-embedding structures.

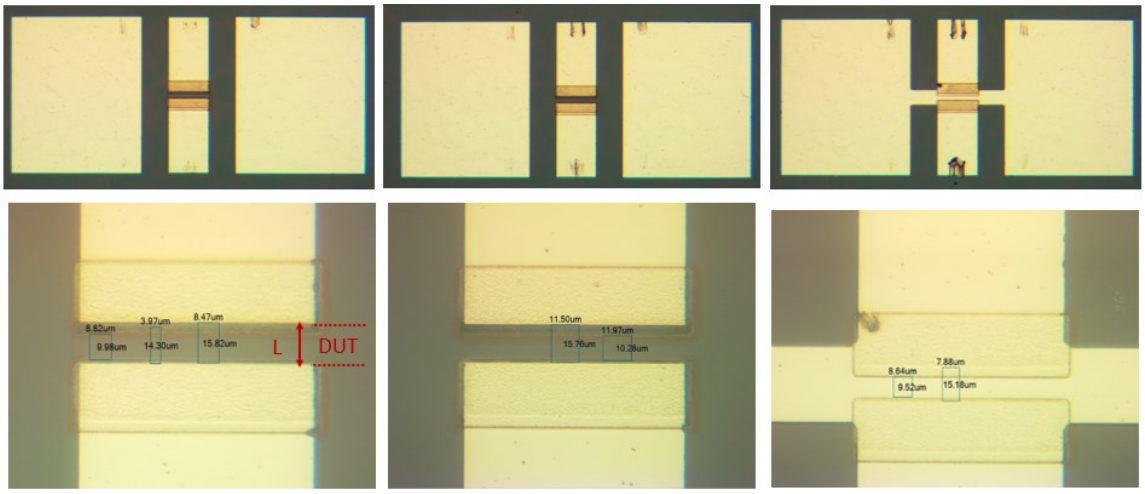


Figure 3-24 2DEG transmission lines and de-embedding structures fabricated using mask set II

3.3.3. Electrically Insulating PECVD SiN Development

One main problem encountered in the first design cycle of the 2DEG CPWs was the leaky behavior of the PECVD SiN. The IV measurements revealed that the SiN that is used to passivate the AlGaN/GaN and GaN surfaces acted as a main leakage path between to adjacent 2DEG regions. The leakage current was measured to be only one order of magnitude smaller than the current in the main conduction path as depicted in Figure 3-25. This necessitated a study into PECVD SiN fabrication and optimization of the SiN recipe.

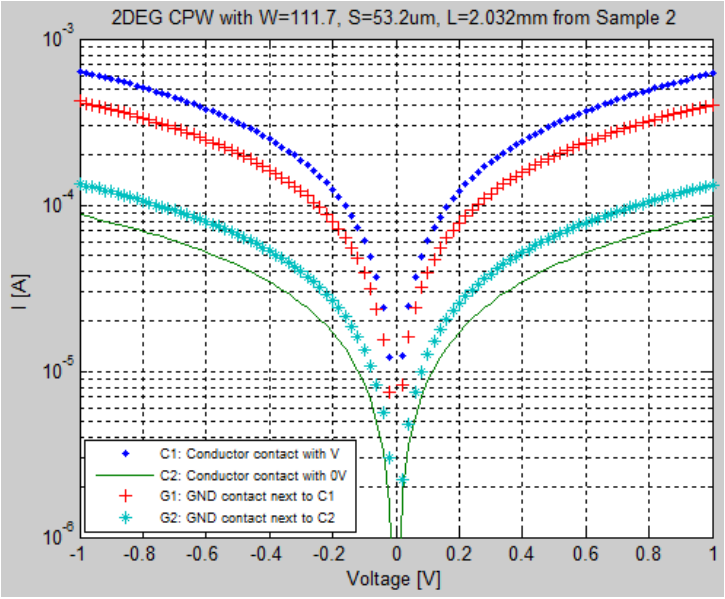


Figure 3-25 Conduction through a 2DEG conductor and the leakage currents at the grounded adjacent 2DEG conductor due to conducting SiN passivation layer.

PECVD SiN properties are known to vary based on the process parameters used. Depending on the PECVD process used, the dielectric strength of the SiN changes between 1 to 5 MV/cm, whereas the resistivity can be anywhere between 10^7 Ωmm to

10^{15} Ωmm. PECVD process parameters that determine the Si_3N_4 properties are SiH_4, N_2 and He flows, process temperature and RF power. These parameters determine the N/Si ratio, H content and bonding, and as a result the electrical quality. For example, low SiH_4 flow results in large H content with larger fraction of N-H groups. This causes H diffusing in SiN and, as a result, trap formation. The final product is a 'leaky' SiN.

Optical and DC measurements were conducted to verify the quality of the SiN produced by the developed PECVD recipe. Optimized SiN has high resistivity and higher etch rate. Refractive index is measured to be n≈1.97-1.99 which implies N/Si ratio of approximately 1.3 with optimal H content. The DC measurements, plotted in Figure 3-26, indicate approximately 3 orders of magnitude lower leakage currents.

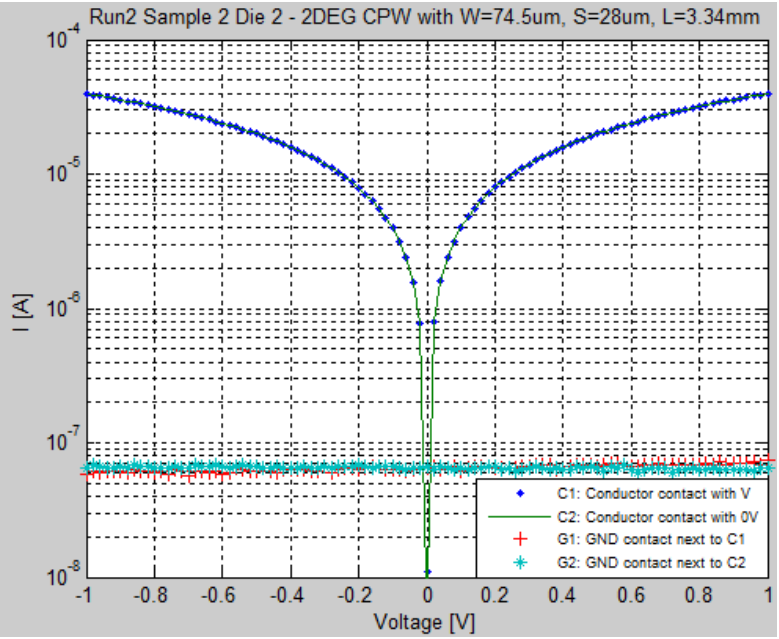


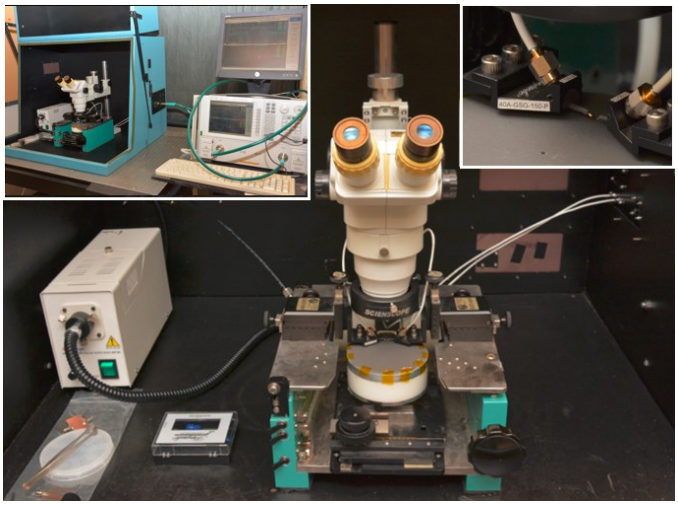
Figure 3-26 Leakage current reduction with optimized SiN recipe

3.4. Measurement Setup

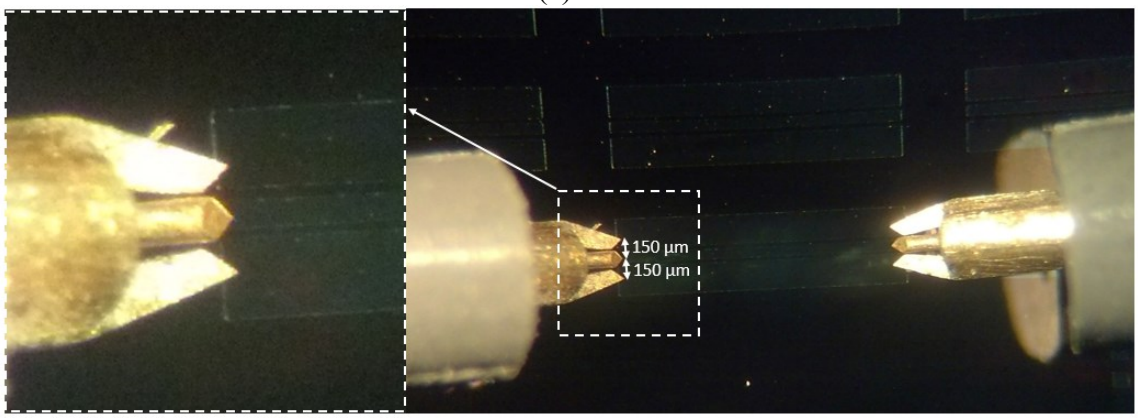
S-parameter measurements for the fabricated CPWs were taken using RF probes with Ground-Signal-Ground configuration and an Agilent E8362C PNA Microwave Network Analyzer over 6-20 GHz range, 0 dBm power and 500 Hz IF bandwidth. Single RF sweep rather than continuous was employed to avoid heating related drift. Measurements were conducted in the dark to avoid carrier generation. The floating metal chuck was covered with an electrically non-conductive RF absorber to minimize parasitic modes. Measurement setup with the probe station and instrumentation is depicted in Figure 3-27(a). Figure 3-27(b) shows a picture taken through the microscope of the RF probes with 150 μm pitch over the fabricated CPW structures, with the inset illustrating the approximate probing position.

SOLT (short-open-load-through) calibration was performed at the beginning of the measurements using an impedance standard substrate (ISS). On-wafer TRL (through-reflect-line) standards were fabricated, but SOLT calibration was preferred over TRL calibration because of initial difficulties in obtaining reliable calibration results with the on-wafer TRL standards. Lack of accuracy and repeatability of the on-wafer TRL calibration is attributed to imperfect TRL standards due to GaN material and fabrication tolerances, relatively high dielectric losses for AlN-on-Si, and poor contact-pad repeatability on aluminum. Using commercially available precision standards enabled more reliable SOLT calibration than on-wafer TRL calibration. SOLT is an accurate calibration for low frequency ranges, especially when similar substrate dielectric constants and transmission line geometries are used for both the calibration standards and DUT [52-

54]. Coplanar standards on alumina substrate are used for the SOLT calibration. Maximum frequency is limited to 20 GHz to achieve the required accuracy for this study and the minimum frequency is limited to 6 GHz to avoid calibration errors related to dispersion below 5 GHz for the given ISS.



(a)



(b)

Figure 3-27 (a) Probe station used for the measurements with the insets depicting the full measurement setup and the probes and (b) RF probes over the fabricated CPW structures with the inset depicting the approximate probing position.

4. DATA EXTRACTION METHODOLOGY

4.1. Transmission Parameters from S-parameter Measurements

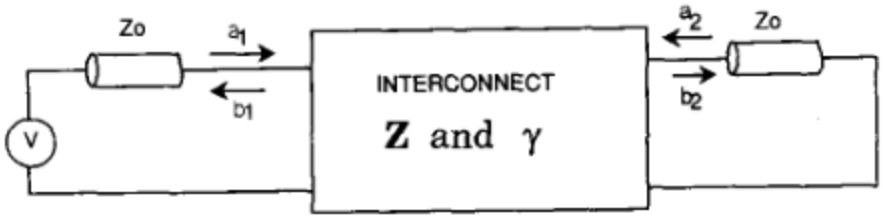


Figure 4-1 S-parameter measurement setup

S-parameters of a transmission line of characteristic impedance Z and propagation constant of γ in a system with impedance Z_0 are:

$$[\boldsymbol{S}] = \begin{bmatrix} \boldsymbol{S_{11}} & \boldsymbol{S_{12}} \\ \boldsymbol{S_{21}} & \boldsymbol{S_{22}} \end{bmatrix} \tag{4-1}$$

$$= \frac{\mathbf{1}}{\boldsymbol{D_s}} \begin{bmatrix} \left(\boldsymbol{Z^2 - Z_0^2}\right)\mathbf{sinh}\,\boldsymbol{\gamma l} & \boldsymbol{2ZZ_0} \\ \boldsymbol{2ZZ_0} & \left(\boldsymbol{Z^2 - Z_0^2}\right)\mathbf{sinh}\,\boldsymbol{\gamma l} \end{bmatrix}$$

where

$$\boldsymbol{D_s} = \boldsymbol{2ZZ_0}\,\mathbf{cosh}\,\boldsymbol{\gamma l} + \left(\boldsymbol{Z^2 + Z_0^2}\right)\mathbf{sinh}\,\boldsymbol{\gamma l} \tag{4-2}$$

The equivalent ABCD matrix is given by:

$$[\boldsymbol{ABCD}] = \begin{bmatrix} \mathbf{cosh}\,\boldsymbol{\gamma l} & \boldsymbol{Z}\,\mathbf{sinh}\,\boldsymbol{\gamma l} \\ \dfrac{\mathbf{sinh}\,\boldsymbol{\gamma l}}{\boldsymbol{Z}} & \mathbf{cosh}\,\boldsymbol{\gamma l} \end{bmatrix} \tag{4-3}$$

The relationship between s-parameters and ABCD matrix is:

$$\boldsymbol{A} = (\mathbf{1} + \boldsymbol{S_{11}} - \boldsymbol{S_{22}} - \Delta\boldsymbol{S})/(\boldsymbol{2S_{21}}) \tag{4-4}$$

$$\boldsymbol{B} = (\mathbf{1} + \boldsymbol{S_{11}} + \boldsymbol{S_{22}} + \Delta\boldsymbol{S})\boldsymbol{Z_0}/(\boldsymbol{2S_{21}})$$

$$\boldsymbol{C = (1 - S_{11} - S_{22} + \Delta S)/(2S_{21}Z_0)}$$

$$\boldsymbol{D = (1 - S_{11} + S_{22} - \Delta S)/(2S_{21})}$$

$$\boldsymbol{\Delta S = S_{11}S_{22} - S_{21}S_{12}}$$

Combining (4-1) to (4-4), propagation contant in terms of S-parameters is obtained as:

$$\boldsymbol{e^{-\gamma l} = \left\{\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K\right\}^{-1}} \tag{4-5}$$

where

$$\boldsymbol{K = \left\{\frac{\left(S_{11}^2 - S_{21}^2 + 1\right)^2 - (2S_{11})^2}{(2S_{21})^2}\right\}^{\frac{1}{2}}} \tag{4-6}$$

The real and imaginary parts of propagation constant give the attenuation and phase constants, respectively:

$$\boldsymbol{\gamma = \alpha + j\beta} \tag{4-7}$$

For a well-matched system with $S_{11} = 0$, propagation constant becomes equal to S_{21}, with its magnitude and phase yielding the attenuation and phase constants, respectively.

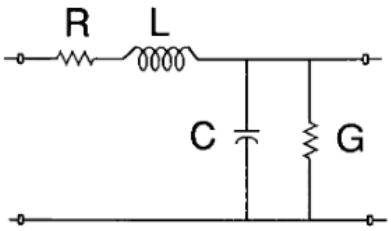


Figure 4-2 Transmission line representation from Telegrapher's equation model

From (4-1) to (4-4), the line impedance is also obtained as a function of s-parameters as:

$$\boldsymbol{Z^2 = Z_0^2 \frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}} \tag{4-8}$$

Propagation constant and characteristic impedance are related to transmission line RLCG parameters, depicted in Figure 4-2, through:

$$\boldsymbol{\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}} \tag{4-9}$$

$$\boldsymbol{Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}}} \tag{4-10}$$

Unit resistance, inductance, conductance and capacitance of the line can be obtained from the propagation constant and line impedance as:

$$\boldsymbol{R = \mathrm{Re}\{\gamma Z\}} \tag{4-11}$$

$$\boldsymbol{L = \mathrm{Im}\{\gamma Z\}/\omega}$$

$$\boldsymbol{G = \mathrm{Re}\{\gamma / Z\}}$$

$$\boldsymbol{C = \mathrm{Im}\{\gamma / Z\}/\omega}$$

(4-9) is simplified for G ≈ 0 as [35]:

$$\boldsymbol{\gamma = j\omega\sqrt{LC}\left[1 - \frac{jR}{2\omega L}\right]} \tag{4-12}$$

from which:

$$\boldsymbol{\alpha = \frac{R}{2}\sqrt{\frac{C}{L}} \quad \& \quad \beta = \omega\sqrt{LC} \quad \text{for } G \approx 0} \tag{4-13}$$

For the low-loss case with ωL >> R and ωC >> G:

$$\alpha = \mathbf{0} \quad \& \quad \beta = \omega\sqrt{LC} \quad \& \quad Z_0 = \sqrt{\frac{L}{C}} \tag{4-14}$$

RLCG parameters in terms of line geometry and material properties are given in Table 4-1 for microstrip and CPW.

Table 4-1 RLCG parameters for parallel-plate transmission line and CPW

	R (Ω/m)	**L (H/m)**	**C (F/m)**	**G (S/m)**
Microstrip	$\frac{\mathbf{R_{sh}}}{\boldsymbol{W}}$	$\frac{\boldsymbol{\mu d}}{\boldsymbol{W}}$	$\frac{\varepsilon' W}{t}$	$\frac{(\omega\varepsilon'' + \sigma)W}{t}$
CPW	$\mathbf{R}_s g$	$\mu_0 \frac{K(k)}{K'(k)}$	$\varepsilon_{eff}\varepsilon_0 \frac{K'(k)}{K(k)}$	$(\omega\varepsilon'' + \sigma)\frac{K'(k)}{K(k)}$

Information about the line impedance can also be obtained from the input and output reflection coefficients in Smith chart. For the transmission line of impedance Z, terminated by Z_L, the reflection coefficient and the input impedance at a distance d from the termination are given by:

$$\boldsymbol{\Gamma_L = \frac{Z_L - Z}{Z_L + Z}} \tag{4-15}$$

$$\boldsymbol{Z_{in} = Z\frac{Z_L + jZ tan\beta d}{Z + jZ_L tan\beta d}} \tag{4-16}$$

For short circuit termination, $\Gamma = -1$ and the input impedance $Z_{in-short} = jZtan\beta d$. Open circuit termination yields $\Gamma = +1$ and $Z_{in} = -jZ_0/tan\beta d$. For short transmission lines with $d/\lambda << 1$, input impedance for short and open termination becomes $Z_{in-short} \approx jZ_0\beta d$ and $Z_{in-short} \approx -jZ_0/\beta d$, respectively. $\Gamma = 0$ in case of matched load and varies between +1 and -1 for any mismatch. Mismatch loss is calculated from the real part of reflection coefficient, ρ, as:

$$\alpha_{mismatch} = -10\log(1-\rho^2) \quad \text{(dB)} \tag{4-17}$$

4.2. CPW Loss Mechanisms

Loss of the CPWs is calculated from the magnitude of S_{21}. Measured loss is a function of transmission length and the unit loss (S_{21}/L) is same for CPWs of similar geometries. Unit loss is used for most of the analysis. Mean and 95% confidence interval of the unit loss are calculated using measurements taken from re-probing of a given CPW and also by including CPWs of different length and position in order to account for measurement repeatability, noise, and substrate and fabrication variations.

Total measured loss of a transmission line is attributed to metal, dielectric and radiation losses.

$$\boldsymbol{\alpha = \alpha_{metal} + \alpha_{dielectric} + \alpha_{radiation}} \tag{4-18}$$

Reflections due to impedance mismatch between the transmission line and the analyzer ports can affect the loss measurement. In case of large impedance mismatch, mismatch loss should be factored in to (4-18). Mismatch loss is calculated from measured input reflection coefficient as:

$$\boldsymbol{\alpha_{mismatch} = -10\log(1-S11^2) \quad (dB)} \tag{4-19}$$

Phase of transmission is calculated from the angle of S21/S12 and is given by:

$$\boldsymbol{\beta\,(l,f) = \frac{2\pi f}{c}\sqrt{\varepsilon_{eff}(f)}\cdot l} \tag{4-20}$$

where $\varepsilon_{eff}(f)$ is the frequency dependent effective permittivity of the coplanar structure and l is the transmission length. $\varepsilon_{eff}(f)$, hence the unit phase, is dependent on CPW geometry and cutoff frequency for TE_1 mode. $\varepsilon_{eff}(f)$ is extracted from the unit phase.

In order to observe the change in loss due to GaN-on-Si epilayers, dielectric loss is extracted from the measured loss according to (4-18). Radiation loss and metal loss are calculated as described below.

The attenuation due to radiation loss of a CPW, including the effect of radiation angle and the frequency dependence of effective dielectric constant, is given as [29]:

$$\boldsymbol{\alpha_{radiation}} = \left(\frac{\boldsymbol{\pi}}{\boldsymbol{2}}\right)^{\boldsymbol{5}} \boldsymbol{2} \left(\frac{\left(\boldsymbol{1} - \frac{\boldsymbol{\varepsilon_{eff}(f)}}{\boldsymbol{\varepsilon_r}}\right)^{\boldsymbol{2}}}{\sqrt{\frac{\boldsymbol{\varepsilon_{eff}(f)}}{\boldsymbol{\varepsilon_r}}}} \right) \frac{(\boldsymbol{W}+\boldsymbol{2S})^{\boldsymbol{2}} \boldsymbol{\varepsilon_r}^{\boldsymbol{3/2}}}{\boldsymbol{c^3 K'(k) K(k)}} \boldsymbol{f^3} \qquad (4\text{-}21)$$

where W is the center conductor width, S is the separation between the center conductor and the ground conductors, $K(k)$ is the complete elliptic integral of the first kind with $k = W/(W+2S)$, and $K'(k) = K(\sqrt{1-k^2})$. (4-21) is expected to be valid for geometries with $0.1 < W/S < 10$, $h > 2S$, and $\lambda > W+2S$ [29]. Note that the elliptic integral of this equation assumes infinite ground planes. In order to take into account the effect of finite ground planes, elliptic integral is evaluated with:

$$\boldsymbol{k} = \frac{\boldsymbol{x_c}}{\boldsymbol{x_b}} \sqrt{\frac{\boldsymbol{x_b^2 - x_a^2}}{\boldsymbol{x_c^2 - x_a^2}}}, \qquad (4\text{-}22)$$

where $x_a = W/2$, $x_b = W/2 + S$ and $x_c = W/2 + S + W_{GND}$ [31].

Metal loss for a transmission line is expressed with low-loss approximation as:

$$\alpha_{metal} \approx \frac{R}{2Z_0} \tag{4-23}$$

where Z_0 is the characteristic impedance and R is the unit resistance of the transmission line. Using the quasi-static approximation:

$$Z_0 = \frac{1}{Cv_{ph}} \tag{4-24}$$

$$v_{ph} = \frac{c}{\sqrt{\varepsilon_{eff}}} \tag{4-25}$$

$$\varepsilon_{eff} = \frac{C}{C_0} \tag{4-26}$$

where v_{ph} is the phase velocity, c is the speed of light, C is the line unit capacitance, and C_0 is the transmission line capacitance in absence of dielectrics. CPW C_0 is calculated using conformal mapping as [31]:

$$C_0 = 4\epsilon_0 \frac{K'(k)}{K(k)} \qquad \text{where} \quad \epsilon_0 = \frac{1}{\mu_0 c^2} \tag{4-27}$$

Substituting (4-25) to (4-27) in (4-24) with $\mu_0 = 4\pi \times 10^{-7}$ H/m, CPW characteristic impedance equation is obtained as [31]:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K(k)}{K'(k)}. \tag{4-28}$$

CPW unit resistance, R_{cpw}, is the sum of CPW center conductor series resistance, R_c, and distributed series resistance of ground planes, R_g:

$$R_c = \frac{R_s}{4W(1-k^2)K^2(k)}\left[\pi + \ln\left(\frac{4\pi W}{t}\right) - k\ln\left(\frac{1+k}{1-k}\right)\right] \tag{4-29}$$

$$R_g = \frac{kR_s}{4W(1-k^2)K^2(k)}\left[\pi + \ln\left(\frac{4\pi(W+2S)}{t}\right) - \frac{1}{k}\ln\left(\frac{1+k}{1-k}\right)\right] \quad (4\text{-}30)$$

where t is the CPW conductor thickness and R_s is the surface resistance of the conductor. Note that these equations assume the metal to be much thicker than the skin depth, δ_s, and therefore use the limit value of RF sheet resistance. Surface resistance is the lowest possible resistance for the conductor as the metal thickness goes to infinity. Taking into account the skin depth and integrating metal conductivity at different depths from surface to bottom, RF conductance of a metal is expressed as:

$$G_{RF} = \int_0^t \frac{1}{\rho} e^{-\frac{t}{\delta_s}} dt \quad \rightarrow \quad G_{RF,max} = \frac{\delta_s}{\rho} \quad \text{for } t = \infty \quad (4\text{-}31)$$

$$\delta_s = \sqrt{\frac{2\rho}{2\pi\mu_0\mu_r f}} \quad (4\text{-}32)$$

From (4-31) and (4-32), RF resistance and surface resistance are derived as:

$$R_{RF} = \frac{\rho}{\delta_s(1-e^{-t/\delta_s})} \quad (\Omega/\square) \quad (4\text{-}33)$$

$$R_s = R_{RF,min} = \sqrt{\pi\mu_0\mu_r\rho f} \quad \text{for } t = \infty \quad (4\text{-}34)$$

Surface resistance has linear dependence on square root of frequency and underestimates the resistance for metals thinner than skin depth, especially at low frequencies. Therefore, (4-33) instead of (4-34) is used in (4-29) and (4-30) as sheet resistance. R_{RF} is close to DC sheet resistance at low frequencies and increases with frequency as skin depth gets smaller. Note that DC sheet resistance of the metal is:

$$R_{DC} = \frac{\rho}{t} \quad (\Omega/\square) \quad (4\text{-}35)$$

For metal loss calculations, first DC resistance of the CPW conductors are measured in order to extract the metal conductivity from the measured sheet resistance through (4-35). Using the measured conductivity of the e-beam deposited Al, RF resistance and CPW unit resistance are calculated for each sample Al thickness. Characteristic impedance is then calculated as (4-28) with the extracted effective permittivity. Finally the metal loss is calculated from (4-23).

Calculated radiation and metal losses are subtracted from the measured loss to obtain the dielectric loss of each sample. Dielectric loss mechanisms, related dielectric parameters and their extraction from the measured data are explained in detail in the next section.

4.3. Dielectric Parameters from CPW Measurements

For an EM wave with wave function $\mathrm{E} = \mathrm{E}_0 e^{j\omega t}$ propagating through a dielectric, Maxwell's curl equation for the magnetic field is given by:

$$\boldsymbol{\nabla \times \mathbf{H} = j\omega\varepsilon' \mathbf{E} + (\omega\varepsilon'' + \sigma)\mathbf{E}} \tag{4-36}$$

where σ is the conductivity and ε' and ε'' are the real and imaginary parts of the dielectric's complex permittivity:

$$\boldsymbol{\varepsilon = \varepsilon' - j\varepsilon'' \quad \text{and} \quad \varepsilon' = \varepsilon_r \varepsilon_0} \tag{4-37}$$

Real and imaginary parts of (4-36) represent the lossless and lossy reaction to E, respectively. ε'' quantifies the loss attributed to bound charge and dipole relaxation, whereas σ quantifies loss due to free charge conduction. The loss tangent of the dielectric is defined as the ratio of lossy to lossless reaction to E in (4-36):

$$\tan\delta = \frac{\omega\varepsilon'' + \sigma}{\omega\varepsilon'} = \frac{\varepsilon''}{\varepsilon'} + \frac{\sigma}{\omega\varepsilon'} \tag{4-38}$$

Loss tangent given by (4-38) is also referred to as *effective loss tangent* ($tan\delta_{eff}$) to differentiate it from the dielectric loss tangent ($tan\delta_d$) that is only a function of complex permittivity but not conductivity:

$$\tan\delta_d = \frac{\varepsilon''}{\varepsilon'} \tag{4-39}$$

Based on (4-38) and (4-39), minimum value of a material's dielectric loss is determined by its complex permittivity. Conductivity of the material introduces additional loss factor that is inversely proportional to frequency. $tan\delta_{eff}$ approaches $tan\delta_d$ as the frequency increases. (4-38) is plotted in Figure 4-3 for various values of σ, depicting the increasing slope for $\tan\delta_{eff}$ with increasing conductivity.

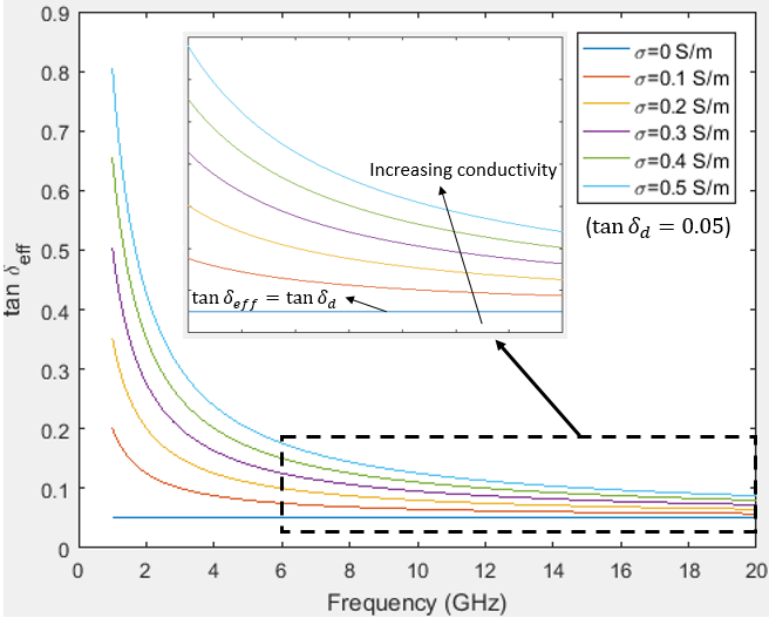


Figure 4-3 Variation in effective dielectric loss with conductivity

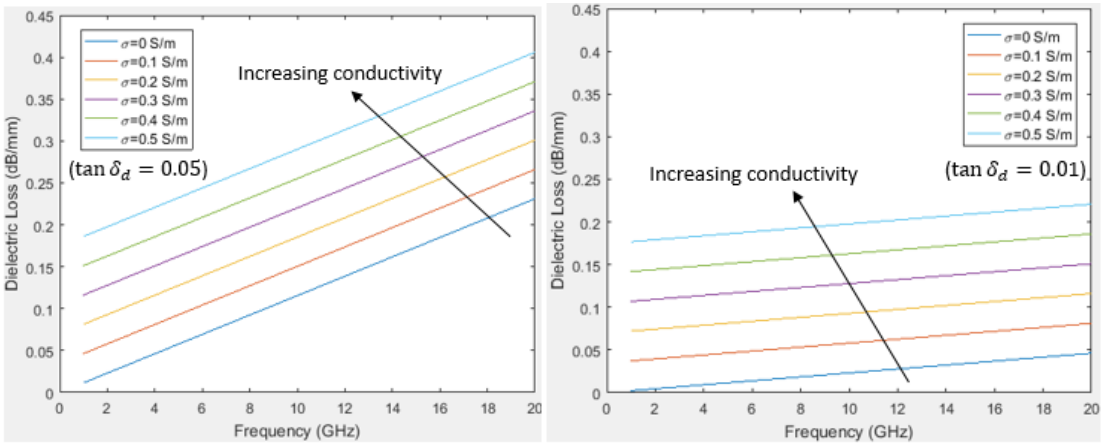
Dielectric loss of a material is given by:

$$\boldsymbol{\alpha_{dielectric} = \frac{\pi\sqrt{\varepsilon_{eff}}}{c} \cdot \tan\delta \cdot f} \tag{4-40}$$

Substituting (4-38) and (4-39) into (4-40) yields:

$$\boldsymbol{\alpha_{dielectric} = \frac{\pi\sqrt{\varepsilon_{eff}}}{c} \cdot \tan\delta_d \cdot f + \frac{\sqrt{\varepsilon_{eff}}}{2\varepsilon_0\varepsilon_r c} \cdot \sigma} \tag{4-41}$$

(4-41) indicates the effect of both $tan\delta_d$ and σ on dielectric loss. Conductivity adds a constant increase to dielectric loss, whereas dielectric loss tangent determines the slope of dielectric loss – frequency curve as depicted in Figure 4-4.



(a) (b)

Figure 4-4 Variation in dielectric loss with σ for (a) $tan\delta_d$ =0.05 and (b) $tan\delta_d$ =0.01

Effective loss tangent of the samples is calculated using (4-40). Conductivity and dielectric loss tangent are then extracted through linear regression using (4-41). Note that $tan\delta_d$ given by (4-39) and ε_r are assumed to be constant for the analysis in this study assuming a frequency-independent complex permittivity. In reality, the there are various

frequency dependent loss mechanisms due to polarization of charges under electric field, which determine the frequency dependent value of both ε′ and ε″ as depicted in Figure 4-5. Note that a good linear fit on (4-41) is only possible in case of frequency independent complex permittivity.

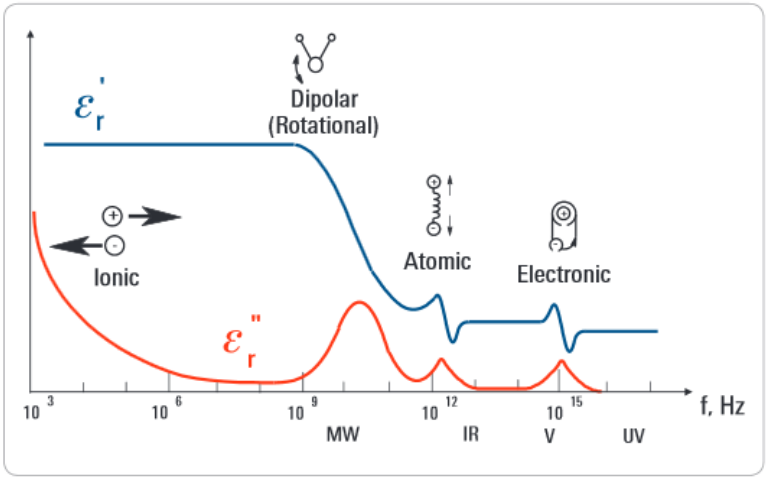


Figure 4-5 Frequency response of dielectric materials and corresponding variation in dielectric complex permittivity [55]

4.4. Loss Mechanisms of AlN-on-Si

Two loss mechanisms are expected to contribute to the dielectric loss observed in GaN-on-Si. One is the conductivity of the epi-layers and the other is a previously reported conductive layer at the Si-AlN interface [23]. In order to determine the relative contribution of both mechanisms on the overall loss, loss increase in AlN-on-Si samples, with different AlN epi-layer thickness, compared to Si is analyzed. The analysis is based on simulations due to lack of dielectric loss equations that include relative contribution of conductivities in multi-layer substrates.

Contributions of AlN and interface layer conductivities on overall loss are determined via simulations using Sonnet®. An AlN layer with $\varepsilon_r = 8.6$ on 500 μm thick 10 kΩ-cm Si substrate with $\varepsilon_r = 11.9$ [3] is simulated with CPWs of the same dimensions and metal thicknesses as the fabricated structures. Dielectric loss tangents of 10^{-4} and 3×10^{-4} are used in the simulations for Si and AlN, respectively. These values are determined from the measurement data via calculation and simulation, matching the loss-frequency slope. Extracted $tan\delta_d$ for Si matches effective loss tangent and conductivity values reported in [56]. For simulations involving a conductive layer at the AlN-Si interface, a 2 μm layer is included in the Si substrate, based on the carrier concentration profile given by [24].

In order to assess their contributions to the overall loss, 219 and 345 nm thick AlN-on-Si layers were simulated, varying the AlN and interface layer conductivities parametrically. Relative error (RE) between the simulation and measurement data is calculated as:

$$\mathbf{RE} = \frac{\|\boldsymbol{\alpha}_{sim} - \boldsymbol{\alpha}_{data}\|}{\|\boldsymbol{\alpha}_{data}\|} = \frac{\sqrt{\sum_{i=1}^{n}\left(\boldsymbol{\alpha}_{sim,i} - \boldsymbol{\alpha}_{data,i}\right)^2}}{\sqrt{\sum_{i=1}^{n}\left(\boldsymbol{\alpha}_{data,i}\right)^2}} \tag{4-42}$$

After individually calculating RE according to (4-42) for 219 and 345 nm AlN samples simulated with the same AlN and interface layer conductivity combination, total relative error for that parameter combination is calculated as:

$$\mathbf{TRE} = \mathbf{RE_{219}} + \mathbf{RE_{345}} \tag{4-43}$$

TRE is calculated for various AlN and interface conductivity combinations. Parameters combinations that yield the lowest TRE values are accepted as the possible values AlN and interface conductivities can attain.

4.5. Open–Short De-embedding Algorithm

For the 2DEG transmission line embedded in CPW test pads, the parasitics series and parallel circuit elements, depicted in Figure 4-6, are de-embedded using open and short structures.

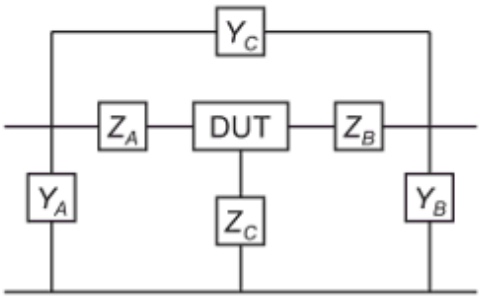


Figure 4-6 Series and parallel parasitics circuit elements for open-short deembedding

First step in de-embedding is conversion of the s-parameters from three measurements to y-parameters (Y_{DUT}, Y_{OPEN}, Y_{SHORT}). In order to subtract Y_A, Y_B and Y_C from DUT data, first Y_{OPEN} is subtracted from Y_{DUT} to obtain intermediate Y-matrix, Y_{DUT2}. Y_{OPEN} is also subtracted from Y_{SHORT} to obtain another intermediate Y-matrix, Y_{SHORT2}. Both intermediate Y-matrices are then converted into Z-matrices. Finally the de-embedded DUT Z-parameter matrix is calculated by subtracting Z_{SHORT2} from Z_{DUT2}.

The de-embedded parallel and series circuits elements are given by:

$$\mathbf{Y}_{\boldsymbol{C}} = -\mathbf{Y}_{\boldsymbol{OPEN}(\mathbf{1},\mathbf{2})} = -\mathbf{Y}_{\boldsymbol{OPEN}(\mathbf{2},\mathbf{1})} \tag{4-44}$$

$$\mathbf{Y}_{\boldsymbol{A}} = \mathbf{Y}_{\boldsymbol{OPEN}(\mathbf{1},\mathbf{1})} - \mathbf{Y}_{\boldsymbol{C}}$$

$$\mathbf{Y}_{\boldsymbol{B}} = \mathbf{Y}_{\boldsymbol{OPEN}(\mathbf{2},\mathbf{2})} - \mathbf{Y}_{\boldsymbol{C}}$$

$$\mathbf{Z}_{\boldsymbol{C}} = \mathbf{Z}_{\boldsymbol{SHORT2}(\mathbf{1},\mathbf{2})} = \mathbf{Z}_{\boldsymbol{SHORT2}(\mathbf{2},\mathbf{1})}$$

$$\mathbf{Z}_{\boldsymbol{A}} = \mathbf{Z}_{\boldsymbol{SHORT2}(\mathbf{1},\mathbf{1})} - \mathbf{Z}_{\boldsymbol{C}}$$

$$\mathbf{Z}_{\boldsymbol{B}} = \mathbf{Z}_{\boldsymbol{SHORT2}(\mathbf{2},\mathbf{2})} - \mathbf{Z}_{\boldsymbol{C}}$$

5. GAN-ON-SI SUBSTRATE CHARACTERIZATION

CPW lengths used in the analysis are tabulated in Table 5-1. They are different from the designed lengths as different amounts of overdrive were required during probing in order to remove the aluminum oxide at the contact points. The actual transmission lengths were determined by measuring the distance between probe contact points under the microscope. Results were confirmed by comparing the phase shifts, which are proportional to length, from the same sample. Accuracy of transmission length affects the analysis as phase and loss are normalized to length and most of the analysis is based on normalized parameters.

Table 5-1 Transmission lengths for the CPWs

	Actual Transmission Lengths (mm)				
Designed L (mm)	Si	219 nm AlN	345 nm AlN	595 nm GaN	795 nm Gan
2.2	2.05	2.09	2.08	2.07	1.97
3.4	3.37	3.35	3.33	3.30	3.15
2.8	2.73	2.71	2.70	2.67	2.64
4	4.04	3.97	3.92	3.93	3.76

To account for measurement, substrate and fabrication variations, five measurements were taken by probing CPWs of different length and position and re-probing a given CPW.

S11 Smith Chart plots of 5 measurements from each sample are depicted in Figure 5-1. Smith chart plots indicate that the characteristic impedance of CPWs from all samples is close to 50 Ω, with a small and, generally, capacitive reactance. 800 nm GaN sample shows the least match to the 50 Ω test setup. Variations observed in S11 are mainly due

to probing, calibration, and noise from the RF measurements. Material and fabrication variations will also contribute to S11 differences.

Characteristic impedance for the 2.2 mm long CPW from each sample is calculated from s-parameters using (4-8). Real and imaginary parts of calculated Z_0 are depicted in Figure 5-2 (a) and (b), respectively. Real part of CPW characteristic impedance increases with frequency for all the samples from 49.5 – 51.5 Ω at 6 GHz to 51 – 54 Ω at 20 GHz. A decrease in real impedance is observed for 200 nm AlN, 400 nm AlN and 600 nm GaN samples with addition of epi-layers, which suggests an increase in CPW effective permittivity. However, Si and 800 nm GaN samples do not follow the same trend. Imaginary part of Z_0 for all samples, except for 600 nm GaN, indicate capacitive reactance over the whole frequency range. Among these samples, Si sample has higher capacitive reactance, while the other three show similar values. 600 nm GaN is the outlier with inductive reactance for frequencies lower than 13 GHz. Its reactance become capacitive and similar to other samples with epi-layers for higher frequencies.

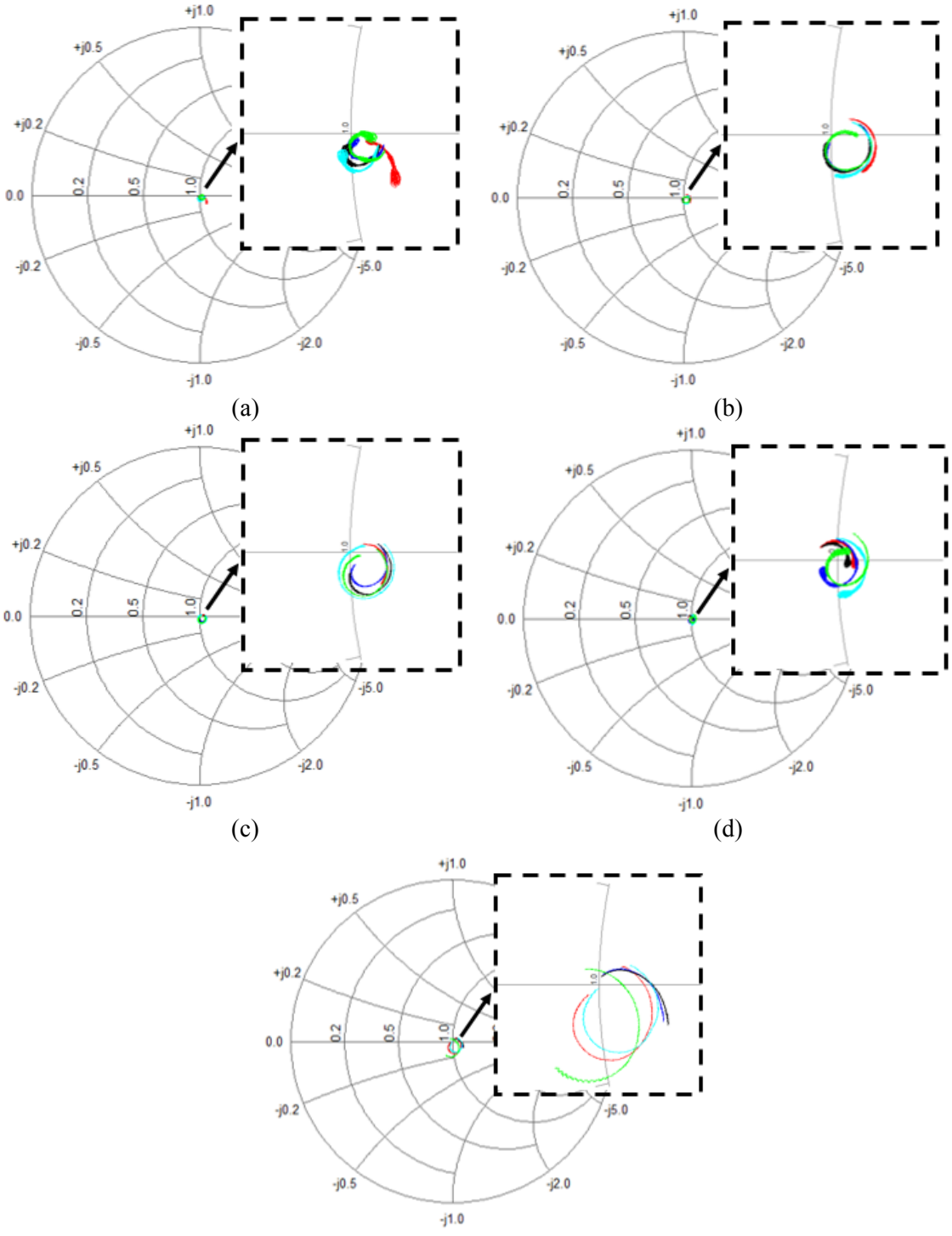
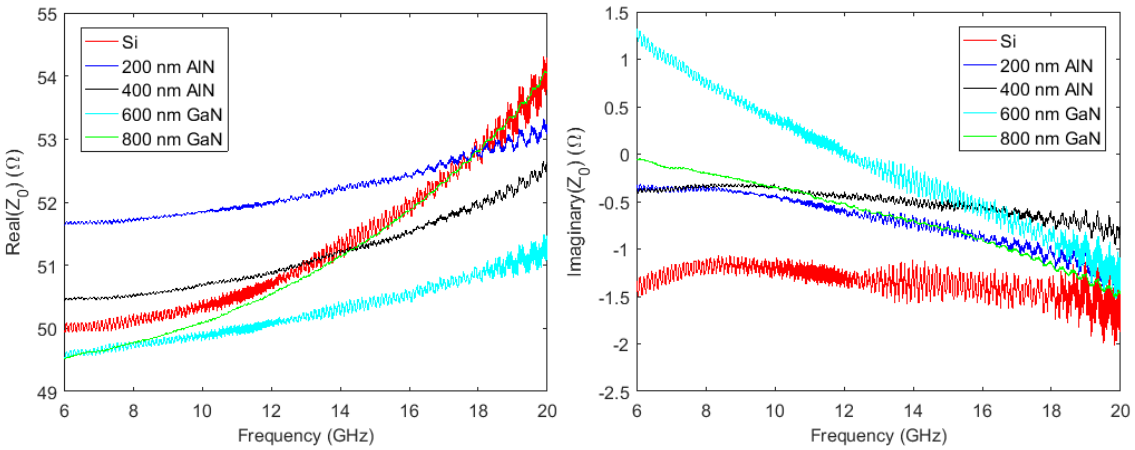


Figure 5-1 S11 Smith Chart plots of the five CPW measurements used in the analysis for (a) Si, (b) 200 nm AlN, (c) 400 nm AlN, (d) 600 nm GaN and (e) 800 nm GaN samples.



(a) (b)

Figure 5-2 (a) Real and (b) imaginary parts of the calculated Z_0 from 2.2 mm CPW of each sample

In order to assess the characteristic impedance variation observed, (4-10) that gives Z_0 in terms of RLCG parameters is expanded into:

$$\boldsymbol{Z = \sqrt{\frac{(RG + \omega L^2 C^2)}{G^2 + \omega^2 C^2} + j\frac{(\omega LG - \omega RC)}{G^2 + \omega^2 C^2}}} \tag{5-1}$$

The real term inside the square root is always positive, whereas the sign of the imaginary term depends on the RLCG values and also determines the nature of Z_0 reactance. Square root of a complex number is calculated as:

$$\sqrt{\boldsymbol{a + jb}} = \pm\frac{\boldsymbol{1}}{\sqrt{\boldsymbol{2}}}\left(\sqrt{\sqrt{\boldsymbol{a^2 + b^2}} + \boldsymbol{a}} + \boldsymbol{j}\sqrt{\sqrt{\boldsymbol{a^2 + b^2}} - \boldsymbol{a}}\right)$$

$$\sqrt{\boldsymbol{a - jb}} = \pm\frac{\boldsymbol{1}}{\sqrt{\boldsymbol{2}}}\left[\sqrt{\boldsymbol{a} + \sqrt{\boldsymbol{a^2 - b^2}}} - \boldsymbol{j}\sqrt{\boldsymbol{a} - \sqrt{\boldsymbol{a^2 - b^2}}}\right] \tag{5-2}$$

Based on (5-2), if the imaginary term of (5-1) is negative, i.e. RC > LG, then the reactance is capacitive. On the other hand, an inductive reactance indicates RC < LG. The reactance is expected to be capacitive at low frequencies and change to inductive as frequency

increases. Therefore, the inductive to capacitive transition of the reactance with increasing frequency for the 600 nm sample in Figure 5-2 and the similar trend observed in Figure 5-1 for some CPWs is not accurate.

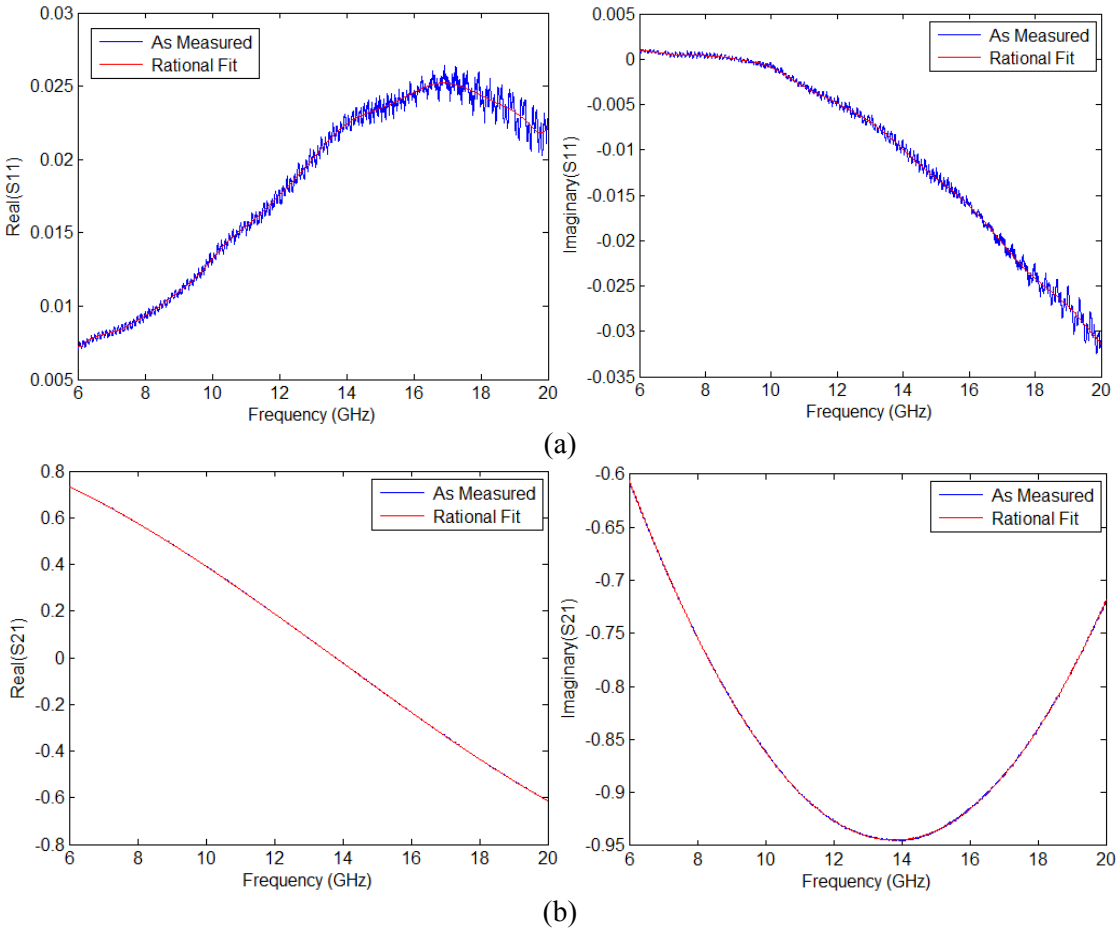


Figure 5-3 Measured and fitted (a) S11 and (b) S21 parameters for the 2.2 mm long CPW on 400 nm AlN.

While evaluating the calculated impedance values, two points need to be taken into consideration. First problem encountered during the Z_0 calculation is related to data and calculation precision. Real and imaginary parts of the S11 data are very small, on the order

of 10^{-2} to 10^{-3}, and very noisy due to small frequency steps and IF bandwidth used to improve the analyzer dynamic range. S11 values and their quality affect the results of square and square root calculations in (5-2). An example of the measured s-parameters is depicted in Figure 5-3 for the 2.2mm long CPW on 400 nm AlN sample. The figure also shows the s-parameters obtained through the *rationalfit( )* function in MATLAB. The fit closely follows the data and only smooths out the noise, especially in S11, as can be observed in the figure. Using the *smoother* s-parameter matrices for the Z_0 calculations results in up to 1 Ω variation in both the real and imaginary parts of Z_0 for all the samples.

A more general source of uncertainty is related to the RF measurement itself. Probing on Al pads is very inconsistent in terms of the contact resistance obtained. Al needs to be scratched through varying amounts of probe overdrive in order to minimize the contact resistance. During probing, Al residue also accumulates over the contact area and/or around the probe tip. Both the Al residue and the varying contact resistance will affect especially the measured reflection coefficients, and hence the extracted characteristic impedance. Therefore, the results depicted in Figure 5-2 include some degree of error due to both measurement and calculation uncertainties and the outlier curves in these figures are largely attributed to these uncertainties. Mean and 95% confidence intervals, calculated from 5 measurements for each sample, are used in the rest of the analysis to account for the aforementioned random variations in probing along with other sources of uncertainty.

The mean and 95% confidence interval of loss, normalized to unit length (S_{21}/L), from the five different samples are depicted in Figure 5-4.

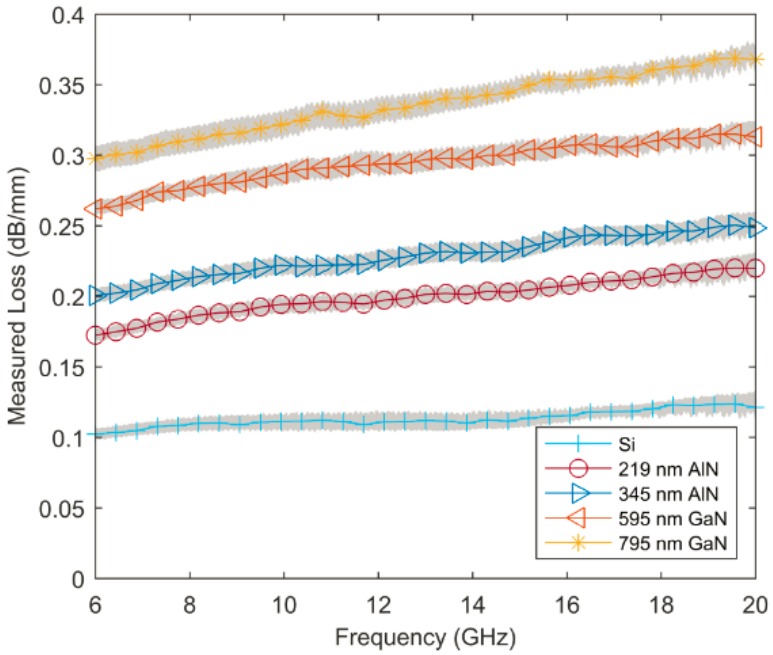


Figure 5-4 Mean and 95% confidence intervals of loss measurements from five samples.

Measured data clearly shows an increase in loss for samples with more or thicker epi-layers compared to the Si control sample. RF loss measured from CPWs on Si sample slightly increases with frequency from 0.10 dB/mm to 0.12 dB/mm. Similar CPW structures exhibit a loss of 0.17 to 0.22 dB/mm on 219 nm AlN sample and 0.20 to 0.25 dB/mm on 345 nm AlN sample for the same frequency range. GaN samples have higher measured loss within the same range: 0.26 – 0.31 dB/mm for 595 nm GaN and 0.30 – 0.37 dB/mm for 795 nm GaN. In order to accurately quantify the amount of increase in loss due to epilayers, variation in metal thickness of different samples and the resulting loss variation have to be taken into account.

Unit phase measured from all 5 samples and given in Figure 5-5 show a very small increase between Si sample and the other samples with added epi-layers. Effective

permittivity for the coplanar structures, calculated from phase using (4-20) and plotted in Figure 5-6, depict a more pronounced increase with addition of epi-layers. Effective permittivity also decreases with frequency for all the samples.

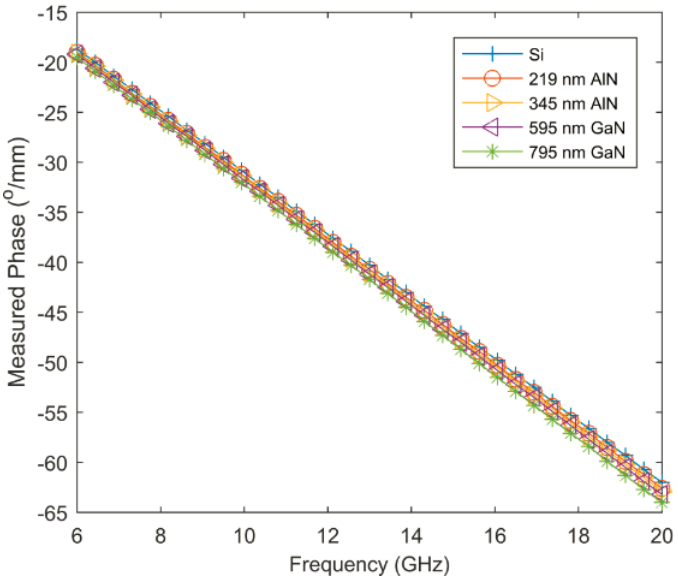


Figure 5-5 Mean unit phase from five samples

The empirical formula used to calculate frequency dependent effective permittivity of a coplanar structure is [30]:

$$\sqrt{\boldsymbol{\varepsilon_{eff}(f)}} = \sqrt{\boldsymbol{\varepsilon_q}} + \frac{\sqrt{\boldsymbol{\varepsilon_r}} - \sqrt{\boldsymbol{\varepsilon_q}}}{\left(\mathbf{1} + \boldsymbol{a}\left(\frac{\boldsymbol{f}}{\boldsymbol{f_{te}}}\right)^{-\boldsymbol{b}}\right)}, \tag{5-3}$$

where ε_q is the quasi-static effective permittivity and f_{te} is the cutoff frequency for TE_1 mode given by:

$$\boldsymbol{f_{te}} = \frac{\boldsymbol{c}}{\mathbf{4}\boldsymbol{h}\sqrt{\boldsymbol{\varepsilon_r} - \mathbf{1}}}. \tag{5-4}$$

The parameter b (≈1.8) is independent of geometry and a is related to geometry as:

$$\boldsymbol{\log(a) \approx u \log(W/S) + v,} \tag{5-5}$$

where

$$u \approx 0.54 - 0.64q + 0.015q^2,$$

$$v \approx 0.43 - 0.86q + 0.54q^2,$$

$$q = \log(W/h).$$

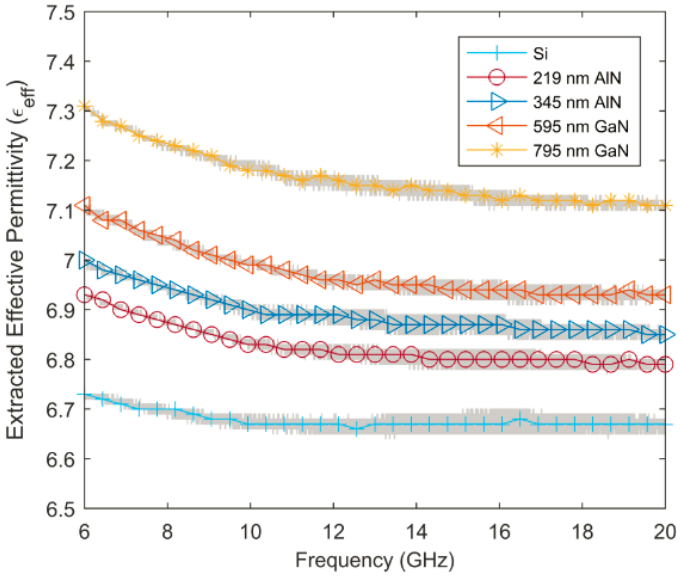


Figure 5-6 Mean and 95% confidence intervals for extracted effective permittivity of CPWs from five samples.

(5-3) is verified to be accurate within 5% for 0.1 < W/S < 5, 0.1 < W/h < 5, 1.5 < ε_r < 50, and 0 < f/f_{te} < 10. Note that quasi-static permittivity assumes equal field distribution in air and in the substrate:

$$\boldsymbol{\varepsilon_q = \frac{\varepsilon_r + 1}{2}.} \tag{5-6}$$

ε_q given by (5-6) is the average of air and substrate permittivities. A more accurate expression for the quasi-static permittivity takes into account uneven field distribution in air and in the dielectric using *filling factor*, *FF*, to indicate the percentage of fields in the material:

$$\boldsymbol{\varepsilon_q = \varepsilon_r \times FF + 1 \times (1 - FF)}. \qquad (5\text{-}7)$$

$\varepsilon_{eff}(f)$ given by (5-3) is plotted in Figure 5-7 for the sample CPW geometry in order to observe its frequency dependence. The figure shows an increase in $\varepsilon_{eff}(f)$ with frequency contrary to the trend observed in extracted $\varepsilon_{eff}(f)$.

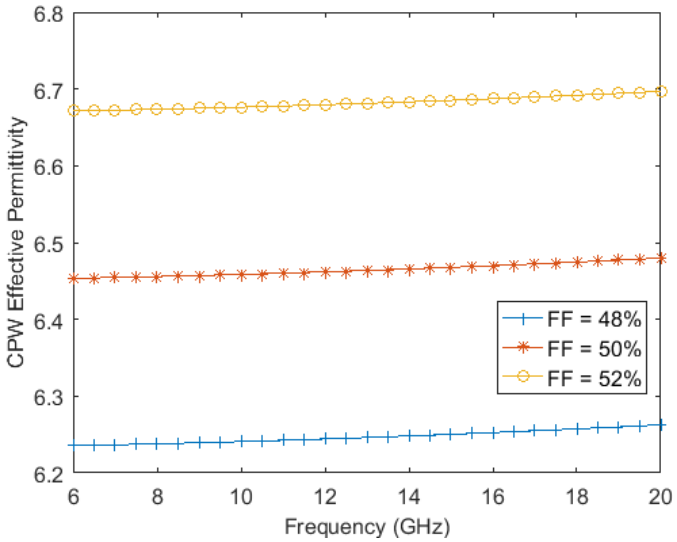


Figure 5-7 Frequency dependency of $\varepsilon_{eff}(f)$ according to (5-3) and change in $\varepsilon_{eff}(f)$ for different field distributions in the substrate.

Figure 5-7 also depicts the effect of FF. Higher concentration of fields in the material, hence higher FF, also causes an increase in $\varepsilon_{eff}(f)$. This indicates that FF and as a result quasi-static permittivity ε_q is higher than expected for the samples. Filling factor for all

the samples are calculated from extracted $\varepsilon_{eff}(f)$ using (5-7) and depicted in Figure 5-8. The filling factor also shows a decrease of ≤ 2% over the frequency range. It changes from 52.5% to 52% for the Si sample between 6 – 20 GHz. Addition of epi-layers increase the filling factor, with the 795 nm GaN sample showing FF = 58% at 6 GHz and 56% at 20 GHz.

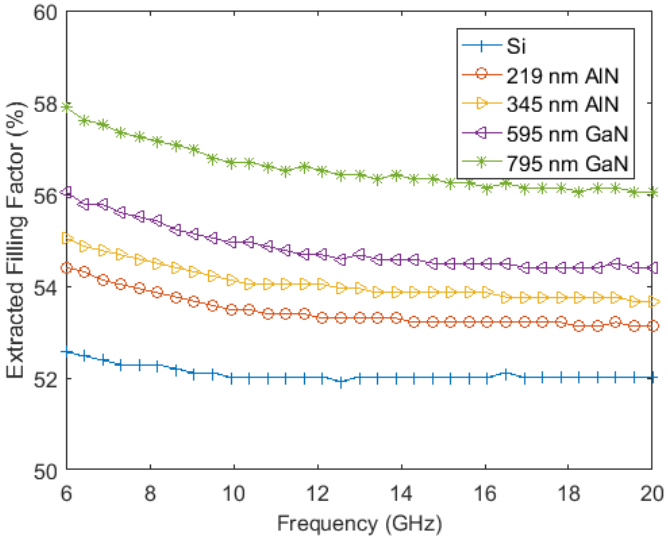


Figure 5-8 Filling factor from extracted $\varepsilon_{eff}(f)$ for all five samples.

An improved analytical expression for ε_q, taking into account the multilayer dielectrics and the finite dimensions of the ground planes, is given in [31]. Using the equations from [31], ε_q for Si is calculated to be 6.44 with FF = 49.91%Figure 5-8 Filling factor from extracted $\varepsilon_{eff}(f)$ for all five samples., lower than measurement results. For multi-layer substrate ε_q calculations, the equations produce a negative capacitance term due to AlN layer over Si having lower ε_r. Resulting ε_q values are too low and physically not meaningful: 4.99 (FF = 36.61%) for 219 nm AlN sample and 5.34 (FF = 39.82%). Using

the absolute value of this negative capacitance term results in a more reasonable trend but very high ε_q values ranging from 7.89 (FF = 63.22%) for 219 nm AlN sample and 8.24 (FF = 66.43%) for the 795 nm GaN sample.

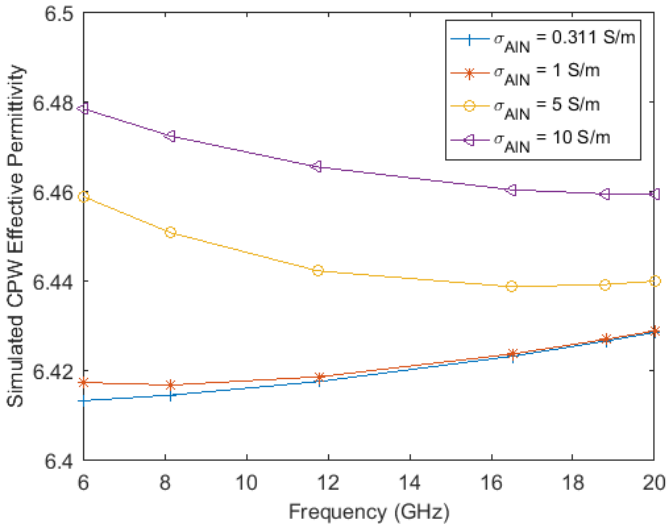


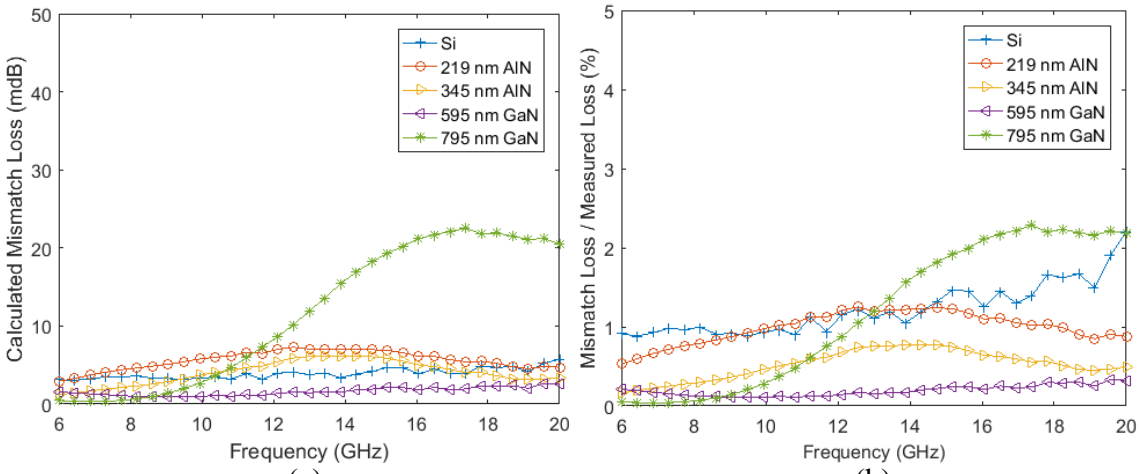
Figure 5-9 Variation of $\varepsilon_{eff}(f)$ with substrate conductivity from Sonnet simulations.

Note that none of the mentioned ε_q or $\varepsilon_{eff}(f)$ equations include the effect of dielectric conductivity on these parameters which quantify dispersion. Due to lack of analytic expressions including the effect of conductivity on $\varepsilon_{eff}(f)$, sample CPW geometry is simulated with Sonnet for a substrate with varying conductivity and the resulting $\varepsilon_{eff}(f)$ is shown in Figure 5-9. The substrate used in this simulation consists of a 219 nm AlN epi-layer on 500 µm Si. Conductivity of Si and dielectric loss tangent of both layers are kept constant while the AlN conductivity is swept. Results indicate not only an increase in $\varepsilon_{eff}(f)$ with increasing conductivity but also a change in its frequency dependency. For higher conductivity values the effective permittivity start decreasing with frequency rather than

increasing as indicated by (5-3). Accordingly, the high values of extracted $\varepsilon_{eff}(f)$ and their decrease with frequency, depicted in Figure 5-6, are attributed to high substrate conductivity which increases with addition of epi-layers.

5.1. Loss Mechanisms and Overall Dielectric Loss of GaN-on-Si Epilayers

In order to observe the effect of epi-layers on loss, radiation and metal losses are calculated and subtracted from the measured loss. Resulting dielectric loss is analyzed to extract dielectric parameters for different epi-layers.



(a) (b)

Figure 5-10 (a) Total calculated mismatch loss and (a) its percentage to overall measured loss for all five samples.

Note that as the characteristic impedance is not purely 50 Ω, mismatch loss and its contribution to overall loss need to be taken into account. The mismatch loss for all five samples is calculated using (4-19) from the measured input reflection coefficient and depicted in Figure 5-10. It is at most a little over 2% of the measured S_{21}, over the 6 – 20

GHz frequency range, and typically much smaller. Due to minimal contribution of mismatch loss, it is not included in the loss analysis.

Radiation loss, calculated using (4-21) and the extracted $\varepsilon_{eff}(f)$, is plotted in Figure 5-11 for all five samples. The radiation loss contribution to overall loss is comparable for all samples and ≤ 0.11% at 6 GHz. At 20 GHz, maximum radiation loss contribution of 4.8% is observed for the Si sample and < 3% for the other samples.

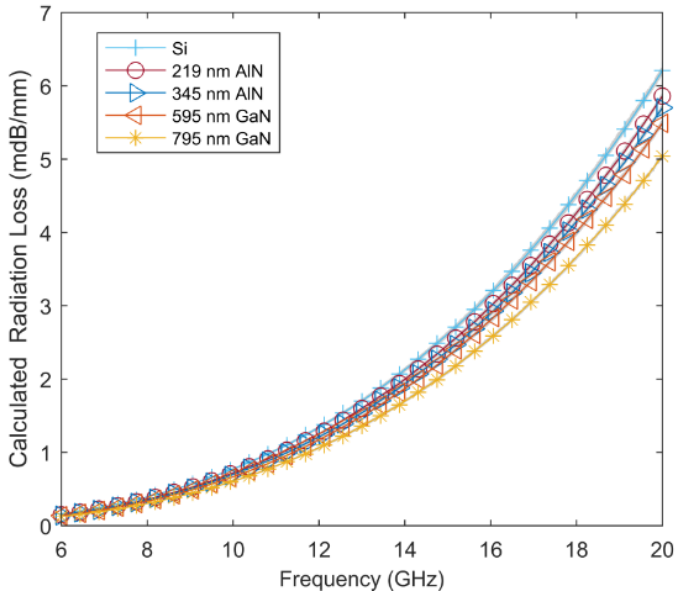


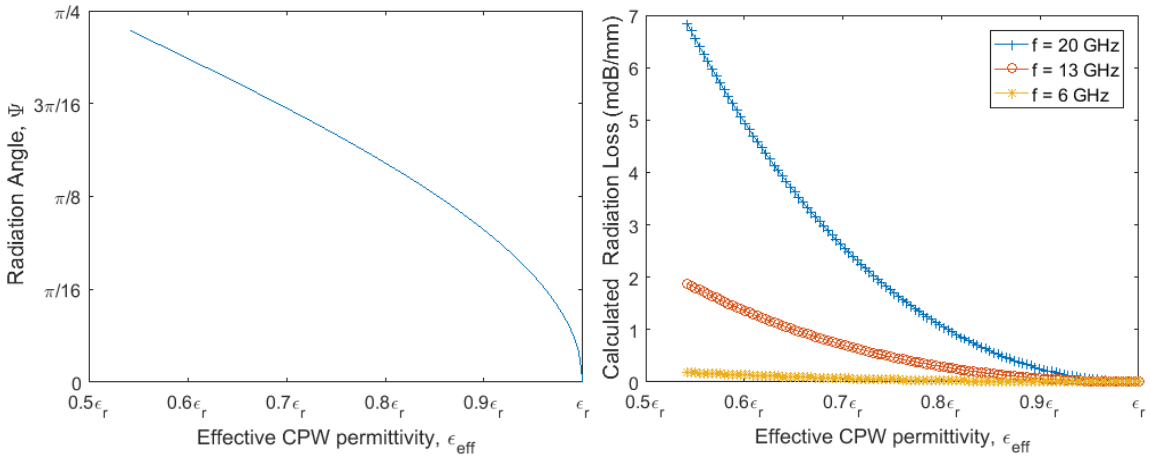
Figure 5-11 Mean and 95% confidence intervals for calculated radiation loss of CPWs from five samples.

Another important observation in Figure 5-11 is the decreasing radiation loss with epi-layers. This is due to increasing ε_{eff} that results in a smaller radiation angle. Radiation angle, Ψ, of the electromagnetic shock wave emitted into the substrate, is determined by the mismatch between the effective permittivity of the coplanar structure, ε_{eff}, and the permittivity of the dielectric substrate, ε_r:

$$\cos(\Psi) = \sqrt{\frac{\varepsilon_{eff}(f)}{\varepsilon_r}} \tag{5-8}$$

Change in radiation angle with increasing effective permittivity is depicted in Figure 5-12(a) for ε_r =11.9. As effective permittivity approaches ε_r, radiation angle decreases due to decreasing dielectric mismatch. Radiation loss is related to radiation angle and frequency as:

$$\alpha_{radiation} \propto \left(\frac{(1-\cos^2(\Psi))^2}{\cos(\Psi)}\right) f^3 \tag{5-9}$$



(a) (b)

Figure 5-12 Effect of CPW effective permittivity on (a) radiation angle and (b) radiation loss at 6, 13 and 20 GHz for the sample CPW geometry.

(5-9) shows that radiation loss decreases for decreasing radiation angle, hence, increasing ε_{eff}, as observed in Figure 5-11. Radiation loss is also a cubic function of frequency, resulting in the higher radiation loss variation between the samples at higher

frequencies. $\alpha_{radiation}$ is plotted as a function of ε_{eff} in Figure 5-12(b) for three different frequencies in order to highlight the changing effect of ε_{eff} with frequency.

The main loss that needs to be taken into account to make a true comparative analysis that verifies and quantifies the increase in loss with addition of epi-layers and their thickness on Hi-R Si is loss due to metallization. Before metal loss is calculated the conductivity of the e-beam deposited Al is extracted from DC measurements. It is measured to be between 3 to 3.25 × 10^7 S/m, lower than the ideal Al conductivity of ~3.7 × 10^7 S/m. Al conductivity of 3 × 10^7 S/m is used for the rest of the analysis.

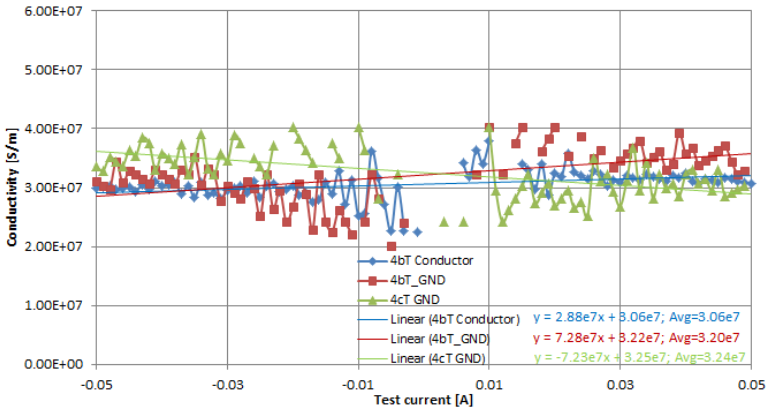
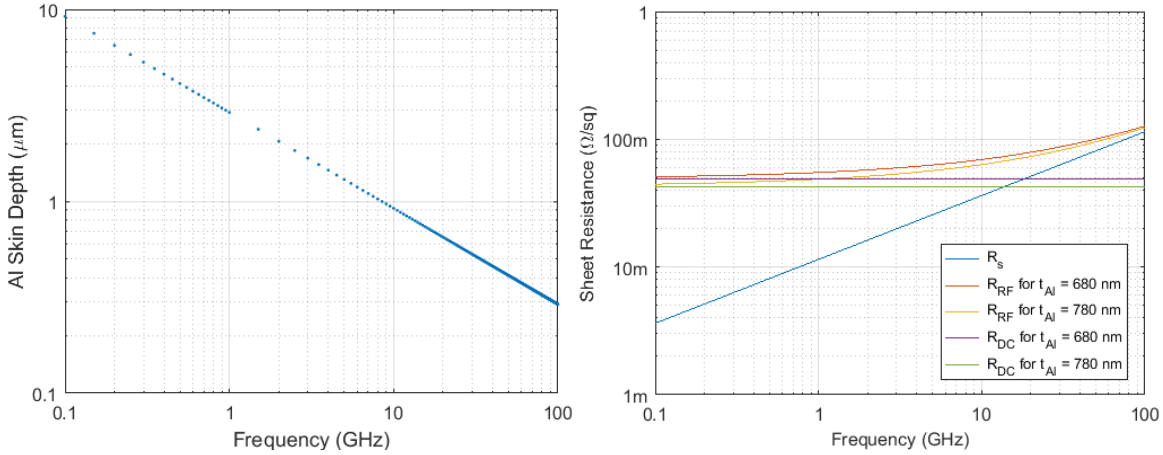


Figure 5-13 E-beam deposited Al conductivity from DC measurements.

The skin depth of the deposited Al is calculated using (4-32) for 0.1 – 100 GHz and plotted in Figure 5-14(a). For the 6 – 20 GHz frequency range, Al skin depth decreases from 1.2 μm to 650 nm. Note that the Al thicknesses for the samples are 680, 700 and 780 nm, less than the calculated skin depth for most of the measurement range. As a result, surface resistance given by (4-34) largely underestimates the actual resistance. R_{RF} given by (4-33) takes into account the metal thickness for a more accurate calculation. R_s as well

as R_{RF} and R_{DC} for Al thicknesses of 680 and 780 nm are plotted in Figure 5-14(b) for comparison. RF sheet resistance changes between 64 – 80 mΩ/□ and 58 – 73 mΩ/□ for 680 and 780 nm Al, respectively, for 6 – 20 GHz frequency range.



(a) (b)

Figure 5-14 (a) skin depth and (b) sheet resistance for e-beam deposited Al films.

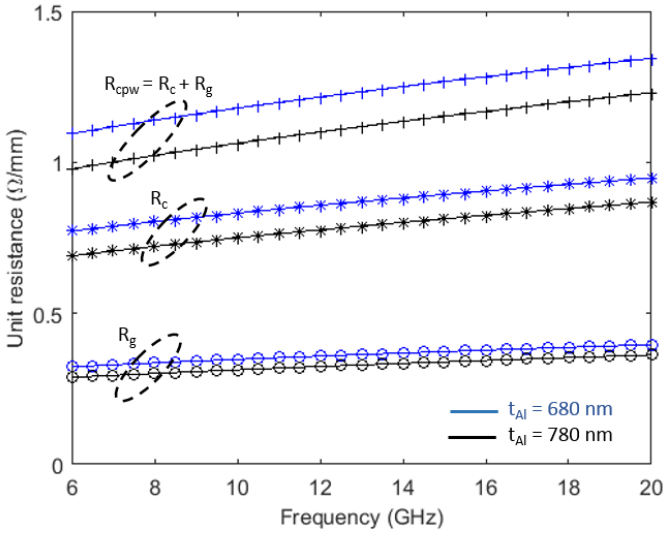


Figure 5-15 Conductor, ground plane and total CPW unit resistance for Al thickness of 680 and 780 nm.

The conductor and ground plane unit resistances, R_c and R_g, for the CPWs of different Al thickness are calculated using (4-29) and (4-30) with RF resistance. R_c and R_g, as well as total unit resistance of the CPW, R_{cpw}, are plotted in Figure 5-15 for 680 and 780 nm thick Al. An increase in resistance with frequency due to skin effect is observed for all curves. Ground plane resistance is ≤ 0.6 Ω/mm, less than half of conductor unit resistance, over the whole frequency range. Figure 5-15 shows that the decrease in Al thickness from 780 to 680 nm results in an increase of about 0.1 Ω/mm in the overall CPW resistance.

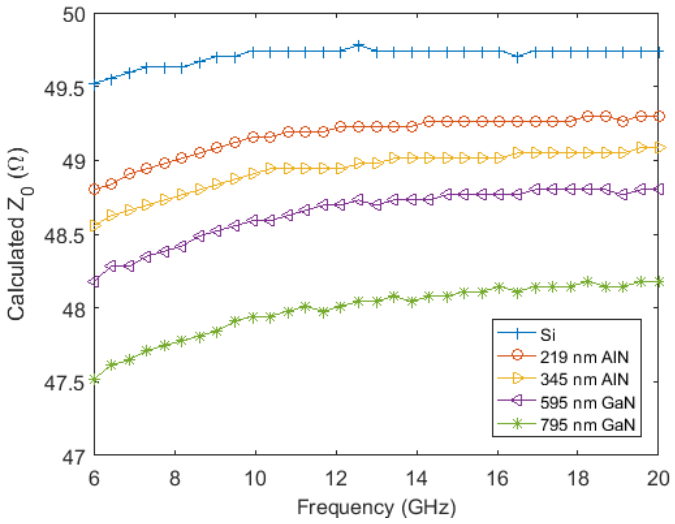


Figure 5-16 Z_0 for all five samples calculated with conformal mapping equations and extracted ε_{eff}.

CPW characteristic impedance Z_0, calculated using (4-28) and the extracted ε_{eff}, is plotted for all the samples in Figure 5-16. A decrease in characteristic impedance is observed with addition of epi-layers. Z_0 also shows an increase with frequency for all the samples, which is more pronounced with addition of epi-layers. Si sample CPW

impedance changes between 49.5 – 49.75 Ω. For the 795 nm GaN sample Z_0 decreases to 47.5 Ω at 6 GHz and with a more pronounced frequency dependence, it increases to 48.2 Ω at 20GHz.

Metal loss is calculated from R_{cpw} and Z_0, depicted in Figure 5-15 and Figure 5-16, respectively, using (4-23) and plotted in Figure 5-17. Metal loss is a function of square root of frequency as expected. It varies between 0.085 -0.1 dB/mm at 6 GHz and 0.107 – 0.122 dB/mm at 20 GHz for the samples. The variation in metal loss between the samples is mainly related to the difference in their metal thickness. 800 GaN sample with the thinnest Al film of 680 nm has the highest metal loss whereas the Si, 400 nm AlN and 600 nm GaN samples with thickest Al film of 780 nm have the lowest loss. The difference in loss is slightly over 10 mdB/mm for samples with 680 and 780 nm Al. The variation between the metal loss of Si, 400 nm AlN and 600 nm GaN samples is due to the variation of their extracted ε_{eff}, depicted in Figure 5-6.

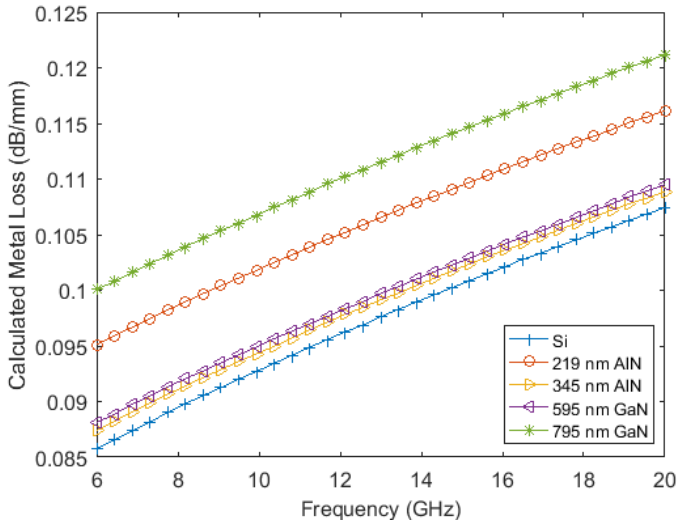


Figure 5-17 Calculated metal loss for all five samples.

Finally, the radiation and metal losses are subtracted from the measured loss to obtain the dielectric loss. Mean and 95% confidence interval of the dielectric loss from the samples are depicted in Figure 5-18. Figure 5-18 indicates a significant increase in dielectric loss as more epi-layers are stacked on to the Hi-R Si substrate and as the epi-layer thickness increases. Dielectric loss extracted from the Hi-R Si sample is less than 0.02 dB/mm within the 6 - 20 GHz frequency range. Dielectric loss at 6 GHz increases to 0.08 dB/mm for the 219 nm AlN sample and 0.11 dB/mm for the 345 nm AlN sample. Further increase in dielectric loss is observed with GaN-on-Si samples with extracted dielectric loss of 0.17 dB/mm for the 595 nm GaN sample and 0.20 dB/mm for the 795 nm GaN sample at 6 GHz.

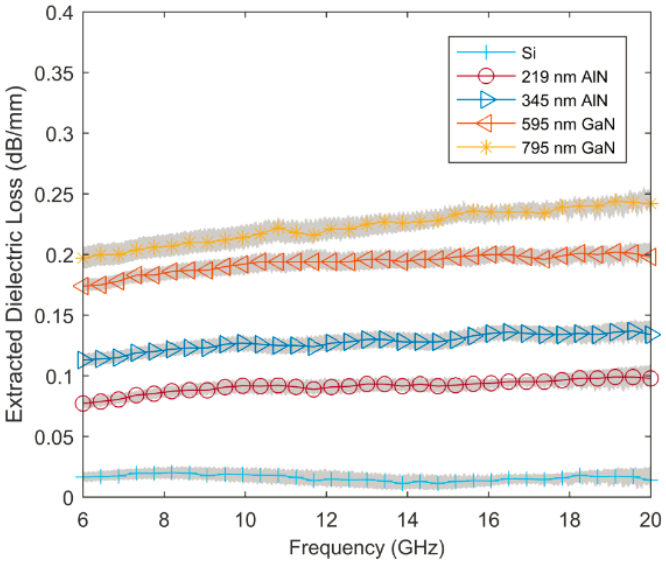


Figure 5-18 Mean and 95% confidence interval of extracted dielectric loss for the samples.

An additional observation from Figure 5-18 is the increase in the dielectric loss slope with added film thickness and epi-layers. Si sample exhibits almost frequency independent dielectric loss behavior whereas both AlN samples and the 595 nm GaN sample exhibit similar frequency dependence. Higher frequency dependence is observed for the 795 nm GaN sample.

Dielectric loss, given by (4-40) is a function of effective loss tangent and frequency. Effective loss tangent has two components, one constant and one with 1/f frequency dependence, resulting in both the constant increase and the slope change of dielectric loss observed in Figure 5-18. Change in $tan\delta_{eff}$ with added nitride layers and the underlying reasons are described in detail in the next section.

5.2. Effective Loss Tangent, Dielectric Loss Tangent and Conductivity due to GaN-on-Si Epi-layers

Effective loss tangent of the samples is calculated from the extracted mean dielectric loss and ε_{eff} using (4-40) and depicted in Figure 5-19. The figure depicts not only an increase in the value of effective loss tangent but also an increase in its frequency slope with addition of epi-layers. (4-38) shows that effective loss tangent is a function of both dielectric loss tangent and conductivity. Dielectric loss tangent causes a frequency-independent increase in the effective loss tangent whereas conductivity adds a term that is inversely proportional to frequency. Therefore, the effective loss tangent variation observed in Figure 5-19 suggests an increase both in dielectric loss tangent and conductivity with addition of epi-layers on Hi-R Si substrate. Increasing overall

conductivity with epi-layers is clearly observed from the increasing frequency dependence of the effective loss tangent except for the 795 nm GaN sample. Shift between effective loss tangents of 595 nm and 795 nm GaN samples indicates a more pronounced increase in polarization losses, given by dielectric loss tangent, rather than conductive losses at the top GaN layer.

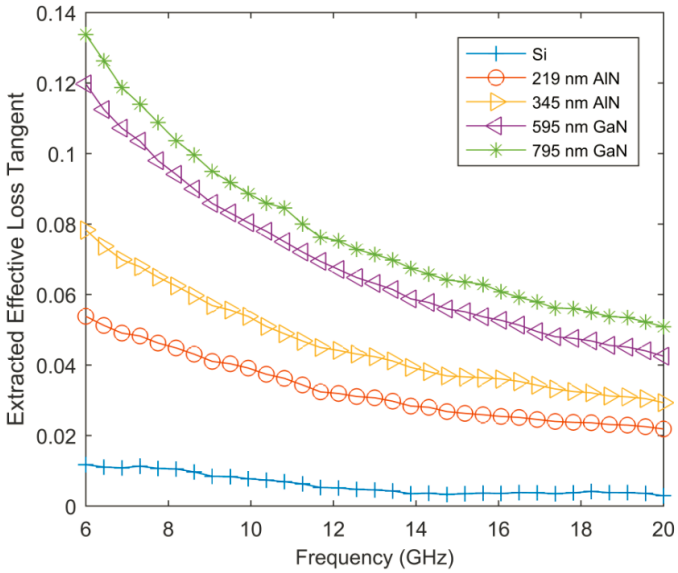
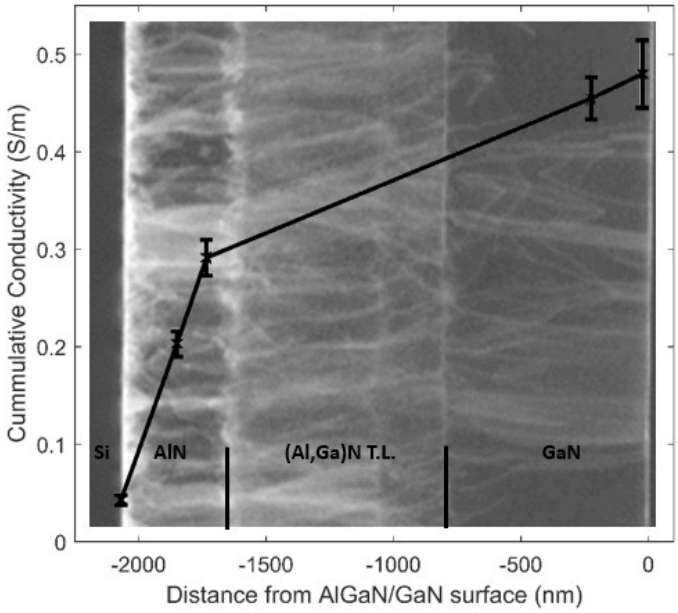


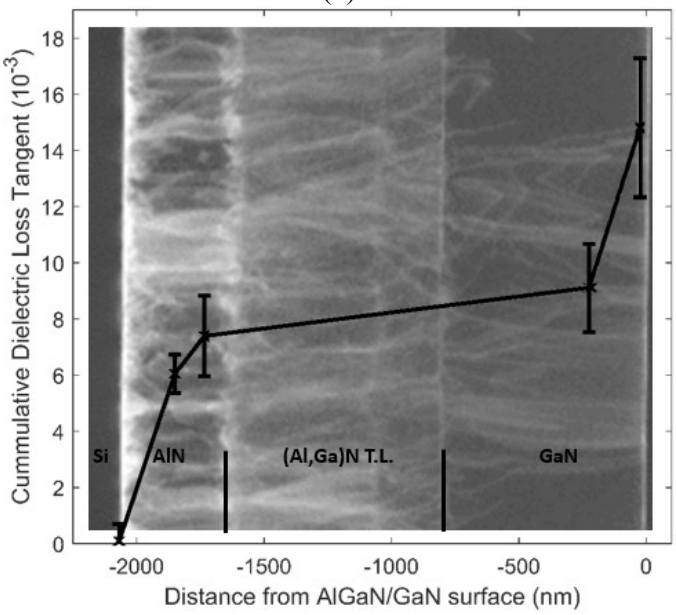
Figure 5-19 Extracted $tan\delta_{eff}$ from five samples

Mean and 95% confidence interval of overall conductivity and dielectric loss tangent are calculated from the data for each sample and plotted in Figure 5-20(a) and (b), respectively. For visual reference, the TEM cross-section of the complete epitaxial nitride structure is superimposed so that each data point represents the total cumulative loss parameters at that point. For these plots, first the effective loss tangent is calculated from

the extracted dielectric loss using (4-40). Then linear regression using (4-41) is applied on the effective loss tangent values to extract σ and $tan\delta_d$.



(a)



(b)

Figure 5-20 Increase in overall (a) conductivity and (b) dielectric tanδ from Si interface to the GaN top surface.

Extracted conductivity for Si is 0.04 ± 0.01 S/m, approximately four times more than the specified bulk conductivity for the Hi-R substrate. This result is in accordance with previously published data showing higher losses for transmission lines on unpassivated Si [57, 58]. This increase in losses is attributed to metal contamination of Si surface in [57], citing studies that show Al contamination to convert deep submicron silicon-on-insulator (SOI) layers to p-type Si. Native oxide formation on Hi-R Si is also considered as a possible cause for the increase in loss. [57] claims that the native oxide is expected to have a small positive potential of 80 mV, resulting in a depletion region at the p-type Hi-R surface that should not contribute to RF losses. Note that Si sample is only used as a point of reference in this study to demonstrate the degree of increase in dielectric loss parameters with GaN-on-Si epi-layers. Therefore, data from Si sample is not investigated further.

Figure 5-20(a) shows that the overall substrate conductivity increases to 0.20 ± 0.01 S/m for 219 nm AlN on Si and to 0.29 ± 0.02 S/m for 345 nm AlN on Si. Further conductivity increase is observed for the samples including the (*Al,Ga*)N transition layer and the top GaN layer: 0.45 ± 0.02 S/m for 595 nm GaN and 0.48 ± 0.03 S/m for 795 nm GaN. Results suggest that AlN layer and its thickness has higher impact on the overall GaN-on-Si conductivity compared to the top GaN layer.

One broadband characterization of CPWs on GaN-on-Si also reports higher microwave losses than expected for the multilayer substrate [23]. This extra loss is attributed to a parasitic conductive layer inside silicon at the AlN/Si interface [50]. A parasitic layer alone would explain the loss increase with addition of AlN layer, however, it cannot account for a further increase in loss with the AlN thickness increase nor with addition of

more epi-layers on AlN. AlN-on-Si substrate losses are analyzed in more detail in the next section to determine if a parasitic conductive layer exists at the interface and if so, its contribution to overall loss.

The sharp increase in conductivity with addition of more or thicker epi-layers is mainly attributed to the threading dislocation density in this study. The contribution of defects to conductivity is suggested by the increase in conductivity with increasing AlN layer thickness, hence, increasing number of dislocations in the overall volume. Further but much smaller increase in overall conductivity is observed with the addition of (*Al,Ga)*N T.L. and GaN buffer layers which have less TD densities as observed in Figure 5-20.

There is an observed dislocation/leakage current correlation established in the literature. Even though edge dislocations are accepted to be non-conductive, studies have shown screw dislocations to be electrically conductive and acting as the main leakage path [59, 60]. Pure edge and mixed dislocations are typically the predominant threading dislocations in MOCVD grown GaN on sapphire [61]. However, there are conflicting reports of screw dislocation densities for Si substrates. A study of dislocation densities in GaN on AlN-Si (111) grown via MOCVD in [62] indicates the screw dislocation density dominating. On the other hand, GaN with a screw dislocation density of less than 10^7 cm^{-2} and edge and mixed dislocation density of 1 to 5×10^9 cm^{-2} is reported in [63] with a similar process as the one employed for the template in this study. The observed epi-layer conductivities and dislocation densities suggest that the dislocations play a role as the source of increased epi-layer conductivity. However, further investigation is needed to confirm the type and character of dislocations primarily responsible for these results.

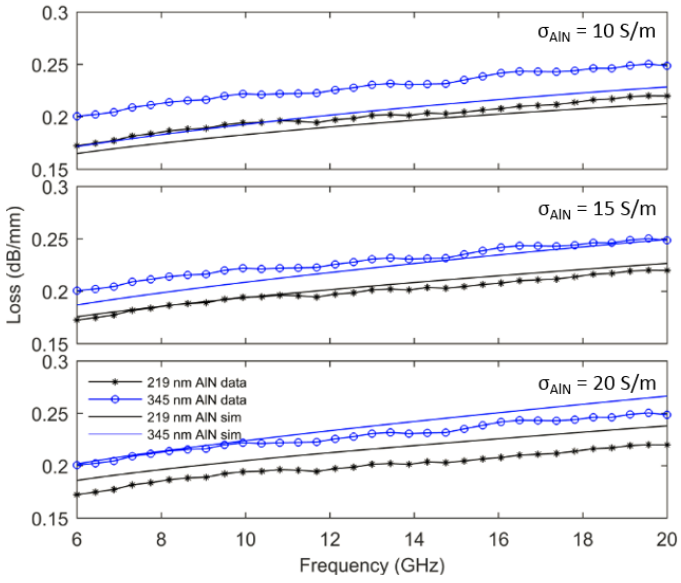
Figure 5-20 (b) depicts a slightly different trend for the change in dielectric loss tangent. The addition of AlN layer on Si sharply increases $tan\delta_d$ from less than 10^{-3} to $6.0 \pm 0.7 \times 10^{-3}$ for 219 nm AlN and to $7.4 \pm 1.4 \times 10^{-3}$ for 345 nm AlN. Adding the transition layer and 595 nm GaN causes only a small increase in $tan\delta_d$ to $9.1 \pm 1.6 \times 10^{-3}$. However, a much higher $tan\delta_d$ of $14.8 \pm 2.5 \times 10^{-3}$ is observed for thicker GaN layer of 795 nm. The culprit for the dielectric loss tangent increase with addition of nitride layers is suspected to be dipolar Debye losses given the frequency of interest [64, 65]. Dipolar loss is a mechanical loss arising from the re-orientation or finite distortion of dipoles due to strain resulting from an applied electric field. The resulting loss is not only related to the dipole moments but is also strongly affected by energy barriers between different dipole positions and related relaxation times. The discrepancy between observed dielectric behavior and theoretical Debye loss has led to various interpretations of relaxation time such as distribution of relaxation times [66] or "universal relaxation/power law" with fractional exponent [65]. Overall, the external electric field is expected to deform the crystal and losses are expected to accompany dipole relaxation, especially in the gigahertz range.

Dipolar losses are very weak in Si due to neutral atoms and strong, essentially pure, covalent bonds, as reflected in its low dielectric loss tangent. The net polarization and the resulting dipole moment within the AlN explains the large jump in dielectric loss tangent with addition of the AlN layer. Given the overlapping confidence intervals, it is not possible to determine the amount of increase, if any, in dielectric loss tangent with increasing AlN layer thickness. The dielectric loss tangent increases slightly with the addition of (*Al,Ga*)N transition layer and 595 nm GaN layer, which could be attributed to

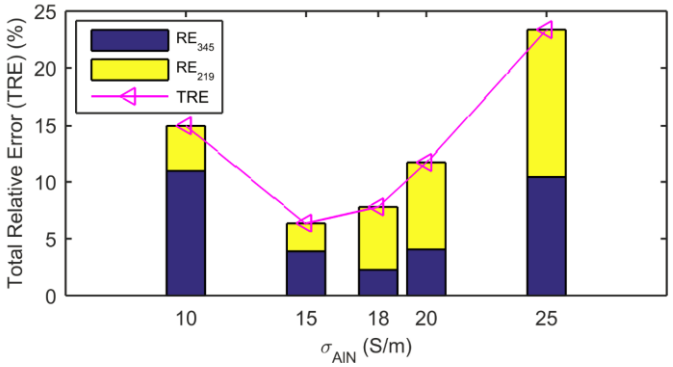
an increase in overall dipole moment due to the addition of nitride layers with non-zero net polarization. A curious observation is the large jump in the dielectric loss tangent for 795 nm GaN sample. This is due to changes in strain of this layer near the top, as expected for a relaxation layer. The AlGaN/GaN template is designed to have a relaxed GaN buffer in order to achieve crack-free thin films and to optimize the interface charge at the AlGaN barrier/ GaN 2DEG channel layer interface. AlN and (*Al,Ga*)N transition layers on Si are optimized to reduce the tensile strain in the layers due to their large lattice mismatch with Si [67]. GaN deposited on such optimized nitride layers initially show compressive strain, then relaxation, and finally tensile strain with increasing GaN layer thickness [68]. The transition thicknesses depend on the growth conditions and also the thickness of the underlying epi-layers. The AlGaN/GaN template used in this study originally has 800 nm GaN buffer that is relaxed near the surface. The 795 nm GaN sample is expected to have nearly the same strain relaxation. Such a relaxed GaN layer for the Ga-face structure has little piezoelectric polarization, only spontaneous polarization in $[000\bar{1}]$ direction. In comparison, the 595 nm GaN sample is relatively more compressively strained and the resulting piezoelectric polarization is antiparallel to the spontaneous polarization. Given spontaneous and piezoelectric polarizations that are opposite in sign, net polarization would be lower than that of relaxed GaN. Higher net polarization, and hence dipole moment, of the 795 nm GaN sample compared to 595 nm GaN could be the reason for the observed increase in dielectric loss tangent. Thus the difference between dipole relaxation processes for the relaxed and the compressively strained GaN would also result in the observed variation.

5.3. Loss Mechanisms of AlN-on-Si

An increase in loss for GaN-on-Si structures with an identical AlN layer was previously observed and attributed to a p-type conductive layer at the AlN-Si interface [23]. This layer is formed by the diffusion of Al and Ga atoms into the Si substrate during the MOCVD growth of the AlN layer. Based on the measured carrier distribution reported in [50], the conductivity of this parasitic layer was obtained through fitting as 8 S/m [23]. However, while a conductive layer at the AlN-Si interface can easily account for the higher loss from AlN-on-Si compared to Si, it cannot account for the observed increase in loss with increasing AlN layer thickness nor with the addition of (*Al,Ga*)N and GaN epi-layers. Such an increase can only be attributed to the dielectric loss of the AlN layer itself as it would scale with the layer thickness. The effective loss tangent of a semiconductor material, which determines its dielectric losses, is a function of dielectric loss tangent and conductivity, as explained in detail previously. Conductivity represents the losses related to conduction or ohmic losses. High threading dislocation densities, especially of conducting dislocations, are expected to affect at least the conductive losses of the 'insulating / semi-insulating' layers. Therefore, it is concluded that a combined effect of bulk dielectric loss of the AlN and a p-type lossy layer in the Si contributes to the observed loss. The relative impact of each loss mechanism is extracted through simulations as detailed in Section 4.4.



(a)



(b)

Figure 5-21 Measured vs. simulated loss for 219 and 345 nm AlN-on-Si with σ_{AlN} of 10, 15, and 20 S/m for $\sigma_{AlN\text{-}Si}$ = 1 S/m (b) relative percentage error for σ_{AlN} = [10, 15, 18, 20, 25] S/m for $\sigma_{AlN\text{-}Si}$ = 1 S/m.

To highlight the methodology, a comparison of the experimental and simulated losses, assuming a single AlN-Si interface conductivity ($\sigma_{AlN\text{-}Si}$) with 3 different AlN bulk conductivities (σ_{AlN}), is shown in Figure 5-21(a). The resulting relative error calculated using (4-42) is seen in Figure 5-21(b). With $\sigma_{AlN\text{-}Si}$ and σ_{AlN} set at 1 and 10 S/m, respectively, Figure 5-21(a), top, shows that the 345 nm sample's simulated and measured

losses are disparate (RE_{345} = 11.0%), while the simulated and measured loss of the 219 nm sample does match somewhat (RE_{219} = 4.0%). As σ_{AlN} is increased to 15 S/m (Figure 5-21 (a), middle), both samples demonstrate a more matched correlation between simulated and measured data (RE_{219} = 2.5%, RE_{345} = 3.9%). However, increasing σ_{AlN} to 20 S/m indicates that the simulated and measured loss of the 219 nm sample start to diverge (RE_{219} = 7.6%, RE_{345} = 4.1%). Using these relative errors as the metric, the total relative error ($TRE=RE_{219}+RE_{345}$) for a fixed $\sigma_{AlN\text{-}Si}$ = 1 S/m is plotted in Figure 5-21(b). It is concluded that, if the $\sigma_{AlN\text{-}Si}$ were indeed 1 S/m, then σ_{AlN} would be at or near 15 S/m as this is the point at which the TRE is minimal.

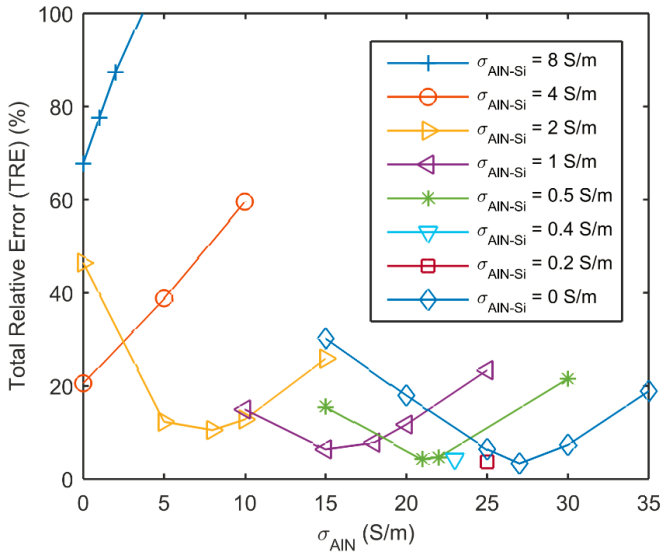


Figure 5-22 Total relative percentage error of 219 and 345 nm AlN-on-Si for various AlN and interface layer conductivities. The minimum TRE increases for increasing interface conductivity values.

This methodology is applied to the same experimental data while varying the simulations of σ_{AlN} from 0-35 S/m for the individual $\sigma_{AlN\text{-}Si}$ values of [0, 0.5, 1, 2, 4, 8]

S/m. Figure 5-22 shows the sum of relative errors of both samples for a given conductivity combination. It can be seen that the lowest minima in error occurs when the p-type conductivity is less than 1 S/m. Additional $\sigma_{AlN\text{-}Si}$ single data points are added between 0 and 0.5 S/m to reinforce the conclusion.

The results obtained from measurement and simulation indicate that the increase in loss for GaN-on-Si cannot only be attributed to a highly conductive layer at the AlN-Si interface. For less than ~ 5% total error between measurement and simulation data, the AlN conductivity is extracted to be at least 15 S/m and AlN-Si interface layer conductivity at most 1 S/m and probably lower. Thus it is concluded that AlN conductivity is the main contributor for the measured AlN-on-Si (111) loss. Dislocation density is suspected to be the cause for the high AlN conductivity as explained in the previous section. Further investigation to confirm the type and character of the dislocations is needed to narrow down the possible values of AlN and interface conductivities presented in Figure 5-22.

As a final note, it is important to understand that plasma damage from the planarization could impact defect states at the AlN surface that might lead to surface conduction between the CPW lines. However, this is eliminated as a significant contributor because loss does not track with plasma exposure. ICP-RIE duration affects the two dimensional electron gas properties in AlGaN/GaN HFET structure; however, this is in a recess isolation etch [69]. Etch duration has minimal impact on simple nitride surfaces [70]. Even if some surface conduction were to contribute to RF loss, subtracting this loss would not void the conclusions on AlN vs. AlN-Si interface conductivities and their relative

contributions to overall RF loss. Thus, the data does not support the proposition that plasma damage is of consequence in this analysis.

6. 2DEG TRANSMISSION CHARACTERIZATION

6.1. Preliminary Results from the First Design Cycle

6.1.1. 2DEG DC Measurements

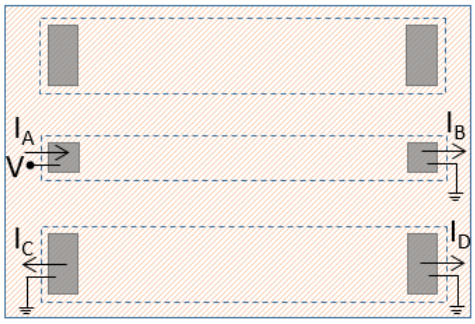


Figure 6-1 2DEG IV measurement setup.

DC measurements were taken from the 2DEG CPWs in order to verify that the contacts are ohmic and also to observe any leakage between the conductors of the CPW. Semiconductor parameter analyzer with four SMUs was used in the IV measurements. Test setup depicted in Figure 6-1 consists of voltage applied to one terminal of the center 2DEG conductor, while the other terminal of the same conductor and the both terminals of the adjacent one are grounded. All four terminal currents are measured to check IV linearity and leakage currents. IV curves from four different CPWs, with two different W and S combinations, on two different samples are depicted in Figure 6-2 in order to observe conduction and leakage variation with 2DEG CPW geometry and also the variation due to fabrication and material. Plots are in logarithmic scale to better demonstrate the linearity, which indicate that the 2DEG contacts are ohmic. The leakage current is approximately three orders of magnitude lower.

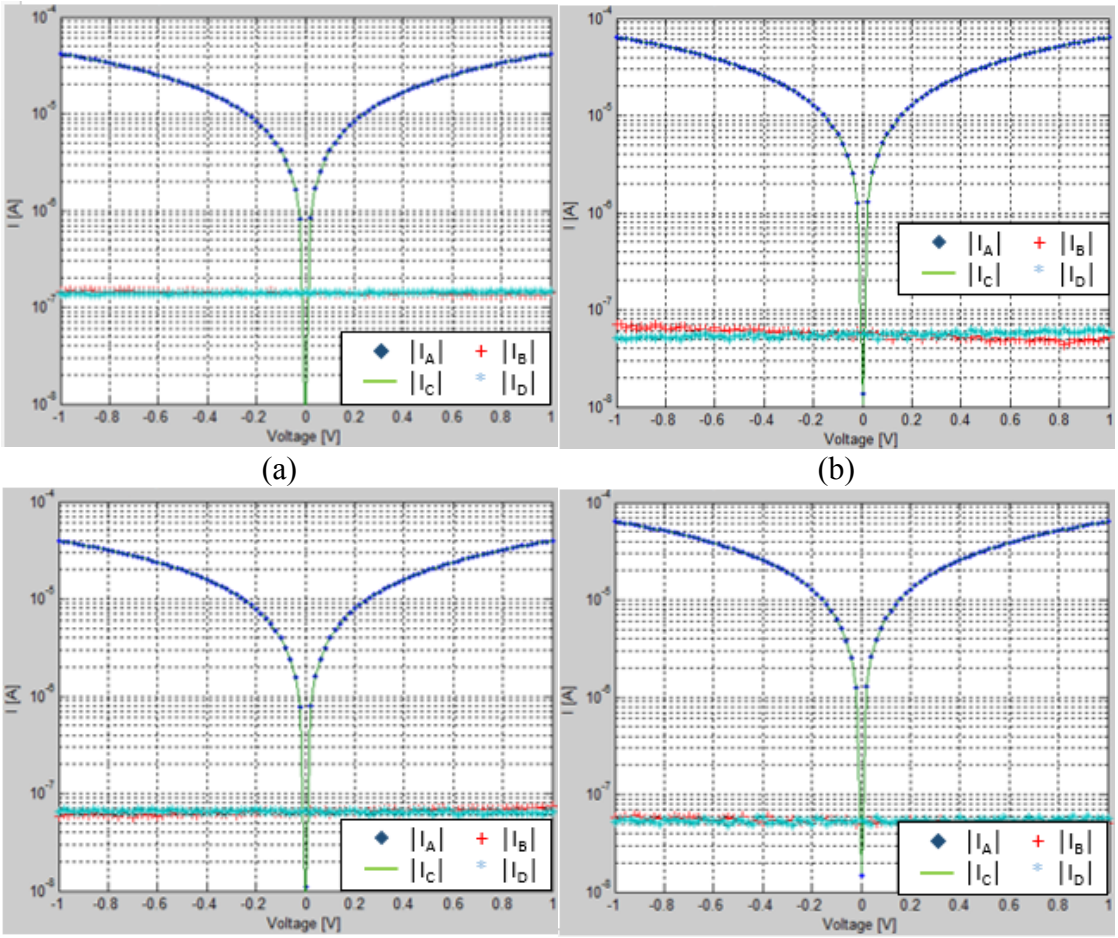


Figure 6-2 2DEG CPW DC conduction and leakage current measurements from four 2DEG CPWs: W = 74.5μm & S = 28 μm from (a) sample 1 and (c) sample 2; W=112 μm & S = 53 μm from (b) sample 1 and (d) sample 2

DC conductivity of the 2DEG is also calculated from these IV measurements. First DC resistance is extracted from the IV measurements. Resistivity, ρ, is a function of electron mobility, μ, and concentration, n, and is related to measured resistance through sheet resistance, R_{sh}, as:

$$\boldsymbol{R_{sh} = \frac{\rho}{t} = \frac{1}{q \cdot \mu \cdot n \cdot t} = R\frac{W}{L}} \qquad (6\text{-}10)$$

2DEG density is derived from (6-10) as:

$$n \cdot t = \frac{L}{q \cdot \mu \cdot R \cdot W} \quad (\mathrm{cm^{-2}}) \tag{6-11}$$

2DEG density calculated from the DC measurement data using (6-11) for electron mobility of 1360 $cm^2/(V \cdot s)$ is depicted in Figure 6-3. Ohmic contact resistance of 0.45 Ω·mm is subtracted from the measured resistance prior to density calculations. The variation in 2DEG density is attributed to AlGaN/GaN material variation, specified by the manufacturer, as well as variations due to fabrication. For a 2DEG density of 10^{13} cm^{-2} the expected 2DEG thickness is approximately 2 nm [25]. Calculated 2DEG conductivity, through (6-10), is between 0.9 – 0.96 × 10^6 S/m. For reference, Au conductivity is ~45.4 x 10^6 S/m, about 50 times higher.

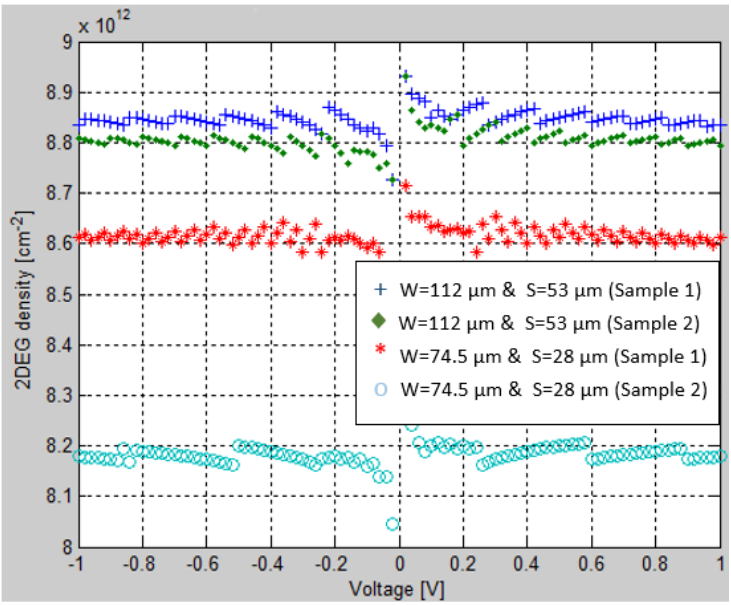


Figure 6-3 2DEG density extracted from four 2DEG CPWs on two different samples

6.1.2. 2DEG RF Measurements with 2DEG CPWs

RF measurement results with the 2DEG CPWs fabricated in the first design cycle indicated highly resistive transmission lines with capacitive reactance as depicted in Figure 6-4 smith chart reflection data. Given the 2DEG sheet resistance, the high impedance of the lines are as expected. Using TRL calibration, which sets the characteristic impedance to that of Line standard, and then impedance transformation on the measured s-parameters, accurate measurements can be obtained despite the high impedance mismatch with the network analyzer test ports.

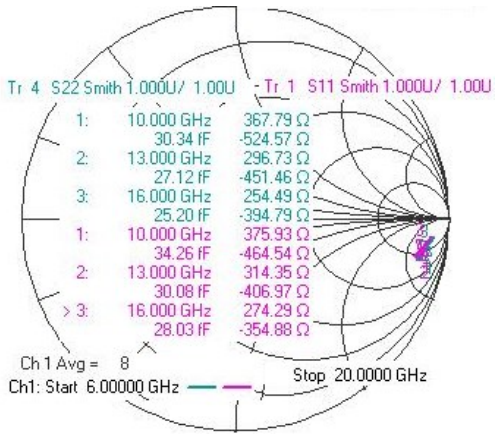


Figure 6-4 Reflection coefficients of a 2DEG CPW after SOLT calibration

Prior to TRL calibration, the delay on each 2DEG transmission line is measured in order to accurately set the TRL Line standard delay in the network analyzer calibration software. Despite several iterations with adjusted Line delay, TRL calibration did not produce consistent results. An example of the TRL calibration results with 2DEG CPWs is depicted in Figure 6-5.

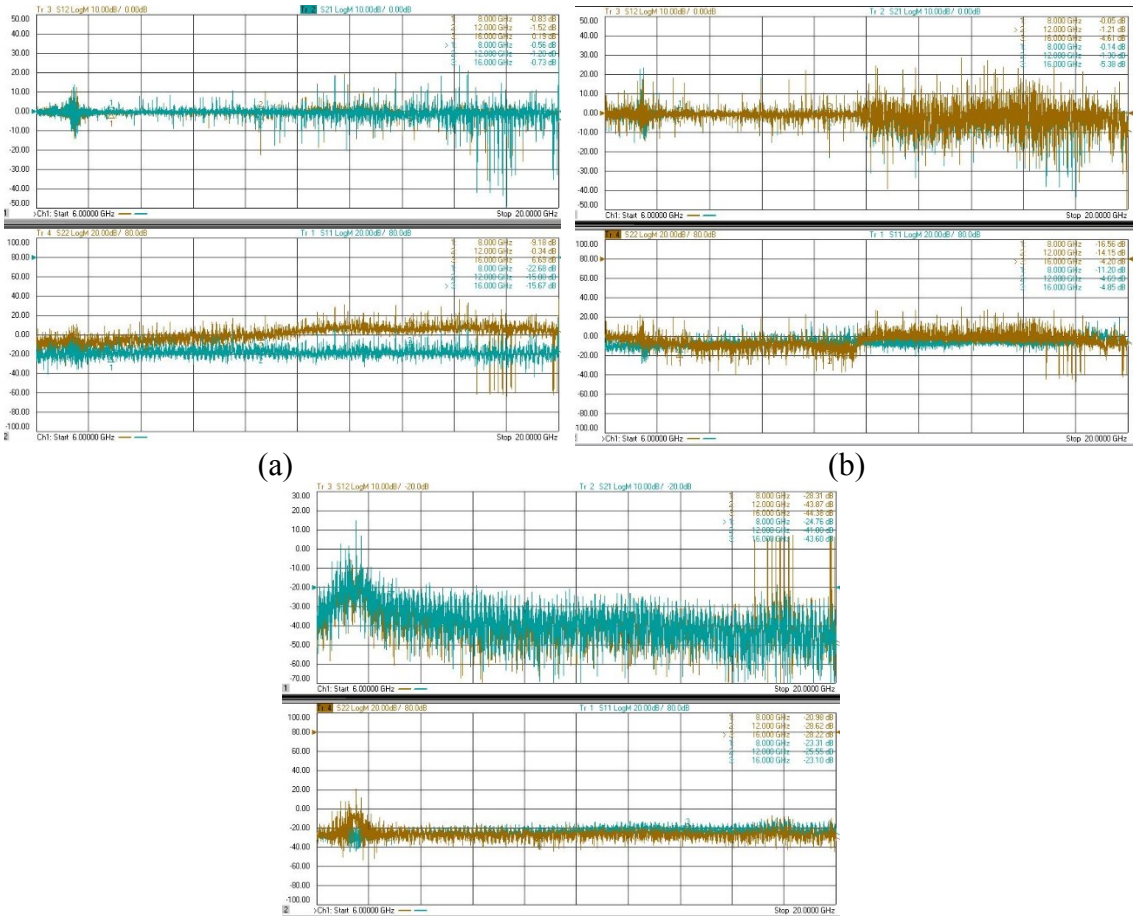
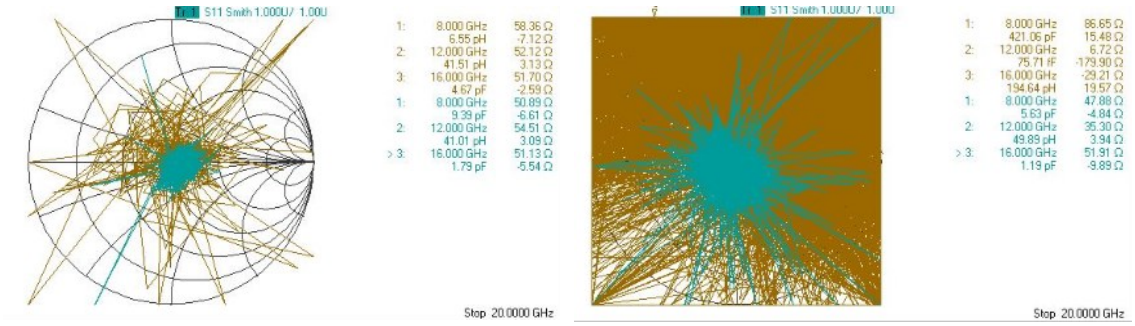


Figure 6-5 2DEG TRL Calibration difficulty illustrated with measurements taken after a TRL calibration: s-parameters from (a) the Thru standard (b) the Thru standard after re-probing and (c) Line standard.

Figure 6-5 (a) and (b) show the s-parameters of the Thru standard measured at the end of the TRL calibration. The transmission seem to be around 0 dB – and 15% smoothing applied on the data confirm this observation – as would be expected from a Thru standard that sets the reference planes to its midpoint but the results are too noisy to generate a meaningful analysis. Re-probing the Thru line changes the measured s-parameters, especially the S11 and S22, as depicted in Figure 6-5 (b). Figure 6-5 (c) shows the response

of Line standard used in the calibration. There is loss of more than 20dB for the ~ 2 mm of 2DEG between the TRL reference planes and it shows increase with frequency. S11 and S22 for the Line standard are less than -20dB, indicating a relatively good match. This is an expected result as the Line standard sets the calibration reference impedance. S11/S22 for Line and Thru standards are plotted in Smith Chart in Figure 6-6 (a) and (b), respectively. The results indicate the TRL calibration did set the reference impedance to the Line impedance but the variation in the S11/S22 parameters are too large for any analysis. Also there is a clear impedance deviation in one of the Thru standard terminals.



(a) (b)

Figure 6-6 Reflection coefficients on Smith chart for (a) Line and (b) Thru standards after 2DEG TRL Calibration.

The TRL measurement results presented so far suggest that the problem with the TRL calibration is the non-idealities in the fabricated test structures and also probing variations on Al. TRL calibration algorithm assumes symmetry for the main transmission parameters and is only immune to random, uncorrelated errors. 2DEG fabrication, especially the ohmic contacts, has high tolerances. Another important issue is repeatability with Al

probing. Al oxides readily and it is difficult to have consistent probing. TRL algorithm assumes identical - except for length - Thru, Reflect and Line standards. Any variation in these parameters during the calibration will obstruct meaningful calibration results. Table 6-1 lists input and output impedance readings from Smith Chart for a 2DEG CPW after SOLT calibration. Data from CPWs of same geometry but four different lengths, used in TRL calibration as standards, are included. The difference between input and output impedances of a 2DEG CPW, and the impedance variation between the lines of same geometry. These results explain the random errors observed in TRL calibration. The variation is attributed to fabrication tolerances and probing repeatability issues as explained previously.

Table 6-1 Input and output impedances from reflection coefficients showing the asymmetry of 2DEG s-parameters and variation between different length, same geometry CPWs.

	Thru (L=2.2mm)		**Line2 (L=3.5mm)**		**Line1 (L=2.85mm)**		**Line 3 (L=4.15mm)**	
Freq	**S22**	**S11**	**S22**	**S11**	**S22**	**S11**	**S22**	**S11**
8GHz	466.85Ω 33.4fF	514.03Ω 34.0fF	423.7Ω 40.7fF	442.1Ω 38.2fF	427.6Ω 41.6fF	403.7Ω 40.46fF	433.0Ω 39.9fF	407.5Ω 40.47fF
12GHz	337.4Ω 27.5fF	390.26 Ω 27.4fF	319.8Ω 33.1fF	334.2Ω 31.5fF	329.4Ω 33.79fF	303.7Ω 33.50fF	331.1Ω 32.26fF	306.7Ω 33.28fF
16GHz	266.8 Ω 24.4fF	317.3 Ω 23.8fF	261.0Ω 28.9fF	272.7Ω 27.5fF	272.2Ω 29.32fF	248.7Ω 29.45fF	270.9Ω 27.9fF	249.5Ω 29.2fF

Due to TRL issues, measurements are taken with SOLT calibration. It is difficult to determine the loss characteristics of the 2DEG CPW given the large reflections that will result from the impedance mismatch with the 50 Ω test setup. An example of the 2DEG

CPW measurement after SOLT calibration is depicted in Figure 6-7. It was not possible to analyze the results from these measurements but two general observations were the decrease in loss and impedance with increasing frequency. De-embedding structures were included in the next design cycle instead of TRL structures.

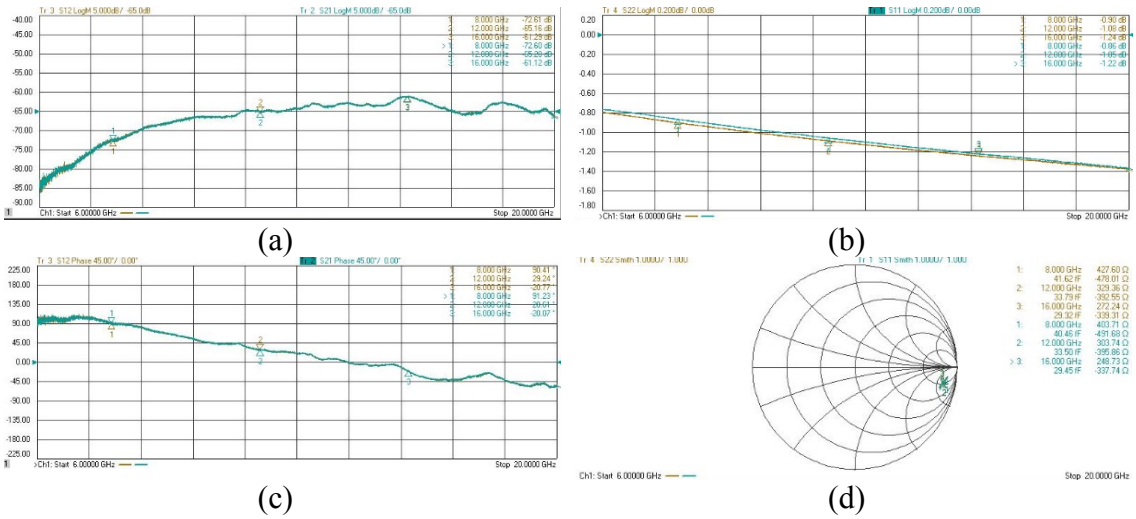


Figure 6-7 Example 2DEG CPW measurements after SOLT calibration: (a) S12/S21 (b) S11/S22 (c) S12/S21 phase and (d) S11/S22 on Smith

6.2. Results From Second Design Cycle

6.2.1. 2DEG Ohmic Contact Characterization

TLM data from a wide contact set and its linear fit are plotted in Figure 6-8. Sheet resistance of the contacted material as well as the contact resistance and the transfer length are extracted from the slope, y-intercept and x-intercept, respectively, as described in Section 3.2.2.

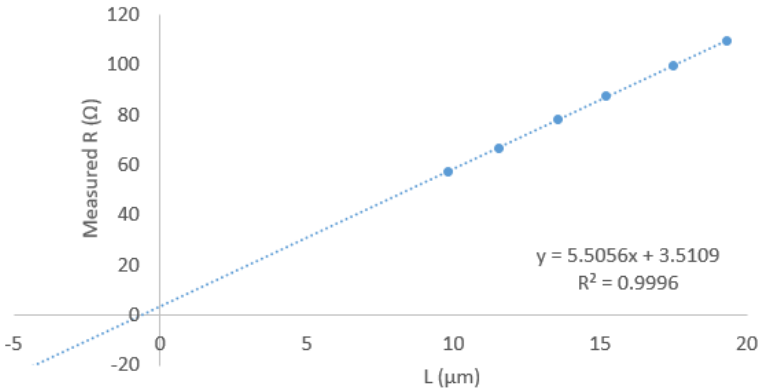
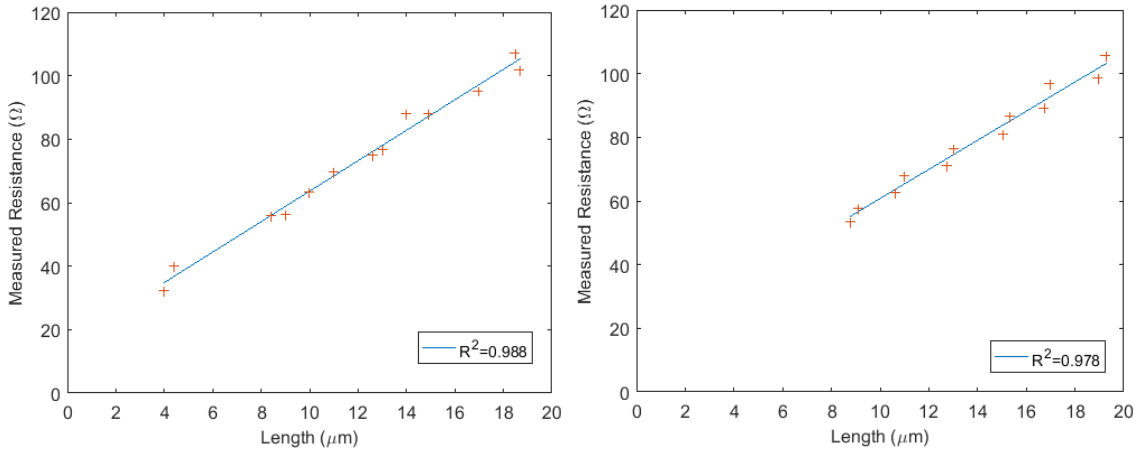


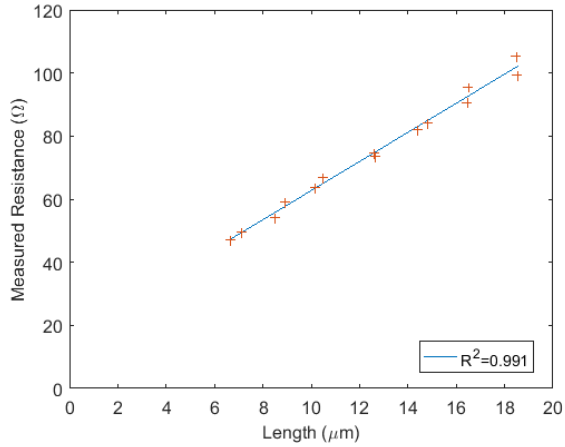
Figure 6-8 Example 2DEG CPW measurements after SOLT calibration: (a) S12/S21 (b) S11/S22 (c) S12/S21 phase and (d) S11/S22 on Smith

Figure 6-8 depicts a very good linear fit with very high R^2 value. However, it is known that imperfections at the semiconductor surface, such as surface states (i.e. dangling bonds or other defects), affect the barrier height and the contact formation. [49] states that the error in extracted ρ_c and R_{sh} can be as high as 100-1000% if the wafer shows a variation of 10-30% in electrical parameters and the best results are obtained for $L \geq 2L_T$. Considering the material and fabrication tolerances, more than one TLM structure is used for the ohmic contact characterization. At least two TLM sets from different sides of the wafer are included in the analysis. The TLM plots for the ohmic contact after contact formation and RTP are depicted in Figure 6-9 and the extracted parameters are summarized in Table 6-2.

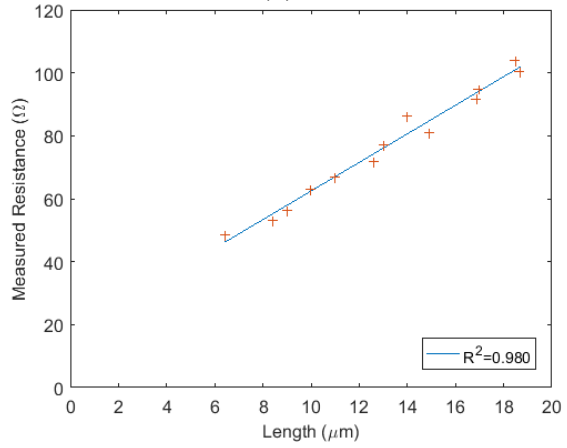


(a)

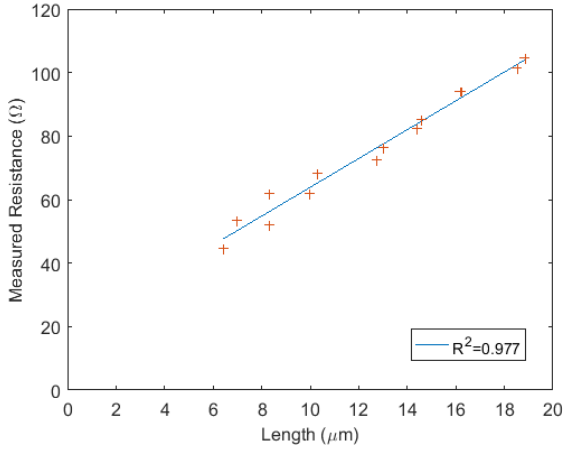
(b)



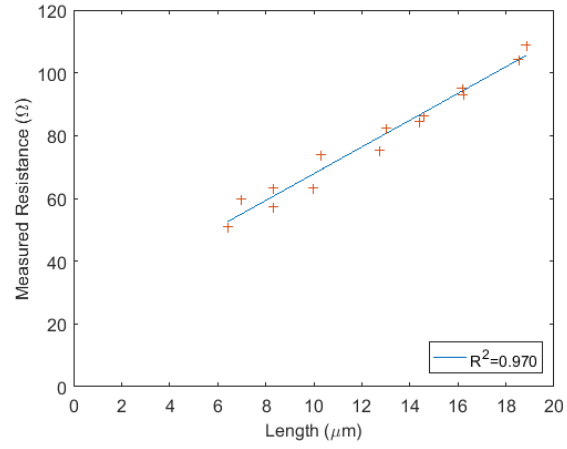
(c)



(d)



(e)



(f)

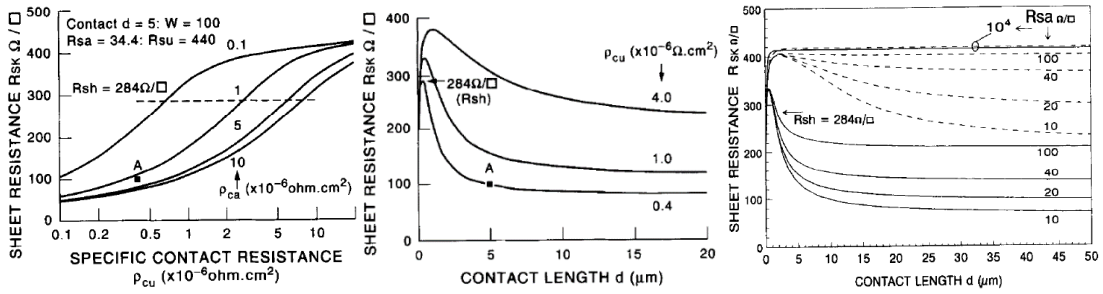
Figure 6-9 TLM results for (a) Narrow (b) Wide (c) Norm (d) Active (e) 5by 1 and (d) 5 by2 ohmic contacts after RTP

Table 6-2 Ohmic contact parameters extracted from TLM after RTP

Contact	R_{sh} (Ω/□)	Rc (Ω)	Rc (Ωmm)	Lt (μm)	Rho (Ωcm^2)	Fit R^2
Narrow	436.69	7.82	0.71	1.63	1.15e-5	0.988
Wide	415.23	7.52	0.68	1.64	1.13e-5	0.978
Norm	419.94	8.29	0.75	1.80	1.36e-5	0.991
Active	413.26	8.52	0.78	1.88	1.46e-5	0.980
5 by 2	387.89	12.62	1.15	2.96	3.40e-5	0.970
5 by 1	412.99	9.25	0.84	2.04	1.71e-5	0.977

It should be noted that the expressions for TLM are derived assuming simple metal / semiconductor combinations and they do not accurately represent alloyed contacts or non-alloyed heterojunction contacts. These contacts do not consist of only the contact metal, the semiconductor and a single interface, but also a third layer in between and total of two interfaces with different resistivities which alters the lateral current flow. As a result, the R_{sh} extracted with TLM can be different than the actual R_{sh} of the contacted layer. Reported values are generally lower than the semiconductor sheet resistance but some higher values are also reported. A 'tri-layer transmission line model' is derived for more accurate modeling of these contacts in [71]. [71] suggests that if some of the epilayers is consumed by the alloying process, its sheet resistance will increase in the unalloyed portion. The decrease is determined by the ratio of thickness variation. The change in the sheet resistance of the alloyed portion depends on the alloying process. The sheet resistance extracted from TLM is the combination of sheet resistances from both alloyed and underlying unalloyed regions, with the combination depending on the current flow in these layers, determined by the resistivities of the two interfaces. Figure 6-10(a) shows the effect of interface resistivities on the TLM extracted sheet resistance. Whether this value

is higher or lower than the actual sheet resistance depends on the combination of both resistivities. Figure 6-10 (b) and (c) depict the contact length dependence of the extracted R_{sh} for varying values of alloyed - unalloyed layer interface resistivity and alloyed layer sheet resistance, respectively. The dashed values in Figure 6-10(c) are for interface resistivities of 10^{-6} Ωcm^2 and for the solid lines the resistivity of alloyed-unalloyed interface is increased to 10^{-5} Ωcm^2. Figure 6-10 indicates that the sheet resistance extracted from alloyed contacts is length-dependent and it varies significantly for short contacts, showing a peak for some short length value, determined by the combination of other parameters. This is observed in for the Narrow and 5 by 2 contact sets with contact lengths lower than 11 μm.

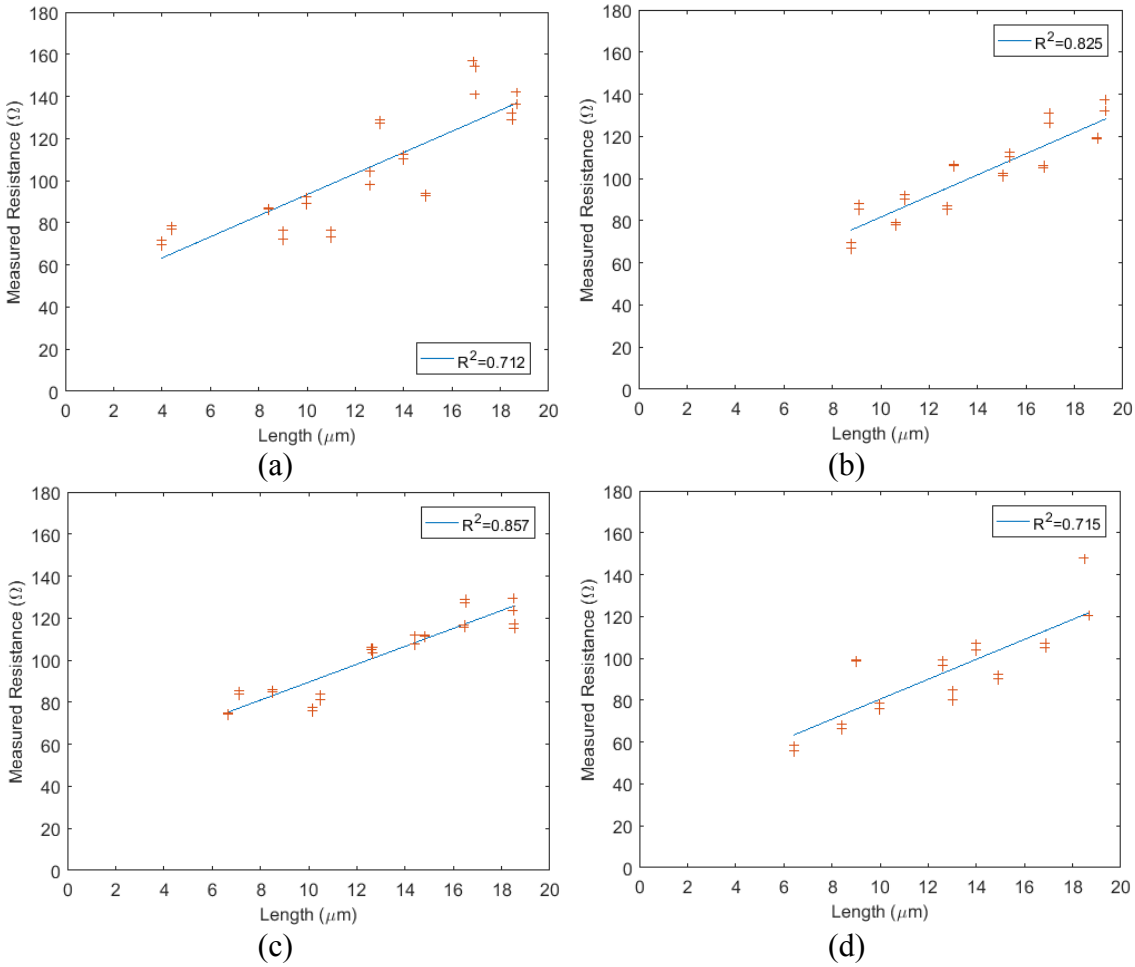


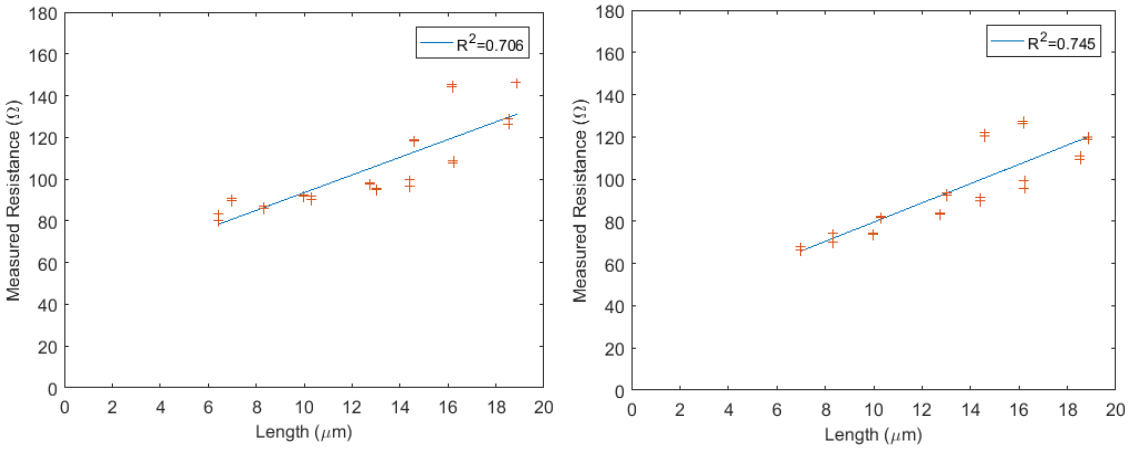
(a) (b) (c)

Figure 6-10 Deviation of sheet resistance extracted with TLM from alloyed contacts from actual material sheet resistance due to (a) interface layer resistivities, (b) unalloyed interface layer resistivity and contact length and (c) alloyed region sheet resistance and contact length [71]

TLM measurements are repeated after the Al measurement pads are fabricated over the ohmic contacts. The TLM data are plotted in Figure 6-11 and the extracted values are tabulated in Table 6-3. Results show a large increase in extracted values after Al

deposition. The resistivity of the e-beam deposited Al is higher than ideal as according to the measurements included in Section 6.1.1. Contact resistance repeatability issues while probing Al also results in a larger variation in the data as can be observed in Figure 6-11. Al deposition was rotational to obtain uniform film thickness. However, there can still be non-uniformities related to fabrication that also contribute to the resistance variations.





(e) (f)

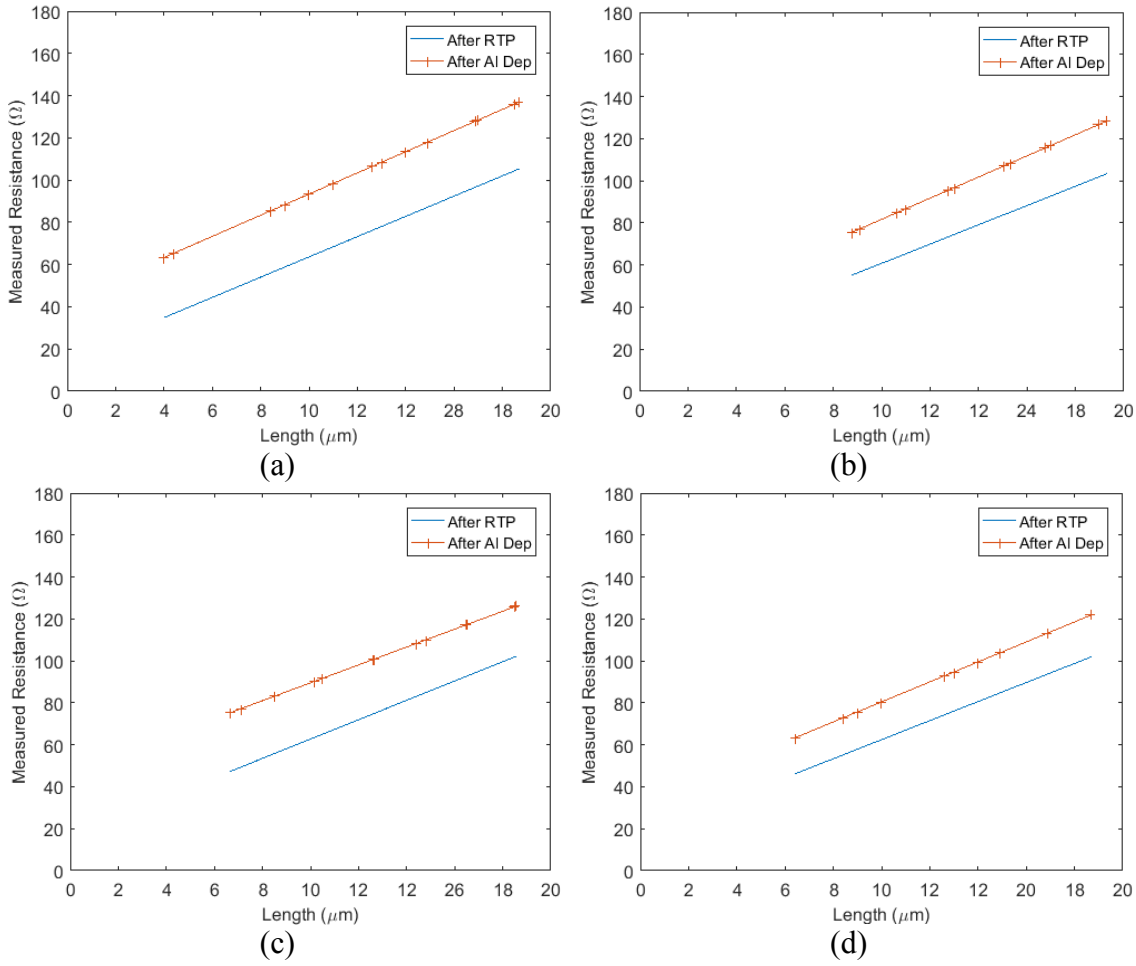
Figure 6-11 TLM results for (a) Narrow (b) Wide (c) Norm (d) Active (e) 5by 1 and (d) 5 by2 ohmic contacts after Al deposition

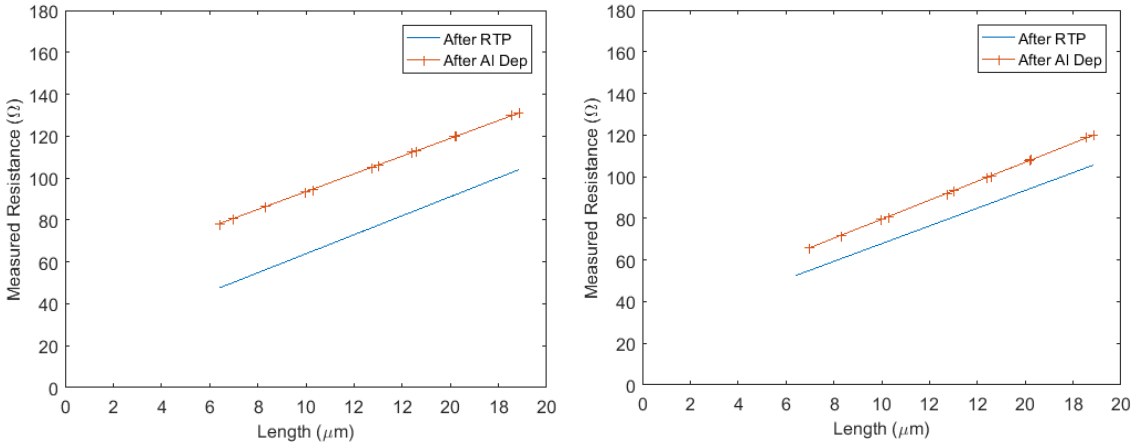
Table 6-3 Ohmic contact parameters extracted from TLM after Al deposition

Contact	R_{sh} (Ω/□)	Rc (Ω)	Rc (Ωmm)	Lt (μm)	Rho (Ωcm^2)	Fit R^2
Narrow	456	21.64	1.97	4.32	8.50e-5	0.712
Wide	456.56	15.77	1.43	3.14	4.51e-5	0.825
Norm	388.01	23.45	2.13	5.5	1.17e-4	0.857
Active	433.6	16.4	1.49	3.44	5.14e-5	0.715
5 by 2	415	16.99	1.55	3.73	5.76e-5	0.745
5 by 1	386	25.5	2.32	6.02	1.4e-4	0.706

The fits obtained from TLM measurements before and after Al deposition are plotted together for comparison in Figure 6-12. The large increase in resistance with Al deposition is clearly observed. The slopes of the TLM curves are similar before and after the deposition; the variation observed is attributed to the difference in probing repeatability on Al and Au. Same slope is expected as the Al is not alloyed and will not affect the sheet resistance of the area under the contact. However, any extraction of x- and y- intercepts for TLM structures with Al will result in erroneous contact parameters. The Al pads are

created for ease of TLM measurements and in order not to damage the contacts during measurement. Results suggest parameter extraction with large pad structures do not yield accurate results.





(e) (f)

Figure 6-12 Resistance of TLM structures before and after Al deposition for (a) Narrow (b) Wide (c) Norm (d) Active (e) 5by 1 and (d) 5 by2 ohmic contacts

6.2.2. De-embedded Circuit Elements from RF Test Structures

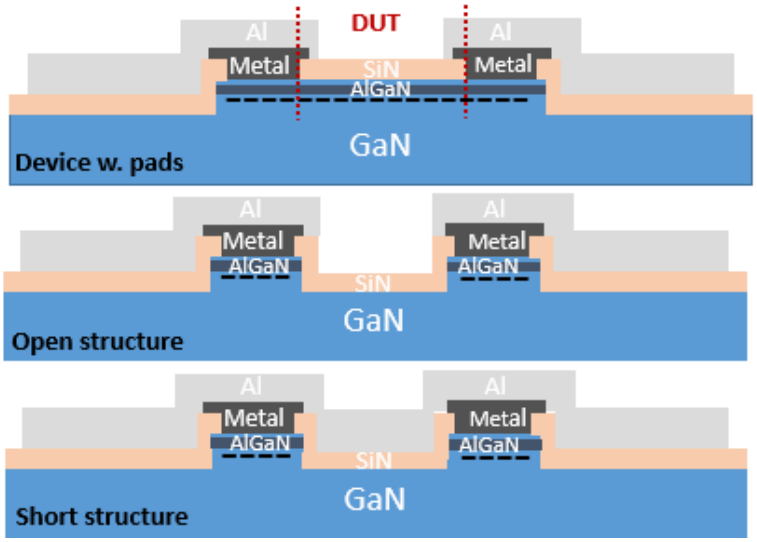


Figure 6-13 2DEG transmission line embedded in CPW pads and the open – short deembedding structures used in RF measurements.

RF measurements are taken after SOLT calibration from the 2DEG transmission line embedded in CPW pads, and corresponding open and short de-embedding structures, all

depicted in Figure 6-13. Three sets of s-parameter data from these three structures are used to de-embed the 2DEG transmission line s-parameters, as described in Section 4.5. The de-embedded circuit elements, depicted in Figure 6-14, are plotted in Figure 6-15 for test structures with different length 2DEG transmission lines.

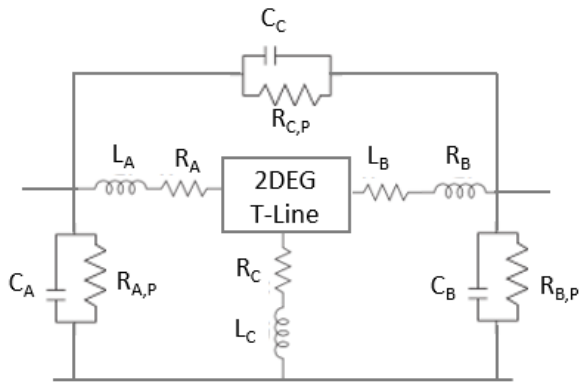
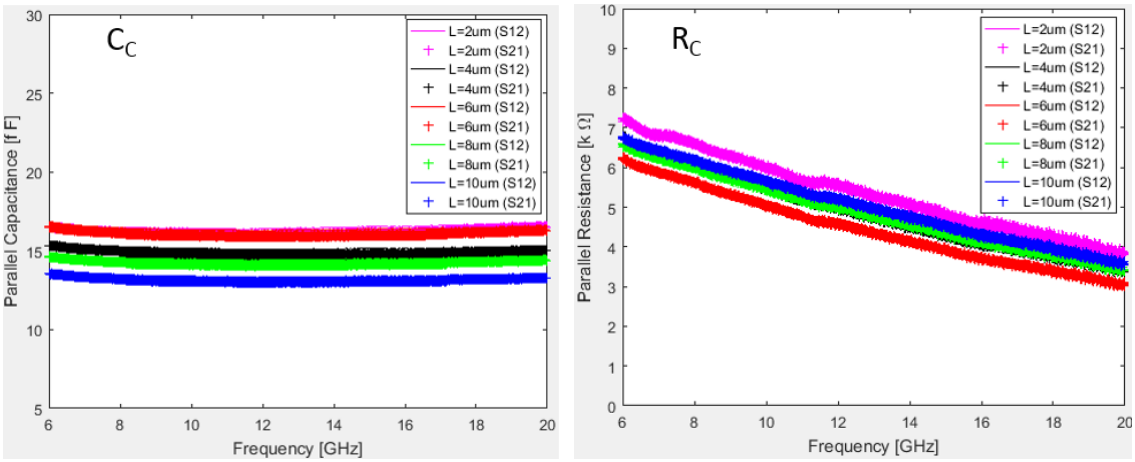
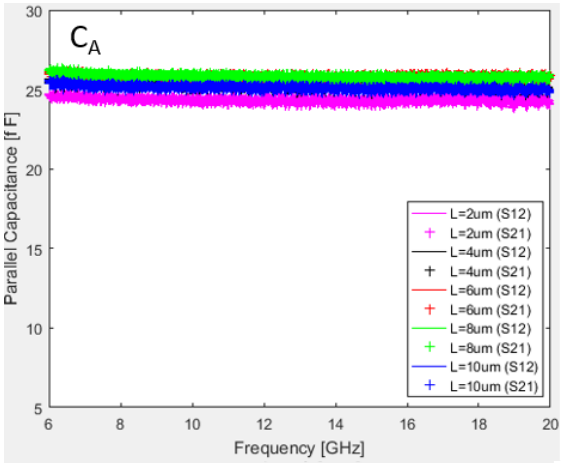
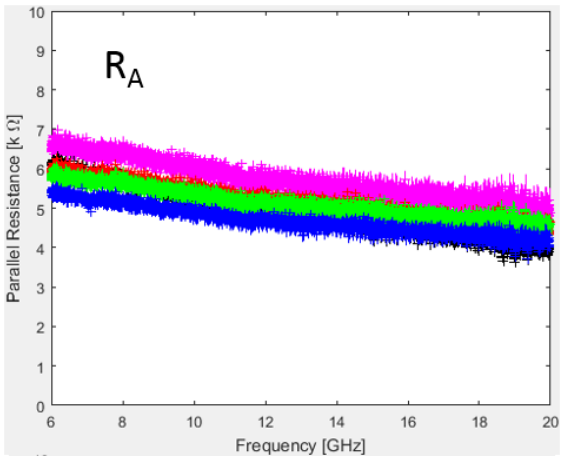
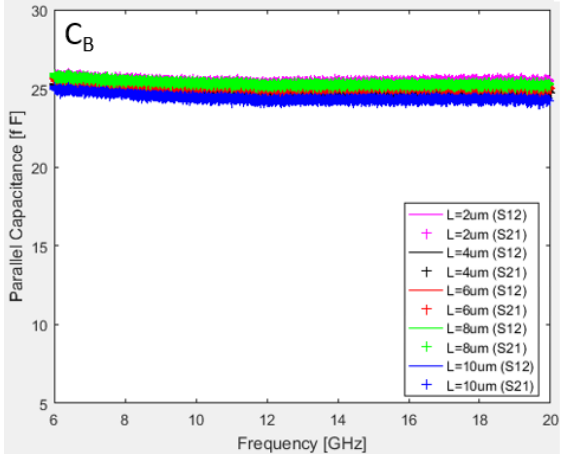


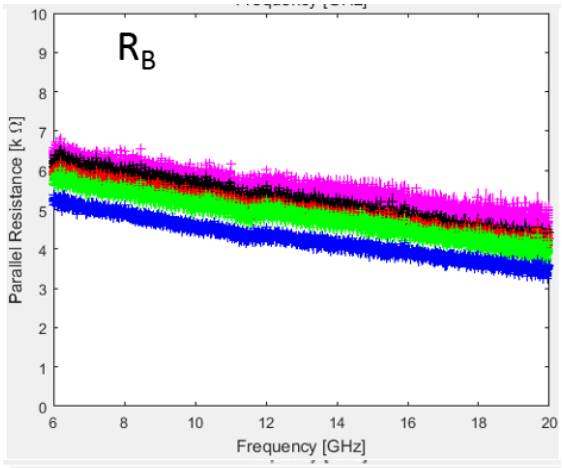
Figure 6-14 De-embedded circuit elements with open – short structures.

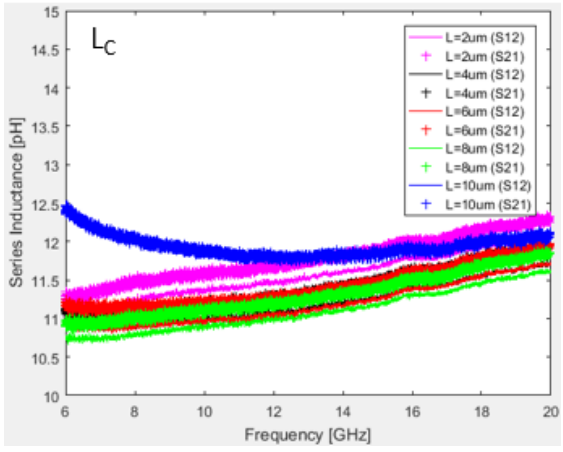


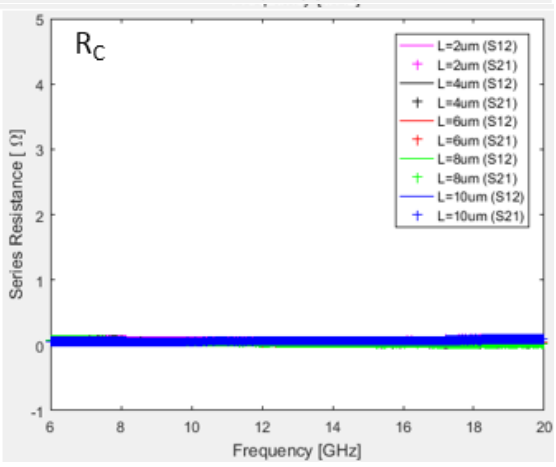

C_A
Parallel Capacitance [f F]
Frequency [GHz]
L=2um (S12)
L=2um (S21)
L=4um (S12)
L=4um (S21)
L=6um (S12)
L=6um (S21)
L=8um (S12)
L=8um (S21)
L=10um (S12)
L=10um (S21)


R_A
Parallel Resistance [k Ω]
Frequency [GHz]


C_B
Parallel Capacitance [f F]
Frequency [GHz]
L=2um (S12)
L=2um (S21)
L=4um (S12)
L=4um (S21)
L=6um (S12)
L=6um (S21)
L=8um (S12)
L=8um (S21)
L=10um (S12)
L=10um (S21)


R_B
Parallel Resistance [k Ω]
Frequency [GHz]


L_C
Series Inductance [pH]
Frequency [GHz]
L=2um (S12)
L=2um (S21)
L=4um (S12)
L=4um (S21)
L=6um (S12)
L=6um (S21)
L=8um (S12)
L=8um (S21)
L=10um (S12)
L=10um (S21)


R_C
Series Resistance [Ω]
Frequency [GHz]
L=2um (S12)
L=2um (S21)
L=4um (S12)
L=4um (S21)
L=6um (S12)
L=6um (S21)
L=8um (S12)
L=8um (S21)
L=10um (S12)
L=10um (S21)

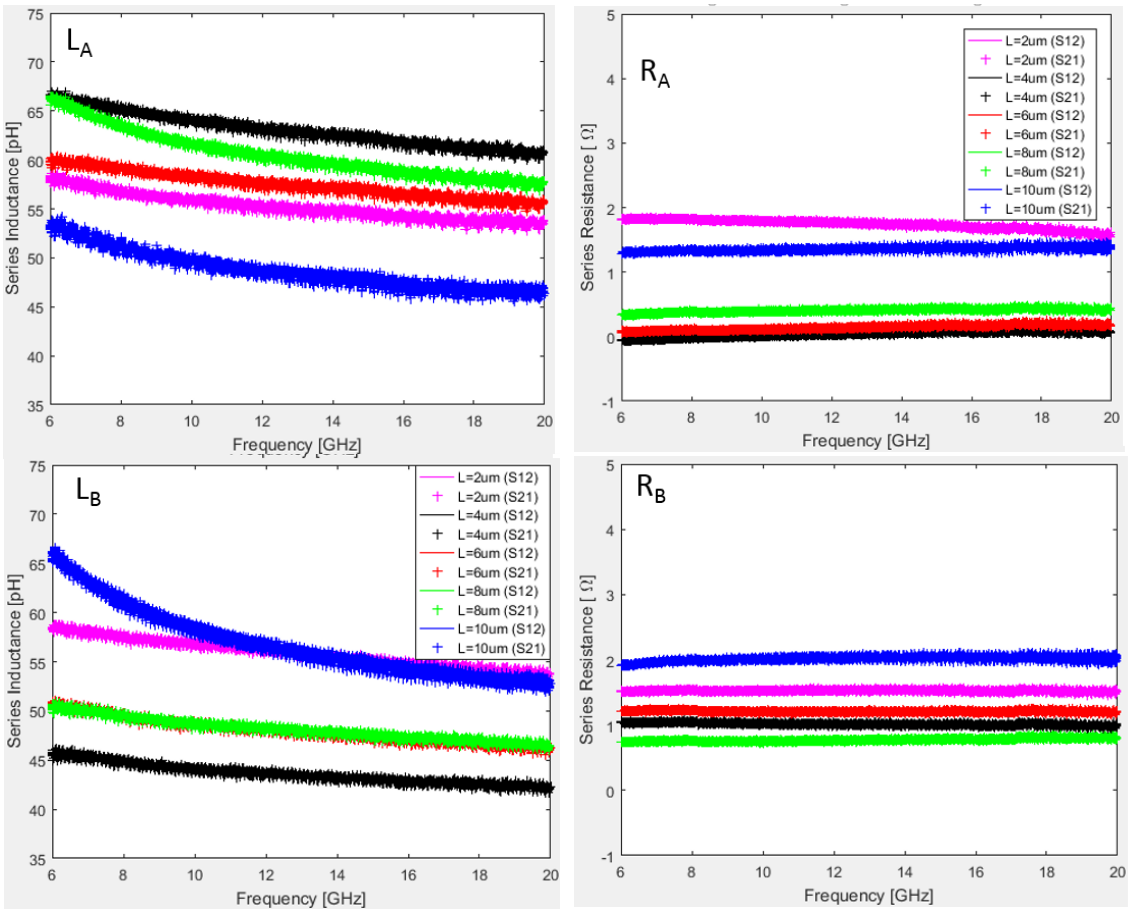
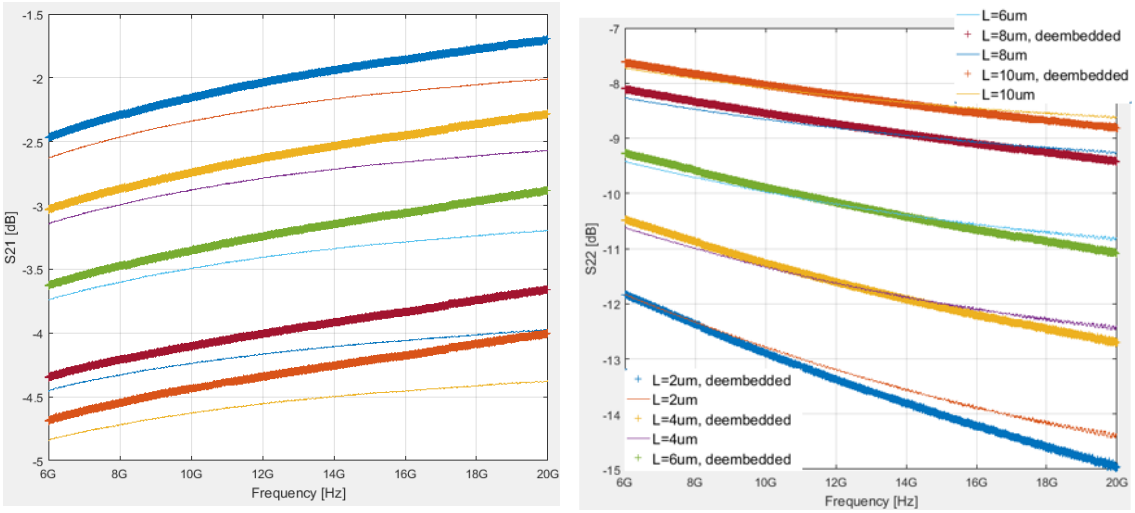


Figure 6-15 De-embedded circuit element values.

6.2.3. 2DEG RF Transmission

Measured and de-embedded S21 and S22 data from DUTs with L = 8, 10, 12, 14 and 16 μm are plotted in Figure 6-16 (a) and (b), respectively, to demonstrate the effects of pad parasitics ohmic contact. One curious result is the decreasing loss with frequency. Plots show that the characteristic impedance match with the measurement ports is improving with increasing frequency and the loss is decreasing. De-embedded data show the same trend.



(a) (b)

Figure 6-16 Measured and de-embedded (a) S21 and (b) S22 from 2DEG transmission line.

S22 data from measured and de-embedded devices are plotted on Smith Chart in Figure 6-17. The 2DEG transmission lines are highly resistive, with the input impedance increasing with L due to high 2DEG resistivity. The measured and deembedded data also indicate capacitive reactance, with deembedding reducing the capacitance as expected.

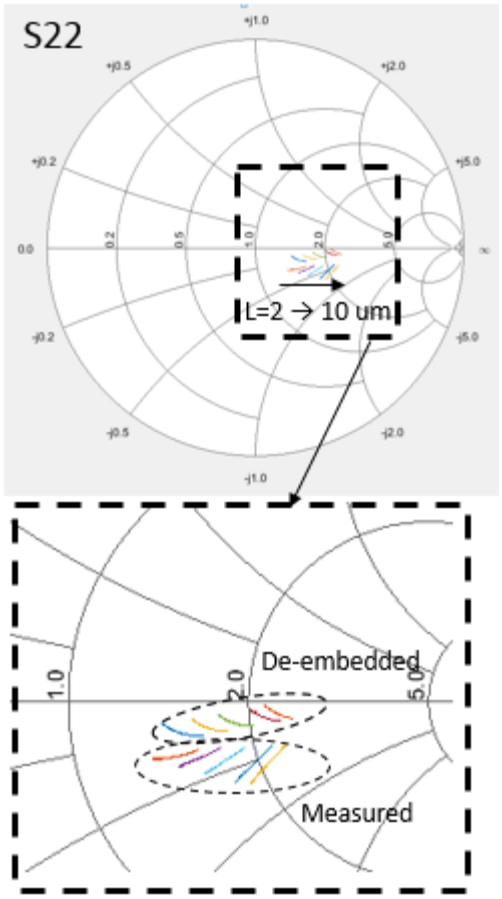


Figure 6-17 Smith Chart S22 for measured and de-embedded 2DEG transmission lines.

Normalized loss (S21/L) is given in Figure 6-18. The variation is unit loss is attributed to material and fabrication tolerances. Average unit loss varies between 0.32 and 0.25 dB/μm. Transmission line loss is expected to increase with frequency because of increasing dielectric losses and, especially, metal losses due to skin effect. As the GaN-on-Si characterization results show increasing dielectric loss with frequency for this substrate, one explanation for the loss data is an opposite trend in metal loss due to 2DEG properties or an unknown parasitic circuit element.

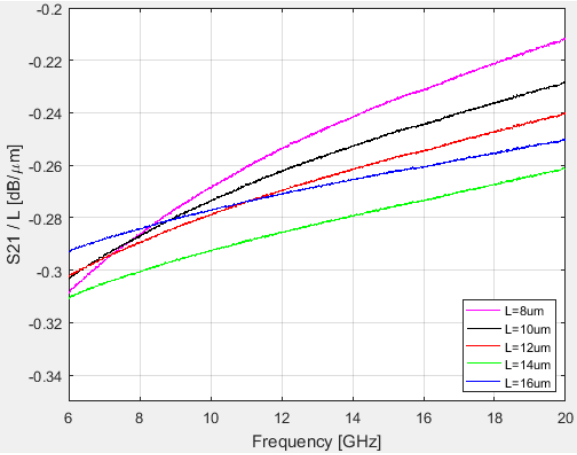


Figure 6-18 Normalized loss for 2DEG transmission line.

Increasing loss could be due to some circuit elements in the transmission path resulting in a high-pass or band-pass transfer function. One possible parasitic element is a depletion capacitance at the ohmic contact to 2DEG. If this is the case, the power level used in the RF measurement would change the depletion region, hence, the capacitance, causing a variation in 2DEG loss with applied RF power. Another possibility is the SiN not properly passivating the AlGaN surface, resulting in positive surface charge and a secondary transmission path. If this is the case, the RF power level would effect this parasitic transmission path by depleting the area especially around the ohmic contacts. In order to test the bias dependence of measured 2DEG loss, RF measurement is repeated for RF powers of 10, 0, -15 and -25 dBm in order to observe its effect on loss. Results are depicted in Figure 6-19. Results do not suggest a systematic variation with RF power; the variation in measured loss is attributed to probing and calibration. A depletion capacitance in the transmission path does not seem probable based on these results.

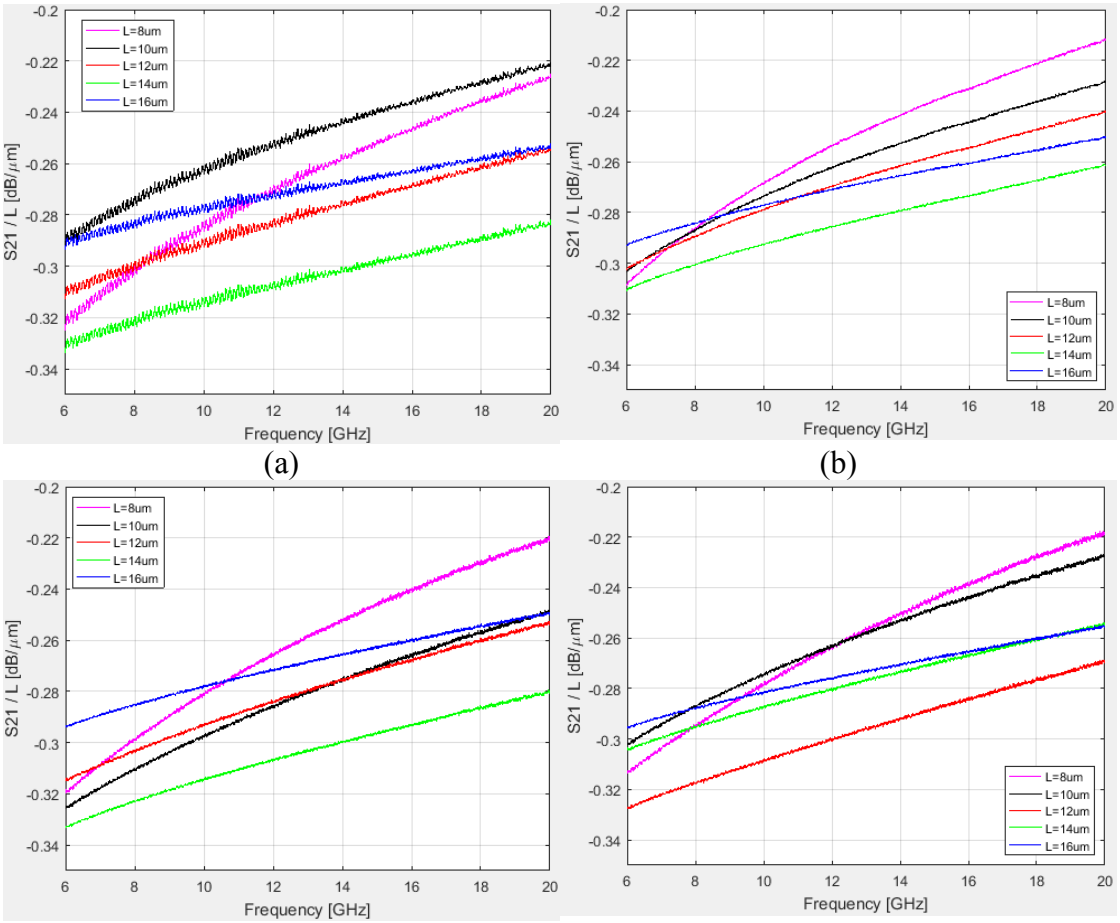


Figure 6-19 Normalized loss for 2DEG transmission line for RF Power of (a) 10 dBm, (b) 0 dBm, (c) -15 dBm and (d) -25 dBm

The short distance between the two ohmic contacts and the metal pads they are embedded in can be resulting in a capacitive path which could explain the loss decrease with frequency. However, this coupling capacitance is expected to be de-embedded with the open-short de-embedding algorithm. The same loss decrease with frequency observed in the mm-long 2DEG CPWs fabricated in the previous design cycle also eliminate this possibility.

Effect of ohmic contact dimensions on the transmission is also investigated by comparing the loss of same geometry 2DEG transmission lines with different ohmic contacts. RF loss observed with three different contact lengths of 11, 22, and 44 µm with contact width of 97 µm are depicted in Figure 6-20. The figure suggests that the ohmic contact length does not have any effect on the 2DEG transmission. The minimum contact length of 11 µm is longer than the transfer length of the ohmic contact.

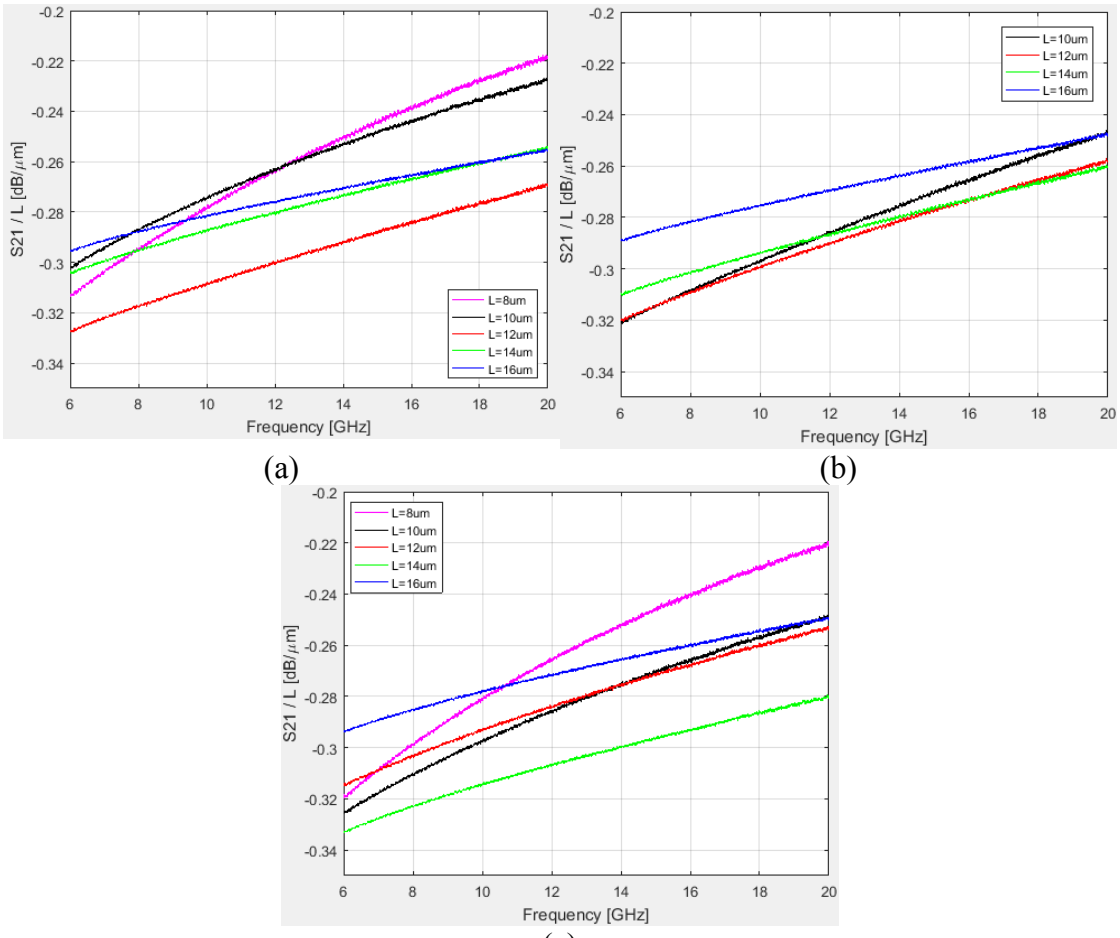


Figure 6-20 Normalized loss for 2DEG transmission line with different ohmic contacts of (a) L = 11 µm narrow, (b) L = 22 µm norm and (c) L = 44 µm wide

7. SUMMARY AND CONCLUSIONS

Microwave loss of CPW structures built on AlN-on-Si and GaN-on-Si with different AlN and GaN layer thicknesses is measured and analyzed as a part of this study. Overall effective loss tangent, as well as conductivity and dielectric loss tangent of different samples are extracted and reported. Results demonstrate an increase in conductivity not only with the addition of III-nitride epi-layers but also with the thickness of these layers. Based on literature and our results, the change in conductivity seems to be correlated with the change in screw type threading dislocation density, but physical characterization of screw-type dislocations is required. A sharp increase in dielectric loss tangent is observed with nitride layers compared to Si and this is associated with dipolar losses. AlN samples and 595 nm GaN sample is found to have similar dielectric loss tangents but a large increase in $tan\delta_d$ is observed for 795 nm GaN sample. The increase in dielectric loss tangent for thicker GaN is attributed to change in strain state and overall net polarization with GaN thickness.

Microwave loss of AlN-on-Si is further investigated to understand underlying loss mechanisms. Measured results demonstrate an AlN thickness dependence on the overall dielectric loss, leading to a need to separate loss of AlN and the previously reported parasitic conductive layer at the AlN-Si interface. Simulations and comparison thereof with the data indicate a higher loss contribution due to AlN. The results indicate an upper limit of 1 S/m on interface layer conductivity, at most, while the lower boundary of AlN conductivity is 15 S/m. The high density of threading dislocations is a potential contributor

to the extracted AlN conductivity, but additional physical characterization is required to illuminate the reason for the loss.

Finally the 2DEG RF transmission properties over 6 – 20 GHz range is reported for the first time. Transmission loss is found to be decreasing with frequency, contrary to metal transmission lines. SiN leakage and depletion capacitance at the ohmic contact – 2DEG interface are eliminated as possible causes. Further analysis is required to determine the underlying reasons for the loss behavior. As a part of the 2DEG transmission study, different ohmic contact geometries are also characterized.

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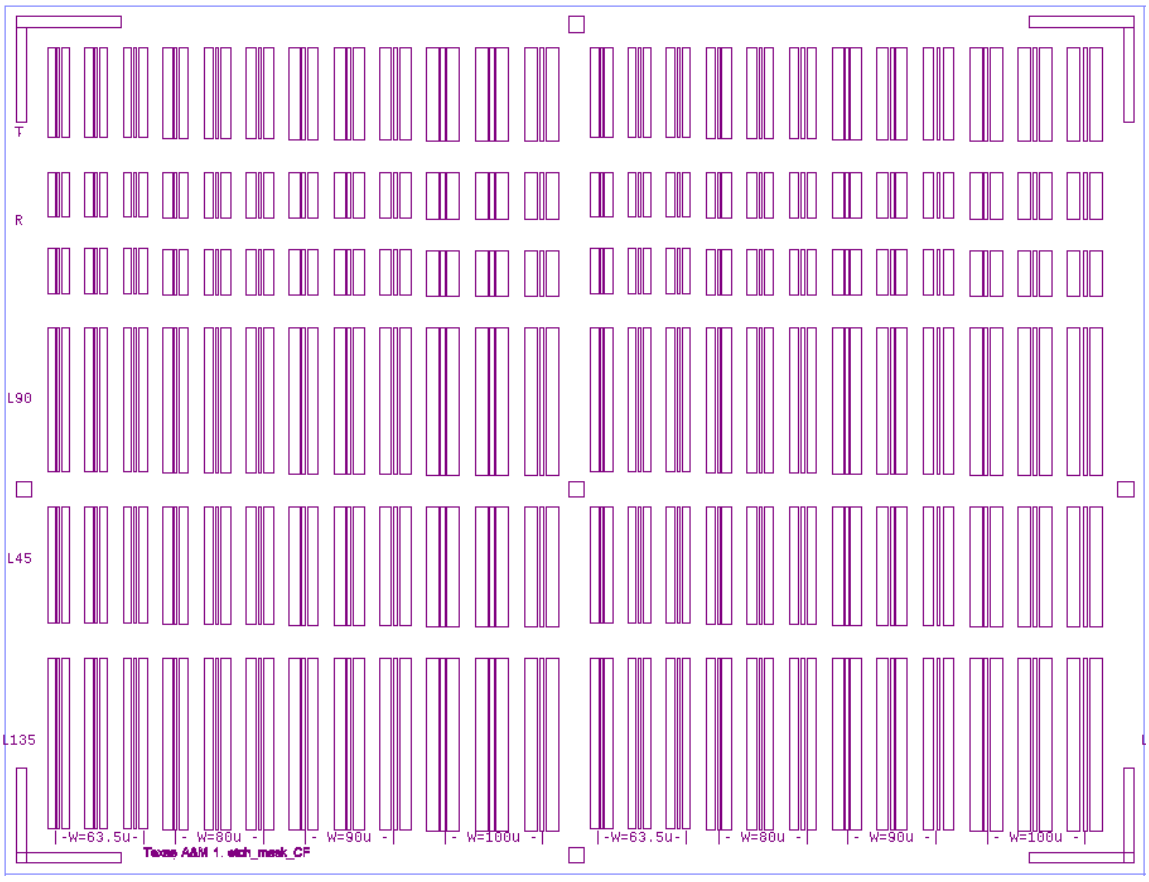
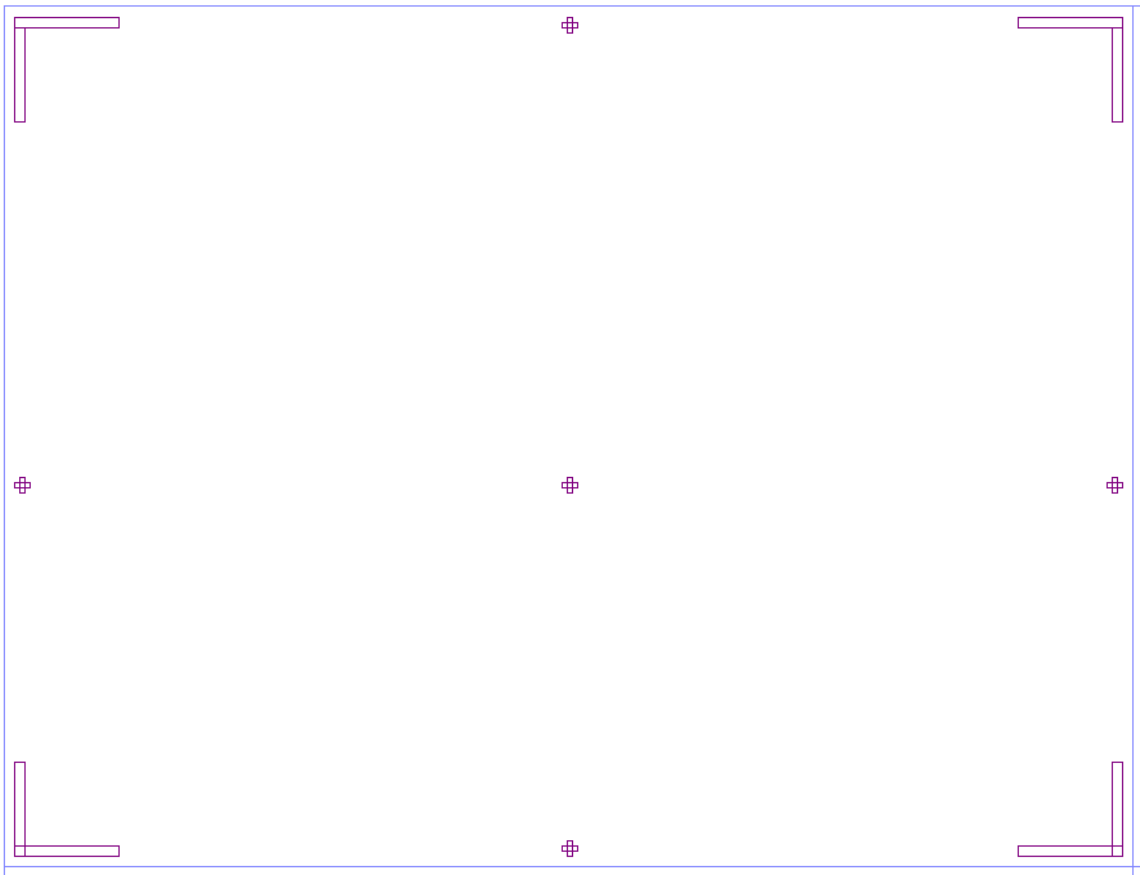
APPENDIX

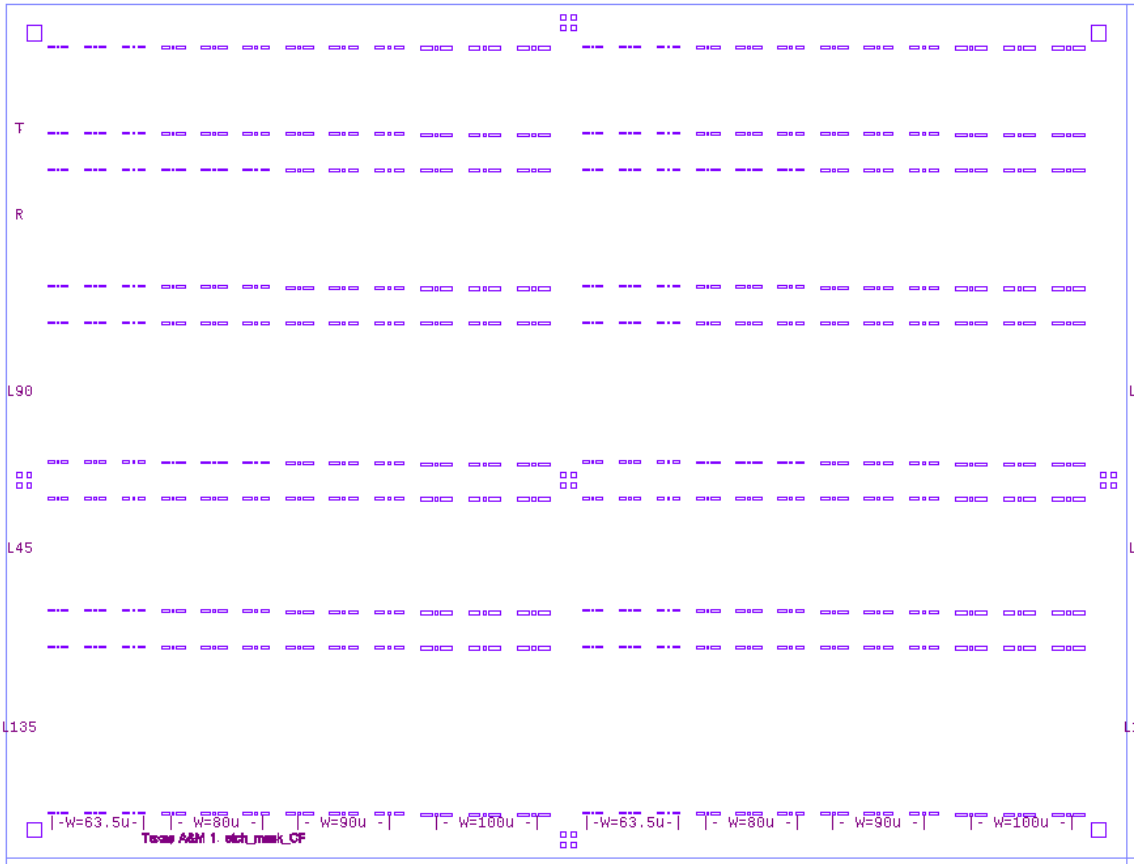
FIGURES



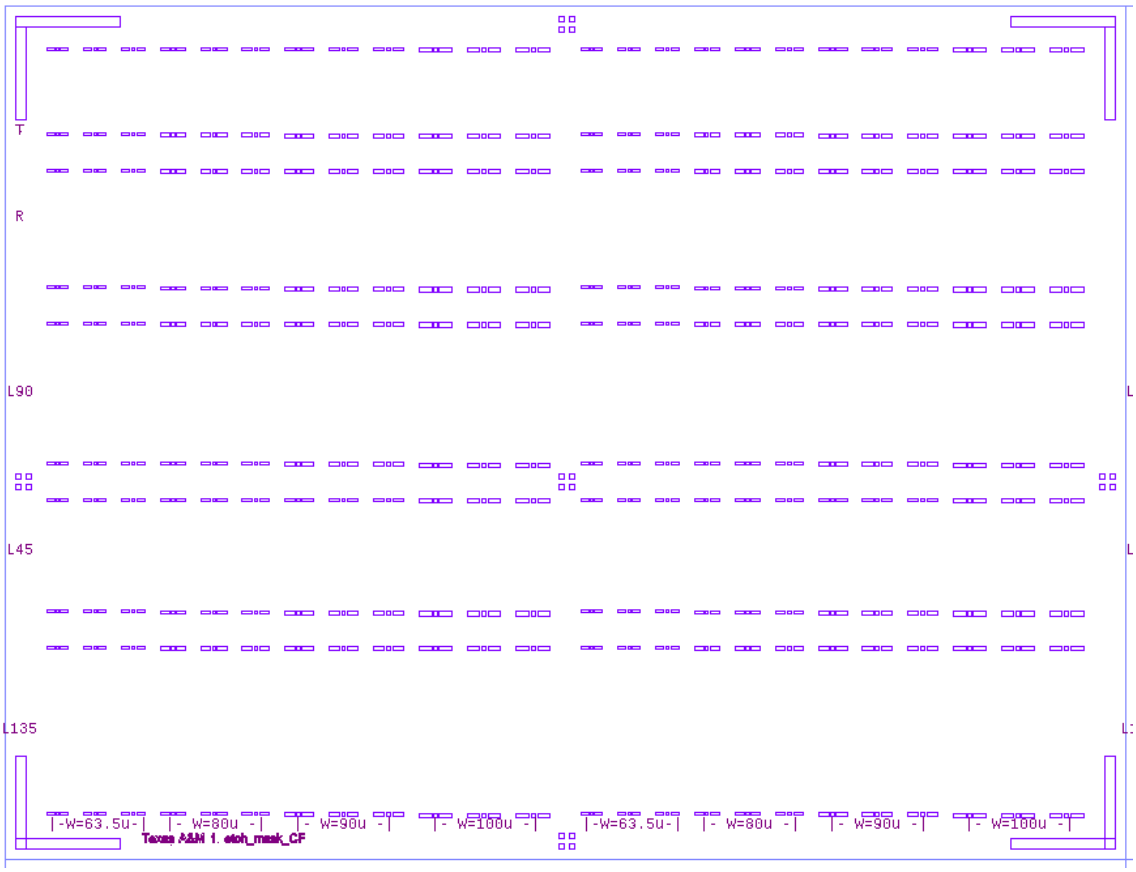
A.1. Mask 1 – Clear Field



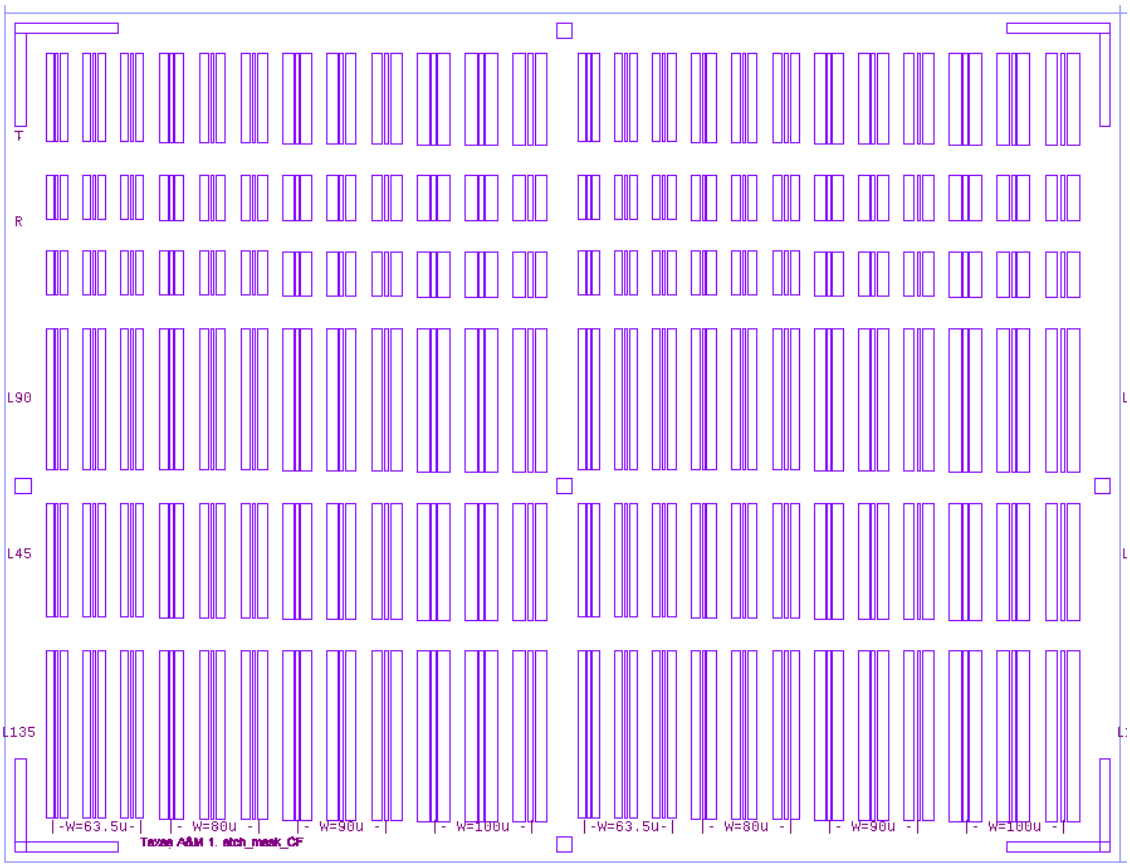
A.2. Mask 2 – Clear Field



A.3. Mask 3 – Dark field



A.4. Mask 4 – dark field



A.5. Mask 5 – dark field