LOW NOISE, JITTER TOLERANT CONTINUOUS-TIME SIGMA-DELTA MODULATOR

A Dissertation

by

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ABSTRACT

The demand for higher data rates in receivers with carrier aggregation (CA) such as LTE, increases the efforts to integrate large number of wireless services into single receiving path, so it needs to digitize the signal in intermediate or high frequencies. It relaxes most of the front-end blocks but makes the design of ADC very challenging. Solving the bottleneck associated with ADC in receiver architecture is a major focus of many ongoing researches. Recently, continuous time Sigma-Delta analog-to-digital converters (ADCs) are getting more attention due to their inherent filtering properties, lower power consumption and wider input bandwidth. But, it suffers from several non-idealities such as clock jitter and ELD which decrease the ADC performance.

This dissertation presents two projects that address CT-$\Sigma\Delta$ modulator non-idealities. One of the projects is a CT-$\Sigma\Delta$ modulator with 10.9 Effective Number of Bits (ENOB) with Gradient Descent (GD) based calibration technique. The GD algorithm is used to extract loop gain transfer function coefficients. A quantization noise reduction technique is then employed to improve the Signal to Quantization Noise Ratio (SQNR) of the modulator using a 7-bit embedded quantizer. An analog fast path feedback topology is proposed which uses an analog differentiator in order to compensate excess loop delay. This approach relaxes the requirements of the amplifier placed in front of the quantizer. The modulator is implemented using a third order loop filter with a feed-forward compensation paths and a 3-bit quantizer in the feedback loop. In order to save power and improve loop linearity a two-stage class-AB amplifier is developed. The prototype modulator is implemented in $0.13\mu m$ CMOS technology, which achieves peak Signal to Noise and Distortion

Ratio (SNDR) of 67.5dB while consuming total power of 8.5-mW under a 1.2V supply with an over sampling ratio of 10 at 300MHz sampling frequency. The prototype achieves Walden's Figure of Merit (FoM) of $146fJ/step$.

The second project addresses clock jitter non-ideality in Continuous Time Sigma Delta modulators (CT-$\Sigma\Delta$M), the modulator suffer from performance degradation due to uncertainty in timing of clock at digital-to-analog converter (DAC). This thesis proposes to split the loop filter into two parts, analog and digital part to reduce the sensitivity of feedback DAC to clock jitter. By using the digital first-order filter after the quantizer, the effect of clock jitter is reduced without changing signal transfer function (STF). On the other hand, as one pole of the loop filter is implemented digitally, the power and area are reduced by minimizing active analog elements. Moreover, having more digital blocks in the loop of CT-$\Sigma\Delta$M makes it less sensitive to process, voltage, and temperature variations. We also propose the use of a single DAC with a current divider to implement feedback coefficients instead of two DACs to decrease area and clock routing. The prototype is implemented in TSMC 40 nm technology and occupies 0.06 mm^2 area; the proposed solution consumes 6.9 mW, and operates at 500 MS/s. In a 10 MHz bandwidth, the measured dynamic range (DR), peak signal-to-noise-ratio (SNR), and peak signal-to-noise and distortion (SNDR) ratios in presence of 4.5 ps RMS clock jitter (0.22% clock period) are 75 dB, 68 dB, and 67 dB, respectively. The proposed structure is 10 dB more tolerant to clock jitter when compared to the conventional $\Sigma\Delta$M design for similar loop filter.

DEDICATION

To my lifelong love and best friend, Ali

To my precious and devoted parents, Farideh and Gholamreza

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NOMENCLATURE

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
CT-ΣΔM	Continuous Time Sigma Delta modulators
STF	Signal Transfer Function
NTF	Noise Transfer Function
DR	Dynamic Range
SNR	Signal to Noise Ratio
SNDR	Signal to Noise and Distortion Ratio
GD	Gradient Descent
FoM	Figure of Merit
OOB	Out Of Band
MASH	Multi-stAge noise SHaping
PLL	Phase Locked Loop
PN	Phase-Noise
OSR	Over Sampling Ratio
OBG	Out of Band Gain
OpAmp	Operational Amplifier
ELD	Excess Loop Delay

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1. INTRODUCTION: THE IMPORTANCE OF RESEARCH

In this chapter we discuss the motivation for high resolution, low power ADCs, research contribution and dissertation organization.

1.1 Motivation for high resolution, low power ADC

With the tremendous developments on wireless communications, different wireless services and standards are proposed each year, such as GSM, CDMA, UMTS and most recently 4G and 5G. Wireless communication is rapidly advancing and new wireless applications emerges. More recent application is Internet of Things(IoT), which combines all the wireless standards. Each standards has special signal power, signal bandwidth, signal frequency and coding methods, so the required hardware for each one should be unique and challenging. As a result, integrating different wireless in a single chip and to make them work efficiently for different standards is challenging trend in semiconductor industry. The software-defined radio receiver architecture is a potential candidate to realize the multi-standard receiver. With no DC offset and the relaxed image problem, this architecture eases the front-end circuit specifications. However, the requirements of large bandwidth (10MHz for video communication), high operational performance and trend to move ADC as close to antenna as possible make the ADC design a challenging problem in today's technology. And among many ADCs CT-$\Sigma\Delta$ is more suitable due to their oversampling, dynamic range, power consumption and trading speed for resolution.

1.2 Research contribution, technical challenges associated with ADC

In this work the problem of designing low power, high resolution CT-$\Sigma\Delta$ ADCs has been addressed. The solution to some of the non-idealities including ELD and jit-

ter is investigated. Two CT-ΣΔ modulators are proposed, implemented and tested in this thesis. Quantization noise reduction technique is proposed and several common issues of the modulator are presented and they resolved by use of the new proposed modulators.

1.3 Dissertation organization

The dissertation is organized as follows: Chapter 2 briefly describes the difference between Nyquist and oversampling ADC, and fundamental of CT-ΣΔM, and non-idealities associated with that. Chapter 3 propose a CT-ΣΔM to solve problem of ELD, and noise calibration. Chapter 4 presents the proposed modulator to reduce the effect of clock jitter in CT-ΣΔ ADC. Chapter 5 concludes the thesis and discusses the future work.

2. OVERSAMPLING ADC

Among different kinds of ADC, CT-ΣΔM is getting popularity due to its inherent properties. In this section we review oversampling ADCs and specially CT-ΣΔM. Also, we discuss the common non-idealities associated with it, and we review the literature about solving the non-idealities issues in CTΣΔM.

2.1 Nyquist rate ADC vs oversampling ADC

According to sampling theory in order to avoid aliasing, sampling frequency (f_s) should be at least twice signal bandwidth (f_{BW}): $f_s > 2f_{BW}$. In Nyquist ADCs which the spectrum is shown in Fig 2.1(a) f_{BW} is as close to $0.5f_s$ as possible. Assuming quantization noise as white noise, the total quantization noise power and spectral density of quantization noise are [52]:

$$\sigma_e^2 = \int_{-\infty}^{\infty} e^2 pdf_e de = \frac{\Delta^2}{12}, \quad S_e(\omega) = \frac{\Delta^2}{12}.\frac{1}{f_s} \tag{2.1}$$

where Δ is quantization step ($\frac{FS}{2^N}$),

If the sampling frequency of ADC is much larger than band-width ($f_s \gg 2f_{BW}$), the ADC becomes oversampling ADC. One of the benefit of oversampling ADC is that the anti-alias filter implementation becomes easier as its transient band increase (Fig. 2.1(b)). Moreover, as total quantization noise power is constant and independent from sampling frequency, by increasing sampling frequency the spectral density of quantization noise decrease, and as a result in-band quantization noise reduces. So, by using a low-pass filter after ADC which is called decimation filter, the out of band quantization noise will be filtered out. In other words it trades precision for speed.

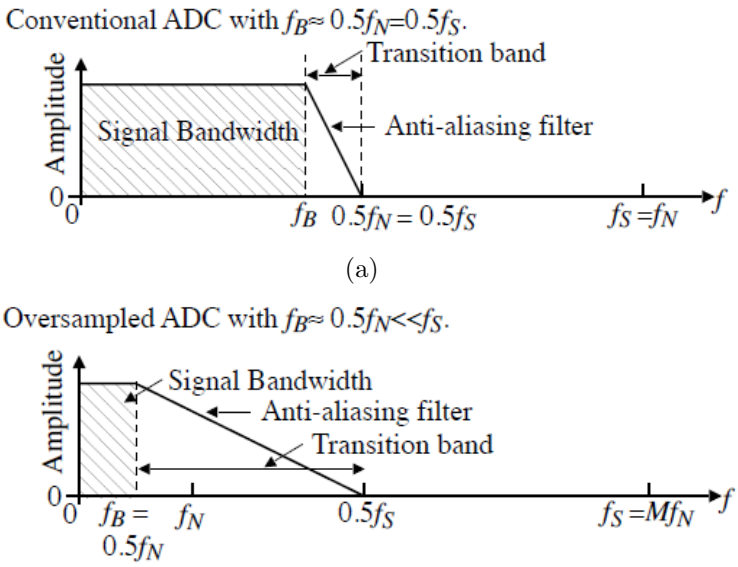


Figure 2.1: Bandwidth requirment [2] (a) Nyquist ADC , (b) Oversampling ADC

The integrated inband quantization noise for oversampling ADC is [52]:

$$IBN_{OSR} = \frac{1}{f_s}\int_{-f_{BW}}^{f_{BW}} \sigma_e^2 df = \frac{\Delta^2}{12}\frac{2f_{BW}}{f_s} = \frac{\Delta^2}{12}\frac{1}{OSR} \tag{2.2}$$

The block diagram of a oversampled ADC is shown in Fig 2.2. It consist of a low-pass anti-alias filter to prevent sampled signal from aliasing to in-band, a modulator which convert analog signal to digital, and a decimator to downsample the high frequency output to lower frequency outputs and finally a digital low pass filter is needed to remove high frequency noise and preserve input signal.

An oversampling converter uses a noise-shaping modulator to reduce the in-band quantization noise to achieve higher degree of resolution. Noise-shaping modulator ($\Sigma\Delta$ modulator) introduce a feedback path to further increase the accuracy. The general form of discrete time (DT) and continuous time (CT) modulator are shown

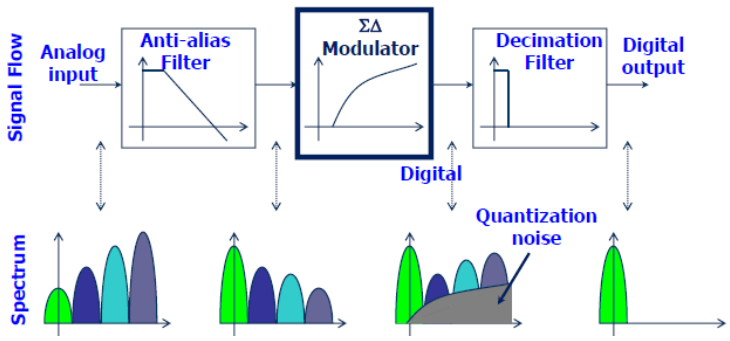


Figure 2.2: Block diagram of a oversampled ADC

in Fig. 2.3. The Signal Transfer Function (STF) and Noise Transfer Function (NTF) euqation for the general system is shown in Eq. 2.3:

$$\begin{aligned} STF &= \frac{D_{out}}{V_{in}} = \frac{LF}{1+LF} \\ NTF &= \frac{D_{out}}{E_Q} = \frac{1}{1+LF} \end{aligned} \tag{2.3}$$

If LF is chosen to be large in band, the STF will be very close to 1 and NTF will be very small in band, so the modualator will pass signal and rejects the quantization noise. The integrated inband quantization noise in presence of L^{th} order noise shaping ($NTF(z) = |1 - z^{-1}|^L$) can be computed as follows:

$$IBN_{OSR,L} = \frac{1}{f_s}\int_{-f_{BW}}^{f_{BW}} NTF^2 \sigma_e^2 df = \frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \tag{2.4}$$

here we assumed that $f_s \gg f_{BW}$, so $|1 - z^{-1}|^2 = (2sin\Omega/2)^2 \approx \Omega^2 = (\frac{2\pi f}{f_s})^2$. So, the maximum SNR assuming input as a sine wave with amplitude of $FS/2$ will be:

$$SQNR_{Max}(dB) = 6.02N + 1.76 + 10(2L+1)\log OSR - 10\log\frac{\pi^{2L}}{2L+1} \tag{2.5}$$

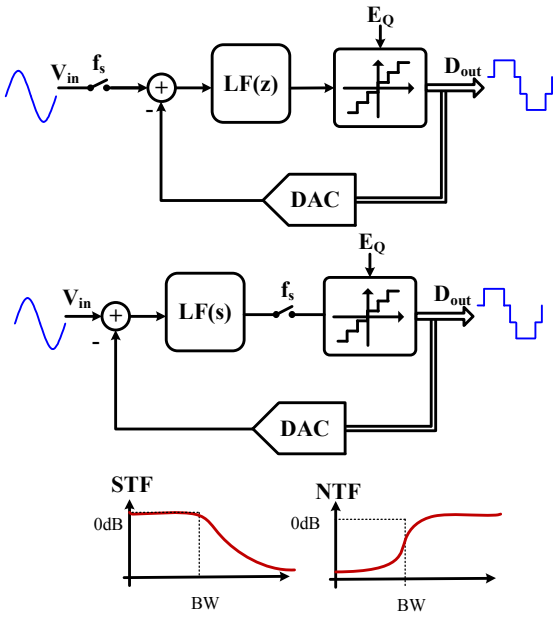


Figure 2.3: DT and CT modulator and general STF and NTF

2.2 Discrete time vs continuous time ΣΔ modulator

Based on place of sampling the modulator can be discrete-time or continuous time. If sampling takes place at input, it results DT modulator and if it takes place after filter and before quantizer it makes CT modulator.

In order to determine the equivalence, in Fig. 2.3 the loop around quantizer is opened and inputs are zeroed, which is shown in Fig. 2.4. A continuous-time modulator would produce the same output bits as the discrete-time modulator if the outputs were equal at the sampling instants, meaning that $u[n] = u(t)|_{t-nt_s}$. This would be satisfied if the following condition were satisfied:

$$LF(z) = Z\{L^{-1}[DAC(s).LF(s)]_{t=nT}\} \tag{2.6}$$

where DAC(s) is the transfer function of the DAC, it can be rectangular, triangular,

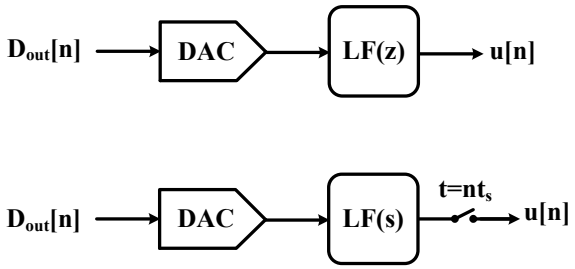


Figure 2.4: DT and CT equivalence

quadratic, sine function [52]. In this thesis we used rectangular DAC shape, so we ignore the analysis of the other functions. We assume rectangular pulse of DAC to have magnitude of 1 that lasts from a to b:

$$DAC(t) = \begin{cases} 1 & a < t < b, 0 < a < b \\ 0 & otherwise \end{cases} \tag{2.7}$$

and the s-domain equivalent of DAC response is:

$$DAC(s) = \frac{e^{-as} - e^{-bs}}{s} \tag{2.8}$$

For $a = 0,\ b = t_s$, this becomes a None-Return-Zero (NRZ) DAC pulse. A Return Zero (RZ) DAC pulse would exist if $a = 0,\ b = 0.5t_s$. Eq. 2.6 allows the transformation between continuous-time and discrete-time filters, and thus allows an analysis of the effects of non-ideal DAC output pulses to be performed on discrete-time equivalents of continuous-time filters. To find an equivalent DT-$\Sigma\Delta$ modulator for a CT-$\Sigma\Delta$ modulator (and vice versa), a time-domain DT-CT transformation method has to be used. The impulse invariant transformation (IIT) is one such method. To actually perform the transformation, the DAC feedback pulse shape has to be

Table 2.1: Continuous time Sigma-Delta modulator advantages vs disadvantages

CT Advantages	CT disadvantages
CT-ΣΔ modulators remove (or relax the requirement) the need for an anti-aliasing filter	CT filters are much more difficult to design and simulate since DT filters are simply made up of delays and gain stages in various loops.
The CT operation of the loop filter relaxes the requirements on the GBW of amplifiers and hence allows the operation at higher speeds or lower power consumption	CT-ΣΔ modulators exhibit several non-idealities such as clock jitter and excess loop delay
The requirements on the sample-and-hold (S/H) circuitry are relaxed because the sampling is performed after the loop filter	

used in Eq. 2.6. There are several references that computed the transformation for different DAC pulse shapes. The use of continuous-time filters provides some improvements over discrete-time filters, while they suffer from some issues. Continuous time advantages and disadvantages are listed in Table 2.1.

2.3 CT-ΣΔ non-ideality

Beside the advantages of CT-ΣΔ, it suffers from some of the non-idealities, in this section we focus on Excess Loop Delay (ELD), clock jitter and effect of OOB blocker.

2.3.1 Excess loop delay

Excess loop delay is a constant delay $t_d = \tau_d T_s$, between the sampling clock edge and the change in output of DAC which is shown in Fig. 2.5 . The sources of ELD include switching time of DAC's output respect to clock edge and input, also the delay between quantizer clocking edge and subsequent latch (which used intentionally to have all the data at output of quantizer at the same time) [52]. τ_d is dependent on the switching speed of the transistors f_t, the quantizer clock f_s, the

number of transistors in the feedback path as well as the loading on each transistor.

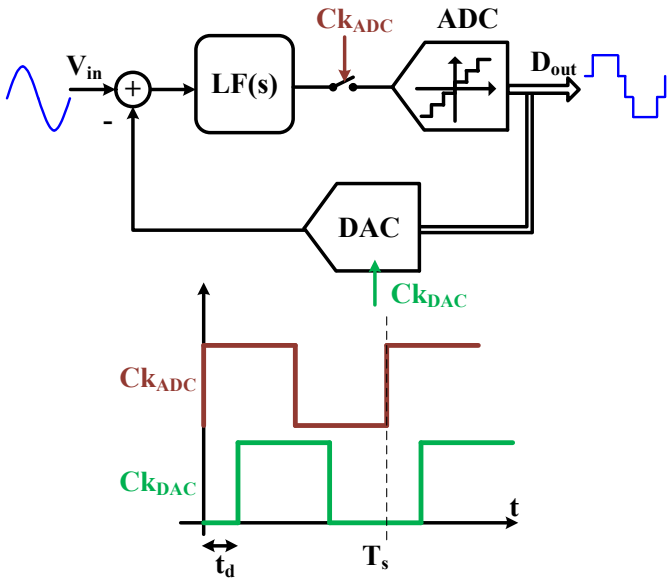


Figure 2.5: ELD in CT-ΣΔ modulator

If the maximum switching frequency of transistor is comparable with sampling frequency, ELD's effect on performance is severe. This is becoming more possible nowadays, as desired speed of ΣΔ increases and it becomes comparable with transistors' maximum switching frequency [13]. In Non-Return-Zero (NRZ) and high speed Return-Zero (RZ) DACs, excess loop delay shifts the DAC's pulse and it is extended to next sampling instant, so it increases the modulator's order and moves the poles of NTF toward unit cycle and exceed the stability boundary for certain excess delay. This issue is becoming more relevant nowadays, as the switching frequency increases to accommodate wider standards such as LTE with aggregated channels.

2.3.2 *Clock jitter effect in CT-ΣΔ*

The CT-ΣΔ modulator is getting more attention in high speed power efficient receivers due to compatibility with CMOS technology and its inherent properties [22], [3]. However, the CT-ΣΔM is sensitive to clock jitter, and the problem becomes critical by increasing the sampling rate of ADC as high frequency low phase noise Phase Locked Loop (PLL) becomes more challenging to design [10]. Clock jitter is a common problem associated with the uncertainty in the timing of the clock edges caused by the finite phase noise (PN) in the generated clock waveform [61]. The clock signal driving sampling switches suffers from unavoidable clock jitter due to the noise components that accompany the frequency synthesizer. Fig. 2.6 shows the phase noise density in a typical oscillator. In the time-domain, the integrated effect of these noise components convolve with out-of-band noise and high frequency blockers, so folding back part of that information to baseband.

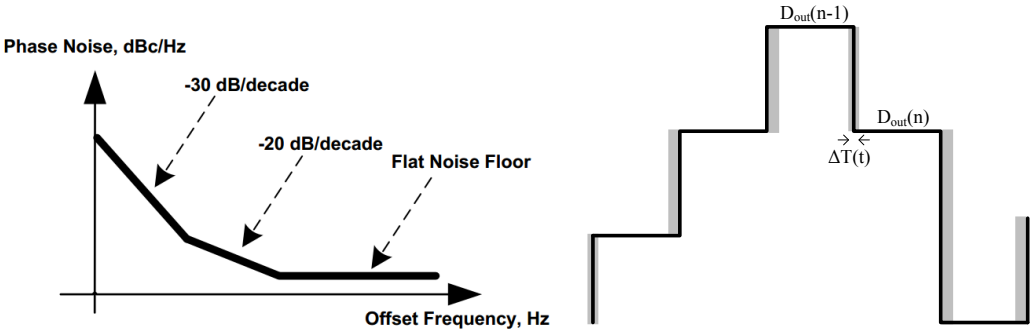


Figure 2.6: (a) Clock phase noise [28], (b) effect of jitter in DAC signal, and the error due to jitter

In data converters, the problem of clock-jitter is a very critical issue and can

significantly deteriorate the achievable SNR. The effect of clock jitter in CT-ΣΔ is divided in two parts, the jitter in forward path and feedback path. The jitter effect in forward path (aperture jitter embedded in the sample and hold) is strongly suppressed by loop filter, similarly to the noise shaping, so it has very little effect in system performance. But, clock jitter in feedback path introduce some error that deteriorates the ADC performance. As main focus of this dissertation is CT-ΣΔ modulators with NRZ rectangular shape DACs, so the jitter analysis of other types DACs are excluded.

Non-return-to-zero DACs are known to be highly sensitive to excess loop delay and also they cause even-order nonlinearities due to mismatch between rise and fall times, in contrast to RZ DAC waveforms. However, they are commonly used in CT modulators due to their simple implementation, relaxed SR requirement on the integrating amplifiers, and lower sensitivity to clock-jitter compared to RZ DACs [61]. Fig. 2.6(b) illustrates the effect of clock jitter in DAC, which can be approximated as [58]:

$$J_{error}(n) = (D_{out}(n) - D_{out}(n-1))\frac{\Delta T(t)}{T} \tag{2.9}$$

where ΔT is the time uncertainty because of jitter in DAC's clock. So, the frequency domain equivalent of Eq. 2.9 will be as:

$$J_{error}(\omega) = [(1 - z^{-1})D_{out}(\omega)] \otimes J_n(\omega) \tag{2.10}$$

where the symbol $\otimes$ means the convolution of the functions. The clock jitter free ΣΔ feedback signal carries digital data ($D_{out}(\omega)$), which includes the in-band desired signal ($V_{in}(\omega)$), the high-pass shaped quantization noise coming from the quantizer

$(E_Q(\omega))$, and the remaining out-of-band thermal noise and blocker signal represented by $(V_B(\omega))$ leading to:

$$D_{out}(\omega) = (V_{in}(\omega) + V_B(\omega)).STF_c(\omega) + E_Q(\omega).NTF_c(\omega) \tag{2.11}$$

where, $STF_c(\omega)$ is the signal transfer function, and $NTF_c(\omega)$ is the noise transfer function. So, the jitter-induced error signal can be computed as:

$$J_{error}(\omega) = (1 - z^{-1}) \left[(V_{in}(\omega) + V_B(\omega)).STF_c(\omega) + E_Q(\omega).NTF_c(\omega)\right] \otimes J_n(\omega) \tag{2.12}$$

The in-band signal is shaped by $1 - z^{-1}$ and only the low-frequency in-band clock phase noise convolves with it and fall in-band, so its effect usually is not critical. The error due to out-of-band quantization noise and blockers increases at higher frequencies where the errors convolves with wide-band clock phase noise, and the result of the convolution falls over the desired band and increases the in-band noise level, as illustrated in Fig. 2.7. The SNR degradation due to jitter is well studied

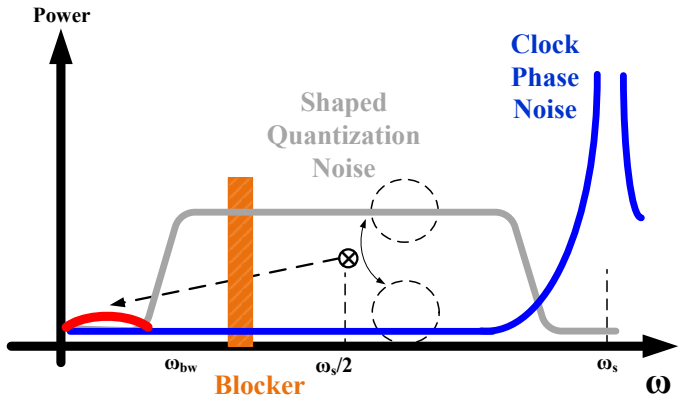


Figure 2.7: PN and quantization noise modulation in DAC

in [11, 12], and the in-band jitter induced noise power is equal to [11]:

$$\sigma^2_{e_{j,NRZ}} = 4OSR.BW^2.\sigma^2_{jitter}.\{\frac{\pi^2}{2}(\frac{A}{\frac{f_s}{2f_{in}}})^2 + \frac{V^2_{FS}\sigma^2_H}{3(N-1)^2}\} \tag{2.13}$$

where $\sigma^2_H = \frac{1}{2\pi}\int_{-\pi}^{\pi} |NTF(e^{j\omega})(1-e^{-j\omega})|^2 d\omega$ is RMS value of high pass filtered NTF. So, the SNR will have two parts, one associated with first part of inband jitter induced due to input signal and second part due to noise shaping behavior of CT-ΣΔM:

$$SNR_{signal} = \frac{OSR}{4\pi^2 f^2_{in}\sigma^2_{jitter}} \tag{2.14a}$$

$$SNR_{NTF} = \frac{3(A/V_{FS})^2(M-1)^2}{8OSR.BW^2\sigma^2_{jitter}\sigma^2_H} \tag{2.14b}$$

According to the Eq. 2.14, if the first term is dominant, SNR can be improved by increasing the OSR, for a given modulator and clock source. But, if the out of band gain of NTF is high, the jitter due to noise shaping behavior of ΣΔM will be dominant, and for improving SNR one can increase the quantizer levels; also σ_H (the RMS value of the transfer function $NTF(z)(1-z^{-1})$) can be decreased by reducing the aggressiveness of the noise shaping or optimizing the shape of NTF. So, although increasing the out-of-band gain (OBG) of NTF results in a lower in-band quantization noise, but it results in large jitter. Also, it is interesting that the second term of SNR is inversely proportional to the oversampling ratio. So, if we want to optimize the total jitter-induced noise power by changing the OSR, it is necessary to know first which part of the noise power is dominant.

So, the most critical clock-jitter errors in a CT-ΣΔ modulator are those generated at the feedback path through the outermost DAC [61], and the challenge is to decrease the jitter error due to out-of-band quantization noise and high frequency blockers without demanding very low phase noise clock generator.

2.3.3 Out-Of-Band blocker effect in CT-ΣΔ

Moving analog to digital converter toward antenna makes the ADC more complex, and the ADC should be more robust to unwanted signals. Without filtering in receiver front-end, unwanted signals (particularly adjacent channel and alternate channel) propagate through the receiver chain without adequate suppression and hence show up at the ADC input. Moreover, strong out-of-band (OOB) blockers can saturate/overload the ADC building-blocks, degrade the quality of the analog to digital conversion (e.g., due to distortion, insufficient anti-aliasing, and folding OOB noise back over the desired band), and degrade the ADC dynamic-range (DR) [60].

The strength of OOB blocker suppression at a given blocker frequency varies according to the magnitude of STF. Owing to the higher OOB attenuation offered by feedback structure of CT-ΣΔ modulators, large OOB blocking power appearing at the quantizer input can be adequately suppressed and become comparable to the maximum input of the desired channel or even much weaker when they appear at the output of the modulator.

The OOB blocker's most significant effect is on first integrator's output. If slewing happens at the integrator output, the combined waveform including the desired in-band signal and the OOB blockers will experience hard nonlinearity due to nonlinear settling. This will give rise to substantial distortion at the modulator output as well as dramatic increase in the noise floor due to noise. The problem of increased SR requirements caused by OOB blockers is relaxed in later integrators as later stages are shaped by previous ones, also the OOB signals are attenuated as they propagate in the loop filter chain [60].

As shown in Eq. 2.12, the effect of blocker in jitter induced noise is notable. Assuming the modulator output and the clock-jitter are statistically independent of

each other and the clock-jitter is a stationary white process, the integrated in-band jitter-induced noise power (IBJN) due to the blocker $x_{Blocker}(t) = A_B.cos(\omega_B t)$ in CT-ΣΔ with NRZ DAC is given by [60]:

$$\sigma^2_{e_{j,Blocker}} = 8.OSR.BW^2.\sigma^2_{j,rms}.A^2_B.|STF(j\omega_B)|^2.sin^2(\omega_B.\frac{T_s}{2}) \tag{2.15}$$

The blocker induced IBJN depends on the power of the blocker component in the feedback signal, determined by the product $A^2_{BLK}.|STF(j\omega_B)|^2$. The dependence of the blocker induced IBJN on the blocker frequency is twofold. First, for a given blocker level at the modulator input, the amplitude of the blocker component in the feedback depends on the value of the STF magnitude response at the blocker frequency , $|STF(j\omega_B)|$. Second, the term $sin^2(\omega_{BLK}.\frac{T_s}{2})$ depends on the frequency of the blocker tone, ω_{BLK} .

2.4 Literature review for CT-ΣΔ issues

2.4.1 State of the art solutions for low noise, low power CT-ΣΔ ADC

The theoretical Signal-to-Quantization Noise Ratio (SQNR) of the L-th order modulator, with an N-bit quantizer and oversampling ratio of OSR is shown in Eq. 2.5. In order to increase the SQNR, we can increase the order of the modulator (L), but higher order modulators are more difficult to stabilize, so usually the order of the system is limited to five. The Out of Band Gain (OBG) of higher order filter is significant and it causes instability because of overloading quantizer.

By increasing the OSR, the SQNR improves, and it relaxes the front-end filter. Designing a filter with relaxed transient band is more power and area efficient. However, if the Band-Width (BW) is kept constant, the maximum frequency is usually limited by technology, and operation in higher speeds leads to high power dissipation.

Moreover, designing the decimation filter with high frequency causes some challenges in digital circuit design.

The other parameter to increase the SQNR is quantizer resolution (N). By increasing N, the quantization noise decreases and therefore, the SQNR will increase. However, the power and area of the quantizer are proportional to the number of bits and higher number of bits in the quantizer requires more stringent requirements on the DAC elements in the feedback path. A flash ADC is a popular candidate for CT-$\Sigma\Delta$ due to its small delay but it is not suitable for high resolution quantizer because power and area increase 4 times by increasing each bit of the quantizer.

A higher value for OBG tends to push more of the quantization noise from signal band to higher frequencies, but on the other hand it causes the system to be sensitive to clock jitter and become unstable due to the reduction in the maximum stable amplitude. Lee's rule states that $OBG < 2$ should yield a stable modulator with a binary quantizer [62].

Another way to improve CT-$\Sigma\Delta$ modulator's performance in terms of quantization noise is using cascaded or MASH structure [42], [64]. The original idea of noise canceling technique using cascaded structures was proposed in [43] by using one bit quantizer in loop. A 2-stage MASH is shown in Fig. 2.8. In a cascaded converter, the quantization errors in each stage are processed in the following stage and output of the stages are digitally processed to cancel the quantization errors of all stages except the last one as shown in Eq. 2.16:

$$V1 = STF1.X + NTF1.E1 \tag{2.16a}$$

$$V2 = STF2.E1 + NTF2.E2 \tag{2.16b}$$

$$Y = V1.H1 - V2.H2 \tag{2.16c}$$

$$Y = X.STF1.H1 + E1(NTF1.H1 - STF2.H2) + E2.NTF2.H2 \qquad (2.16d)$$

As shown in Eq. 2.17, if $NTF1.H1 = STF2.H2$, the quantization noise of first stage is canceled and the output will have just the quantization noise of second stage (E2). So, without degrading the modulator stability the quantization noise is decreased.

$$NTF1.H1 = STF2.H2 \Longrightarrow Y = X.STF1.H1 + E2.NTF2.H2 \qquad (2.17)$$

However, the matching of digital filter with analog loop filter is essential for geting the best performance of ADC without leakage of quantization errors of previous stages. Moreover, MASH structure usually needs extra loops which needs extra filter, quantizer and DACs.

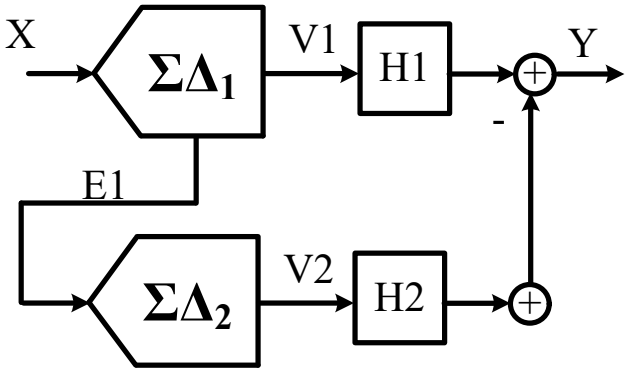


Figure 2.8: 2-stage MASH

For example [7] proposes a cascaded CT-$\Sigma\Delta$ modulator, in which 5-bit flash ADC is cascaded with a four stage 12-bit pipeleine ADC to reduce the in-band quantization noise. The flash ADC is in feedback loop with low resolution and the pipeline ADC is out of the loop so its latency does not affect the whole stability.

2.4.2 State of the art solutions for ELD compensation in CT-ΣΔ ADC

In literature, there are several ways to compensate excess loop delay [39]. In presence of ELD, for the case of RZ DAC, the DT-CT scaling factors are modified to match the original z-domain transfer function. For NRZ DAC which the pulse exceeds the sampling instant, some different way is proposed to compensate the ELD. [13] introduces one extra auxiliary Half-delay Return-Zero DAC (HRZ) which is delayed to next clock cycle the same as feedback pulse of main DAC, so the output is half delayed RZ DAC (also it can be fed-back to any integrator), and new scaling coefficient can be calculated by matching the converted DT transfer function with original ideal one. The simplest and classical ELD compensation technique is the insertion of an additional feedback path around quantizer [4], [39], which is shown in Fig. 2.9. This method is becoming the most popular way to make

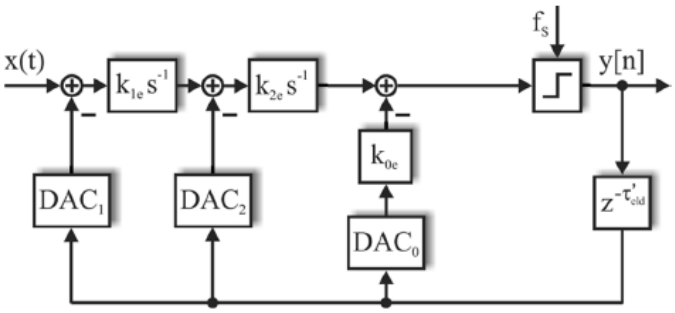


Figure 2.9: Insertion of an additional feedback path around quantizer to compensate ELD [39]

the modulator to be tolerant to one period of ELD. However, the method needs one more DAC and also power hungry summing amplifier. By adding extra path around quantizer (specially in presence of high integrator gain variation), the [13]

shows that even the robustness of the modulator improves, and the feasibly measure of robustness is proposed as a filter gain margin in [81]. According to [52], the tolerable loop delay decreases with higher amplitude and NRZ feedback, so higher order modulators are more sensitive to excess loop delay and they are more prone to instability (because of increasing the order of modulator by one). [54] proposed ELD compensating by adding $e^{s\tau}$ after filter, they assume that input is piecewise constant and just considering output as a sampled data, equations $\frac{e^{s\tau}}{s}$, $\frac{e^{s\tau}}{s^2}$ and ... are approximated with their expanded and truncated values, so the coefficients are scaled based on new parameters. [23] proposes ELD compensation using a predictive comparator. In this method they change the input reference voltage of comparator based on derivative of loop filter output, so they force the comparator output to have an early decision (with adaptive control, based on the sign-LMS algorithm). Almost similar method is used by [85], they proposed switching matrix with simple control logic for ELD compensation. This technique avoids the use of a power-hungry signal adder and the extra feedback, based on output sign the reference voltage of quantizer will be changed. Moreover, a digital ELD compensation method is proposed by [25], which is similar to classical compensation but the auxilary path is shifted after quantizer. In this method, the analog summing amplifier and the additional DAC are replaced by a register and digital adders (Fig. 2.10). However this method requires to increase the DAC resolution in order to fully restore the performance. Also, the STF will have large peaking due to non-touching path in the loop. ELD compensation using a PI-Element is proposed by [71] and used in [35]. It combines two inner loops of the classical compensation to one single proportional-integrating element (PI-element). A resistor in series with a capacitor can be used as a feedback element in last Operational Amplifier (OpAmp). In this technique, the STF will be affected because the feedback path is removed and added as a

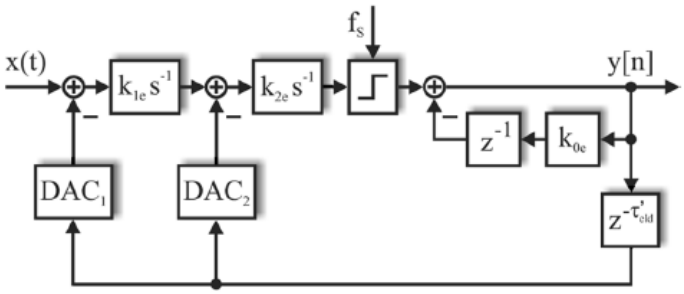


Figure 2.10: Insertion of auxiliary digital path after quantizer [39]

feedforward path. Another compensation is analog compensation which is proposed by [66, 67, 80]. In this method the compensation loop is placed around sample and hold by bypassing the Flash ADC. Using this technique, ELD of more than one clock cycle can be compensated with a small loss in resolution. Basically this technique add feedback loop around sample and hold instead of whole quantizer. This technique requires one extra DAC and summing amplifier and also changes the STF.

Another method which is proposed by [47] and [74] is using digital differentiation, which is shown in Fig. 2.11.

In this method the ELD compensation path moved from the output of the last integrator to its input. In return, the DAC output signal must be differentiated before being integrated. In this method if ELD is larger than sampling period it can not be compensated with simple proportional gain. This technique avoid the summing amplifier at the expense of one register (since DAC2 and DAC3 may be combined to one single DAC whose current is scaled) and maybe one extra DAC.

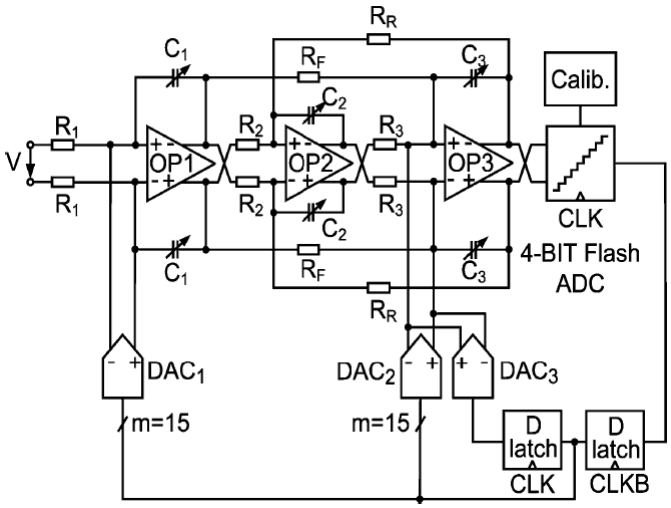


Figure 2.11: Using digital differentiation to compensate ELD [47]

2.4.3 State of the art solutions for clock jitter problem in CT-ΣΔ ADC

In literature, some techniques are proposed to degrade the jitter effect in CT-ΔΣ. Non-Return-to-Zero(NRZ) DAC waveforms are known to be robust to jitter effect in comparison with RZ DAC, due to one transition in each cycle. In RZ-DAC, uncertainty in clock timing affects the rising and falling transition of clock signal [14], so it is more sensitive to jitter error. [51] claimed to have improvement of 14dB for NRZ DAC. Some papers are using Finite Impulse Response DAC (FIR-DAC) feedback to reduce the sensitivity of CT-ΔΣ to jitter [19, 44, 51, 56, 63] which is shown in Fig. 2.12. They propose to generate multilevel DAC signal while using 1Bit quantizer. DAC response extends over multiple clock cycles, so the clock jitter effect is averaged [9]. [56] claimed to reduce the noise floor due to clock jitter by 18dB using FIR filter. However, the FIR filter introduces excess loop delay, and the loop will need an extra path to compensate the FIR filter delay and make the system stable which will increase both power and area. [63] has proposed a method

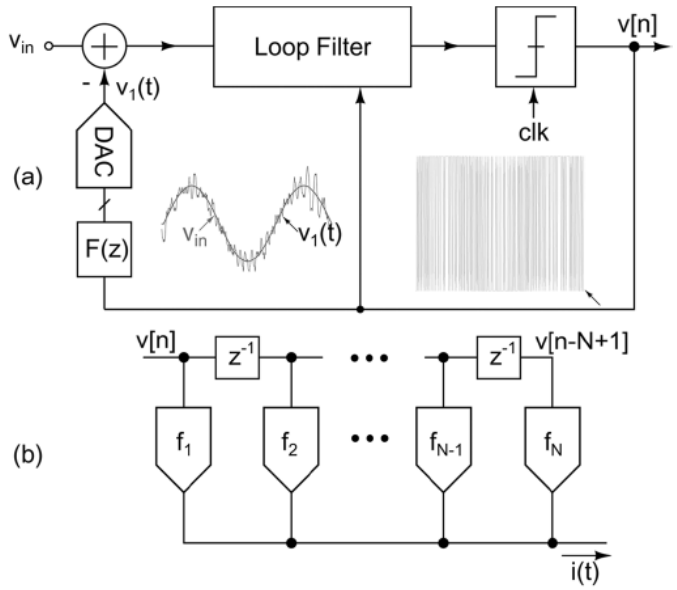


Figure 2.12: Using FIR-DAC to reduce sensitivity to jitter [63]

to compensate the delay introduced by FIR DAC and [16] suggests CT-$\Delta\Sigma$ with PWM and a FIR-DAC in the feedback path. The idea is to convert the output of multi-bit quantizer to a single bit PWM signal, then the PWM signal is fed back to input through FIR filter.

Some other techniques are proposed to elaborate on the shape of the DAC signal to decrease the effect of jitter which are shown in Fig. 2.13. Ortmanns, et al [53] propose using SCR (Switched-Capacitor-Resistor) feedback which is used in DT modulators. Instead of having the traditional rectangular signal as a feedback, an exponentially decreasing feedback is generated. Hence, at time of the clock transition, almost all charge has been transferred to the integrator outputs and clock jitter causes little error. The more recent works on SC feedback are done by [18] and [50]. [18] propose Dual-Switched-Capacitor-Resistor(DSCR) to improve jitter performance of CT-$\Delta\Sigma$. The idea of DSCR is to divide the exponential feedback pulse into several

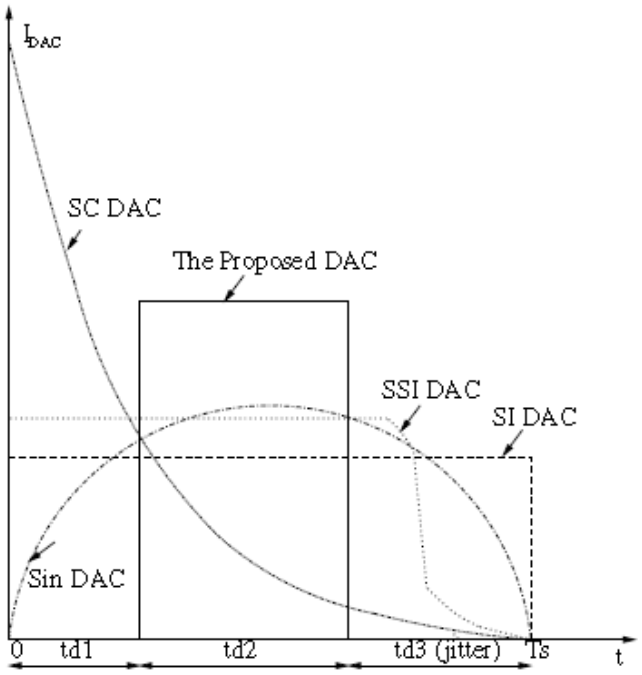


Figure 2.13: Different DAC shapes to reduce clock jitter effect [9]

identical unit pulses in order to alleviate the slew-rate requirement of OpAmp. In SCR and DSCR methods the first integrator needs high slew-rate and high GBW which will increase the power drastically. Some other pulse shaping techniques are SSI (Switched-Shaped-Current) [83], and sin-shaped DAC feedback [45], [41]. In SSI technique instead of generating an exponentially decreasing feedback waveform over the whole clock period as in SC or SCR feedback, a rectangular pulse is used in most of the clock period, and then feedback is exponentially decreased in the rest of the clock period. In order to generate such signal the method is benefited from the behavior of transistor in saturation and triode region. However, synthesis of a modulator with pulse shaped techniques are complicated. In sin-shaped DAC feedback, clock transition takes place when the sin-shaped feedback is at its minimum slope, so it will reduce charge error. The circuit complexity and thermal noise over-

head of some of these techniques prevent their adoption in high-resolution low-cost applications. [9] and [33] propose clock control methods to decrease jitter effect in Switched Current DACs. The idea is to generate delayed version of RZ rectangular DAC feedback. In this technique, RZ time period and active DAC feedback time is fixed by delay elements, but the problem is that the delay elements are PVT variant.

3. GRADIENT DESCENT BASED CALIBRATION FOR MASH 3-0 SIGMA-DELTA MODULATOR

3.1 Introduction

The Analog-to-Digital Converter (ADC) is an essential building block in most consumer electronics products. Oversampling ADCs trade digital signal processing and clock frequency for relaxed analog circuits, and among many data converters, CT-$\Sigma\Delta$ ADC is one of the most suitable candidates for high-speed, high-resolution and low power applications. Recently, the applications of CT-$\Sigma\Delta$ are continuously growing and covering areas such as wireless front-end [36], [20], imaging [27] and advanced Long Term Evolution (LTE) standards [22], [3]. Although CT-$\Sigma\Delta$ is well known for achieving higher resolution in comparison with other ADC architectures, still there are many challenges to improve its performance.

Increasing the Signal-to-Quantization Noise Ratio (SQNR) of the modulator always has been a challenging issue. Increasing order of the modulator, oversampling ratio, and the quantizer/DAC resolution are well known approaches to improve the SQNR. But increasing those parameters contradict with some system performances such as loop stability, bandwidth, power consumption and silicon area. Another way to improve SQNR in CT-$\Sigma\Delta$ modulator is cascaded or Multi-stage Noise SHaping (MASH) structure [42, 43, 64]. A major issue in a cascaded converter is maintaining good matching between digital compensating transfer function and process-temperature-voltage (PVT) sensitive analog loop filter.

As explained before, another challenge in CT-$\Sigma\Delta$ is loop sensitivity to Excess Loop Delay (ELD) [1, 52, 54, 66, 67, 80]. This issue is becoming more relevant nowadays, as the switching frequency increases to accommodate wider standards such as

LTE with aggregated channels. The classical ELD compensation technique is the insertion of an additional feedback path around quantizer that dominates loop performance at high frequency as well as system stability [4], [39]. However, the method needs an additional DAC and a power hungry summing amplifier that must be functional at clock rate. Another method uses digital differentiation after DAC [47], [74]. This technique avoids the use of an extra summing amplifier at the expense of one extra DAC that stresses the operational amplifier and can introduce extra delay that jeopardizes loop stability [74].

A key contribution of this chapter is the use of a modulator with an embedded 7-bit quantizer. The 3 most significant bits (MSB) of quantizer are used in feedback loop so it relaxes the main DAC linearity requirement and it saves power and area [6]. On the other hand, all 7-bits are used to mimic the operation of a MASH $\Sigma\Delta$ modulator, so theoretically the over all quantization noise level will be competitive with a CT-$\Sigma\Delta$ with 7 bit quantizer. The adaptive Gradient Decent (GD) method is used to extract the analog loop gain transfer function of cascaded CT-$\Sigma\Delta$ and improve the modulator performance. The proposed method adaptively adjusts the digital FIR filter coefficients to decrease the rms of the quantization noise at output of the cascaded modulator. The feasibility of these techniques are experimentally verified in a prototype achieving SNDR of 51dB before calibration and SNDR of 60dB after the proposed calibration scheme is employed.

The ELD compensation is implemented through a current based differentiator which is applied after fast DAC and does not need any extra DAC nor a dedicated summing amplifier. The use of analog differentiator makes the circuit more tolerant to ELD, so it does not significantly affect loop stability. Further, in order to decrease power consumption, a linear class AB amplifier is used which can handle large current to improve fast path slew rate.

This chapter is organized as follows. Section 3.2 describes the system level architecture of the modulator. The circuit implementation of different blocks are presented in Section 4.3. Section 3.4 demonstrates the Gradient Descent based post-processing methods, and Section 3.5 shows modulator realization and measurement results. Finally, Section 4.5 concludes the chapter and compare the chip prototype with the state of the art designs.

3.2 System Architecture

3.2.1 Transfer function and stability

The proposed CT-ΣΔ modulator architecture is shown in Fig. 3.1, and its specification and expected performance from system level design are given in Table 3.1 .

The prototype was designed with limited performance (on purpose) to make the quantization the dominant source of noise. The modulator comprises a 7-bit internal quantizer, which only 3 bits are in ΣΔ loop, operating at 300 MHz, and a third-order single-loop filter. Peak gain of noise transfer function is set to 5.3 dB. The third-order loop filter is realized as an active-RC topology due to its high linearity and large signal swing. Quantizer and DAC's excess loop delays are compensated using

Table 3.1: System level specification

Design Parameters	**Specification**
Sampling Frequency	300 MHz
OSR	10
Main feedback DAC	3-Bit
CT-ΣΔ loop order	3
Expected SQNR of 3-bit (-2 dBFS)	51 dB
Expected Signal to thermal noise of 3-bit (-2 dBFS)	75 dB
Expected SNDR after cancellation (-2 dBFS)	70 dB
Expected total power consumption	8.5 mW

fast path compressed by analog differentiator. The summing amplifier is combined with loop filter's last stage to decrease the number of amplifiers and save power, so the last integrator is used to add low-pass and band-pass outputs while completing the loop doing integration for the fast path.

The filter coefficients are chosen based on thermal noise, filter's node saturation (specially band pass output [26]) and feedback factor of summing amplifier. In order to increase SNR, the input resistor (R_{in}) and input full scale voltage (V_{FS}) are scaled up by 2; the passive component's values are given in Table 3.2. Input referred noise of filter is computed as shown in Eq.4.6:

$$V^2_{n,in,total} = [I^2_{n,DAC}R^2_{in} + V^2_{n,R_{in}} + (\frac{1}{A_{lp}Q})^2 V^2_{n,R_Q} + (\frac{1}{A_{lp}})^2 V^2_{n,R_F} + (\frac{1}{A_{lp}Q} + \tau_1 s)^2 V^2_{n,R_L} + (1 + \frac{1}{A_{lp}Q} + \tau_1 s)^2 V^2_{n,G_{m1}} + (\frac{1}{H_{LP}} + \frac{1}{A_{lp}}(\frac{1}{Q} - 1)\tau_1 s)^2 V^2_{n,G_{m2}}]BW \quad (3.1)$$

where, $V_{n,X}$ and $I_{n,X}$, are rms noise voltage and current of component X, respectively. H_{LP} is transfer function from input to low-pass output of filter. $A_{lp} = R_F/0.5R_{in}$, $Q = R_Q/R_F$, and $\tau_1 = R_{in}C_1$ are low-pass gain and quality factor of biquad filter and time constant of first integrator, respectively. The noise current of DAC is approximately equal to $I^2_{n,DAC} \simeq 4KT\gamma(g_m cs + g_m b) \times 2$, where $g_m cs$ is transconductance of all DAC current sources, and $g_m b$ is transconductance of bias currents of DAC. At low frequencies dominant noise sources are due to R_{in}, G_{m1} and main path DAC, $I_{n,DAC}$, which the rms noise contribution of them are about 4 nV/rHz, 6.5 nV/rHz, and 6.3 nV/rHz respectively, so the noise is dominated by quantization noise. As the noise contribution of other components are reduced due to the voltage gain of previous stages, their contribution are minimum.

In order to compensate for process variations, capacitor bank is used which covers ±18% with 3-bit programmability, so the RC time constant variations are minimized.

Table 3.2: Passive element values

R_{IN}	R_Q	R_F	R_L	R_{lp}	R_t	C_1	C_2	C_f
1KΩ	5.4KΩ	1.8KΩ	1.8KΩ	41.5KΩ	1MΩ	5.6pF	5.6pF	0.2pF

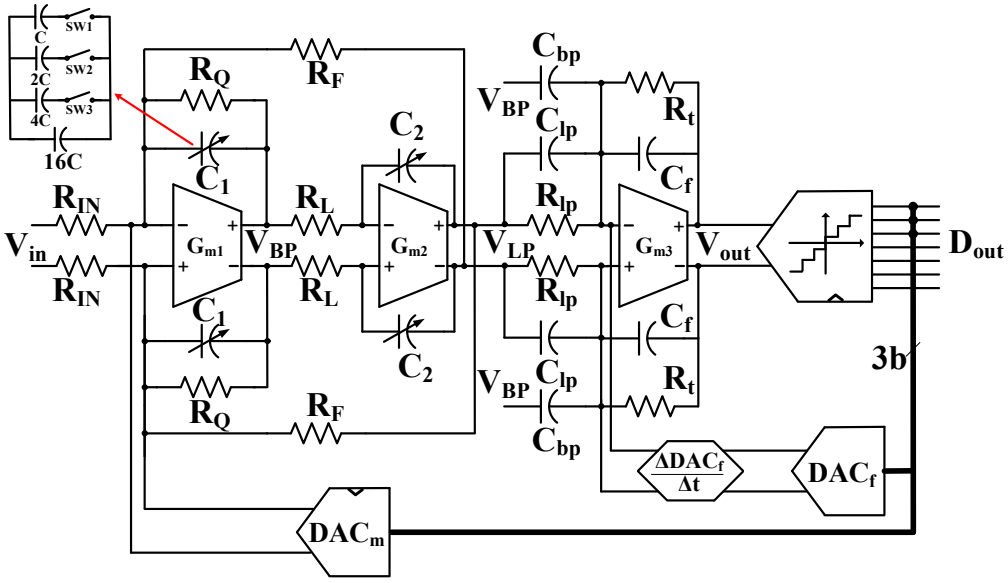


Figure 3.1: Proposed continuous-time Sigma-Delta modulator

3.2.2 Quantization noise reduction technique using a high resolution quantizer

Fig. 3.2 shows the proposed technique for reducing the quantization noise. The

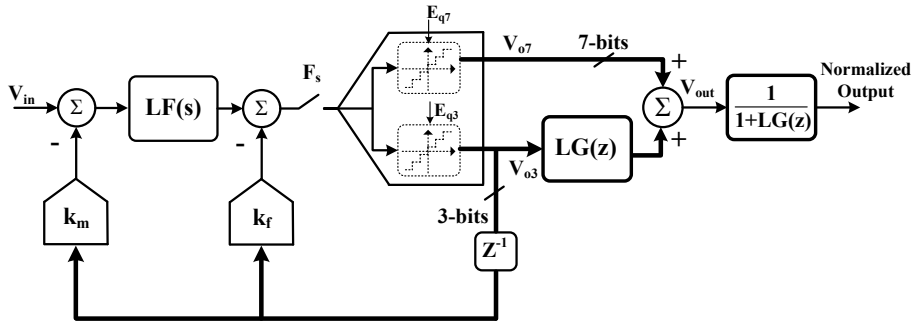


Figure 3.2: Block diagram of the proposed noise reduction technique

output of the 3-MSB of quantizer is fed-back into the loop and the whole 7-bit digital output is used for noise reduction. The 3 most significant bits (V_{o3}) are filtered by the digital filter (LG(z)) which is ideally equal to the analog loop gain ($LG(s)$), and then the result is combined with the output of 7-bit quantizer (V_{o7}). Ignoring the effect of the sample and hold circuit at the input of the quantizers, conventional analysis shows that:

$$V_{o3} = \frac{LF(s)}{1+LG(s)}(V_{in}+V_{th}) + \frac{1}{1+LG(s)}E_{q3} \tag{3.2}$$

$$V_{o7} = \frac{LF(s)}{1+LG(s)}(V_{in}+V_{th}) - \frac{LG(s)}{1+LG(s)}E_{q3} + E_{q7} \tag{3.3}$$

$$V_{out} = \frac{1+LG(z)}{1+LG(s)}LF(s).(V_{in}+V_{th}) + \frac{LG(z)-LG(s)}{1+LG(s)}E_{q3} + E_{q7} \tag{3.4}$$

In this equation, $LF(s)$ is the loop filter's transfer function, and V_{th} is thermal noise. According to Eq. 3.4 if digital gain, $LG(z)$, matches with analog loop gain,

$LG(s)$ within the desired bandwidth, the quantization noise of 3-bit loop quantizer is canceled, and just the quantization noise of the 7-bit quantizer will affect the output signal, which is much smaller than the quantization noise of 3 bit quantizer; the final result is shown in Eq. 3.5.

$$V_{out} = LF(s)(V_{in} + V_{th}) + E_{q7} \tag{3.5}$$

And, normalizing the Eq. 3.5 to loop gain $(1 + LG(s))$, The output will be as:

$$V_{out}|_{normal} = STF(s).(V_{in} + V_{th}) + NTF(s).E_{q7} \tag{3.6}$$

Ideally, improvement due to quantization noise cancellation technique is equal to difference between feedback (3-bit) and whole resolution of quantizer (7-bit). A common issue in cascaded $\Sigma\Delta$ converter architectures is that inband $LG(s)$ must accurately match with $LG(z)$ in order to reduce quantizer noise of the low resolution in-loop quantizer. Errors in the analog circuitry cause the actual $LG(s)$ of the modulator to deviate from the desired transfer function and then limits the benefits of MASH approach, causing leakage of E_{q3} into the combined output of the cascaded modulator. In this thesis we used Gradient Decent method to match the digital loop gain with analog counterpart.

3.3 Circuit implementation

3.3.1 Linear class AB amplifier

One of the challenges in $\Sigma\Delta$-ADC design is to make it power efficient. In literature, several methods are proposed to decrease the power consumption of the loop filter [84], [82]. Folded-cascode and multi-stage amplification techniques are the most popular ones for low voltage design. However, in a CT-$\Sigma\Delta$ loop filter composed of

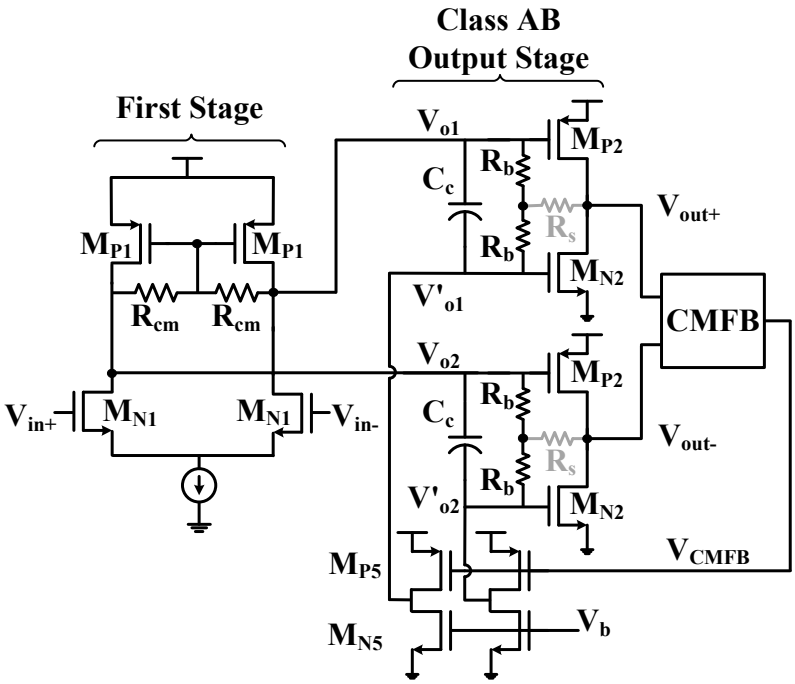


Figure 3.3: Class-AB amplifier schematic

the active RC integrators, the resistive load makes the folded-cascode OpAmp less efficient in terms of low frequency gain than the multi-stage amplifier. In this thesis, in order to save power, a two-stage amplifier with class-AB output stage is used to provide large output current with modest biasing current.

The two stage amplifier is shown in Fig. 3.3. First stage (M_{N1}, M_{P1}) is conventional differential pair and second stage is class AB amplifier composed by (M_{N2}, M_{P2}, R_b and R_s, C_c) with modified Monticelli [48] bias circuitry which increase second stage amplifier's linearity. Signals from V_{o1} to V'_{o1} are AC coupled by large capacitor C_c. Resistors R_b and control current generated by common-mode detector and transconductance amplifier (M_{N5}, M_{P5}) set the bias voltage for class-AB transistor, M_{N2}. The common mode feedback mechanism adjusts the V_{gs} of M_{N2} through voltage drop in R_b resistor to force the drain current of M_{P2} equal to the

bias current of M_{N2}. Ignoring the effect of R_s, the transfer function from V_{o1} to V'_{o1} is shown in Eq. 3.7.

$$\frac{V'_{o1}}{V_{o1}} \approx \frac{1 + (2R_bC_c)s}{1 + s(C_c + C_{gsN2})2R_b} \tag{3.7}$$

where in this design $R_b = 10K\Omega$, and $C_c = 3pF$. If $C_c \gg C_{gsN2}$ the frequency of the pole and zero pair will be very close to each other and V_{o1} and V'_{o1} will be almost identical. Considering the effect of the large feedback resistor R_s the low frequency gain of OTA will be as follows:

$$\frac{V_{out}}{V_{in}} = g_{m_{n1}}.R_{L1}.(g_{m_{n2}} + g_{m_{p2}}).R_{L2} \tag{3.8}$$

where, $R_{L1} = R_{cm}||R_{n1}||R_{p1}$ and $R_{L2} = R_L||R_{n2}||R_{p2}$ are first stage and second stage's load, respectively; R_L is load of the amplifier. The large resistor R_s provides shunt feedback to decrease the output impedance of second stage but at the same time reduces the low-frequency gain. Fig. 3.4, shows a two tone test for the filter's first stage which is a lossy integrator. The tones are placed at 10 MHz and 11 MHz and the rms value of the composed signal is -4 dBFS, and the third order inter-modulation is -64 dB. Although Rs reduces the loop gain, it prevents the class AB to suffer from significant cross over distortion.

Fully loaded, the total low frequency gain of the amplifier is 29dB, and using 1.2V power supply, the first stage and second stage's power consumptions are 0.27mW and 0.12mW, respectively. Table 3.3 shows the comparison of proposed class AB amplifier vs the conventional two-stage class A (miller amplifier) counterpart with the same gain-bandwidth product. According to this table, in order to have same GBW, class A amplifier needs almost twice current of class AB amplifier. Moreover, although

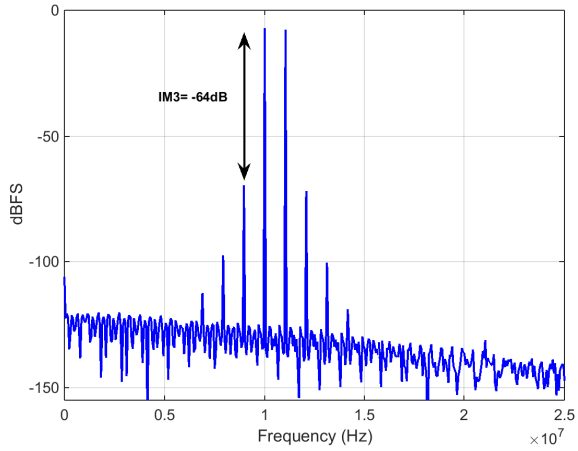


Figure 3.4: 2 tone test for linearity simulation of first lossy integrator with rms output amplitude of -4dBFS at 10MHz and 11MHz

small signal linearity are almost the same (demonstrating that cross-over distortion is not an issue in the class AB topology), the large signal IM3 of class AB amplifier is almost 10 dB smaller than the class A amplifier.

Table 3.3: Comparison of Class-AB vs Class-A output stage

	Class A	**Class AB**
GBW	2.36 GHz	2.4 GHz
power	0.83 mW	0.39 mW
noise	6.53 nV/rHz	6.59 nV/rHz
IM3, cross over distortion (RMS Vout = -20 dBFS)	-88 dBc	-92 dBc
IM3, large signal distortion (RMS Vout = -6 dBFS)	-67 dBc	-58 dBc

3.3.2 Mixed signal fast path employing analog differentiator

In this section we describe the fast path operation, and the way we increase ELD tolerance. Analog differentiator is proposed in order to avoid the use of power hungry summing amplifier and at the same time compensate excess loop delay without

compromising fast path performance, while we increase ELD tolerance.

The main concept relies on minimizing the use of delayed clocks and the use of a wide-band analog differentiator. The proposed continuous time differentiator is shown in Fig. 3.5, and the fast path circuit parameters are displayed in Table 3.4. Feedback DAC output current I_{dac}, is converted to voltage by resistor R_b and

Table 3.4: Differentiator circuit parameters

$g_{m_{M2}}$	C_d	C_f	R_b	C_p	τ_1	τ_2
4.2m℧	0.27pF	0.2pF	350Ω	20fF	7ps	120ps

then fed to capacitive degenerated differential pair M_{N2}. DAC current signal is then indirectly differentiated on capacitors $2C_d$. Capacitor C_f along with an OTA G_{m3} integrates the output current of differentiator and generates a zero order path around quantizer. Overall, the fast path operates as a broadband amplifiers with half delay required by the quantizer. The input to differentiator is NRZ DAC's output with an equivalent trans-impedance gain of R_{dac}. Differentiator input is then characterized as:

$$V_{idiff}(s) = \frac{R_b}{R_b C_p s + 1} I_{dac}(s) \tag{3.9}$$

Transistor M_{N2} with capacitor of $2C_d$ form a source degenerated circuit which provides the required differentiation operation. Ignoring the effect of the transistor output resistance, the output current of differentiator is described as:

$$i_{diff}(s) = \frac{2C_d s}{\frac{2C_d}{g_m} s + 1} V_{idiff}(s) \tag{3.10}$$

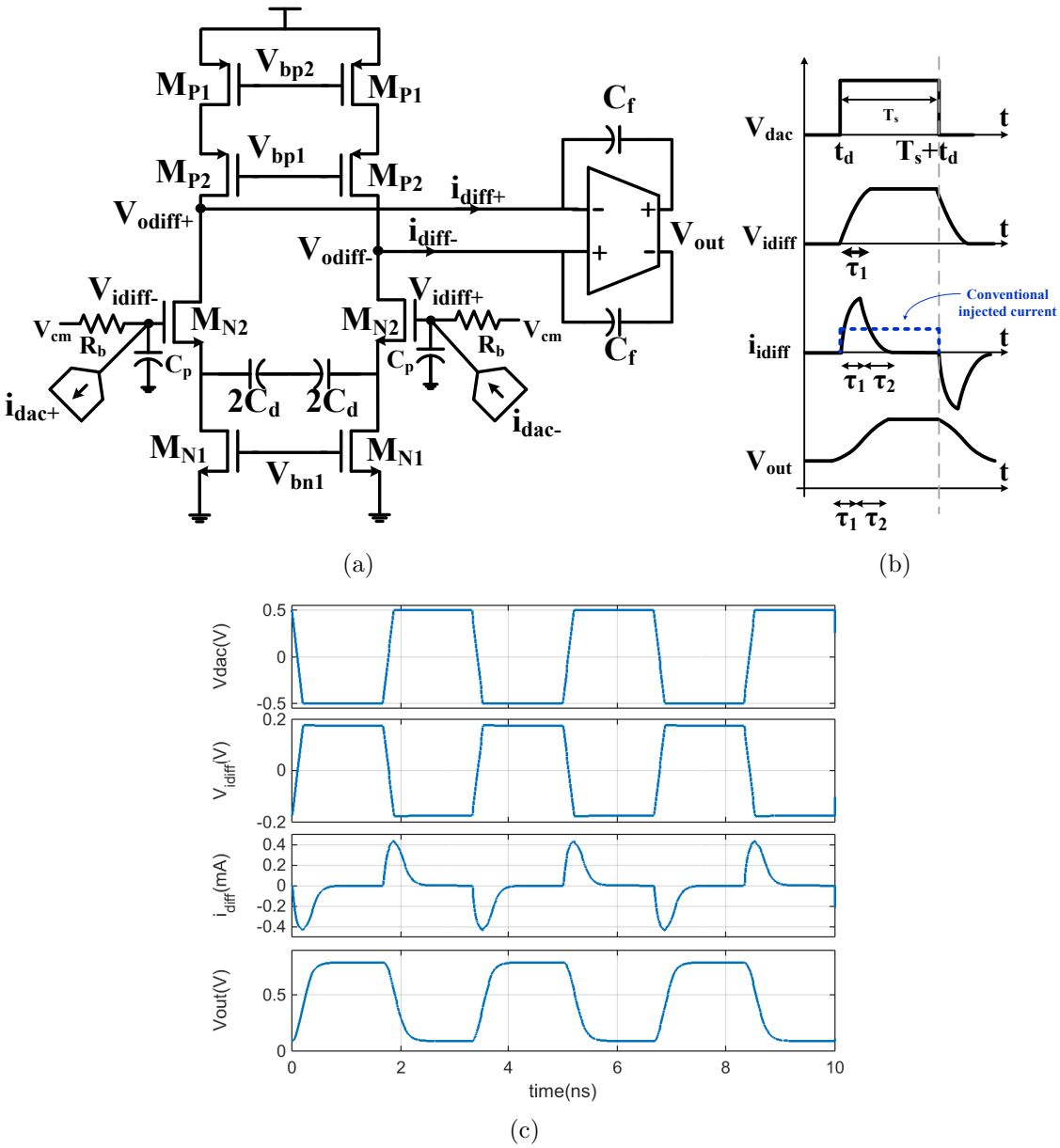


Figure 3.5: (a) Fast path and differentiator circuit (b) transient response of different nodes (c) schematic simulation

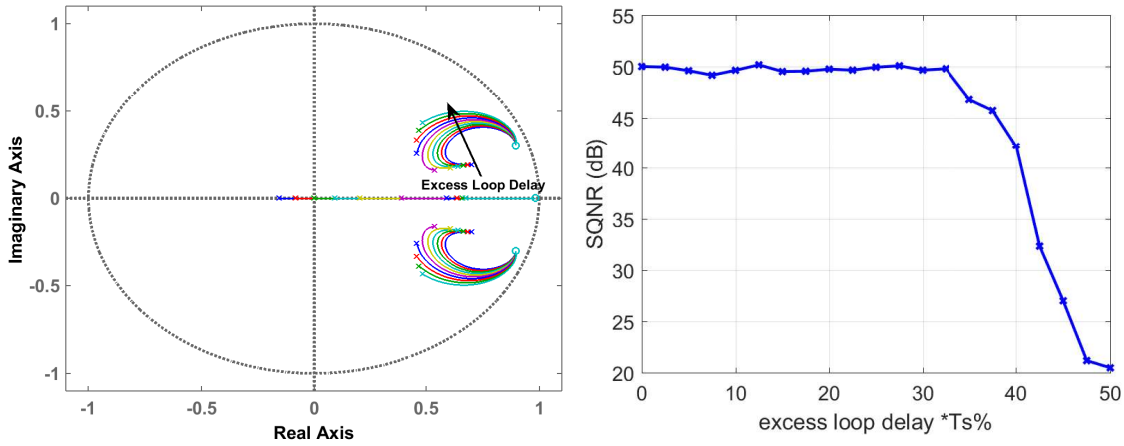
$$i_{diff}(t) = \begin{cases} \frac{-2R_bC_d}{\tau_2-\tau_1}(e^{-t/\tau_1} - e^{-t/\tau_2}).I_{DAC}, & \text{if } \tau_1 \neq \tau_2 = 2C_d/g_m \\ \frac{-2R_bC_d}{\tau^2}.te^{-t/\tau}.I_{DAC}, & \text{if } \tau_1 = \tau_2 = \tau \end{cases} \tag{3.11}$$

Passing $I_{diff}(t)$ through C_f, yields integration operation; the final output of integrator is obtained replacing $t = T_s/2$.

$$V_{out}(\frac{T_s}{2}) = \frac{1}{C_f}\int_0^{T_s/2} i_{diff}(t)dt = \frac{2R_bC_d.I_{DAC}}{C_f(\tau_2-\tau_1)}[\tau_1(e^{-T_s/2\tau_1}-1) - \tau_2(e^{-T_s/2\tau_2}-1)] \tag{3.12}$$

If $T_s \gg \tau_1,\ \tau_2$, then $V_{out}(T_s/2) \sim 2R_bI_{dac}C_d/C_f$, so the fast path is strong function of R_bI_{dac}. The concept is shown in Fig. 3.5(b) and the schematic simulation (Cadence) is shown in Fig. 3.5(c). According to the figures the differentiator's current settles in less than half of sampling period, which makes it more tolerant to ELD. As shown in Fig. 3.5(b), the settling time of differentiator circuit should be less than half period $4\tau_1 + 4\tau_2 < \frac{T_s}{2}$ to guarantee 98% or better voltage settling accuracy. Notice that the signal swing at M_{N2} gate should not be too large, otherwise the transistor might be pushed into triode region. To keep M_{N2} in saturation region, R_bI_{dac} is set to be 300 mV. Capacitor C_f (and accordingly $2C_d$) is related to the capacitor loading of OpAmp by feed-forward path in loop filter and there is enough design flexibility to choose its value. To make the modulator more tolerant to ELD, we need to decrease τ_1 and τ_2, which means decreasing R_b, C_p, C_d and increasing g_m; the trade off is additional power consumption.

The effect of excess loop delay in system performance is shown in Fig. 3.6 which is system level simulation which is done using Matlab/Simulink. Fig. 3.6(a) shows the Root-Locus of Noise Transfer Function (NTF(z)) with $0 - 100\%$ excess delay. The ELD is modeled as τ in $NTF(z) = \frac{1}{1+e^{-\tau s/T_s}LG(z)}$. According to Fig. 3.6(a) all



(a) (b)

Figure 3.6: Excess loop delay variation 0-100%T_s (a) root-locus of NTF(z) poles including mixed signal fast path (b) SNDR vs ELD variation

of the poles remain inside the unit circle which shows the system is very tolerant to loop delay variations. Moreover, Fig. 3.6(b) shows SNDR variation vs excess loop delay. The system's dynamic performance does not degrade up to 30% of sampling period excess delay.

3.3.3 7-Bit quantizer

In order to reduce power and area, a 7-bit quantizer is implemented using a modified version of the subranging ADC [6]. Only 3-bits are used in the ΣΔ-modulator loop, so it relaxes the DAC specifications and saves power; the extra 4 bits are used to implement the MASH 3-0 algorithm to increase the resolution of the ΣΔ-ADC. Fig. 3.7 shows the implemented quantizer, which consists of one MSB comparator, 7 passive sample and hold circuits, 7 bits coarse/fine comparators, and a MUX to select proper reference voltage; details can be found in [6]. During the first clock phase, and employing single sign comparator, the polarity of the input signal is detected and the MSB bit is then resolved. Next clock phase, the coarse 3 bits are extracted

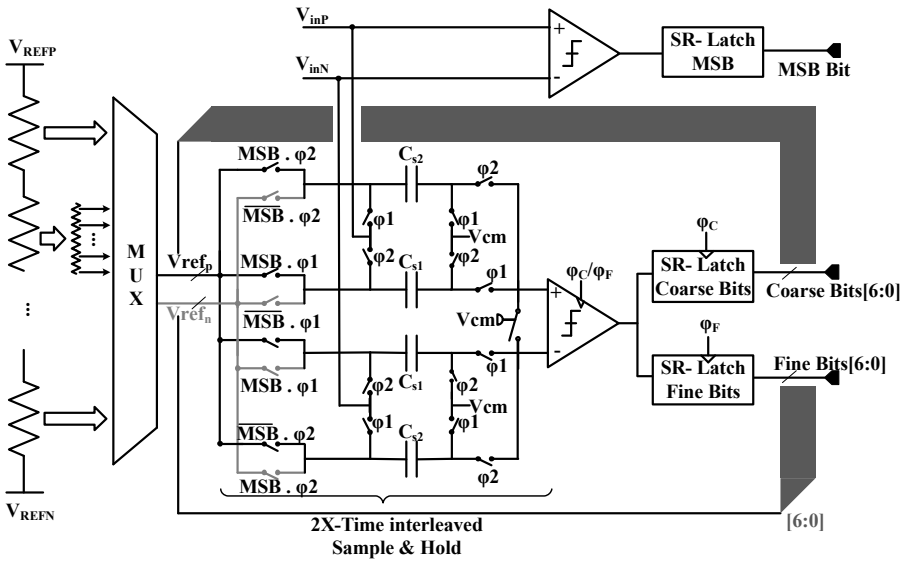


Figure 3.7: Simplified two step, 7 bit quantizer [6]

using 7 comparators, and during the third clock phase the fine 3-bits are obtained employing the same comparator just by switching the references to fine reference voltages. Digital logic is used to select the proper reference voltages. The output of quantizer are resolved in half clock cycle to give the fast DAC and summing amplifier enough time to settle.

3.3.4 Current steering DAC

The 3-bit main feedback DAC employs 7 cells of n-type cascoded current source M_1-M_2 and a pair of current-steering switches M_3-M_4 as shown in Fig. 3.8. Each current source cell M_1-M_2 is sized to carry a nominal current of 155.5 μA. With 1 $K\Omega$ of CT-$\Sigma\Delta$ modulator's input resistors, the equivalent fullscale differential input range is 1.2 V. The current-steering switches M_3-M_4 are designed to operate in saturation region to increase DAC output impedance. In addition, they are driven by a high-crossing switch driver [24].The drivers shift the control signal of the switch transistors so that these transistors never simultaneously turn off. This design choice minimizes

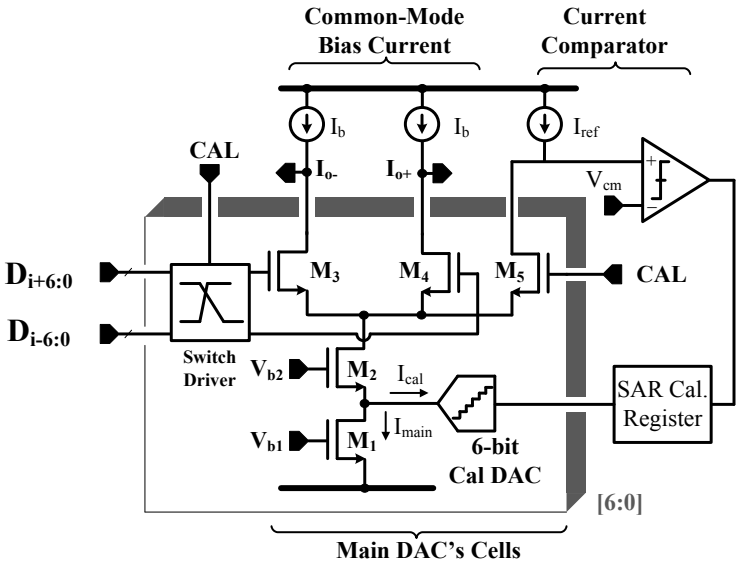


Figure 3.8: Simplified main DAC schematic highlighting unit current source cell with fully digital on-chip calibration circuitry.

feedthrough current from parasitic gate to drain capacitances C_{gd} of M_3-M_4. Fully digital on-chip calibration through a 6-bit calibration DAC is performed on power-up to reduce static mismatch of unit main DAC's current. Each unit current source has its own 6-bit calibration DAC. During calibration, the current-steering switches M_3-M_4 are turned off and the current I_{main} is routed through M_5 to be compared by a reference current I_{ref}. A comparator detects the result of this comparison and drives the successive approximation register (SAR) accordingly to get the best digital code such that $I_{main} + I_{cal}$ current value is the closest to I_{ref}; this process is repeated serially for all the 7 current cells.

3.4 Digital calibration

The proposed digital calibration method uses Gradient Descent (GD) methodology. In this section, first we revise the generic gradient descent algorithm and its relation with the Least Mean Squares (LMS) algorithm. Then, we discuss the

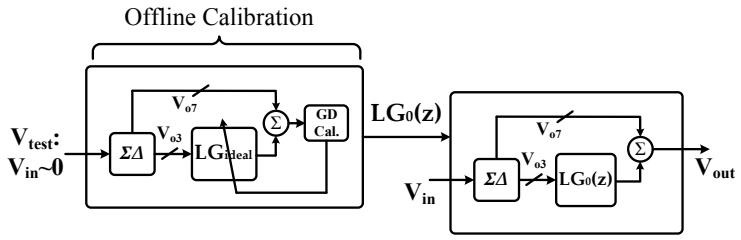


Figure 3.9: Different phases of proposed method

proposed offline calibration method (see Fig. 3.9). We discuss how the analog filter transfer function that matches the digital loop gain is extracted and also show how we use this transfer function to reduce quantization noise.

3.4.1 The generic gradient descent method

The Gradient Descent (GD) algorithm is used to find the local minimum of a function [5]. GD-based signal processing techniques increase the precision and reliability of analog circuits which are exposed to PVT variations and device non-linearities [8]. The GD algorithm employs steps proportional to the negative of the gradient at the current point of the function. It relies on the observation that a multi-variable function $F(x, y, z, ...)$ at point $x = x_0$ (keeping all other variables y, z, ... constant) decreases faster if one goes from $x = x_0$ in the direction of the negative gradient of $F(x, y, z, ...)$ at $x = x_0$, denoted by $-\nabla_x F(x_0) = -\frac{dF}{dx}|_{x_0}$. Starting from x_0, and considering the sequence x_0, x_1, x_2, ...such that $x_{n+1} = x_n - \gamma_n \nabla F(x_n)$ for $n \geq 0$ and sufficiently small $\gamma > 0$, it follows that:

$$F(x_0, y, z, ...) \geq F(x_1, y, z, ...) \geq F(x_2, y, z, ...) \geq \cdots \geq F(x_n, y, z, ...). \tag{3.13}$$

Hence, the sequence $F(x_n, y, z, ...)$ converges to the desired local minimum for the variable x, if exists. The same property applies to all other variables.

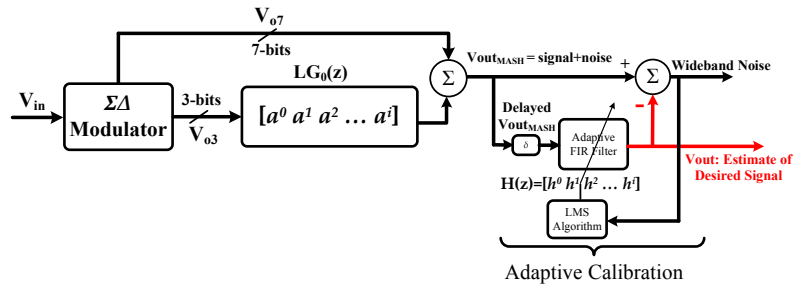
To compute the optimal coefficient of a linear FIR or IIR filter we apply the gradient descent method to the error function. However, in many applications, the true gradient of function $F(x, y, z, ...)$ cannot be determined. Thus, a practical implementation involves estimating the gradient from the available data using the Least-Mean-Squares (LMS) algorithm [29]. In other words, the LMS algorithm is a variant of the gradient descent method in which the mean square of the error is minimized. Fig. 3.10(a) shows a simplified version of the LMS-based adaptive noise cancellation technique used in $\Sigma\Delta$ modulator design before; more details can be found in [31, 32, 75–77]. The main advantages of the approach is that it can remove noise when the NTF is not available or process parameters variations due to temperature gradient or device aging change the NTF in a such way that it does not match the original NTF.

In this project, we use a modified version of the LMS algorithm which reduces the digital resources by combining cancellation filter $LG_0(z)$ and adaptive filter $H(z)$ in Fig. 3.10(a) into a single filter $LG(z)$ shown in Fig. 3.10(b). First, we show how the mean square of the error can be obtained in the frequency domain; this derivation is the rationale behind the proposed methodology.

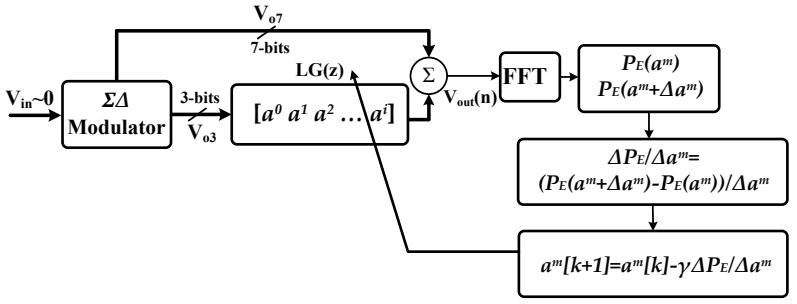
Consider a $\Sigma\Delta$M without the adaptive filter (Fig. 3.10(b)), the goal is to find the coefficients of $LG(z) = a^0 + a^1 z^{-1} + \ ... \ a^i z^{-1}$ (i is the number of taps used in the FIR filter) and to use the LMS algorithm to minimize the mean square of error:

$$LMS[e(n)] = \min_{a^i}\{\frac{1}{N}\sum_{k=0}^{N-1} e(n)^2\} \tag{3.14}$$

where, N is number of samples for LMS estimation, and $e(n) = V_{out}(n)|_{inband\ V_{in}=0}$ is the n^{th} discrete time quantization error; if inband input signal is zero, the output will be equal to the quantization error which is shown in Fig. 3.10(b). From the



(a)



(b)

Figure 3.10: Digital Calibration (a) LMS based adaptive noise cancellation technique [32, 77], (b) proposed FFT based Gradient Descent technique for offline phase

Parseval's Theorem, we know that $\sum_{k=0}^{N-1} e(n)^2 = \frac{1}{N}\sum_{0}^{N-1} E(\omega)^2$, where $E(\omega)$ is the Discrete Fourier Transform (DFT) of $e(n)$. Thus, in Eq. 3.14 we can replace the time-domain error with frequency-domain error (DFT of noise), leading to:

$$LMS[e(n)] = \min_{a^i}\{\frac{1}{N^2}\sum_{0}^{N-1} E(\omega)^2\} = \min_{a^i}\{\frac{1}{N^2}P_E\} \tag{3.15}$$

where P_E is the error power, and $min\{\cdot\}$ operator returns the minimum of its input argument. Thus, computing error power in frequency domain and minimizing it, is equivalent to minimizing the mean square error in time domain. So, we use an adjustable FIR filter to minimize the error function in the frequency domain.

3.4.2 Matching analog loop filter and digital filter

The first phase of the proposed method is to extract the analog filter transfer function. According to Eq. 3.4, when an input signal with a very low inband amplitude ($V_{in}^{inband} \simeq 0$) is applied at the modulator's input, the inband output will only be comprised of quantization noise of the 3-bit and 7-bit quantizers, as shown in Eq. 3.16.

$$V_{out} \simeq (1 + LG(z)).STF(s).V_{th,cal} + \frac{LG(z) - LG(s)}{1 + LG(s)}E_{q3} + E_{q7} \quad \textbf{if} \quad V_{in}^{inband} \simeq 0 \tag{3.16}$$

where E_{q3} and E_{q7} are quantization noise densities, and $V_{th,cal}$ is thermal noise during calibration. The aim of the calibration algorithm is to minimize Eq. 3.16. If thermal noise is minimum, and quantization noise is dominated by E_{q3}, minimization of Eq. 3.16 leads to matching between digital loop gain LG(z) and analog loop gain LG(s). The diagram for the post-processing phase is shown in Fig. 3.10(b). As seen in the figure, we pass the 3-bit output of $\Sigma\Delta$M through $LG(z)$ with FIR coefficients

of $[a^0 a^1 a^2 ... a^i]$ and add them with the 7-bit output of the $\Sigma\Delta$ modulator. Then we compute the FFT to extract the power of in-band noise (P_E) in the frequency domain and then use the GD algorithm to update the FIR filter coefficient to decrease the noise power. Note that P_E is computed by adding the power of all in-band bins resulting from the FFT of V_{out}.

Since there is no closed-form equation for the gradient of the noise power P_E with respect to the filter coefficients, we rely on numerical methods to compute it. To do so, for each filter coefficient a^i, we compute the noise power $P_E(a^i)$ and the perturbed noise power $P_E(a^i + \Delta a^i)$, where Δa^i is a small perturbation (typically an order of magnitude smaller than a^i) of the coefficient value. Therefore, we can numerically calculate the gradient of noise power with respect to filter weight:

$$\nabla_{a_k^i} P_E = \frac{dP_E(a)}{da}|_{a_k^i} \simeq \frac{P_E(a_k^i + \Delta a_k^i) - P_E(a_k^i)}{\Delta a_k^i} \tag{3.17}$$

Then, we use the GD method to update the FIR filter coefficients:

$$a_{k+1}^i = a_k^i + \gamma \nabla_{a_k^i} P_E \tag{3.18}$$

where γ is the step size and a_k^i is the i-th filter coefficient in the k-th iteration. The gamma value that we used for the simulations is 0.5. By using very small value of γ the system takes more iteration to converge and large value of γ increases the effect of derivation in Eq. 3.18 and it will deviate a lot from the coefficients previous value. We continue this process iteratively until filter weights converge, and the difference between consecutive weights falls bellow a suitably small threshold $\epsilon = a_k^i/100$ (i.e., $|a_k^i - a_{k-1}^i| < \epsilon$).

As a proof of concept, a third order SD modulator was designed and fabricated in

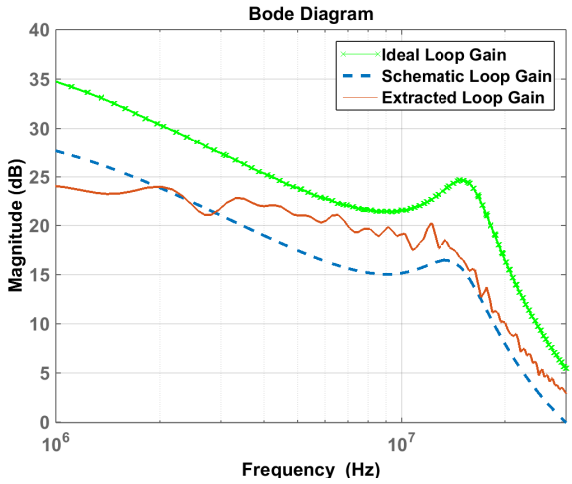


Figure 3.11: Ideal loop gain and loop gain from schematic versus extracted one

a mainstream CMOS technology; the details are fully described in the following sections. Figure 3.11 shows 1) the ideal loop gain (infinite gain amplifier) from Matlab, 2) the schematic level loop gain transfer function obtained from Cadence simulations, and 3) the experimental loop gain from the proposed matching algorithm. The initial values of 100 tap FIR filter coefficients are chosen based on the estimation of the ideal transfer function required for the calibration of the designed $\Sigma\Delta$ modulator. This steers the algorithm away from undesired local minima and reduces the convergence time. The estimated power consumption for the FIR filter is about 2.5mW [40] which can be decreased by 40% if it is implemented in polyphase structure [40]. Also if we use downsampling and decimation filter the frequency will decrease and as a result the dynamic power consumption will decrease. According to [40] the area estimation for 100tap FIR filter in $0.13\mu m$ technology is about $0.05mm^2$, which can be decrease further for very advanced CMOS technologies. According to Fig. 3.11, low frequency gain dropped from 35dB for the ideal case (Matlab model with infinite gain amplifiers) down to 28dB for loop gain extracted from the schematic (cadence)

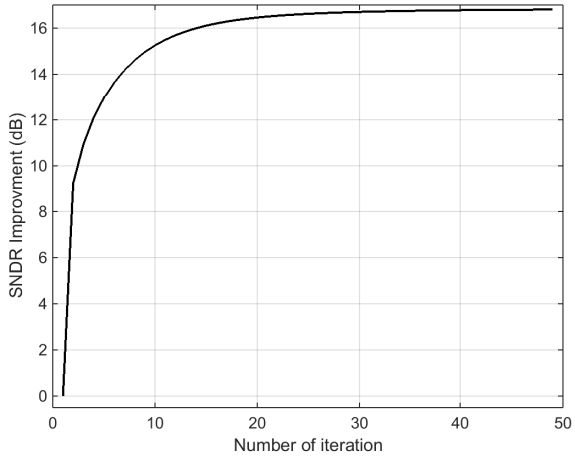


Figure 3.12: Settlement of algorithm after 50 iterations

simulation. The gain attenuation is the result of the limited gain of OTAs. The extracted one from the GD method follows the trend of schematic result except that the schematic result does show the dips and peaks.

Figure 3.12 shows the convergence of the algorithm, the algorithm settles after 20 iterations, and for the first several iterations the slope of SNDR improvements is very sharp.

When used in the cascade scheme, the extracted transfer function leads to 8-10 dB SNR improvement as a result of noise cancellation (offline calibration), whose results for 4MHz input with amplitude of -6 dBFS is shown in Fig. 3.13. The measured SNDR of 3-bit CT$\Sigma\Delta$M is 47 dB and after calibration it reaches 57 dB. As shown in Eq. 3.16, if there is significant thermal noise, the extracted transfer function is not going to match the analog transfer function and it will degrades the system performance.

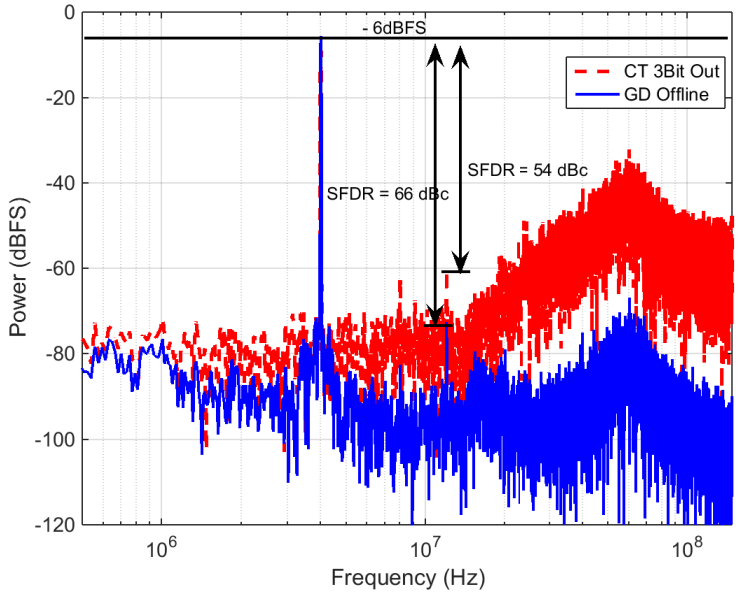


Figure 3.13: Experimental results: spectrum of the 3-bit output, and cancellation after convergence, input 4 MHz with amplitude of -6 dBFS

3.5 ADC realization

The CT-ΣΔM is fabricated in 130 nm IBM CMOS technology. Fig. 3.14 shows the die photograph; the active area of ADC is 1.1 mm^2 including clock generator and current mode logic (CML) buffers for measurement purpose. The modulator's power consumption is 8.5 mW, where dynamic and static power consumptions are 2.5 mW and 6 mW, respectively. The power and area distribution are shown in Fig. 3.15.

A passive 10 MHz band-pass and a 5 MHz low-pass filters were used during testing. The signal is converted from single-ended to differential with appropriate common-mode voltage using an on-board transformer (ADT1-6T). The clock signal is generated using PSG Vector Signal Generator (Agilant E8267D) and converted to square wave and differential signals on chip. The data streams were captured using a

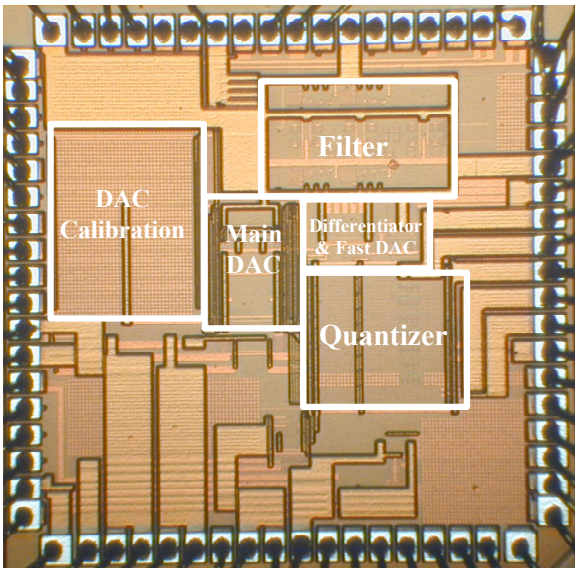


Figure 3.14: Die micrograph of chip, active area is $1.1mm^2$ including clock generator and CML buffers

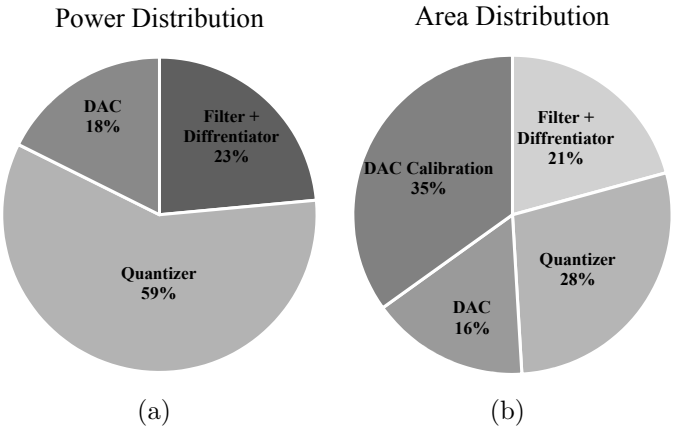


Figure 3.15: (a) Power distribution of modulator, overall power 8.5 mW, (b) area distribution of modulator, overall area 1.1 mm^2

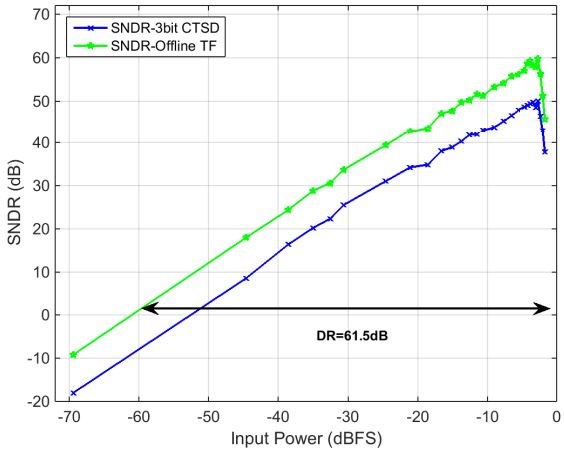


Figure 3.16: Experimental results: SNDR vs input power for 3-bit ΣΔ loop and output of the gradient descent algorithm (input frequency 4MHz)

Digital Signal Analyzer and then processed offline using Matlab/Simulink. 16K data points were used for spectral estimation and a Hann window was used to minimize spectral leakage effects.

The proposed offline FFT-based Gradient Descent algorithm was employed. The algorithm matches the digital loop gain with analog one. The offline process can be repeated during time slots available in the system to make the calibration less sensitive to PVT variations. Fig. 3.13 shows the spectrum of the modulator's output, before and after calibration, for input signal of -6 dBFS and frequency of 4 MHz. The SNDR of the 3-bit ΣΔM and the calibrated one are 47 dB and 57 dB, respectively, so the SNDR improvement is about 10 dB. The noise increase around the 4 MHz is due to signal generator's noise which was not filtered by the low-pass filter.

Figure 3.16 shows SNDR versus input power for the 3-Bit ΣΔM and output of the GD algorithm using offline calibration. The input signal frequency is 4 MHz, the SNDR improvement is about 10 dB. Fig. 3.17 shows two tone test close to the modulator's loop corner. This is the worst case linearity test since loop gain reduces

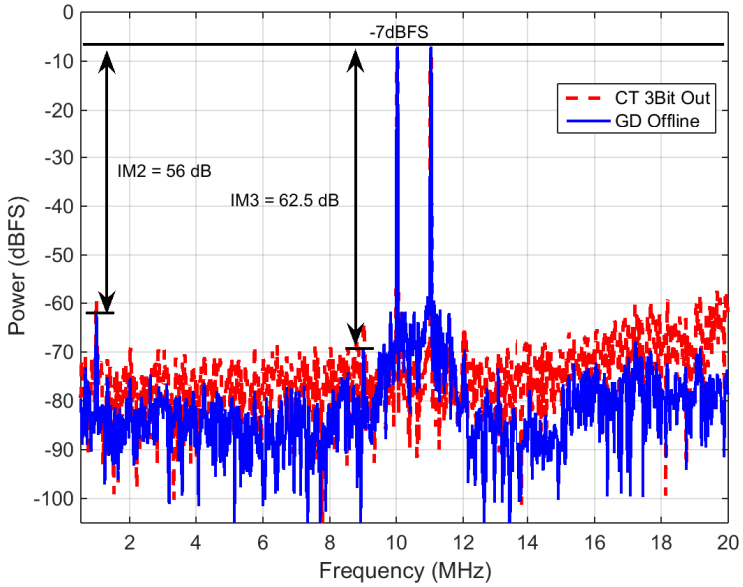


Figure 3.17: Spectrum of outputs, two tone test, input at 10MHz and 11MHz with amplitude of -7dBFS, compensated using Gradient Descent

with frequency, then limiting the benefits of linear loop feedback. The input signals are placed at frequency of 10 MHz and 11 MHz with amplitude of -7 dBFS each. As shown in Fig. 3.17, the second and third order inter-modulation products (IM2 and IM3) after calibration are -56 dBc and -62.5 dBc, respectively.

Table 4.5 summarizes performance of the prototype and compares it with some of the state-of-the-art CT-$\Sigma\Delta$Ms which have bandwith less than or equal to 25 MHz and greater than or equal to 10 MHz. The prototype was deliberately designed with the limited performance to make the quantization noise the dominant source of noise to prove the proposed calibration methodology, and that is the reason the FoM is higher than the state-of-the-art designs.

Table 3.5: Performance comparison, 10MHz$\leqslant$ BW $\leqslant$ 25MHz

Author	BW (MHz)	F_{samp} (MHz)	DR/SNR/SNDR (dB)	Power (mW)	Area (mm^2)	Technology (nm)	FOM (fJ/c) Walden*	FOM (dB) Schreier**
G. Taylor [68]	18	1152	NA/70/67.3	17	0.07	65	250	–
Y. Ke [38]	20	640	58/NA/56	8.5	0.4	90	412	151
C. Lu [17]	25	400	69/68.5/67.7	48	2.6	180	484	156
K. Matsukawa [46]	10	300	70.2/68.2/62.5	5.32	0.32	110	244	162
E. Prefasi [55]	20	2560	63/63/61	7	0.08	65	191	157
V. Dhanasekaran [21]	20	500	68/NA/60	10.5	0.15	65	321	161
J. Kauffman [35]	25	500	70/NA/63.5	8	0.15	90	131	165
K. Reddy [59]	10	600	NA/83/78.3	16	0.36	90	120	NA
A. Jain [30]	15.6	1000	67/64.5/59.8	4	0.38	130	160	163
P. Witte [79]	25	500	72/69.1/67.5	8.5	.23	90	88	167
R. Zanbaghi [82]	7.2	185	80/78.2/76.8	13.7	1.3	130	168	167
J. Kauffman [37]	25	500	72/NA/67.5	8.5	0.19	90	87.7	166
M. Andersson [3]	9	288	84/61.7/58.1	5.4	0.13	65	456	176
M. Geddada [26]	20	500	69/66/64	17.1	0.43	90	330	160
This work	**15**	**300**	**61.5/61/60**	**8.5**	**1.1**	**130**	**346**	**153**

* $FOM_{Walden} = P/\left(2BW \times 2^{(SNDR-1.76)/6.02}\right)$

** $FOM_{Schreier} = DR_{dB} + 10log\left(BW/P\right)$

3.6 Conclusion

In this project, a continuous-time $\Sigma\Delta$ modulator with digital noise cancellation technique has been presented. The prototype of a cascaded 3-0 $\Sigma\Delta$ modulator with feed-forward structure and a 3-bit quantizer in the feedback loop was implemented in 0.13 μm CMOS technology. In order to save power and improve linearity, we have adopted class-AB amplifiers in the continuous-time filter. Using modified version of Monticelli bias stage the linearity is improved. An analog differentiator is proposed in the fast path to compensate ELD without an extra DAC, so the feedback signal settles in less than one period. Finally, we have proposed a fully digital post-processing techniques to compensate analog and digital loop gains' mismatch and improve the SNR. The modulator demonstrates peak DR/SNR/SNDR of 61.5/61/60 dB, respectively while consuming 8.5 mW under a 1.2 V power supply. The OSR is 10 at sampling frequency of 300 MHz.

4. LOW POWER, JITTER TOLERANT SIGMA-DELTA MODULATOR

4.1 Introduction

In high resolution data converters, the problem of clock-jitter is a very critical issue and can significantly deteriorate the achievable SNR. A detailed analysis of clock jitter effect in CT-ΣΔM is discussed in [15, 52, 61].

In this thesis, in order to decrease the jitter effect, the quantizer output is passed through a digital low-pass filter, and as a first order analog filter is removed both power and area decrease. Also, this technique is independent of the DAC structure, and it can be combined with SCR or SSI DACs. Moreover, a current divider technique is used instead of one of the DACs which yields significant savings in silicon area and facilitates clock routing.

This chapter is organized as follows. Section 4.2 describes the system level architecture of the modulator and the proposed jitter tolerant concept. The circuit implementation of different blocks are presented in Section 4.3, and Section 4.4 demonstrates the measurement results of a prototype chip, and compare it with the state-of-the-art designs. Finally, Section 4.5 concludes the chapter.

4.2 Architecture detail

In this section the idea of jitter tolerant ΣΔM technique and system level parameters are discussed.

4.2.1 Jitter effect reduction technique

In order to decrease the effects of clock jitter, the proposed solution uses a digital low-pass filter after the quantizer to filter-out medium and high frequency quantization noise. Fig. 4.1(a) shows the third-order proposed hybrid feed-forward and

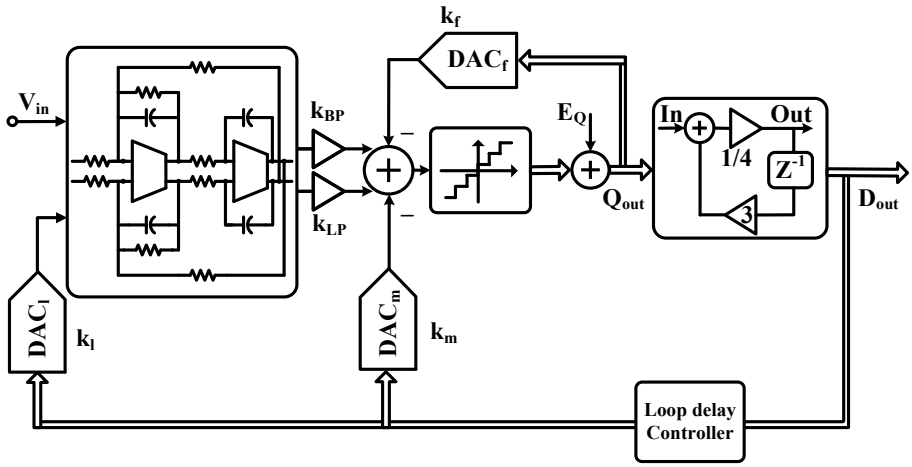
feedback structure. The loop filter is split in two parts, an analog Tow-Thomas biquad filter and a digital first-order filter. The output of quantizer (Q_{out}) is passed through a first-order digital filter and the modulator's output is set to the digital filter output (D_{out}).

The signal transfer function (STF) and noise transfer function (NTF) of proposed system are shown in Eq. 4.1:

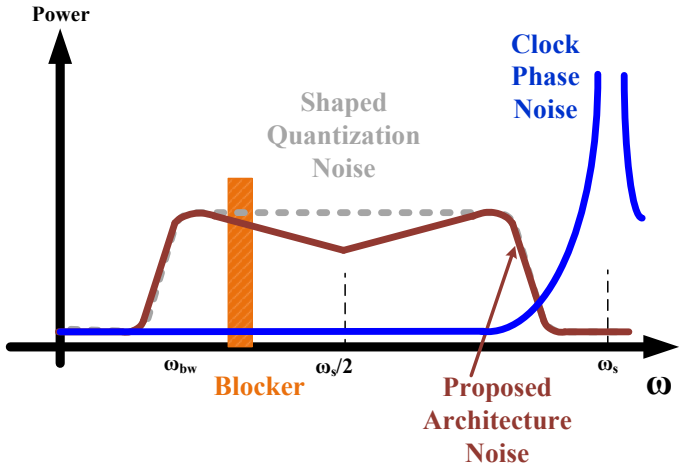
$$\begin{aligned} STF &= \frac{D_{out}}{V_{in}} = \frac{(k_{bp}HA_{BP} + k_{lp}HA_{LP}).HD_{LP}}{1 + LG} = STF_c \\ NTF &= \frac{D_{out}}{E_Q} = \frac{HD_{LP}}{1 + LG} = NTF_c.HD_{LP} \\ LG &= (k_{bp}HA_{BP} + k_{lp}HA_{LP}).HD_{LP}.k_l + HD_{LP}.k_m + k_f \end{aligned} \tag{4.1}$$

where HA_{BP} and HA_{LP} are the biquad filter's bandpass and lowpass transfer functions, HD_{LP} is the first-order digital filter's transfer function, and LG is the system loop gain.

STF_c and NTF_c correspond to signal and noise transfer functions for the conventional case where the output is taken at the quantizer output, and all the filtering is done in analog. According to Eq. 4.1, STF is similar to the conventional structure ($STF = STF_c$), but NTF includes a low pass digital filter in comparison with the conventional case ($NTF = NTF_c.HD_{LP}$). Choosing the modulator's output as the output of the digital filter, the NTF decreases with the digital filter slope, which causes the effect of convolution with PN to be decreased. Fig. 4.1(b) shows the idea graphically, adding the first order low-pass filter with a gain of one after the quantizer does not change the Signal Transfer Function (STF), but it decreases the high pass quantization noise by a slope of -20 dB/decade per every pole used in the digital filter.



(a)



(b)

Figure 4.1: (a) Block diagram of proposed CT-ΣΔM and (b) clock jitter and out-of-band noise modulation for conventional and proposed architecture

Jitter error in the presence of digital filter after quantizer is shown in Eq. 4.2; $Q_{out}(\omega)$ is multiplied by $HD_{LP}(z)$ and since for in-band signal the gain is unity, it does not have a major effect on signal gain, but it reduces the effect of out-of-band signals.

$$\begin{aligned} J_{error}(\omega) &= [(1-z^{-1})[V_{in}(\omega).STF + E_Q(\omega).NTF] \otimes J_n(\omega) = \\ &= [(1-z^{-1})[V_{in}(\omega).STF_c + E_Q(\omega).NTF_c.HD_{LP}] \otimes J_n(\omega) \end{aligned} \tag{4.2}$$

According to Eq. 4.2, the input signal's effect in jitter error is the same in comparison with the conventional architecture but the component due to shaped quantization noise reduces by HD_{LP}. High frequency quantization noise components are lowpass filtered; then, their power reduce before convolving with clock jitter, so it reduces the effect of phase noise at ΣΔM output.

4.2.2 Modulator architecture

The third-order loop filter with a 4-bit quantizer is targeted to achieve resolution of 12.5 bits in bandwidth of 10 MHz and sampling frequency of 500 MHz. As shown in Fig. 4.1(a), filter implementation uses a hybrid feed-forward/feed-back (FF/FB) structure in order to decrease excessive out-of-band peaking.

One of the poles of the loop filter is moved after the quantizer and implemented in the digital domain, so it saves almost 18% of total area, and 14% of total power. Since one of the active integrators is removed, the RC variation will have less effect on the stability of the proposed structure. The modulator utilizes a 4-bit flash ADC as a quantizer. In order to improve stability and compensate excess loop delay (ELD) a zero order loop around the quantizer is used which is implemented by DAC_f.

Extensive MATLAB/Simulink simulations were carried out to optimize the filter

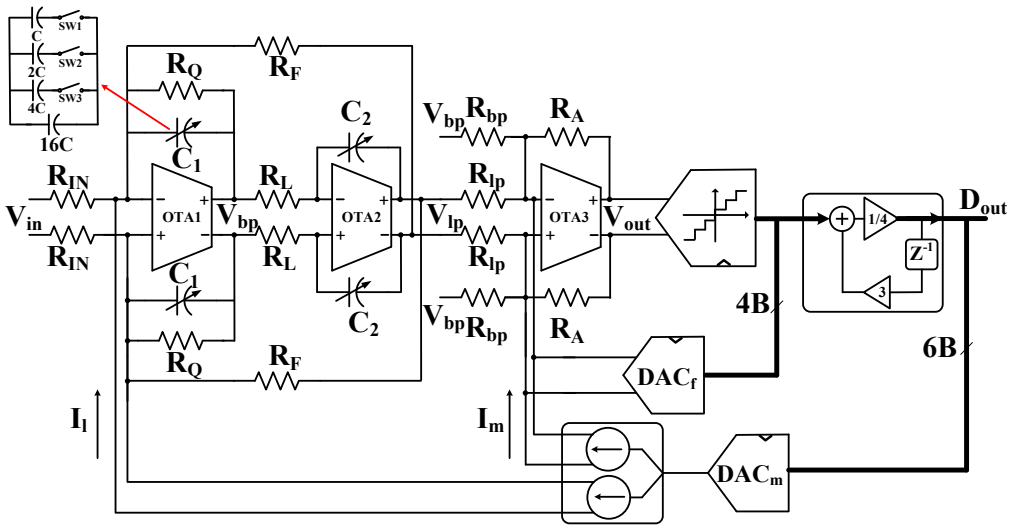


Figure 4.2: Schematic of proposed CT-ΣΔ

parameters accounting for finite OpAmp bandwidth and system non-idealities. The system parameters are shown in Table 4.1, ω_0 is analog filter bandwidth; Q is filter quality factor; A_{lp} is the in-band gain of the biquad, and k_{LP} and k_{BP} are lowpass and bandpass path coefficients, respectively. The biquad gain and lowpass/bandpass coefficients are selected based on internal peaking at bandpass output and to relax the gain requirement of the summing amplifier [26].

The feedback coefficients k_f, k_m, and k_l need to be implemented by three different DACs. In this project we combine k_m and k_l coefficient in a single DAC and use a current divider with the ratio of two coefficients to be connected to common ground of OTAs, which is shown in Fig. 4.2. By doing so, we can save significant area and improve DACs' synchronization and reduce clock routing and layout complexity.

The signal transfer function and noise transfer function of the proposed system are shown in Fig. 4.3. The out-of-band peaking of STF is about 4 dB, and NTF decreases at high frequencies with a slope of -20 dB/dec due to digital filter effect as

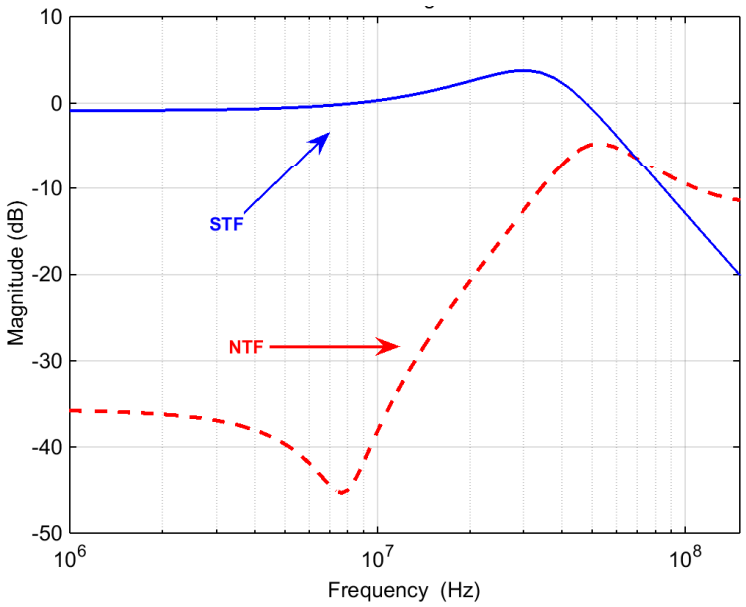


Figure 4.3: STF and NTF of proposed system

it is confirmed by Eq. 4.1.

As shown in Fig. 4.2, the integrating capacitors are tunable using three control bits which cover ±20% RC variations. The passive components are given in Table 4.2. In a combined FF-FB modulator, the noise and nonlinearity contributed by the loop filter are predominantly due to the first amplifier and the outer most DAC, as the other OTAs' noise and linearity are relaxed by first stage's gain. The input resistor is chosen based on noise performance, and other passive elements are designed based on system parameters (Table 4.1) and input resistor value.

The first order digital low pass filter transfer function is shown in Eq. 4.3.

$$H_{LP}(z) = \frac{\alpha_0}{1 - \alpha_0\beta_0 z^{-1}} \tag{4.3}$$

where α_0 and β_0 are feedforward and feedback parameters of digital filter, respectively. Since the digital low-pass filter is used after the quantizer, low-frequency gain

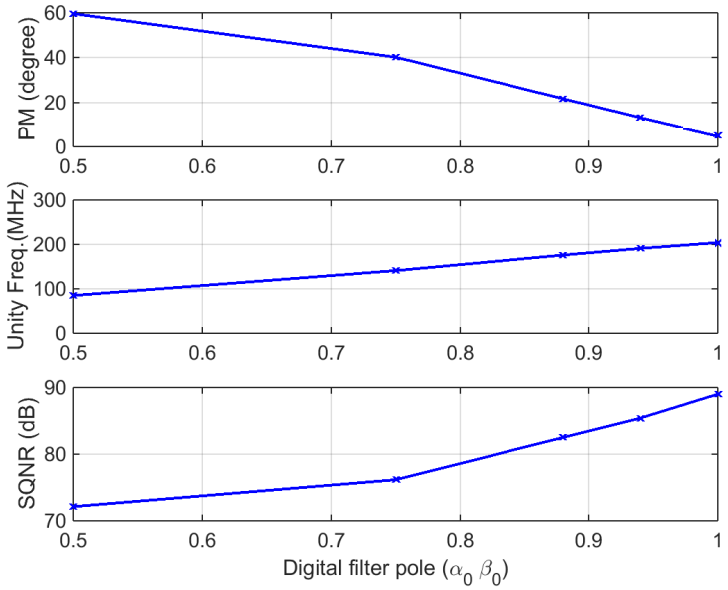


Figure 4.4: Loop performance (phase margin, loop unity gain frequency and SQNR) vs $\alpha_0\beta_0$ of digital low pass filter

is selected to be unity ($\alpha_0 = 1-\alpha_0\beta_0$), to avoid quantization noise amplification after quantizer. So, all the in-band gain of loop filter is provided by the analog filter. The nominal value of digital filter pole ($\alpha_0\beta_0$) is 0.65, but in order to optimize hardware resources and system performance, we swept the pole value and studied the system performance to find its optimum value. One of the constraints was to choose the digital filter coefficients to be a factor of 2, so we just needed a shift left/right for multiply/divide by 2, which can be done in less than one clock period. The system signal-to-quantization-noise-ratio (SQNR), phase margin (PM) and unity gain frequency vs $\alpha_0\beta_0$ for input frequency of 2.5 MHz and amplitude of -2.4 dBFS are shown in Fig. 4.4. According to these results, in order to have large SQNR, $\alpha_0\beta_0$ should be large but increasing $\alpha_0\beta_0$ affects system stability and its implementation becomes complicated. On the other hand if we choose the value of $\alpha_0\beta_0$ to be small, the digital filter is less effective, and the SQNR degrades. In order to have good

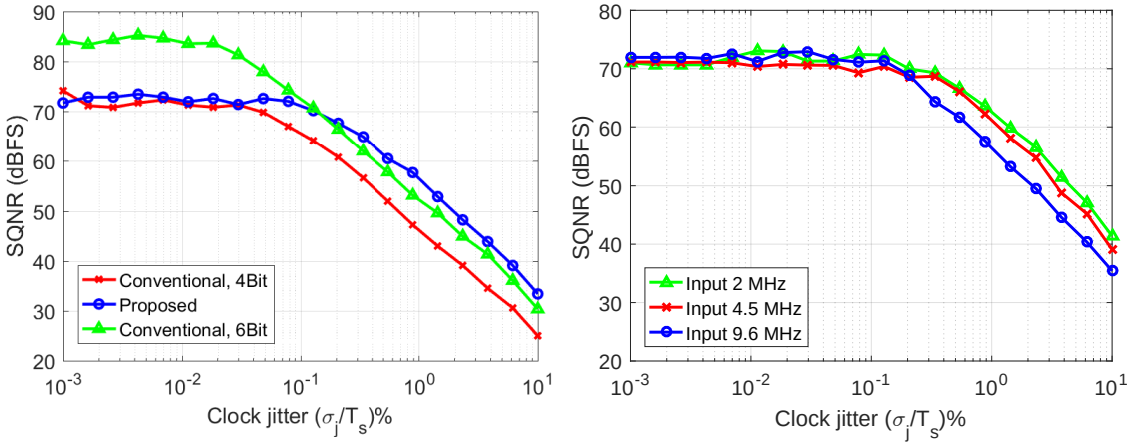
trade-off between SQNR, complexity of digital filter, and stability, we chose $\alpha_0\beta_0$ to be 3/4, so the place of the pole in the digital filter will be at 26 MHz. By choosing $\alpha_0\beta_0 = 3/4$, the discrete time recursive equation of the lowpass filter is:

$$V_o[n] = \frac{3}{4}V_o[n-1] + \frac{1}{4}V_i[n] \tag{4.4}$$

So the digital filter needs two shift registers and a couple of adders to be implemented. The details of the implementation are discussed in Section 4.3.2 .

To observe the effect of using the digital filter after quantizer on CT-ΣΔM performance in the presence of clock jitter, the system was simulated using the additive jitter error model in NRZ DAC [61]. In this model, the jitter error is modeled as Eq. 2.9, and added to feedback path. The RMS jitter is swept up to 10% Ts, and SNR for the conventional system with 4-Bit DAC and 6-Bit DAC and the proposed one is shown in Fig. 4.5(a). The input tone is 9.6 MHz with an amplitude that corresponds to -6 dBFS. It is clear that using a digital filter after quantizer results in more than 10 dB tolerance in comparison with 4-Bit conventional system for the case rms clock jitter is as large of 1% of the clock period; moreover the proposed method is more tolerant to jitter than 6-Bit conventional modulator while it can save area and power of 6-Bit quantizer. So, the proposed modulator can handle higher jitter figures than the conventional CT-ΣΔ with the same loop gain transfer function. Fig. 4.5(b) shows the sensitivity of CT-ΣΔM to different input frequencies. According to the figure, higher frequency inputs are affected more by jitter noise, which is clear from the in-band jitter induced noise (σ_{IBJN}) equation as well [11].

The sensitivity of CT-ΣΔM to clock jitter in the presence of a blocker is shown in Fig. 4.6(a). The signal and blocker frequencies are 9.6 MHz and 55 MHz, with amplitude of -6 dBFS and -20 dBFS, respectively. The frequency of the blocker is



(a) (b)

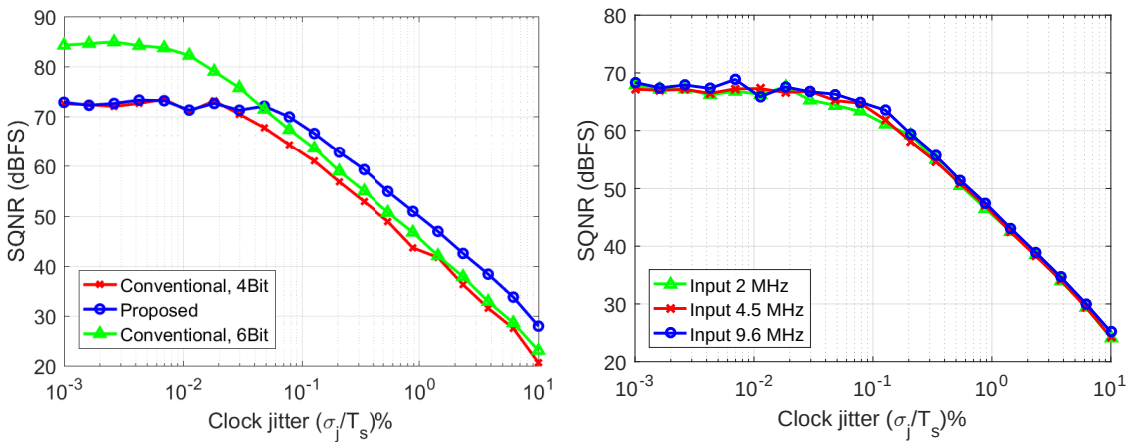
Figure 4.5: Simulation results (a) SQNR for both conventional and proposed CT-ΣΔM as function of clock jitter; input signal power is -6 dBFS at 9.6 MHz and (b) SQNR variation for different frequencies; input power is -6 dBFS

placed at the peak of the NTF. In the presence of the blocker the SNR reduces by 5dB when jitter standard deviation is around 0.1% Ts; but the proposed design is more tolerant to jitter than the conventional 4-Bit and 6-Bit architecture. Fig. 4.6(b) shows the sensitivity of CT-ΣΔM for different input signal frequencies in the presence of a close-in-band 20 MHz blocker. In this case, both input signal and blocker power are -10 dBFS. In the presence of the blocker, SNR for different jitter rms noise voltages are almost the same for different in-band frequencies. A comparison between the results in Fig. 4.5 and 4.6 shows that the blocker components are dominant factor when considering clock jitter effects. If strong blockers are close to the peak of the STF, signal power increases and non-linearities may arise that increase the in-band noise power. Also, near in-band blockers are partially up-converted due to the embedded sampling at the input of the quantizer; this component convolves with clock jitter in the main DAC, then folds back additional noise components.

The qualitative comparison between conventional system vs proposed one for a

Table 4.1: Loop filter parameters

ω_0	Q	A_{lp}	k_{LP}	k_{BP}	k_f	k_m	k_l
$2\pi\times$7.8MHz	3	7	7.8	3.5	1	3.6	1



(a) (b)

Figure 4.6: Simulation results (a) SQNR for conventional and proposed CT-ΣΔM as function of clock jitter in presence of -20 dBFS blocker at 55 MHz; input signal power is -6 dBFS at 9.6 MHz and (b) SQNR variation for different input frequencies in presence of -10 dBFS blocker at 20 MHz; input power is -10 dBFS

Table 4.2: Passive components

R_{in}	$R_L = R_F$	R_Q	R_{lp}	R_{bp}	R_A	$C1 = C2$
1K	7K	21K	1.27K	2.84K	10K	2.89p

Table 4.3: Qualitative comparison of proposed modulator vs conventional 4-Bit and 6-Bit

	Conventional with 4-Bit Quantizer and DAC	**Proposed with 4-Bit Quantizer and 6-Bit DAC**	**Conventional with 6-Bit Quantizer and DAC**
Quantizer power and area	Low	Low	High
DAC power and area	Low	High	High
Jitter Sensitivity	High	Very Low	Low
Loop filter power	Static	1/3 of power dynamic	Static
Loop filter area	High due to capacitors	Lower due to digital filter	High due to capacitors

third order loop is summarized in Table 4.3. According to the table the proposed structure increase jitter tolerance while it saves power and area.

4.3 Circuit design

In this section CT-ΣΔM circuit implementation is discussed. The description of the quantizer is not included in this thesis, but details can be found in [57, 70, 72].

4.3.1 Operational transconductance amplifier

A two-stage amplifier with feed-forward compensation is adopted [69] to satisfy the requirement of high amplifier gain. The simplified fully-differential schematic of the amplifier is shown in Fig. 4.7. The loop parameters and some parameters of first operational transconductance amplifier (OTA), including load capacitor and

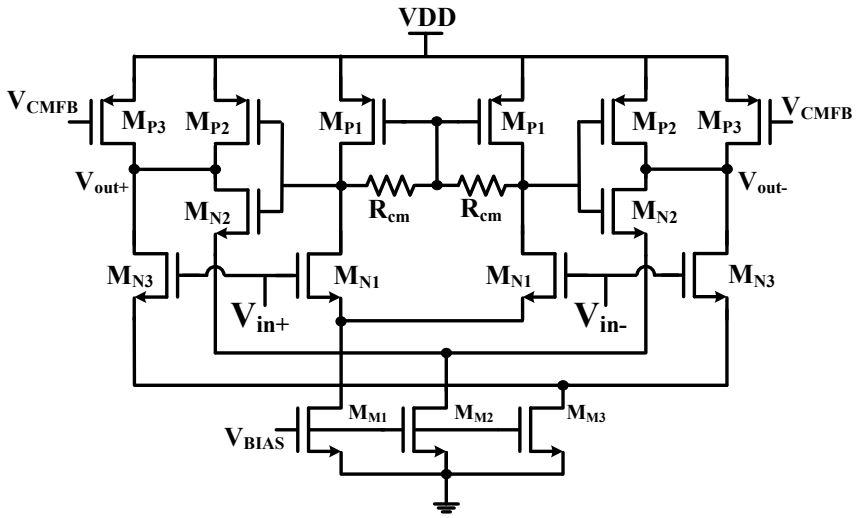


Figure 4.7: Fully differential feed-forward compensation OTA

Table 4.4: OTA specification including first integrator's resistors and capacitor as a load

Amplifier specs	DC Gain 34dB	GBW 2GHz	Input Refereed Noise 6.4nV/sqrt(Hz)	Power 0.6mW
Parameters	$gmN1$, $gdsN1$ 1.1mA/V, 51uA/V	$gmN2$, $gdsN2$ 1.1mA/V, 69uA/V	$gmP2$, $gdsP2$ 1.7mA/V, 83uA/V	$gmN3$, $gdsN3$ 2mA/V, 110uA/V

resistors are given in Table 4.4.

The first stage differential pair was optimized based on high gain and bandwidth. The second stage is a differential push-pull inverting amplifier (M_{N2}, M_{P2}, M_{M2}), which is optimized for high linearity and to have a high transconductance gain ($g_{m_{N2}} + g_{m_{P2}}$). Fully differential feed-forward compensation (M_{N3}, M_{M3}) provides LHP zero, which makes the OTA stable without using a miller capacitor. All OTAs in filter architecture (OTA1, OTA2 and OTA3) have the same topology, but they are optimized in terms of power for later stages.

4.3.2 Digital first order low pass filter

The ASIC implementation of the digital filter is shown in Fig. 4.8. The modulator utilizes a flash-ADC as a multi-bit quantizer, so input data of the digital filter is 4-bit, but the output is chosen to have a 6-bit resolution to preserve most significant decimal points. The 4-bit output of the quantizer is applied to the first adder (Σ_1), and it is summed with delayed version of output. Both inputs of adder Σ_2 are the same which results in multiply by two operation, adder Σ_2 is used instead of shift left to have the same delay as feed-forward path (Σ_1). So, overall adder blocks Σ_1, Σ_2 and Σ_3 generates the function of $3D_{out}(n-1)+D_{in}(n)$, and in order to divide by 4, two LSBs are right shifted. The internal adders are designed to have 11/12 bits for recursive operation and to preserve accuracy internally. Only 6 bits are used for the modulator's feedback. The adders are Ripple-Carry adder, and the worst case delay (passing the carry-in of first full-adder to carry-out of last full-adder) for 10 bit adder is about 50 ps, and the worst case overall delay from first adder to third adder is about 120 ps, which is about fifteen times smaller than clock period. The delay block (z^{-1} function) consists of 10 D-Flip-Flops (D-FF) to delay the output by one sampling period.

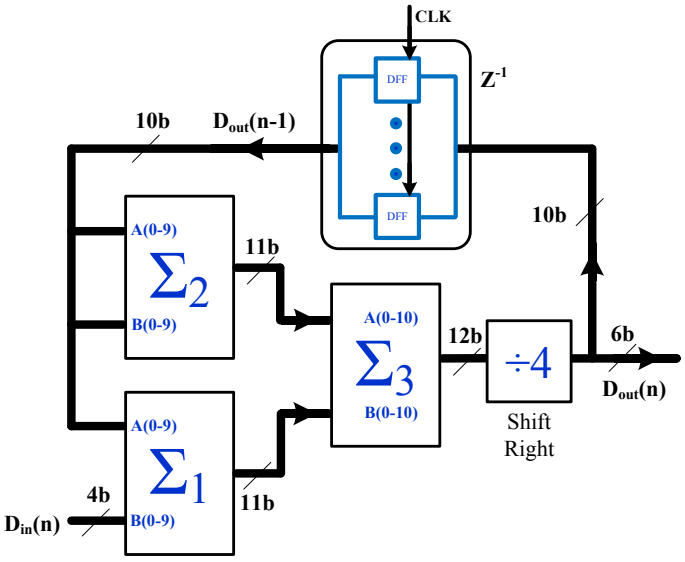


Figure 4.8: Digital filter schematic

4.3.3 Current steering DAC

The proposed system employs three DACs as shown in Fig. 4.2. DAC_m used as the main feedback path and employs a current divider circuitry making the effect of two DACs: one for main path (I_l) and the other one for intermediate DAC functionality (I_m). DAC_f is used for the realization of the fast path. Since DAC_f is connected to the quantizer output, and DAC_m is connected to the digital filter, they need a 4-bit and 6-bit DAC, respectively. In this design the non-return-to-zero (NRZ) DAC is used for its low sensitivity to jitter.

Main DAC has the most stringent requirements in terms of linearity and noise, and it requires large devices to achieve the required matching. In order to have good balance between DNL, noise, power consumption, silicon area, speed, and 6-bit DAC complexity [73], we employed a segmented current steering DAC. Current steering blocks can easily be switched, sum, scale and usually operate at high frequencies [78],

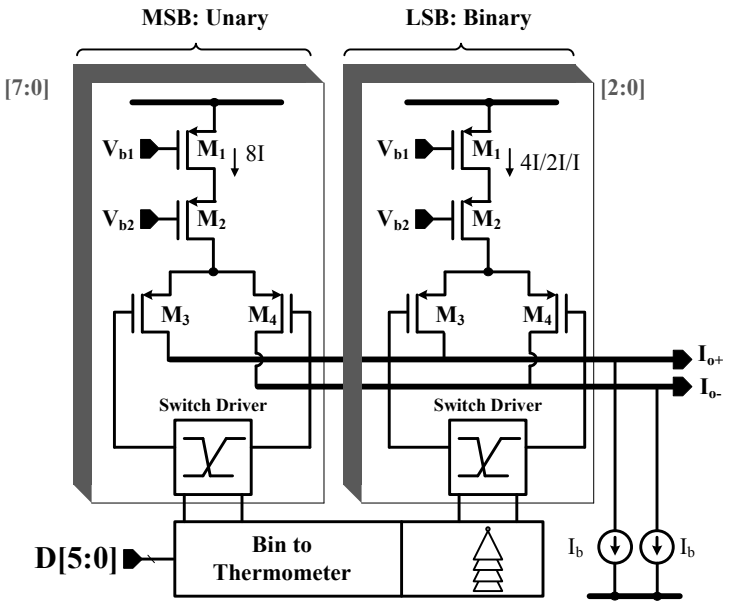


Figure 4.9: Segmented DAC schematic

so the current steering DAC is the best candidate for this design. Fig. 4.9 shows the circuit level realization of the segmented current steering DAC. The DAC is divided into two sub-DACs: the 3 least significant bits (LSBs) are implemented using a binary architecture while the 3 most significant bits (MSBs) are implemented in a unary way. Since the segmented architecture is a mixture of binary and unary sections it has the benefits of a unary DAC such as good DNL, small glitch and high monotonicity, as well as the benefits of a binary DAC such as simplified clock routing, reduced clock delay mismatches, small area and relaxed layout complexity. Since the output of the digital filter is binary, just the MSBs need a binary-to-thermometer decoder to convert the 3-MSBs in to 8-decoded output. In order to equalize the delay between the segmented parts a dummy decoder is used for binary 3-LSBs.

Each DAC unit element comprises four separate circuits: a re-timing D-FF, low-swing low-crossing nMOS switch drivers, cascode devices and p-type switched-current

sources. In order to synchronize all the inputs of DAC, D-FFs are used in front of the DAC. With this retimed D-FF, the explicit ELD of 50% sampling time is realized. Low-swing low-crossing nMOS switch drivers are used to prevent the cascode current sources from switching between cut-off and active mode; hence, the glitch is decreased. So, one switch will go on before the other one goes off enabling the cascode mirrors to remain active at all times. The low-swing digital input reduces clock feed-through and low crossing prevent the p-type current switches from turning off simultaneously to minimize glitch energy.

High output impedance current mirrors using cascode devices are implemented to reduce the currents sensitivity to the output voltage, and thus reduce current glitches that might occur because of a change in the output voltage. The PMOS current sources are sized based on a Monte Carlo analysis to achieve the desired 12.5-bit intrinsic matching. As there is no calibration, the linearity of Main DAC is limited by the device matching, Monte Carlo simulations show that worst case mismatch for unity current sources is around 0.31%. As the main DAC combines the two coefficients of feedback (k_m and k_l in Fig. 4.1), the overall current of main DAC is $I_l + I_m = 751.85uA$. So, the LSB unit current is $I_{cell} = 751.85uA/63 = 11.93uA$.

Fast DAC which is connected to the output of the loop filter, has relaxed requirements, since most of its non-idealities are suppressed by the loop gain. However, fast path dominates loop operation at high frequencies and its non-linearities increase the in-band noise due to the mixing of blocker and high out-of-band quantization noise, as well as self mixing of high frequency noise. Fast DAC linearity is then critical as well, and cautions must be taken when designing it. The fast path DAC is a unary 4-bit current steering DAC with an overall current of 55 uA, and an LSB current of 55uA/15=3.66uA.

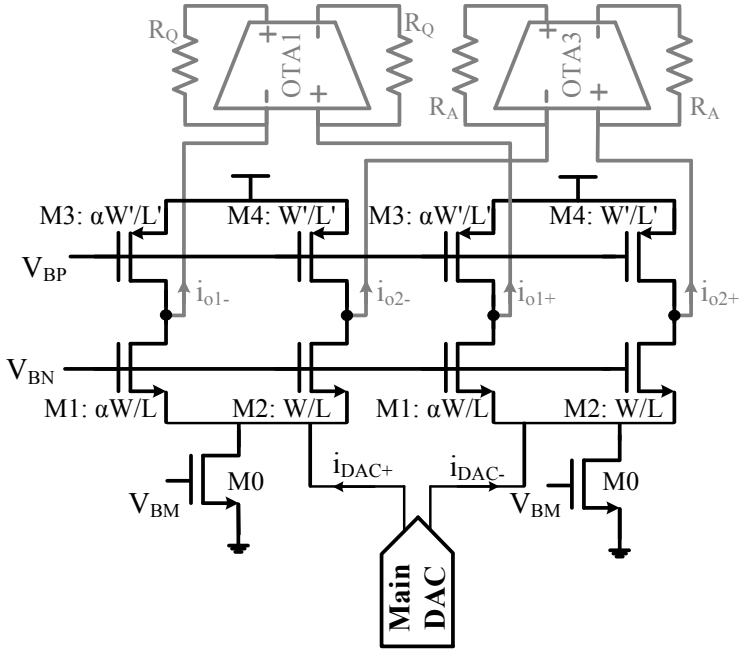


Figure 4.10: Current divider schematic

4.3.4 Current divider

In order to decrease layout complexity, we propose to use one main DAC and a current divider, which divides the current of DAC_m, and provides currents for two branches. The fully differential current divider schematic is shown in Fig. 4.10.

The main DAC (DAC_m) is connected to the common source of the transistors M1 and M2, which are biased with current source (M0). So, the AC current that passes through M1 and M2 is proportional to their dimensions and as their V_{GS} is the same, the current in each branch is proportional to transistor sizes. Eq. 4.5 shows the small signal analysis of the circuit. The drain of M1 and M2 is connected to the virtual ground of OTA1 and OTA2 and their common mode feedback force the drain voltage of M1 and M2 to be constant. PMOS transistors, M3 and M4, have the same ratio as M1 and M2 $\left(\frac{(W/L)_1}{(W/L)_2} = \frac{(W/L)_3}{(W/L)_4} = \rho\right)$, and the sum of their currents

are equal to the bias current of M0. So, only AC current will be injected to OTAs.

$$\begin{cases} i_{o1} = \frac{(W/L)_1}{(W/L)_1+(W/L)_2} i_{DAC} = \frac{\rho}{\rho+1} i_{DAC} \\ i_{o2} = \frac{(W/L)_2}{(W/L)_1+(W/L)_2} i_{DAC} = \frac{1}{\rho+1} i_{DAC} \end{cases} \tag{4.5}$$

The maximum AC current of the main DAC, and accordingly the maximum AC current of the current divider is 751.85u, so in order to have good linearity, we used 0.8 mA bias to provide the current divider with enough bias current. Based on feedback coefficients ($k_m = 3.6$ and $k_l = 1$) the NMOS and PMOS transistor sizes (W/L and W'/L') are found to be $\frac{25\mu m}{0.16\mu m}$ and $\frac{45\mu m}{0.2\mu m}$, respectfully; the scaling factor (ρ) is 2.7 (Fig. 4.10).

The noise contribution of the feedback path ($V_{n,in,FB}$) at input of $\Sigma\Delta$ is:

$$V^2_{n,in,FB} = [(\frac{\rho}{\rho+1})^2 I^2_{n,DAC} + I^2_{n,CD}].R^2_{in}.BW \tag{4.6}$$

where, $I_{n,DAC}$ and $I_{n,CD}$ is main DAC and current divider noise, respectively. The thermal noise contribution of the main DAC and current divider are about 5 $nV/\sqrt{Hz}$ and 7 $nV/\sqrt{Hz}$, respectively. So the overall signal to thermal noise ratio is around 80 dB, which is about 6 dB higher than theoretical signal to quantization noise ratio.

4.4 Measurement results

The proposed prototype is fabricated in a 40 nm CMOS process through TSMC and assembled in a 56-pin QFN package. Fig. 4.11 shows the die photograph. The modulator occupies 0.06 mm^2 and consumes 6.9 mW from a 1.1 V supply. The static and dynamic powers are 5.7 mW, and 1.2 mW, respectively. The power and area distribution are shown in Fig. 4.12. The analog filter consumes the highest

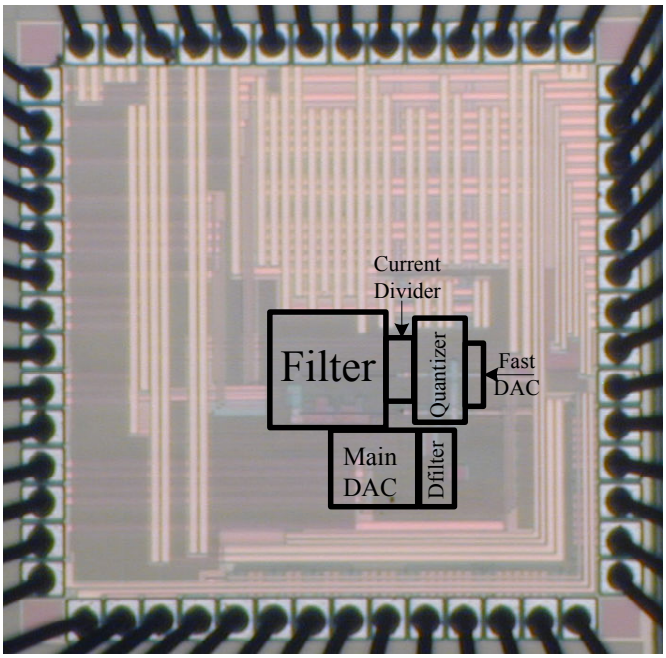
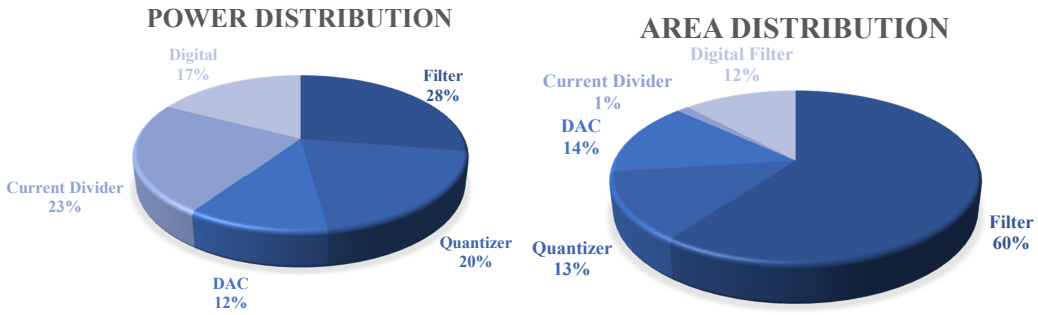


Figure 4.11: Die micrograph of chip

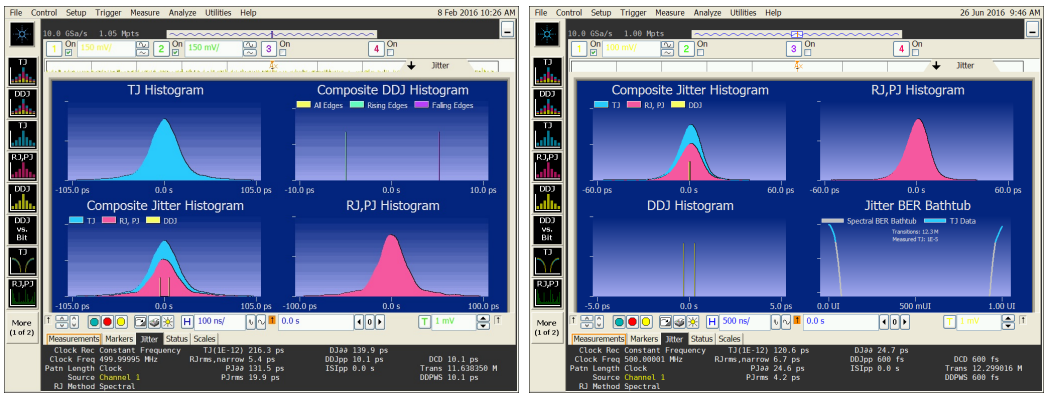
portion (28% of total power). The current divider and quantizer consumes 1.6 mW and 1.4 mW static power, respectively. The dynamic power consumption of digital blocks, including the digital first-order filter, is about 1.2 mW, thus digital filter saves almost 1 mW in comparison with its analog counterpart. Fig. 4.12(b) shows the filter occupying 60% of the area due to capacitors. So, it is clear that removing one of the integrators and implementing it in the digital domain can save a significant area, as the area of the digital filter is only 12% of the total modulator area.

The signal is converted from single-ended to differential with appropriate common-mode voltage using an on-board RF transformer (ADT1-6T). The clock signal is generated using a PSG Vector Signal Generator (Agilant E8267D), which has peak to peak jitter of almost 215 ps (with a BER of 1E-12), and Silicon Lab's Clock Generator Development Kit (Si5341) which has peak to peak jitter of 120 ps (with a



(a) (b)

Figure 4.12: (a) Power distribution of modulator with overall power of 6.9 mW and (b) area distribution of modulator with overall area of 0.06 mm^2



(a) (b)

Figure 4.13: (a) Input clock jitter of PSG Vector Signal Generator (b) input clock jitter of Clock Generator Development Kit

BER of 1E-12) at the sampling frequency of 500 MHz. The measured clock jitter is shown in Fig. 4.13 which captured by Agilent DSA91304A, the RMS jitter is around 20 ps and 4.2 ps for two clock generators.

The modulator output, which was brought out of the chip at full rate using an LVDS interface, was captured using a real-time oscilloscope (Agilent Infinium DSA91304A) and then processed offline using MATLAB/Simulink to determine the

output sequence. A 16K Hann window was used for spectral estimation to avoid spectral leakage.

Two passive 2 MHz and 4.1 MHz band-pass filters were used to reduce the harmonic distortion components and minimize noise from the input signal source. The single sinusoidal input tone was then converted into a differential signal using the on-board RF transformer (ADT1-6T).

Figure 4.14 shows the measured power spectral density (PSD) of the modulator with 20 ps RMS jitter (1% of sampling period) and 4.5 ps RMS jitter (0.22% of sampling period) for input tone with power of -4 dBFS and frequency of 2 MHz. The measured SNR and SNDR with RMS jitter of 20 ps are 63 dB and 62.5 dB, respectively and with RMS jitter of 4.5 ps are 66 dB and 65.5 dB, respectively. According to Fig. 4.14 the SFDR is 78 dB.

Fig. 4.15 shows measured SNR and SNDR of the proposed $\Sigma\Delta$M as a function of input signal amplitude for a 2 MHz input in the presence of 1% Ts RMS jitter (20 ps). Peak SNR and peak SNDR are 65 dB and 64 dB, respectively.

Fig. 4.16 shows the dynamic range of the proposed $\Sigma\Delta$M as a function of the signal amplitude for a 4 MHz input. The measured and post-layout simulation results with an RMS jitter of 0.2% Ts and 1% Ts are included. It is clear that the simulation results with RMS jitter of 1% match closely with measured data, but the measured results with RMS jitter of 0.2% Ts has some discrepancy with simulation results which authors believe it is due to the lack of purity of their clock generator which produces low power spurious tones at 125 MHz, that convolves with out-of-band noise and increase in-band noise level. The measured dynamic range with an RMS jitter of 0.2% Ts and 1% Ts are 75 dB and 70 dB, respectively, while the dynamic range of post-layout simulation with RMS jitter of 0.2% Ts is 83 dB.

In order to better quantify CT-$\Sigma\Delta$M linearity, two tone signals at frequencies

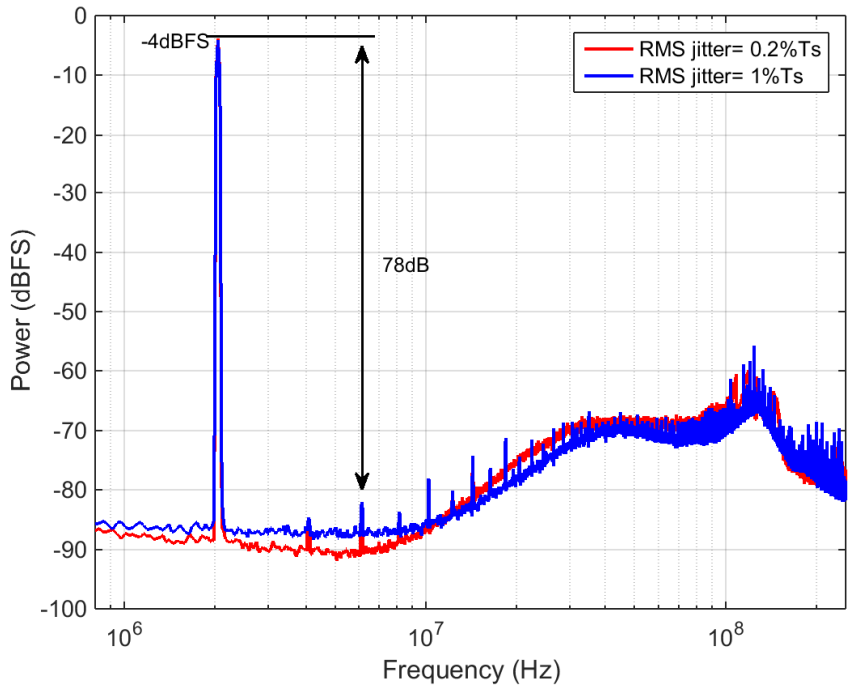


Figure 4.14: Measured spectrum of CT-ΣΔ for input signal of -4 dBFS at 2 MHz, for the cases peak-to-peak clock jitter is 215 ps (RMS jitter = 1% Ts) and 120 ps (RMS jitter = 0.22% Ts)

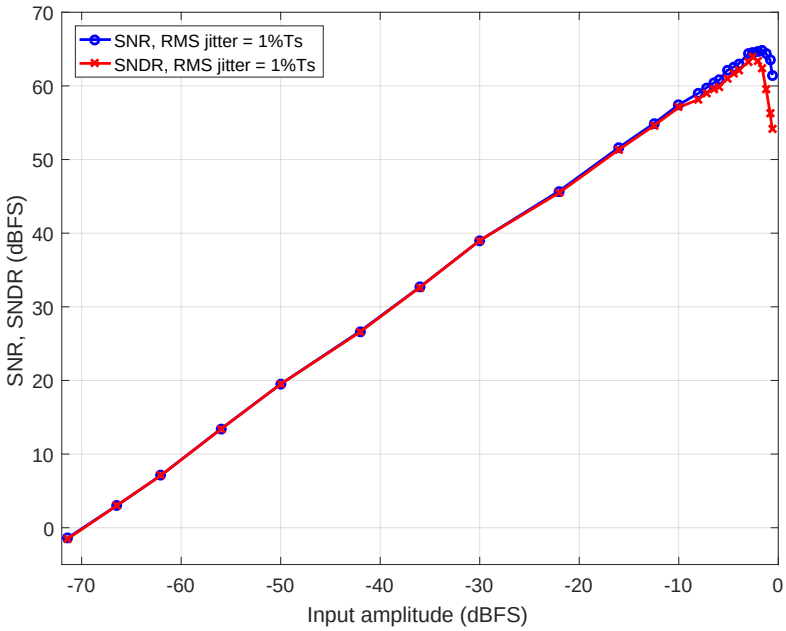


Figure 4.15: Measured SNR and SNDR vs input power; input frequency is 2 MHz

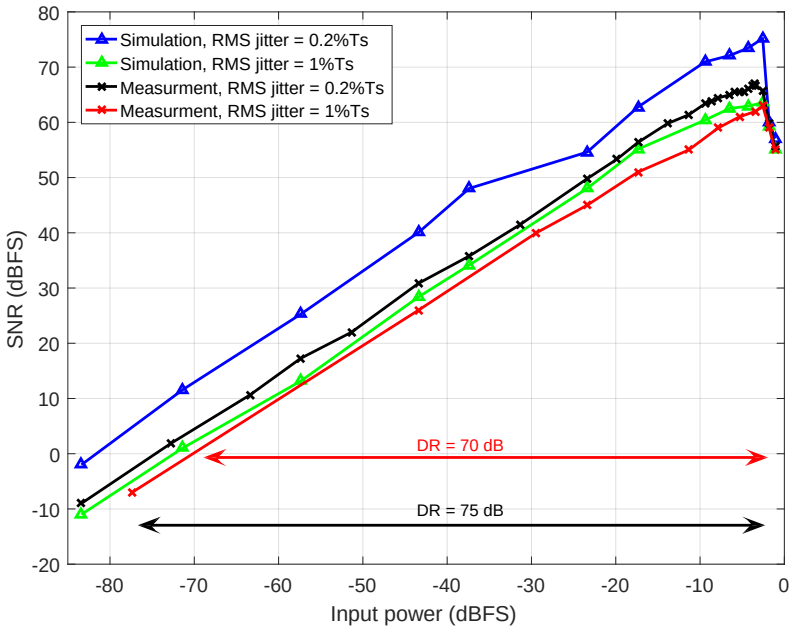


Figure 4.16: SNR vs input power with input of 4 MHz

of 3.8 MHz and 4.5 MHz were applied to the modulator input, the power of each tone is -7 dBFS (with total RMS power of -4 dBFS), and the measurement result is shown in Fig. 4.17. The IM2 is -71 dB, while the modulator's IM3 is around -73 dB. For these measurements, the RMS clock jitter is around 20 ps. Thus, significant area, power and design efforts can be saved due to the low clock jitter sensitivity properties of the proposed architecture.

In order to quantify the jitter sensitivity of proposed architecture in presence of clock jitter and out-of-band signals, a blocker signal is applied to CT-ΣΔM. A blocker tone with different amplitudes at frequency of 40 MHz are applied to input of ΣΔM while the in-band signal was set at -15 dBFS and 2 MHz and RMS clock jitter was 20 ps. The measured integrated in-band noise (IBN) are shown in Fig. 4.18(a). Due to large clock jitter used in this test, for sufficiently large OOB blocker (larger than -25 dBFS) the IBN increase drastically. To see the effect of blocker frequency

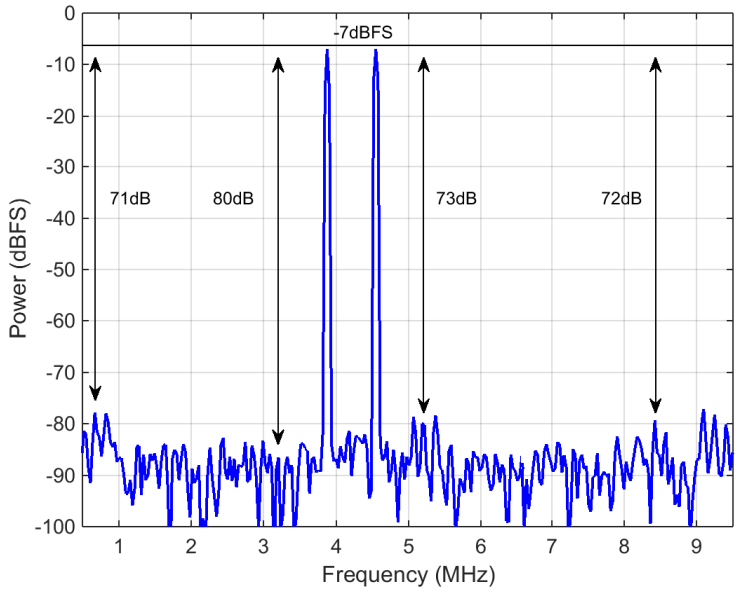
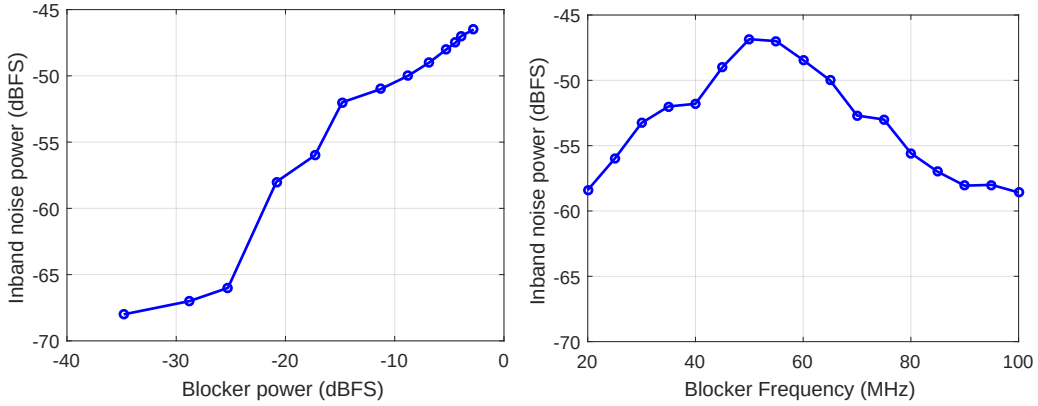


Figure 4.17: Measured two-tone test with RMS power of -4 dBFS and frequencies of 3.8 MHz and 4.5 MHz with RMS clock jitter of 20 ps

in jitter induced in-band noise, a blocker tone with different frequencies and fixed amplitude of -10 dBFS is applied to input of ΣΔM while the in-band signal was -15 dBFS at 2 MHz and RMS clock jitter was 20 ps. The measured integrated inband noise (IBN) vs blocker frequency is shown in Fig. 4.18(b). For blocker frequencies in the range of 40-65 MHz the IBN increase due to peaking in STF but for higher frequencies the IBN decrease due to effect of low-pass STF; also as a result of first order filter in NTF, the convolved high frequency quantization noise with phase noise is reduced.

Table 4.5 shows some of the most efficient ΣΔ modulators that have been published recently. The reported results in those papers do not include jitter effect. The table includes the proposed design with 0.2% Ts and 1% Ts RMS clock jitter. The proposed design with 0.2% Ts RMS jitter is better than most of the designs in terms of Schreier FOM except [3] and [65]. Reference [3] has sampling frequency almost



(a) (b)

Figure 4.18: Measured integrated in-band noise with RMS jitter of 20 ps, input tone -15 dBFS at 2 MHz (a) sweeping amplitude of 40 MHz blocker (b) sweeping blocker frequency, inband signal -15 dBFS at 2 MHz

half of the proposed architecture and [65] used 28 nm technology as a result they could save almost half of the power of proposed architecture. In presence of RMS clock jitter as high as 1% Ts the performance of proposed architecture is comparable with several designs with minimum jitter. The jitter tolerance in the proposed design is more than 10 dB in comparison with the conventional design and same loop filter, and it can relax the clock generator circuits.

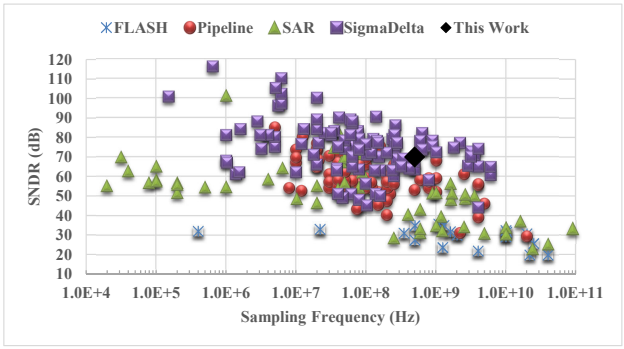
Fig. 4.19 shows the SNDR and FoM of the proposed system in comparison with all the ISSCC and VLSI papers since 1996 [49], in this plot we used the results with no jitter in order to make the performance comparable with others. According to the figures, SNDR is comparable with most of the $\Sigma\Delta$ modulators, and FoM is is smaller than 10% of the architectures.

Table 4.5: Performance comparison, $2010 \leqslant Year$, $10MHz \leqslant BW \leqslant 25MHz$

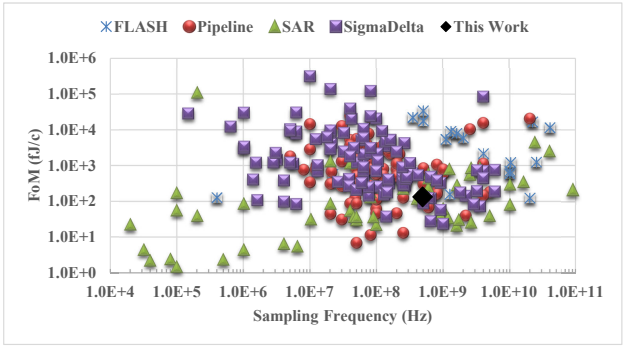
Author	BW (MHz)	F_{samp} (MHz)	DR/SNR/SNDR (dB)	Power (mW)	Area (mm^2)	Technology (nm)	FOM (fJ/c) DR/SNR/SNDR*	FOM (dB) Schreier**
G. Taylor [68]	18	1152	NA/70/67.3	17	0.07	65	NA/182/250	FOM
Y. Ke [38]	20	640	58/NA/56	8.5	0.4	90	327/NA/412	151
Y. Shu [64]	18	360	68/64/62.5	183	0.68	180	2476/3925/4664	147
C. Lu [17]	25	400	69/68.5/67.7	48	2.6	180	416/441/484	156
K. Matsukawa [46]	10	300	70.2/68.2/62.5	5.32	0.32	110	100/126.6/244.1	162
E. Prefasi [55]	20	2560	63/63/61	7	0.08	65	151/151/191	157
V. Dhanasekaran [21]	20	500	68/NA/60	10.5	0.15	65	127/NA/321	161
J. Kauffman [35]	25	500	70/NA/63.5	8	0.15	90	62/NA/131	165
J. Jo [34]	20	640	68/67.9/63.9	58	1.17	130	706/714/1132	153
K. Reddy [59]	10	600	NA/83/78.3	16	0.36	90	NA/69/120	NA
A. Jain [30]	15.6	1000	67/64.5/59.8	4	0.38	130	70/93/160	163
V. Singh [67]	16	800	75/67/65	47.6	0.66	180	323/813/1023	160
P. Witte12 [79]	25	500	72/69.1/67.5	8.5	.23	90	52/73/88	167
Y. Shu [65]	18	640	78.1/NA/73.6	3.9	0.08	28	16.5/NA/28	174
R. Zanbaghi [82]	7.2	185	80/78.2/76.8	13.7	1.3	130	116/143/168	167
J. Kauffman [37]	25	500	72/NA/67.5	8.5	0.19	90	52/NA/87.7	166
M. Andersson [3]	9	288	84/61.7/58.1	5.4	0.13	65	23/301/456	176
M. Geddada [26]	20	500	69/66/64	17.1	0.43	90	185/262/330	160
This work, $\sigma_{j,RMS} = 0.2\%T_s$	**10**	**500**	**75/68/67**	**6.9**	**0.06**	**40**	**75.5/168/188**	**166.5**
This work, $\sigma_{j,RMS} = 1\%T_s$	**10**	**500**	**70/65/64**	**6.9**	**0.06**	**40**	**133/237/266**	**161.5**

* $FOM_{xx} = P/\left(2BW \times 2^{(xx-1.76)/6.02}\right)$

** $FOM_{Schreier} = DR_{dB} + 10log\,(BW/P)$



(a)



(b)

Figure 4.19: Comparison of the proposed system with ISSCC and VLSI papers [49] (a) SNDR vs sampling frequency (b) FoM vs sampling frequency

4.5 Conclusion

In this project the loop filter is divided into analog and digital parts to overcome the sensitivity of feedback DAC to clock jitter without adding extra delay to the loop. By implementing one of the poles of the loop filter digitally, the power consumption and area are saved. Moreover, two feedback coefficients were combined into one DAC, and a current divider was used to generate the coefficients which saves area and relaxes the layout complexity. The prototype chip achieved a dynamic range of 75 dB and a peak SNDR of 67 dB in presence of 0.2% Ts RMS jitter and in a 10 MHz bandwidth while sampling at 0.5 GS/s in 40 nm CMOS technology. Consuming 6.9 mW from a 1.1 V supply, the converter has an Schreier FOM of 166.5 dB with 0.2% Ts RMS jitter and 161.5 dB with 1% Ts RMS jitter. The jitter tolerance in the proposed design is 10 dB in comparison with the conventional design and same loop filter.

5. CONCLUSION

This chapter describes the contribution of this dissertation and explain the future works.

5.1 Summary of contribution

In this dissertation, the following topics associated with the wideband low-power continuous-time $\Sigma\Delta$ modulator were studied in detail, and two main project is designed, implemented and tested.

The detail contribution for first project is as follows:

- A thorough trade-off study was made determining different system-level parameters, based on the considerations of the power consumption, dynamic range requirement, linearity, OpAmp limited GBW and ELD sensitivity.
- The GD algorithm is used to extract loop gain transfer function coefficients.
- A quantization noise reduction technique is employed to improve the SQNR of the modulator using a 7-bit embedded quantizer.
- A fast path feedback topology is proposed which uses an analog differentiator in order to compensate excess loop delay, so it relaxes the requirements of the amplifier placed in front of the quantizer.
- The modulator is implemented using a third order loop filter with a feed-forward compensation paths and a 3-bit quantizer in the feedback loop.
- In order to save power and improve loop linearity two-stage class-AB amplifier is developed

- The fully differential prototype modulator is implemented in $0.13\mu m$ CMOS technology, and layout technique such as interdigitizing and common center are used.

- Prototype chip tested using 4 layer board to have large ground and vdd layer.

- Combining all the above techniques, the modulator achieved peak SNDR of 67.5dB while consuming total power of 8.5-mW under a 1.2V supply with an over sampling ratio of 10 at 300MHz sampling frequency.

- The prototype achieves Walden's Figure of Merit (FoM) of $146fJ/step$

The detail contribution for second project is as follows:

- A thorough trade-off study was made determining different system-level parameters, based on the considerations of the power consumption, dynamic range requirement, linearity, OpAmp limited GBW and clock jitter sensitivity.

- This dissertation proposes to divide the loop filter in two parts, digital and analog part to overcome the sensitivity of feedback DAC to clock jitter.

- By using the digital first order filter after the quantizer, as one pole of the loop filter is implemented digitally, the power and area are reduced by minimizing active elements, moreover having more digital elements in loop of CT-$\Sigma\Delta$M makes it less sensitive to process, voltage and temperature variations.

- We proposed the use of a single DAC with a current divider to implement the feedback coefficients instead of two DACs to decrease area and routing.

- The prototype is implemented in TSMC 40nm technology and occupies $0.06mm^2$ area.

- Prototype chip tested using 4 layer board to have large ground and vdd layer.
- The proposed solution consumes about 7.5mW, and operates at 500MS/s. In a 10MHz bandwidth, the dynamic range(DR), maximum signal to noise ratio(SNR), and maximum signal to noise and distortion(SNDR) ratios in presence of 10% total jitter are 67dB, 63dB, and 62dB

5.2 Future work

To improve the performance of this work several issues need to be considered:

- On chip PLL needs to be designed in order to have low jitter and improve the measurment results performance
- For jitter tolerant ADC, full filter operation can be done in digital domain and just high gain implementation can be implemented by analog filter.
- Other DAC shapes such as SCR or SSI can be used to see effect of jitter tolerant technique in other DAC shapes.
- For calibration ADC, OpAmp, quantizer and DAC performance needs to improve to make the dominant noise, quantization noise.

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