

DEVICE DESIGN PARAMETERIZATION OF III-V MULTI-GATE FETS

A Dissertation

by

JAE WOO SUH

Submitted to the Office of Graduate and Professional Studies of  
Texas A&M University  
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Chair of Committee,	H. Rusty Harris
Committee Members,	Gregory H. Huff
	Philip Hemmer
	Rupak Mahapatra
Head of Department,	Miroslav M. Begovic

December 2016

Major Subject: Electrical Engineering

Copyright 2016 Jae Woo Suh

## ABSTRACT

The use of group III-V semiconductor materials promise superior performance compared to silicon and can be considered a fundamental paradigm shift away from mature silicon technology. Group III-V semiconductors allow for high power operation, drastically high clock speeds, large breakdown fields, and higher Johnson's Figure of Merit (JFoM). Due to higher electron drift velocity ( $v_d$ ) of the material set, higher on-state current ( $I_{on}$ ) is expected than the one in silicon with reduced supply voltage operation. Additionally, strong spontaneous and piezoelectric polarization properties in the III-Nitrides support tighter carrier confinement with high carrier density in a quantum well channel at the heterointerface. By engineering the III-nitride properties, designing a 3D architecture device includes important physical parameters that must be taken into account to analyze device performance. GaN-based devices are desirable for high RF and high power applications for reducing parasitics and improving efficiency. For this reason, III-nitride semiconductor materials provide the possibility of future integration of GaN fin-based 3D devices.

This dissertation describes the experimental realization and electrical analysis of III-V FinFET devices with an AlGaIn/GaN heterostructure, called "Multi-Gate Heterostructure Fin Field Effect Transistor (MUG-HFinFET)." Process development begins with the experimental demonstration of a Si-compatible baseline AlGaIn/GaN FinFET technology, and an exploration of the impact of physical device design parameters such as fin widths, heights, angles and gate lengths. The ohmic contact formation on

AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure is realized using different metal stacks while taking into account additional annealing effects and produces comparably low contact resistance to other literature reports. Different fabrication processes to distinguish the impact of the device architectures are demonstrated while simultaneously applying for the integration of high-k dielectric metal-gate stack including surface clean and passivation techniques developed for high quality interfaces and low-leakage performance. After MUG-HFinFET technology is implemented and characterized, the impacts of the device design parameters are benchmarked and shows the guidance to device design at the initial stage forward proper device application. The work concludes by assessing the novel characteristics of AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure FinFET devices for 3D device design with distinguished performance. According to the distinguished performance across the device geometries and crystal directions, the benchmarks made in this dissertation will guide future device application development toward an AlGa<sub>N</sub>/Ga<sub>N</sub> FinFET device design to ensure that a proper device design is achieved.

To my family, Heijoung Kim, Leah Hyuna Suh, Anna Younga Suh ...  
my parents, Hangoun Seo, Jungrye Choi, and my brother, Jaegon Seo...

You are more than everything. I love you and remember.

I sincerely thank you forever...

## ACKNOWLEDGEMENTS

I would like to thank my advisor and committee chair, Dr. H. Rusty Harris, for his advice, guidance, and support. His careful approach and pursuit of perfection on the research work deserves my sincere deep respect. It was possible to accomplish this project with his encouragement and his ability to challenge me while still providing excellent guidance. I appreciate the opportunity that he has provided me and the confidence he had in me to accomplish this.

I want to express my gratitude to my committee members, Dr. Phillip Hemmer, Dr. Rupak Mahapatra, and Dr. Gregory Huff for giving their guidance and support through the course of this research. They have my greatest appreciation for offering their valuable support and insightful advice to complete this project. Special thanks to Dr. Edwin L. Piner of Texas State University for his significant contribution and support.

I truly thank the ECEN department and AggieFab staffs for making this research accomplishable. Thanks to Dennie Spears, Jim Gardener, Rebert Atkins, and Larry Rehn for years of supporting and maintain AggieFab with their time and help. Their given support enabled this research and will be remembered sincerely.

Thanks to all my colleagues and friends, Jung Hwan Woo, Derek W. Johnson, Michael Babb, William Baker, Pranav Sharma, Feyza Berber, Alexandre Yamamoto, and Fahad Al Ghannam for their help and friendship through the years.

Finally, I would like to most warmly thank my family. None of this would have been possible without the love, belief, and support of my family. Thanks to my wife, Hei-

Joung and daughters, Leah Hyuna, Anna Younga, for encouragements with endless belief and hope. Thanks to my parents, Hangoun and Jungrye, who always deserve my most respect throughout my life. It was a long journey which was made possible only because of them. I sincerely appreciate their support and belief and will forever. Thanks to my brother, Jaegon, for pushing me forward and being the only one in my life. My love always be into my family. It is only by you, Jesus, through your love and guidance, I can stand here.

## NOMENCLATURE

ALD	Atomic Layer Deposition
AlGaN	Aluminum Gallium Nitride
DI	Deionized
DIBL	Drain induced barrier lowering
$E_c$	Critical breakdown electric field
$E_g$	Bandgap energy
EBL	Electron beam lithography
GaN	Gallium Nitride
$h$	Plank constant
HEMT	High electron mobility transistor
$I_d$	Drain current
ICP-RIE	Inductively coupled plasm-reactive ion etching
IPA	Isopropyl Alcohol
I-V	Current-voltage measurement
$k$	Boltzmann constant
$m^*$	Effective mass of electron
MIBK	Methyl isobutyl ketone
$n_i$	Intrinsic electron density
$P_p$	Total polarization
$P_{PE}$	Piezoelectric polarization

$P_{SP}$	Spontaneous polarization
PDA	Post-deposition anneal
PECVD	Plasma enhanced chemical vapor deposition
$q$	Magnitude of electron charge
$R_C$	Contact resistance
$R_{ON}$	ON-state resistance
SCE	Short channel effect
SEM	Scanning electron microscope
Si-CMOS	Silicon complementary metal-oxide-semiconductor
SS	Subthreshold swing
T	Temperature
TLM	Transfer length method
$V_{BR}$	Breakdown voltage
$V_d$	Drain voltage
$V_g$	Gate voltage
$v_{sat}$	Saturation velocity of electrons
$V_{th}$	Threshold voltage
$\Theta_K$	Thermal conductivity
$\epsilon_j$	Components of the strain field
$\epsilon_r$	Relative electric permittivity
$\epsilon_0$	Electric permittivity of vacuum
$\mu_n$	Mobility of electrons



## TABLE OF CONTENTS

	Page
ABSTRACT .....	ii
ACKNOWLEDGEMENTS .....	v
NOMENCLATURE .....	vii
TABLE OF CONTENTS .....	ix
LIST OF FIGURES .....	xi
LIST OF TABLES .....	xvii
CHAPTER I INTRODUCTION .....	1
Literature review .....	4
Proposed device.....	9
CHAPTER II PROCESS DEVELOPMENT AND OPTIMIZATION FOR III-NITRIDE HIGH ELECTRON MOBILITY MULTI-GATE FINFET .....	13
Introduction .....	13
Surface cleaning and preparation .....	15
S/D Ohmic contact modules.....	17
AlGaIn/GaN heterostructure mesa isolation and formation .....	20
AlGaIn/GaN fin formation using fluorine based ICP-RIE .....	23
Gate contact module.....	26
CHAPTER III ELECTRICAL CHARACTERIZATION OF III-NITRIDE HETEROSTRUCTURE FINS AND SIMULATION FOR STRAIN PROFILE IN THE FINS .....	28
Introduction .....	28
Impacts on S/D contact resistance due to fabrication process variation .....	29
Two possible conduction paths investigation using I-V characteristic .....	31
Simulation for strain profile in the heterostructure fins .....	34
Electrical measurement and simulation/calculation results on 2DEG density.....	39

CHAPTER IV MASK REGISTRATION AND LITHOGRAPHY PLATFORM PORTABILITY FOR III-NITRIDE HETEROSTRUCTURE FINS PROTOTYPING ..	43
Introduction .....	43
Prototyping of III-nitride FinFET device fabrication.....	45
Electrical characterization results of the III-nitride FinFET .....	48
CHAPTER V ENHANCEMENT MODE ALGAN/GAN FINFET AND ADDITIVE STRAIN EFFECT .....	52
Introduction .....	52
Device channel width down-scaling and passivation using PECVD on AlGaIn/GaN FinFET .....	53
CHAPTER VI ALGAN/GAN FINFET DESIGN PARAMETER EFFECT ON THE DEVICE CHARACTERISTICS .....	63
Introduction .....	63
Fin sidewall control using the combination of RIE and wet etching process .....	64
Effect on electrical characterization based on AlGaIn/GaN FinFET design parameters .....	77
Non-via fabrication process for simpler device fabrication and less cost.....	87
CHAPTER VII CONCLUSION .....	103
REFERENCES .....	107
APPENDIX A .....	114

## LIST OF FIGURES

	Page
Figure 1. (a) An alternate transistor design architecture, FinFET, (b) Drain induced barrier lowering (DIBL) and subthreshold swing (SS) versus channel length ( $L_g$ ) for multi-gate and planar-silicon nFET. ....	1
Figure 2. Improved performance gain of III-V semiconductor material device over Si-based FinFET. ....	3
Figure 3. The origin of the FinFET from planar FET: (left) Thin-body MOSFET to (center) Double-gate (DG) FET and (right) Modern 3D FinFET. ....	4
Figure 4. Spontaneous polarization formed in GaN due to asymmetry crystal structure, and piezoelectric polarization induced by mechanical strain due to lattice mismatch in the heterostructure, leads to the formation of 2DEG at the heterointerface. ....	5
Figure 5. JFoM comparison of various high speed and high power semiconductor materials. ....	6
Figure 6. (a) DIBL vs Gate length ( $L_g$ ) and (b) DIBL vs Channel width ( $W_{ch}$ ) for the comparison of different semiconductor materials' FinFET for $W_{ch} = 30$ nm, $L_g = 45$ nm, and $t_{ox} = 2$ nm. ....	7
Figure 7. Transistor fin profiles of (a) AlGaIn/GaN fin with flat/round top and slope on sidewall, (b) with flat top and vertical sidewall, (c) <i>Intel's</i> 1 <sup>st</sup> and 2 <sup>nd</sup> generations with different height and slope. ....	8
Figure 8. Corner rounding FinFET device profile to reduce corner effects. ....	10
Figure 9. Proposed device schematics of a III-V semiconductor FinFET and cross-sectional view of the FinFET which has a main 2DEG channel region near the interface and two possible conductive channels along the fin sidewalls. ....	11
Figure 10. (a) Possible fin sidewall design with different angles. (b) Possible electron energy band diagram for AlGaIn/GaN heterostructure. Possible charge density associated with each interface is shown. ....	12
Figure 11. An overall device schematic and cross-section of Au-free, gate-last AlGaIn/GaN heterostructure FinFETs. ....	14

Figure 12. Two different contact openings for source and drain regions after SiN <sub>x</sub> etching on windows patterned by EBL, (top) only contact openings and (bottom) contacts with fins openings.....	16
Figure 13. A schematic of planar ohmic contact formation and optical image after ohmic metallization. ....	17
Figure 14. Plot of normalized resistance versus TLM spacing for the metallic stack of Ti / Al / Ni / Au ohmic contact. Inset: linear I-V plot for the structure.....	18
Figure 15. Plot of normalized resistance versus TLM spacing for the metallic stack of Ta / Al / Ta ohmic contact. Inset: (top) logarithm I-V plot for the structure, (bottom) SEM image for the distance measurement. ....	19
Figure 16. A schematic of the mesa-etch process using Cr and SiN <sub>x</sub> etch stop masks with fluorine based ICP-RIE. ....	21
Figure 17. The cross-sectional SEM of AlGa <sub>N</sub> /Ga <sub>N</sub> heterostructure after 7 minutes dry etching at 44 mTorr and 13 °C with 40 sccm SF <sub>6</sub> and 10 sccm Ar at RF power of 200 W with ICP power of (a) 250 W, (b) 300 W, and (c) 350 W.....	22
Figure 18. Top-view SEM image of the multi-fins between ohmic contacts .....	24
Figure 19. A cross-sectional SEM image of the fin structure and the compositing layers in the heterostructure.....	24
Figure 20. A cross-sectional TEM image of a fin heterostructure with a flat plane top region using Cr/SiN <sub>x</sub> etch stop masks. ....	25
Figure 21. A cross-sectional TEM image of a collapsed fin heterostructure due to high ICP power confinement along the edge of the etch stop masks. ....	25
Figure 22. A SEM image of Au/Ni metal stack gate on top of a gate dielectric and an AlGa <sub>N</sub> /Ga <sub>N</sub> fin heterostructure.....	27
Figure 23. Variation of the contact resistance for different Ta/Al/Ta ohmic metallization ratio with different pre-cleaning methods is obtained by using TLM structure at various annealing temperatures. ....	30
Figure 24. I-V characteristic of recess-etched Ga <sub>N</sub> region. ....	32
Figure 25. The log current level difference from the I-V measurements for the regions with and without fins. ....	33
Figure 26. Numerical simulation results for strain profiles (a) in-plane biaxial strain, ε <sub>xx</sub> , profile of a nano fin Ga <sub>N</sub> /AlGa <sub>N</sub> /Ga <sub>N</sub> heterostructure. The red color	

represents tensile strain and the blue color represents compressive strain. It shows a very abrupt change at the interfaces, (b) growth axis strain,  $\epsilon_{zz}$ , profile indicates possible structural deformation along the fin sidewalls.....35

Figure 27. In-plane biaxial stain profile along the AlGa <sub>N</sub> layer near the AlGa <sub>N</sub> /Ga <sub>N</sub> interface as a function of fin widths. ....	36
Figure 28. Maximum in-plane biaxial strain variation due to fin widths variation. ....	37
Figure 29. Simulated 2DEG sheet density profile, $n_{sh}(x)$ , as a function of position along the fin widths in the Ga <sub>N</sub> /AlGa <sub>N</sub> /Ga <sub>N</sub> heterostructure.....	38
Figure 30. Experimentally measured 2DEG sheet density versus different fin widths of Al <sub>0.26</sub> Ga <sub>0.74</sub> N/Ga <sub>N</sub> heterostructure. ....	40
Figure 31. The square profile represents the effective and the actual profile represents the real 2DEG density profile in the fin by the simulation.....	41
Figure 32. III-nitride heterostructure etch process using two etch stop masks, Cr(M1)/SiN <sub>x</sub> (D1).....	46
Figure 33. Registration marks at the beginning of the overall process using high atomic weight number material. ....	47
Figure 34. Fin patterning using EBL aligning to registration marks and predefined S/D contact metal.....	47
Figure 35. Ability of common Si-CMOS like gate-first and -last process and overall device view with well-defined gate, drain, and source regions.....	47
Figure 36. Extracted contact resistance ( $R_c$ ), as a function of annealing temperature for Ta/Al/Ta ohmic contact for S/D. Inset: Normalized resistance as a function of linear TLM spacing.....	49
Figure 37. (a) DC $I_{ds} - V_{ds}$ output characteristics of the AlGa <sub>N</sub> /Ga <sub>N</sub> FinFET fabrication prototyping with Au-free contacts. (b) Subthreshold currents as a function of gate voltage. ....	51
Figure 38. Top view of 34 nm of AlGa <sub>N</sub> /Ga <sub>N</sub> fin width, measured by SEM. ....	53
Figure 39. PECVD grown SiN <sub>x</sub> passivated nano fin of AlGa <sub>N</sub> /Ga <sub>N</sub> structure, imaged by SEM. ....	54
Figure 40. $I_d - V_d$ curves of the AlGa <sub>N</sub> /Ga <sub>N</sub> FinFET before and after PECVD grown SiN <sub>x</sub> passivation. $\Delta I_{d,max}$ is 147 mA/mm. ....	55

Figure 41. A comparison of $V_{th} - W_{fin}$ curve of the AlGaIn/GaN FinFET before and after PECVD grown $SiN_x$ passivation. ....	56
Figure 42. $I_{d,max} - W_{fin}$ and $g_{m,max} - W_{fin}$ curves of the AlGaIn/GaN FinFET before and after PECVD grown $SiN_x$ passivation. There are overall $I_{d,max}$ increase and transconductance, $g_{m,max}$ , after the passivation. $I_{d,max}$ and $g_{m,max}$ are measured at $V_d = 3 V$ and $V_g = 0.6 V$ . ....	57
Figure 43. Before and after passivation effect on the 34 nm fin shows an ohmic behavior reconstruction. ....	58
Figure 44. Effective 2DEG density curves of AlGaIn/GaN FinFET before and after PECVD grown $SiN_x$ passivation ....	59
Figure 45. Contact resistance dependency on the fin width variation with the process and calculation error. Red line indicates a corrected contact resistance along with the fin width variation. ....	61
Figure 46. Contact resistance effect on the 2DEG density of AlGaIn/GaN device. ....	62
Figure 47. Fabricated fin structure mapping on AlGaIn/GaN on Si (111) substrate. This substrate shows induced dislocation growth along the crystal direction after 25 % TMAH etching for approximately 17 hours. ....	65
Figure 48. AlGaIn/GaN fin formation along $\langle 11\bar{2}0 \rangle$ crystal direction after ICP-RIE process for 5 minutes. ....	66
Figure 49. AlGaIn/GaN fin formation along $\langle 01\bar{1}0 \rangle$ crystal direction after ICP-RIE process for 5 minutes. ....	67
Figure 50. TEM image of the cross-sectional view of a fin along with the crystal direction of $\langle 01\bar{1}0 \rangle$ . Measured fin sidewall internal angle is $63^\circ$ . ....	68
Figure 51. TEM image of the cross-sectional view of a fin with the sidewall collapse issue. ....	68
Figure 52. AlGaIn/GaN fin formation along $\langle 1\bar{1}00 \rangle$ crystal direction after ICP-RIE process for 5 minutes. ....	69
Figure 53. (a) Hexagonal unit cell of GaN wurtzite structure with crystallographic directions and (b) its basal planes. ....	70
Figure 54. Fin profiles taken by SEM after 25 % TMAH additional different etch process time at $85^\circ C$ with the fins along with the crystal direction of $\langle 11\bar{2}0 \rangle$ . ....	71

Figure 55. Triangular shape of fin formation progress with additional etching time and with crystal orientation preference along the direction of $\langle 11\bar{2}0 \rangle$ .....	73
Figure 56. SEM image of the cross-sectional fin image after 10 minutes 25 % TMAH etching process and it shows clear effect on the fin sidewall angle along the direction of the crystal orientation (top etch mask (Cr) / second etch mask ( $\text{SiN}_x$ / $\text{SiO}_2$ ) over AlGaIn/GaN fin structure) .....	75
Figure 57. Graphical schematic illustration for the steps from bare AlGaIn/GaN substrate before ICP-RIE mesa isolation process to AlGaIn/GaN fin structure with different sidewall angles after ICP-RIE and subsequent TMAH wet etching process. ....	76
Figure 58. A schematic of AlGaIn/GaN FinFET device is depicted including the via connection.....	78
Figure 59. An output characteristic of $I_d - V_d$ versus $V_g$ , and transfer characteristics of $I_d$ , $I_s$ , $I_g - V_g$ and $g_m$ profiles.....	80
Figure 60. Output characteristics of $I_d - V_d$ versus $V_g$ after additional annealing process from top-left to bottom-right at no anneal, 575 °C, 675 °C, and 755 °C, respectively.....	81
Figure 61. Transfer characteristics of $I_d$ , $I_s$ , $I_g - V_g$ at three different $V_d = 0.5$ V, 5.25 V, and 10 V after additional annealing process at no anneal, 575 °C, 675 °C, and 775 °C, respectively. (figures from top-left to bottom-right) .....	83
Figure 62. Transfer characteristics of $I_d$ , $I_s - V_g$ at three different $V_d = 0.5$ V, 5.25 V, and 10 V after additional annealing process at no anneal, 575 °C, 675 °C, and 755 °C, respectively. ....	84
Figure 63. Transfer characteristics of $I_g - V_g$ at three different $V_d = 0.5$ V, 5.25 V, and 10 V after additional annealing process at no anneal, 575 °C, 675 °C, and 775 °C, respectively.....	85
Figure 64. I-V characteristic of the fine before and after the $\text{SiN}_x$ passivation.....	86
Figure 65. AlGaIn/GaN FinFET device scheme is illustrated. It reduces additional steps in fabrication processes so as for device fabrication cost and time.....	88
Figure 66. Output characteristic of $I_d - V_d$ versus $V_g$ of AlGaIn/GaN FinFET using reduced fabrication process. As $W_{\text{fin}}$ increases $I_d$ increases. ....	89
Figure 67. Transfer characteristics of $I_d - V_g$ in linear and logarithm scale and $g_m - V_g$ at $V_d = 10$ V of AlGaIn/GaN FinFET using reduced fabrication process. ....	90

Figure 68. Threshold voltage versus fin width (EBL mask file layer dimension) .....	92
Figure 69. Electrical output and transfer characteristics of 3 different fin heights device ( $H_{fin} = 70, 110, \text{ and } 160 \text{ nm}$ from the top to bottom). .....	94
Figure 70. Fin height effects on DIBL. ....	95
Figure 71. Electrical output and transfer characteristics based on gate length variation .	96
Figure 72. (Continued from Figure 70) Electrical output and transfer characteristics based on gate length variation .....	97
Figure 73. Gate length effect on the output current. ....	98
Figure 74. Measured DIBL effect on different gate length FinFET device. ....	99
Figure 75. Electrical output and transfer characteristics of vertical sidewall shape AlGaIn/GaN FinFET device. ....	101
Figure 76. Simulated in-plane biaxial strain profile variation due to the fin sidewall angle variation within a 2DEG width of 50 nm. ....	102
Figure 77. Normalized device performance comparison of fabricated AlGaIn/GaN FinFETs parallel to the crystal orientation. ....	104
Figure 78. Normalized device performance comparison based on the device design parameters of fabricated AlGaIn/GaN FinFETs. ....	105

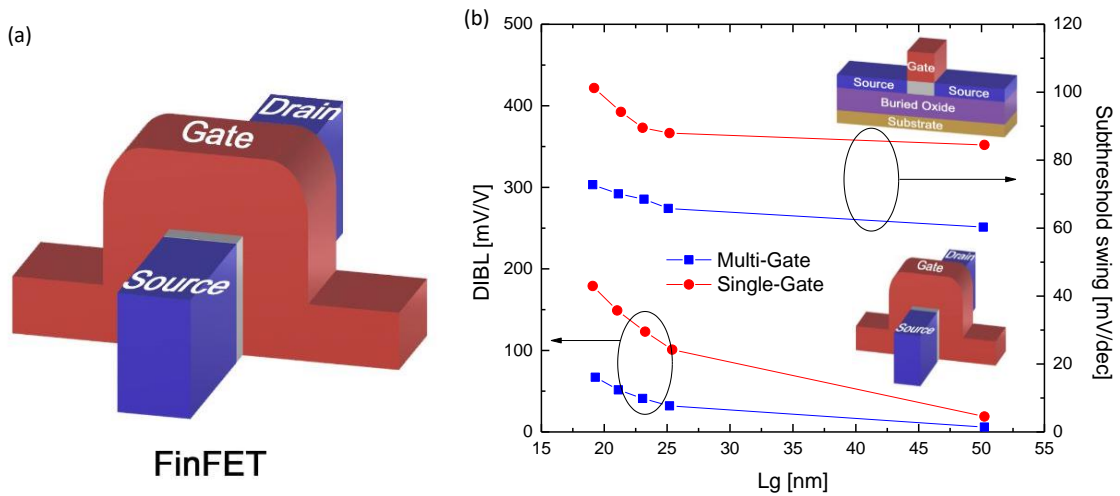


## LIST OF TABLES

	Page
Table 1. Physical properties of different semiconductor materials .....	2

CHAPTER I  
INTRODUCTION

The level of scalability on transistors has a practical interest in modern transistor technology because it has led to improved transistor performance and allowed for very large scale integration (VLSI) systems. Significant challenges have arisen in creating new transistor design architectures at smaller dimensions due to limitations on classical planar scaling and the material properties of silicon. Classical scaling faces obstacles such as high leakage current due to short-channel effects (SCEs), doping level variation, and process tool limitations. Alternative device structures have been introduced to overcome the previously mentioned obstacles experienced by classical planar transistor technology.



**Figure 1.** (a) An alternate transistor design architecture, FinFET, (b) Drain induced barrier lowering (DIBL) and subthreshold swing (SS) versus channel length ( $L_g$ ) for multi-gate and planar-silicon nFET.

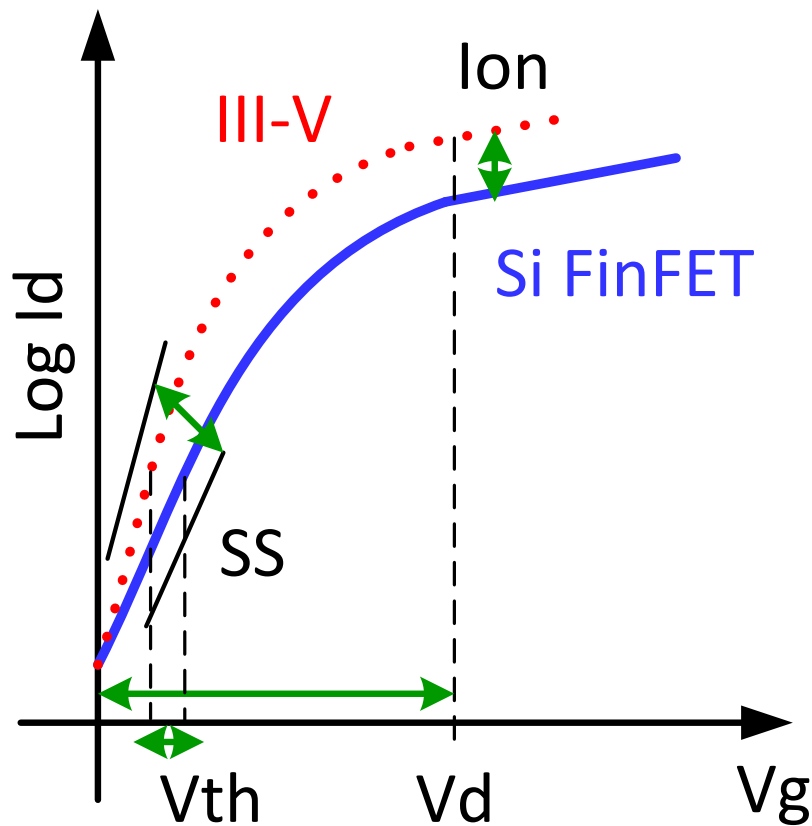
Multiple (two or three) gates field-effect transistors, generally referred to as FinFETs in Figure 1(a), are an alternate transistor design architecture with improved SCEs, reduced device variability, and improved volume inversion of channel regions without relevant fabrication process modification [1-3]. The multi-gate FinFETs, Figure 1(b), exhibit reduced DIBL effects and reduced subthreshold swing.

The use of group III-V semiconductor materials promise superior performance compared to silicon and can be considered a solution to scaling challenges. Group III-V semiconductor allows for higher power operation, drastically higher clock speeds, larger breakdown fields, and higher Johnson's Figure of Merit (JFoM), as shown in Table 1 [4].

**Table 1.** Physical properties of different semiconductor materials

Material	Si	GaAs	GaN	AlN
$E_g$ at 300 k (eV)	1.12	1.42	3.39	6.2
$\epsilon_r$	11.8	12.9	9	8.5
$\mu_n$ ( $\text{cm}^2/\text{V}\cdot\text{s}$ )	1350	8500	2000 (2DEG)	300
$v_{\text{sat}}$ ( $10^7$ V/cm)	1.0	1.5	2.5	1.4
$E_{\text{br}}$ (MV/cm)	0.3	0.4	3.3	15
$\Theta_k$ ( $\text{W}/\text{cm}\cdot^\circ\text{C}$ )	1.3	0.43	1.3	2.85
Melting Point ( $^\circ\text{C}$ )	1414	1238	2400	3200
Hardness (GPa)	11.5	7.0	13.4	11.8
JFoM (Normalized)	1	2.7	27.5	

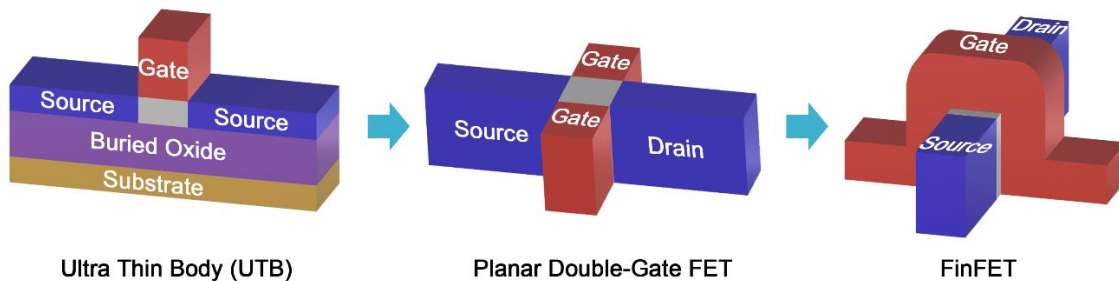
Also, due to higher electron velocity, a higher on-state current ( $I_{on}$ ) is expected in comparison to silicon with Group III-V semiconductors operating at a reduced supply voltage. Tight carrier confinement in quantum well channel makes sharp turn-on possible, which is indicated by subthreshold swing (SS), the reciprocal value of the subthreshold slope which is the ratio of transistor's logarithmic subthreshold drain current to gate voltage, in Figure 2 [5].



**Figure 2.** Improved performance gain of III-V semiconductor material device over Si-based FinFET.

## Literature review

In the 1990s, a new structure for the transistor was proposed by a UC Berkeley team led by Dr. Chenming Hu. The suggested structure was a thin-body MOSFET structure which could reduce SCEs and eliminate body doping. The structure results in higher drive current and reduced impact of random dopant fluctuations (RDF) so that leakage current could be suppressed [2, 3]. The proposed structures are shown in Figure 3.

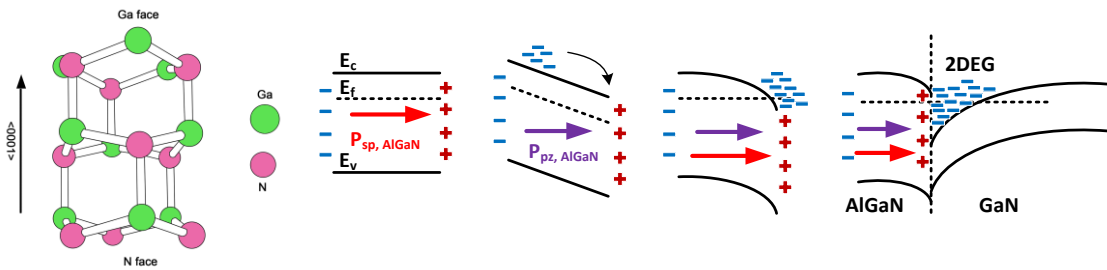


**Figure 3.** The origin of the FinFET from planar FET: (left) Thin-body MOSFET to (center) Double-gate (DG) FET and (right) Modern 3D FinFET.

The structures are possible by using standard complementary metal-oxide-semiconductor (CMOS) transistor processing technique as the gate module becomes self-aligned and the layout is similar to that of a planar FET. The new 3D design of a FinFET gives it more volume than a planar FET for the same area. This enables better control of the conducting channels by the wrapped gate and lower leakage current through the body, allowing for applications in high speed and power electronics. Despite the new device architecture, transistor scaling has become a problem again due to the limit of silicon material properties and the extremely short channel lengths of FinFETs becoming smaller

than 10 nm. Therefore, new channel materials such as III-V compound semiconductor materials can be introduced due to much higher carrier velocity and breakdown electric field than those in Si.

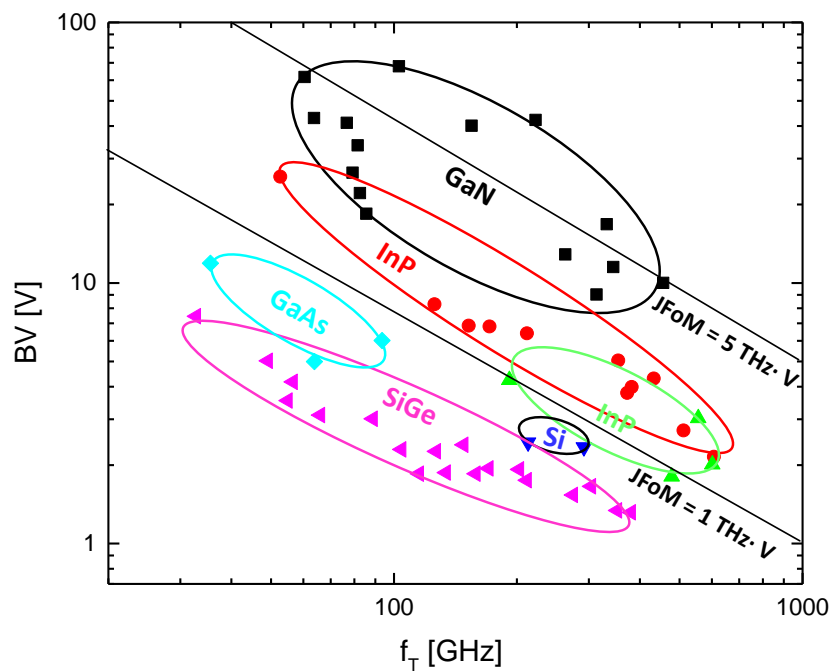
With these excellent properties, the III-V material system especially such as III-Nitride makes it possible to continue improving device performance. The III-Nitride system here with GaN has a high density of states at the quantum well formed at the interface with additional hetero-epitaxial layer of AlGaN which is a large potential barrier as well. This large potential barrier supports the formation of a high free carrier density of 2-dimensional electron gas (2DEG) in the quantum well channel at the heterointerface and near GaN layer [4]. GaN-based transistors strongly rely on inherent polarizations in III-Nitride heterostructure system. GaN has an intrinsic asymmetry of the bonding and electronegativity in the equilibrium wurtzite crystal structure inducing dipoles so that it leads to the formation of a spontaneous polarization in the structure. In addition to the spontaneous polarization, piezoelectric polarization can be induced by strained films due to lattice mismatch in the AlGaN/GaN heterostructure interface. These two polarizations



**Figure 4.** Spontaneous polarization formed in GaN due to asymmetry crystal structure, and piezoelectric polarization induced by mechanical strain due to lattice mismatch in the heterostructure, leads to the formation of 2DEG at the heterointerface.

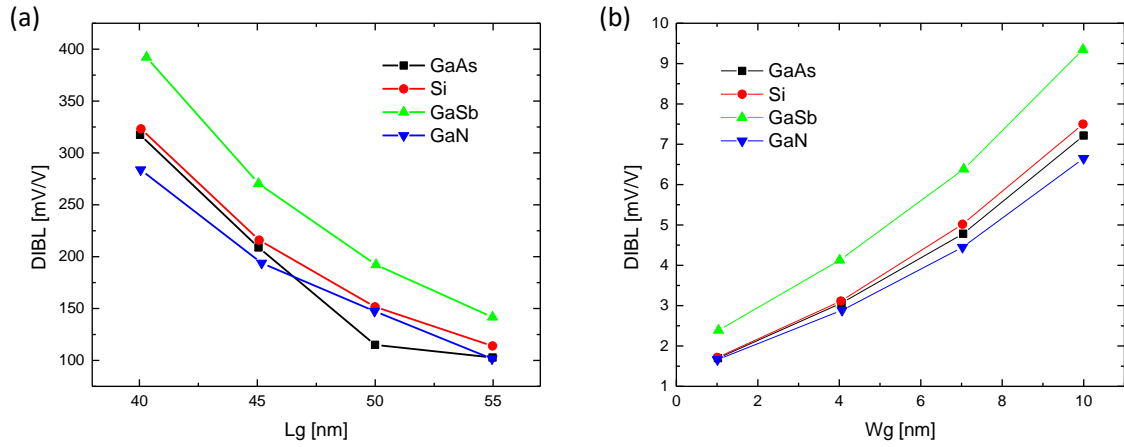
induce a high density of 2DEG in the quantum well near the interface, obtained by thorough heterostructure engineering. These special properties are shown in Figure 4 [6].

The excellent performance of AlGaN/GaN heterostructure transistors over other semiconductor materials are reported in the applications of high frequency and high power devices, as shown in Figure 5 [4].



**Figure 5.** JFoM comparison of various high speed and high power semiconductor materials.

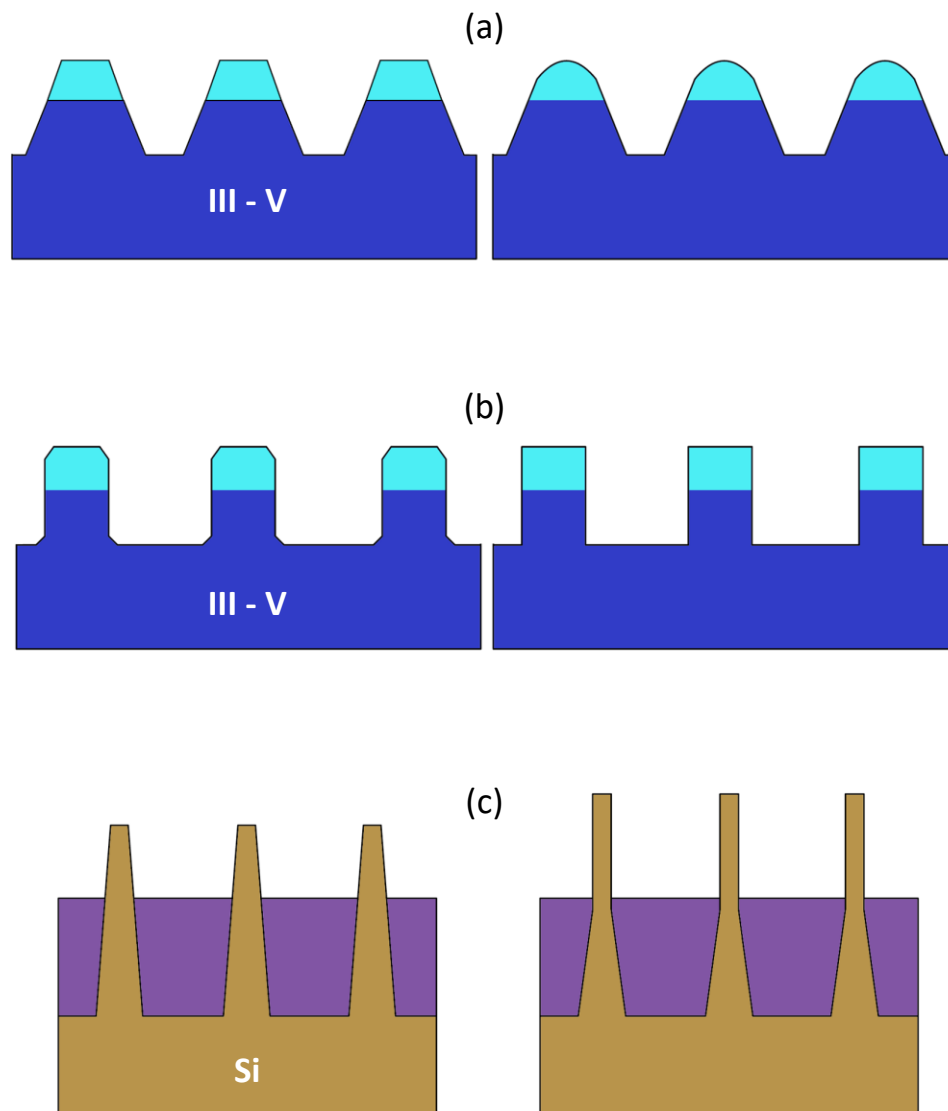
Among the different channel materials, GaN has the lowest drain induced barrier lowering (DIBL). Figure 6 shows that DIBL increases as the gate length ( $L_g$ ) decreases while it decreases as the channel width ( $L_w$ ) decreases [7]. From the results, GaN can be a good candidate to reduce SCEs.



**Figure 6.** (a) DIBL vs Gate length ( $L_g$ ) and (b) DIBL vs Channel width ( $W_{ch}$ ) for the comparison of different semiconductor materials' FinFET for  $W_{ch} = 30$  nm,  $L_g = 45$  nm, and  $t_{ox} = 2$  nm.

However, the impact of the fin design such as fin sidewall angle, height, width and pitch, has not been thoroughly reported and thus benchmarks do not exist to guide proper application design of III-V FinFET devices. Optimized processes for 3D transistor fin formation is extremely important to device characterization with reliable and repeatable product fabrication. Figure 7 shows previously reported fin designs [8, 9].





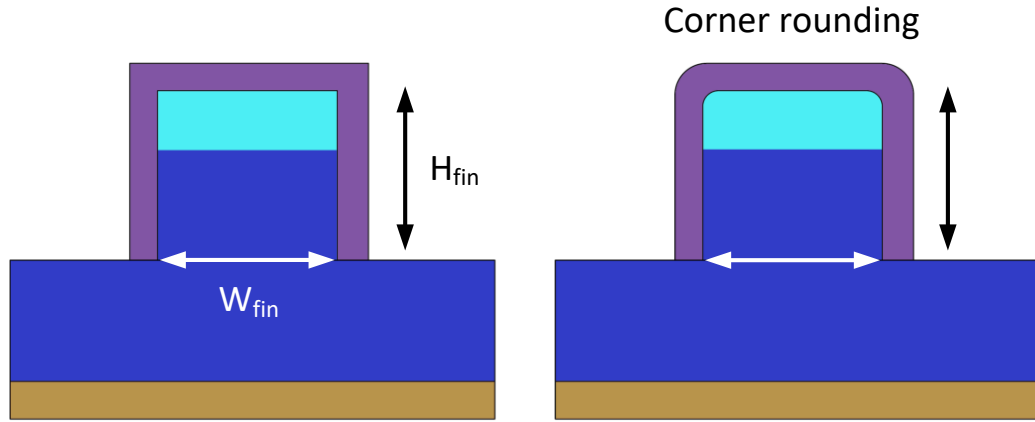
**Figure 7.** Transistor fin profiles of (a) AlGaIn/GaN fin with flat/round top and slope on sidewall, (b) with flat top and vertical sidewall, (c) *Intel's* 1<sup>st</sup> and 2<sup>nd</sup> generations with different height and slope.

## Proposed device

An alternate transistor design architecture, a FinFET, using III-V semiconductor materials (AlGaIn/GaN) is proposed which will greatly improve device performance. The goal of the proposed work is to fabricate and characterize AlGaIn/GaN FinFETs supporting higher on-state current ( $I_{d,on}$ ), lower off-state leakage current ( $I_{d,off}$  and  $I_{gs}$ ), and better transconductance ( $g_m$ ) and to look for the guidance of a device design space bounded by device characteristic tradeoff limit among the various device design factors as mentioned in the previous paragraph. By modulating fin design, inherent strain can be engineered in order to control 2DEG channel density internally and externally. In order to achieve this goal, nanoscale fin structure has to be well defined using electron beam lithography system (EBL), reactive ion etching (RIE), and additional chemical wet etching processes. Ohmic contact modules for source/drain (S/D) regions are developed for the reduction of series resistance in FinFET devices, and a gate contact module is implemented to exert better control over dense charge carrier transport through the FinFET.

The proposed work hypothesizes that effective 2DEG density profile is controlled by the fin sidewall angle, width, and height resulting in a strain modulated heterostructure. Control over fin geometry during the fabrication process affects residual strain at the hetero-interface or in the layers of the epitaxially grown III-V semiconductor materials. In general, mobile carrier density of a Si-based FinFET is higher in the corner at the subthreshold region due to higher electric field at sharp edges, which degrades the subthreshold slope so that threshold voltage ( $V_{th}$ ) is changed [10]. Furthermore, the corner

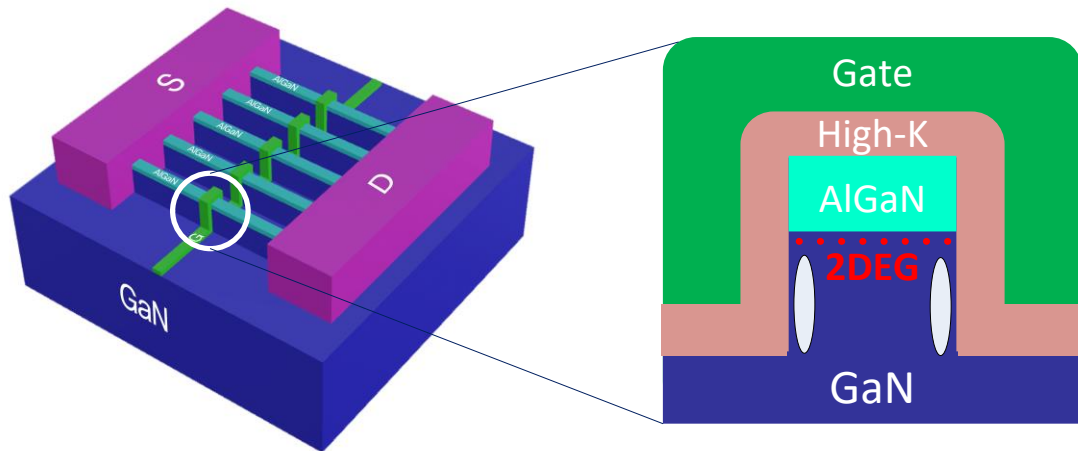
effects are more significant at high channel doping levels, thus directly affecting the device profile design [11-13], as shown in Figure 8.



**Figure 8.** Corner rounding FinFET device profile to reduce corner effects.

However, the channel of III-V devices has a separation from the corners due to a ternary III-V barrier which supports 2DEG quantum well near the heterointerface between the binary and ternary III-V materials, as shown in Figure 9.

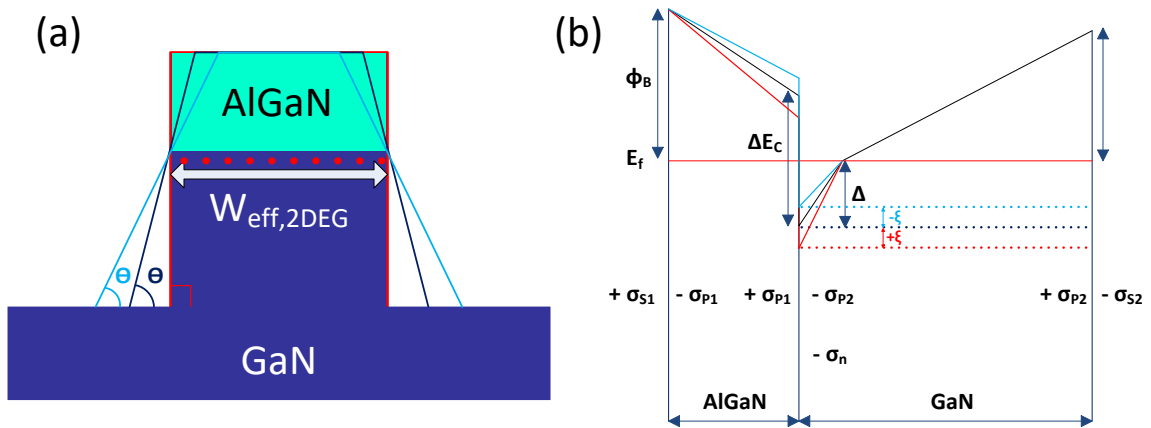
The epitaxial heterostructure of AlGaIn/GaN materials forms a channel quantum well at the interface with high density electrons,  $n_{sh} \geq 1 \times 10^{13} \text{ cm}^{-2}$ , due to wurtzite crystal structure and lattice mismatch between ternary and binary III-V materials. The high free 2DEG density is correlated with spontaneous and piezoelectric polarization due to the crystal structure and the lattice mismatch, respectively. The strain induced polarization charge density is affected by physical layer thickness, or volume, and composition of ternary III-V material.



**Figure 9.** Proposed device schematics of a III-V semiconductor FinFET and cross-sectional view of the FinFET which has a main 2DEG channel region near the interface and two possible conductive channels along the fin sidewalls.

The physical dimensions as well as electrical and crystal properties of regions containing ternary III-V materials are important to control. These variables directly impact the channel 2DEG density, and are also able to buffer out the corner effects, leading to a reduced effect on 2DEG regions with low electric field. Due to the ternary III-V layer between the gate dielectric, and the channel region, high electron mobility can be sustained because of the mitigated impact of interface roughness and reduced Coulomb scattering from the charged interface and bulk oxide states as well as remote phonon scattering from oxide phonons [14]. Effects of the fin sidewall roughness and surface states should be taken into account as well, leading us to consider the effects of the barrier dimensions and properties on 2DEG density. These effects highlight the importance of thickness and composition of ternary III-V material and fin design. Variations in these characteristics

change the strain profile inside fins, resulting in changes in 2DEG density and subsequently, electrical device performance characteristics. Strain control is the key factor in extracting effective 2DEG channel carrier density in the III-V FinFETs. Possible fin designs are depicted in Figure 10, as well as their predicted effect on the magnitude of the quantum well energy depth,  $\Delta \pm \xi$ , which determines the carrier density in the well channel.



**Figure 10.** (a) Possible fin sidewall design with different angles. (b) Possible electron energy band diagram for AlGaN/GaN heterostructure. Possible charge density associated with each interface is shown.

CHAPTER II  
PROCESS DEVELOPMENT AND OPTIMIZATION FOR III-NITRIDE HIGH  
ELECTRON MOBILITY MULTI-GATE FINFET\*

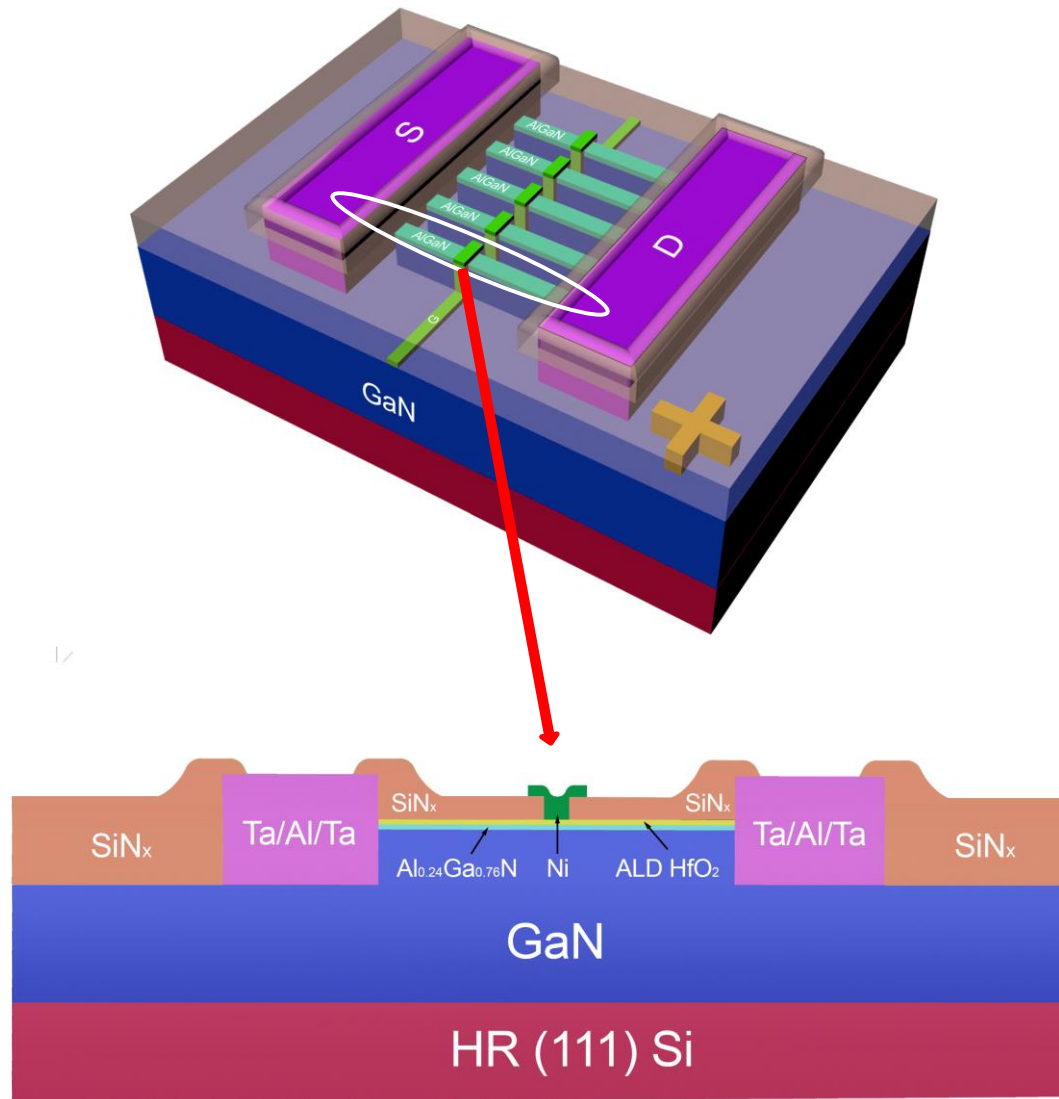
**Introduction**

In this chapter, the baseline AlGaIn/GaN FinFET process integration and performance are introduced and its initial results are discussed. The process integration employs a gate-last process flow including contact modules for source/drain and gate, AlGaIn/GaN fin formation using fluorine-based Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE), and high-k gate dielectric formation using Atomic Layer Deposition (ALD), resulting in depletion mode switching operation. The AlGaIn/GaN surface preparation and cleaning methods before an integration starts are introduced and discussed to ensure surface related processing steps while minimizing possible leakage paths. Au-based and Au-free metal schemes for source/drain ohmic contacts are applied to obtain lower contact resistance ( $R_c$ ), using Transfer Length Method (TLM) analysis extractions. AlGaIn/GaN fin isolation/formation is achieved using fluorine based ICP-RIE with two etch stop masks, Cr/SiN<sub>x</sub>, to avoid process encroachment on the fin geometry. Gate-module is explored with Au-based and Au-free metal schemes on ALD grown high-k

---

\*Part of this section is reprinted with permission from “Mask registration and lithography platform portability for nitride fin-based field effect transistors prototyping” by J. W. Suh, M. E. Babb, E. L. Principe, H.R. Harris, 2016. J. Vac. Sci. Technol. B, 34, 06k602, Copyright 2016 by American Vacuum Society.

dielectric layer,  $\text{HfO}_2$ . Figure 11 shows a device overview and a cross-section of a baseline AlGaN/GaN FinFET structure.



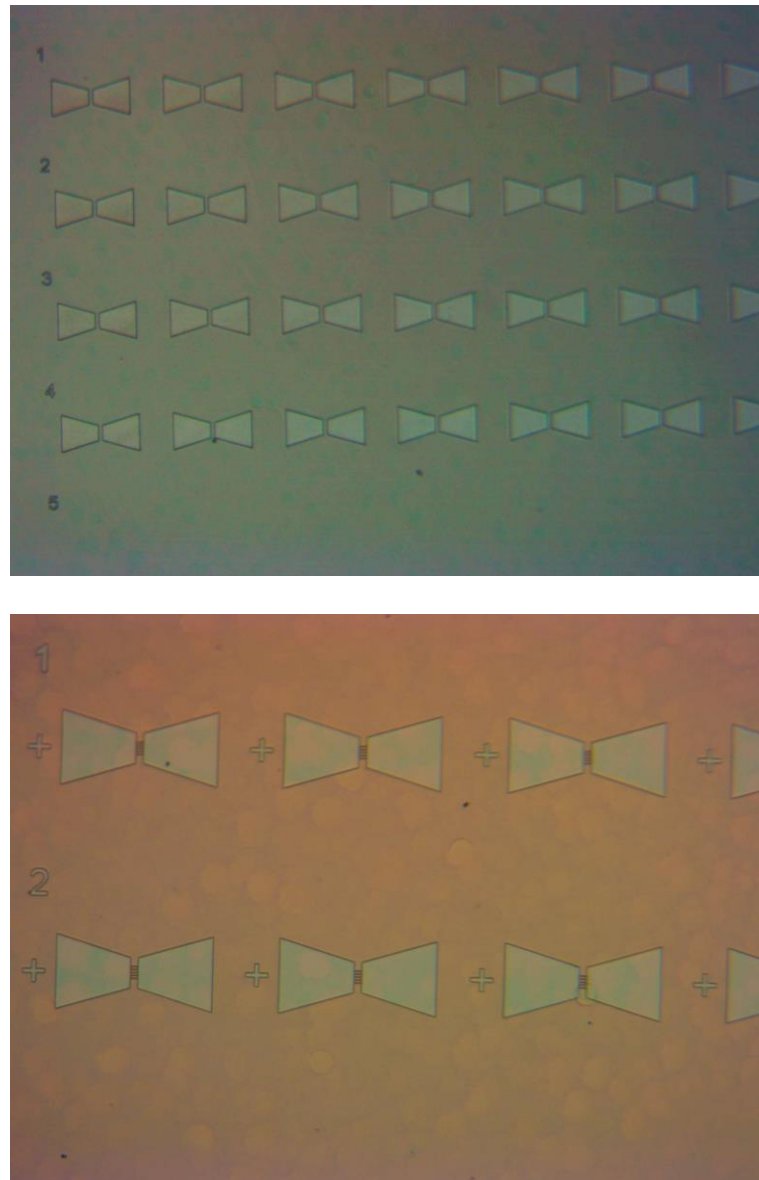
**Figure 11.** An overall device schematic and cross-section of Au-free, gate-last AlGaN/GaN heterostructure FinFETs.

## Surface cleaning and preparation

In order to analyze the electrical properties of the fin structure, low-resistance ohmic contacts in the AlGaIn/GaN heterostructure are required. Forming low-resistance ohmic contacts requires additional chemical surface treatments to improve interface properties prior to an initial metal deposition. These treatments are critical in preparing the heterostructure surface for ohmic contact formation as organic and oxide contamination is removed or reduced from the surface, which degrades ohmic contact quality. To achieve low-resistance ohmic contacts, the surface cleaning and preparation starts with substrate cleaning, surface passivation and S/D contact opening. The initial cleaning starts with a solvent clean (Acetone / IPA / DI water for 2 minutes each) to remove organic contaminants, and a 10 minutes dilute HCl clean at different ratios (HCl : DI H<sub>2</sub>O = 1 : 2, 1 : 5, 1 : 10) to strip off native oxide and a 5 minutes BOE clean to ensure the native oxide strip, followed by two DI H<sub>2</sub>O rinse cycles for 2 minutes each. Finally, the substrates are blown dry with N<sub>2</sub> and dehydrated in an oven at 135 °C for 10 minutes. Immediately after cleaning steps, the substrates are loaded into an Oxford Plasmalab 80 PECVD system to deposit 100 nm of SiN<sub>x</sub> with 125 sccm 1% SiH<sub>4</sub>/N<sub>2</sub>, 700 sccm N<sub>2</sub> flow rates at 350 °C of a table temperature, at 600 mTorr and an RF power of 15 W for surface passivation. The applications of PECVD grown SiN<sub>x</sub> passivation are reported as an effective surface barrier between atmospheric moisture and donor-like AlGaIn surface states which may cause improving the 2DEG channel carrier concentration, limiting current collapse and possibly virtual gate effects on the surface[15, 16]. The substrate is then patterned using TESCAN MIRA EBL system to open S/D contact regions and SiN<sub>x</sub>



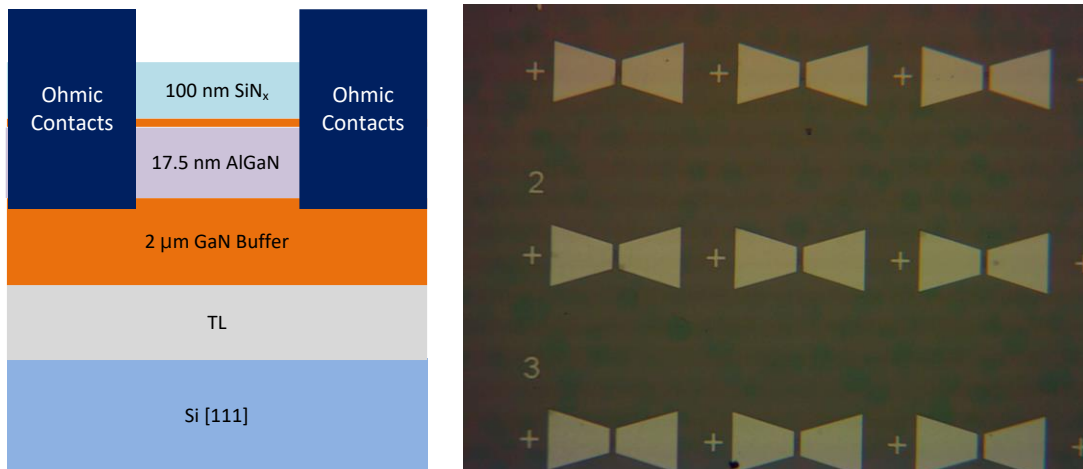
is etched away from the openings using BOE, shown in Figure 12. The EBL resist, PMMA, is left in place for a contact metal lift-off process after metal deposition.



**Figure 12.** Two different contact openings for source and drain regions after  $\text{SiN}_x$  etching on windows patterned by EBL, (top) only contact openings and (bottom) contacts with fins openings.

### S/D Ohmic contact modules

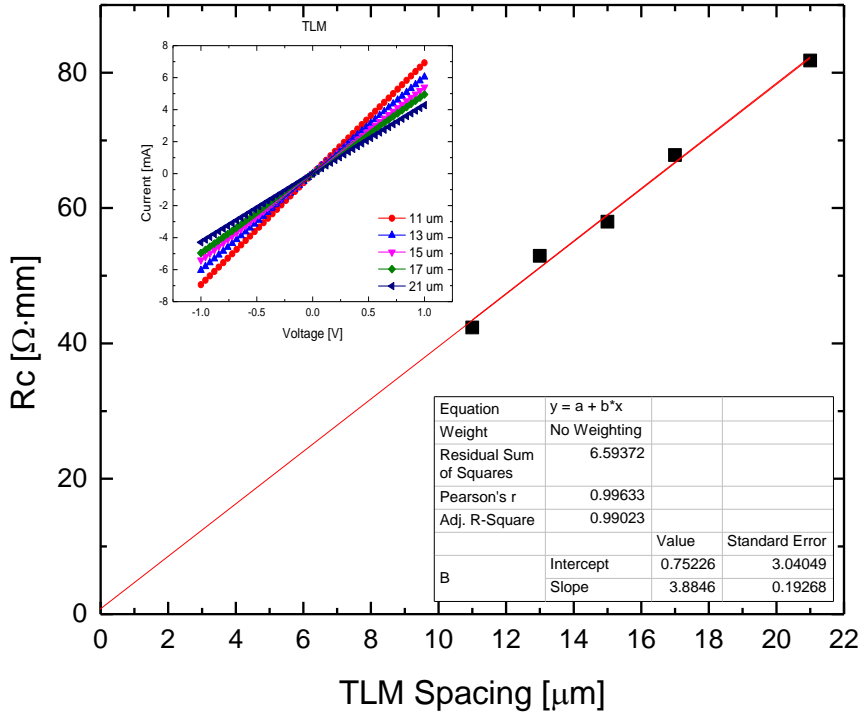
Au-based and Au-free ohmic contacts with different metallic scheme ratios of Ti / Al / Ni / Au [17-19] and Ta / Al / Ta metal stack are deposited using the Lesker PVD 75 electron beam (e-beam) evaporator. After lift-off process, the substrate is annealed in a MTI OTF 1200-X Rapid Thermal Processing (RTP) system for 30 seconds at 865 °C and for 240 seconds at 575 °C in N<sub>2</sub> ambient, respectively. Figure 13 shows a schematic of ohmic contact formation in the AlGaIn/GaN heterostructure and actual metal-stack deposited contacts before annealing process.



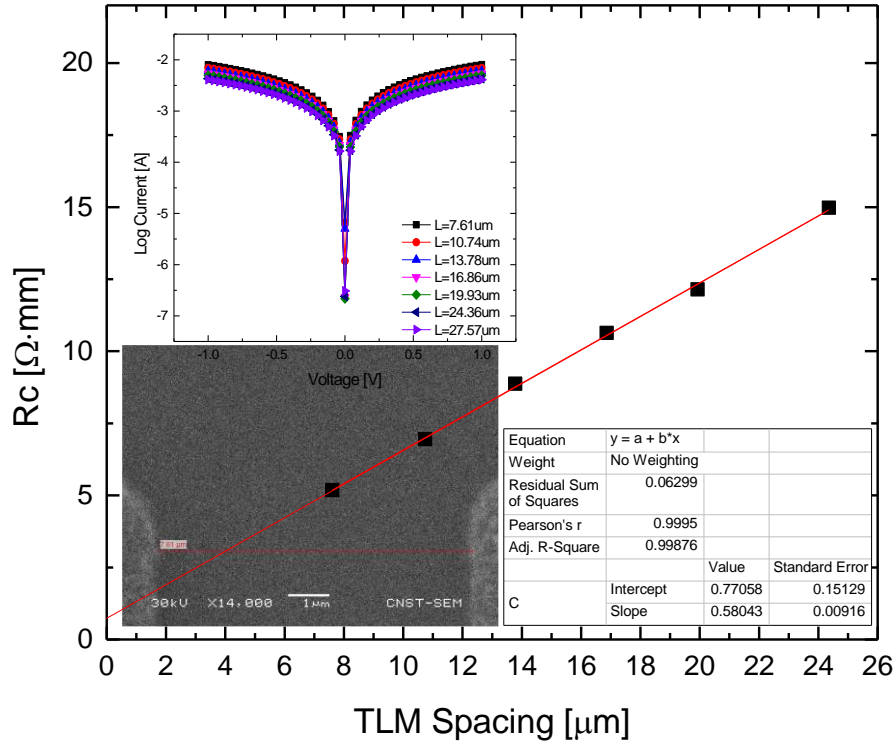
**Figure 13.** A schematic of planar ohmic contact formation and optical image after ohmic metallization.

Different metal stack ratios are used to find the lowest achievable contact resistance value in the HIPER lab at Texas A&M University. Figure 14 shows the normalized resistance versus TLM spacing plot using the metallic scheme of 30 nm / 180

nm / 40 nm / 50 nm of Ti / Al / Ni / Au. The metals are e-beam-evaporated but Au is sputtered for the non-mesa/planar AlGaN/GaN heterostructure. To form TiN bonds with Nitrogen atoms of GaN at the interface, titanium is deposited as the first layer and a thick aluminum is deposited so as to support a low resistance and is believed to do a main role to have an ohmic behavior in the stack. Nickel prevents top gold diffusion into lower aluminum layer during the annealing process and the top gold layer prevents oxidation of the contact metals.



**Figure 14.** Plot of normalized resistance versus TLM spacing for the metallic stack of Ti / Al / Ni / Au ohmic contact. Inset: linear I-V plot for the structure.



**Figure 15.** Plot of normalized resistance versus TLM spacing for the metallic stack of Ta / Al / Ta ohmic contact. Inset: (top) logarithm I-V plot for the structure, (bottom) SEM image for the distance measurement.

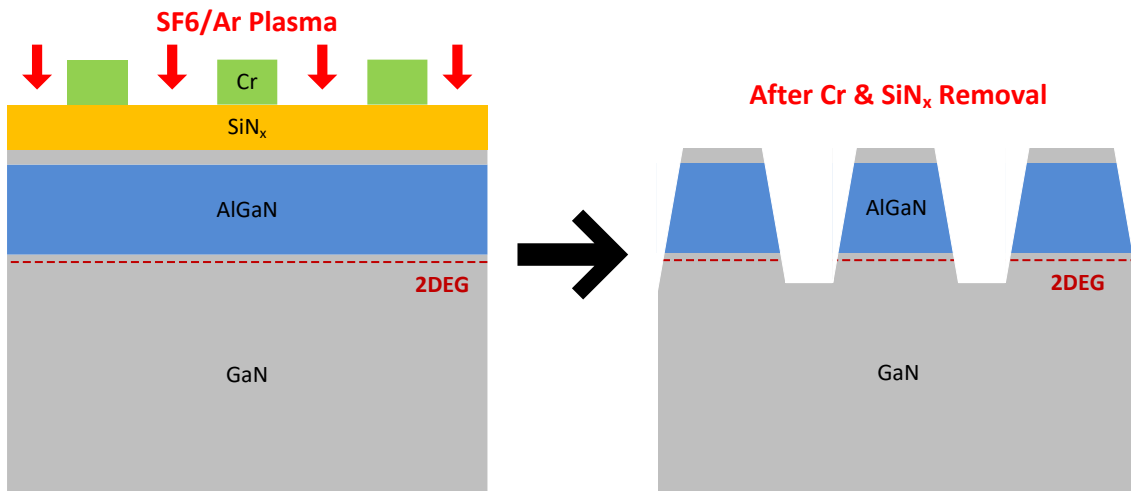
Figure 15 shows the normalized resistance versus TLM spacing plot using the metallic scheme of 7 nm / 280 nm / 15 nm of Ta / Al / Ta. The metals are e-beam-evaporated for the non-mesa/planar AlGaIn/GaN heterostructure. The TLM spacing is measured using scanning electron microscope (SEM), shown in the inset (bottom) of Figure 15. The contact resistance values are realized as  $0.35 \Omega \cdot \text{mm}$  and  $0.37 \Omega \cdot \text{mm}$  for Au-based and Au-free metal stack, respectively. According to the extracted contact

resistance values which are reasonably close, it is worth to focus on Au-free metallic structure to save overall process cost and to avoid high temperature annealing process. The current-voltage characteristics of the fabricated ohmic contacts with different TLM spacing are measured using the HP 4145B Semiconductor Parameter Analyzer in Figure 14 and Figure 15. As shown in Figure 11, the device is a 3-dimensional isolated mesa structure. The contact resistance should be acquired in the AlGaIn/GaN mesa heterostructure. To fabricate a mesa structure, physical and chemical etching process should be developed and optimized to avoid process damage and unexpected chemical treatment on the exposed surface.

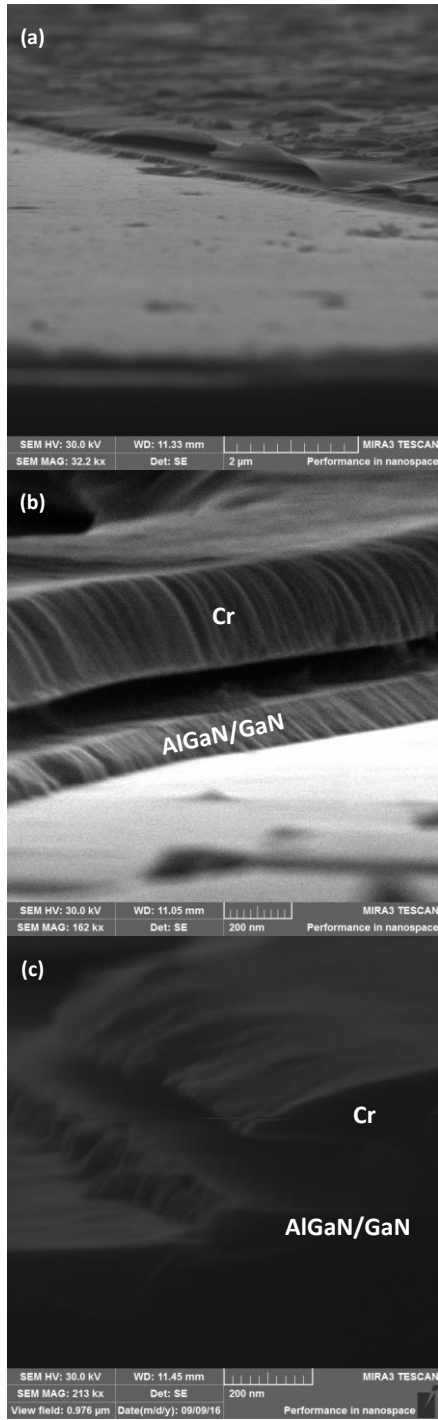
### **AlGaIn/GaN heterostructure mesa isolation and formation**

In order to fabricate the AlGaIn/GaN mesa heterostructure, chlorine and fluorine based dry etching are usually used to apply for etching the heterostructure [20-22]. From the prior studies, fluorine-based plasmas with low bias power are sufficiently gentle to avoid the AlGaIn/GaN surface damage [23]. According to the previous etch studies, the dry etch recipe introduced in reference [22] is initially used to confirm the AlGaIn/GaN mesa isolation structure using the Oxford PlasmaLab 100 Plus RIE system at Texas A&M University. The process is briefly illustrated in Figure 16. Firstly, the substrate cleaning and preparation steps need to go through thoroughly, as mentioned in the earlier paragraph. Patterns in Figure 12 are transferred after lift-off process in acetone using EBL system and 70 nm of Cr deposition by e-beam evaporation. Cr and SiN<sub>x</sub> act as hard masks during the dry etching. The reason of using a blanket deposition of SiN<sub>x</sub> between metal

mask and the AlGa<sub>N</sub> surface is to reduce stress of the subsequent chromium hard mask and electric field build-up on the top corners during the etch process. The inductively coupled plasma-RIE (ICP-RIE) is performed with flow rates of 40 sccm SF<sub>6</sub> and 10 sccm Ar, with RF power of 200 W and ICP power of 250, 300 W, 350 W at the temperature of 13 °C, and a chamber pressure of 44 mTorr. Using the higher ICP power causes mesa collapse even with the two etch stop masks. The effect of higher ICP power is shown in the later fin formation section. The etch profiles after each recipe are shown in Figure 17.



**Figure 16.** A schematic of the mesa-etch process using Cr and SiN<sub>x</sub> etch stop masks with fluorine based ICP-RIE.

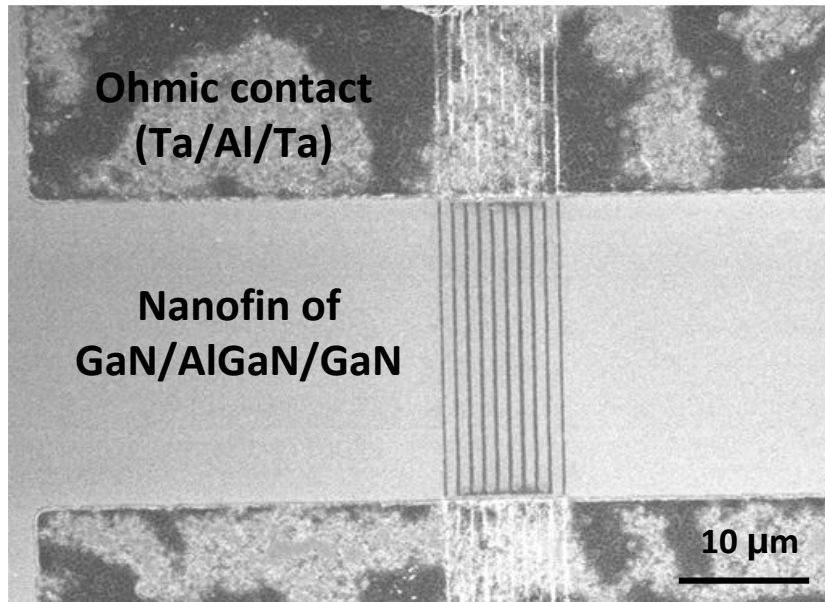


**Figure 17.** The cross-sectional SEM of AlGaIn/GaN heterostructure after 7 minutes dry etching at 44 mTorr and 13 °C with 40 sccm SF<sub>6</sub> and 10 sccm Ar at RF power of 200 W with ICP power of (a) 250 W, (b) 300 W, and (c) 350 W.

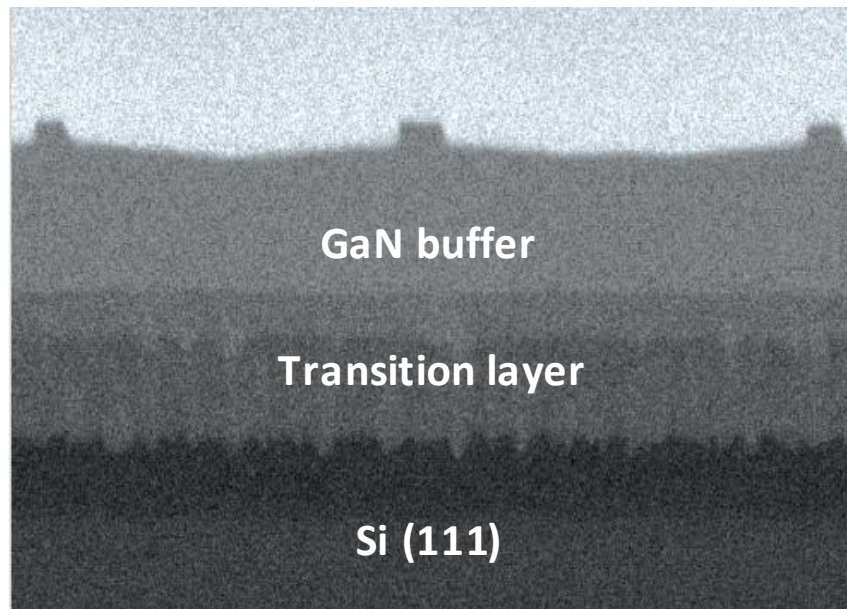
### **AlGaN/GaN fin formation using fluorine based ICP-RIE**

The array of fins is patterned using EBL between the mesa ohmic contacts previously fabricated. First, a blanket deposition of  $\text{SiN}_x$  on the bare wafer is used to reduce stress of the subsequent Chromium hard mask. EBL resist is patterned to produce a lift-off notch, and Cr is deposited so that the lift-off leaves Cr as a hard mask for the fin etch process. Exposed AlGaN/GaN is etched using a fluorine-based (40 sccm  $\text{SF}_6$  / 10 sccm Ar) ICP-RIE for 4 minutes at RF power of 200 W and ICP power of 300 W at 44 mTorr and 13 °C. This etch process is chosen because it has a slow etch rate and minimal damage to the GaN. The etch is performed to a depth of ~10 nm into the GaN, effectively removing the 17 nm AlGaN and 2 nm GaN cap. Further etching is not necessary and may increase damage at dislocations as we progress deeper into the GaN [20, 24]. The Cr hard mask and  $\text{SiN}_x$  layer are subsequently removed by acid etch. A schematic of the fin process is shown in Figure 18. After the fin-etch, the top view image and the cross-sectional image of the multi fins between ohmic contacts using the SEM are taken in Figure 18 and Figure 19, respectively. For the higher resolution verification of the fin structure formation, the transmission electron microscope (TEM) image is taken as well, to obtain the cross-sectional fin image, shown in Figure 20. It shows that the top region of the AlGaN/GaN fin structure has a flat plane geometry. This is different from previous study showing round top geometry [9]. The higher ICP power impact on the fin geometry is shown in Figure 21. The effect of a structural difference is investigated in the later paragraph.

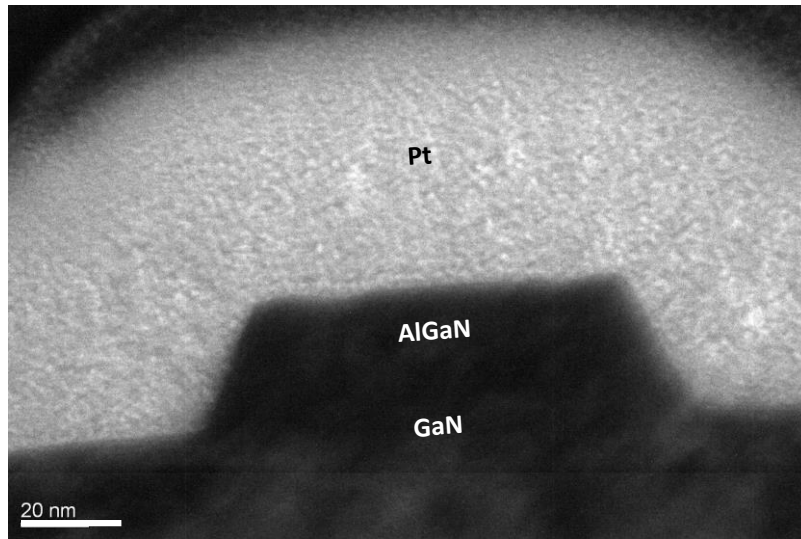




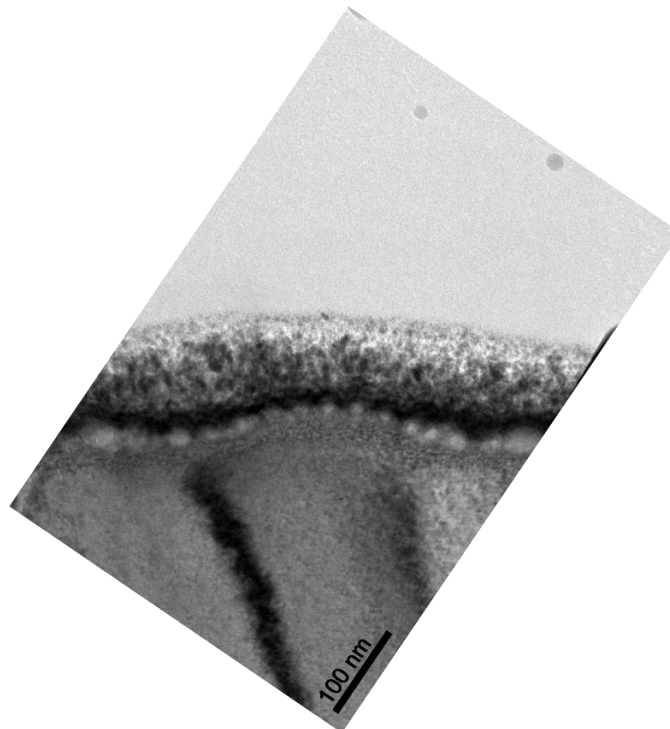
**Figure 18.** Top-view SEM image of the multi-fins between ohmic contacts



**Figure 19.** A cross-sectional SEM image of the fin structure and the compositing layers in the heterostructure.



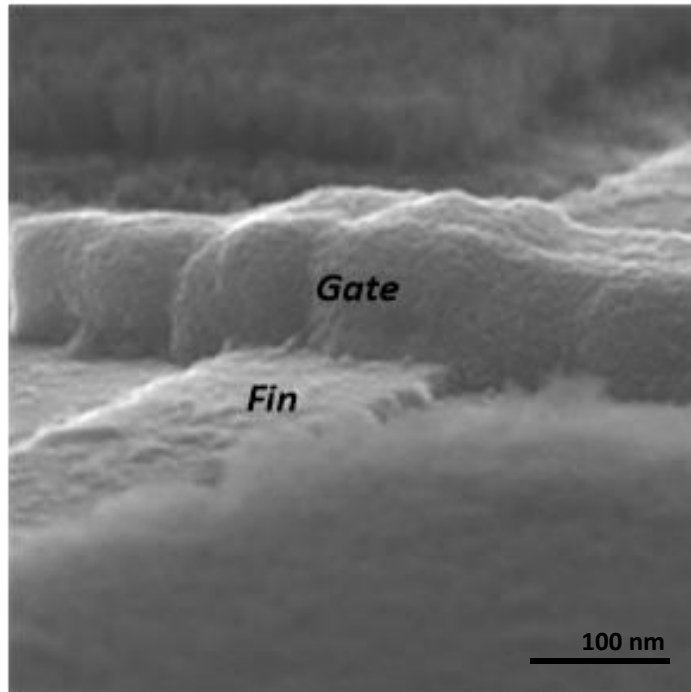
**Figure 20.** A cross-sectional TEM image of a fin heterostructure with a flat plane top region using Cr/SiN<sub>x</sub> etch stop masks.



**Figure 21.** A cross-sectional TEM image of a collapsed fin heterostructure due to high ICP power confinement along the edge of the etch stop masks.

## Gate contact module

The gate contact module includes surface cleaning, high-k gate dielectric deposition using ALD system, gate window patterning using EBL system, and gate stack deposition using e-beam evaporator and sputter systems. Before processing the gate module integration, AlGaIn/GaN fin heterostructures go through the aforementioned cleaning process to insure no remaining residue left during the fin formation and no oxide related byproduct on the surface. After the cleaning process, ALD deposition is carried out to deposit HfO<sub>2</sub> using DI-H<sub>2</sub>O and Tetrakis-(ethylmethylamino) hafnium (TEMAH) precursors at 200 °C. Different gate length ( $L_g$ ) is patterned using EBL system with PMMA resist. The choice of gate metals is limited because it requires a sufficient barrier height to operate the device with low gate leakage and good gate voltage controlled output current. Nickel has a high work function of 5.01 eV, therefore it is chosen to be a good candidate as a gate metal. Especially, a high work function gate metal on the GaN device also possibly shifts the threshold voltage more toward the positives [25]. Ni is evaporated and Au is sputtered on top of it, and they are lifted off as a gate contact metal stack. The fabricated gate metal stack on the AlGaIn/GaN fin heterostructure is shown in Figure 22. The S/D contact windows are opened and HfO<sub>2</sub> in the windows are etched using an Oxford PlasmaLab 100 RIE system with the conditions of 20 sccm SF<sub>6</sub>, 10 sccm Ar, 50 W RF power, 500 W ICP power, at 10 mTorr and 23 °C. 120 cycles of HfO<sub>2</sub> is totally open after 50 seconds of etching time. After the HfO<sub>2</sub> etch, PMMA EBL resist as an etch mask is removed using acetone so that the contacts are probed.



**Figure 22.** A SEM image of Au/Ni metal stack gate on top of a gate dielectric and an AlGaN/GaN fin heterostructure.

CHAPTER III  
ELECTRICAL CHARACTERIZATION OF III-NITRIDE HETEROSTRUCTURE  
FINS AND SIMULATION FOR STRAIN PROFILE IN THE FINS

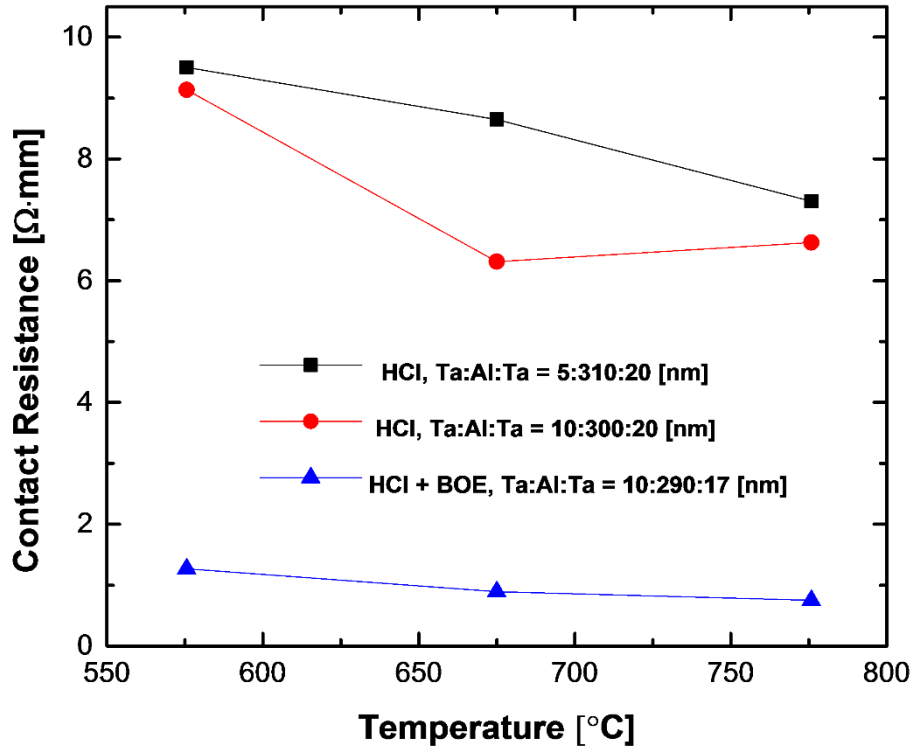
**Introduction**

In this chapter, for AlGaIn/GaN 2DEG devices, the 2DEG density is necessarily dependent on the amount of biaxial strain that will ultimately produce c-axis strain, thereby increasing the piezoelectric-induced surface potential necessary to allow 2DEG formation. As we examine nanoscale features where we etch the heterostructure into fins, the uniaxial relaxation that occurs in the transverse direction relative to the fin axis can lead to reduction of 2DEG density. Current literature has made an attempt to quantify the amount of relaxation and its impact on the 2DEG [26]. However, a true spatial understanding of strain, polarization and 2DEG formation as the fin width is scaled to 10's of nanometers has not been fully explored. Next paragraphs discuss the processing of fin devices using AlGaIn/GaN heterostructures, extraction of electrical properties of the fins and calculation of the density in the 2DEG that results. The data is validated with numerical simulation and a strain distribution of the fin profile is extracted. In order to ensure accurate electrical characterization of the fins, an understanding of fin contact using Au-free contact technology and fin pre-cleaning is described.

### **Impacts on S/D contact resistance due to fabrication process variation**

To achieve low-resistance ohmic contacts, a different pre-cleaning methods before the metallization are carried out. After the typical solvents clean, all samples undergo a dilute HCl chemical clean for the same time period. The pre-cleaning methods are 1) a dilute HCl clean with three different dilution ratios of HCl to H<sub>2</sub>O (1:1, 1:4, and 1:10), 2) a buffered oxide etchant (BOE) clean only, 3) a dilute HCl Clean followed by a BOE clean. Au-free ohmic contacts with different metallic ratio schemes of Ta/Al/Ta are formed by e-beam evaporation deposition followed by rapid thermal annealing (RTA) at different annealing temperatures in ambient N<sub>2</sub>. Previous studies [27, 28] have been demonstrated a Ta/Al/Ta scheme with low resistance ohmic contact formation with a thickness ratio of  $t_{Al}$  to  $t_{Ta} \approx 28$  at an annealing temperature of 575 °C. The contacts include TLM structures which are formed in close proximity to the fabricated fins on the same substrate. The contact pad width is 100 μm and the TLM spacing varies from 1.5 to 25 μm with 10 fins per spacing. Extra annealing is carried out at higher temperature in order to examine the temperature effect on  $R_c$ . The  $R_c$  is nearly independent of the anneal temperature range from 575 C to 775 C, which possibly is attributed to wrapping of the metal around the fin, thereby increase diffusion directionality from one to multiple dimensions, thereby increasing contact area, compared to planar ohmic contacts. The lowest  $R_c$  measured by the TLM structure is 0.32 Ω-mm for the fins and recessed regions without the fins at 575 °C when a dilute HCl (1:10) pre-clean is followed by a BOE pre-clean. Using the TLM structures, the contact resistance is shown at various annealing

temperatures and different metal stack ratios with different surface pre-cleaning methods in Figure 23.



**Figure 23.** Variation of the contact resistance for different Ta/Al/Ta ohmic metallization ratio with different pre-cleaning methods is obtained by using TLM structure at various annealing temperatures.

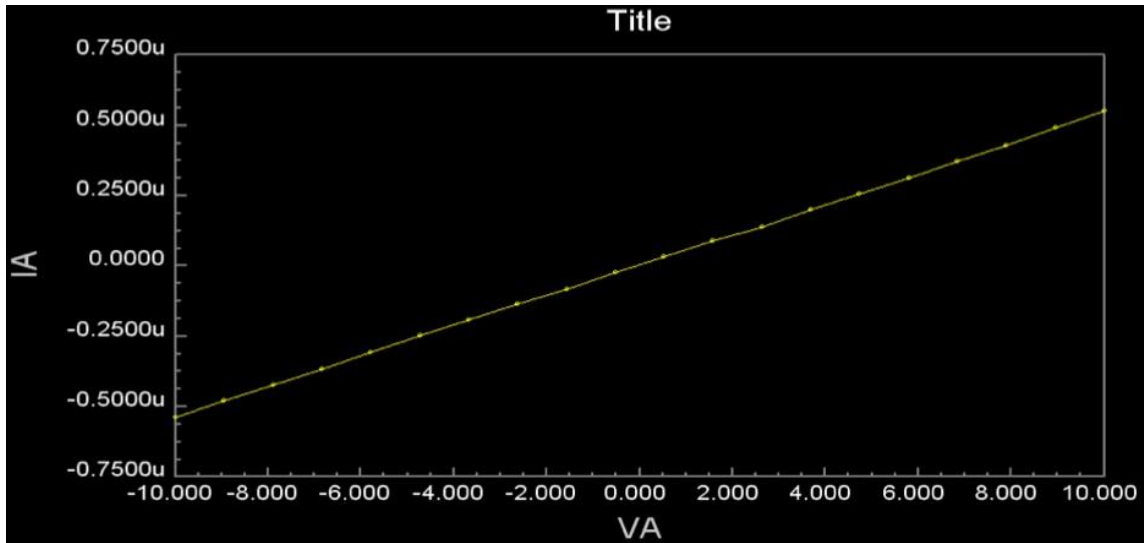
Among the three different dilution ratios of HCl to H<sub>2</sub>O (1:1, 1:4, and 1:10), the lowest contact resistance is observed in the sample with the 1:10 ratio pre-clean. Highly dilute HCl solution reduce the effective reaction time, reducing damage to the surface so that

surface roughness is not increased [29]. This pre-clean procedure is used to remove any oxide layers on the surface, however, it is not strong enough to remove all oxide layers. Therefore, a BOE (dilute HF) pre-clean is also carried out as an additional chemical clean to remove left oxide layers from the surface [30]. After the additional BOE cleaning step, there is significant improvement in the contact resistance as shown in Figure 23. From the previous literature [30, 31], it is found that a BOE clean is the most efficient way to remove most of the oxides from the GaN surface.

### **Two possible conduction paths investigation using I-V characteristic**

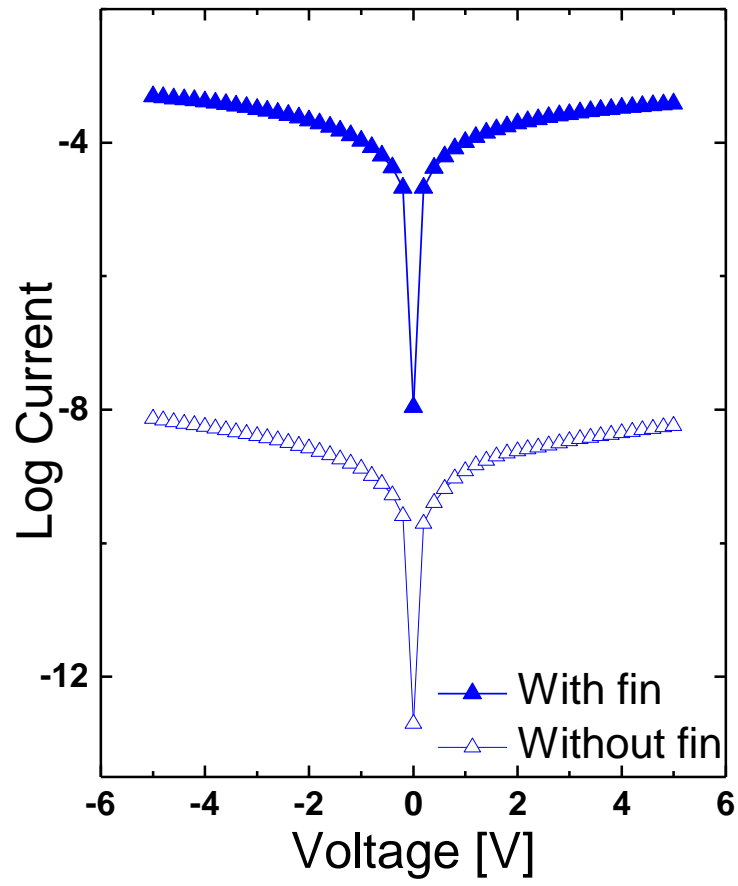
Prior to extracting 2DEG density from the electrical data, we must ensure that the impact of substrate conduction is not affecting the calculations. With resistance ohmic contact formation using Au-free metallization scheme (Ta / Al / Ta), the conductivity with the fins and without fins (recess etched GaN regions) is measured using the electrical current-voltage characterization method. I-V characteristic for recess-etched GaN regions where no fins exist, is shown in Figure 24.





**Figure 24.** I-V characteristic of recess-etched GaN region.

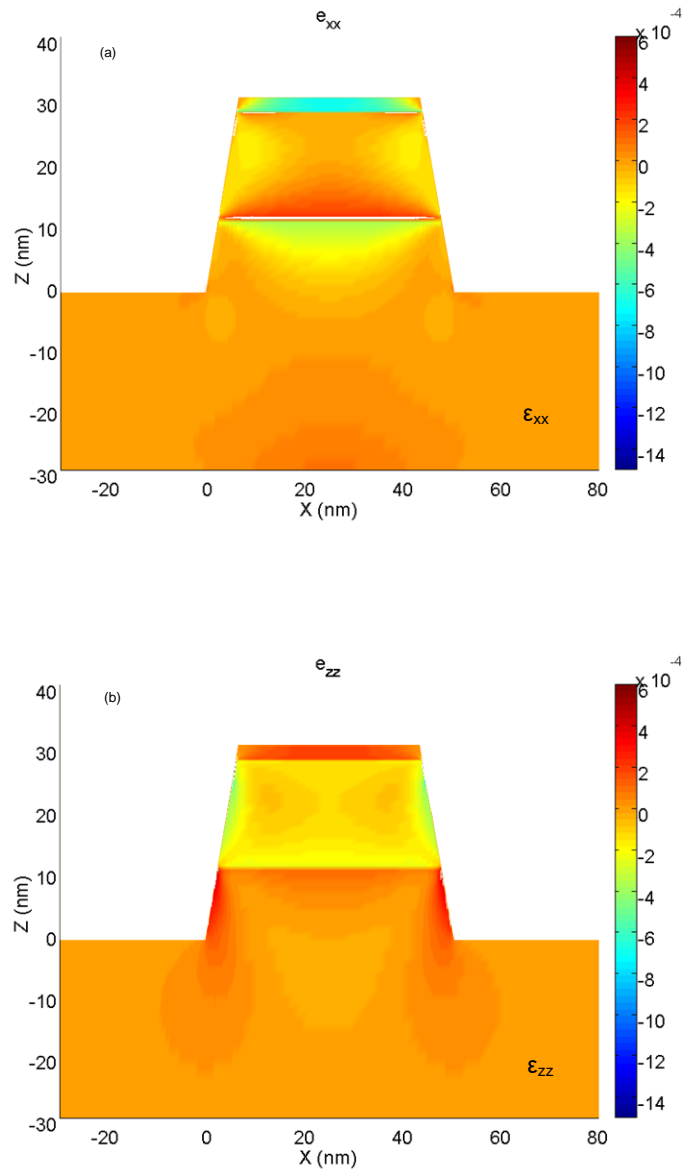
I-V characteristic for multi-fin AlGaIn/GaN structures, as well as for recess-etched GaN regions where no fins exist, is shown in Figure 25. The difference in the current between the contacts with and without fins displays more than 5 orders of magnitude difference, clearly indicating that substrate conduction is not contributing to the current which is used to calculate the 2DEG density in the fin. For accuracy and completeness, several sheet resistances for the no-fin contacts on the same substrate are measured with sheet resistance in the range of  $2 \times 10^7 - 7.5 \times 10^9 \Omega/\square$ , further supporting the conclusion that no additional charge density contribution from recessed GaN regions needs to be considered in the calculation of the overall 2DEG sheet density.



**Figure 25.** The log current level difference from the I-V measurements for the regions with and without fins.

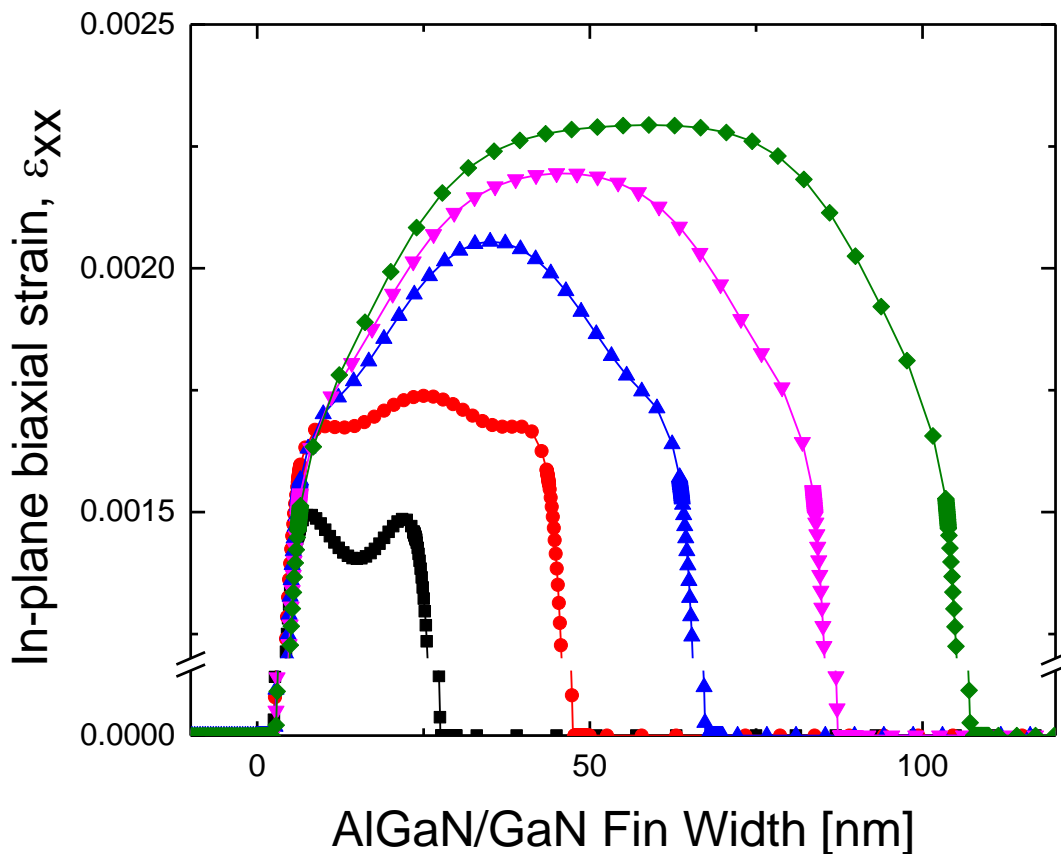
### **Simulation for strain profile in the heterostructure fins**

For an AlGa<sub>N</sub>/Ga<sub>N</sub> fin structure with the side wall angle of 78° (based on TEM) in Figure 20, the simulated isotropic, in-plane biaxial strain ( $\epsilon_{xx}$ ), and growth axis strain ( $\epsilon_{zz}$ ) is shown in Figure 26. The relaxation of AlGa<sub>N</sub> tensile and Ga<sub>N</sub> compressive strain at the edges of the fin are clearly visible in the longitudinal direction, and the vertical strain demonstrates the expected edge enhancement as predicted by [32].



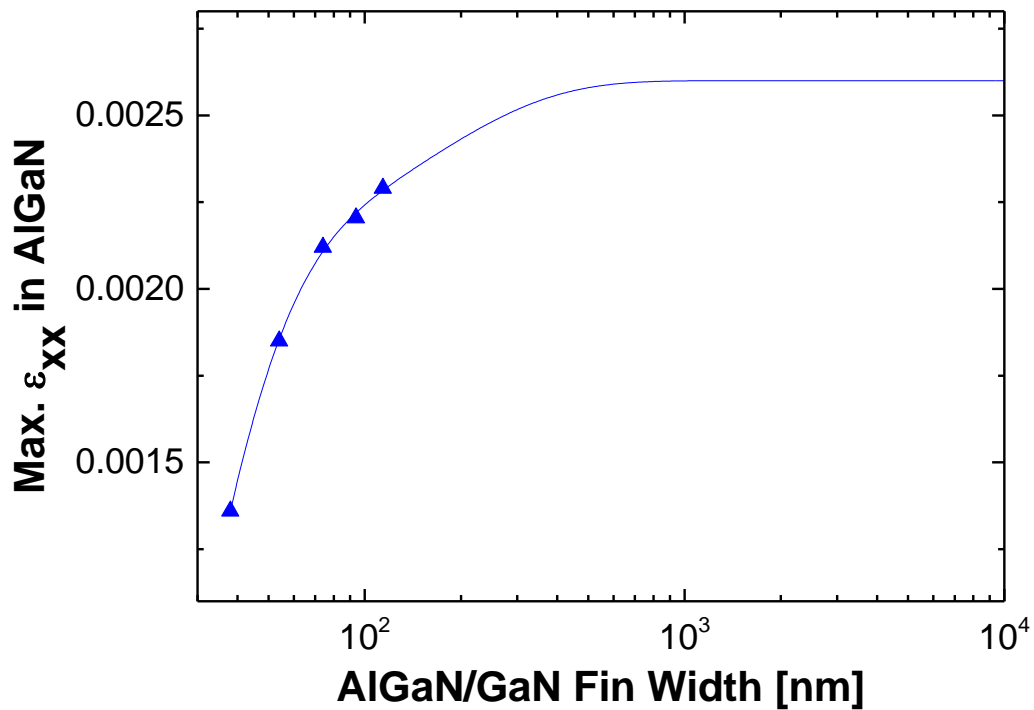
**Figure 26.** Numerical simulation results for strain profiles (a) in-plane biaxial strain,  $\epsilon_{xx}$ , profile of a nano fin GaN/AlGaIn/GaN heterostructure. The red color represents tensile strain and the blue color represents compressive strain. It shows a very abrupt change at the interfaces, (b) growth axis strain,  $\epsilon_{zz}$ , profile indicates possible structural deformation along the fin sidewalls.

Since the magnitude of surface potential in the GaN that forms the 2DEG depends strongly on the AlGaN strain directly above the interface, the AlGaN strain along the fin right above the AlGaN/GaN interface is plotted in Figure 27, along with the same strain-position data for the several fin widths made for this study, as measured by TEM. It can be seen that there is approximately 40% reduction in the biaxial strain at the center of the fin as we reduce fin width from 114 nm to 34 nm, showing the compounding effect of edge relaxation throughout the fin structure [26, 33].



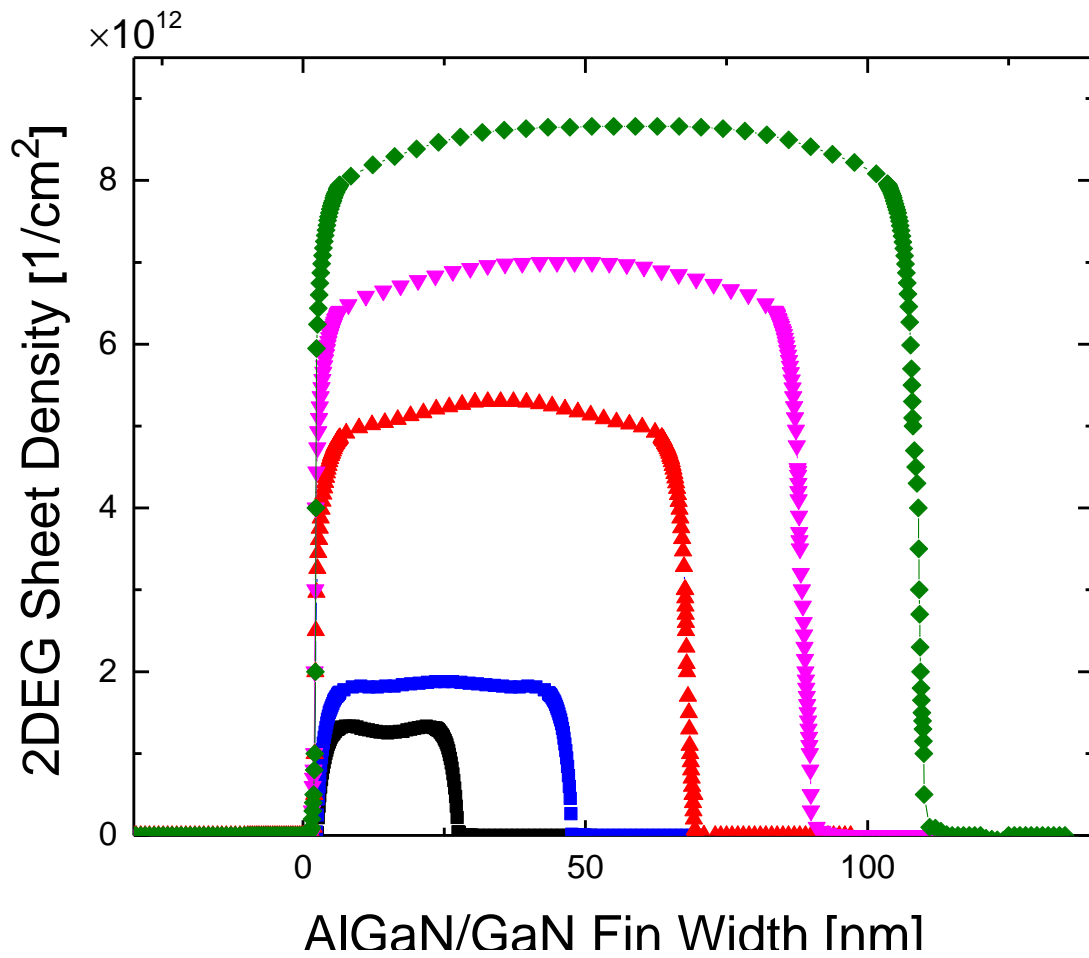
**Figure 27.** In-plane biaxial strain profile along the AlGaN layer near the AlGaN/GaN interface as a function of fin widths.

As the fin width approaches  $< 40\text{nm}$ , the biaxial relaxation has encompassed the entire fin width, thereby reducing the peak value of  $\epsilon_{xx}$ . The edge-enhanced  $\epsilon_{zz}$  (Figure 26) creates a concomitant increase in  $\epsilon_{xx}$  due to the lattice relationship  $\epsilon_{zz} = -2\frac{c_{13}}{c_{33}}\epsilon_{xx}$ , but the influence of  $\epsilon_{zz}$  does not become apparent until the overall x-direction strain reduces as seen in the 32nm fin [26]. Figure 28 shows that the maximum in-plane biaxial strain decreases exponentially as the fin width gets narrower in agreement with [34].



**Figure 28.** Maximum in-plane biaxial strain variation due to fin widths variation.

Based on the strain profile simulation data, made possible by correlation of the cross sectional data collected in TEM analysis, it is possible to calculate the spatial polarization due to relaxation at the edge of the fin, and thus the resulting amount of 2DEG formation for each of the fin widths, shown in Figure 29.



**Figure 29.** Simulated 2DEG sheet density profile,  $n_{sh}(x)$ , as a function of position along the fin widths in the GaN/AlGaN/GaN heterostructure.

## Electrical measurement and simulation/calculation results on 2DEG density

Instead, an effective sheet charge density ( $n_{sh,eff}$ ) can be found from

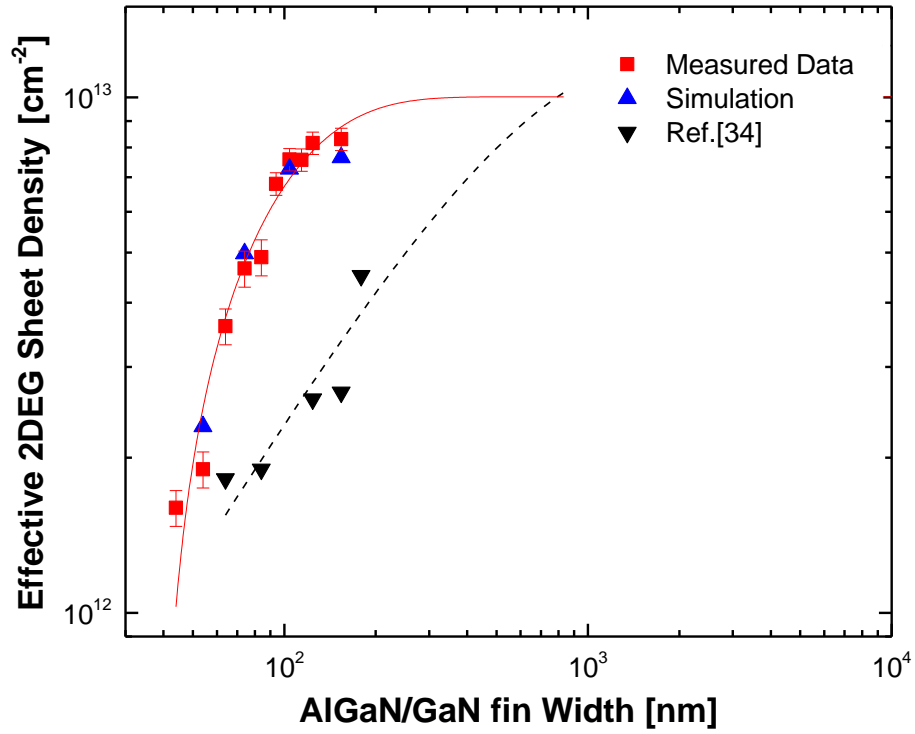
$$n_{sh,eff} = \frac{1}{w_{eff}} \int_0^{w_{eff}} n(x) dx. \quad (1)$$

where

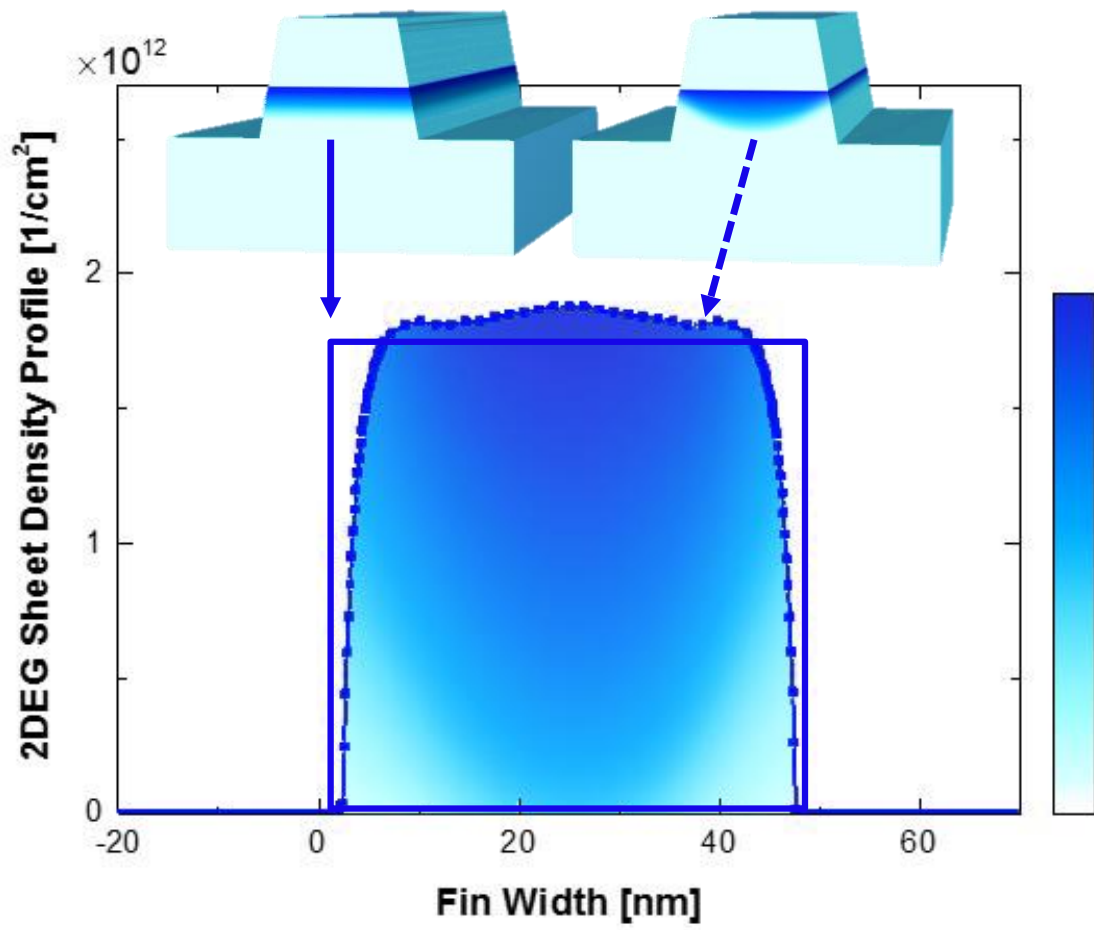
$$w_{eff} = w_{top} + 2 \times \frac{t_{AlGaN}}{\tan(\theta)} \quad (2)$$

Here,  $w_{top}$  and  $t_{AlGaN}$  are the top fin width and the thickness of AlGa<sub>N</sub> layer, respectively, and  $\theta$  is the fin side wall angle. This integration provides an effective density over the fin that allows us to correlate an electrical measurement that is an aggregate measurement itself. Planar sheet density is measured using Leighton Model 1605 non-contact Hall mobility measurement system before the process starts for comparison. Electrical measurements, corrected for contact resistance, are used to extract the effective 2DEG density and compared with the aggregate 2DEG density determined by simulations above. Figure 30 shows the calculated and measured effective  $n_{sh,eff}$  together. The distinction between effective and real 2DEG density is highlighted in Figure 31, where the square profile represents the effective density as measured by electrical extraction and the actual profile from simulations is the shaded region. In this manner, we can make direct comparison of the measured effective sheet charge and the simulated sheet charge from strain profiles and corrected for geometric variations.





**Figure 30.** Experimentally measured 2DEG sheet density versus different fin widths of  $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}/\text{GaN}$  heterostructure.



**Figure 31.** The square profile represents the effective and the actual profile represents the real 2DEG density profile in the fin by the simulation.

The precise modeling of the strain due to fin geometry proves to be the best method of extracting 2DEG density based on the clear match of actual and modeled data. Furthermore, we see that the fin maintains a higher percentage of 2DEG density at short fin widths, as indicated by the steep  $dn_{sh,eff} / dW_{fin}$  around 50 nm. From this data, we can project a decade reduction of 2DEG density at a fin width of 43 nm. To compare, the effective density calculated from [34] is shown in Figure 30 as well, showing that the extracted  $n_{sh,eff}$  from this work is greater by a half order of magnitude at 100nm. The difference can be accounted for in the more precise fin geometry extraction of strain, but it should be noted that process differences can alter  $n_{sh}(x)$ . For instance, the type of plasma etch can form fin sidewall charge that will change the 2DEG density. For this reason, process variations from reports across the literature make absolute conclusions challenging. It can only be stated that it is possible to maintain approximately 80% of the planar sheet charge density around a fin width of 100 nm.

## CHAPTER IV

### MASK REGISTRATION AND LITHOGRAPHY PLATFORM PORTABILITY FOR III-NITRIDE HETEROSTRUCTURE FINs PROTOTYPING\*

#### **Introduction**

As the scaling of device technology continues past the 14 nm technology node, it is imperative that power devices and high performance RF devices find a common platform. III-nitride devices with a 2 dimensional electron gas (2DEG) that demonstrates high mobility may need to be integrated in high performance power devices with CMOS FinFET technology [35, 36]. As such devices are lithographically carved into the 2D electron gas, nano-scale strain changes due to relaxation are induced in local areas depending on geometry. An understanding of the feature size and its impact based upon electron gas composition has been studied, but a complete picture is not currently portrayed in the literature. Further understanding of how to design and prototype 3D devices in nitrides, including 2D and drift devices, is required to keep the production platforms similar so that complete integration of silicon and nitride devices is accomplished.

Two of the most important processing modules for integration include lithography and Au-free ohmic contact formation. The lithography integration has been studied and

---

\* Part of this section is reprinted with permission from “Mask registration and lithography platform portability for nitride fin-based field effect transistors prototyping” by J. W. Suh, M. E. Babb, E. L. Principe, H.R. Harris, 2016. J. Vac. Sci. Technol. B, 34, 06k602, Copyright 2016 by American Vacuum Society.

demonstrated, but ohmic contacts or etching require restrictive process rules to account for contamination in CMOS processing environment [36-38]. Integration of an Au-free contact into III-nitrides materials satisfies the contamination requirement for processing silicon and nitride devices in parallel [39]. Ta-based contacts have been explored and optimized, but the impact of additional heat treatment during device processes is not yet fully understood [36]. The combination of photolithography and electron beam lithography (EBL) has been reported in silicon technologies with technical benefits [40-42]. The combination of lithography techniques simultaneously leverages high throughput process and high-resolution capability. However, these have not been applied in nitride FinFET fabrication process. To this end, we examine the requirements of wide band gap nitride device technology using the process prototyping with common i-line photolithography and electron beam lithography. The extreme difficulty in etching, pattern transfer and hard masking an already extremely hard material is discussed and prototyping processes for mask to mask pattern registration is explored.

The primary challenge in combining EBL and standard lithography is the observation and correct alignment to registration in EBL. Inherent in this challenge is the fact that EBL resist is sensitive (i.e. degrades) when the act of viewing it with an e-beam is performed. This alignment is detrimental to process quality. In limited cases the alignment in standard lithography can be challenging as well, but only in aggressive etching or thick deposition. The deleterious result of misalignment of the two lithography processes is non-working devices as critical regions are either shorted or result in high

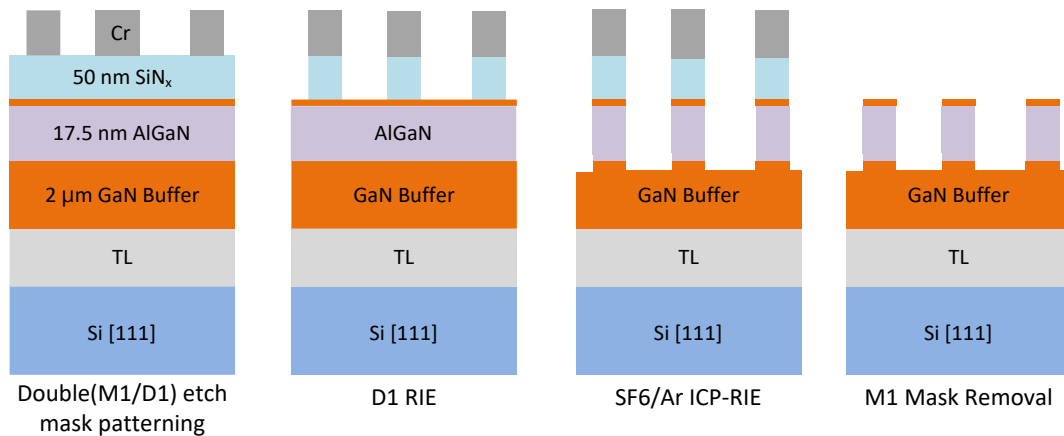
resistance. Therefore, this work endeavors to find the efficacy of combining such processes.

### **Prototyping of III-nitride FinFET device fabrication**

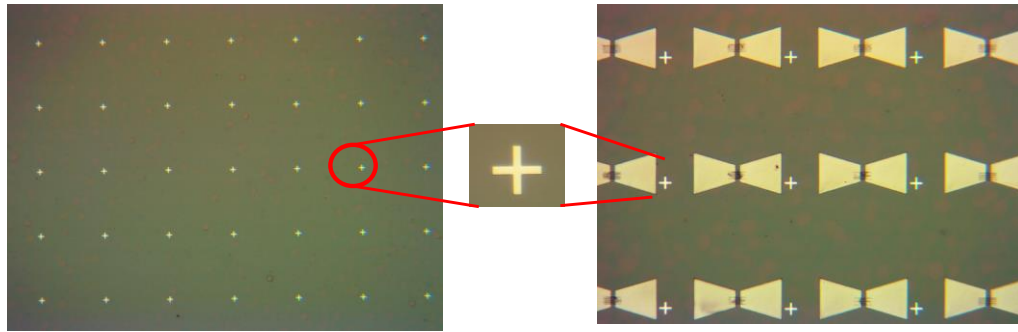
Prototyping of III-nitride FinFET device fabrication started with a GaN (2nm)/Al<sub>0.24</sub>Ga<sub>0.76</sub>N (17.5 nm)/GaN on Si substrate grown by metal organic vapor deposition (MOCVD) with a total buffer layer thickness of 2 μm, including transition layers between GaN and Si. Process platforms were kept similar to Si based CMOS processes in addition to electron beam lithography. The substrates were cleaned in HCl:H<sub>2</sub>O with a 1 to 10 ratio for 10 min and buffered oxide etchant (BOE) for 5 min. A surface passivation layer of 50 nm silicon nitride was deposited using plasma enhanced chemical vapor deposition (PECVD) at 350 °C.

Before depositing registration marks and source/drain (S/D) ohmic contact metals, patterns were transferred using an optical i-line aligner and pattern windows were opened in SiN<sub>x</sub> via BOE etching. The diluted HCl pre-metallization clean was carried out immediately prior to the deposition of the Ta/Al/Ta (8/220/17 nm) metal stack by electron beam evaporation. Linear transmission line method (TLM) structures were fabricated along with S/D contacts. The registration marks and contacts were defined after a lift-off process in Acetone. A rapid thermal annealing process was done at 575 °C for 4 min in ambient N<sub>2</sub> to ensure ohmic contact formation on the III-nitride surface [43]. Temperature effects on contact resistance were acquired with additional annealing at higher temperatures.

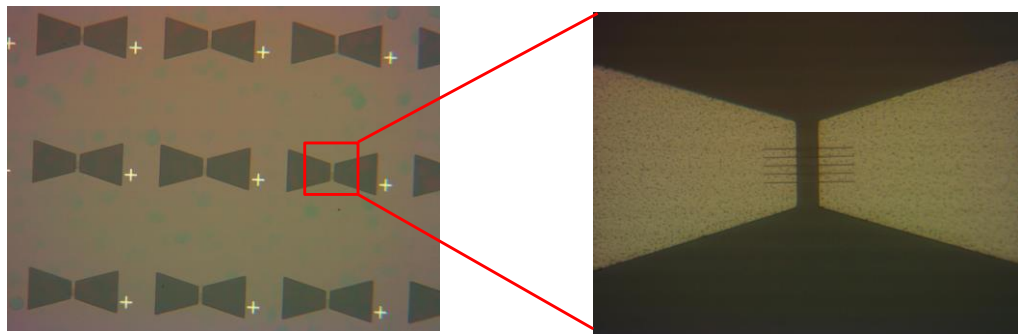
Using EBL to align with the registration marks and contact metals, various fin widths in the range of 30 nm to 120 nm were patterned to produce lift-off notches between the contacts. Chromium was deposited so that the lift-off left Cr as a hard mask on the blanket of SiN<sub>x</sub> layer. The blanket SiN<sub>x</sub> layer reduces surface damage during the direct fin etch process and prevents the top corners of the fin from collapsing. The etch process was performed using a fluorine-based (SF<sub>6</sub>/Ar) inductively coupled plasma reactive ion etch (ICP-RIE). The etch process was performed to a depth of ~10 nm into GaN buffer region. After the etch process, the etch stop layers were removed by acid etchant. Figure 32 shows the schematic of the III-nitride fin etch process using two etch stop masks of Cr/SiN<sub>x</sub>. An additional SiN<sub>x</sub> layer between Cr and GaN mitigates electric field build-up at the sharp edges of the top Cr etch stop mask during the ICP-RIE process so that damage to the GaN region is reduced. Also, a blanket layer of SiN<sub>x</sub> prevents surface damage, which would increase surface roughness due to the high power etching process.



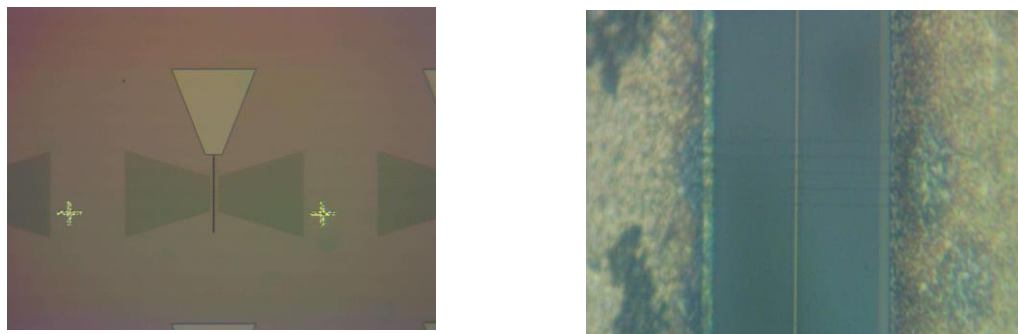
**Figure 32.** III-nitride heterostructure etch process using two etch stop masks, Cr(M1)/SiN<sub>x</sub>(D1)



**Figure 33.** Registration marks at the beginning of the overall process using high atomic weight material.



**Figure 34.** Fin patterning using EBL aligning to registration marks and predefined S/D contact metal.



**Figure 35.** Ability of common Si-CMOS like gate-first and -last process and overall device view with well-defined gate, drain, and source regions.

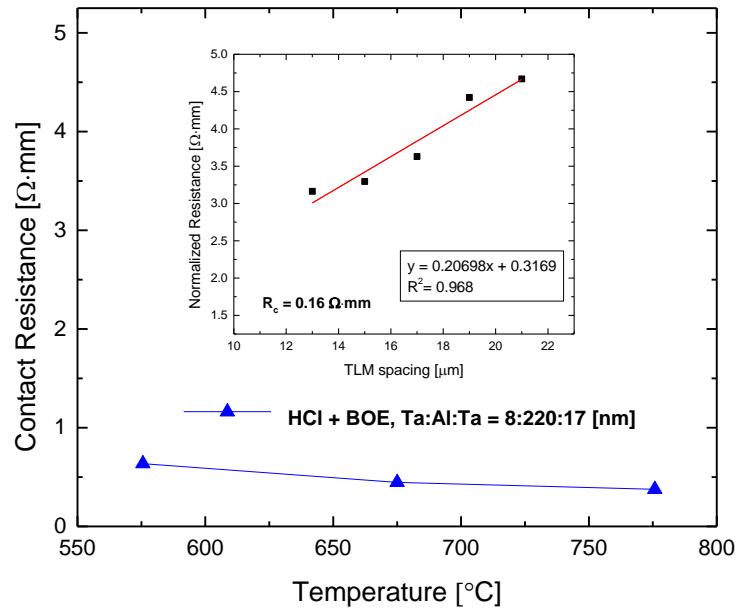


After opening the gate window over exposed AlGaIn/GaN fin regions using EBL resist, the samples were cleaned in diluted HCl and BOE immediately before atomic layer deposition (ALD) of 15 nm of HfO<sub>2</sub>. Finally, 150 nm of nickel was deposited using electron beam evaporation. Figure 33, Figure 34 and Figure 35 show a final III-nitride device schematic and prototyping process flow with the combination of optical and electron beam lithography. DC I-V characteristics were acquired using a Hewlett-Packard 4145B parameter analyzer.

### **Electrical characterization results of the III-nitride FinFET**

Figure 36 shows the contact resistance of Ta/Al/Ta metallization as a function of annealing temperature, and the inset shows the resistance versus linear TLM spacing plot. The TLM spacing was measured by top down SEM for the use of contact resistance extraction. The lowest extracted contact resistance,  $R_c$ , was 0.16  $\Omega$ -mm, comparable to previous studies [27]. Additional temperature effects on  $R_c$  were extensively studied by Malmros *et al.*[27] and Lee *et al.*[36], which showed that  $R_c$  was affected by different annealing temperature; however, in our study, it was nearly independent of the annealing temperature range. This is attributed to the existence of multiple directions of metal/AlGaIn interaction now that we have fin geometry as the fins are fabricated first, and the metal stack is deposited to wrap over the fins and annealed. An important consequence is seen with subsequent processing temperatures: there is negligible impact the quality of the ohmic contact to the AlGaIn/GaN heterostructure with further annealing. The process is further improved by the diluted HCl and BOE pre-cleaning, which strips

native gallium oxides and other residual oxides from the surface [29-31, 44]. Hence interface ohmic properties of the metals may have been improved.

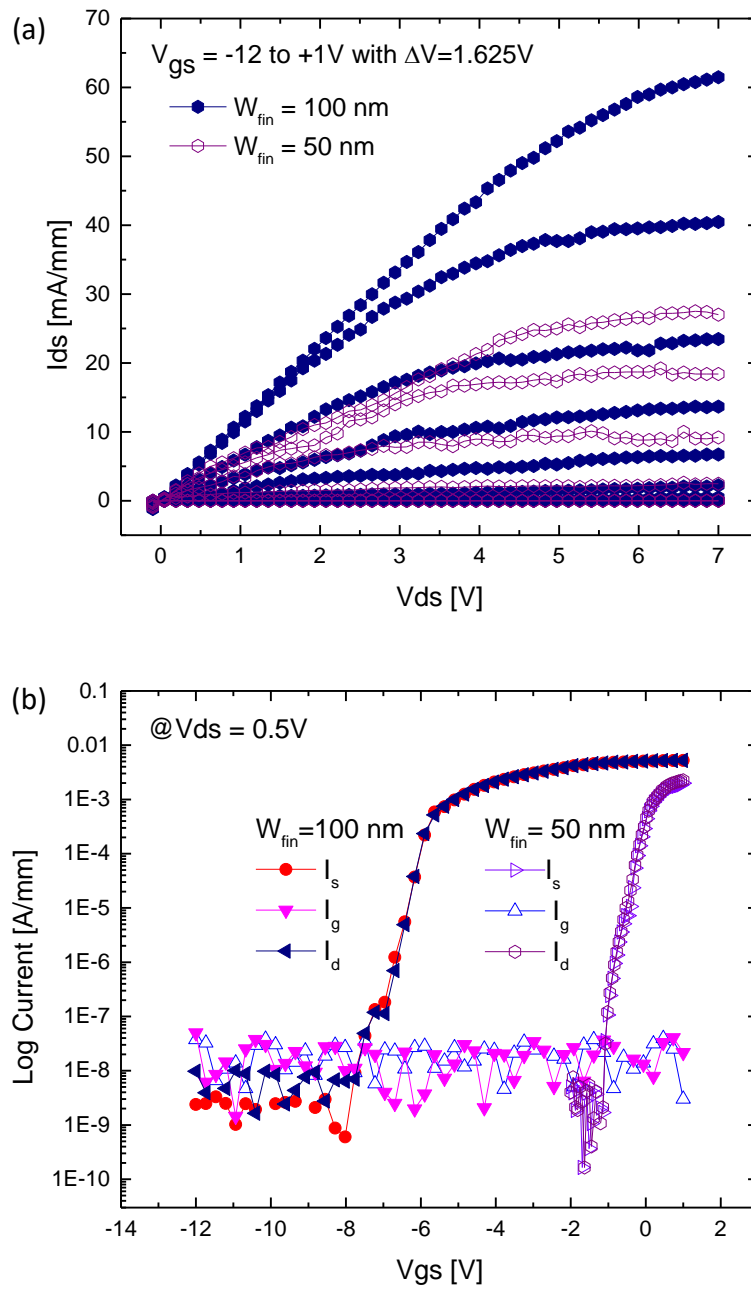


**Figure 36.** Extracted contact resistance ( $R_c$ ), as a function of annealing temperature for Ta/Al/Ta ohmic contact for S/D. Inset: Normalized resistance as a function of linear TLM spacing.

The DC I-V output characteristics of the AlGaIn/GaN FinFET fabricated using this process prototyping technique with  $W_{\text{fin}} = 50 \text{ nm}$ ,  $100 \text{ nm}$  and  $L_g = 500 \text{ nm}$  are shown in Figure 37 shows the absolute S/D current and gate leakage current versus gate bias, measured at  $V_{\text{ds}} = 0.5 \text{ V}$ . Devices maintain a ratio of  $I_{\text{on}}/I_{\text{off}}$  greater than  $10^6$ . During the process prototyping, the inherent nature of the nitride FinFET is such that device symmetry is preserved (Figure 35). Because of this, the DC output and transfer

characteristics as shown in Figure 37 occur regardless of which fin contact is used as source/drain. Furthermore, gate leakage current is below  $10^{-8}$  A/mm over the applied gate bias region, indicating that the high resistive nature of substrated GaN acts as a good insulator in the absence of a field dielectric or amorphization implant. For this reason, the EBL/i-line combination can be more efficiently combined during rapid device prototyping without more complex isolation modules added to the process.

The threshold voltage of AlGaN/GaN 2DEG HFET transistors is generally depletion mode, showing a negative value due to the existence of a 2DEG channel region at the AlGaN/GaN interface. The extracted threshold voltage,  $V_{th}$ , was found to be -0.2 V for  $W_{fin} = 50$  nm and -5.8 V for  $W_{fin} = 100$  nm. The difference in saturation current at  $V_{gs} = 1$  V is primarily due to  $V_{gs} - V_{th}$  being so much larger for the 100nm fin device.



**Figure 37.** (a) DC  $I_{ds}$  -  $V_{ds}$  output characteristics of the AlGaIn/GaN FinFET fabrication prototyping with Au-free contacts. (b) Subthreshold currents as a function of gate voltage.

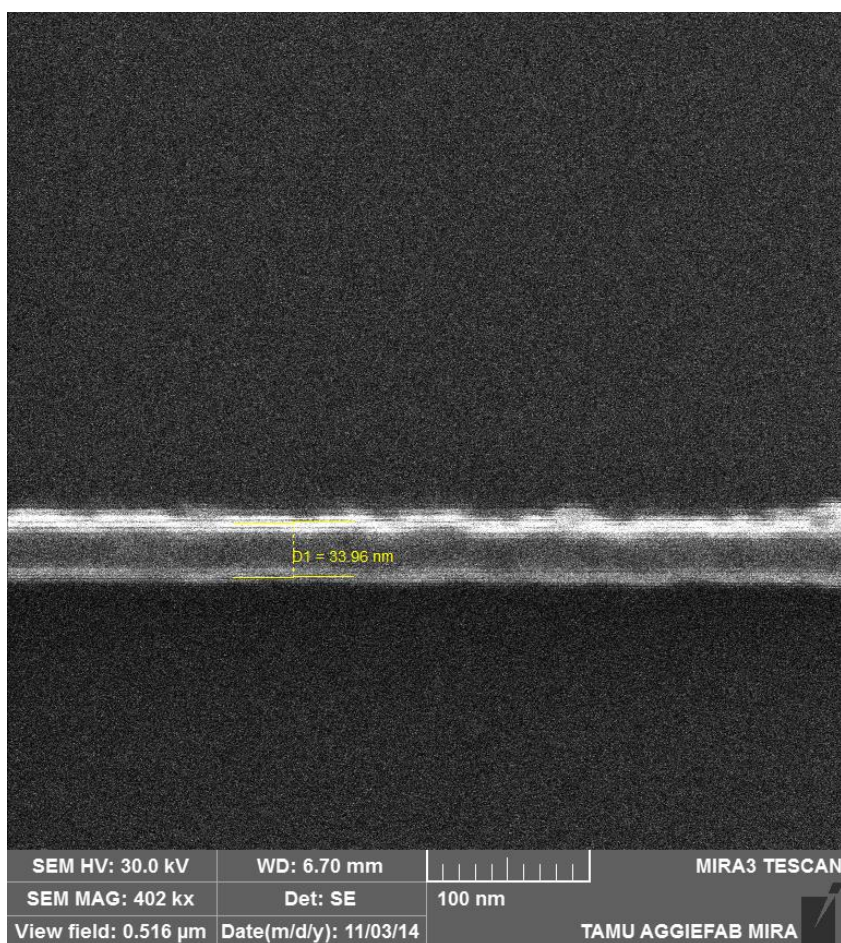
CHAPTER V  
ENHANCEMENT MODE ALGaN/GaN FINFET AND ADDITIVE STRAIN  
EFFECT

**Introduction**

While excellent advances have been achieved toward fabricating normally-off, enhancement mode (E-mode), AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure FinFET devices [9, 45], challenges remain due to strong spontaneous and piezoelectric polarization of the nature of AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure itself. Scaling down AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure FinFETs grown on Si below 45 nm fin width produces a positive threshold voltage ( $V_{th}$ ) E-mode III-V FinFET device. Applying a passivation layer of PECVD grown SiN<sub>x</sub> as an additive tensile strain source to AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure FinFETs results in an  $I_{d,max}$  increase over the range of the fin width from 34 nm to 124 nm. The maximum change of  $I_{d,max}$  is found to be 147 mA/mm before and after the passivation. Also, contact resistance dependency on fin width variation is observed and the effect on the 2DEG density is calculated. Consequently, effective 2DEG sheet density at the interface of the heterostructure AlGa<sub>N</sub>/Ga<sub>N</sub> is extracted based on the device performance before and after the passivation and increases by  $\sim 3.7 \times 10^{12} \text{ cm}^{-2}$  due to the additive strain on the device.

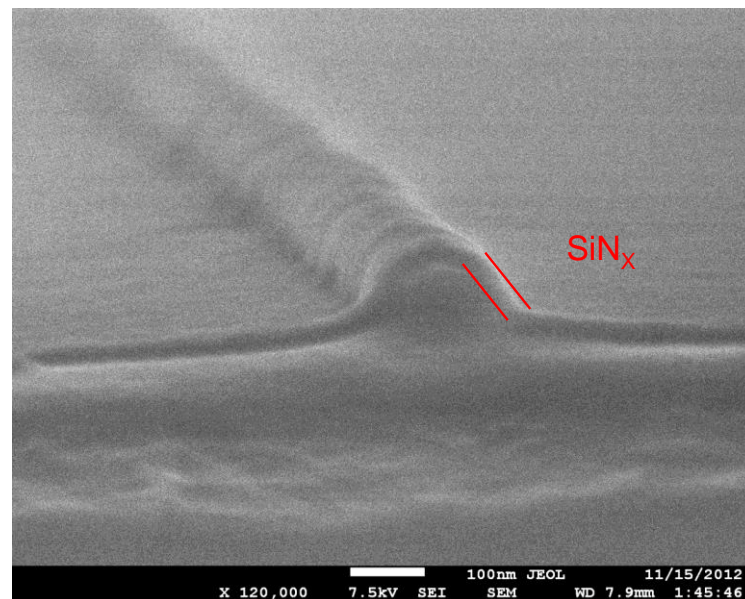
## Device channel width down-scaling and passivation using PECVD on AlGaIn/GaN FinFET

According to the effective 2DEG density profile along with the fin width scaling in the previous section, enhancement mode AlGaIn/GaN FinFETs are realized when scaling-down the fin width. The minimum fin width is 34 nm as shown in Figure 38. The fin widths have a range of 34 nm to 124 nm and the devices are fabricated as previously mentioned.

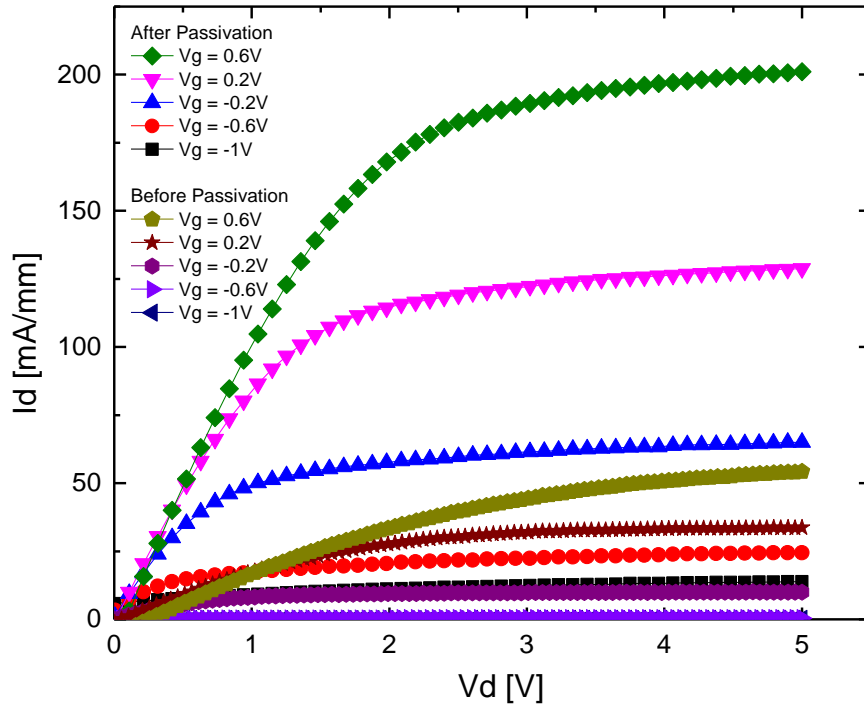


**Figure 38.** Top view of 34 nm of AlGaIn/GaN fin width, measured by SEM.

Positive threshold voltages are obtained with the fin widths of 34 nm and 44 nm, which are 0.2455 V and 0.0347 V, respectively. As the fin width scales down, piezoelectric polarization is reduced due to free facets at the side walls which causes strain relaxation along the facets. Free surface charges at the side walls also deplete the charge density of the 2DEG near the side wall surfaces. This makes the confined 2DEG density less along the overall fin width which results in a decreased effective 2DEG density. This data suggests that approximately 45 nm of fin width is the critical dimension which can obtain a positive  $V_{th}$ . After the electrical characterization of the non-passivated devices,  $\text{SiN}_x$  is deposited using PECVD with the recipe given in the previous section. The passivated fin is shown in Figure 39. The obtained, normalized before and after  $I_d - V_d$  output characteristics are shown in Figure 40.



**Figure 39.** PECVD grown  $\text{SiN}_x$  passivated nano fin of AlGaN/GaN structure, imaged by SEM.

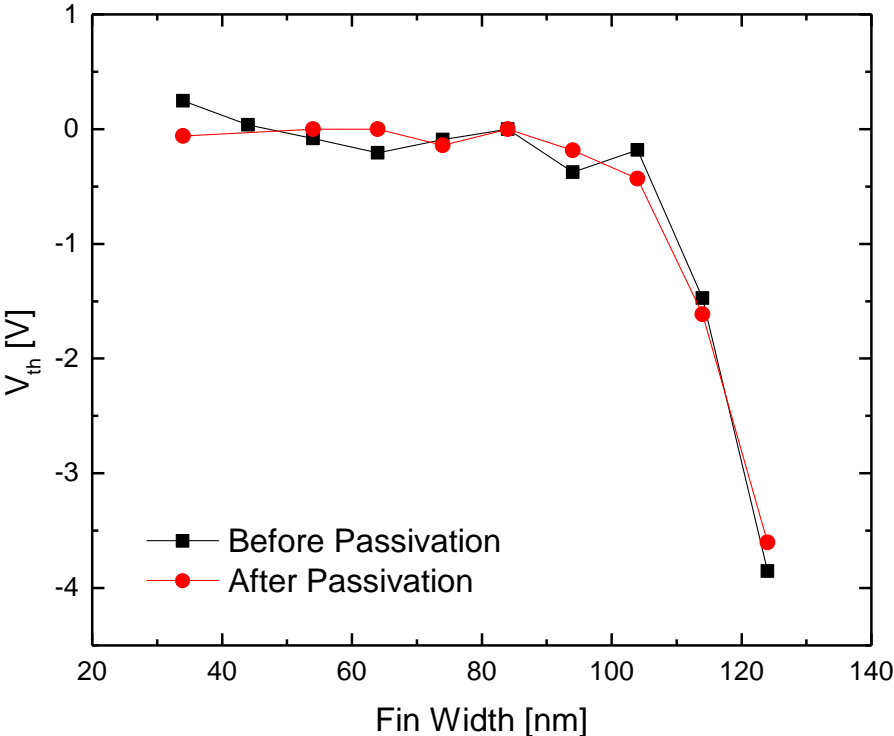


**Figure 40.**  $I_d$ - $V_d$  curves of the AlGaN/GaN FinFET before and after PECVD grown  $\text{SiN}_x$  passivation.  $\Delta I_{d,\text{max}}$  is 147 mA/mm.

There is a before and after  $I_{d,\text{max}}$  difference of 147 mA/mm, measured at  $V_d = 5$  V and  $V_g = 0.6$  V, considered a significant increase only by passivating a surface of the device. The  $\text{SiN}_x$  passivation introduces external strain into the FinFET so that it induces more piezoelectric polarization charge at the interface. The PECVD grown  $\text{SiN}_x$  gives the AlGaN layer an additive tensile strain resulting in the current increase. Also, the free surface states along the side walls are passivated from the  $\text{SiN}_x$  so that they do not deplete the 2DEG charge from the interface. During the passivation layer deposition, the FinFET sidewalls get healed with the PECVD deposition temperature so that most of trapped charges inside of the structure are possibly released to increase the current. Figure 41

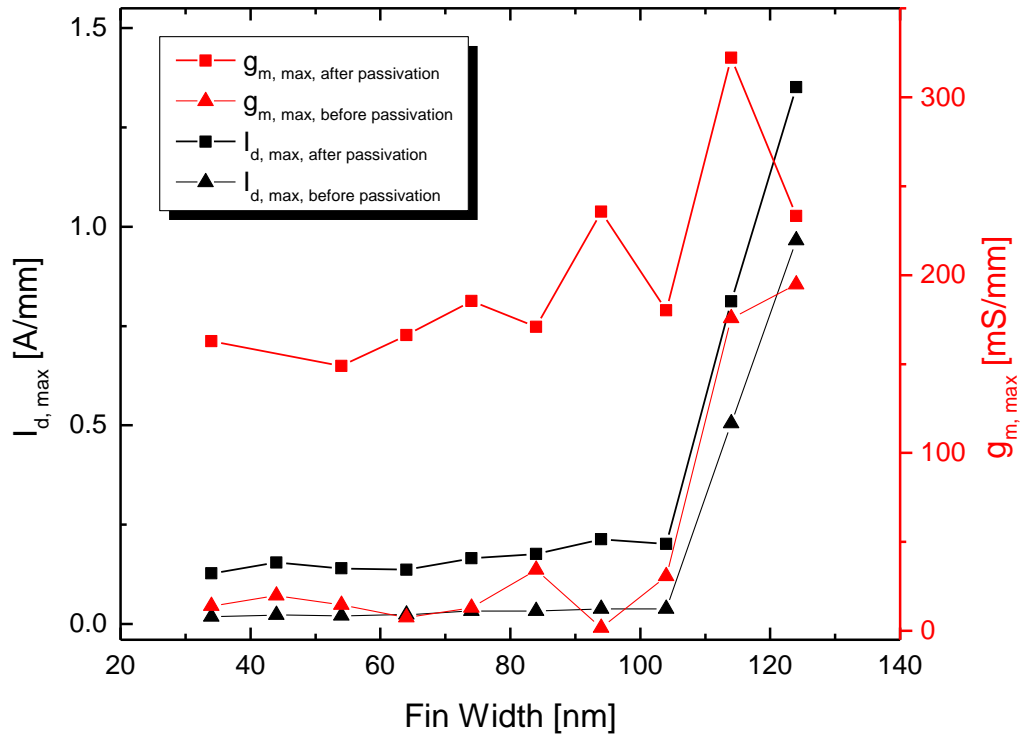


shows  $V_{th}$  variation along with the varied fins width effect with before and after the surface passivation. There could be an effect on the threshold voltage due to the passivation, however, the results show no trend in that regard. It is hard to conclude that any variation could be caused only by the additional passivation layer [15, 46-50]. Experimental process factors should be taken into account as well because BOE is used to open the contact regions to probe after passivation, which causes ohmic contact metal degradation underneath the passivation layer.



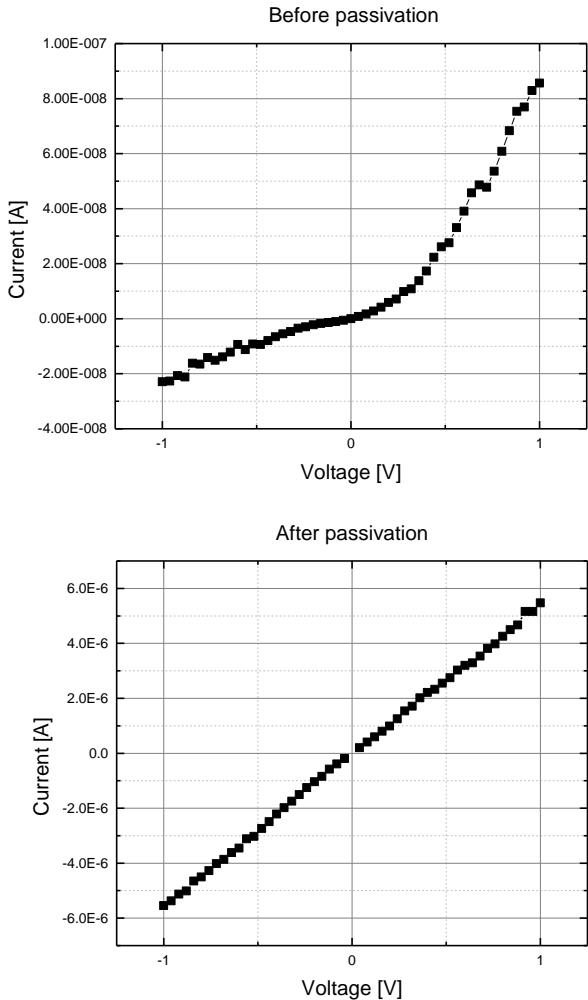
**Figure 41.** A comparison of  $V_{th} - W_{fin}$  curve of the AlGaIn/GaN FinFET before and after PECVD grown  $SiN_x$  passivation.

Transconductance ( $g_{m,max}$ ), increases in accordance with the observed increase  $I_{d,max}$ , as shown in Figure 42.  $I_{d,max}$  and  $g_{m,max}$  are measured at  $V_d = 6$  V and  $V_g = 0.6$  V. The maximum  $g_{m,max}$ , is obtained as 322 mA/mm with  $W_{fin} = 114$  nm.



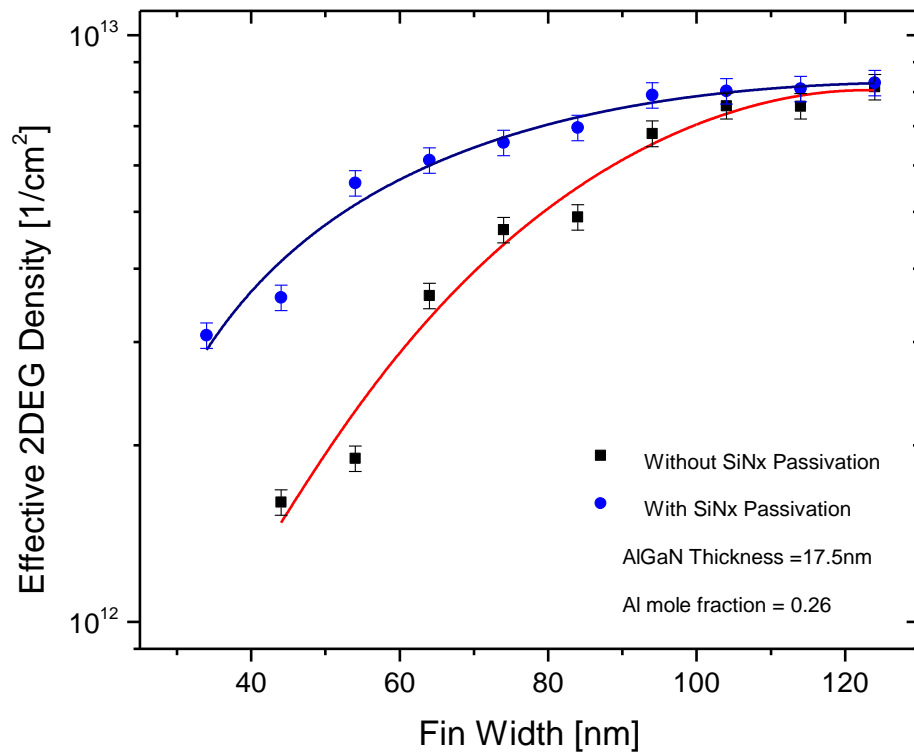
**Figure 42.**  $I_{d,max} - W_{fin}$  and  $g_{m,max} - W_{fin}$  curves of the AlGaIn/GaN FinFET before and after PECVD grown  $SiN_x$  passivation. There are overall  $I_{d,max}$  increase and transconductance,  $g_{m,max}$ , after the passivation.  $I_{d,max}$  and  $g_{m,max}$  are measured at  $V_d = 3$  V and  $V_g = 0.6$  V.

The passivation effect on the fin itself is observed by measuring the current. Figure 43 shows I-V of approximately 34 nm AlGaIn/GaN fin structure before and after the SiN<sub>x</sub> passivation. Before the passivation, there is no ohmic behavior of the fin, however, it shows the ohmic behavior after the passivation. The effect on the recess etched GaN regions (without fins) does not show this effect at all (not shown here).



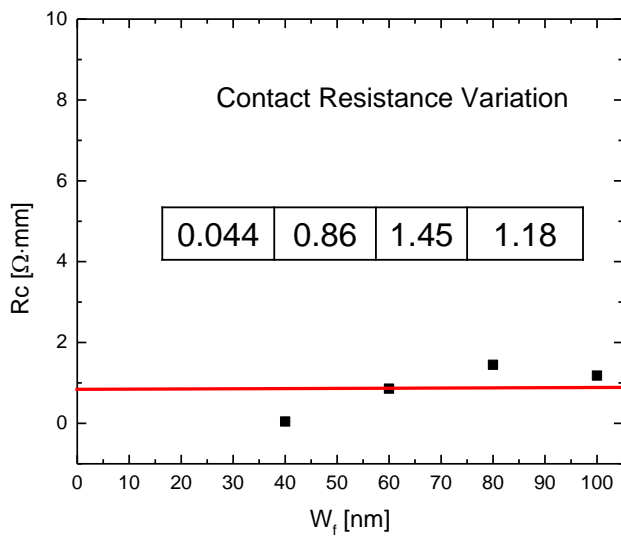
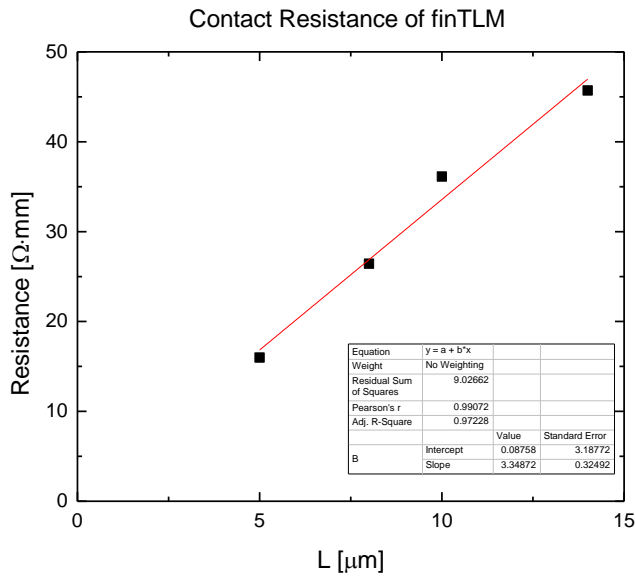
**Figure 43.** Before and after passivation effect on the 34 nm fin shows an ohmic behavior reconstruction.

With the results before and after the passivation on the fins and FinFETs, the effective 2DEG density is calculated using the method introduced in the previous section. As a result, the effective 2DEG sheet density increases by  $\sim 3.7 \times 10^{12} \text{ cm}^{-2}$  at most. It shows a strong dependence of the fin width and the external passivation effect. Figure 44 shows the calculated effective 2DEG density.



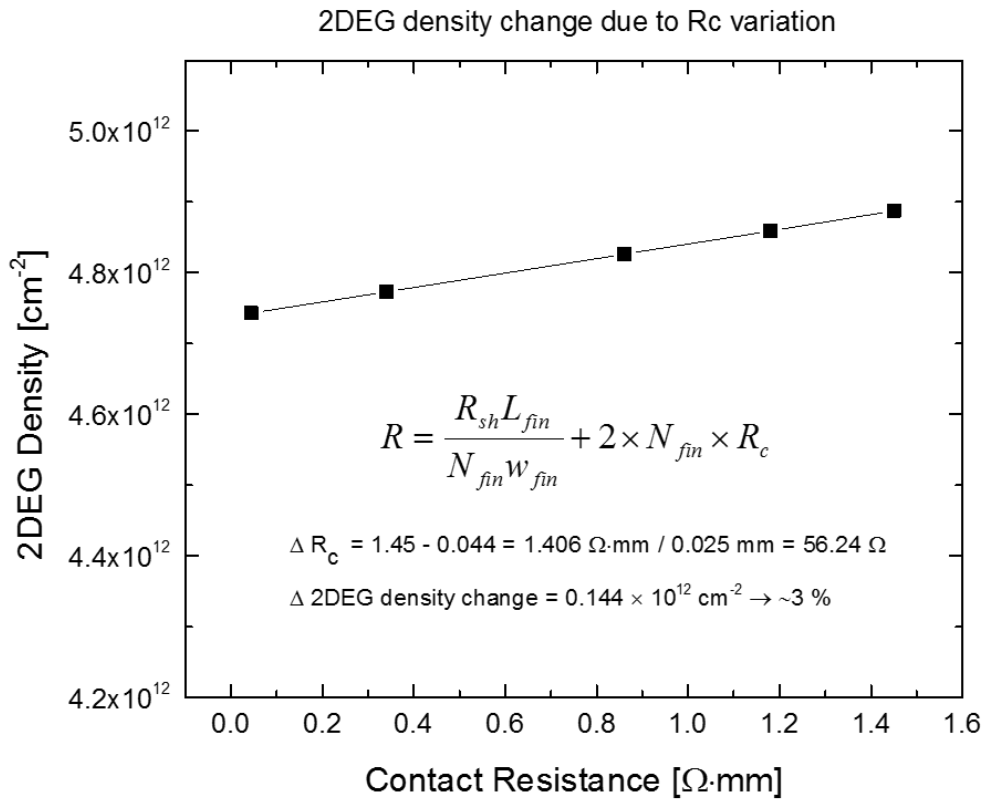
**Figure 44.** Effective 2DEG density curves of AlGaN/GaN FinFET before and after PECVD grown SiN<sub>x</sub> passivation

To see contact resistance effect on the 2DEG density, it is investigated using fin-TLM with different fin-widths. The ohmic contact metal stack is used as introduced in the previous section. The lowest contact resistance is obtained as low as  $0.044 \Omega \cdot \text{mm}$  with the stack ratio of Ta : Al : Ta = 8 : 230:17 nm, shown in Figure 45. As shown in Figure 44, it is clear that the narrower fin exhibits higher sheet resistance,  $R_{\text{sh}}$ , (lower 2DEG density) and width normalized  $R_c$  suggesting improper fin width,  $W_{\text{fin}}$  scaling because  $R_{\text{sh}}$  and normalized  $R_c$  should not depend on  $W_{\text{fin}}$  [51]. In addition to the  $W_{\text{fin}}$ , the fin height,  $H_{\text{fin}}$ , should be taken into account to normalize the contact width over the fins, which the total width is  $(W_{\text{fin}} + 2 \times H_{\text{fin}}) \times \text{number of fins}$ , furthermore,  $H_{\text{fin}}$  is a function of the fin sidewall angle which consequently causes the total width variation. Also, during the etch process, there is an induced damage by high power plasma on the sidewalls which creates higher sheet resistance. Along the sidewalls, there may be a regions that does not contribute to charge transport, which can be called a dead zone and it could exist as a depletion region of the fin sidewalls associated with Fermi level pinning at the fin sidewall surface [51]. The fin structure has 3 surfaces exposed during the entire device fabrication procedure. Figure 45 shows that contact resistance dependency on the fin width variation with the process and calculation error. When the contact width normalization is performed, the fin angle from the previous TEM image is also considered for the accurate calculation and extraction. Red line indicates a corrected and averaged contact resistance along with the fin width variation.



**Figure 45.** Contact resistance dependency on the fin width variation with the process and calculation error. Red line indicates a corrected contact resistance along with the fin width variation.

According to the precisely considered contact resistance extraction, the contact resistance effect on the 2DEG density is calculated in Figure 46. By taking into account of a maximum difference of the contact resistance obtained in Figure 45, the possible variation of the 2DEG density is within 3 % of the original density. While this may seem to be insignificant, such a variation could be detrimental when the process is applied to very large scale integration architectures.



**Figure 46.** Contact resistance effect on the 2DEG density of AlGaIn/GaN device.

## CHAPTER VI

### ALGAN/GAN FINFET DESIGN PARAMETER EFFECT ON THE DEVICE

#### CHARACTERISTICS

##### **Introduction**

Electrical characteristics of AlGa<sub>N</sub>/Ga<sub>N</sub> FinFET device is explored according to the device design parameters such as fin height, width, length, and sidewall angle, using the fabrication process techniques previously developed. However, a significant challenge in III-Nitride device fabrication process is of the structural and chemical robustness of Ga<sub>N</sub>, due to the high bond strength and wide bandgap. This is advantageous for high power and high frequency application using Ga<sub>N</sub> material properties, however it induces great challenges to device fabrication processing. One of the most difficult challenges has been etching group III-nitride materials at a reasonable etch rate. Due to its high chemical stability, it is difficult to wet-etch Ga<sub>N</sub> compared to other III-V semiconductor materials and thus the most common etching technique used has been chlorine or fluorine-based reactive ion etching (RIE). High energy ion bombardment is required for etching, causing surface damage to the Ga<sub>N</sub> which can degrade the device performance with surface roughness, additional leakage paths, and interface states [22, 24, 52, 53]. Also, it is hard to control the shape of the features, especially on vertical sidewalls, facades of Ga<sub>N</sub> mesa structures only by the dry etching technique itself because of a limitation on anisotropy depending on crystal orientation direction of the wurtzite structure and dopants type in Ga<sub>N</sub> [54, 55].



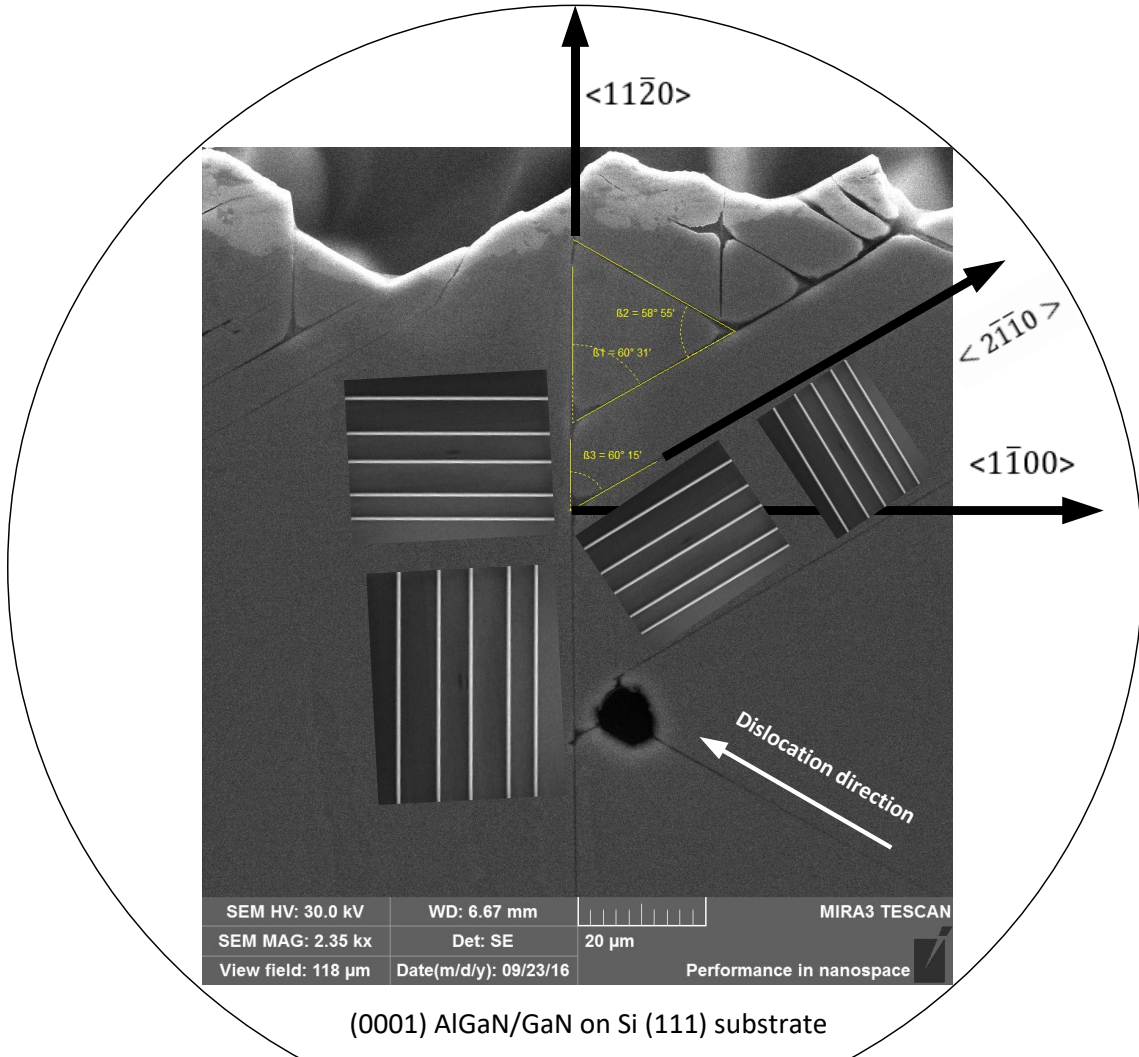
Here specific sidewall angle processes are introduced to control fin sidewall profiles. This is accomplished by using additional wet-etching process followed by dry etching process (RIE) introduced in the previous section.

### **Fin sidewall control using the combination of RIE and wet etching process**

Several chemical solutions in the literature have been demonstrated for wet etching process of GaN such as aqueous solution of potassium hydroxide (KOH) and tetra-methyl-ammonium hydroxide (TMAH) mixed with H<sub>2</sub>O solution. These are widely used anisotropic etchants to etch GaN even though the etch rate is slow and have a polarity and doping dependency of grown GaN layer [8, 55-58]. These solutions require elevated etchant temperatures and proper concentrations so that adequate etch rate can be achieved for GaN material. The combination of dry and wet etching processes is realized with the utilized etch solution for the purpose of sidewall control, reduction of surface roughness, and removal of surface damage as GaN crystal bonds are physically discontinued, or broken during high power plasma ICP-RIE process.

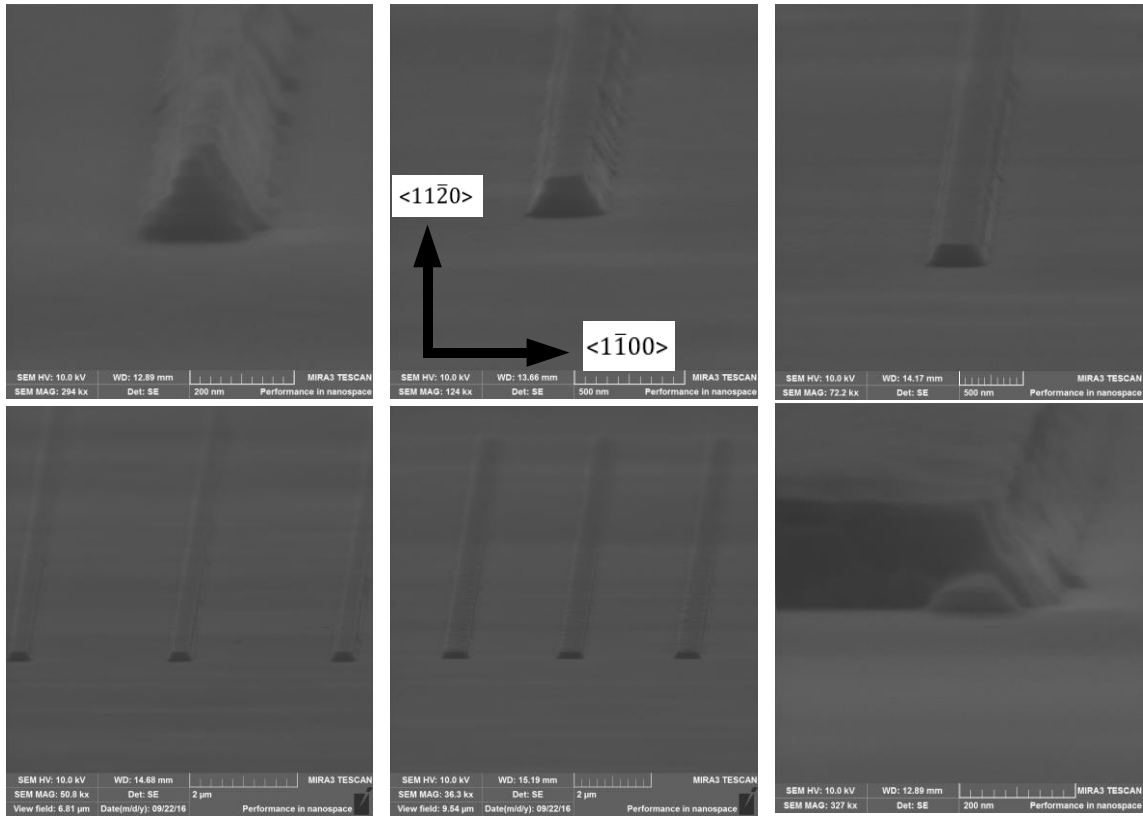
Using the previously introduced ICP-RIE recipe with the flow rates of 40 sccm SF<sub>6</sub> and 10 sccm Ar at the pressure of 44 mTorr at the temperature of 13 °C with RF power of 200 W and ICP of 300 W on AlGaIn/GaN surface, the fin etch profiles are obtained along with different crystal orientation. The fins are fabricated in parallel to the crystal directions of  $\langle 1\bar{1}00 \rangle$ ,  $\langle 2\bar{1}\bar{1}0 \rangle$ ,  $\langle 11\bar{2}0 \rangle$  and  $\langle 01\bar{1}0 \rangle$ . Figure 47 shows the fabricated fins before the wet etch process along with the actual crystal orientation of AlGaIn/GaN on Si (111) substrate. The substrate shows the induced dislocation expansion along the crystal direction during additional wet etch process using 25 % TMAH. The

dislocations get together at the structure vertex and create huge pits. The further effect of the TMAH etching is explained in next section.



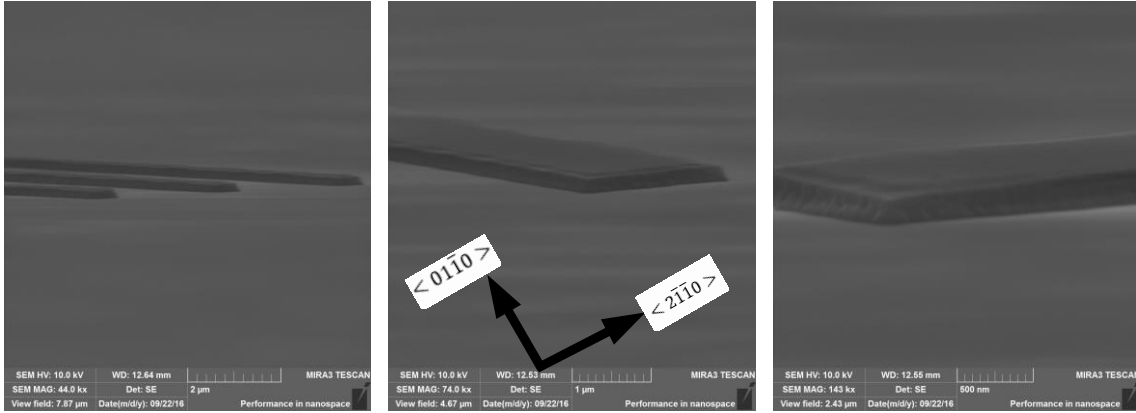
**Figure 47.** Fabricated fin structure mapping on AlGaIn/GaN on Si (111) substrate. This substrate shows induced dislocation growth along the crystal direction after 25 % TMAH etching for approximately 17 hours.

Figure 48 shows the fin profiles immediately after ICP-RIE process using SEM and the fins with various  $W_{fin}$  formed along with the crystal direction of  $\langle 11\bar{2}0 \rangle$ .



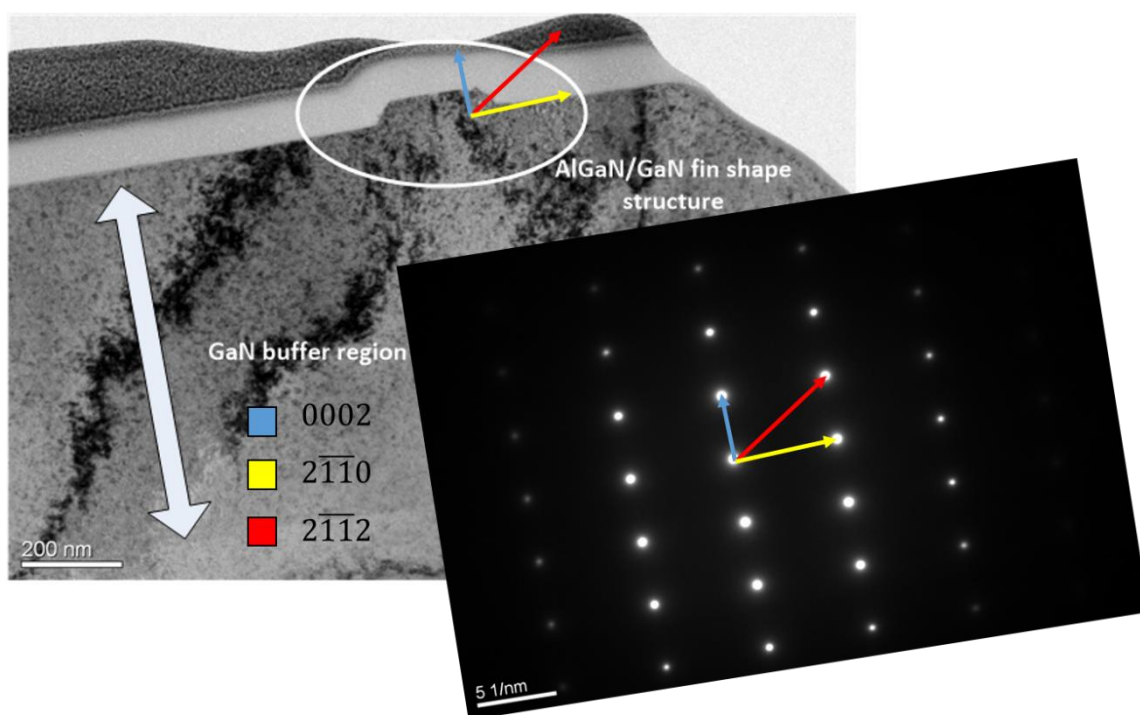
**Figure 48.** AlGaIn/GaN fin formation along  $\langle 11\bar{2}0 \rangle$  crystal direction after ICP-RIE process for 5 minutes.

Figure 49 shows the fin profiles immediately after ICP-RIE process using SEM and the fins with various  $W_{\text{fin}}$  formed along with the crystal direction of  $\langle 01\bar{1}0 \rangle$  and  $\langle 2\bar{1}\bar{1}0 \rangle$  are shown in Figure 49.

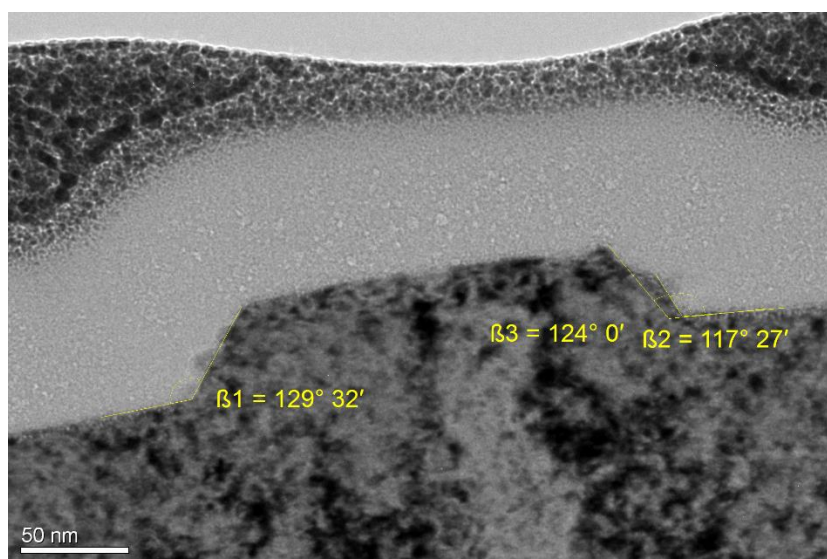


**Figure 49.** AlGaIn/GaN fin formation along  $\langle 01\bar{1}0 \rangle$  crystal direction after ICP-RIE process for 5 minutes.

TEM micrographs show the detailed fin profile and the fin formed along with the crystal direction of  $\langle 01\bar{1}0 \rangle$  in Figure 50, including a TEM diffraction pattern image. Measured fin sidewall internal angle is approximately  $63^\circ$ . However, the fin structure has a damaged top corner with two different angles formed as shown in Figure 51. The measured internal angles are approximately  $51^\circ$  and  $63^\circ$ . The collapsed corners could be attributed to a surface defect during the  $\text{SiN}_x$  deposition using PECVD or line roughness after Cr lift-off as a metal etch mask. The etch stop masks may not endure long enough during the ICP-RIE process.

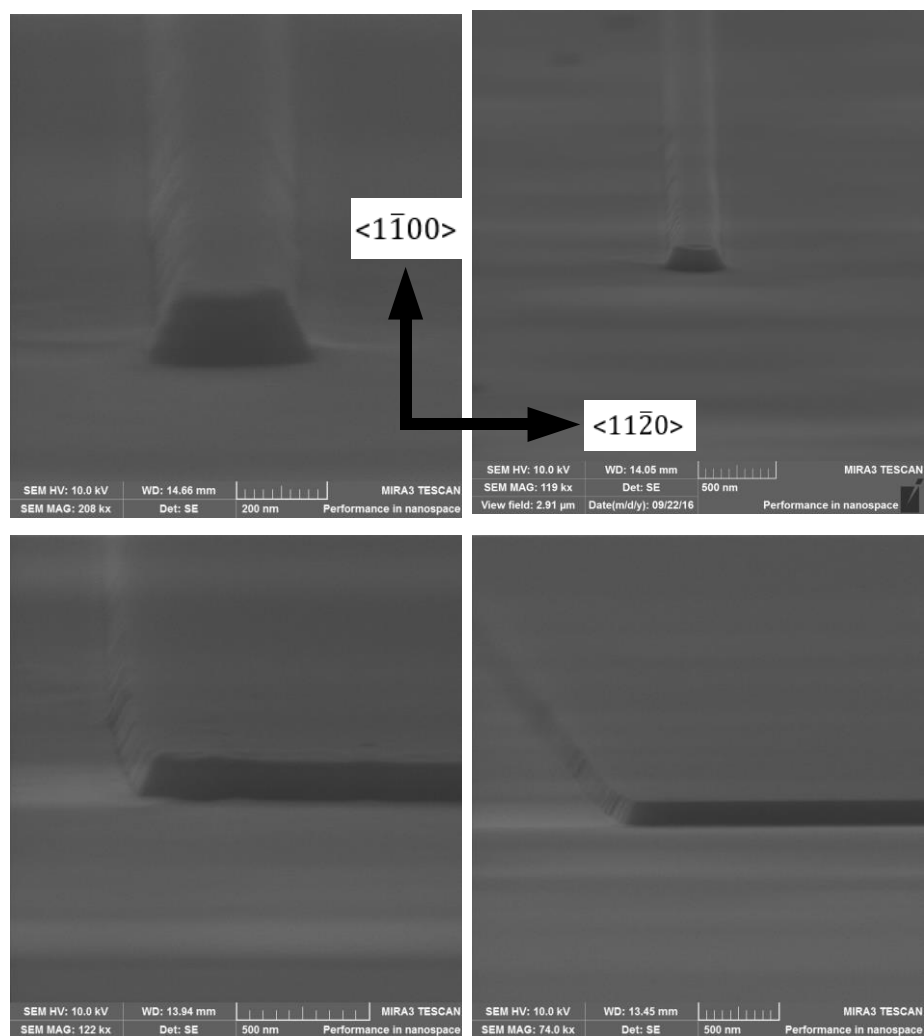


**Figure 50.** TEM image of the cross-sectional view of a fin along with the crystal direction of  $\langle 01\bar{1}0 \rangle$ . Measured fin sidewall internal angle is  $63^\circ$ .



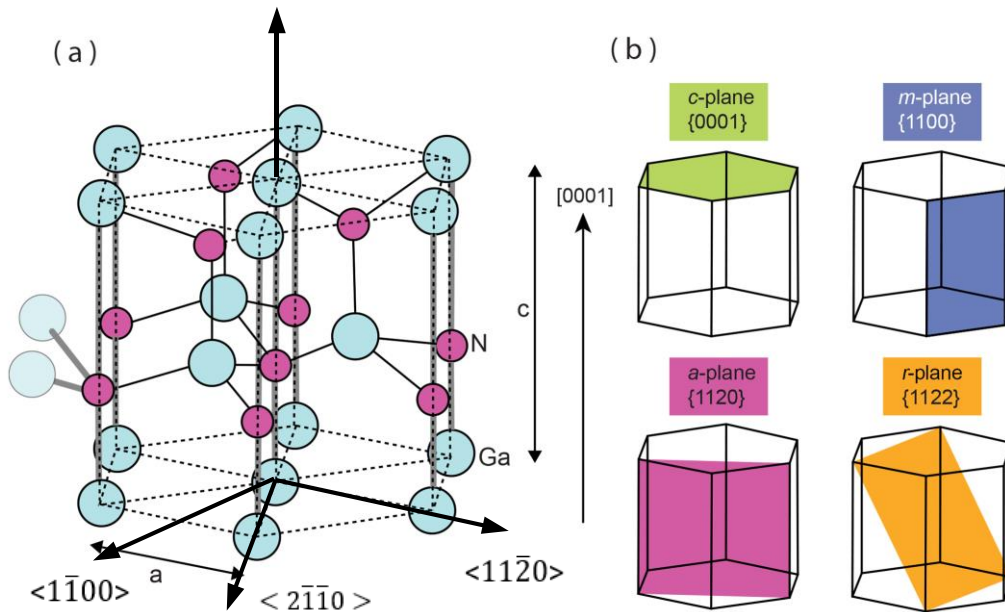
**Figure 51.** TEM image of the cross-sectional view of a fin with the sidewall collapse issue.

Figure 52 shows the fin profiles immediately after ICP-RIE process using SEM and the fins with various  $W_{fin}$  formed along the  $\langle 1\bar{1}00 \rangle$  crystal direction.



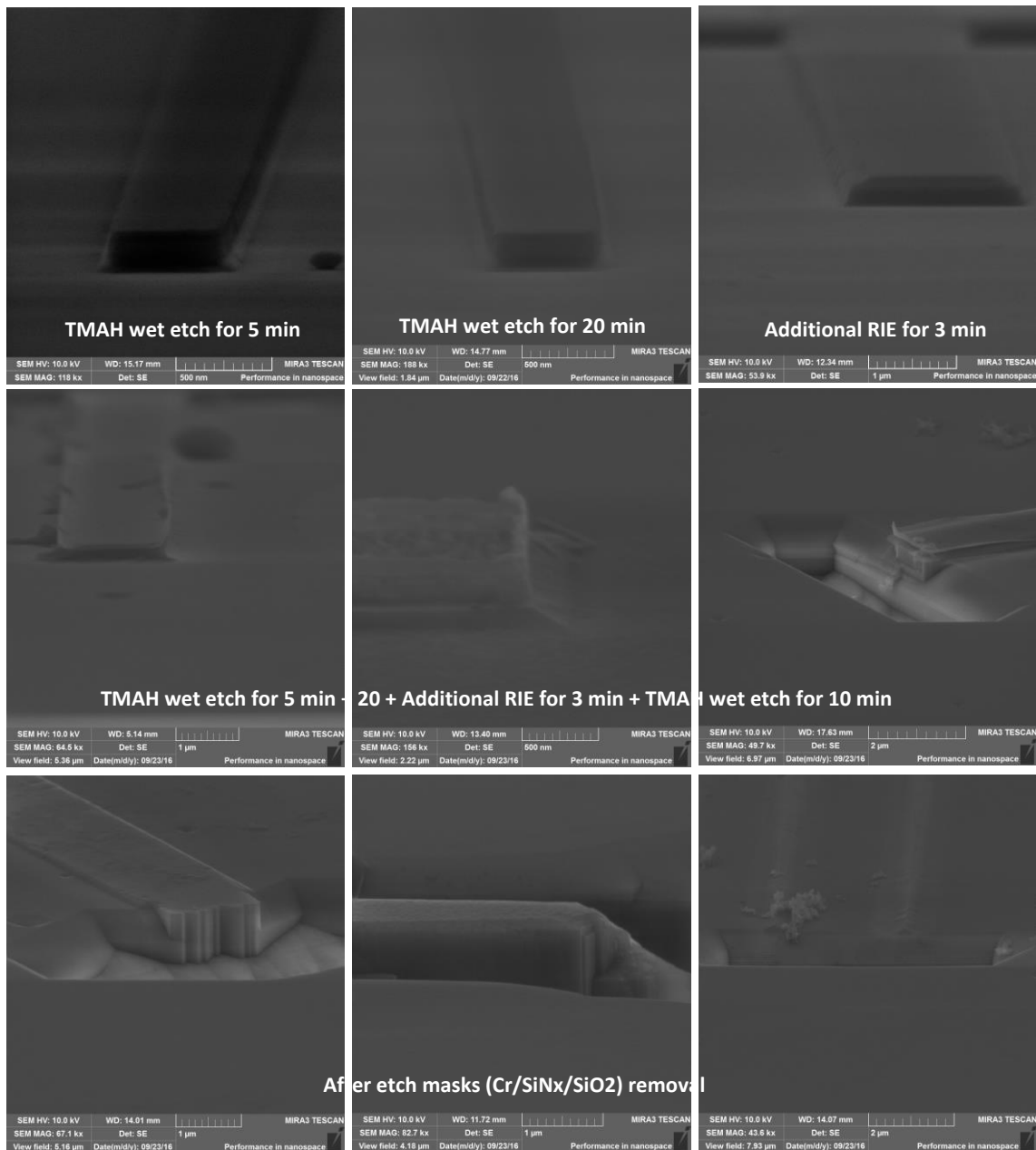
**Figure 52.** AlGaIn/GaN fin formation along  $\langle 1\bar{1}00 \rangle$  crystal direction after ICP-RIE process for 5 minutes.

GaN wurtzite structure is revisited to show the atomic level crystal orientation in the hexagonal unit cell and each basal plane of the structure in Figure 53.



**Figure 53.** (a) Hexagonal unit cell of GaN wurtzite structure with crystallographic directions and (b) its basal planes.

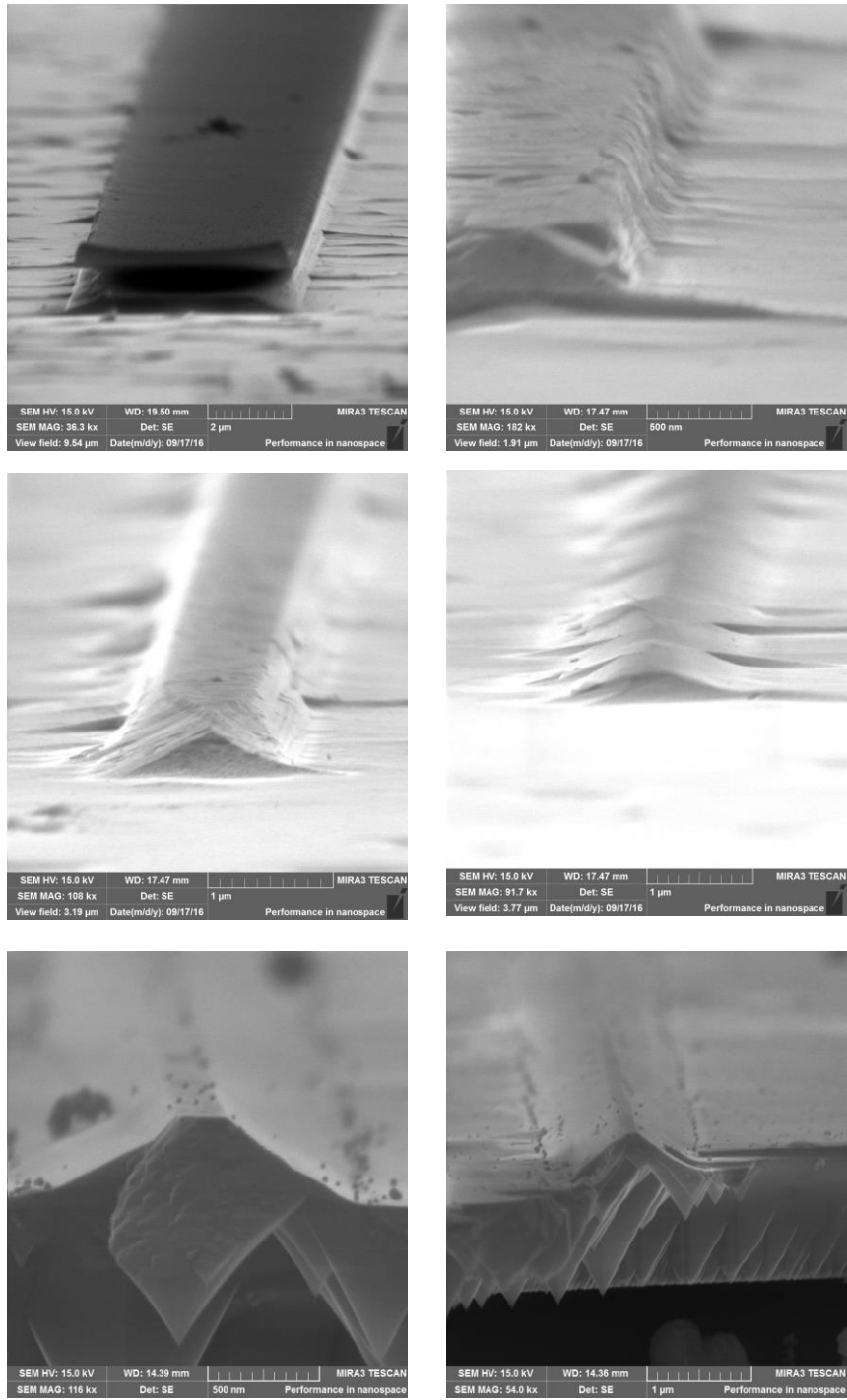
After the ICP-RIE etch process, wet etch process is performed using 25 % TMAH etch solution and the chemical temperature is elevated on the hot plate to 85 °C ~ 90 °C. Then, the fin-formed substrates are immersed into the solution for 5 minutes, 20 minutes, subjected to another ICP-RIE for 3 minutes, and a final wet-etching for 10 minutes before the etch masks are removed. The etch progress in the fins according to additional etching time is shown with the fins along the crystal direction of  $\langle 11\bar{2}0 \rangle$  in Figure 54.



**Figure 54.** Fin profiles taken by SEM after 25 % TMAH additional different etch process time at 85 °C with the fins along with the crystal direction of  $\langle 11\bar{2}0 \rangle$ .



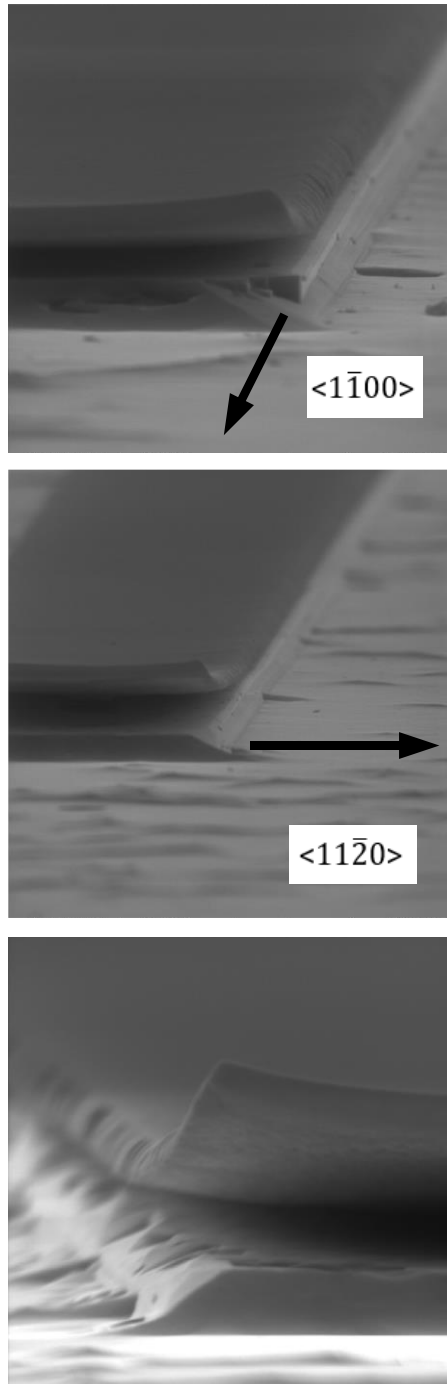
The steep sidewall of the AlGaIn/GaN fin structure is achieved. After 5 minutes of etching, anisotropic behavior of TMAH is observed as the vertical fin shape is formed. The supporting pillar region of the fins are in the buffer GaN region, which may not have an effect on the final device performance. The interesting region is at the AlGaIn/GaN interface which involves 2DEG region, located about 20 nm below the top surface. The height impact on the AlGaIn/GaN FinFET device is investigated in the following section. The vertically formed AlGaIn/GaN fin structure is shown in the top right of Figure 55. The prism-like shape is also observed on the facade side of the fins and it is due to the m-plane in the crystal direction of  $\langle 11\bar{2}0 \rangle$  periodically. Similar observation is made in the previously reported literature [54, 55]. In the case of a triangular shape fin formation after the long etch, it is found out that the mask layers are not stuck onto the top region of the fin facade at the interface. After losing the etch mask layers, the facade region gets attacked and has the lateral etching process which forms a triangular fin shape. Also, the triangular fin shape is reported in the literature with a directional preference in the direction of  $\langle 11\bar{2}0 \rangle$  after an etch process [59]. The triangular shape fin formation progress is shown in Figure 55.



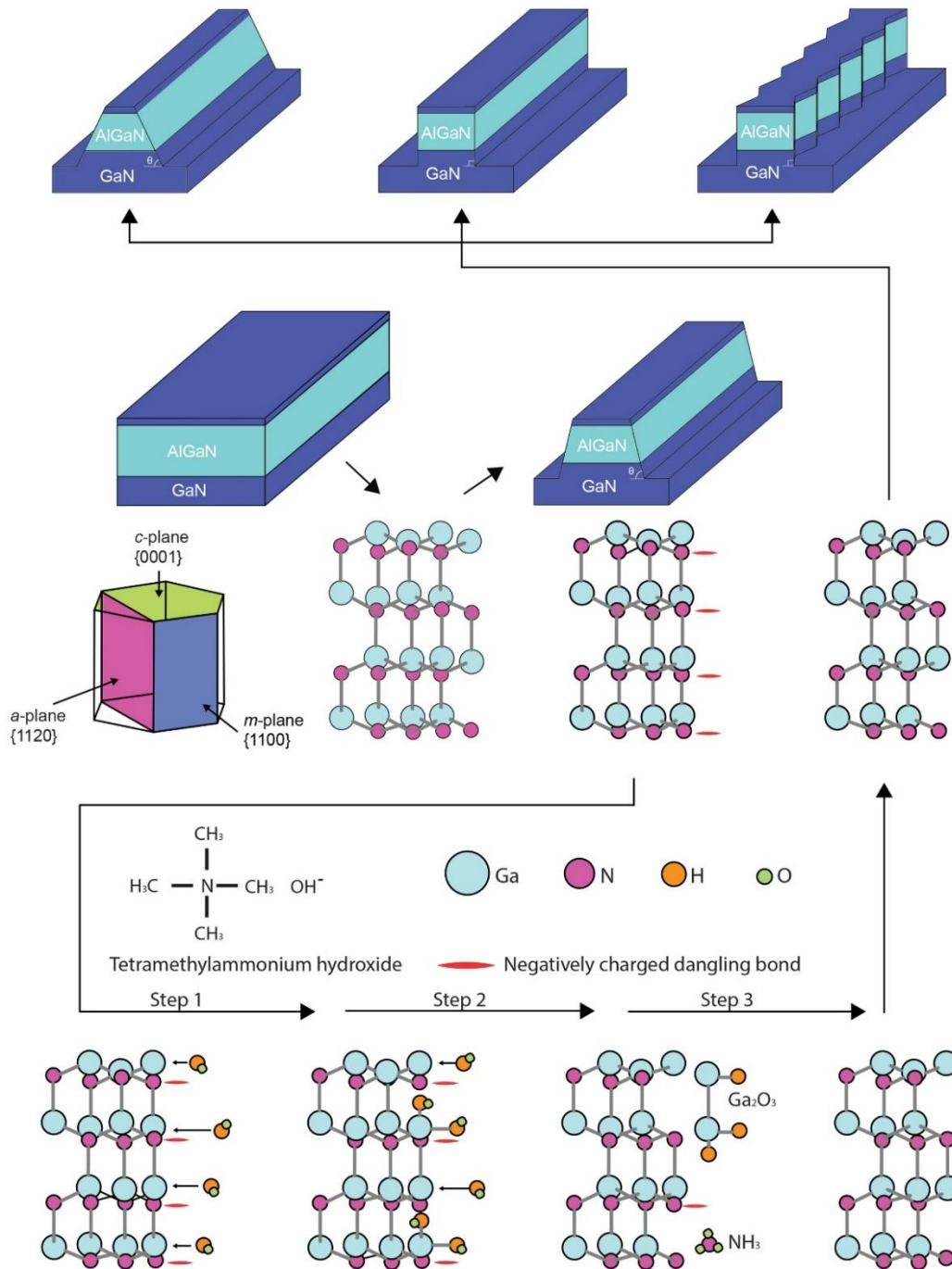
**Figure 55.** Triangular shape of fin formation progress with additional etching time and with crystal orientation preference along the direction of  $\langle 11\bar{2}0 \rangle$ .

This data proves that a TMAH solution can etch only in the lateral direction of a GaN structure from strongly anisotropic etching characteristics. Having an additional TMAH wet etching along with the direction of  $\langle 11\bar{2}0 \rangle$ , the fin shape is changed from the trapezoidal shape to a narrower vertical rectangle with a steep sidewall angle, however, the etching along the direction of  $\langle 1\bar{1}00 \rangle$  maintains the trapezoidal shape even after the long etching time. The similar observation is made in the previous literature [54]. Figure 56 confirms that the effect of the etching performance based on the direction of the crystal orientation and the etch process is done for 10 minutes at 90 °C. The etch rate finding comes out to be approximately 20 nm/min along the lateral direction.

The chemical reaction between TMAH and water ( $\text{H}_2\text{O}$ ) shows as  $(\text{CH}_3)_4\text{NOH} + \text{H}_2\text{O} \rightarrow (\text{CH}_3)_4\text{N}^+ + \text{OH}^- + \text{H}_2\text{O}$ . During the ICP-RIE dry etching, high energy ion bombardment is active, so relatively high N-rich face is exposed on the surface of trapezoidal sidewall compared to the c-plane Ga-face [60]. The higher lateral etch rate on this sidewall removes the trapezoidal shape [61]. The possibly chemical reaction between GaN and the TMAH solution is depicted in Figure 57 [55].



**Figure 56.** SEM image of the cross-sectional fin image after 10 minutes 25 % TMAH etching process and it shows clear effect on the fin sidewall angle along the direction of the crystal orientation (top etch mask (Cr) / second etch mask ( $\text{SiN}_x$  /  $\text{SiO}_2$ ) over AlGaIn/GaN fin structure) .



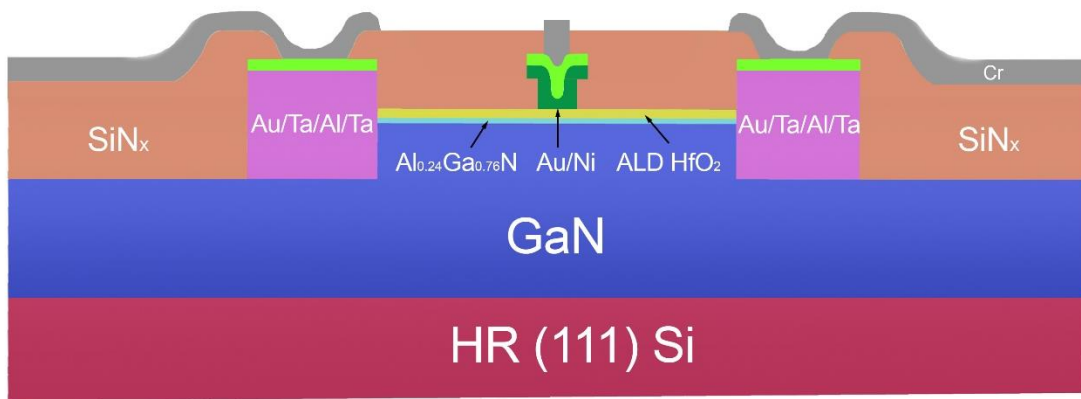
**Figure 57.** Graphical schematic illustration for the steps from bare AlGaIn/GaN substrate before ICP-RIE mesa isolation process to AlGaIn/GaN fin structure with different sidewall angles after ICP-RIE and subsequent TMAH wet etching process.

## **Effect on electrical characterization based on AlGaIn/GaN FinFET design parameters**

The device electrical performances are measured to validate the impact of the device design parameters according to fin width ( $W_{fin}$ ), fin height ( $H_{fin}$ ), fin sidewall angle ( $\Theta_{fin}$ ) including TMAH etch effect after all of the AlGaIn/GaN FinFET fabrication procedures are thoroughly investigated and optimized to measure electrical characteristics of the 3D devices.

Device fabrication starts with the surface cleaning and preparation: 1) solvents clean using Acetone / Methanol / IPA for hydrocarbon removal followed by a 10 minutes native oxide strip in the solution of 1: 10 = HCl : DI-H<sub>2</sub>O and followed by BOE clean for 5 minutes. Immediately after the cleaning procedure, SiN<sub>x</sub> deposition is made by PECVD system as an etch buffer layer with a thickness of 70 nm SiN<sub>x</sub>. After various fin widths patterning by EBL system, 70 nm Cr etch stop layer is deposited and lifted off using Acetone. Using the fluorine-based ICP-RIE as described in the previous section, the AlGaIn/GaN fins are defined as isolated mesa structure. After etching Cr/SiN<sub>x</sub> is stripped using Cr etchant and BOE. Aligning the fins to have S/D ohmic contact regions using the EBL system, the S/D contact regions are defined. Using e-beam evaporator and sputter, Au (30 nm) / Ta (170 nm) / Al (230 nm) / Ta (7 nm) are deposited and lifted off in acetone. The substrate gets annealed in the RTP system for 240 seconds at 575 °C in N<sub>2</sub> ambient. 150 cycles of HfO<sub>2</sub> is deposited by ALD system. The gate region is patterned by the EBL system and Au (70 nm) / Ni (230 nm) are deposited and lifted off. And 300 nm of SiN<sub>x</sub> is deposited all over the substrate using PECVD system for the field isolation dielectric.

To make via connections to S/D and gate regions, window regions are patterned using EBL and open by etching the field  $\text{SiN}_x$  by BOE. Using EBL system, the final contact regions are aligned to the S/D and gate window opening regions and patterned. The final contact metal of 250 nm Cr is evaporated and lifted off. The fabricated device is depicted in Figure 58.

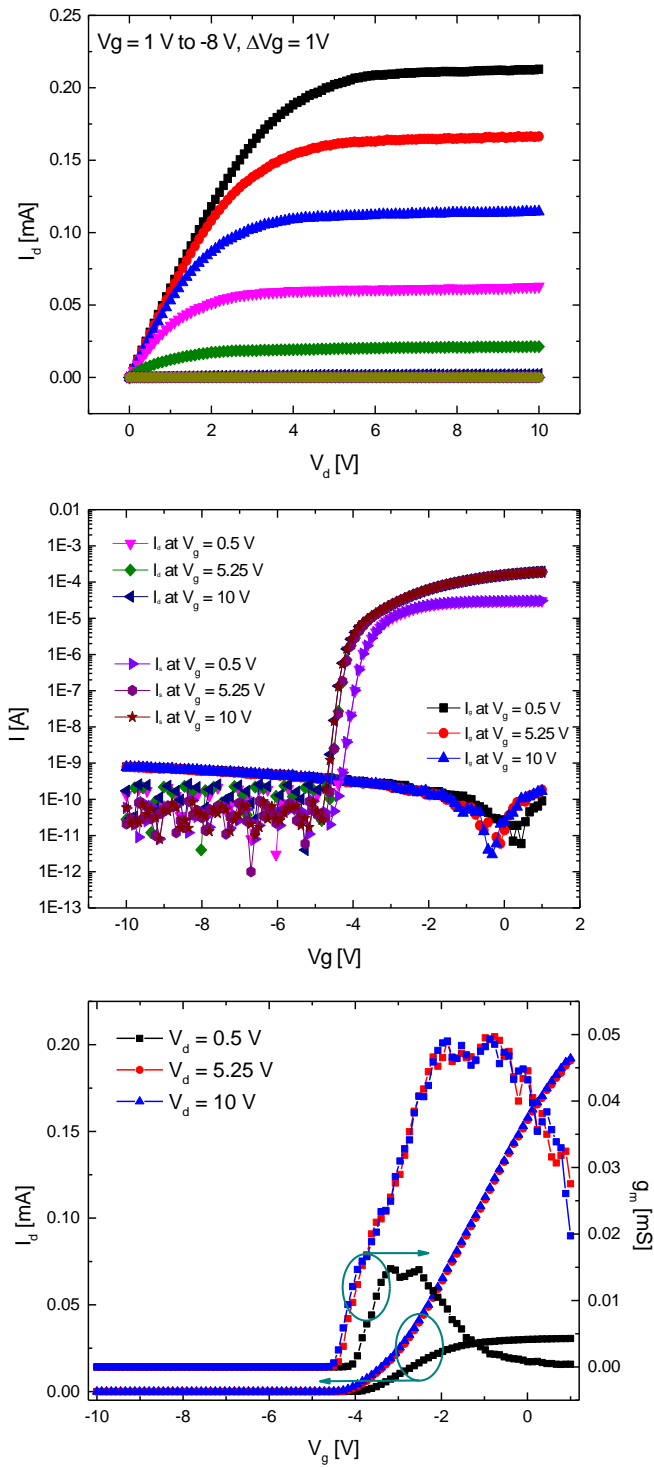


**Figure 58.** A schematic of AlGaN/GaN FinFET device is depicted including the via connection

Au is newly introduced in this process due to the ohmic contact degradation after S/D contact window opening with BOE etchant. Without degrading the contact resistance, addition Au layer protects the ohmic contact metal stack. As an interconnecting metal contact line, Cr is chosen after the issue with the adhesion of Ni on  $\text{SiN}_x$  field layer.

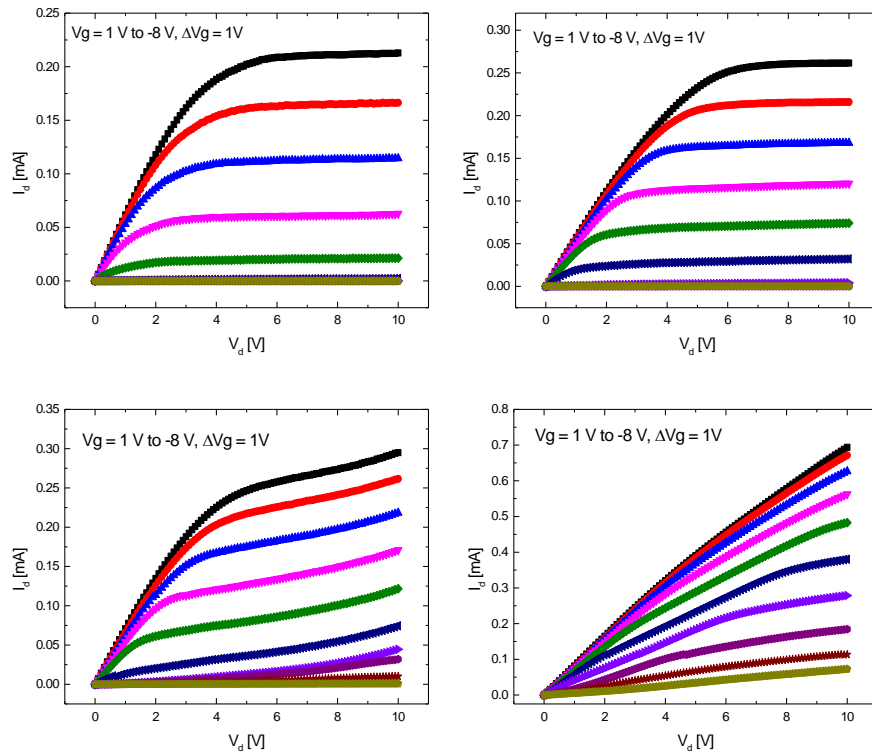
The AlGa<sub>N</sub>/Ga<sub>N</sub> FinFET device output and transfer characteristics are shown in Figure 59. Large device output currents are achieved with an  $I_{on}/I_{off}$  ratio of  $10^7$  which from the  $I_d$ - $V_g$  current profile in Figure 59, the extracted threshold voltage comes out to be  $V_{th} = -3.31$  V at  $V_d = 10$  V at the maximum of  $g_m$  and subthreshold swing (SS) of 98 mV/dec at  $V_d = 10$  V. Larger gate voltage swing and higher linearity are observed as compared to the previously reported literatures [62, 63]. Drain-induced barrier lowering (DIBL) is observed as 47.95 mV / V using the values at  $V_d = 0.5$  V and  $V_d = 10$  V.





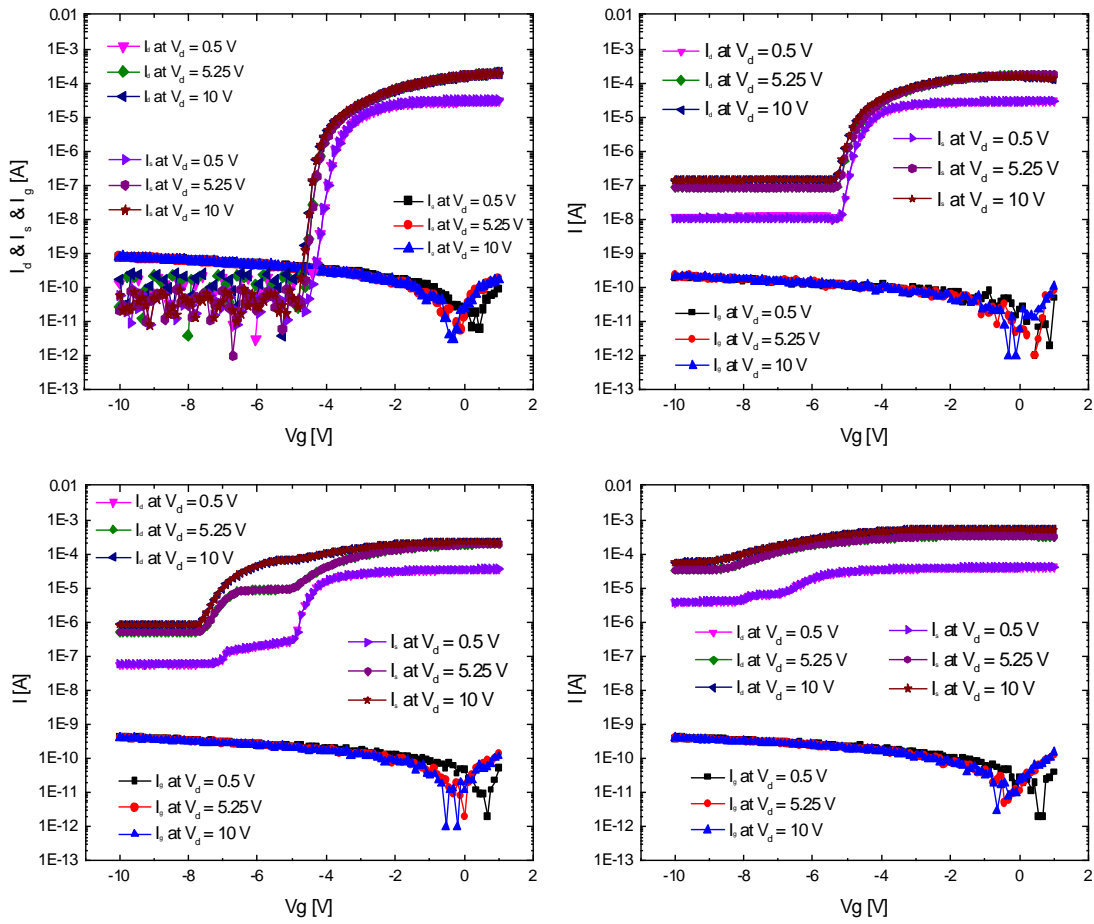
**Figure 59.** An output characteristic of  $I_d - V_d$  versus  $V_g$ , and transfer characteristics of  $I_d$ ,  $I_s$ ,  $I_g - V_g$  and  $g_m$  profiles.

Additional thermal effects on the AlGaIn/GaN FinFET devices are investigated by performing RTP annealing in N<sub>2</sub> ambient at 575 °C, 675 °C, and 755 °C for 4 minutes. Maximum output currents increase with higher temperature anneals and the device is less sensitive on the gate control, as shown in Figure 60. After annealing process at 675 °C, the channel length modulation effect is observed and could be an issue if higher temperature annealing process is required. Even after annealing process 757 °C, it is not able to turn off and the device does not work properly.

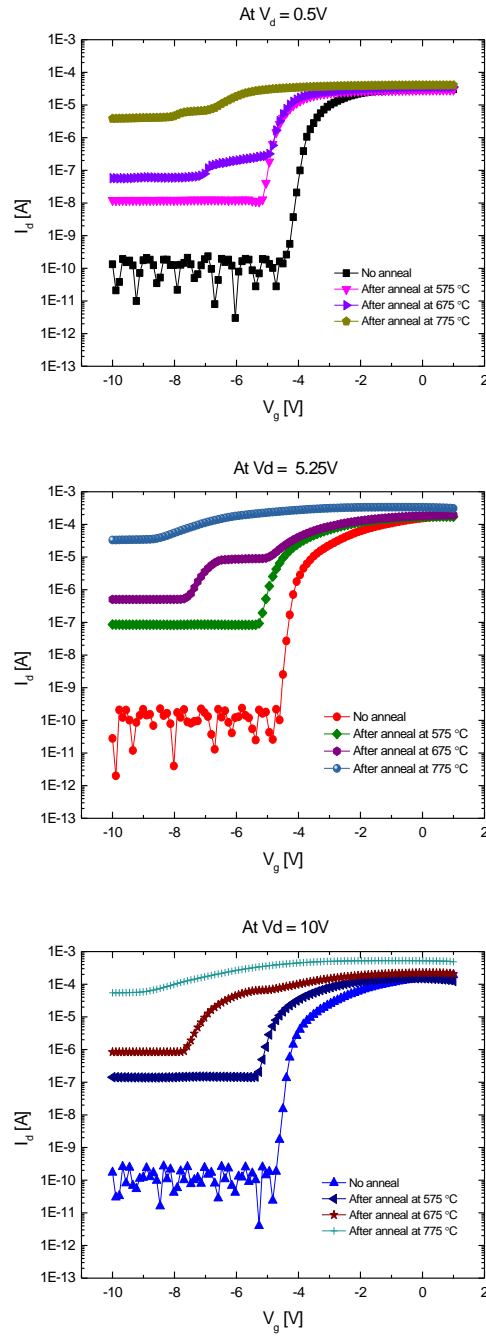


**Figure 60.** Output characteristics of  $I_d - V_d$  versus  $V_g$  after additional annealing process from top-left to bottom-right at no anneal, 575 °C, 675 °C, and 755 °C, respectively.

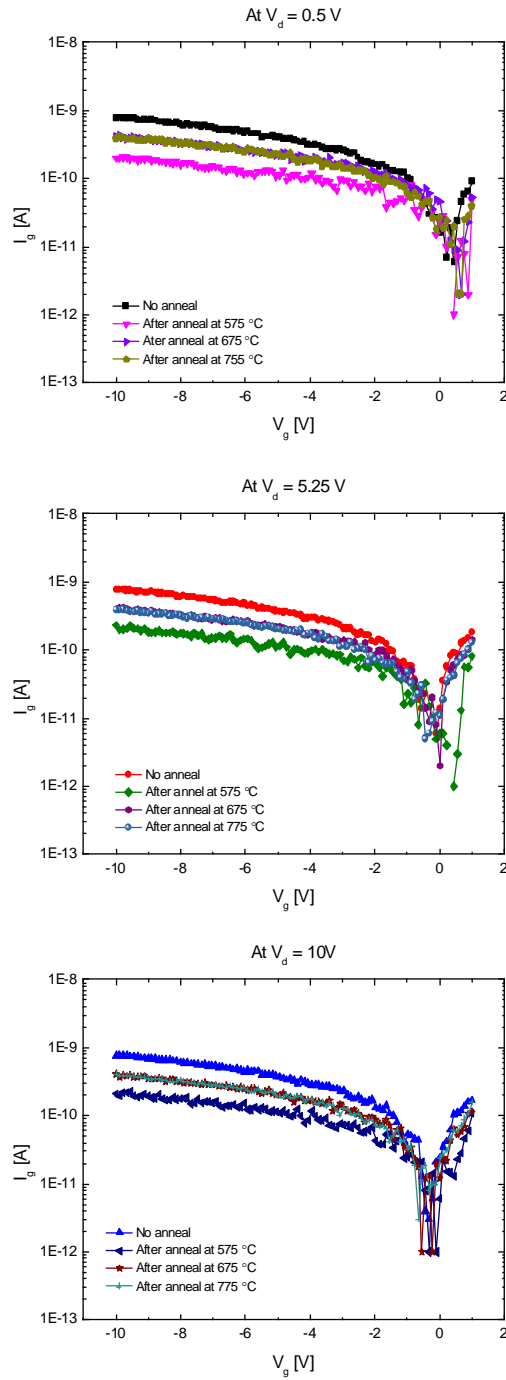
The behavior of the device on-current and off-current, and leakage currents are observed after each annealing process, as shown in Figure 61. A slightly better gate-leakage is induced after the additional anneal processes. However, most of the device off-current or leakage currents are increased more than  $10^5$  after the 757 °C. This tells that the fabricated gate stack is very strong at withstanding external thermal anneal. However Ga atoms predominantly reacted with gate dielectric layer of HfO<sub>2</sub> and formed GaO<sub>x</sub> including GaO and GaO<sub>2</sub> at the Ga / HfO<sub>2</sub> interface [63] which leaves Ga vacancies on the surface and fin sidewalls. This could be attributed to the surface and fin sidewalls with Fermi level shifting toward the valance-band edge so that the increased leakage currents could be from the fin-sidewalls. For the better comparison of the annealing effect data, it is replotted in Figure 62 and Figure 63.



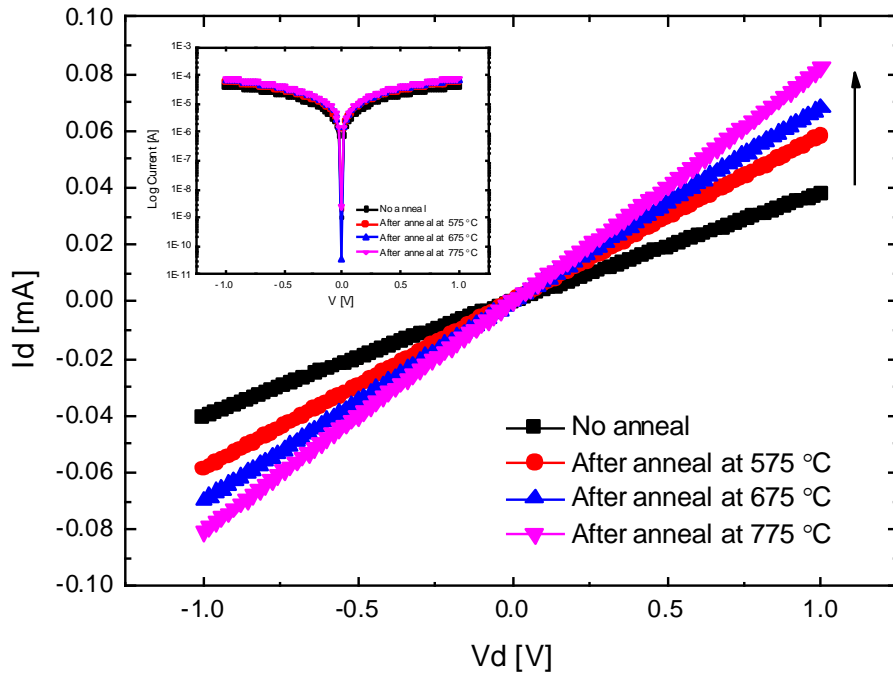
**Figure 61.** Transfer characteristics of  $I_d$ ,  $I_s$ ,  $I_g - V_g$  at three different  $V_d = 0.5$  V, 5.25 V, and 10 V after additional annealing process at no anneal, 575 °C, 675 °C, and 775 °C, respectively. (figures from top-left to bottom-right)



**Figure 62.** Transfer characteristics of  $I_d$ ,  $I_s - V_g$  at three different  $V_d = 0.5 V$ ,  $5.25 V$ , and  $10 V$  after additional annealing process at no anneal,  $575\text{ }^\circ\text{C}$ ,  $675\text{ }^\circ\text{C}$ , and  $755\text{ }^\circ\text{C}$ , respectively.



**Figure 63.** Transfer characteristics of  $I_g - V_g$  at three different  $V_d = 0.5 \text{ V}$ ,  $5.25 \text{ V}$ , and  $10 \text{ V}$  after additional annealing process at no anneal,  $575 \text{ }^\circ\text{C}$ ,  $675 \text{ }^\circ\text{C}$ , and  $775 \text{ }^\circ\text{C}$ , respectively.



**Figure 64.** I-V characteristic of the fine before and after the SiN<sub>x</sub> passivation.

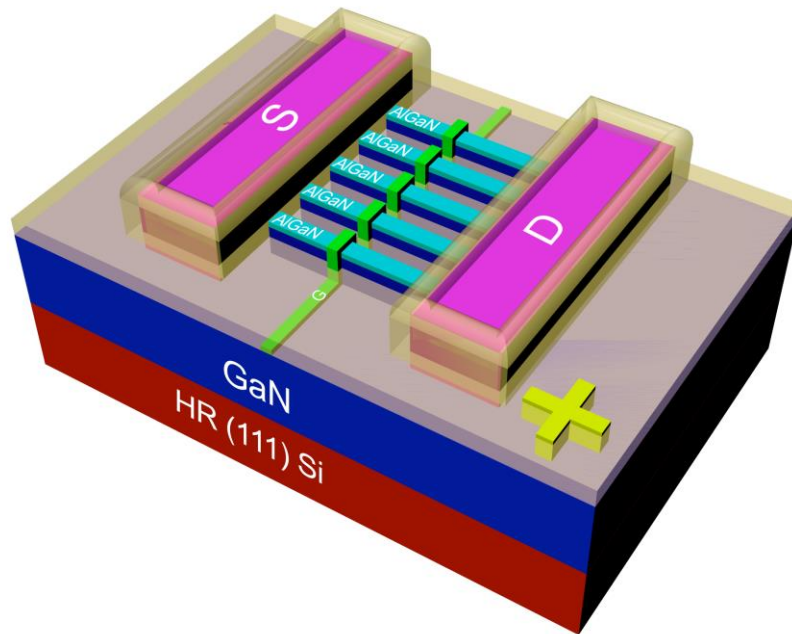
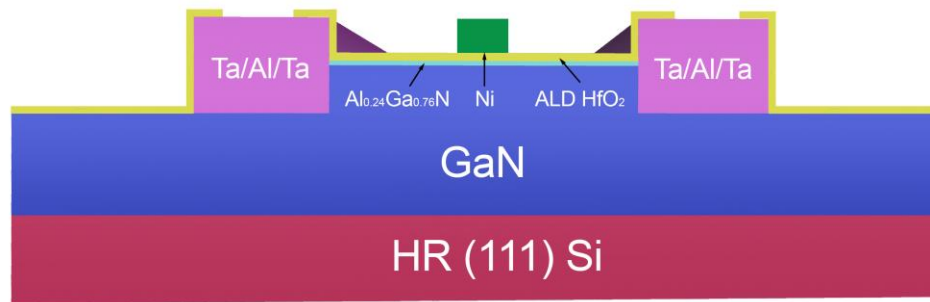
At  $V_g = 0$  V, the current level change of  $I_d - V_d$  is observed as annealed and additionally at higher temperature, as shown in Figure 64. This is attributed that the RIE damage and defects of the fin sidewalls and recess etched GaN field region gets reduced as well to reduce scattering effect from the surfaces. The source of these increase is under investigation for further understanding.

### **Non-via fabrication process for simpler device fabrication and less cost**

A simpler AlGaN/GaN FinFET device fabrication process is introduced to reduce time and cost while maintaining similar device performance. From Figure 64 and 65, it is confirmed that recess etched GaN region (non-active region of the device) has a relatively low current level,  $\sim 10^{-9}$  A at the bias condition of 10 V. It proposes the device fabrication by skipping via integration and field isolation steps from the previous device fabrication procedures.

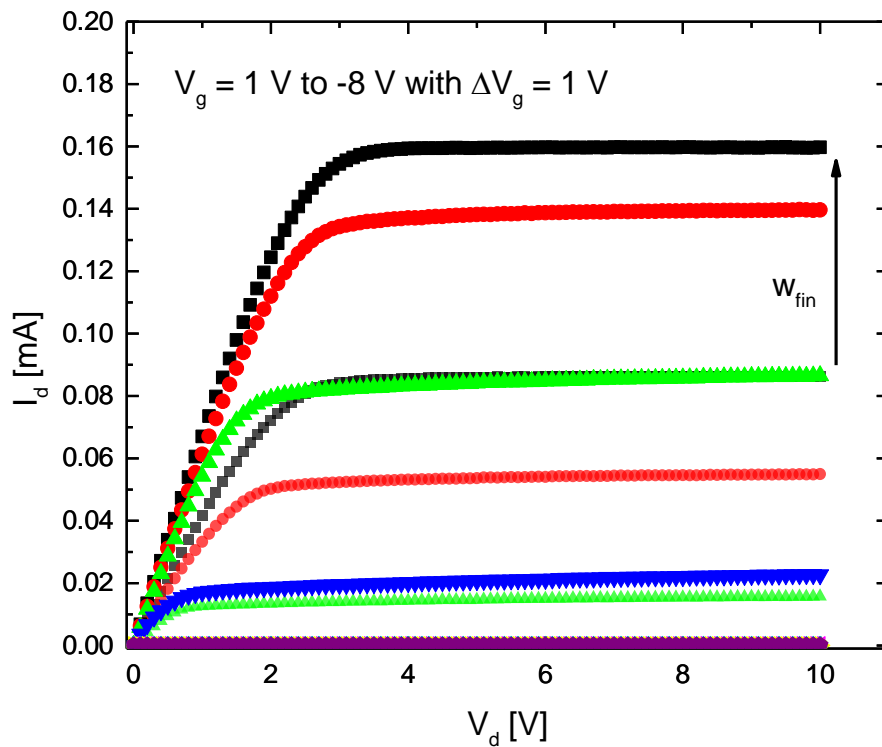
The overall device scheme is illustrated in Figure 65. The fabrication is started with surface cleaning/preparation, fin formation using RIE (5 minutes) and EBL systems, ohmic contact formation (Ta / Al / Ta) using e-beam evaporator, gate dielectric deposition using ALD (200 cycles HfO<sub>2</sub>), gate metal (Ni) deposition using the evaporator. This reduces via integration to the device, which can reduce additional deposition, EBL patterning, etching, chemical treatment, final device fabrication cost and time.



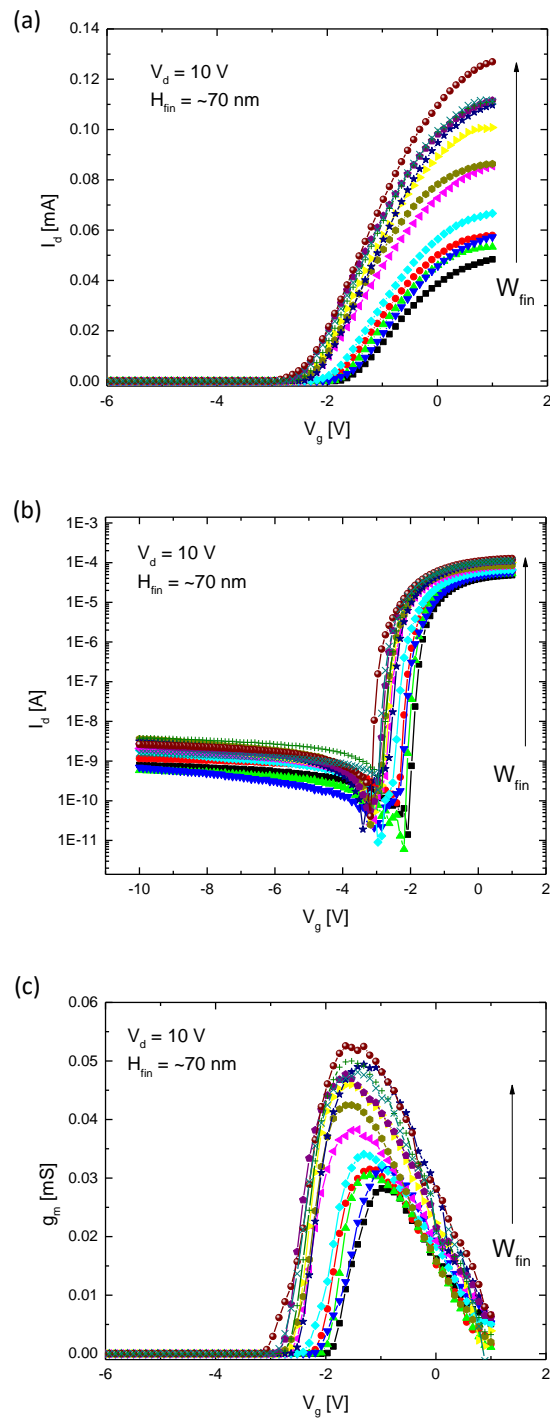


**Figure 65.** AlGaIn/GaN FinFET device scheme is illustrated. It reduces additional steps in fabrication processes so as for device fabrication cost and time.

The fabricated AlGaN/GaN FinFET device with the introduced process method has fin widths from 50 nm to 170 nm as defined in mask pattern dimension in EBL system. Figure 66 shows the output characteristic of  $I_d - V_d$  versus  $V_g$  of the FinFET device. The solid line shows the characteristic of the widest fin width AlGaN/GaN FinFET and the faded line shows the characteristic of the narrowest fin width fabricated in this fabrication process. A significant output current increases as the fin width gets wider as shown in the previous sections.

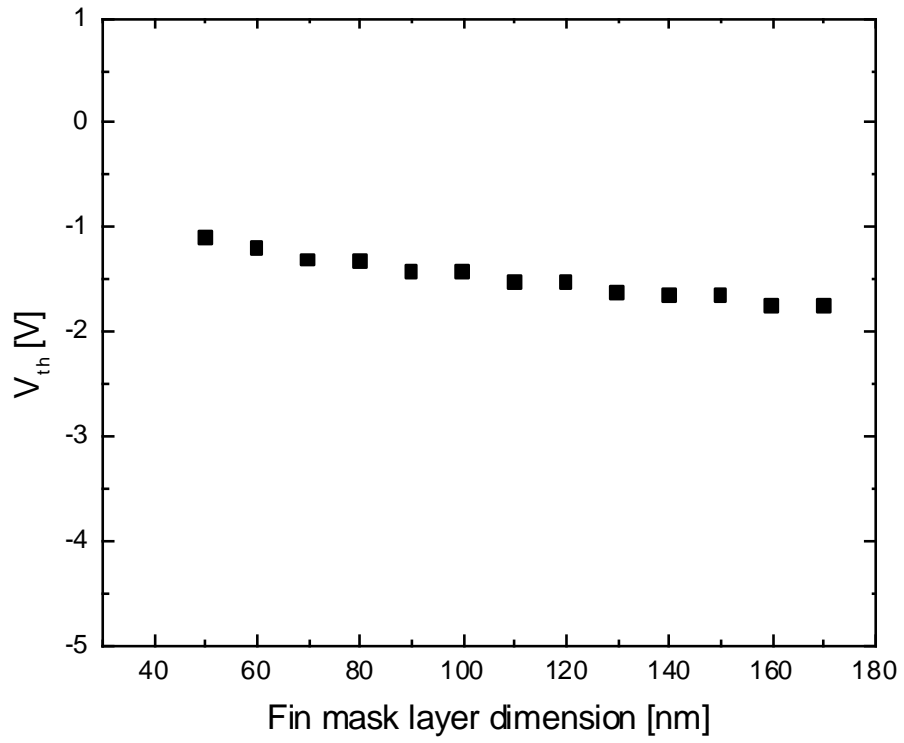


**Figure 66.** Output characteristic of  $I_d - V_d$  versus  $V_g$  of AlGaN/GaN FinFET using reduced fabrication process. As  $W_{fin}$  increases  $I_d$  increases.



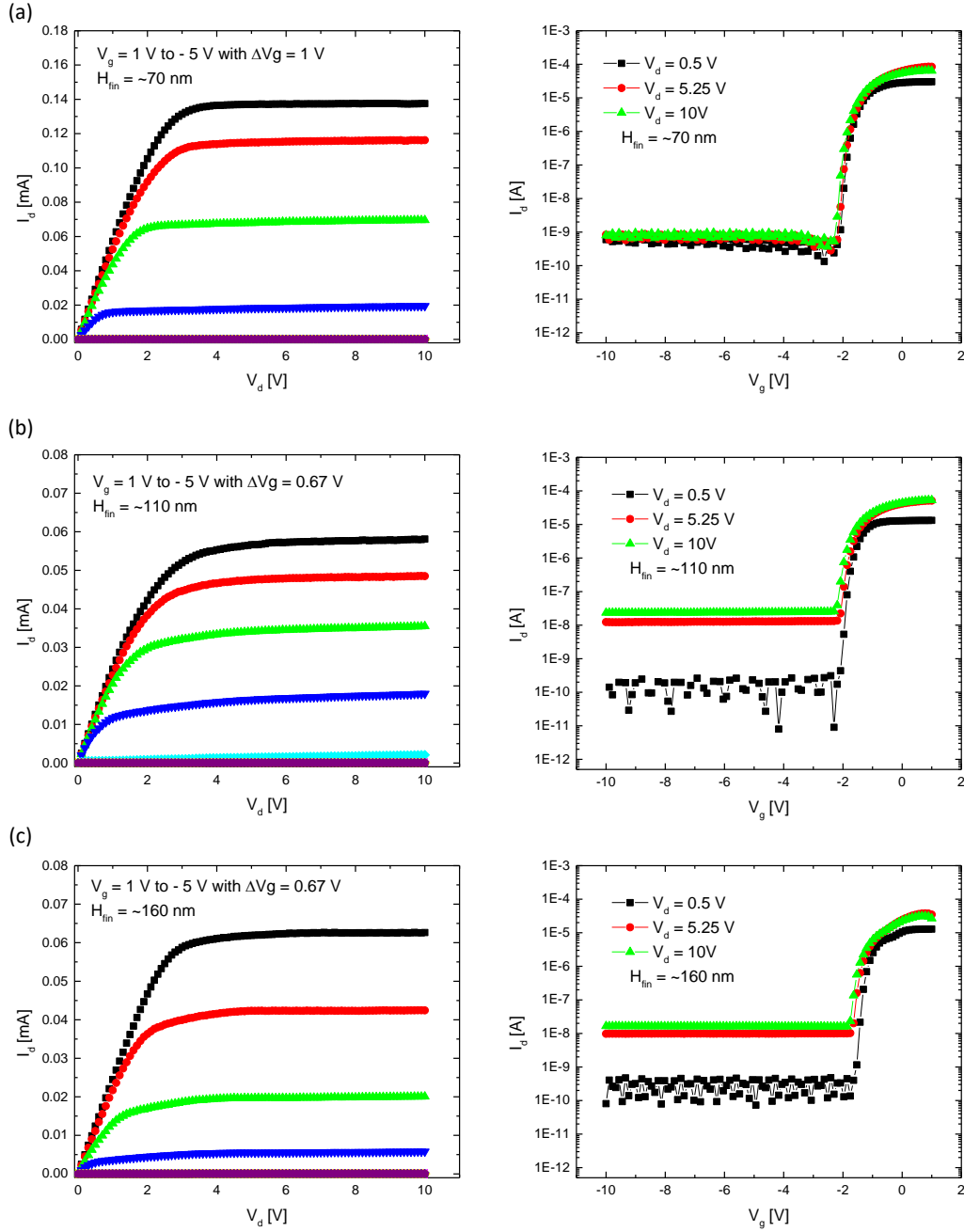
**Figure 67.** Transfer characteristics of  $I_d - V_g$  in linear and logarithm scale and  $g_m - V_g$  at  $V_d = 10$  V of AlGaIn/GaN FinFET using reduced fabrication process.

Figure 67 shows the device transfer characteristics of  $I_d - V_g$  in linear and logarithm scale and  $g_m - V_g$  at  $V_d = 10$  V of AlGaIn/GaN FinFET using the proposed fabrication process in this section. It shows  $I_{on} / I_{off}$  ratio of more than  $10^5$  which proves the recess etched GaN effects little on the leakage path. To avoid fabrication complexity using the via-integration, it could be omitted from the process flow, however if the device is integrated in large scale, then the effect should not be ignored. From Figure 67, the extracted threshold voltages and subthreshold swing values are from -1.1 V to -1.75 V and 38 mV/dec to 71 mV/dec at  $V_d = 10$  V, respectively, from the narrow to wide fin. Extremely good SS value obtained as the fin width gets narrower using the briefly modified process is observed. The threshold variation on fin width dependency is shown in Figure 68. It shows the threshold voltage is increasing as the fin width gets narrower.

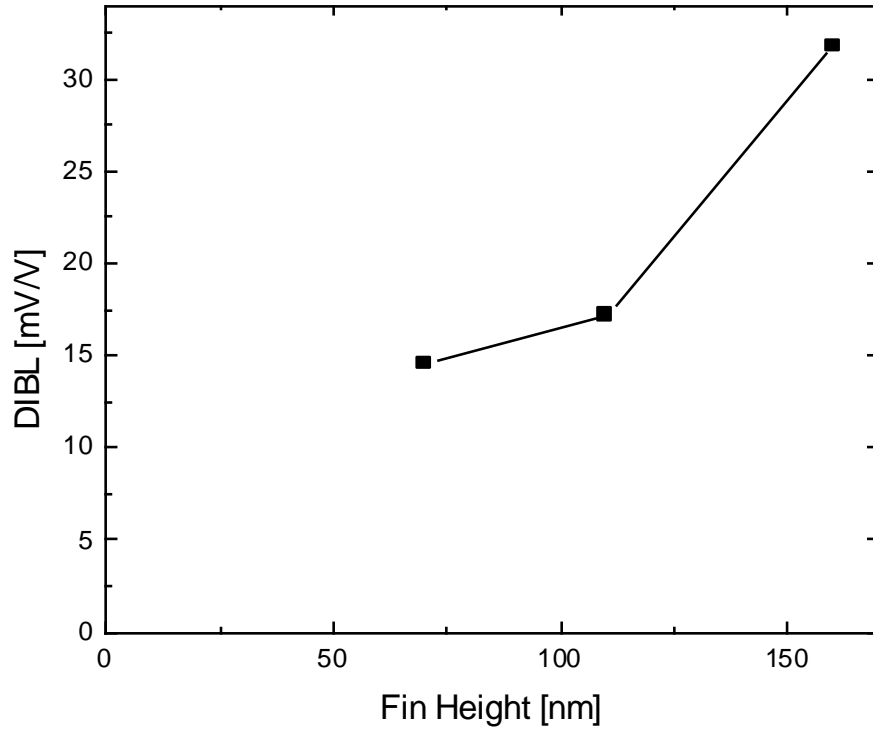


**Figure 68.** Threshold voltage versus fin width (EBL mask file layer dimension)

As one of the device design parameters to consider, a fin height effect on the device performance is investigated. Three different device fin height of 70 nm, 110 nm, and 160 nm are achieved during the device fabrication. The device electrical characterization is shown for each device in Figure 69. The output current of taller devices ( $H_{\text{fin}} = 110$  and 160 nm) is half of the output current of the 70 nm fin height device. This can be attributed to a physical fin dimension loss during the long etching time to the current loss. Physical fin width dimension is not the same for all fin heights. As the fin height increases the off-current at high  $V_d$  is increased. The  $I_{\text{on}} / I_{\text{off}}$  ratio is reduced by the magnitude of  $\sim 10^2$  while the ratio is kept well in the linear region of the device. With the taller devices, it enhances the ratio even better in comparison to the 70 nm tall device. It concludes that additional fin etching creates extra states more along the sidewalls while it is isolating from the gate more because it is taller, however at applied higher potential, there is more conduction path under control along the tall sidewalls and it includes more defects, damage on the sidewall surface. Also it has a trend on the DIBL measurement, as shown in Figure 70. As a fin height increase DIBL effect increases as well.



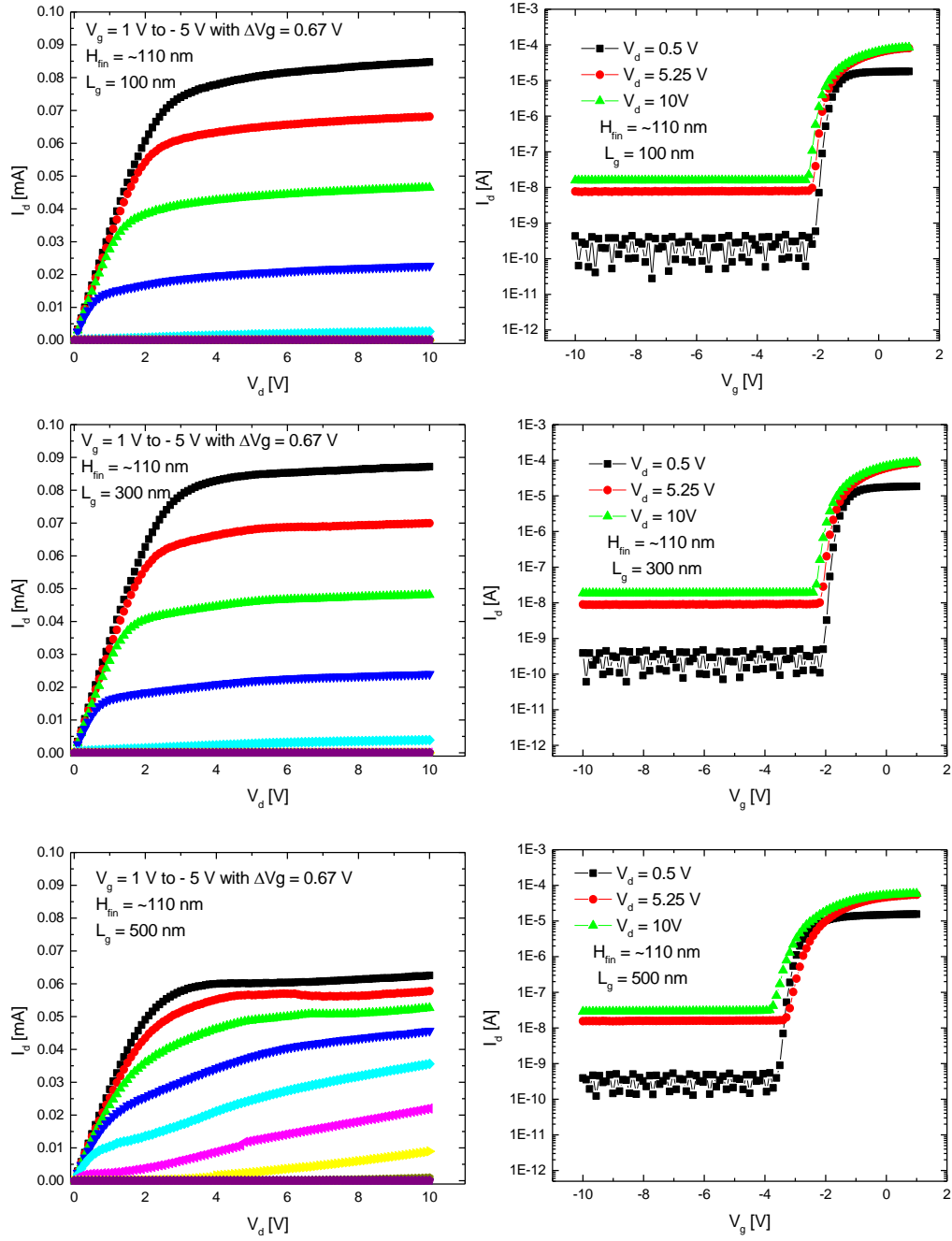
**Figure 69.** Electrical output and transfer characteristics of 3 different fin heights device ( $H_{fin} = 70, 110, \text{ and } 160 \text{ nm}$  from the top to bottom).



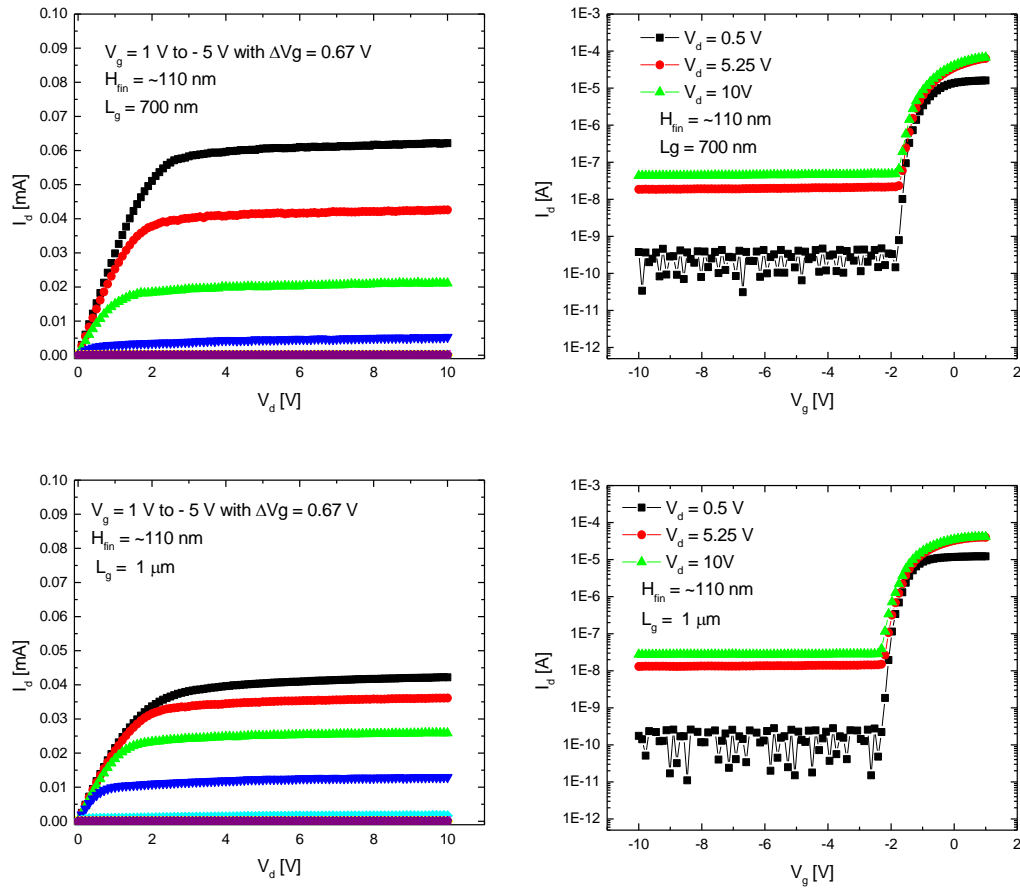
**Figure 70.** Fin height effects on DIBL.

As one of the FinFET design parameters, gate length effects by varying the length from 100 nm to 1  $\mu\text{m}$ , are investigated and the electrical output and transfer characteristic is shown in Figure 71 and Figure 72.





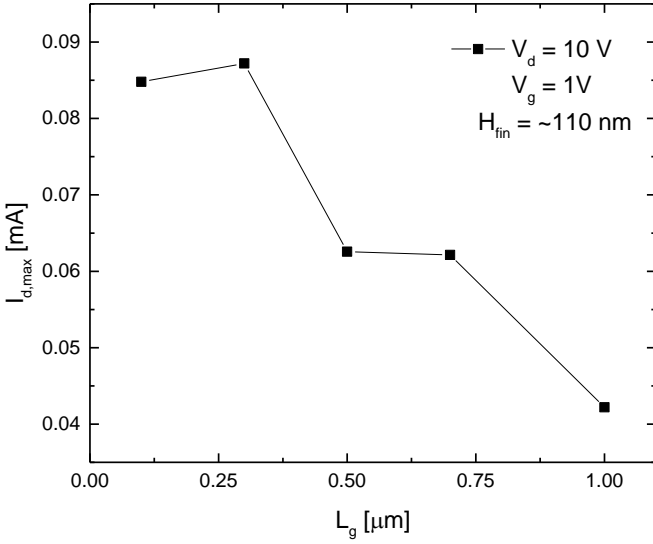
**Figure 71.** Electrical output and transfer characteristics based on gate length variation



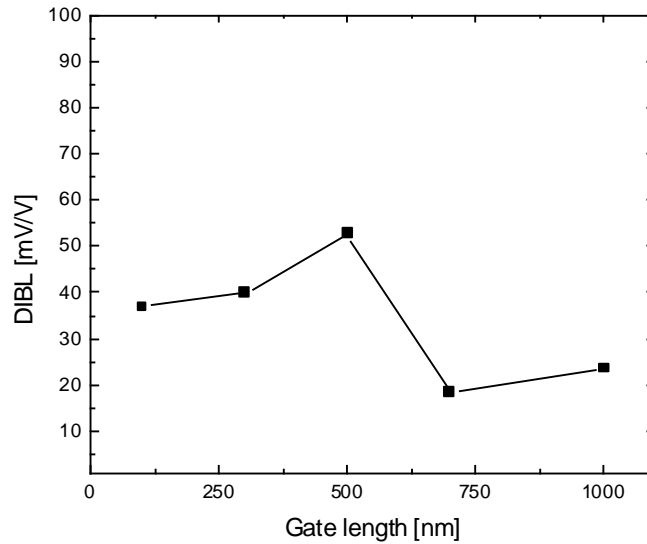
**Figure 72.** (Continued from Figure 70) Electrical output and transfer characteristics based on gate length variation

The effects are observed with 110 nm tall FinFET and it has similar effect on the transfer characteristics discussed previously. Also the output current is decreased as the gate length gets wider. The maximum output current is measured at  $V_d = 10$  V and  $V_g = 1$  V, and is

shown in Figure 73. Figure 74 shows DIBL behavior but no trend yet because it seems the gate length is still too wide to see the DIBL effect.



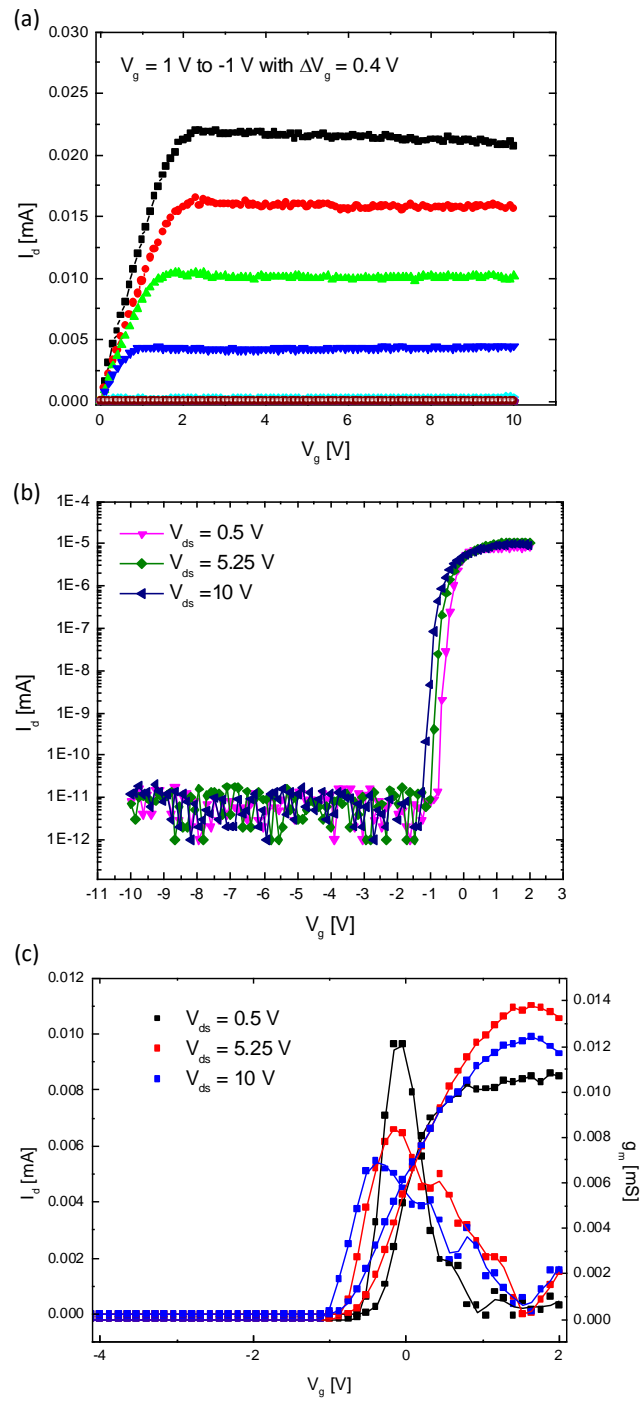
**Figure 73.** Gate length effect on the output current.



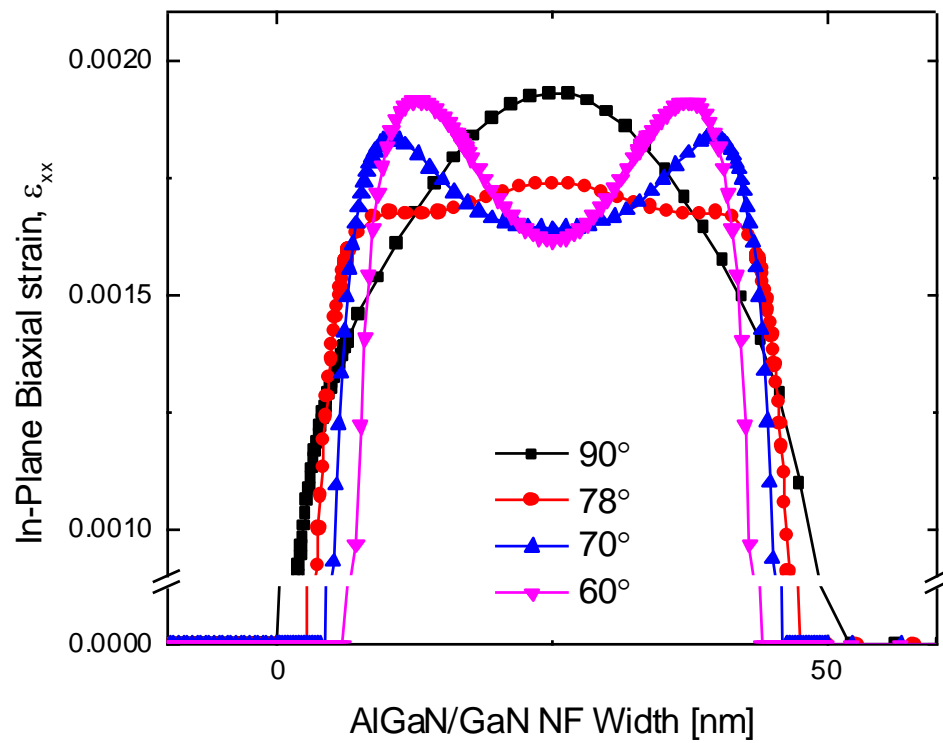
**Figure 74.** Measured DIBL effect on different gate length FinFET device.

As one of the FinFET design parameters, fin sidewall angle effect is investigated using the built and optimized etch process so far which includes additional 25 % TMAH etching process at 95 °C for 10 minutes right after ICP-RIE for 5 minutes. Having most-likely vertical sidewalls for AlGaIn/GaN FinFET device, the device characteristics are very impressive. It has larger output current than ones from other angle shapes, subthreshold swing of 52 mV / dec, and more than  $10^7$  of  $I_{on} / I_{off}$  ratio at  $V_d = 10$  V. The electrical output and transfer characteristic is shown in Figure 75. While fin sidewalls get laterally etched, defects and damages of the sidewalls also get removed and smoothed as shown in the previous figures. The electrical characteristic change is affected by the fin angle resulting from fabrication process modulation. Consequently, the total 2DEG sheet

density, from simulations, decreases by  $\sim 15\%$  as the angle between the c-plane (0001) and the growth axis of the fin sidewall decreases from  $90^\circ$  to  $60^\circ$ . There is a critical angle and dimension over which the growth axis strain dominates the in-plane strain which causes the peak tensile strain in AlGa<sub>N</sub> barrier to shift outward which is compensated with surface state charges, therefore reduced 2DEG density. With smooth and vertical sidewalls, better strain profile can be formed to support more 2DEG density as the in-plane strain profile is simulated and shown in Figure 76.



**Figure 75.** Electrical output and transfer characteristics of vertical sidewall shape AlGaIn/GaN FinFET device.



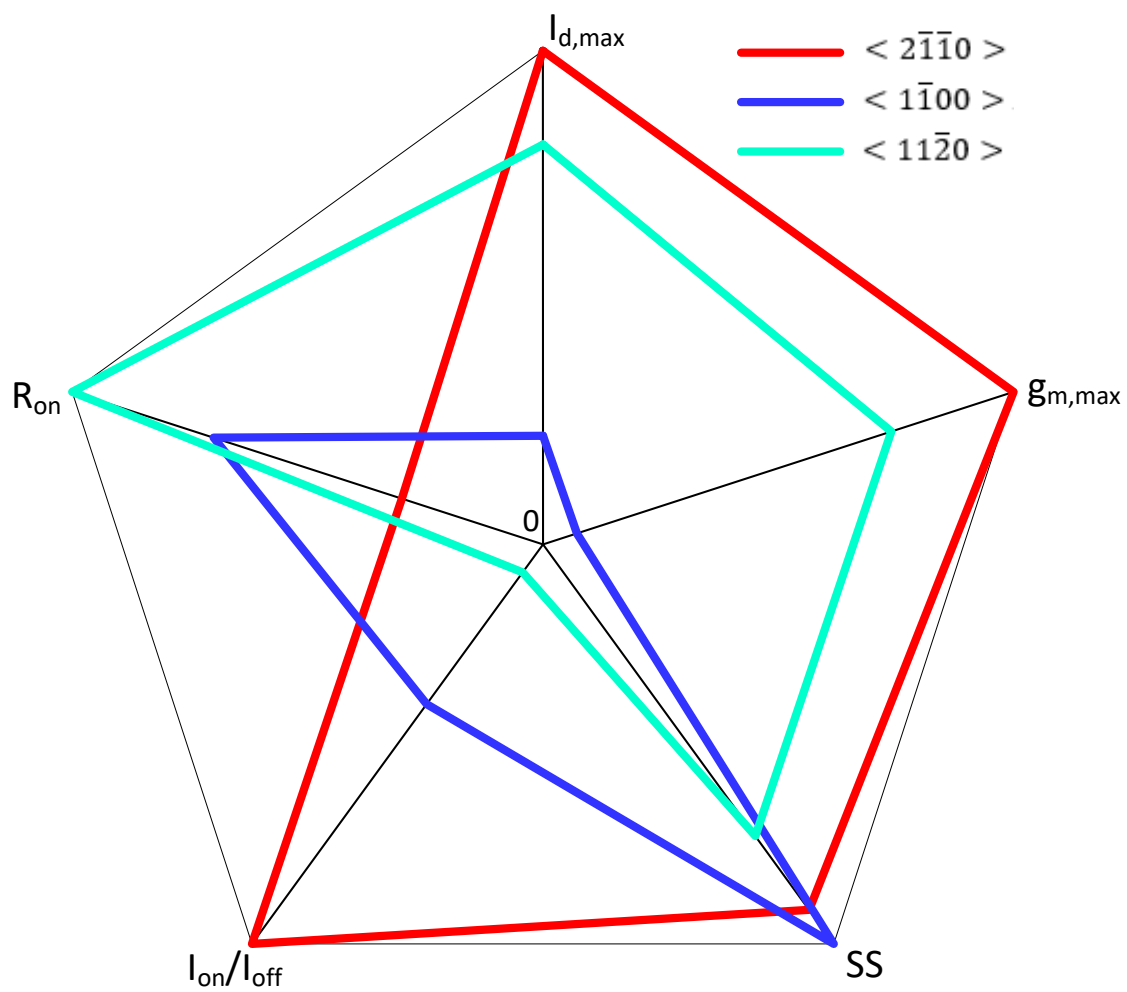
**Figure 76.** Simulated in-plane biaxial strain profile variation due to the fin sidewall angle variation within a 2DEG width of 50 nm.

## CHAPTER VII

### CONCLUSION

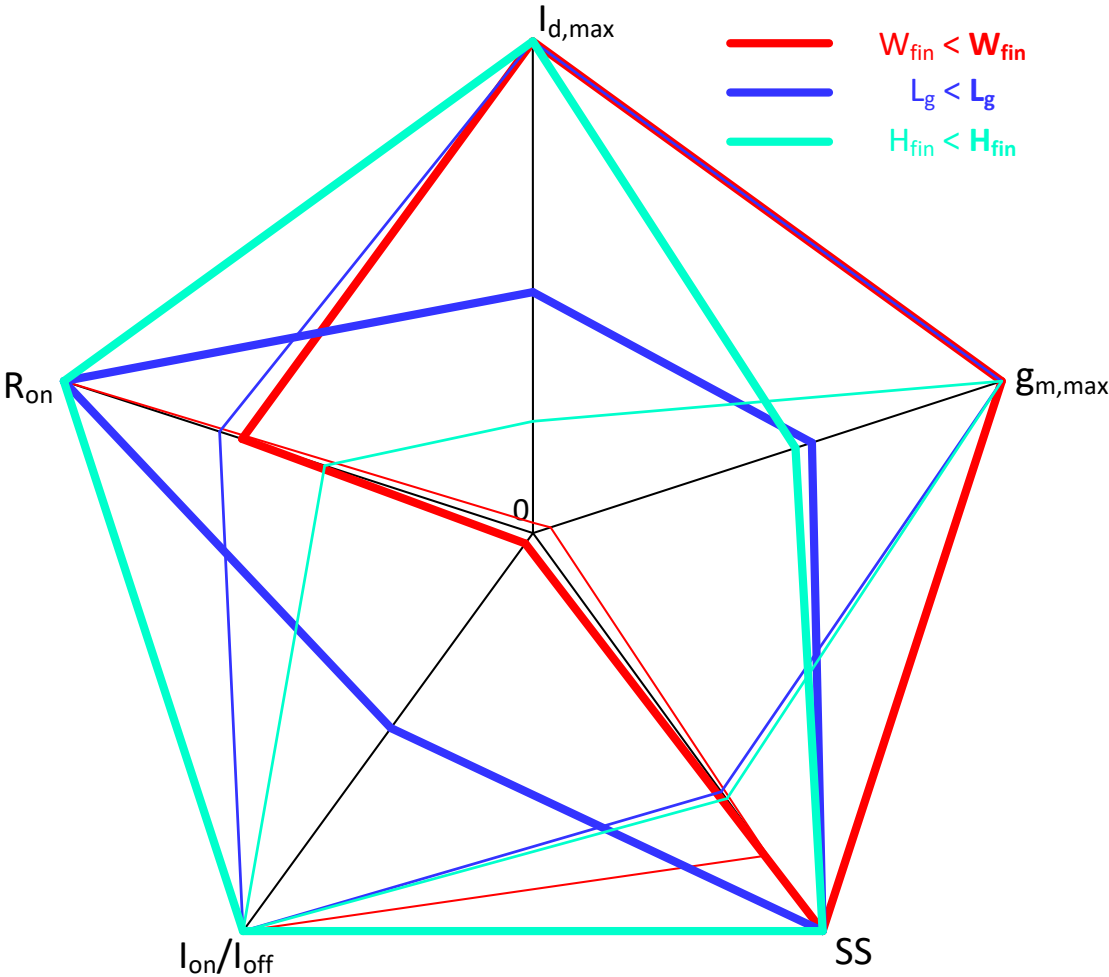
The impact of physical design parameters of AlGaN/GaN FinFET device are thoroughly demonstrated toward the realization of III-V FinFET logic applications, realizing well controlled fabrication process such as surface cleaning/preparation, S/D ohmic contact module, fin mesa isolation, and gate contact module. Figure 77 shows the normalized device characteristics of the fabricated AlGaN/GaN FinFETs after 10 minutes TMAH etch process along the crystal orientations.





**Figure 77.** Normalized device performance comparison of fabricated AlGaIn/GaN FinFETs parallel to the crystal orientation.

Figure 78 shows the comparison of the normalized device electrical characteristics based on the device design parameters of the fabricated AlGaIn/GaN FinFETs.



**Figure 78.** Normalized device performance comparison based on the device design parameters of fabricated AlGaIn/GaN FinFETs.

The benchmarks made in this dissertation is of one reference toward an AlGaN/GaN FinFET device design. With the benchmarks, future research can be performed and compared across device geometries to ensure that a proper device design is achieved.

## REFERENCES

- [1] D. Bhattacharya and N. K. Jha, "FinFETs: From Devices to Architectures," *Advances in Electronics*, vol. 2014, pp. 1-21, 2014.
- [2] N. Collaert, S. Brus, A. D. Keersgieter, A. Dixit, I. Ferain, M. Goodwin, *et al.*, "Integration Challenges for Multi-Gate Devices," *International Conference on Integrated Circuit Design and Technology (ICICDT)*, 2005, pp. 187-194.
- [3] H. S. P. Wong, "Beyond the Conventional Transistor," *IBM Journal of Research and Development*, vol. 46, pp. 133-168, 2002.
- [4] K. Shinohara, D. C. ReGaN, T. Yan, A. L. Corrion, D. F. Brown, J. C. Wong, *et al.*, "Scaling of GaN Hemts and Schottky Diodes for Submillimeter-Wave Mmic Applications," *Electron Devices, IEEE Transactions on*, vol. 60, pp. 2982-2996, 2013.
- [5] A. V. Thathachary, "Physics , Fabrication and Characterization of III-V Multi-Gate FETs for Low Power Electronics," Ph.D., Electrical Engineering, The Pennsylvania State University, State College, Pennsylvania, 2015.
- [6] J. He, Y. Tian, P. Wu, L. Liao, H. Quan, J. Kang, *et al.*, "Heterogeneous Bovine Acellular Dermal Matrix for Mucosal Repair in Reconstructive Surgery for Laryngeal and Hypopharyngeal Carcinoma," *Oncology Research Treatment*, vol. 38, pp. 282-284, 2015.
- [7] M. M. Tawseef A. Bhat, M.R. Beigh, "Study of Short Channel Effects in N-FinFET Structure for Si, GaAs, GaSb and GaN Channel Materials," *Journal of Nano- and Electronic Physics*, vol. 7, p. 5, 2015.
- [8] D.-h. Son, Y.-w. Jo, R.-h. Kim, C. Heo, J. H. Seo, J. S. Kim, *et al.*, "Fabrication of High Performance AlGaIn/GaN FinFET by Utilizing Anisotropic Wet Etching in Tmah Solution," *IEEE 2015 45th European Solid State Device Research Conference (ESSDERC)*, pp. 130-133, 2015.
- [9] K.-S. Im, R.-H. Kim, K.-W. Kim, D.-S. Kim, C. S. Lee, S. Cristoloveanu, *et al.*, "Normally Off Single-Nanoribbon Al<sub>2</sub>O<sub>3</sub>/GaN MISFET," *IEEE Electron Device Letters*, vol. 34, pp. 27-29, 2013.
- [10] M. H. Chiang, J. N. Lin, K. Kim, and C. T. Chuang, "Optimal Design of Triple-Gate Devices for High-Performance and Low-Power Applications," *IEEE Transactions on Electron Devices*, vol. 55, pp. 2423-2428, 2008.

- [11] Y. Ji-Woon and J. G. Fossum, "On the Feasibility of Nanoscale Triple-Gate CMOS Transistors," *IEEE Transactions on Electron Devices*, vol. 52, pp. 1159-1164, 2005.
- [12] W. Xiong, J. W. Park, and J. P. Colinge, "Corner Effect in Multiple-Gate SOI Mosfets," in *SOI Conference, 2003. IEEE International*, 2003, pp. 111-113.
- [13] J. G. Fossum, J. W. Yang, and V. P. Trivedi, "Suppression of Corner Effects in Triple-Gate MOSFETs," *IEEE Electron Device Letters*, vol. 24, pp. 745-747, 2003.
- [14] J. A. del Alamo, "Nanometre-Scale Electronics with III-V Compound Semiconductors," *Nature*, vol. 479, pp. 317-323, Nov 17 2011.
- [15] S. Rajan, Y. Pei, Z. Cheng, S. P. DenBaars, and U. K. Mishra, "Surface Passivation of AlGaIn/GaN HEMTs," in *Device Research Conference, 2008*, 2008, pp. 131-132.
- [16] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The Impact of Surface States on the DC and RF Characteristics of AlGaIn/GaN HFETs," *IEEE Transactions on Electron Devices*, vol. 48, pp. 560-566, 2001.
- [17] Z. X. Qin, Z. Z. Chen, Y. Z. Tong, X. M. Ding, X. D. Hu, T. J. Yu, *et al.*, "Study of Ti/Au, Ti/Al/Au, and Ti/Al/Ni/Au Ohmic Contacts to n-GaN," *Applied Physics A*, vol. 78, pp. 729-731, 2004.
- [18] N. A. Papanicolaou, M. V. Rao, J. Mittereder, and W. T. Anderson, "Reliable Ti/Al and Ti/Al/Ni/Au Ohmic Contacts to n-Type GaN Formed by Vacuum Annealing," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 19, p. 261, 2001.
- [19] B. Jacobs, M. C. J. C. M. Kramer, E. J. Geluk, and F. Karouta, "Optimisation of the Ti / Al / Ni / Au Ohmic Contact on AlGaIn GaN FET Structures," *Journal of Crystal Growth*, vol. 241, pp. 15-18, 2002.
- [20] T. Sreenidhi, K. Baskar, A. DasGupta, and N. DasGupta, "Reactive Ion Etching of GaN in SF<sub>6</sub> + Ar and SF<sub>6</sub> + N<sub>2</sub> Plasma," *Semiconductor Science and Technology*, vol. 23, pp. 125019-125019, 2008.
- [21] R. Cheung, B. Rong, E. van der Drift, and W. G. Sloof, "Etch Mechanism and Etch-Induced Effects in the Inductively Coupled Plasma Etching of GaN," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 21, p. 1268, 2003.

- [22] D. Basak, M. Verdú, M. T. Montojo, M. A. Sánchez-García, F. J. Sánchez, E. Muñoz, *et al.*, "Reactive Ion Etching of GaN Layers Using SF<sub>6</sub>," *Semiconductor Science and Technology*, vol. 12, pp. 1654-1654, 1997.
- [23] J. W. Johnson, J. Gao, K. Lucht, J. Williamson, C. Strautin, J. Riddle, *et al.*, "Material, Process, and Device Development of GaN-Based HFETs on Silicon Substrates," *Electrochemical Society Proceedings*, 2004.
- [24] B. Rong, R. J. Reeves, S. A. Brown, M. M. Alkaisi, E. van der Drift, R. Cheung, *et al.*, "A Study of Reactive Ion Etching Damage Effects in GaN," *Microelectronic Engineering*, vol. 57–58, pp. 585-591, 2001.
- [25] C. Li, X. Bao, J. Xu, Y. Zhang, and X. Li, "Optical Characterization of GaN/AlGa<sub>N</sub> Bilayer by Transmission and Reflection Spectra," *Journal of Applied Physics*, vol. 108, p. 063104, 2010.
- [26] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, *et al.*, "Two Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization in Undoped and Doped AlGa<sub>N</sub>/Ga<sub>N</sub> Heterostructures," *Journal of Applied Physics*, vol. 87, p. 334, 2000.
- [27] A. Malmros, H. Blanck, and N. Rorsman, "Electrical Properties, Microstructure, and Thermal Stability of Ta-Based Ohmic Contacts Annealed at Low Temperature for GaN HEMTs," *Semiconductor Science and Technology*, vol. 26, p. 075006, 2011.
- [28] Y. Li, G. I. Ng, S. Arulkumaran, C. M. M. Kumar, K. S. Ang, M. J. Anand, *et al.*, "Low-Contact-Resistance Non-Gold Ta/Si/Ti/Al/Ni/Ta Ohmic Contacts on Undoped AlGa<sub>N</sub>/Ga<sub>N</sub> High-Electron-Mobility Transistors Grown on Silicon," *Applied Physics Express*, vol. 6, p. 116501, 2013.
- [29] N. Nepal, N. Y. Garces, D. J. Meyer, J. K. Hite, M. A. Mastro, and J. Charles R. Eddy, "Assessment of GaN Surface Pretreatment for Atomic Layer Deposited High- K Dielectrics," *Applied Physics Express*, vol. 4, p. 055802, 2011.
- [30] S. W. King, J. P. Barnak, M. D. Bremser, K. M. Tracy, C. Ronning, R. F. Davis, *et al.*, "Cleaning of AlN and GaN Surfaces," *Journal of Applied Physics*, vol. 84, pp. 5248-5260, 1998.
- [31] F. Gonzalez-Posada, J. A. Bardwell, S. Moisa, S. Haffouz, H. P. Tang, A. F. Brana, *et al.*, "Surface Cleaning and Preparation in AlGa<sub>N</sub>/Ga<sub>N</sub>-Based HEMT Processing as Assessed by X-Ray Photoelectron Spectroscopy," *Applied Surface Science*, vol. 253, pp. 6185-6190, 2007.

- [32] S. C. Jain, M. Willander, and H. Maes, "Stresses and Strains in Epilayers, Stripes and Quantum Structures of III-V Compound Semiconductors," *Semiconductor Science and Technology*, vol. 11, pp. 641-641, 1996.
- [33] A. Soltani, A. BenMoussa, S. Touati, V. Hoel, J. C. De Jaeger, J. Laureyns, *et al.*, "Development and Analysis of Low Resistance Ohmic Contact to n-AlGaIn/GaN Hemt," *Diamond and Related Materials*, vol. 16, pp. 262-266, 2007.
- [34] M. Azize and T. Palacios, "Top-Down Fabrication of AlGaIn/GaN Nanoribbons," *Applied Physics Letters*, vol. 98, p. 042103, 2011.
- [35] K. S. Boutros, S. Burnham, D. Wong, K. Shinohara, B. Hughes, D. Zehnder, *et al.*, "Normally-Off 5a/1100v GaN-on-Silicon Device for High Voltage Applications," in *2009 IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 1-3.
- [36] H. S. Lee, D. S. Lee, and T. Palacios, "AlGaIn/GaN High-Electron-Mobility Transistors Fabricated through a Au-Free Technology," *IEEE Electron Device Letters*, vol. 32, pp. 623-625, 2011.
- [37] A. Fontseré, A. Pérez-Tomás, M. Placidi, J. Llobet, N. Baron, S. Chenot, *et al.*, "Nanoscale Investigation of AlGaIn/GaN-on-Si High Electron Mobility Transistors," *Nanotechnology*, vol. 23, p. 395204, Oct 5 2012.
- [38] S. Lenci, B. D. Jaeger, L. Carbonell, J. Hu, G. Mannaert, D. Wellekens, *et al.*, "Au-Free AlGaIn/GaN Power Diode on 8-in Si Substrate with Gated Edge Termination," *IEEE Electron Device Letters*, vol. 34, pp. 1035-1037, 2013.
- [39] D. Marcon, B. D. Jaeger, S. Halder, N. Vranckx, G. Mannaert, M. V. Hove, *et al.*, "Manufacturing Challenges of GaN-on-Si HEMTs in a 200 mm CMOS Fab," *IEEE Transactions on Semiconductor Manufacturing*, vol. 26, pp. 361-367, 2013.
- [40] S. E. Steen, S. J. McNab, L. Sekaric, I. Babich, J. Patel, J. Bucchignano, *et al.*, "Looking into the Crystal Ball: Future Device Learning Using Hybrid E-Beam and Optical Lithography (Keynote Paper)," *SPIE Proceedings*, vol. 5751, pp. 26-34, 2005.
- [41] S. Pauliac-Vaujour, P. Brianceau, S. Landis, J. Chiaroni, and O. Faynot, "Sub-30-nm Hybrid Lithography (Electron Beam/Deep Ultraviolet) and Etch Process for Fully Depleted Metal Oxide Semiconductor Transistors," *Journal of Vacuum Science & Technology B*, vol. 25, pp. 2030-2033, 2007.
- [42] S. Pauliac-Vaujour, C. Comboroure, C. Vizioz, S. Barnola, P. Brianceau, V. M. Alvaro, *et al.*, "Hybrid High Resolution Lithography (E-Beam/Deep Ultraviolet) and Etch Process for the Fabrication of Stacked Nanowire Metal Oxide

- Semiconductor Field Effect Transistors," *Journal of Vacuum Science & Technology B*, vol. 26, pp. 2583-2586, 2008.
- [43] D. W. Johnson, P. Ravikirthi, J. Woo Suh, R. T. P. Lee, R. J. W. Hill, M. Hoi Wong, *et al.*, "Challenges of Contact Module Integration for GaN-Based Devices in a Si-CMOS Environment," *Journal of Vacuum Science & Technology B*, vol. 32, p. 030606, 2014.
- [44] D. Selvanathan, F. M. Mohammed, J.-O. Bae, I. Adesida, and K. H. A. Bogart, "Investigation of Surface Treatment Schemes on n-Type GaN and Al<sub>0.20</sub>Ga<sub>0.80</sub>N," *Journal of Vacuum Science & Technology B*, vol. 23, pp. 2538-2544, 2005.
- [45] Y. Ohmaki, M. Tanimoto, S. Akamatsu, and T. Mukai, "Enhancement-Mode AlGaN/AlN/GaN High Electron Mobility Transistor with Low on-State Resistance and High Breakdown Voltage," *Japanese Journal of Applied Physics*, vol. 45, pp. L1168-L1170, 2006.
- [46] S. M. Dinara, S. K. Jana, S. Ghosh, P. Mukhopadhyay, R. Kumar, A. Chakraborty, *et al.*, "Enhancement of Two Dimensional Electron Gas Concentrations Due to Si<sub>3</sub>N<sub>4</sub> Passivation on Al<sub>0.3</sub>Ga<sub>0.7</sub>N/GaN Heterostructure: Strain and Interface Capacitance Analysis," *AIP Advances*, vol. 5, p. 047136, 2015.
- [47] H. Kim, M. R. Thompson, V. Tilak, T. R. Prunty, J. R. Shealy, and L. F. Eastman, "Effects of SiN Passivation and High-Electric Field on AlGaIn-GaN HFET Degradation," *IEEE Electron Device Letters*, vol. 24, 2003.
- [48] I. R. Gatabi, D. W. Johnson, J. H. Woo, J. W. Anderson, M. R. Coan, E. L. Piner, *et al.*, "PECVD Silicon Nitride Passivation of AlGaIn/GaN Heterostructures," *IEEE Transactions on Electron Devices*, vol. 60, pp. 1082-1087, 2013.
- [49] Z. H. Liu, G. I. Ng, H. Zhou, S. Arulkumaran, and Y. K. T. Maung, "Reduced Surface Leakage Current and Trapping Effects in AlGaIn/GaN High Electron Mobility Transistors on Silicon with SiN/Al<sub>2</sub>O<sub>3</sub> Passivation," *Applied Physics Letters*, vol. 98, p. 113506, 2011.
- [50] T. R. Prunty, J. A. Smart, E. M. Chumbes, B. K. Ridley, L. F. Eastman, and J. R. Shealy, "Passivation of AlGaIn/GaN Heterostructures with Silicon Nitride for Insulated Gate Transistors," *2000 IEEE/Cornell Conference on High Performance Devices, Proceedings*, pp. 208-214, 2000.
- [51] A. Vardi, W. Lu, X. Zhao, and J. A. del Alamo, "Nanoscale Mo Ohmic Contacts to III-V Fins," *IEEE Electron Device Letters*, vol. 36, pp. 126-128, 2015.



- [52] T. Sreenidhi, K. Baskar, A. DasGupta, and N. DasGupta, "Reactive Ion Etching of GaN in SF<sub>6</sub> + Ar and SF<sub>6</sub> + N<sub>2</sub> Plasma," *Semiconductor Science and Technology*, vol. 23, p. 125019, 2008.
- [53] G. Vanko, T. Lalinský, Š. Haščík, I. Rýger, Ž. Mozolová, J. Škriniarová, *et al.*, "Impact of SF<sub>6</sub> Plasma Treatment on Performance of AlGaN/GaN HEMT," *Vacuum*, vol. 84, pp. 235-237, 2009.
- [54] K. S. Im, V. Sindhuri, Y. W. Jo, D. H. Son, J. H. Lee, S. Cristoloveanu, *et al.*, "Fabrication of AlGaN/GaN Omega-Shaped Nanowire Fin-Shaped FETs by a Top-Down Approach," *Applied Physics Express*, vol. 8, p. 066501, 2015.
- [55] S. P. R. M, H. Park, S.-M. Kim, S.-H. Jang, and J.-S. Jang, "High-Performance Light-Emitting Diodes Using Hierarchical m-Plane GaN Nano-Prism Light Extractors," *Journal of Materials Chemistry C*, vol. 3, pp. 8873-8880, 2015.
- [56] K. W. Kim, S. D. Jung, D. S. Kim, H. S. Kang, K. S. Im, J. J. Oh, *et al.*, "Effects of TMAH Treatment on Device Performance of Normally Off Al<sub>2</sub>O<sub>3</sub>/GaN MOSFET," *IEEE Electron Device Letters*, vol. 32, pp. 1376-1378, Oct 2011.
- [57] M. H. Wong, F. Wu, J. S. Speck, and U. K. Mishra, "Polarity Inversion of N-Face GaN Using an Aluminum Oxide Interlayer," *Journal of Applied Physics*, vol. 108, p. 123710, Dec 15 2010.
- [58] A. R. Clawson, "Guide to References on III-V Semiconductor Chemical Etching," *Materials Science & Engineering R-Reports*, vol. 31, pp. 1-438, 2001.
- [59] A. Wierzbicka, J. Domagala, M. Sarzynski, D. Luebbert, and Z. R. Zytkeiwicz, "Investigation of Strain and Lattice Parameters Distribution in Epitaxial Laterally Overgrown InGaN/GaN Structures," *IX Krajowe Sympozjum Użytkowników Promieniowania Synchrotronowego*, 2011.
- [60] S. Y. Bae, D. J. Kong, J. Y. Lee, D. J. Seo, and D. S. Lee, "Size-Controlled InGaN/GaN Nanorod Array Fabrication and Optical Characterization," *Optical Express*, vol. 21, pp. 16854-16862, 2013.
- [61] D. Li, M. Sumiya, S. Fuke, D. Yang, D. Que, Y. Suzuki, *et al.*, "Selective Etching of GaN Polar Surface in Potassium Hydroxide Solution Studied by X-Ray Photoelectron Spectroscopy," *Journal of Applied Physics*, vol. 90, p. 4219, 2001.
- [62] D. W. Johnson, "Si-CMOS-Like Integration of AlGaN/GaN Dielectric-Gated HEMT," Ph. D., Electrical Engineering, Texas A&M University, College Station, Texas, 2014.

- [63] T. Lalinský, G. Vanko, M. Vallo, E. Dobročka, I. Rýger, and A. Vincze, "AlGaN/GaN High Electron Mobility Transistors with Nickel Oxide Based Gates Formed by High Temperature Oxidation," *Applied Physics Letters*, vol. 100, p. 092105, 2012.

## APPENDIX A

Following sample code is used for strain profile simulation using nextnano.

```
%DebugLevel = 0 !

!-----!
$numeric-control
simulation-dimension = 2

zero-potential = yes
newton-method = Newton-2
nonlinear-poisson-iterations = 150

piezo-charge-at-boundaries = no
pyro-charge-at-boundaries = no
piezo-constants-zero = no
pyro-constants-zero = no

lattice-constants-temp-coeff-on = no
varshni-parameters-on = no
strain-iterations = 4000
strain-residual = 1d-15
strain-lin-eq-solv = BiCGSTAB ! (default)

new-strain-routine = yes
strain-volume-correction-residual = 1d-10
strain-volume-correction-iterations = 20
discretize-only-once = yes

$end_numeric-control
!-----!

!-----!
$warnings
warnings = .TRUE.
$end_warnings
!-----!
```

!\*\*\*\*\* OVERALL SIMULATION PARAMETERS

\*\*\*\*\*!

!-----!

\$simulation-dimension

dimension = 2

orientation = 0 1 1

\$end\_simulation-dimension

!-----!

!-----!

\$global-parameters

lattice-temperature = 300.0d0 ! Kelvin

\$end\_global-parameters

!-----!

!-----!

\$simulation-flow-control

flow-scheme = 0 ! 0 = calculate strain only

raw-directory-in = raw\_data/

raw-potential-in = no

strain-calculation = strain-minimization

\$end\_simulation-flow-control

!-----!

!-----!

\$strain-minimization-model ! for "strain-calculation = strain-minimization"

substrate-cluster-number = 1 2

!boundary-condition-x = Neumann

boundary-condition-y = Neumann

boundary-condition-z = Neumann

grown-on-substrate = no ! freestanding

!grown-on-substrate = yes ! thick substrate

deformed-volume-correction = no

\$end\_strain-minimization-model

!-----!

!-----!

\$domain-coordinates

domain-type = 0 1 1

y-coordinates = -30.0d0 80d0

z-coordinates = -30d0 60d0

hkil-y-direction = -1 2 -1 0

hkil-z-direction = 0 0 0 1

pseudomorphic-on = GaN  
growth-coordinate-axis = 0 0 1  
\$end\_domain-coordinates

!-----!

!\*\*\*\*\* END OVERALL SIMULATION PARAMETERS  
\*\*\*\*\*!

!\*\*\*\*\* REGIONS AND CLUSTERS  
\*\*\*\*\*!

!-----!

\$regions

region-number = 1 base-geometry = trapezoid region-priority = 1 ! GaN  
top-coordinates = 10d0 40d0 50d0 50d0  
base-coordinates = 0d0 50d0 0d0 0d0

region-number = 2 base-geometry = trapezoid region-priority = 2 ! AlGaIn  
top-coordinates = 9.6d0 40.4d0 48d0 48d0  
base-coordinates = 6.1d0 43.9d0 30.5d0 30.5d0

region-number = 3 base-geometry = rectangle region-priority = 1  
y-coordinates = -30d0 80d0  
z-coordinates = -30d0 0d0

\$end\_regions

!-----!

!-----!

\$grid-specification

grid-type = 1 1 1

x-grid-lines = -10d0 0d0 50d0 60d0  
x-nodes = 3 25 3  
x-grid-factors = 1d0 1d0 1d0

y-grid-lines = -30d0 -10d0 0d0 2d0 6.1d0 9.6d0 10d0 40d0 40.4d0 43.9d0 48d0 50d0  
80d0  
y-nodes = 24 24 24 24 24 24 24 2 24 24 24 24  
y-grid-factors = 1d0 1d0 1d0 1d0 1d0 1d0 1d0 1d0 1d0 1d0 1d0 1d0

```
z-grid-lines = -30d0 -10d0 0d0 10d0 25d0 30.5d0 48d0 50d0 60d0
z-nodes = 10 10 10 15 19 40 10 10
z-grid-factors = 1d0 1d0 1d0 1d0 1d0 1d0 1d0 1d0
```

```
$end_grid-specification
```

```
!-----!
```

```
!-----!
```

```
$region-cluster
```

```
cluster-number = 1 region-numbers = 1 3
```

```
cluster-number = 2 region-numbers = 2
```

```
cluster-number = 3 region-numbers = 4
```

```
$end_region-cluster
```

```
!-----!
```

```
!***** END REGIONS AND CLUSTER
```

```
*****!
```

```
!***** MATERIALS AND ALLOY PROFILES
```

```
*****
```

```
!-----!
```

```
$material
```

```
material-number = 2
```

```
material-name = Al(x)Ga(1-x)N
```

```
alloy-function = constant
```

```
cluster-numbers = 2
```

```
material-number = 1
```

```
material-name = GaN
```

```
cluster-numbers = 1
```

```
material-number = 3
```

```
material-name = Air-wz
```

```
cluster-numbers = 3
```

```
$end_material
```

```
!-----!
```

```

!-----!
$binary-wz-default
binary-type = GaN-wz-default
apply-to-material-numbers = 1 2
lattice-constants = 0.3189d0 0.3189d0 0.5185d0          ! [nm] a,a,c 300 K
elastic-constants = 390d0 145d0 106d0                  !
                    398d0 105d0                        ! C11,C12,C13,C33,C44 [GPa]
$end_binary-wz-default
!-----!

```

```

!-----!
$binary-wz-default
binary-type = AlN-wz-default
apply-to-material-numbers = 2
lattice-constants = 0.3112d0 0.3112d0 0.4982d0        ! [nm] a,a,c 300 K
elastic-constants = 396.0d0 137.0d0 108.0d0            !
                    373.0d0 116.0d0                    ! C11,C12,C13,C33,C44 [GPa]
$end_binary-wz-default
!-----!

```

```

!-----!
$binary-wz-default
binary-type = Air-wz-default
apply-to-material-numbers = 3
lattice-constants = 0.3189d0 0.3189d0 0.5185d0        ! [nm] a,a,c
elastic-constants = 0d0 0d0 0d0                        !
                    0d0 0d0                            ! C11,C12,C13,C33,C44 [GPa]
$end_binary-wz-default
!-----!

```

```

!-----!
$alloy-function
material-number = 2
function-name = constant
xalloy = 0.26d0
$end_alloy-function
!-----!

```

```

!***** OUTPUT
*****!

```

```

!-----!
$global-settings
output-directory = output/
debug-level = %DebugLevel
$end_global-settings
!-----!

!-----!
$output-raw-data
destination-directory = raw_data/
strain = yes
potential = yes
$end_output-raw-data
!-----!

!-----!
$output-strain
destination-directory = strain/
strain = yes
hydrostatic-strain = yes
strain-crystal-system = no
strain-simulation-system = yes
elastic-energy-density = yes           ! in units of [eV/nm^3]
$end_output-strain
!-----!

!-----!
$output-bandstructure
destination-directory = band_structure/
conduction-band-numbers = 1 ! 2 3     ! only Gamma band
valence-band-numbers = 1 2 3
!potential = yes
potential = no
electric-field = no
$end_output-bandstructure
!-----!

!-----!
$output-densities
destination-directory = densities/
electrons = yes
holes = yes
charge-density = yes
piezo-electricity = yes

```



```
pyro-electricity = yes
interface-density = yes
integrated-density = yes
$end_output-densities
!-----!

!-----!
$output-file-format
simulation-dimension = 2
file-format = AVS
VTK-XML = no
$end_output-file-format
!-----!
!***** END OUTPUT
*****!
```