A FOUR-STAGE POWER AND AREA EFFICIENT OTA WITH 30× (400pF – 12nF) CAPACITIVE LOAD DRIVE RANGE

A Thesis

by

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ABSTRACT

Multistage operational transconductance amplifier (OTA) has been a major research focus as a solution to high DC Gain high Gain Bandwidth and wide voltage swing requirement on sub-micron devices. These system requirements, in addition to ultra-large capacitive load drivability (nF-range load capacitor), are useful in applications including LCD drivers, low dropout (LDO) linear regulators, headphone drivers, etc. The major drawback of multistage OTAs is the stability concerns since each added stage introduces low frequency poles. Numerous compensation schemes for three stage OTAs have been proposed in the past decade with only a few four stage OTA in literature.

The proposed design is a four stage OTA which uses an active zero block (AZB) to provide left half plane (LHP) zero to help with phase degradation. AZB is embedded in the second stage ensuring reuse of existing block hence providing area and power savings. This design also uses single miller capacitor in the outer loop which ensures improved speed performance with minimal area overhead. A very reliable slew helper is implemented in this design to help with the large signal performance. The slew helper is only operational in the events slewing and does not affect the small signal performance.

The proposed design achieves a DC gain of 114 dB, GBW $> 1.77MHz$ and PM $> 46.9^{\circ}$ for capacitive load ranging from 400pF–12nF ($30\times$) which is the highest recorded range in literature for these type of compensation. It does this by consuming a total power of $143.5\mu W$ and an area of $0.007mm^2$

DEDICATION

To my family.

ACKNOWLEDGMENTS

Firstly, I would like to thank my advisor, Dr. Edgar Sánchez-Sinencio, for his guidance and supervision through out my master's program in Texas A&M University. I also want to thank my thesis committee members, Dr. Samuel Palermo, Dr. Bryan Rasmussen and Dr. Garng M. Huang, for their time and support.

I would also want to thank my colleagues especially Joseph Samy Riad, who helped me immensely in my research, providing comments and answers when needed. I also want to extend my gratitude to the department faculty and staff for making my time at Texas A&M University a wonderful experience. I am very grateful to Texas Instruments for supporting and financing my tuition in graduate school.

Finally, I must express my very profound gratitude to my family for providing me with unfailing support and continuous encouragement throughout my years of study and through the process of researching and writing this thesis. This accomplishment would not have been possible without them. Thank you.

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1. INTRODUCTION

1.1 Motivation

Operational Transconductance Amplifier (OTA) is an essential building block in analog circuit design. OTAs with ultra large capacitive loads find applications in LCD drivers [3], low-dropout (LDO) linear regulators [4], headphone drivers [5], sample-and-hold amplifier circuits [6], driving cables with load capacitances in the nF range [7] etc. High DC gain, wide Gain-Bandwidth (GBW) product and large output swing are defining marks of high performance OTAs. Complementary metal-oxide semiconductor (CMOS) technology nodes has seen remarkable scaling of lower feature sizes in recent years. This trend results in improvement in speed and lower power consumption for digital logic but posing a challenging design consideration for analogue design.

The expression for a short channel MOS transition frequency (f_T) and intrinsic gain ($g_m r_o$) are given in Equation 1.1 and 1.2 obtained from [8]

$$f_T \propto \frac{V_{EB}}{L} \tag{1.1}$$

$$g_m r_o \propto \frac{L}{V_{EB}} \tag{1.2}$$

where V_{EB}, L, g_m and r_o are the excess bias voltage (overdrive voltage), channel length, transconductance and output impedance respectively.

From Equ. 1.1, reduction in the feature size of the CMOS results in higher f_T and hence faster transistor, however Equ. 1.2 shows reduction in the open loop gain. To improve the reliability of sub-micron devices the V_{DD} scales with minimum feature size. However, in order to have control over the sub-threshold leakage current, threshold voltage

(V_{TH}) don't scale by the same factor [9]. All these culminates to reduced DC Gain and reduced output swing affecting the very parameters we care for in high performance OTAs.

Multistage OTA is a viable option to counteract these effects since cascoding is not possible because of reduced voltage headroom. However each added cascade stage introduces a low frequency pole, in which case a suitable compensation scheme is needed to ensure the stability of the system. Designing a compensation scheme is relatively easy for a fixed load, no matter how large. However, designing for a range of load proves to be challenging for reasons that; at low end of the load the stability is limited by the gain margin requirement whiles the phase margin place restriction the largest load that can be driven [3].

Three stage OTAs have been an active research area this past decade providing performance enhancement for large capacitive load drive.Four stage OTAs have gained research interest recently and has been shown to provide similar or even better performance as the three stage counterpart with less power consumption [10]. The additional transconductance stage relax the requirement of the various gm blocks and provide extra degree of freedom. This added benefit of the forth transconductance stage is exploited and a new topology is proposed.

1.2 Thesis Organization

The 1st chapter introduces the background.

The 2nd chapter describes the concept of frequency compensation. Existing compensation schemes for both three stages and four stages are reviewed and motivation for proposed design is derived.

The 3rd chapter details the proposed design with transfer function and design procedure. Simulation results validating the proposed design is also given

The 4th Chapter explains the various design trade off of the proposed design.

The 5th Chapter issues the discussions and gives the summary.

The Appendix contains some less-interesting but still significant details. Appendix A explains ROC and its significance, Appendix B talks about the concept of miller multiplication, Appendix C explains Local Feedback Loop analysis as a means of comparing the effectiveness of various topologies in light of load range, Appendix D shows proposed design layout and Appendix E, some results from Monte Carlo simulation of the proposed design.

2. LITERATURE REVIEW

2.1 Introduction

Feedback system is ubiquitous and has various applications. It is mainly grouped under *Positive* and *Negative Feedback systems* with the *Negative Feedback System* finding most widely used application in electronics and control following Black's invention of the Negative Feedback Amplifier [11]. Negative feedback system has numerous application benefits which includes gain stabilization, reduction of nonlinearity, impedance transformation (both input and output) and bandwidth enhancement. However feedback systems suffer from the potential of being unstable if not designed properly. This chapter explains the fundamental of feedback control system, stability requirement and discussion of exiting frequency compensation of OTA as an application of feedback system.

2.2 Feedback Control Theory

The basic block diagram of negative feedback control system is shown in Figure 2.1. It has a direct path (forward) gain denoted by *G(s)* and feedback gain, *H(s)*. Also *X(s)* and *Y(s)* serves as the input and output of the block diagram with *E(s)*, the feedback error, being the difference between the input, *X(s)* and the fed-back output *Y(s)H(s)*.

The following procedure can be followed to obtain the transfer function from *X(s)* to

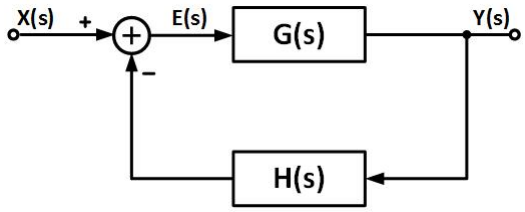


Figure 2.1: Basic feedback system block diagram

Y(s)

$$E(s) = X(s) - H(s)Y(s) \tag{2.1}$$

$$Y(s) = G(s)E(s) = G(s)[X(s) - H(s)Y(s)] \tag{2.2}$$

From Equ. 2.2, the transfer function, $\frac{Y(s)}{X(s)}$, is given by

$$\frac{Y(s)}{X(s)} = \frac{G(s)}{1 + H(s)G(s)} \tag{2.3}$$

Equ. 2.3 is called the closed-loop transfer function, so called because the output is sensed and fed-back to the input (forming a closed-loop) to control the system response. The feedback, in this case the negative feedback, works by minimizing the feedback error function, Equ. 2.1, in such a way that the output become a replica of the input. Another important notation is the Loop Gain, L(s) given in Equation 2.5.

The feedback system in Figure 2.1 can be applied to OTA in feedback with G(s) representing the open loop gain, A(s) of OTA and H(s) the feedback factor mostly denoted by β which may or may not be frequency dependent. The benefits for connecting OTA in this configuration can not be overemphasized. Using the open loop gain A(s) and feedback factor β, the closed loop transfer function similar to that in Equ. 2.3 is obtained as shown below with Y(s) and X(s) respectively denoted as V_{out} and V_{in}.

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1 + \beta A(s)} \tag{2.4}$$

$$L(s) = G(s)H(s) = \beta(s)A(s) \tag{2.5}$$

Open loop gain of OTA are mostly sensitive to process, voltage and temperature (PVT) variations and hence not accurately defined. Desensitization to these open loop effects is provided through negative feedback.

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+\beta A} = \frac{1}{\beta}\left(1 + \frac{1}{1+\beta A}\right) \approx \frac{1}{\beta} \tag{2.6}$$

From Equ.2.6, the closed loop gain to the first approximation is given by $\frac{1}{\beta}$ which is independent of A(s) and hence PVT assuming that the loop gain, $\beta A \gg 1$. Gain sensitivity function is defined by Equ. 2.7 which is inversely proportional to the amount of feedback (1+L(s)).

$$S_A^{A_{CL}} = \frac{\delta A_{CL}}{\delta A}\frac{A}{A_{CL}} = \frac{1}{1+\beta A} \tag{2.7}$$

$$\frac{\Delta A_{CL}}{A_{CL}} = S_A^{A_{CL}}\frac{\Delta A}{A} = \frac{1}{1+\beta A}\frac{\Delta A}{A} \tag{2.8}$$

Equ. 2.8 shows the application of the sensitivity function showing that variation in the open loop gain is reduced by the amount of feedback and hence the closed loop gain is desensitized from the open loop gain variations [1].

The transfer curve (plot of output against input) of amplifier in open loop has sigmoid shape and the open loop gain variation with respect to the input, Vin, is bell-shaped with the highest gain in the vicinity where Vin=0. As Vin moves away from this vicinity the gain drops creating non-linear effect and finally saturating to the supply rails as shown in Fig.2.2. Non-linearity can be defined as the change in the small signal gain of a system (in this the amplifier) as the input dc level is varied. To avoid this non-linearity and distortion, the negative feedback subtract a fed-back output from the input creating a predistorted error function. This works to linearized the closed loop and evident in Fig. 2.3

Comparing Fig. 2.2 and Fig. 2.3, it can easily be seen that the linear region of the open

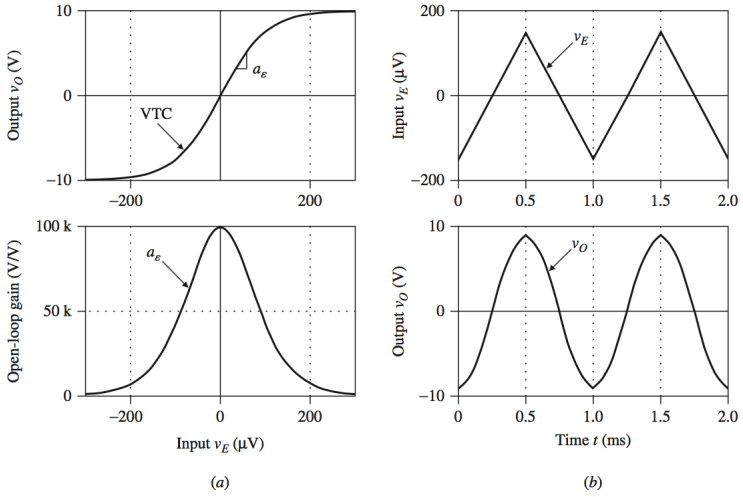


Figure 2.2: (a) Open-loop characteristics (VTC and gain a_ϵ) (b) Response of v_o to triangular input v_E. Reprinted from [1]

loop system has been extended to wider input range for the closed loop case. The negative feedback has linearized the system. Analysis of feedback on nonlinearity is extensively treated in [8, 2]

Negative Feedback also helps in extending the bandwidth of the amplifier. Assuming that A(s) is modelled as single pole system, the transfer function is given by

$$A(s) = \frac{A_o}{1 + \frac{s}{\omega_o}} \tag{2.9}$$

where A_o and ω_o are the low frequency gain and the 3-dB bandwidth respectively. With this definition for A(s), the closed loop transfer function can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{\frac{A_o}{1+\frac{s}{\omega_o}}}{1 + \frac{\beta A_o}{1+\frac{s}{\omega_o}}} = \frac{\frac{A_o}{1+\beta A_o}}{1 + \frac{s}{(1+\beta A_o)\omega_o}} \tag{2.10}$$

Comparing the 2.9 and 2.10, it can be seen that the closed loop 3-dB bandwidth has been extended by the amount of feedback $(1 + \beta A_o)$. It can also be seen that the gain has

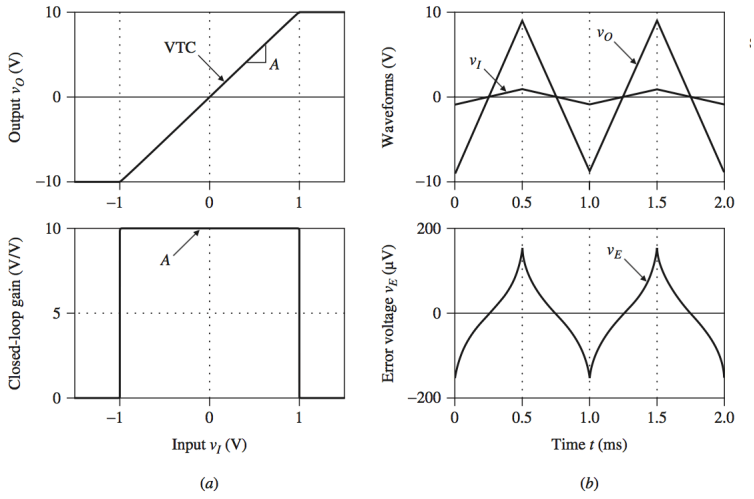


Figure 2.3: (a) Closed-loop characteristics (VTC and gain A= $\frac{1}{\beta} = 10$) (b) Input v_i undistorted output v_o and predistorted error signal v_E. Reprinted from [1]

been reduced by the same amount and as a results the gain bandwidth is constant for both open and closed loop system.

2.3 Stability of Feedback System

It is important to note that the transfer function derivation is based complex numbers and hence has magnitude and direction. Despite the numerous advantages of feedback system, there is a risk of instability if care is note taking in its design. Negative feedback works on the principle reduction of error function between the input and fedback output. However there is a delay between when the output is sensed and finally subtracted from the input to generate the error function. This delay may results in overcompensation of the input error resulting in regenerative effect causing the error function to diverge and hence drive the system unstable.

Considering Equ. 2.4, repeated below for emphasis

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+\beta A} = \frac{1}{\beta}\left(1 + \frac{1}{1+\beta A}\right)$$

when $\beta A(s = jw) = -1$, $\frac{V_{out}}{V_{in}} = 1/0 = \infty$ resulting in instability. Under this condition the circuit amplifies its own noise until it eventually begins to oscillate. This condition is defined formally below

$$|\beta A(jw)| = 1 \tag{2.11}$$

$$\angle \beta A(jw) = 180^\circ \tag{2.12}$$

and are called the "Barkhausen's Criteria". The criteria state that oscillation occurs at a frequency ω when a total phase shift of 360° is travelled around the loop and at a gain greater than or equal to 1. Since negative feedback accounts for 180° phase of the total 360° phase required for oscillation, the signal is left with additional 180° phase shift for oscillation to occur if the gain ≥ 1 hence the criteria.

From another perspective, stability can be determined by inspecting the denominator of the closed loop transfer function and observing if the real parts of the roots are negative or positive. The system is stable if the real parts of roots of closed loop denominator, called poles of the closed loop system, are negative [12].

This may suggest the determination of closed loop poles to establish stability but closed loop transfer function is not always readily available. An alternative way is to determine the stability from the open loop transfer function and there are existing tools to do this. One the numerous ways is using Stability Margins to determine stability. Phase Margin (PM) and Gain Margin (GM) form the stability margins.

Phase Margin is the amount degrees by which $\angle \beta A(j\omega_x)$ can be reduced until it reaches -180°. Crossover frequency, ω_x, is the frequency at which the open loop gain becomes

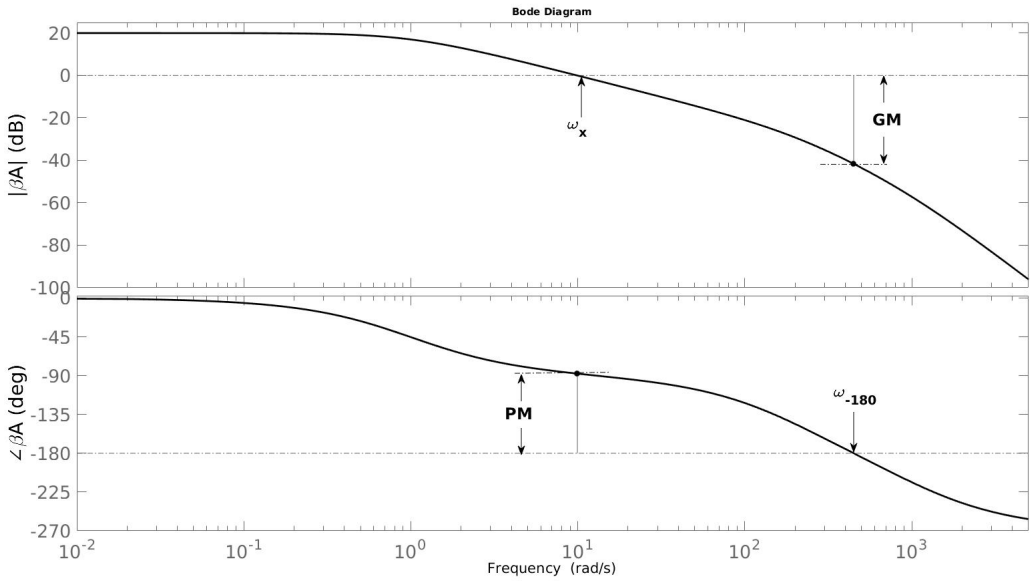


Figure 2.4: Bode plot with GM and PM

unity or 0 dB. The mathematical expression of PM is given below in Equ. 2.13

$$PM = 180^\circ + \angle \beta A(j\omega_x) \tag{2.13}$$

Though a positive number for phase margin means the system is stability, to ensure acceptable transient response, that is a system with less overshoot and sufficient settling time, a PM >45° is required [13].

Gain Margin (GM) on the other hand is referenced to ω_{-180} which is the frequency at which the phase crosses -180°. It is the inverse of the gain measured at a frequency of ω_{-180} ie it is the amount, the gain at $|\beta A(j\omega_{-180})|$ can be reduced until it reaches 0 dB. It is mathematically expressed dB as

$$GM = 20log\left(\frac{1}{|\beta A(j\omega_{-180})|}\right) \tag{2.14}$$

Like the PM, a positive GM is required for stability and can be seen on Figure 2.4. PM most especially has a direct relationship to the overshoot, settling time, rise time etc in second order system. Its effect can not be directly seen for higher order system, however they are still used as a measure of the effectiveness of OTA compensation. This approach will be followed as we discuss the various exiting OTA compensation in the next section.

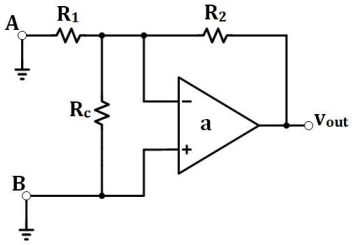
2.4 Various Compensation

The condition for stability as stated above requires that the total cumulated phase around the loop be $\angle L(j\omega_x) \leq -180°$. Frequency compensation is modifying the loop transfer function L(s) in such a way to provide adequate phase margin. From Equation 2.5 $L(s) = \beta(s)A(s)$, one can say that frequency compensation can be achieved by

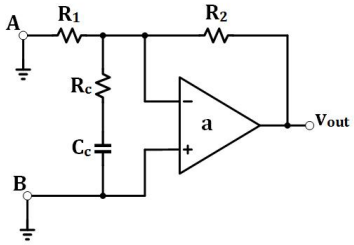
- modifying the feedback factor $\beta(s)$ which leads to external frequency compensation
- modifying the open loop transfer function A(s), which leads to internal frequency compensation
- modifying both $\beta(s)$ and A(s)

External compensation which includes loop gain reduction, input-lag compensation, feedback-lead compensation etc is usually done to change the amplifier characteristics at the application level [1]. Figures 2.5 and 2.6 show respectively the various external compensation strategies and their frequency response. Internal compensation strategy on the other hand is concerned with modifying the amplifier characteristics at the integrated circuit (IC) level and will be the focus of this review.

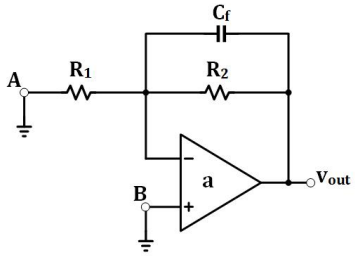
Modification of the open loop characteristics is done so as to ensure that even in the worse case frequency independent feedback ($\beta = 1$), the system remains stable. Internal frequency compensation is broadly grouped under 5 headings, namely:



(a) Loop gain reduction



(b) Input-lag compensation



(c) Feedback lead compensation

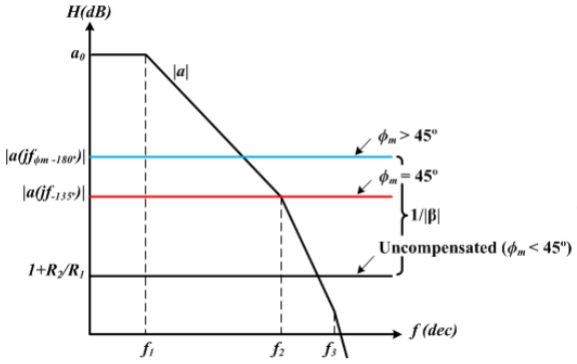
Figure 2.5: External compensation strategies.
Reprinted from [1]

1. Dominant Pole Compensation
2. Shunt Capacitance Compensation
3. Miller Compensation
4. Pole-Zero Compensation
5. Feedforward Compensation

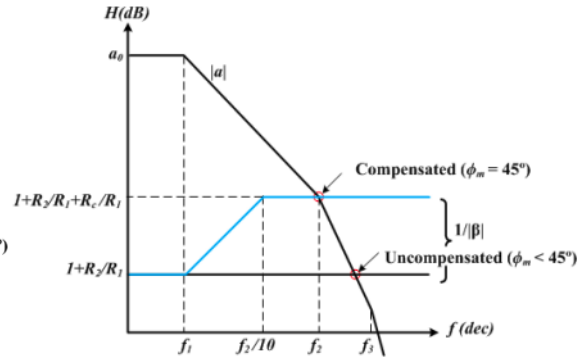
2.4.1 Dominant Pole Compensation (DPC)

Under this compensation scheme, the poles of the uncompensated amplifier are not altered. Compensation is achieved by creating additional pole at a low enough frequency such that it becomes the dominant pole and produces -20 dB/dec roll-off until the crossover frequency (f_x). This ensures that the rate of closure (ROC) given by Equation 2.15 is ≤ 30 dB which implies PM $\geq 45°$. The relationship between ROC and PM is elaborated in Appendix A

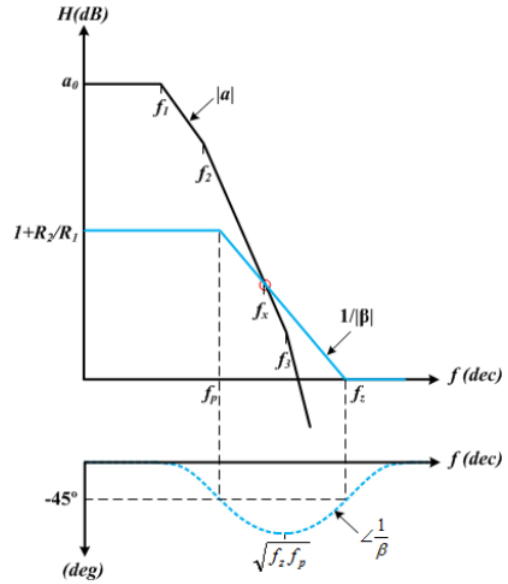
$$ROC = |\frac{1}{\beta(jf_x)}| - |A(jf_x)| \tag{2.15}$$



(a) Loop gain reduction response



(b) Input-lag response



(c) Feedback lead response

Figure 2.6: Frequency response of various external compensation strategies
Reprinted from [1]

$$T_{DPC} = \frac{a_o}{(1+s/f_1)(1+s/f_2)(1+s/f_3)(1+s/f_4)} \tag{2.16}$$

where $f_i \approx \frac{1}{2\pi R_i C_i}$, i=1, 2, 3, 4 and $f_D = f_4$.

Dominant Pole Compensation does not use any of the exiting poles but introduce another pole shown in Figure 2.7 which limits the bandwidth of the system. The approximate transfer function of the system is given by Equation 2.16. The highest achievable gain

bandwidth is the dominant pole (f_1) of the uncompensated system which is mostly low. Figure 2.8 illustrate the compensation and the gain bandwidth limitation.

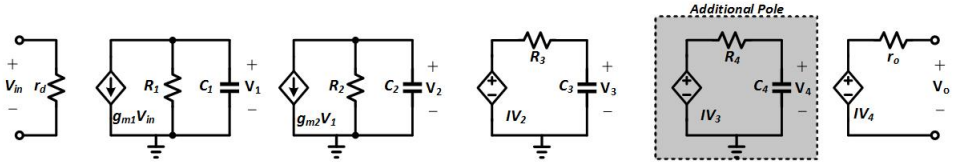


Figure 2.7: Amplifier with dominant pole compensation
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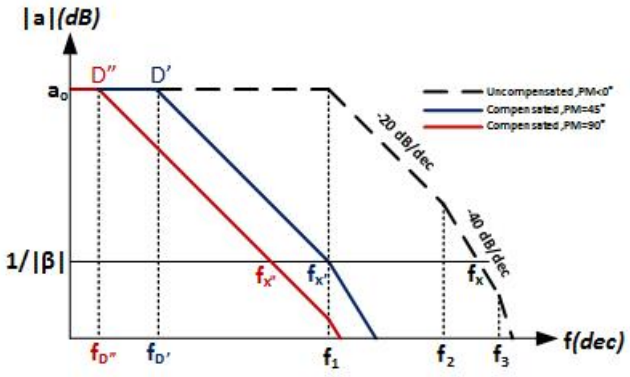


Figure 2.8: Magnitude response showing dominant pole compensation

2.4.2 Shunt Capacitance (SCC)

Unlike the DPC, shunt capacitance compensation (SCC) uses the system's exiting poles by rearranging these poles to ensure an ROC of $\leq$ 30 dB. It does this through C_c which pushes the first pole to lower enough frequency as shown in Figure 2.9. Equation 2.17 is the transfer function of the system shown in Figure 2.9.

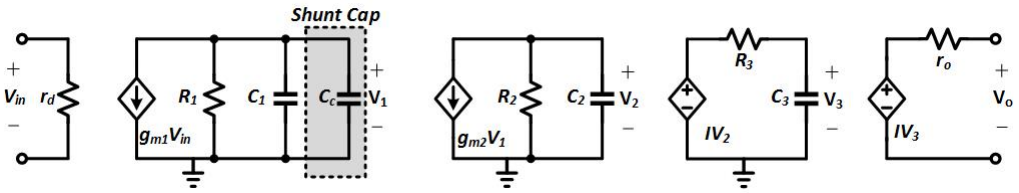


Figure 2.9: Amplifier with shunt capacitance compensation
Reprinted from [1]

$$T_{SCC} = \frac{a_o}{(1 + s/f_D)(1 + s/f_2)(1 + s/f_3)} \tag{2.17}$$

where $f_i \approx \frac{1}{2\pi R_i C_i}$, i=2, 3 and $f_D \approx \frac{1}{2\pi R_1 (C_1 + C_c)}$.

The highest gain bandwidth product that can be obtained is f_2 which is mostly larger that f_1 ie higher GBW can be obtained in this case than in the DPC case. The capacitor C_c required for compensation is mostly big and may not suitable for monolithic IC design because of area constraint. Figure 2.10 shows the compensation using SCC and the movement of the poles.

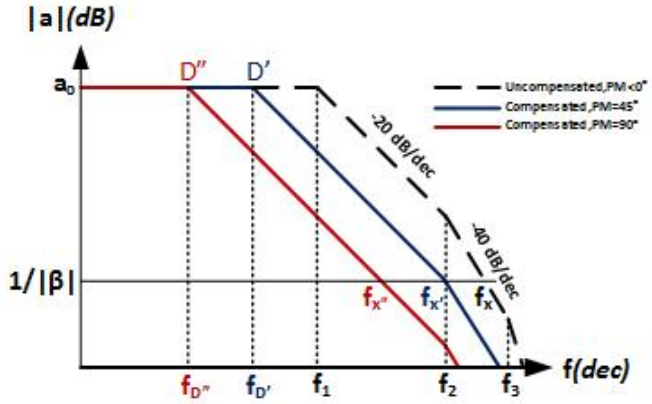


Figure 2.10: Magnitude response showing shunt capacitor compensation

2.4.3 Miller Capacitor Compensation(MCC)

This compensation strategy shown in Figure 2.11 uses the miller multiplication of capacitor (explained in Appendix B) to implement compensation using smaller capacitor value hence saving area. It ensures pole-splitting pushing the dominant pole to lower frequency and the non-dominant pole to higher frequency for increasing compensation capacitor C_c.

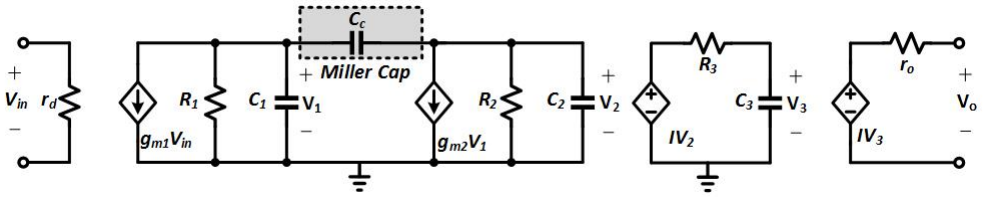
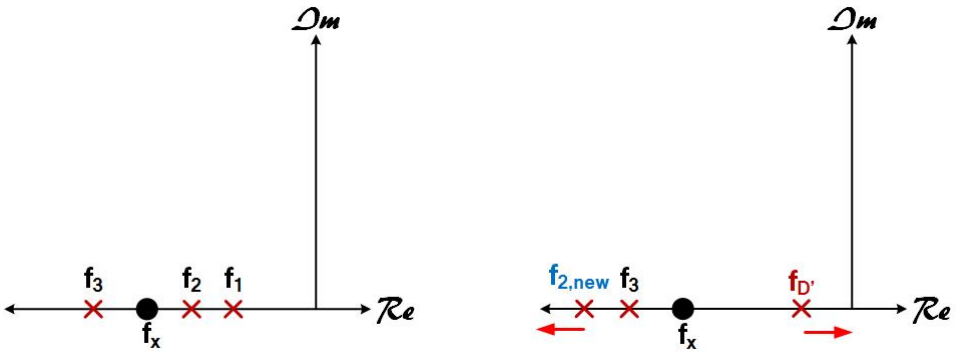


Figure 2.11: Amplifier with miller capacitor compensation
Reprinted from [1]

Miller capacitor compensation (MCC) is one of the widely used compensation scheme in monolithic IC because it achieves pole splitting, shown in Figure 2.12, with minimum capacitor which saves area. It however, creates a non-minimum phase zero (RHP zero) because of the alternative feedforward path it provides for signal to flow to the output through C_c. There exit numerous techniques to combat this effect and still harness its benefits. These techniques will be touched on in a later section. Figure 2.13 shows the magnitude response and the gain bandwidth limitation of miller capacitor compensation. It can be seen that GBW is limited by f_3 which is higher than f_2 hence MCC has the highest achievable GBW in comparison to SCC and DPC.



(a) Before miller compensation (b) After miller compensation

Figure 2.12: P-Z map illustrating miller compensation

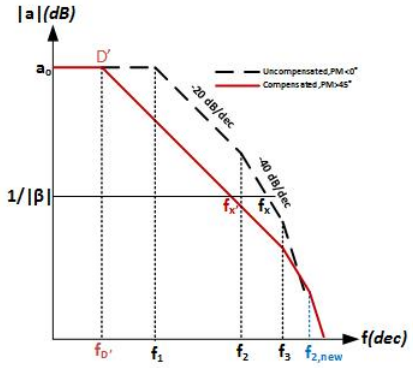


Figure 2.13: Magnitude response showing miller capacitor compensation

2.4.4 Pole Zero Compensation (PZC)

Pole Zero Compensation (PZC) is a variant of SCC where a capacitor in series with resistor, illustrated in Figure 2.14, is used instead of just a shunt capacitor. $R_c \ll R_1$ and $C_c \gg C_1$ ensures that the first dominant pole is pushed to a sufficiently low frequency so as to obtained an $ROC \leq 30$ dB ensuring stability.

In addition to this PZC create a zero to cancel the first non-dominant pole f_2 such that f_3 becomes the first non-dominant pole after compensation. It can be seen that the

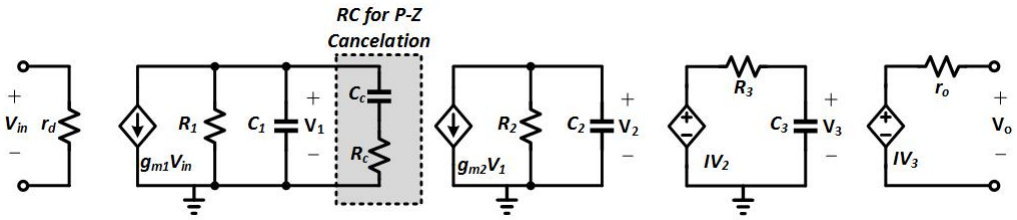
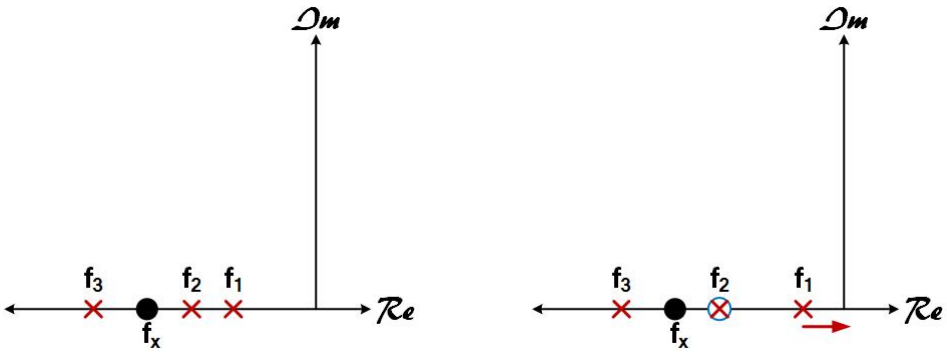


Figure 2.14: Amplifier with PZ compensation
Reprinted from [1]

maximum achievable GBW is f_3 which is mostly greater than f_2. The p-z map of the system, before and after PZC is illustrated in Figure 2.15. Also Figure 2.16 shows the magnitude response and the GBW limitation of system with pole-zero compensation.



(a) Before pole-zero compensation (b) After pole-zero compensation

Figure 2.15: P-Z map illustrating pole-zero compensation

2.4.5 Feedforward Compensation

Under this compensation scheme, a feedforward bypass is provided around the speed bottleneck path. This ensures that slow path is avoid at high frequency to increase the speed of the system. The feedforward path is mostly implemented shown in Equ.2.19 as

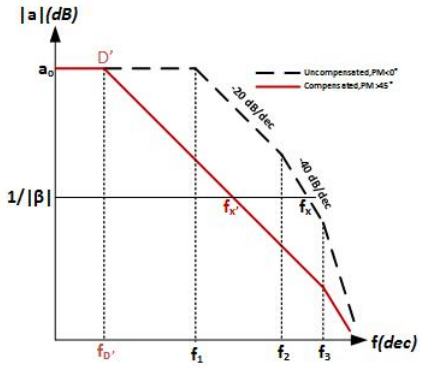


Figure 2.16: Magnitude response showing pole-zero compensation

a high pass attenuating the signal at low frequency but passing it at high frequency. From Figure 2.17 one can write input-output transfer function as Equ.2.18

$$\frac{V_o}{V_{in}} = (a_1(s) + h_{ff}(s))a_2 \tag{2.18}$$

$$h_{ff} = \frac{jf/f_o}{1 + jf/f_o} \tag{2.19}$$

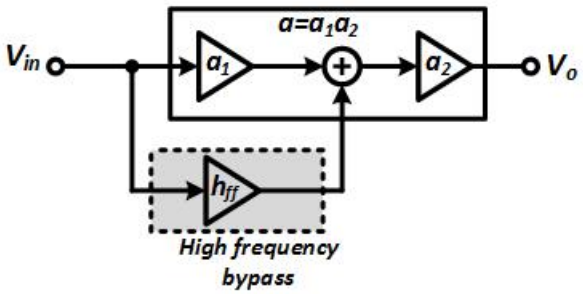


Figure 2.17: Amplifier with feedforward compensation
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At low frequency $|h_{ff}(s)| \ll |a_1(s)|$ hence $V_o/V_{in} = a_1(s)a_2(s) = a(s)$. This shows that the high gain at low frequency for the uncompensated amplifier is not degraded. At

high frequency $|h_{ff}(s)| \approx 1 \gg |a_1(s)|$ hence $V_o/V_{in} \approx a_2(s)$. This proves that the systems dynamics at high frequency is solely controlled by a_2 and the slow path a_1 is avoided.

The feedforward path can also be implemented with a transconductance stage. Numerous benefits including RHP zero compensation, pole-zero cancellation and improvement in large signal performance can be obtained by using a single transconductance stage as feedforward path.

2.5 Existing Op Amp Compensation

Under this section we look at existing amplifier compensations, which include, as we will see a combination of the above internal frequency compensation strategies. This sections looks at the various three-stage and four-stage OTA compensation schemes.

2.5.1 Compensation Schemes: Three Stage OTA

Compensation schemes for three-stage OTAs has been a well-developed research area. There exist numerous schemes and for the purpose of this thesis will be grouped under three main headings.

Compensation with two miller capacitor

The direct application of miller compensation to three stages results in a famous compensation scheme called nested miller compensation (NMC) [14] shown in Figure 2.18a. From the transfer function of NMC given in Equation 2.20, there two zeros associated with this configuration, a left half plane (LHP) zero and a right half plane (RHP) zero. The zeros are assumed to be at higher frequency and hence do not affect the stability. This assumption requires pumping more current to push these zeros out of the frequency of

interest.

$$
\begin{aligned}
A_{v,NMC} &= \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}\left(1 - s\frac{C_{m2}}{g_{mL}} - s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}}\right)}{(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1 + s\frac{C_{m2}(g_{mL}-g_{m2})}{g_{m2}g_{mL}} + s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right]} \\
&\approx \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}}{(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left(1 + s\frac{C_{m2}}{g_{m2}} + s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right)}
\end{aligned}
\tag{2.20}
$$

The most common design procedure involves the assumption of unity feedback and using butterworth condition as elaborated in [15]. According to [15], the internal compensation capacitor limits the speed of the system. Also the sizes of the compensation capacitors are comparable to C_L hence not suitable for large capacitive loads.

There are variants of NMC so implemented to improve its short comings. To avoid the RHP zero of NMC which is due to the feedforward path for the small signal, nested miller with nulling resistance (NMCNR) is implemented [16]. As shown in Figure 2.18b ,the resistor, R_m, increases the forward path impedance reducing the feedforward signal and hence pushing the RHP to higher frequency. The RHP zero can altogether be eliminated by ensuring that $R_m = 1/g_{mL}$ as can be seen from the transfer function in Equation 2.21. The PM is increased because of the LHP left after the elimination of the RHP.

$$
\begin{aligned}
A_{v,NMCNR} &= \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}}{1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L} \\
&\times \left(\frac{1 + s\left[C_{m1}R_m + C_{m2}\left(R_m - \frac{1}{g_{mL}}\right)\right] + s^2\frac{C_{m1}C_{m2}(g_{mL}R_m - 1)}{g_{m2}g_{mL}}}{1 + s\frac{C_{m2}(g_{mL}-g_{m2})}{g_{m2}g_{mL}} + s^2\frac{(1-g_{m2}R_m)C_LC_{m2}}{g_{m2}g_{mL}}}\right) \\
&\approx \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}\left(1 + s\frac{C_{m1}}{g_{mL}}\right)}{(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1 + s\frac{C_{m2}(g_{mL}-g_{m2})}{g_{m2}g_{mL}} + s^2\frac{(1-g_{m2}R_m)C_LC_{m2}}{g_{m2}g_{mL}}\right]}
\end{aligned}
\tag{2.21}
$$

Multipath nested miller compensation (MNMC)[15] uses a feedforward transconduc-

tance to create a low frequency zero to cancel the first non-dominant pole so as to increase both GBW and PM. As shown in Figure 2.18c, g_{mf1} is sized so as to eliminate the second pole. Though the pole-zero cancellation is within the band of interested it was shown in [15], to be stable for different condition of C_L and g_{mL} hence it is stable under dynamic conditions at the output. The transfer function is given in Equation 2.22 from which the condition of g_{mf1} is given (Equation 2.23) and elaborated in [15]

$$A_{v,MNMC} = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left(1+s\frac{C_{m1}g_{mf1}}{g_{m1}g_{m2}}\right)}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left(1+s\frac{C_{m2}}{g_{m2}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right)} \tag{2.22}$$

$$g_{mf1} = 4.45g_{m2} \tag{2.23}$$

NGCC (shown in Figure 2.18d) introduced by You *et al* [17] has a compact transfer function and hence compact design procedure than any of the above schemes. It ensures that the feed forward signal through the various compensation capacitors are eliminated by a feedforward transconductance. By setting $g_{mfi} = g_{mi}$, the circuit reduces to a non-zero system similar to NMC without requiring the $g_{mL} \gg g_{m1}, g_{m2}$ condition. The transfer function is given in Equation 2.24. A variant of NGCC called NMC with feedforward Gm stage (NMCF) [15] shown in Figure 2.18e takes advantage of LHP zero to improve the PM. The transfer function of NMCF is given by Equation 2.25 with $k_g = g_{m2}/g_{mL}$ and $m = (g_{mf2}/g_{m2}) > 1$. The condition on *m* is necessary to ensure LHP poles and hence stability of the system.

$$A_{v,NGCC,3} = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left[1+s\frac{C_{m2}(g_{mf2}-gm2)}{g_{m2}g_{mL}}+s^2\frac{C_{m1}C_{m2}(g_{mf1}-g_{m1})}{g_{m1}g_{m2}g_{mL}}\right]}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1+s\frac{C_{m2}(g_{mf2}-g_{m2}+g_{mL})}{g_{m2}g_{mL}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right]}$$
$$= \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1+s\frac{C_{m2}}{g_{m2}g_{mL}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right]} \tag{2.24}$$

$$A_{v,NMCF} = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L\left[1+s\frac{C_{m2}(m-1)}{g_{mL}}-s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}}\right]}{(1+sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L)\left[1+s\frac{C_{m2}(g_{mf2}-g_{m2}+g_{mL})}{g_{m2}g_{mL}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{mL}}\right]} \tag{2.25}$$

Transconductance with capacitance feedback compensation, TCFC [18] is another variant of NMC where a current buffer is added to the innermost loop capacitor as shown in Figure 2.18f. This has the advantage of preventing the feedforward small signal and hence blocking RHP zero. It has additional feedforward transconductance which helps with large signal performance.

Another compensation scheme using two miller compensation capacitors is reverse nested miller compensation (RNMC)[14]. As shown in Figure 2.18g, this compensation scheme differs from NMC primarily by the internal loop. RNMC does not suffer speed degradation because the internal compensation capacitor C_{m2} does not load the output capacitor. RNMC feedforward with nulling resistor (RNMCFNR) and Reversed active feedback frequency compensation (RAFFC) [19] are variants of RNMC as shown in Figure 2.18h and 2.18i respectively, with enhanced performance and also power and area savings. Also RAFFC has the added advantage of no extra circuitry as proposed by [19]. Positive feedback compensation (PFC)[20] is topologically similar to RNMC with the only difference being the polarity of the second and third transconductance stages as shown in Figure 2.18j. The second stage form a positive feedback with C_{m2} which provides damping factor control for complex poles.

Compensation with no inner miller capacitor

Though RNMC and its variant improves the speed by reducing the output loading by the inner capacitor, the presence of two capacitors for compensation increases the area especially for large capacitive loads. To further improve the speed and reduce the area for large loads, the innermost capacitor is removed and various means are provided to control the damping factor in the following compensation schemes.

Damping factor control frequency compensation (DFCFC) [21] as said earlier removes the inner capacitor and with damping factor control block made up of a transconductance and a feedback capacitor, controls the damping factor of the complex pole. This helps prevent peaking in the frequency response. Large signal improvement is ensured by a push-pull effect through g_{mf2} as shown in Figure 2.19a.

Single miller capacitor (SMC) and single miller capacitor with feedforward compensation (SMFFC) [22] uses feedforward transconductances (one in SMC and two in SMFFC) to improve system performance shown respectively in Figures 2.19b and 2.19c. SMC uses pole-zero cancellation for improved system performance and in addition to this, SMFFC adds LHP improving the PM of the system.

To prevent the RHP zero and to reduce the compensation capacitance saving the area overhead, a variant of SMC without the feedforward transconductance and with current amplifier in the feedback path is proposed as shown in Figure 2.19d. This scheme called single capacitor with current amplification compensation (SCCAC)[23] has recorded load range of about $20\times$ in literature.

Cross feedforward cascode compensation (CFCC)[24] is topologically same as SMFFC with the only different being the cascode compensation shown in Figure 2.19e. The cascode compensation which is miller compensation with current buffer prevents the RHP zero due to feedforward signal through C_m

To counteract the damping factor effect of the complex pole of system after remov-

ing the inner capacitance, a passive LHP zero is introduce to improve system performance. This compensation scheme called impedance adapting compensation (IAC)[25] has increased bandwidth with this added zero. A variant of IAC called ultra area-efficient (UAE)[26] amplifier has all the benefits of IAC with an added benefit of area savings. Also the position of passive zero block which is a resistor in series with a capacitor is at the output of the first stage not at the second stage as in IAC. The current buffer in feedback path help eliminate the RHP zero in the system. Figures 2.19f and 2.19g show compensation schemes IAC and UAE respectively.

The authors of [3] proposed a compensation which similar to UAE with the only difference being how the LHP zero is generated. In the case of [3], LHP zero is created from an active zero generation block shown in Figure 2.19h. The author of [3] uses local feedback loop (LFL) analysis and realized that the added passive zero block in addition to creating a LHP zero creates a low frequency pole with limits the ω_μ of the local feedback loop of IAC [25]. An active zero generation block does not have this effect and hence ensures extension of the load range of the amplifier ($15\times$).

The author of [27] introduces a buffer between the active zero block of [3] to further prevent the limit on the ω_μ provided by the active block. The active zero generation block provides a heavy savings on area with minimal/no power overhead when blocks are reused. This compensation scheme is shown in Figure 2.19i

Compensation with complex compensation

This section comprises compensation schemes that involve combination of already exiting schemes.

Dual active capacitive feedback compensation (DACFC)[28] uses only one capacitor with two buffers feedback to the output of the first and second stages as shown in Figure 2.20a. It is similar to CFCC and because of the single capacitor prevents the output stage loading by the inner capacitor which in effect improve the speed performance. The buffers

help in the elimination of RHP zero of the system saving power and ensuring improved system performance.

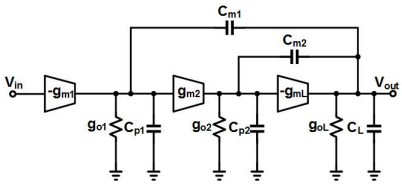
Dual loop parallel compensation (DLPC)[29] combines the benefits of DFCFC in controlling the damping factor and cascode miller compensation which eliminate the RHP zero in a single amplifier as shown in Figure 2.20b. This results in an increased unity gain frequency.

Active feedback frequency compensation (AFFC) [30] has two basic blocks, a high gain block and a high speed block. The high speed block provides an alternate path to skip slow high gain block. The high speed block is composed of cascode miller compensation. This helps to increase the bandwidth. AC boosting compensation (ACBC)[31] is similar to AFFC in the sense that an alternate path is provided to curb the gain reduction of the second stage at high frequency. This alternate path called a high frequency gain stage is wrapped around the second stage and help to extend the unity bandwidth. AFFC and ACBC are shown in Figure 2.20c and 2.20d respectively.

2.5.2 Compensation Schemes: Four Stage OTA

Four stage OTAs have been an active research area recently. The compensation scheme can be traced back to application of three stage compensation schemes on four stages. The initial assumption that the added stage increases power consumption and complicates the compensation scheme has been refuted as some compensation schemes have comparable or even lower power consumption with comparable or better results as their three stage counterpart. Also the added stage can serve to provide extra degree of freedom to realize various performance parameters cared about.

[32] is a four stage OTA using two miller compensation with nulling resistor shown in 2.21a. Two zeros generated are placed in such a way to help with the phase degradation. The system has improved performance but at the expense of power consumption. The



(a) NMC
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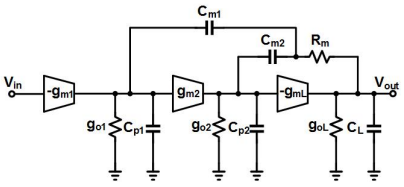

(b) NMCNR
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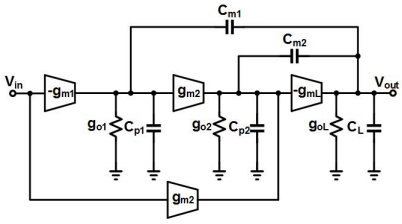

(c) MNMC
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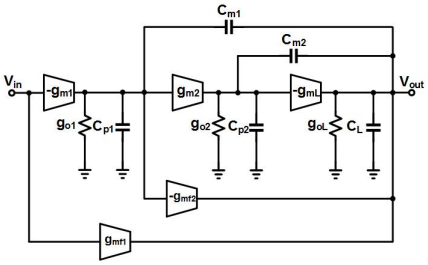
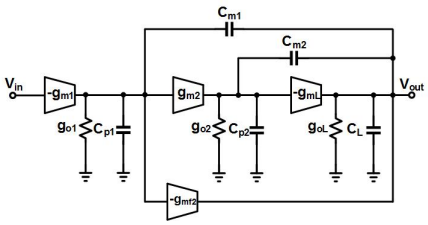
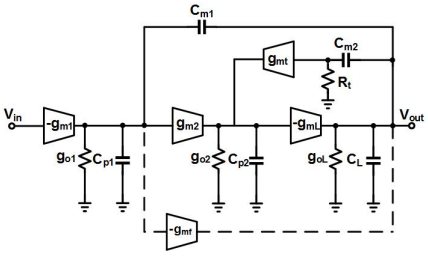


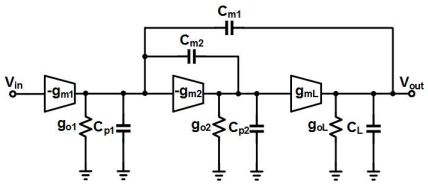
(d) NGCC
Reprinted from [17]



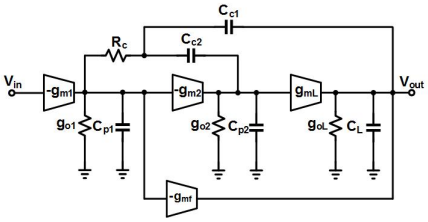
(e) NMCF
Reprinted from [15]



(f) TCFC
Reprinted from [18]



(g) RNMC
Reprinted from [14]



(h) RNMCFNR
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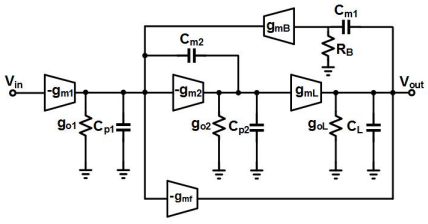
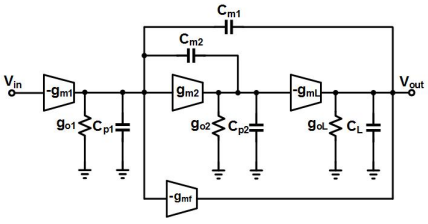


(i) RAFFC
Reprinted from [19]



(j) PFC
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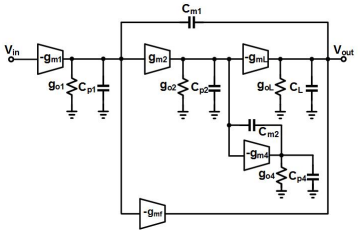
Figure 2.18: Three stage OTA:Compensation with two miller capacitor



(a) DFCFC
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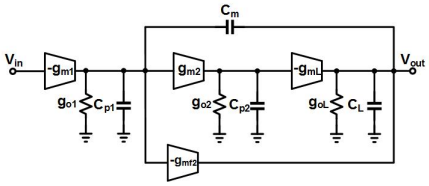
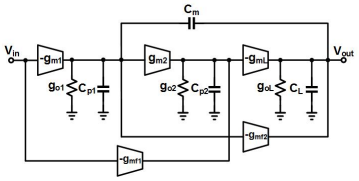
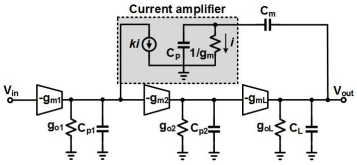


(b) SMC
Reprinted from [22]



(c) SMFFC
Reprinted from [22]



(d) SCCAC
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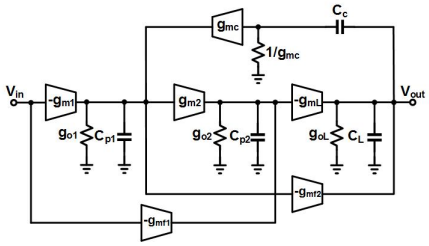
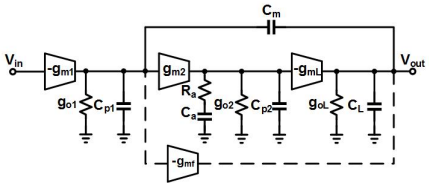


(e) CFCC
Reprinted from [24]



(f) IAC
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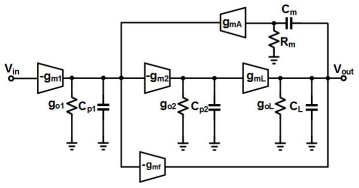
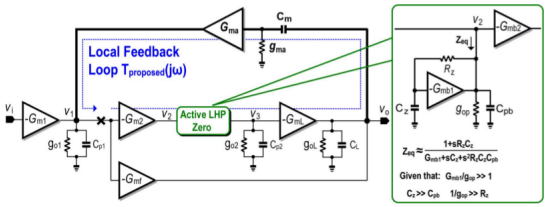
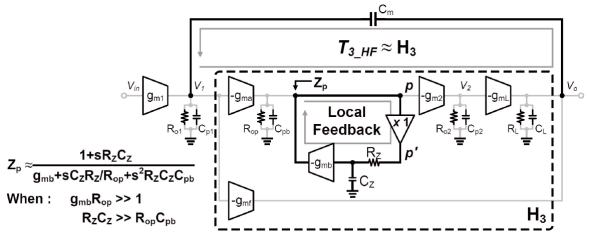


(g) UAE
Reprinted from [26]

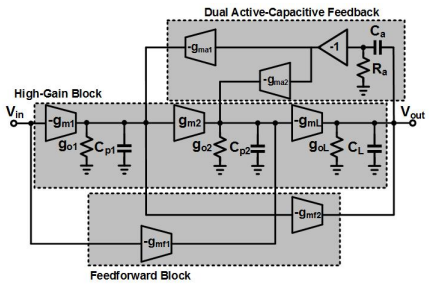


(h) Reprinted from [3]



(i) Reprinted from [27]

Figure 2.19: Three stage OTA:Compensation with a single miller capacitor



(a) DACFC
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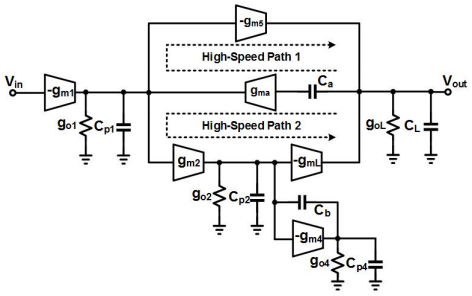

(b) DLPC
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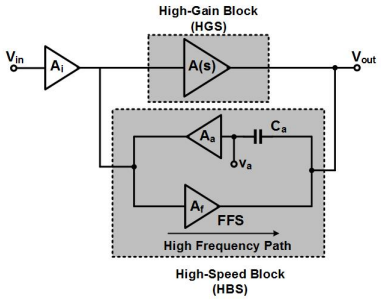

(c) AFFC
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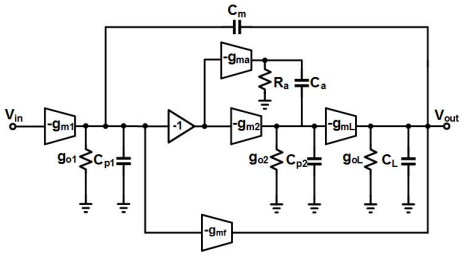
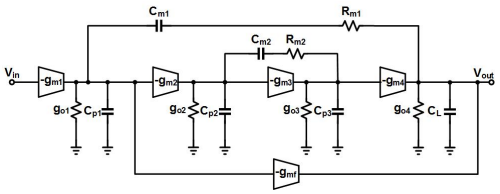
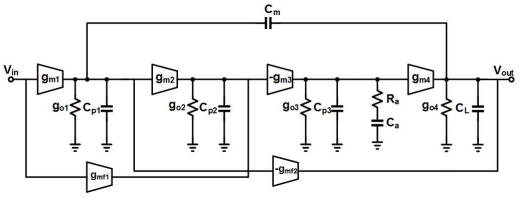


(d) ACBC
Reprinted from [31]

Figure 2.20: Three stage OTA:Complex compensation



(a) Reprinted from [32]



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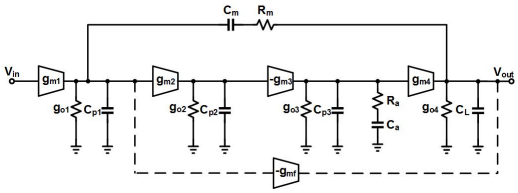

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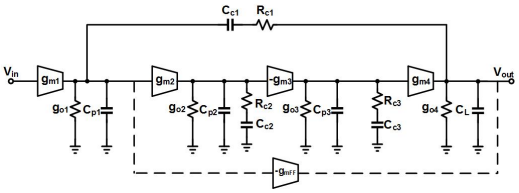

(d) Reprinted from [34]

Figure 2.21: Four stage OTA:Compensation schemes

presence of two resistor increases the noise of the system.

Impedance adapting compensation (IAC) scheme is applied to four stage OTA in [34], [10] and [33]. [10] and [34] has cascode miller compensation which help eliminate RHP zero in the system. Also according to Figure 2.21c [10] has only one passive zero generation block at the output of the third stage whiles [34] has two passive generation blocks at the output of second and third stages as shown in Figure 2.21d. Like [10], the authors of [33] uses a single passive zero generation block at same location and a simple miller compensation in the outermost loop as can be seen in Figure 2.21b. [33] uses feedforward transconductance stages to help improve system performance by ensuring 2 pole-zero cancellation in addition to the passive zero generated. Also the large signal performance is enhanced through second feedforward transconductance.

The effectiveness of the passive zero generation block in these four stage OTA influenced the proposed design which uses a single compensation capacitor and active zero generation block similar to [3] in a four stage OTA.

3. PROPOSED DESIGN

As the number gain stages increases, only one form of internal compensation becomes insufficient to provide the required stability margins for acceptable transient response and as a results a combination of the various internal compensation technique is used. In this chapter a four stage OTA with wide capacitive load drive is proposed. The proposed OTA uses miller compensation and active LHP zero compensation, which is similar to pole-zero compensation, to compensate the OTA over a wide range of capacitive loads. A slew rate helper is used to enhanced the slew performance of OTA with minimal power overhead. The transfer function and design procedure is given in this chapter elaborating the advantage of this design over the already existing techniques.

3.1 Principle of Operation

The block diagram of proposed design is shown Figure 3.1. As can be seen, there are five transconductances, namely;g_{m1}, g_{ma}, g_{mb}, g_{m3} and g_{m4}, in the forward path with g_{ma} and g_{mb} implementing g_{m2} and effectively giving a four stage OTA. Parasitic conductances and capacitances per stage is denoted by g_{oi} and C_{pi} respectively where i=1, b, 3, 4. g_{oz} and C_{pz} are the parasitics of the active zero LHP generation block. As stated in previous chapter, the care about of amplifiers are the gain, speed, area and power consumption. The gain of the OTA is given by the product of per stage transconductance and conductance ratios as shown is Figure 3.1.

Each added gain stage introduce a low frequency pole which poses stability issues. The stability of proposed OTA is ensured through C_m which implements miller compensation and an active LHP zero block implemented with g_{mz}, R_z and C_z. The miller capacitor, C_m, ensures pole splitting pushing the dominant pole to a lower enough frequency to ensure single pole characteristics until the crossover frequency. The interaction between high

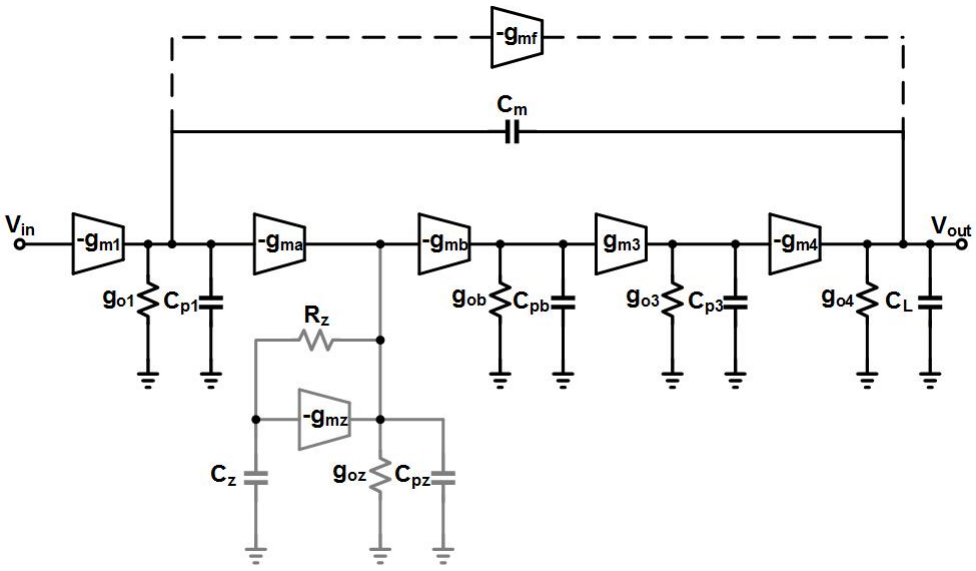

Figure 3.1: Block diagram of proposed design

frequency pole due to miller compensation and the second non-dominant pole creates a high-Q complex pole. This is suppress by the zero created by the active zero generation block. With this zero carefully placed, the phase degradation by the complex pole is compensated giving an acceptable PM and hence a good transient response. To help with the large signal response, an optional feed-forward transconductance, g_{mf}, can be used.

3.2 Transfer Function

The transfer function of the proposed design is obtained based on the following assumptions;

- $C_L \gg C_m > C_z \gg C_{pi}$ where i=1,..,4,z and b=2
- $\frac{g_{mi}}{g_{oi}} \gg 1$ where $g_{m2} = \frac{g_{ma}g_{mb}}{g_{mz}}$, i=1,..,4,z and b=2

The detailed transfer function using the above conditions is given in Equation 3.1.

$$H(s) = \frac{b_0 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4 + b_5 s^5}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5 + a_6 s^6} \tag{3.1}$$

where

$$
\begin{aligned}
a_0 &= \frac{g_{o1}g_{o3}g_{o4}g_{ob}g_{mz}}{R_z} & b_0 &= \frac{g_{m1}g_{m3}g_{m4}g_{ma}g_{mb}}{R_z} \\
a_1 &= \frac{C_m g_{m3}g_{m4}g_{ma}g_{mb}}{R_z} & b_1 &= C_z g_{m1}g_{m3}g_{m4}g_{ma}g_{mb} \\
a_2 &= C_m C_z g_{m3}g_{m4}g_{ma}g_{mb} & b_2 &= -\frac{C_m C_z g_{m1}g_{o3}g_{ob}}{R_z} \\
a_3 &= \frac{C_L C_m C_z g_{o3}g_{ob}}{R_z} & b_3 &= -\frac{C_m C_z C_{pb} g_{m1}g_{o3}}{R_z} \\
a_4 &= \frac{C_L C_m C_z C_{pb}}{R_z} & b_4 &= -\frac{C_m C_z C_{pb} C_{p3} g_{m1}}{R_z} \\
a_5 &= \frac{C_L C_m C_z C_{pb} C_{p3}}{R_z} & b_5 &= -C_m C_z C_{pb} C_{p3} C_{pz} g_{m1} \\
a_6 &= C_L C_m C_z C_{pb} C_{p3} C_{pz}
\end{aligned}
\tag{3.2}
$$

The above transfer function, Equation 3.1, can be expressed in factored form as given in Equation 3.3 by using the approach in [35].

$$
H(s) = \frac{A_{dc}[(1+\frac{1}{\omega_{z1}}s)(1+\frac{1}{\omega_{z2}}s)(1+\frac{1}{\omega_{z3}}s)(1+\frac{1}{\omega_{z4}}s)(1+\frac{1}{\omega_{z5}}s)]}{(1+\frac{1}{\omega_{3dB}}s)(1+\frac{1}{\omega_o Q}s+\frac{1}{\omega_o^2}s^2)(1+\frac{1}{\omega_{p3}}s)(1+\frac{1}{\omega_{p4}}s)(1+\frac{1}{\omega_{p5}}s)} \tag{3.3}
$$

where

$$
\begin{aligned}
A_{dc} &= \frac{g_{m1}g_{m3}g_{m4}g_{ma}g_{mb}}{g_{o1}g_{o3}g_{o4}g_{ob}g_{mz}} & \omega_{3dB} &= \frac{g_{o1}g_{o3}g_{o4}g_{ob}g_{mz}}{C_m g_{m3}g_{m4}g_{ma}g_{mb}} \\
\omega_{z1} &= \frac{1}{R_z C_z} & \omega_o Q &= \frac{1}{R_z C_z} \\
-\omega_{z2} &= \frac{g_{m3}g_{m4}g_{ma}g_{mb}R_z}{C_m g_{o3}g_{ob}} & \omega_o^2 &= \frac{g_{m3}g_{m4}g_{ma}g_{mb}}{C_L C_z g_{o3}g_{ob}} \\
\omega_{z3} &= \frac{g_{ob}}{C_{pb}} & \omega_{p3} &= \frac{g_{ob}}{C_{pb}} \\
\omega_{z4} &= \frac{g_{o3}}{C_{p3}} & \omega_{p4} &= \frac{g_{o3}}{C_{p3}} \\
\omega_{z5} &= \frac{1}{R_z C_{pz}} & \omega_{p5} &= \frac{1}{R_z C_{pz}}
\end{aligned}
\tag{3.4}
$$

From the detailed transfer function in factored form, we obtain a simplified transfer function by observing that $\omega_{z(3-5)} = \omega_{p(3-5)}$ resulting in pole zero cancellation at very

high frequency, outside the band of interest. It can be noted that imperfections in the pole-zero cancellation does not affect system performance as they are way outside the band of interest. Also the non-minimum phase zero (RHP) ω_{z2} is at high enough frequency and hence ignored in the simplified transfer function given in Equation 3.5 with the terms having similar definitions as that of the detailed transfer function in factored form given in Equation 3.4

$$H(s) = \frac{A_{dc}(1 + \frac{1}{\omega_{z1}}s)}{(1 + \frac{1}{\omega_{3dB}}s)(1 + \frac{1}{\omega_o Q}s + \frac{1}{\omega_o^2}s^2)} \tag{3.5}$$

From the simplified transfer function Equation 3.5, it can be seen that the somewhat complex transfer function reduces to a simple form which enhances circuit analysis and performance tracking.

The phase margin of the proposed system is given in Equation 3.6. Improvement in the phase performance by ω_{z1} can clearly be seen is this equation.

$$\begin{aligned} PM =& 180^\circ - arctan\left(\frac{GBW}{w_{3dB}}\right) - arctan\left[\frac{\frac{GBW}{w_o}}{Q\left[1 - \left(\frac{GBW}{w_o}\right)^2\right]}\right] + arctan\left(\frac{GBW}{w_{z1}}\right) \\ =& 90^\circ - arctan\left[\frac{\frac{GBW}{w_o}}{Q\left[1 - \left(\frac{GBW}{w_o}\right)^2\right]}\right] + arctan\left(\frac{GBW}{\omega_{z1}}\right) \end{aligned} \tag{3.6}$$

Similarly, GBW of the proposed design is given by Equation 3.7 which follows the general GBW of multistage amplifiers.

$$GBW = A_{dc} \times \omega_{3dB} \approx \frac{g_{m1}}{C_m} \tag{3.7}$$

3.3 Circuit Performance

The circuit performance can be broadly placed under two groups, namely small signal performance and large signal performance.

3.3.1 Small Signal Performance

The small signal performance is mainly characterized by the GBW and the stability margins, PM and GM of the system. The simplified transfer function was obtained under small signal conditions. The DC gain given by A_{dc} in Equation 3.4 shows that the gain term is contributed by an additional transconductance g_{m4} which increases the gain in comparison to the other 3 stage counterpart [3]. Also for the same DC gain, the additional gm stage reduces the individual gm's required in the 3 stages OTA which effectively reduces the current consumption assuming the same overdrive in both cases.

From Equation 3.6, the effect of the active zero can clearly be seen. The design steps start by setting the GBW given in Equation 3.7 and placing $\omega_o > GBW$. According to Equation 3.4, ω_o depends on g_{ma}, g_{mb}, g_{m3} and g_{m4} which can be optimized to place ω_o for a given power and a particular capacitive load, C_L and PM. Also the ω_{z1} is placed in the vicinity of ω_o so as to reduce the phase degradation by the complex pole. C_z should be set so as to not push ω_o to close to GBW and at the same time sized well to create zero to prevent the phase degradation. The flexibility in placing the zero is then achieved through R_z which may affect the noise performance and also the range of load drive.

3.3.2 Large Signal Performance

The main large signal specification is slew rate which is defined as the maximum rate of change of the output voltage with respect to time. As said earlier, g_{mf} is implemented optionally to help in the large signal performance of the OTA and hence has little or no influence on the small signal performance. g_{mf} forms a push-pull with the main input

transistor of the fourth stage, g_{m4}, mimicking a class AB effect. The slew rate (SR) is given by Equation 3.8 which, due to the class AB effect provided by g_{mf}, is limited by C_m for low enough capacitive load. However for capacitive loads in the nF-range, the SR is mostly limited by C_L and hence the output stage.

$$SR \approx min\left(\frac{I_1}{C_m}, \frac{I_4}{C_L}\right) \tag{3.8}$$

The simplest way to improve SR is to increase the output load current. This however increases the power consumption of the proposed design, hence a slew helper was implemented to improve the SR performance of the system. This is will elaborated in a later section (Section 3.5).

3.4 Design Procedure

Local feedback loop analysis (explained in Appendix C) is applied to the proposed design and loop transfer function is given in Equation 3.9 and it magnitude plot is shown in Figure 3.2. From the LFL of the proposed design, there is control over how $omega_\mu$, ω_{z1} and the limiting pole ω_3 are placed, hence its effective in its ability to drive wide range as explained in Appendix C.

$$T_{LFL} = -\frac{g_{ma}g_{mb}g_{m3}g_{m4}}{g_{mz}g_{o1}g_{ob}g_{o3}g_{o4}} \frac{sC_m(1+\frac{s}{\omega_{z1}})}{(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_2})(1+\frac{s}{\omega_3})(1+\frac{s}{\omega_4})(1+\frac{s}{\omega_5})(1+\frac{s}{\omega_6})} \tag{3.9}$$

$$\begin{aligned}
\omega_1 &= \frac{g_{o4}}{C_L} & \omega_2 &= \frac{g_{o1}}{C_m} & \omega_3 &= \frac{g_{mz}}{C_z} \\
\omega_4 &= \frac{g_{ob}}{C_{pb}} & \omega_5 &= \frac{g_{o3}}{C_{p3}} & \omega_6 &= \frac{1}{R_z C_{pz}} \\
LG &= \frac{g_{ma}g_{mb}g_{m3}gm4}{g_{mz}g_{o1}g_{ob}g_{o3}}\frac{C_m}{C_L} & \omega_\mu &= \frac{g_{ma}g_{mb}g_{m3}g_{m4}}{g_{mz}g_{o1}g_{ob}g_{o3}}\frac{C_m}{C_L} & \omega_{z1} &= \frac{1}{R_z C_z}
\end{aligned} \tag{3.10}$$

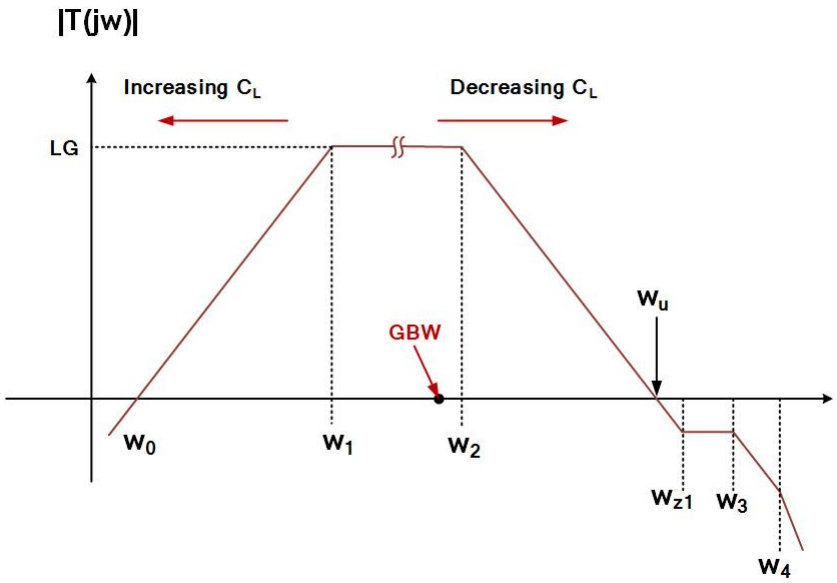

Figure 3.2: LFL magnitude response of proposed design

From the simplified transfer function Equation 3.5, the LFL transfer function Equation 3.9, the equations for PM (Equation 3.6) and GBW (Equation 3.7), the design procedure is given below. Note that this procedure is done with the assumption that the GBW, power consumption, noise level and other important circuit are known priori.

- Determine g_{m1} to satisfy noise requirement and random offset
- From the particular GBW and g_{m1}, C_m is determined
- Ensure that $\omega_\mu > GBW$ at large loads and also $\omega_\mu < \omega_3$ at low loads
- For a good phase margin, say $> 45^\circ$, place $\omega_o >$ GBW. ω_o are placed at $2\times$ GBW for PM=45°
- $\omega_{z1} >$ GBW to ensure single pole characteristics in band of interest. ω_{z1} can ideally

be used to cancel the limiting pole of LFL which will help extend ω_μ. However, this will results in a minimal PM improvement by LHP zero ω_{z1} in amplifier's response

- To save area and also help with LFL's PM at low load, $\omega_{z1} \approx 3\times$ GBW and placed before ω_3 of LFL shown in Figure 3.2 (ie $\omega_{z1} \approx$ GBW $< \omega_3$)
- Choosing $R_z > 1/g_{mz}$ ensures placing ω_{z1} of the LFL before LFL's ω_3 hence improving PM in the LFL at low loads
- From Equation 3.4 $\omega_o \propto \frac{1}{\sqrt{C_L}}$ hence the above condition can be achieved with low power for low loads
- The design is optimized for the largest load
- The 4th-stage provide extra degree of freedom and hence low gm can be used saving power and area.
- ω_o has an extra g_m which means it is easier to situate it where you want in this case $2\times$GBW with less power

3.5 Circuit Implementation

The circuit implementation is shown in Figure 3.3 and is implemented in IBM 130nm CMOS process. The first stage is implemented with $M_{100-108}$ where M_{100} is the biasing transistor. $M_{201-204}$ implements the second stage with the active zero generation block, composed of R_z, C_z and g_{mz}, embedded in the second stage to save power. g_{mz} is implemented with M_{202}, g_{ma} and g_{mb} with M_{201} and M_{204} respectively. The third stage is implemented with $M_{301-304}$ and the fourth stage with $M_{401-402}$. The feedforward g_{mf} is implemented with M_{401} and g_{m4} with M_{402}

As stated in Section 3.3, a slew rate helper is needed to improve the slewing performance of amplifier with nF-range loads. A slew helper [36] which has two main parts, the

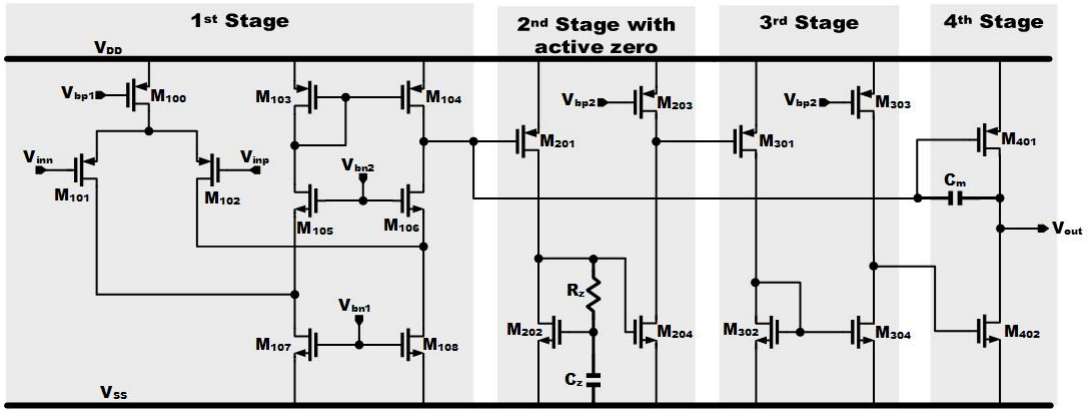

Figure 3.3: Schematics of proposed amplifier core

detection part which detects the on-set of slewing and SR boosting part which is switched on when the circuit starts slewing was implemented. The block diagram illustrating the slew helper is shown in Figure 3.4. It can clearly be seen from this figure that, the slew boosting path and the main signal path do not interrupts each other during normal operation. The detection block turns one of the two switches on, to either pump current into the output capacitor or sink current from the output capacitor. This results in a faster charging or discharging of the capacitor and hence improvement in slew rate. From Figure 3.5, M_{501} and M_{502} serve as the detection part and are connected to the input of the main amplifier core. M_{503} and M_{504} act as current source loads to the input M_{501} and M_{502} and are sized to carry more current than the input pair (i.e. $I_{D(503,504)} > I_{D(501,502)}$). This condition ensures that the drain voltage of M_{503} and M_{504}, $V_{D(503)}$ and $V_{D(504)}$ respectively, are low enough to bias M_{507} and M_{508} which serve as the switch of the SR boosting stage in cut-off at nominal operation. M_{505} and M_{506} mirrors the current from M_{507} to give a symmetric SR boosting independent of whether falling or rising edge of the input is slewing.

At the nominal circuit operation, $V_{D(503)}$ and $V_{D(504)}$ are low, biasing the switches, M_{507} and M_{508}, in cut-off. Assuming a pulse is applied to the input as shown in Figure 3.6,

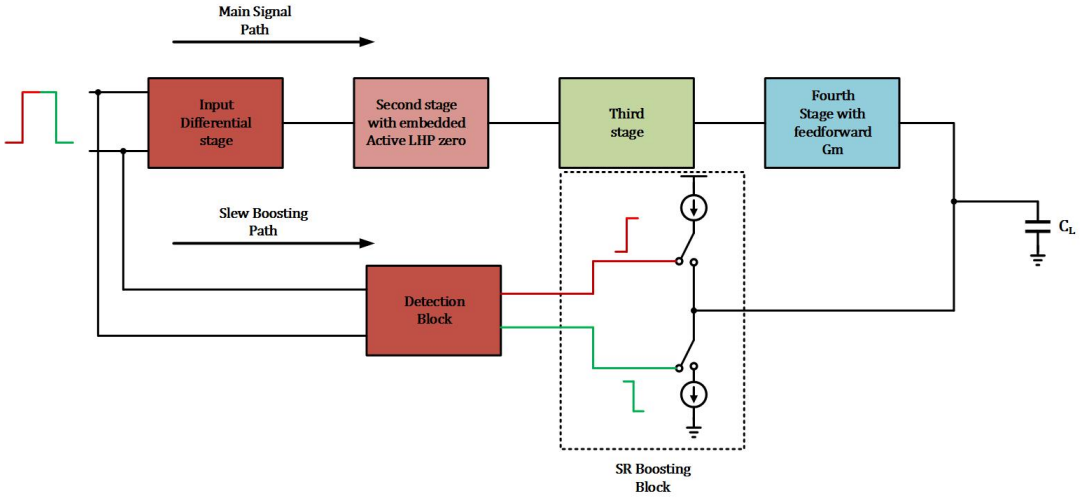

Figure 3.4: Block diagram of slew helper

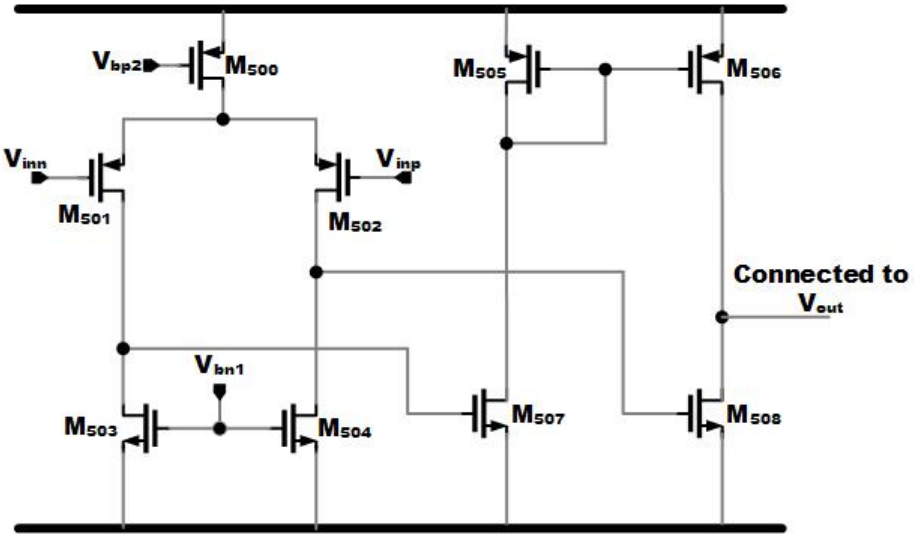

Figure 3.5: Circuit implementation of slew helper

$V_{D(503)}$ goes high turning on M_{507} whiles M_{508} is still off as $V_{D(504)}$ goes down. Through M_{505} and M_{506}, current is injected to the output, charging the output capacitor faster. With a pulse as shown in Figure 3.7 the opposite effect happens. In this case M_{508} is turned on drawing current from the output and hence discharging the output capacitor faster.

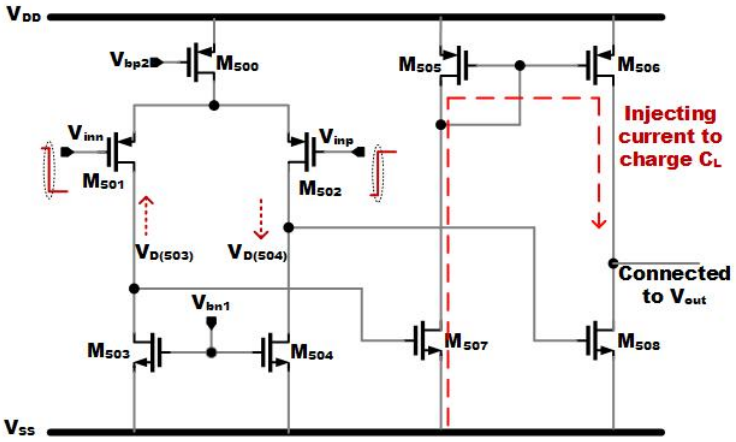

Figure 3.6: Working principle of Slew helper in charging C_L

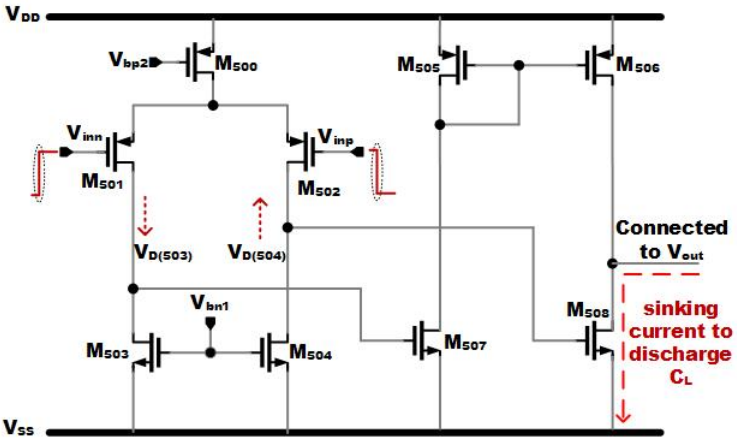

Figure 3.7: Working principle of Slew helper in discharging C_L

This slew helper has minimal power overhead and does not affect the small signal performance of the OTA. This improves large signal performance of the system with minimal or no added current consumption. Care must be taking in deciding on how large $I_{D(503,504)}$ should be in comparison to $I_{D(501,502)}$ since this affects the voltage step that turns on the switches and hence the SR boosting stage.

Following the design procedure in Section 3.4 and using the schematic shown in Figure 3.3, the parameters and transistor sizes are respectively shown in Table 3.1 and Table 3.2.

Parameter	**Value**	**Parameter**	**Value**
g_{m1} (μS)	32.3	g_{m4} (μS)	570.8
g_{ma} (μS)	103.3	g_{mf} (μS)	796.2
g_{mb} (μS)	117.2	C_m (pF)	2.3
g_{mz} (μS)	102.7	C_z (pF)	0.8
g_{m3} (μS)	201.3	R_z (kΩ)	30

Table 3.1: Parameter values

Transistor	**W/L (μm/ μm)**	IF	**Transistor**	**W/L (μm/ μm)**	IF
$M_{101,102}$	4(0.45/0.35)	7	M_{203}	8(0.76/0.4)	9.8
$M_{103,104}$	2(0.81/0.8)	11	M_{301}	12(0.8/0.5)	12.8
$M_{105,106}$	2(0.8/0.7)	1.5	$M_{302,304}$	4(0.5/0.4)	9
$M_{107,108}$	2(1.07/0.8)	2.8	M_{303}	14(0.76/0.4)	10
M_{201}	10(0.6/0.5)	9.7	M_{401}	32(1.44/0.5)	10
$M_{202,204}$	2(0.45/0.4)	10	M_{402}	4(0.5/0.2)	24.5
M_{100} (bias)	8(1.62/1)	5.6			

Table 3.2: Transistor sizing

This design is laid out using IBM 130nm CMOS PDK. The amplifier core alone with-

out slew helper and one with slew helper is laid out. Good layout techniques including common centroid, inter-digitization, guard ringing etc were used ensuring low mismatch effects and reduction in deterministic errors. The layout of both OTA individually and on a padframe is shown in Appendix D.

3.6 Simulation Results

To check both small and large signal performances of the OTA, the following simulations were carried using Virtuoso Analog Design Environment with Spectre as the simulator. For small signal performance which is mainly the measurement of stability margins, DC Gain and GBW, stb analysis was performed. The large signal performance was done using transient response and the slew rate was measured. DC simulation was performed to measure the power consumption of the OTA.

3.6.1 Small Signal Performance

Post layout simulation results obtained from stb analysis performed on the proposed design are given below for 400pF and 12nF loads. Simulation for 15nF is also added to see how the proposed design works at that load (so as to compare with literature).

Figure 3.8 shows the frequency response of the proposed design under 400pF capacitive loading condition. The zero of the active zero generation block can clearly be seen in this response. With $C_L = 400pF$, ω_o is pushed to a higher frequency than the zero hence the zero flattens the $-20dB/dec$ slope before the ω_o kicks in, resulting in $-40dB/dec$ after ω_o. The measured stability margins under this condition is $PM = 86.9^\circ$ and $GM = 15.4dB$, with $GBW = 2.12MHz$.

Under 12 nF loading condition shown in Figure 3.9 the proposed design shows a well-behaved system with stability margins of $PM = 46.9^\circ$ and $GM = 13dB$. The ω_o is within 10 decades of the GBW designed for, (which is 2MHz) hence reducing the GBW to $1.77MHz$

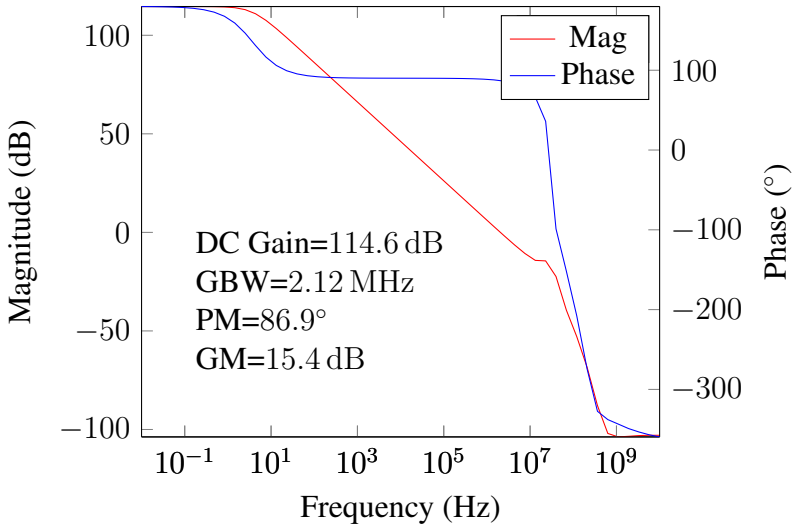

Figure 3.8: Frequency response of proposed design @ 400pF capacitive load

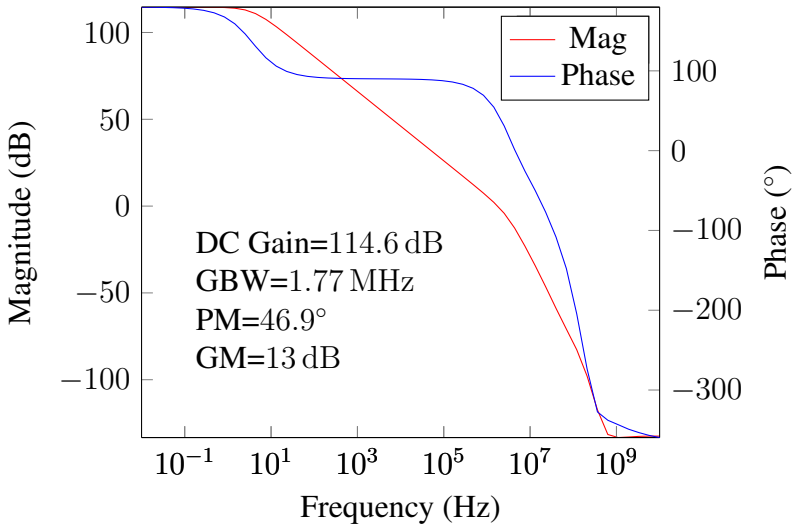

Figure 3.9: Frequency response of proposed design @ 12nF capacitive load

Though the proposed OTA was not design for a capacitive load of 15nF, it can be seen from Figure 3.10 that the system produce acceptable response giving PM and GBW of 42.2° and 1.66 MHz respectively (See Table 3.3). The small signal performance under the different load conditions are tabulated in Table 3.3.

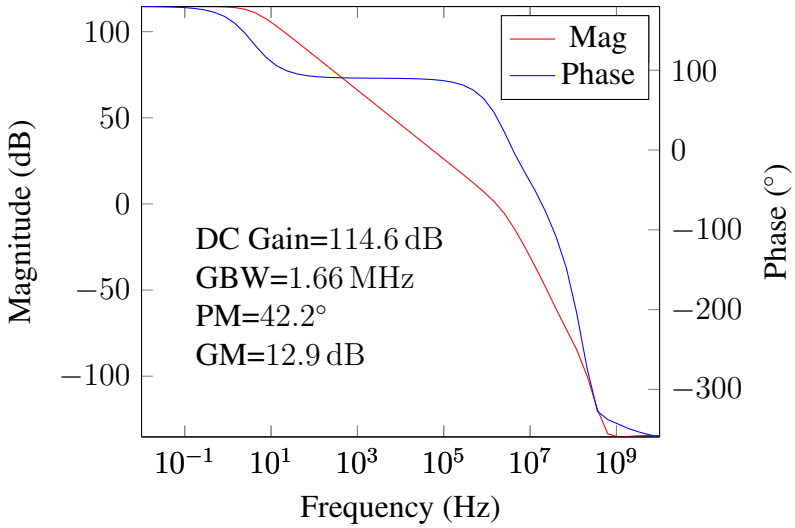

Figure 3.10: Frequency response of proposed design @ 15nF capacitive load

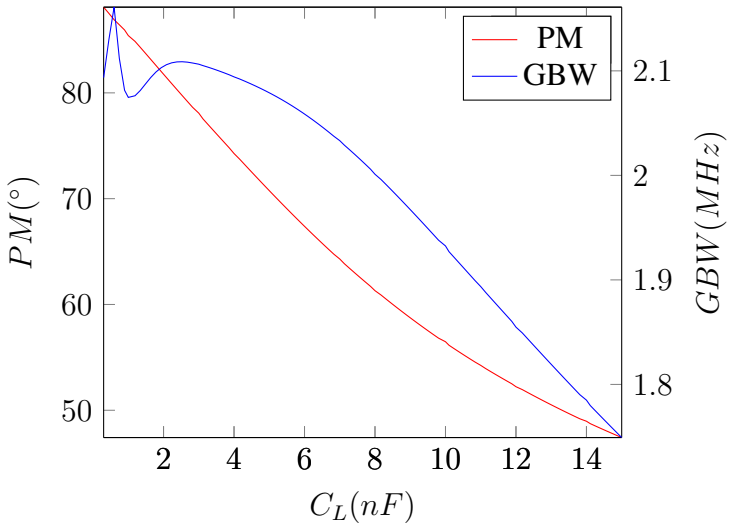

Figure 3.11: PM and GBW variation with load capacitance

3.6.2 Large Signal Performance

The transient response under 400pF, 12nF and 15nF loading conditions are given below. From Figure 3.13 and 3.14, the improvement by the slew helper can clearly be seen.

	400pF	12nF	15nF
DC Gain (dB)	114.6	114.6	114.6
I_{DD} (μA)	119.6	119.6	119.6
GM (dB)	15.4	13	12.86
GBW (MHz)	2.12	1.77	1.66
PM (^{o})	86.9	46.9	42.2
SR(V/μs)	2.66	0.19	0.17

Table 3.3: Post-layout simulation summary

Aside the reduction of the overshoot, the slew helper's effect is not very obvious in the 400pF loading condition. Unlike other enhancement schemes, this slew helper depends on the input signal themselves to detect slewing and not internal nodes like those in [27]. Also the scheme did not affect small signal response and it worked well across corners evident in Table 3.5 and Appendix E.

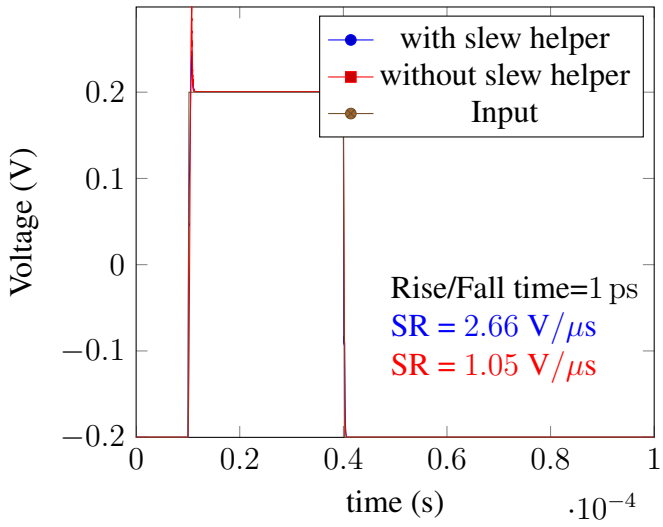

Figure 3.12: Transient response of proposed design @ 400pF load

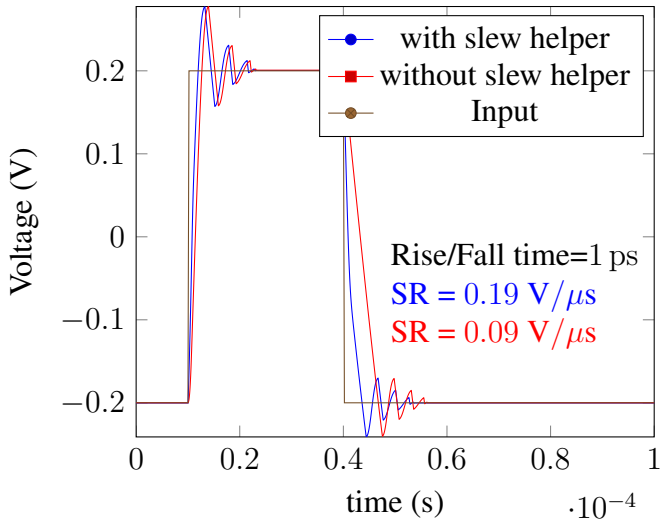

Figure 3.13: Transient response of proposed design @ 12nF load

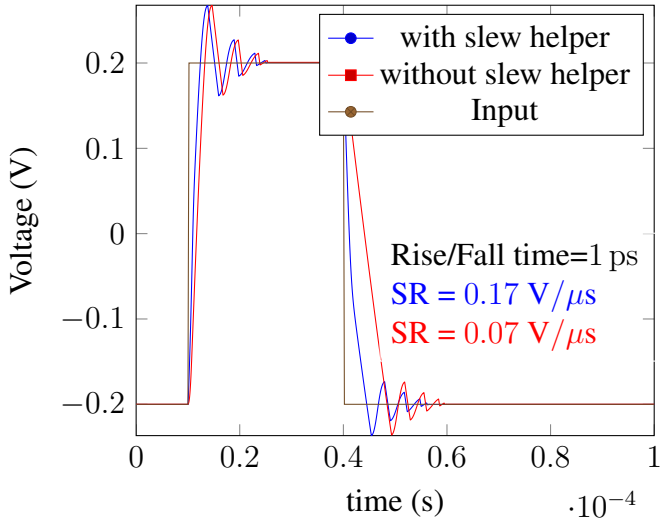

Figure 3.14: Transient response of proposed design @ 15nF load

3.6.3 Monte Carlo and Corner simulation

The summary of Monte Carlo and Corner simulation (details of various simulations are shown in Appendix E).

	Mean	**SD**	Min @ 3σ
DC Gain (dB)	113.56	1.38	109.42
I_{DD} (μA)	125.3	13.43	85.01
GM (dB)	14.83	1.25	11.08
GBW (MHz)	1.85	0.045	1.72
PM (^{o})	52.5	2.43	45.21

Table 3.4: Monte carlo simulation @ 12nF load, N=100

From Table 3.4, the minimum performance parameters @ 3σ suggest that at least 99.7% of the yield will have this minimum parameters. This means that mismatches do not affect the design much if good layout techniques are used. Variation of performance

	TT	**FF**	**SS**	**FS**	**SF**
DC Gain (dB)	113.6	113.4	113.4	112.8	114
I_{DD} (μA)	123.4	129.6	118.4	123.1	123.6
GM (dB)	14.76	16.79	12.95	16.15	13.33
GBW (MHz)	1.86	1.94	1.75	1.75	1.94
PM (^{o})	52.3	54.4	49.7	54.2	49.4

Table 3.5: Corner simulation for 12nF load @ 27^oC

due to process has been done on the proposed design. From Table 3.5, DC gain records worst perform of 112.8 dB under FS corner, worst GM and GBW were recorded as 12.95 dB and 1.75 MHz respectively under SS corner and worst PM of 49.4 $^\circ$ under SF corner. Even under these corners the proposed design has comparable performances as existing strategies in literature.

3.6.4 Table of Comparison

The performance of the proposed OTA was compared with both 3 stage OTAs (Table 3.6) and 4 stage OTAs (Table 3.7) in literature. The proposed designed has admirable performance in comparison to existing solution.

Specifications	**Ref [22]**	**Ref [18]**	**Ref [37]**	**Ref [25]**	**Ref [3]**	**This work (no helper)**	**This work (with helper)**
Tech (μm)	0.5	0.35	0.35	0.35	0.35	**0.13**	**0.13**
C_L(pF)	120	150	500	150	15000	**12000**	**12000**
Power (mW)	0.42	0.045	0.225	0.03	0.144	**0.146**	**0.144**
I_{DD} (mA)	0.21	0.03	0.15	0.02	0.072	**0.12**	**0.12**
V_{DD}(V)	2	1.5	1.5	1.5	2	**1.2**	**1.2**
GBW(MHz)	9	2.85	1.4	4.4	0.95	**1.97**	**1.77**
SR(V/μs)@ **1nF/12nF**	0.51	1.04	2	1.8	0.22	**0.98/0.09**	**1.18/0.19**
$FOM_S = \frac{GBW \times C_L}{Power}$	2567	9500	3111	22000	98958	**161343**	**147993**
$FOM_L = \frac{SR \times C_L}{Power}$	972	3450	4445	9000	22917	**7371**	**15636**
$IFOM_S = \frac{GBW \times C_L}{I_{DD}}$	5134	14250	4667	33000	197916	**193612**	**177591**
$IFOM_L = \frac{SR \times C_L}{I_{DD}}$	1943	5175	6667	13500	45834	**8845**	**19064**
Area (mm^2)	0.015	$<$0.02	0.075	$<$0.02	0.016	**0.006**	**0.007**
C_{Total}(pF)	4	2.02	50	1.6	2.6	**3.1**	**3.1**
Capacitive Load Range	1x	1x	1x	1x	15x	**30x**	**30x**

Table 3.6: Performance comparison with 3 stage OTAs

Specifications	**Ref [38]**	**Ref [39]**	**Ref [17]**	**Ref [32]**	**Ref [10]**	**This Work (no helper)**	**This Work (with helper)**
Tech(μm)	1.5	0.8	2	0.12	0.35	**0.13**	**0.13**
C_L(pF)	250	10	20	500	1000	**12000**	**12000**
Power (mW)	10	4.5	0.68	1.4	0.156	**0.146**	**0.144**
I_{DD} (mA)	2	0.3	0.34	1.4	0.052	**0.12**	**0.12**
V_{DD}(V)	5	1.5	2	1	3	**1.2**	**1.2**
GBW(MHz)	2	6	0.61	40.2	2.98	**1.97**	**1.77**
SR(V/μs)@ **1nF/12nF**	1.5	13	2.5	17.52	1.18	**0.98/0.09**	**1.18/0.19**
$FOM_S = \frac{GBW \times C_L}{Power}$	50	133	18	14357	19103	**161343**	**147993**
$FOM_L = \frac{SR \times C_L}{Power}$	38	289	74	6257	7564	**7371**	**15636**
$IFOM_S = \frac{GBW \times C_L}{I_{DD}}$	250	200	36	14357	57308	**193612**	**177591**
$IFOM_L = \frac{SR \times C_L}{I_{DD}}$	188	433	147	6257	22692	**8845**	**19064**
Area (mm^2)	0.625	0.05	0.22	0.017	0.014	**0.006**	**0.007**
C_{Total}(pF)	34.5	4.9	–	17.6	9.7	**3.1**	**3.1**
Capacitive Load Range	1x	1x	1x	1x	1x	**30x**	**30x**

Table 3.7: Performance comparison with 4 stage OTAs

4. DESIGN TRADE-OFF

Analog Circuit design has a lot of specifications which are dependent and most times trade off among themselves. According to [2], the author refers to these interdependencies as "analog design octagon" as shown in Figure 4.1. From Figure 4.1, we identify these performance specifications as power dissipation, noise, linearity, gain, supply voltage, voltage swings, speed and input/output impedance. I will hasten to add that, area can be added to these interdependencies.

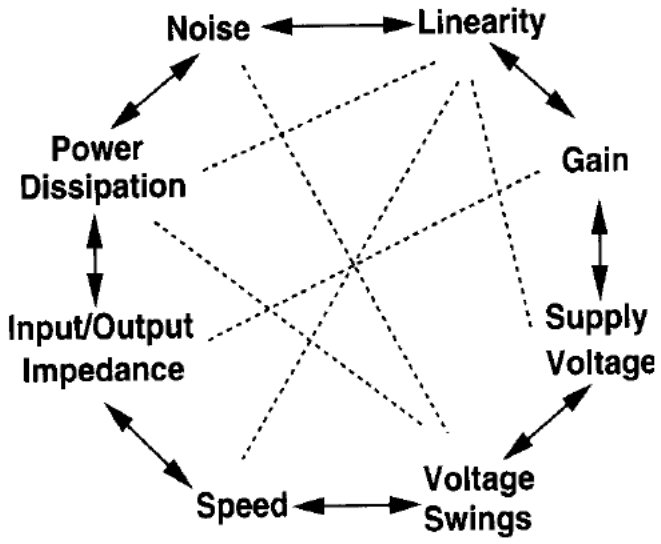

Figure 4.1: Analog design octagon
Reprinted from [2]

To illustrate this trade off, consider a simple common source amplifier shown in Figure 4.2 (a). The gain is given by $V_{out}/V_{in} = g_m R_D$ ignoring all second order effect. As can be seen the input-output characteristics varies with input current level affecting the

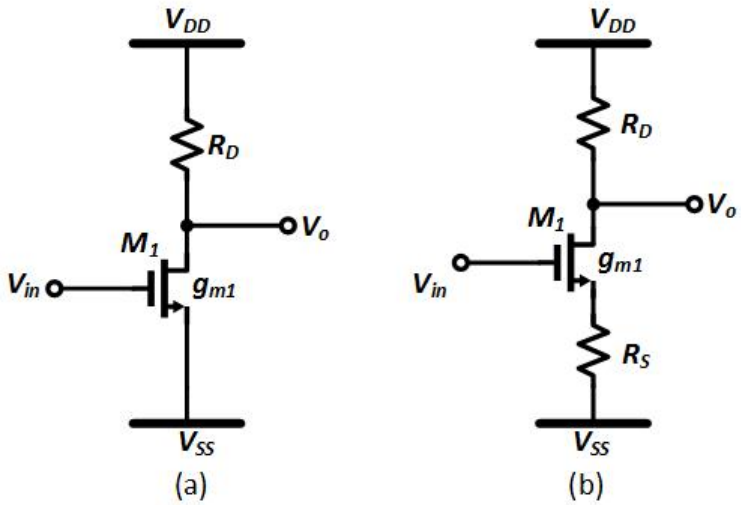

Figure 4.2: (a) Common source amplifier (b) Common source amplifier with resistive degeneration

amplifier linearity. In a quest to improve linearity, resistive degeneration is used as shown in Figure 4.2 (b) with R_s which introduce thermal noise. Also the new gain is reduced to $\approx R_D/R_s$ with this approximation valid for $gmR_s \gg 1$ which requires more power dissipation. From the above illustration, the various performance specifications are interrelated and analog design, as the author of [2] puts it, involves a multidimensional optimization process.

In the sections that follows, the input pair width is varied and the effects on various system performances are observed.

4.1 Linearity

The measure of linearity is mostly done through the use of Total Harmonic Distortion (THD).Linearity is the measure of variation of the small signal gain as the input level changes.A transient response is run and a dft is performed to measure thd (see Figure 4.3 and 4.4)

These responses are obtained for a closed loop system with input amplitude of 300mV

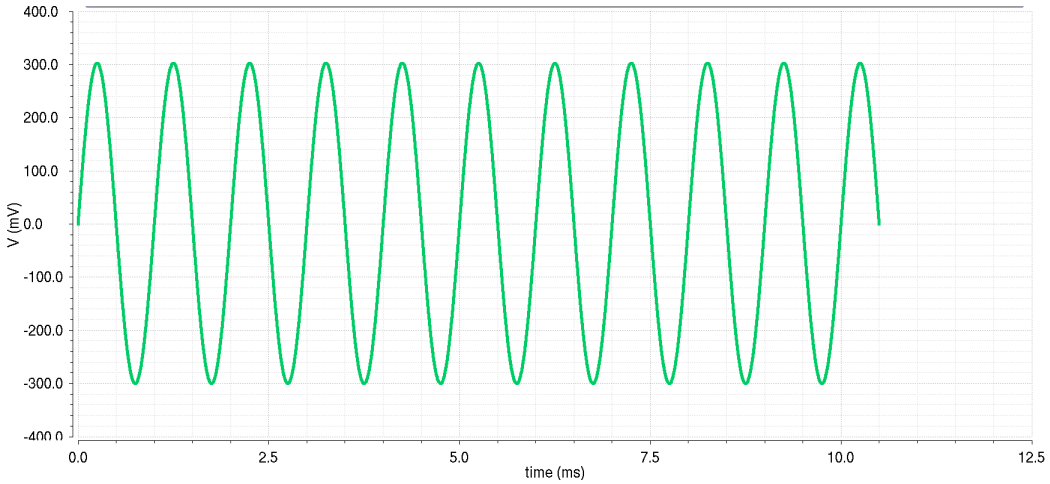

Figure 4.3: Closed loop transient response with 300mV amplitude

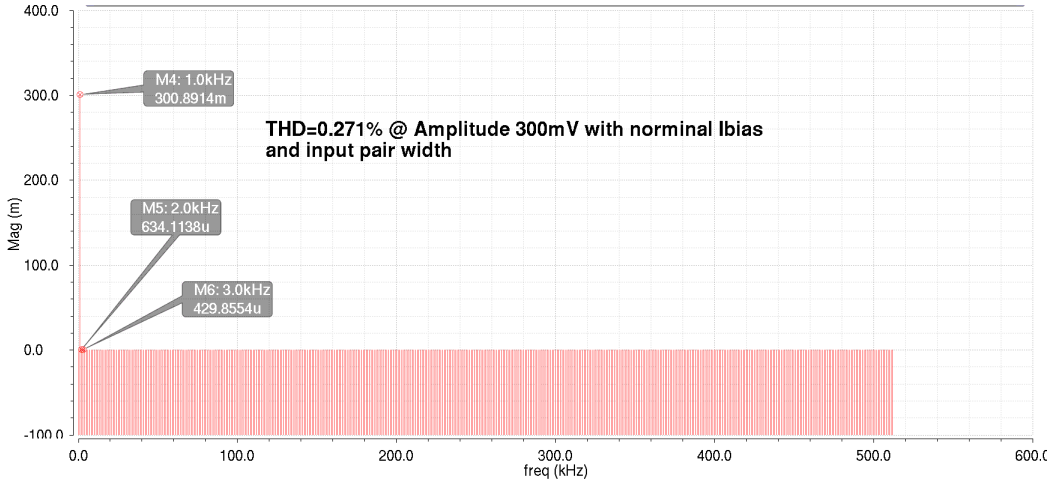

Figure 4.4: DFT performed on the transient response

and a THD of 0.27% is obtained. THD deteriorates as the input amplitude increases and this is illustrated in Figure 4.5. The input amplitude, V_{amp} to obtained 1% THD is 368 mV as shown in Figure 4.5

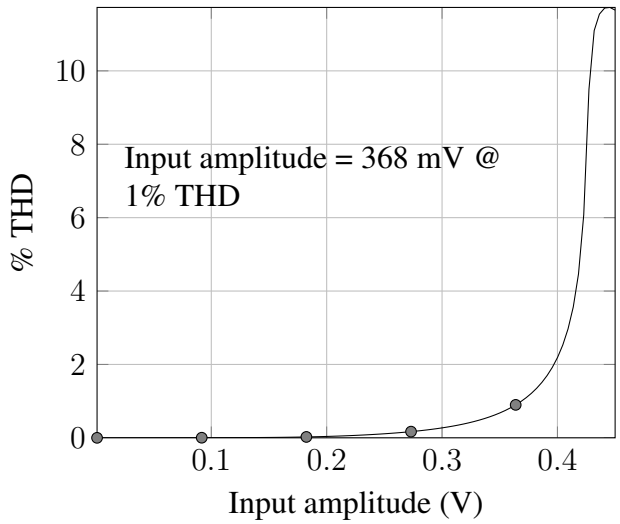

Figure 4.5: Variation of THD with input signal amplitude in unity feedback

The input pair width limits the linearity performance of the system [2]. The linearity is shown to improve for increasing input pair width while maintaining the bias current I_{bias} constant at $4\mu A$. Increasing the input pair with results in increased g_m from Equation 4.2 hence increasing the loop gain. The observed trend off reduction in % THD (improvement in linearity) is mainly due to the increased loop gain of the unity feedback configuration. The linearizing effect of negative feedback (unity feedback) increase for increasing input

pair width as observed in Figure 4.6 with the $I_{bias} = 4\mu A$ $V_{amp} = 300mV$.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{ov})^2 \tag{4.1}$$

$$g_m = \frac{2I_D}{V_{ov}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov} \tag{4.2}$$

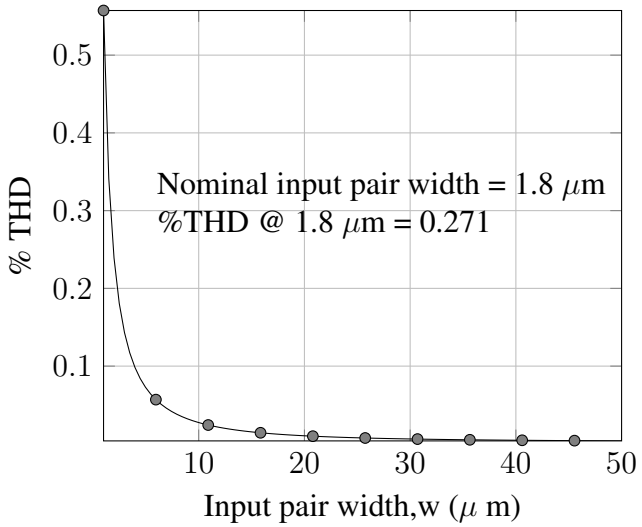

Figure 4.6: Variation of THD with input pair width. Constants : $I_{bias} = 4\mu A$, $V_{amp} = 300mV$

As can be seen, the %THD at input pair width $w = 25\mu m$, is 7.82m compared to the %THD @ nominal input pair width ($w = 1.8\mu m$) = 271m. Figure 4.6 shows that the THD decreases, hence linearity becomes better, as the input pair width increases.

4.2 Noise

There are 5 noise sources according to [40] namely Shot noise, Thermal noise, Flicker noise, Burst (pop-corn) noise and Avalanche noise. The main noise source for MOSFET and hence considered here for the proposed OTA are thermal noise and flicker noise.

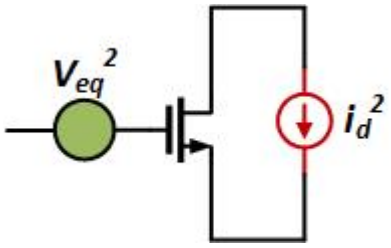

Figure 4.7: Noise source of transistor

Consider a single transistor shown in Figure 4.7, i_d^2 is current noise spectral density and v_{eq}^2 input referred voltage noise spectral density. i_d^2 has two main component, that due to flicker noise $i_{d,fn}^2$ and that due to thermal noise $i_{d,tn}^2$. Similarly v_{eq}^2 is composed of $v_{eq,fn}^2$ and $v_{eq,tn}^2$. Current noise is the real noise source, however to ensure easy system analysis current noise sources are input referred as voltage noise sources. Assuming the transistor is in saturation, the following thermal and flicker noise densities are obtained.

$$i_{d,fn}^2 = \frac{K_F g_m^2}{WLC_{ox}f} \tag{4.3}$$

$$i_{d,tn}^2 = \frac{8kTg_m}{3} \tag{4.4}$$

$$i_d^2 = i_{d,fn}^2 + i_{d,tn}^2 = \frac{K_F g_m^2}{WLC_{ox}f} + \frac{8kTg_m}{3} \tag{4.5}$$

$$v_{eq,fn}^2 = \frac{i_{d,fn}^2}{g_m^2} = \frac{K_F}{C_{ox}}\left(\frac{1}{WL}\right)\left(\frac{1}{f}\right) \tag{4.6}$$

$$v_{eq,tn}^2 = \frac{i_{d,tn}^2}{g_m^2} = \frac{8kT}{3g_m} \tag{4.7}$$

$$v_{eq}^2 = v_{eq,tn}^2 + v_{eq,fn}^2 = \frac{8kT}{3g_m} + \frac{K_F}{C_{ox}}\left(\frac{1}{WL}\right)\left(\frac{1}{f}\right) \tag{4.8}$$

where k is Boltzmann constant, T is absolute temperature in Kelvin, C_{ox} is capacitance per unit gate area of the oxide layer and K_F is the proportionality constant and is device dependent. The noise level is obtained by integrating the spectral density over frequency of interest.

Noise analysis of amplifier involves adding the individual noise source of various transistors and referring it to input as either input referred voltage or current noise. As the number of stages becomes greater in our quest to increase DC Gain or other parameters, the number of transistors and hence noise sources increases. However, according to [41], the thermal noise level of an amplifier is a product of two terms, noise of input differential pair and noise factor which is the contribution from other transistors. Using this approach the noise level of the proposed OTA can be approximated by Equation 4.9

$$V_{noise} \approx \left(\sqrt{\frac{8kT}{g_{m1}}(BW)}\right)\left(\sqrt{1+\frac{g_{m2}}{g_{m1}}+\frac{g_{m3}}{g_{m1}A_{v2}^2}+\frac{g_{m4}}{g_{m1}A_{v3}^2A_{v2}^2}}\right) + \sqrt{6kTR_z\frac{g_{mz}^2}{g_{ma}^2A_{v1}}(BW)} \tag{4.9}$$

where

$$\begin{aligned} A_{v1} &= \frac{g_{m1}}{g_{o1}} \\ A_{v2} &= \frac{g_{ma}g_{mb}}{g_{mz}g_{ob}} \\ A_{v3} &= \frac{g_{m3}}{g_{o3}} \end{aligned} \tag{4.10}$$

Also BW is the signal bandwidth which relates to the noise bandwidth NBW for single pole system by $NBW = (\pi/2)BW$

From Equations 4.9 and 4.10, it can be seen that increasing the input pair transconductance, g_{m1}, through increasing input pair width for a constant current as shown in Equation 4.2, increases the first stage gain which reduces the noise level. Also from the definition of flicker noise voltage spectral density (Equation 4.6), increasing the width increases the transistor area which reduces the flicker noise. Figure 4.8 shows the noise performance of the system at nominal width and current of 1.8 μm and 4 μA respectively.

The noise performance for increasing input pair width @ 300 kHz and 4.5 MHz is shown in Figures 4.9 and 4.10 respectively. It can be observed that, the noise performance

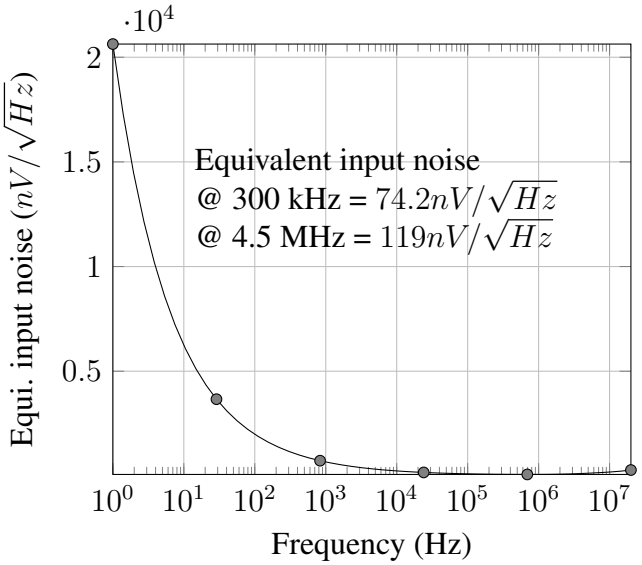

Figure 4.8: Equivalent input referred noise. Constants $I_{bias} = 4\mu A$, $w = 1.8\mu m$

improves at these frequencies of interest (300 kHz and 4.5 MHz) for increasing input pair width. For example, the noise performance for nominal input pair width = 1.8μm @ 300kHz is $74.2nV/\sqrt{Hz}$. This decreased to $52.2nV/\sqrt{Hz}$ at input pair width, w = $25\mu A$.

From the section 4.1 and this section 4.2, it can be seen that both linearity and noise increases for increasing width at the expense of area. Note that, the opposite variation of noise and linearity is mostly due to the linearization technique involving the resistor as illustrated in Figure 4.2

4.3 Stability

To the first approximation, capacitive load does not affect the linearity and noise performance. However, since the g_m of the input pair width increases with w (Equation 4.2), the stability of the proposed OTA should be observed in our quest to increase the linearity and noise performances of the OTA.

At nominal width $w = 1.8\mu m$ and a load of 12nF, $PM = 47.2^\circ$ and $GBW =$

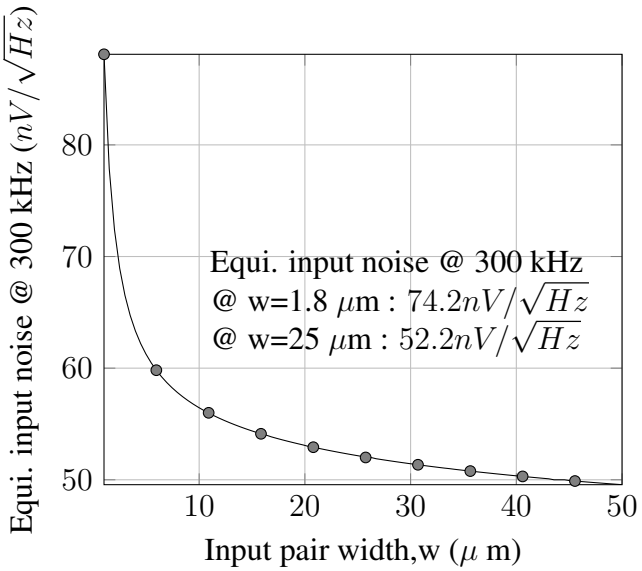

Figure 4.9: Variation equivalent input referred noise @ 300kHz with input pair width. Constant $I_{bias} = 4\mu A$

$1.757MHz$ given a well stabilized system with acceptable transient performance. Figure 4.12 shows that the $PM = 38.4^{\circ}$ and $GBW = 2.55MHz$ @ input pair width, $w = 25\mu m$ which will contain lots of ringing because of PM degradation. Also Figure 4.11 shows that $PM = 85.6^{\circ}$ and $GBW = 3.05MHz$ with a load cap, $C_L = 400pF$ and input pair width $w = 25\mu m$ which is well behaved and has acceptable transient performance.

From the above it can be concluded that, though C_L does not affect the linearity and noise performance of the system, it affects stability and limits the amount of improvement in linearity and noise performance that can be obtained at the large load ends. This effect is minimal or non-observable at low load ends.

4.4 Power Consumption Estimate

The power and area bottleneck is mainly due to the location of complex/real non-dominant poles. For phase margin, PM$> 45^{\circ}$ you want $\omega_o >$ GBW. The transfer function

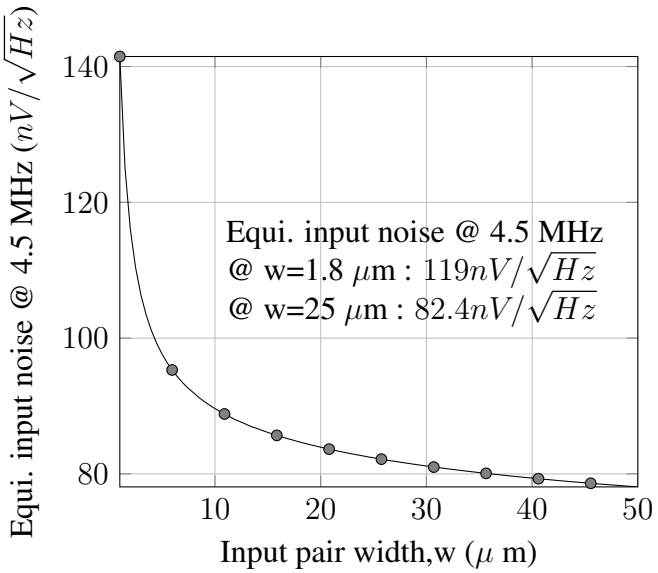

Figure 4.10: Variation equivalent input referred noise @ 4.5MHz with input pair width. Constant $I_{bias} = 4\mu A$

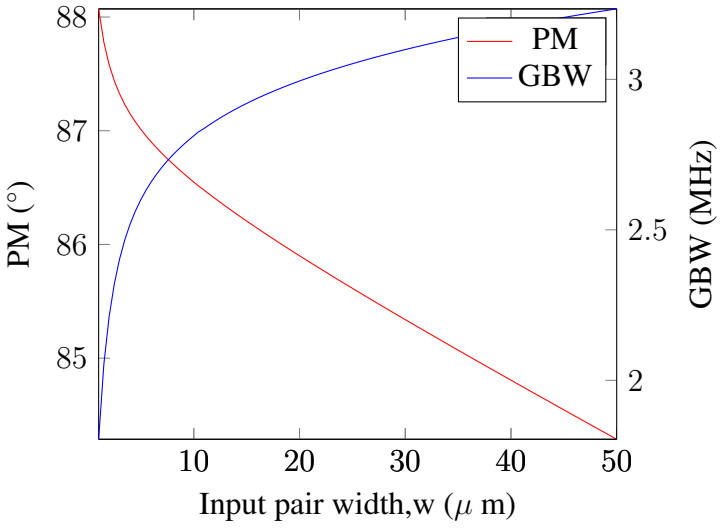

Figure 4.11: Variation of PM and GM with input pair width. Constant:$I_{bias} = 4\mu A$ $C_L = 400pF$

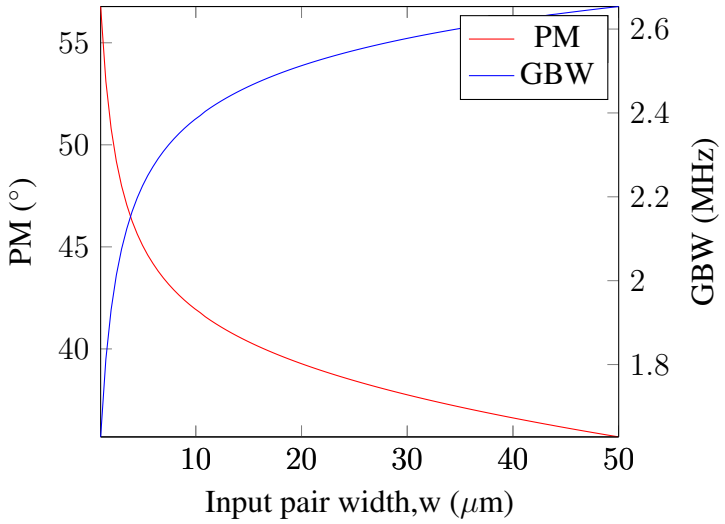

Figure 4.12: Variation of PM and GM with input pair width. Constant:$I_{bias} = 4\mu A$ $C_L = 12nF$

and the various terms are repeated here for continuity.

$$H(s) = \frac{A_{dc}(1 + \frac{1}{\omega_{z1}}s)}{(1 + \frac{1}{\omega_{3dB}}s)(1 + \frac{1}{\omega_o Q}s + \frac{1}{\omega_o^2}s^2)} \tag{4.11}$$

$$A_{dc} = \frac{g_{m1}g_{m3}g_{m4}g_{ma}g_{mb}}{g_{o1}g_{o3}g_{o4}g_{ob}g_{mz}} \tag{4.12}$$

$$\omega_{z1} = \frac{1}{R_z C_z} \tag{4.13}$$

$$\omega_{3dB} = \frac{g_{o1}g_{o3}g_{o4}g_{ob}g_{mz}}{C_m g_{m3}g_{m4}g_{ma}g_{mb}} \tag{4.14}$$

$$\omega_o = \sqrt{\frac{g_{m3}g_{m4}g_{ma}g_{mb}}{C_L C_z g_{o3}g_{ob}}} = \frac{K}{C_L} \tag{4.15}$$

$$Q = R_z C_z \sqrt{\frac{C_L C_z g_{o3}g_{ob}}{g_{m3}g_{m4}g_{ma}g_{mb}}} \tag{4.16}$$

$$GBW = \frac{g_{m1}}{C_m} \tag{4.17}$$

$$PM = 90^o - arctan\left(\frac{\frac{GBW}{w_o}}{Q\left[1 - \left(\frac{GBW}{w_o}\right)^2\right]}\right) + arctan\left(\frac{GBW}{w_{z1}}\right) \tag{4.18}$$

The power consumption for different capacitive load is estimated using the above equations. The steps in arriving at this estimation is enumerated below

- According to Equation 4.15 $\omega_o \propto \frac{1}{\sqrt{C_L}}$, which implies for low loads ω_o becomes bigger.

- For a low capacitive load $C_{L,new} < C_{L,old}$,

$$\frac{\omega_{o,new}^2}{\omega_{o,old}^2} = \frac{K_{new}C_{L,old}}{K_{old}C_{L,new}} = C_r\frac{K_{new}}{K_{old}} \tag{4.19}$$

$$C_r = \frac{C_{L,old}}{C_{L,new}} \tag{4.20}$$

$$K = \frac{g_{m3}g_{m4}g_{ma}g_{mb}}{C_z g_{o3}g_{ob}} \tag{4.21}$$

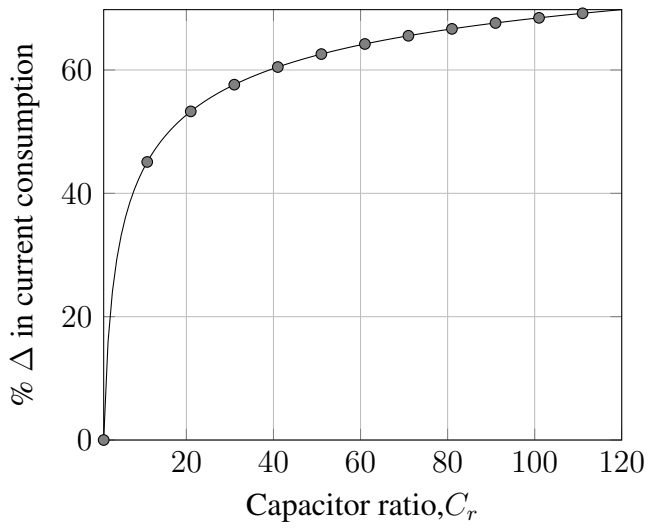

Figure 4.13: Power consumption estimation for different load Constants: V_{ov} and ω_o

Equation 4.19 shows for same ω_o, K_{new} should be reduced by the same amount C_{Lnew} is reduced in comparison with $C_{L,old}$

- Assuming the C_z is not changed, the above condition for K results in the gm's values being reduced by about C_r assuming equal gm reduction
- This means for same V_{ov} the current for implementing g_{m3}, g_{m4}, g_{ma}, and g_{mb} are reduced by about $\frac{1}{\sqrt[4]{C_r}}$ each.
- This results in about $\left(1 - \frac{1}{\sqrt[4]{C_r}}\right)\%$ saving in the total current consumption [1]
- From Figure 4.13, it can be seen that much saving in current consumption can be achieved as the load reduced for a fix ω_o and V_{ov}
- Note that choosing a smaller value of g_{m1} will results in both current and area saving for a particular GBW, however your noise and offset may be high.

[1] This maybe different depending on what you care about and the inversion levels used

- Choosing high g_{m1} for noise offset consideration may require higher C_m for a particular GBW, sacrificing area for noise and offset.

Using the above power estimation, a load of 300pF results in a total current consumption of $40\mu A$ (60% change in current) compared with the $120\mu A$ used in the 12nF case.

5. SUMMARY AND CONCLUSIONS

A four stage OTA with active zero generation block has been proposed. The proposed design has a wide load range ($30\times$) which is the highest in literature. This is achieved with a minimal power and area overhead. The proposed design combines the active zero generation of [3] and the extra transconductance stage to realize a new four stage OTA with admirable system performance. A slew helper discussed in Section 3.5 shows enhanced large signal performance of the proposed design. Chapter 4 considers the various design trade off, which shows power saving as the load capacitor is reduced. Also techniques to improve the various systems parameters like linearity and noise are suggested.

The proposed occupies an active area of $0.007mm^2$ and consumes only $143.5\mu W$ of power. It achieves a DC Gain of 114.6 dB, $GM > 13dB$, $GBW > 1.77MHz$ and $PM > 46.9^{\circ}$. The slew helper ensures a slew rate of $0.19V/\mu s$ @ 12nF load. The proposed design was implemented on 130 nm IBM CMOS process. The table of comparison, Table 3.6 and 3.7, show better enhanced performance of the proposed design in comparison with existing solutions in literature.

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APPENDIX A

RATE OF CLOSURE (ROC)

Rate of closer (ROC) is defined as difference in the slope of |1/β| (feedback factor) and |a| (open loop gain) curves at the crossover frequency. The crossover frequency, f_x in this case is the frequency where |1/β| and |a| curves intersect. ROC is a quick of telling the stability of a system at a glance. This is able to be done by noting the empirical definition of $\angle(T(jf_x))$ in terms of ROC in Equation A.2 and hence the definition of PM in Equation A.3.

$$ROC \text{ (in dB/dec)} = \text{Slope of}\Big|\frac{1}{\beta(jf_x)}\Big| - \text{Slope of}\Big|a(jf_x)\Big| \tag{A.1}$$

$$\angle(T(jf_x)) = -4.5 \times ROC \text{ (in dB/dec)} \tag{A.2}$$

$$PM \text{ (in degrees)} = 180^c irc + \angle(T(jf_x)) = 180 - 4.5 \times ROC \text{ (in dB/dec)} \tag{A.3}$$

From Figure the various ROC's and hence the PM are calculated below.

- $ROC_1(jf_{x1})$=10-(-20)=30 dB, $PM_1 = 180 - 4.5(30) = 45^\circ$
- $ROC_2(jf_{x2})$=0-(-20)=20 dB, $PM_2 = 180 - 4.5(20) = 90^\circ$
- $ROC_3(jf_{x3})$=0-(-40)=40 dB, $PM_3 = 180 - 4.5(40) = 0^\circ$
- $ROC_4(jf_{x4})$=(-20)-(-40)=20 dB, $PM_4 = 180 - 4.5(20) = 90^\circ$

From the definition of PM in Equation A.3 and the examples shown, it can be concluded that ROC< 30 is sufficient for a good PM and acceptable system dynamic performance.

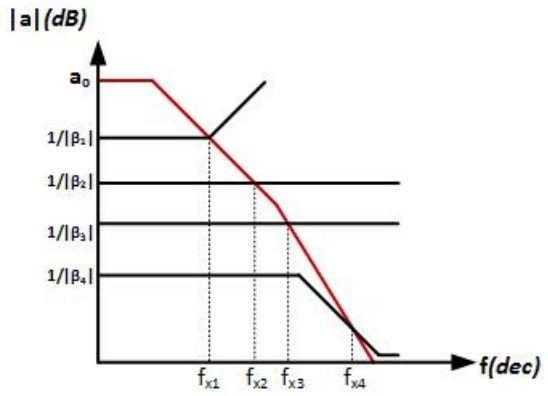

Figure A.1: Magnitude response illustrating ROC.
Reprinted from [1]

APPENDIX B

MILLER EFFECT

A floating impedance Z_F as shown in Figure B.1, can be resolved into two impedances Z_1 and Z_2 according to miller multiplicative effect. The details of this is shown below in Equations

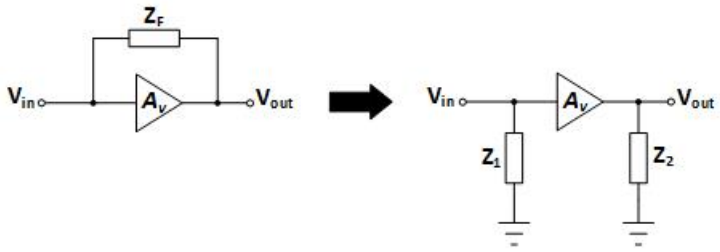

Figure B.1: Miller effect on a float impedance

$$\frac{V_{in} - V_{out}}{Z_F} = \frac{V_{in}}{Z_1} = \frac{-V_{out}}{Z_2} \tag{B.1}$$

$$Z_1 = \frac{V_{in}}{V_{in} - V_{out}} = Z_F \frac{1}{1 - A_v} \tag{B.2}$$

$$Z_2 = -Z_F \frac{V_{out}}{V_{in} - V_{out}} = Z_F \frac{1}{1 - \frac{1}{A_v}} \text{ where } A_v = \frac{V_{out}}{Vin} \tag{B.3}$$

$$\tag{B.4}$$

Assuming a capacitive impedance C_F replaces Z_F, Equation B.2 and B.3 changes accordingly with C_1 and C_2 replacing Z_1 and Z_2 respectively. The new equation of C_1 and C_2 representing the input and output miller capacitance of the floating capacitor C_F is

given below

$$\frac{1}{C_1} = \frac{1}{C_F}\left(\frac{1}{1-A_v}\right) \Rightarrow C_1 = C_F(1-A_v) \tag{B.5}$$

$$\frac{1}{C_2} = \frac{1}{C_F}\left(\frac{1}{1-\frac{1}{A_v}}\right) \Rightarrow C_2 = C_F\left(1-\frac{1}{A_v}\right) \approx C_F \tag{B.6}$$

$$\tag{B.7}$$

It can be seen that the input is miller multiplied by $(1 - A_v)$ termed and the output is approximately C_F

APPENDIX C

LOCAL FEEDBACK LOOP ANALYSIS

Local feedback loop analysis is a concept used by [3] to characterize a compensation strategy's ability to drive wide load range. This concept is based on the reasoning that for an amplifier to be compensated properly, its compensation loop/loops should be active up until the amplifiers unity gain frequency (UGF). Three most important terms in the local loop analysis are local loop gain, LG, local loop's UGF, ω_μ and ω_3 which the pole limiting extension of ω_μ. ω_μ turns out to be non-dominant pole of the amplifier and hence it's extension ensures improvement in PM. Also ω_μ should be greater than amplifier GBW to ensure a good phase margin. A larger ω_μ implies you can get a larger amplifier GBW or trade the GBW for large load drive.

A typical LFL magnitude plot is shown in Figure C.1. It can be observed that as load increases ω_μ decreases, moving towards GBW and hence degrading amplifier's phase margin. Also as the load decreases, ω_μ increases moving towards ω_3 and hence degrading the LFL's PM. This results in peaking the amplifier's frequency response and hence degraded amplifier's gain margin, GM. It can be summarized that

- PM of amplifier limits the highest load an amplifier can drive
- GM of amplifier limits the lowest load an amplifier can drive

From the above discussion it can concluded that, an effective amplifier capable of driving a wide range of load should have control of both ω_μ and the limiting pole ω_4. A table of existing 3 stage amplifiers' ω_μ and limiting pole are giving below.

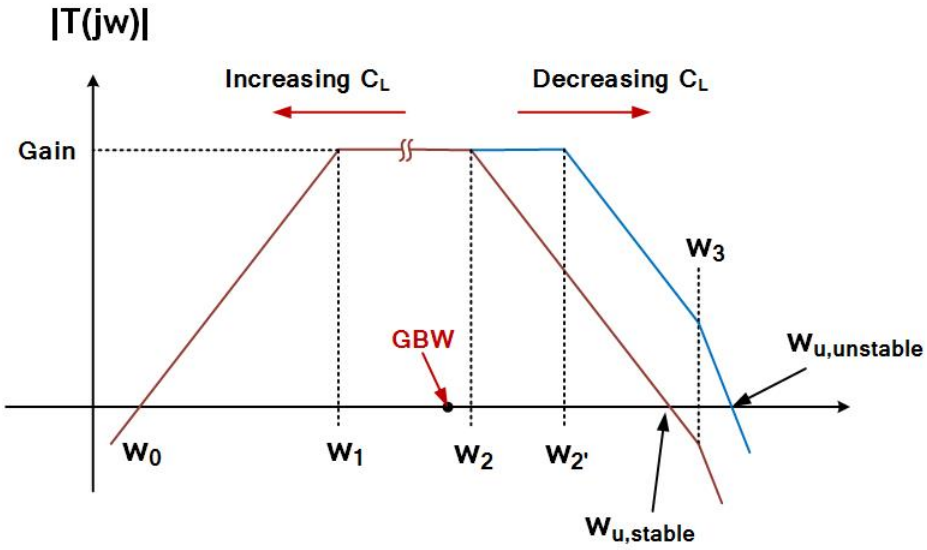

Figure C.1: Typical amplifier's local feedback loop

Topology	$\omega_\mu/(g_{mL}/C_L)$	Limiting Pole
SMC [22]	$\frac{g_{m2}}{g_{o2}}$	$\frac{g_{o2}}{C_L}$
AFFC [30]	$\frac{g_{m2}C_a}{g_{o1}C_m}$	$\frac{g_{o1}}{C_{p1}}$
CFCC [24]	$\frac{g_{m2}C_c}{g_{o1}C_{p1}}$	$\frac{g_{o2}}{C_2}$
DLPC [29]	$\frac{g_{m2}g_{o4}C_a}{g_{m4}g_{o1}C_b}$	$\frac{g_{o1}}{C_{p1}}$
DACFC [28]	$\frac{g_{m2}C_a}{g_{o2}C_{p1}}$	$\frac{g_{o2}}{C_{p2}}$
IAC [25]	$g_{m2}R_a$	$\frac{g_{o2}}{C_a}$
UAE [26]	$\frac{g_{m2}C_m}{g_{o2}C_z}$	$\frac{1}{R_mC_m}$
RAFFC [19]	$\frac{C_{c1}}{C_{c2}}$	$\frac{g_{o1}}{C_{p1}}$
DFCFC [21]	$\frac{g_{m2}+g_{m4}}{g_{m4}}$	$\frac{g_{o1}}{C_{m1}}$
ACBC [31]	$(g_{m2}+g_{ma})R_a\frac{r_{o2}}{r_{o1}}$	$(r_{o2}C_a+r_{01}C_m)\frac{g_{o1}g_{02}g_{03}}{C_mC_aC_L}$
PFC [20]	$\frac{C_{m1}}{C_{m2}}$	$\frac{g_{o1}}{C_m}$
TCFC [18]	$\frac{g_{m2}C_{m1}}{g_{o1}g_{o2}R_tC_{m2}}$	$\frac{g_{o2}}{C_{p2}}$
SCCAC [23]	$\frac{kg_{m2}R_2C_m}{C_{p1}}$	$\frac{g_{o2}}{C_{p2}}$
[3]	$g_{m2}R_z\frac{C_mC_z}{C_{p1}C_{p2}}$	$\frac{g_{mb1}}{C_z}$
Proposed Design	$\frac{g_{ma}g_{mb}g_{m3}}{g_{mz}g_{ob}g_{o3}}$	$\frac{g_{mz}}{C_z}$

Table C.1: LFL parameters of various topologies

APPENDIX D

LAYOUT

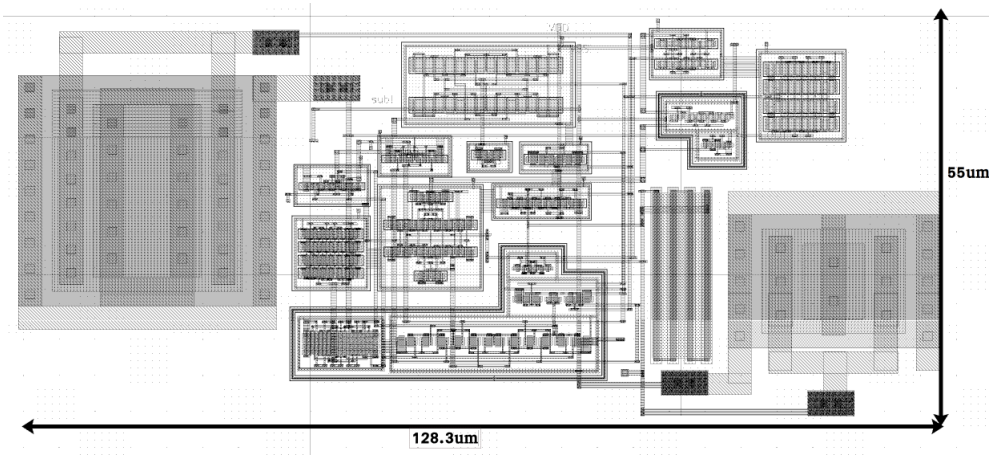

Figure D.1: Layout of OTA with slew helper

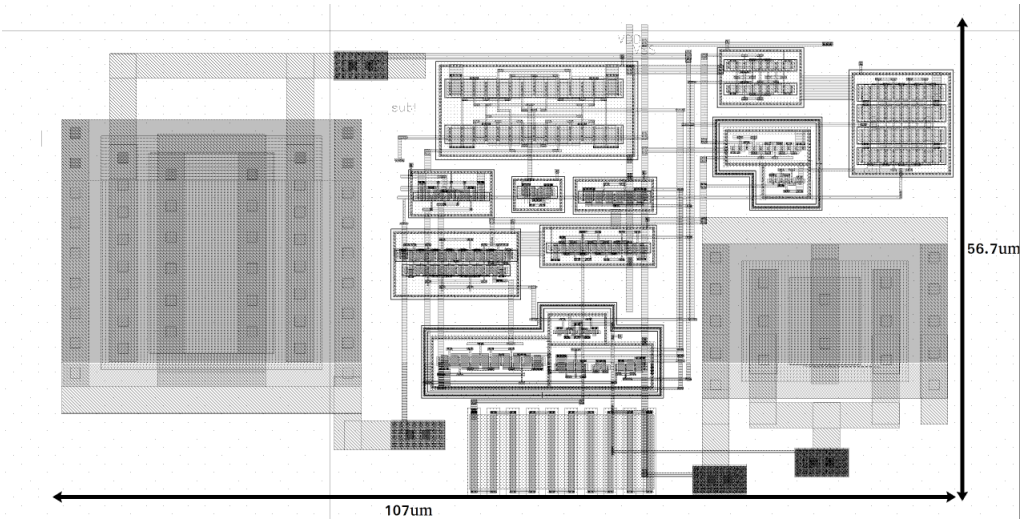

Figure D.2: Layout of OTA without slew helper

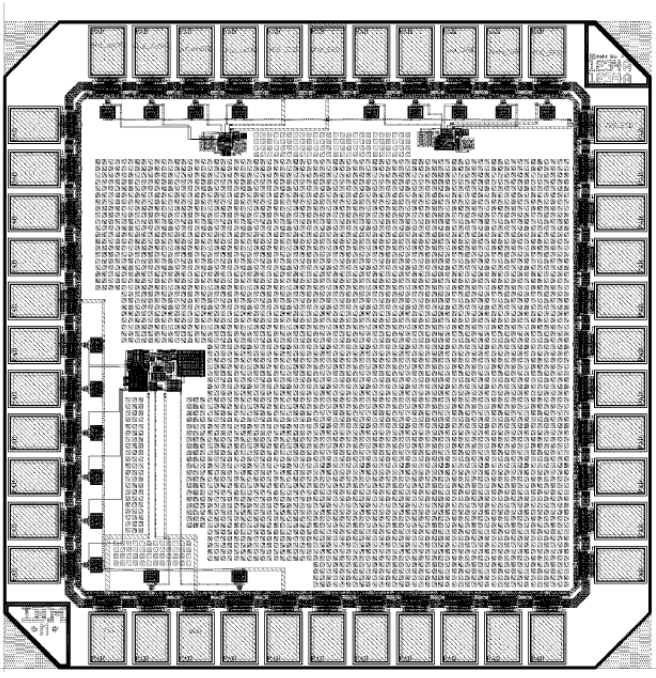

Figure D.3: Pad frame of proposed design

APPENDIX E

MONTE CARLO AND CORNER SIMULATIONS

To ascertain that the proposed design is robust to pvt and circuit mismatch, corner simulations and Monte Carlo simulations were performed. The corners used are TT, SS, SF, FS and FF. Also the Monte Carlo run was done at TT corner with N=100. The results are shown below

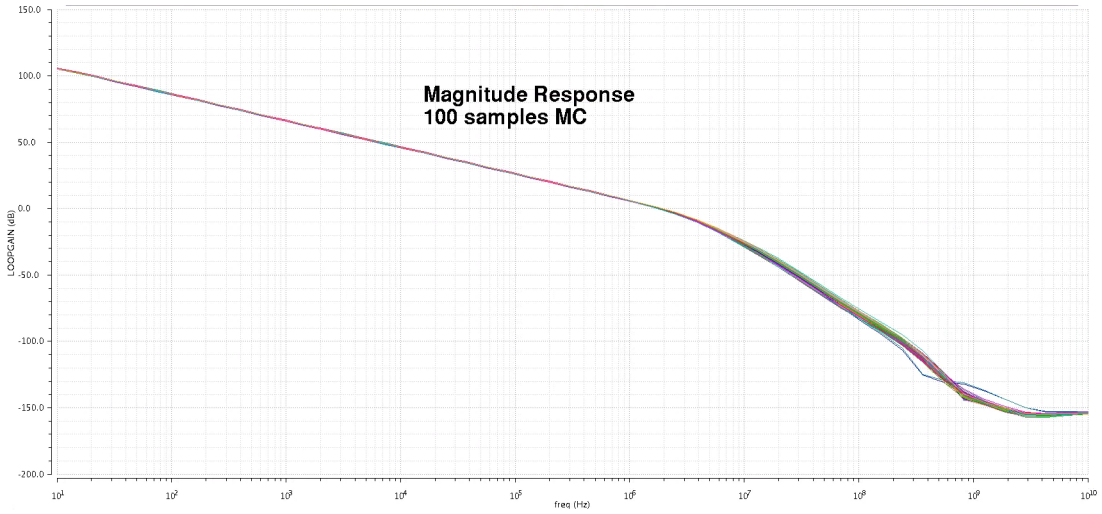

Figure E.1: Monte carlo simulation: Magnitude response

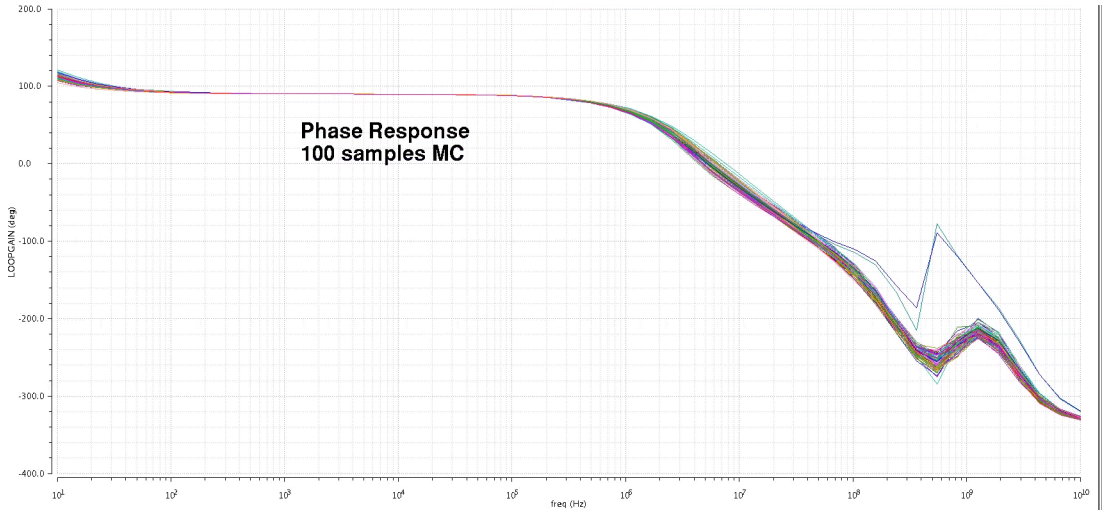

Figure E.2: Monte carlo simulation: Phase response

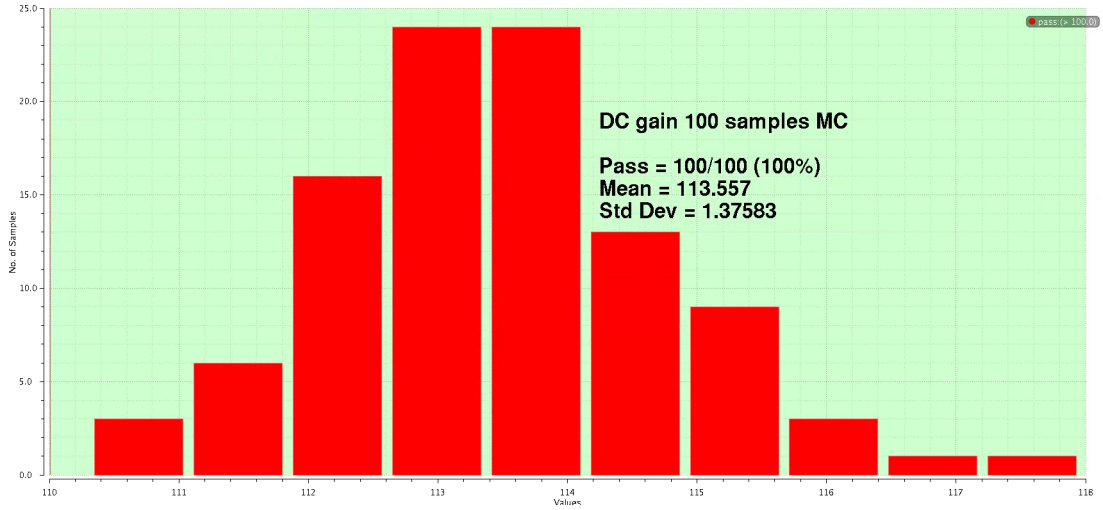

Figure E.3: Monte carlo simulation: DC gain

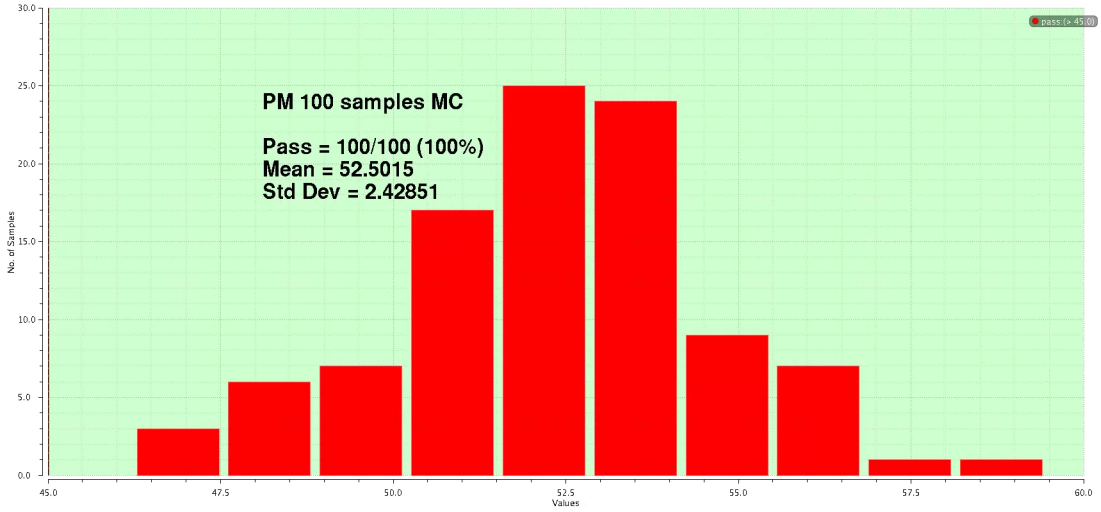

Figure E.4: Monte carlo simulation: Phase margin

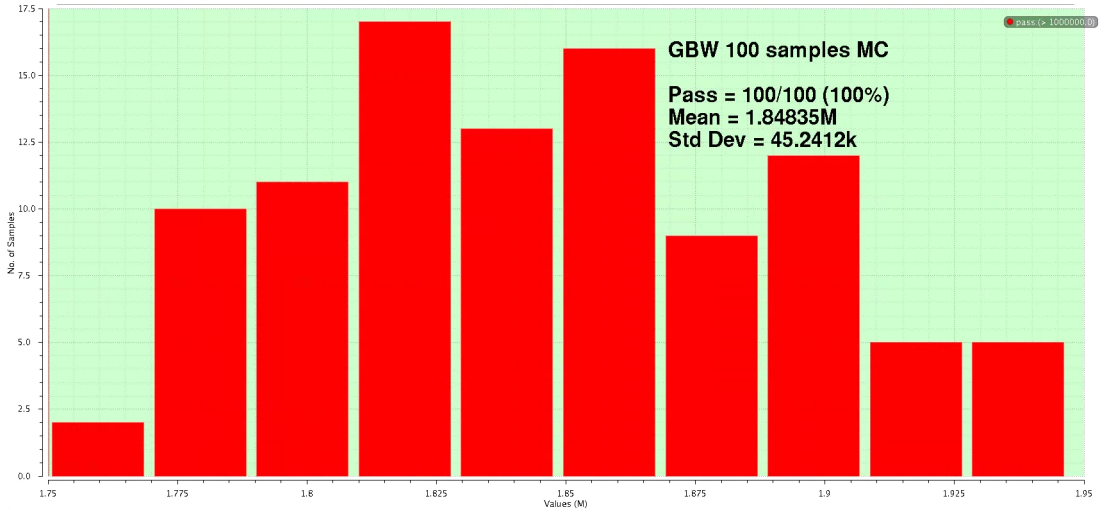

Figure E.5: Monte carlo simulation: GBW

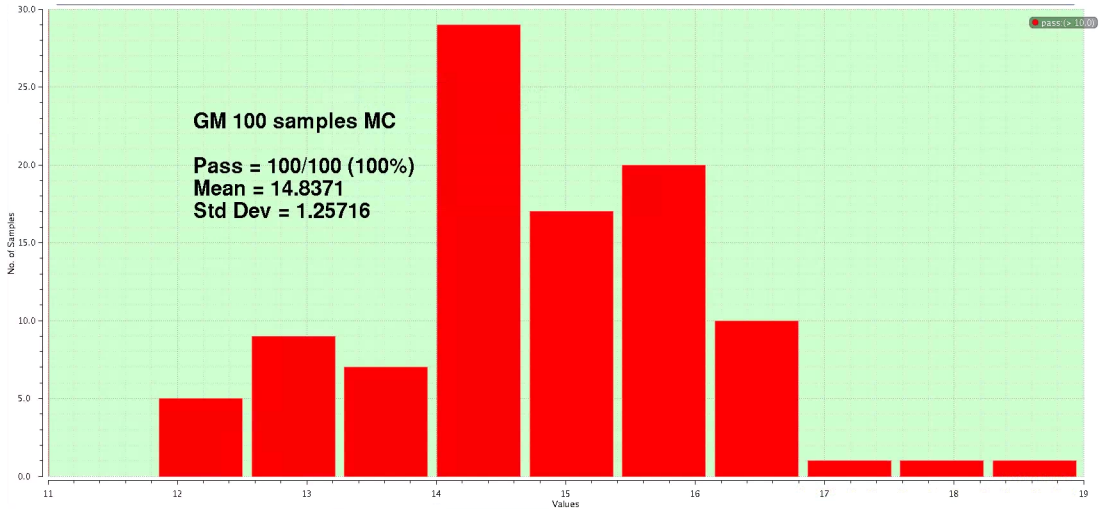

Figure E.6: Monte carlo simulation: Gain margin

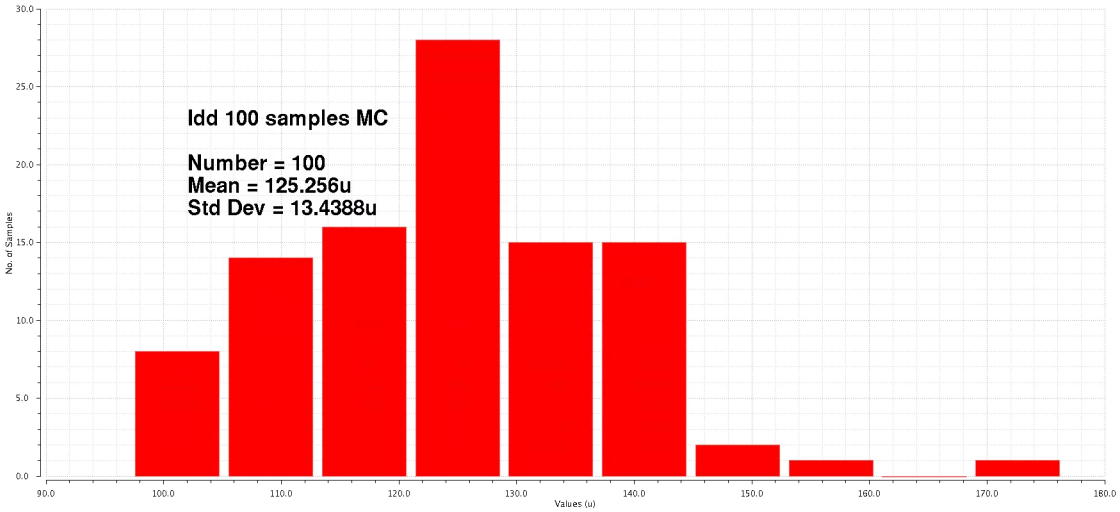

Figure E.7: Monte carlo simulation: Total current