MULTI-STAGE NOISE-SHAPING CONTINUOUS-TIME SIGMA-DELTA MODULATOR

A Dissertation

by

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ABSTRACT

The design of a single-loop continuous-time ΣΔ modulator (CTΣΔM) with high resolution, wide bandwidth, and low power consumption is very challenging. The multi-stage noise-shaping (MASH) CTΣΔM architecture is identified as an advancement to the single-loop CTΣΔM architecture in order to satisfy the ever stringent requirements of next generation wireless systems. However, it suffers from the problems of quantization noise leakage and non-ideal interstage interfacing which hinder its widespread adoption. To solve these issues, this dissertation proposes a MASH CTΣΔM with on-chip RC time constant calibration circuits, multiple feedforward interstage paths, and a fully integrated noise cancellation filter (NCF).

The prototype core modulator architecture is a cascade of two single-loop second-order CTΣΔM stages, each of which consists of an integrator-based active-RC loop filter, current-steering feedback digital-to-analog converters, and a four-bit flash quantizer. On-chip RC time constant calibration circuits and high gain multi-stage operational amplifiers are realized to mitigate quantization noise leakage due to process variation. Multiple feedforward interstage paths are introduced to (i) synthesize a fourth-order noise transfer function with DC zeros, (ii) simplify the design of NCF, and (iii) reduce signal swings at the second-stage integrator outputs. Fully integrated in 40 nm CMOS, the prototype chip achieves 74.4 dB of signal-to-noise and distortion ratio (SNDR), 75.8 dB of signal-to-noise ratio, and 76.8 dB of dynamic range in 50.3 MHz of bandwidth (BW) at 1 GHz of sampling frequency with 43.0 mW of power consumption (P). It does not require external software calibration and possesses minimal out-of-band signal transfer function peaking. The figure-of-merit (FOM), defined as $\mathrm{FOM} = \mathrm{SNDR} + 10\log_{10}(\mathrm{BW}/\mathrm{P})$, is 165.1 dB.

DEDICATION

To my parents

ACKNOWLEDGMENTS

First of all, I would like to express my sincere gratitude to Dr. Jose Silva-Martinez as my advisor. This dissertation would not have been possible without his patience, backing, and encouragement. His deep technical knowledge, strong research integrity, and excellent work ethics taught me to become a better engineer, researcher, and teacher. I could not have imagined having a better supervisor for my graduate study.

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NOMENCLATURE

ADC	Analog-to-Digital Converter
BW	Bandwidth
CMFB	Common-Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CTΣΔM	Continuous-Time ΣΔ Modulator
DAC	Digital-to-Analog Converter
DR	Dynamic Range
DTΣΔM	Discrete-Time ΣΔ Modulator
EA	Error Amplifier
ELD	Excess Loop Delay
FFT	Fast Fourier Transform
FOM	Figure of Merit
FS	Sampling Frequency
FSM	Finite State Machine
GM	Gain Margin
LDO	Low-Dropout
LTE-A	Long-Term-Evolution Advanced
LTF	Leakage Transfer Function
LTI	Linear Time Invariant
LSB	Least Significant Bit
MASH	Multi-Stage Noise-Shaping
MSA	Maximum Stable Amplitude
NCF	Noise Cancellation Filter

NRZ	Non-Return-to-Zero
OA	Operational Amplifier
P	Power Consumption
PCB	Printed Circuit Board
PM	Phase Margin
PSD	Power Spectral Density
Q	Quantizer
QFN	Quad Flat No-Leads
RF	Radio Frequency
SAW	Surface Acoustic Wave
SFDR	Spurious-Free Dynamic Range
SJNR	Signal-to-Jitter-Noise Ratio
SMA	SubMiniature version A
SMASH	Sturdy Multi-Stage Noise-Shaping
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
STF	Signal Transfer Function
SQNR	Signal-to-Quantization-Noise Ratio
UGF	Unity Gain Frequency

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1. INTRODUCTION

1.1 Motivation

Analog-to-digital converters (ADCs) in a long-term-evolution advanced (LTE-A) [1] direct conversion receiver, shown in Fig. 1.1, need at least 50 MHz of bandwidth (BW) for the receiver to obtain 100 MHz of radio frequency (RF) bandwidth with minimum analog baseband complexity [2]. In this wireless application, a continuous-time $\Sigma\Delta$ modulator (CT$\Sigma\Delta$M) is the ADC architecture of choice to meet the stringent specifications of high resolution, wide bandwidth, and low power consumption (P). In addition, it possesses an inherent alias rejection and a tolerance to out-of-band blocker, which are unique features beneficial for this application.

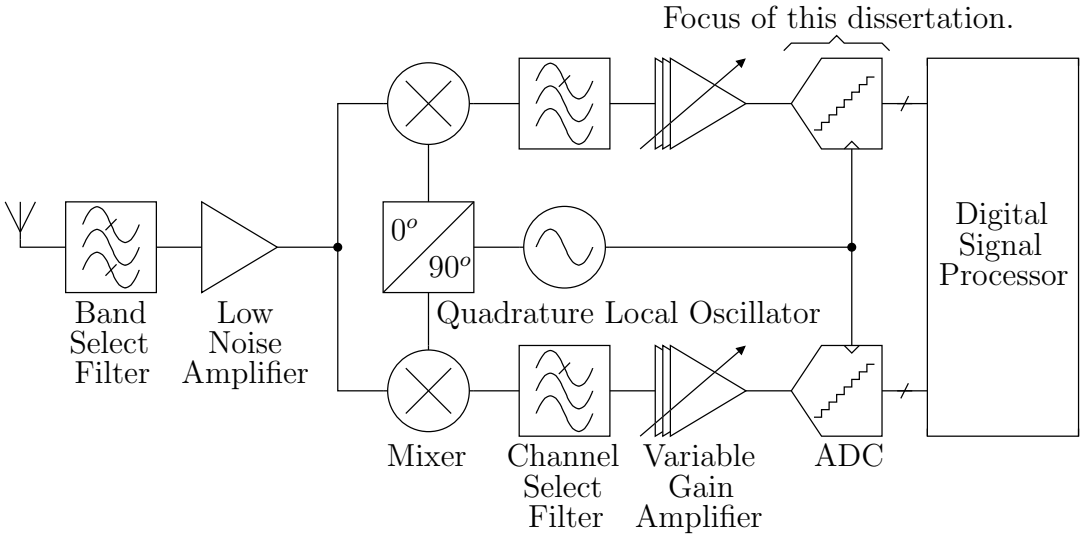


Figure 1.1: Direct conversion receiver architecture.

The historical progression in CMOS low-pass CT$\Sigma\Delta$M design with BW $\geq$ 10 MHz can be followed from Table 1.1. The multi-stage noise-shaping (MASH) CT$\Sigma\Delta$M

Table 1.1: Comparison of CMOS low-pass CTΣΔMs with BW $\geq$ 10 MHz.

Design					Performance in Journal/Conference					
Year	First Author in Journal/Conference	Conference/Journal [Reference]	CMOS (nm)	MASH	BW (MHz)	SNDR (dB)	SNR (dB)	DR (dB)	P (mW)	FOM (dB)
2003	M. Moyal	ISSCC [3]	250	No	12	–	79.0	–	72.0	–
2003	S. Paton	ESSCIRC/JSSC [4, 5]	130	No	15	63.7	64.6	67.0	70.0	147.0
2004	L.J. Breems	ISSCC/JSSC [6, 7]	180	Yes	10	–	63.0	67.0	122.4	–
2005	T.C. Caldwell	ESSCIRC/JSSC [8, 9]	180	No	20	48.8	49.7	55.2	103.0	131.7
2006	G. Mitteregger	ISSCC/JSSC [10, 11]	130	No	20	74.0	76.0	80.0	20.0	164.0
2007	S. Ouzounov	ISSCC [12]	90	No	10	–	–	52	7.0	–
2007	M. Straayer	VLSI/JSSC [13, 14]	130	No	10	72.0	86.0		40.0	156.0
2007	X. Chen	CICC [15]	180	No	25	52.0	53.0	55.0	18.0	143.4
2008	W. Yang	ISSCC [16]	180	No	10	82.0	84.0	87.0	100.0	162.0
2008	K. Reddy	ESSCIRC [17]	180	No	15	64.2	67.2	70.0	20.7	152.8
2009	V. Dhanasekaran	ISSCC/JSSC [18, 19]	65	No	20	60.0	61.6	68.0	10.5	152.8
2009	M. Park	ISSCC/JSSC [20, 21]	130	No	20	78.1	81.2	–	87.0	161.7
2009	P. Crombez	VLSI/JSSC [22, 23]	90	No	10	65.0	–	67.0	6.8	156.7
2009	K. Matsukawa	VLSI/JSSC [24, 25]	110	No	10	62.5	68.2	70.2	5.3	155.2
2009	R.H.M. van Veldhoven	VLSI [26]	45	No	15	–	59.6	–	9.0	–
2009	Y-S. Shu	CICC/JSSC [27, 28]	180	Yes	18	62.5	64.0	68.0	230.0	141.4
2009	H. Kim	JSSC [29]	130	No	10	65.0	68.0	71.0	18.0	152.4
2009	E. Prefasi	JSSC [30]	130	No	17	58.6	59.4	63.4	25.2	146.9
2010	G. Taylor	ISSCC/JSSC [31, 32]	65	No	18	67.0	70.0	–	17.0	157.2
2010	Y. Ke	VLSI [33]	90	No	20	56	–	58	8.5	149.7
2010	C-Y. Lu	JSSC [34]	180	No	25	67.7	68.5	69.0	48.0	154.9
2010	E. Prefasi	ESSCIRC/JSSC [35, 36]	65	No	20	61.0	63.0	63.0	7.00	155.6
2010	J. Sauerbrey	ESSCIRC [37]	65	Yes	15	55.0	58.0	61.0	10.5	146.5
2010	J-G. Jo	A-SSCC/JSSC [38, 39]	130	No	20	63.9	67.9	68.0	58.0	149.3
2011	M. Bolatkale	ISSCC/JSSC [40, 41]	40	No	125	65.0	65.5	70.0	260.0	151.8
2011	J.G. Kauffman	ISSCC/JSSC [42, 43]	90	No	25	63.5	–	70.0	8.0	158.4
2011	A. Jain	ESSCIRC/JSSC [44, 45]	130	No	15.6	59.8	64.5	67.0	4.0	155.7
2011	V. Singh	CICC/JSSC [46, 47]	180	No	16	65.0	67.0	75.0	47.6	150.3
2012	J.G. Kauffman	ISSCC/JSSC [48, 49]	90	No	25	67.5	69.0	72.0	8.5	162.2
2012	K. Reddy	ISSCC/JSSC [50, 51]	90	No	10	78.3	83.0	83.5	16.0	166.3
2012	P. Shettigar	ISSCC/JSSC [52, 53]	90	No	36	70.9	76.4	83.0	15.0	164.7
2012	H. Shibata	ISSCC/JSSC [54, 55]	65	No	150	–	71.0	73.0	750.0	–
2012	V. Srinivasan	ISSCC [56]	45	No	60	60.6	61.5	–	20.0	155.4
2012	K. Matsukawa	VLSI [57]	40	No	10	70.0	70.6	70.6	2.6	165.9
2012	G. Taylor	VLSI/JSSC [58, 59]	65	No	37.5	70.0	71.0	73.0	39.0	159.8
2013	Y-S. Shu	ISSCC [60]	28	No	18	73.6	75.4	78.1	3.9	170.2
2013	C-L. Lo	VLSI [61]	55	No	30	75.1	75.9	77.1	13.0	168.7
2013	T.C. Caldwell	CICC/TCASI [62, 63]	65	No	100	58.4	60.2	62.8	95.0	148.6
2013	J. Huang	CICC/TCASI [64, 65]	180	No	10	74.9	76.6	79.0	70.0	156.4
2013	R. Kaald	CICC [66]	180	No	10	76.0	78.4	80.0	58.0	158.4
2013	J.G. Kauffman	A-SSCC [67]	90	No	50	61.7	62.8	67.0	20.6	155.6
2014	Y. Dong	ISSCC/JSSC [68, 69]	28	Yes	53.3	71.4	83.1	88.0	235.0	154.9
2014	S. Ho	VLSI/JSSC [70, 71]	20	No	80	67.5	70.0	73.0	23.0	162.9
2014	B. Young	VLSI [72]	65	No	50	64.0	71.0	75.0	38.0	155.2
2014	M. Andersson	JSSC [73]	65	No	18.5	56.4	58.9	–	7.9	150.1
2014	S. Zeller	JSSC [74]	65	No	10	68.6	69.3	71.2	1.8	166.0
2014	P. Zhu	ESSCIRC/TCASII [75, 76]	40	Yes	40	66.8	68.7	–	5.0	165.8
2015	Y. Zhang	A-SSCC/TCASI [77, 78]	65	No	15	74.3	77.3	79.4	7.0	167.6
2015	H.M. Geddada	TVLSI [79]	90	No	20	64.0	66.0	69.0	17.1	154.7
2015	D-Y. Yoon	ISSCC/JSSC [80, 81]	28	Yes	50	74.9	76.8	85.0	80.4	162.8
2015	X. Xing	JSSC [82]	28	Yes	40	59.5	60.7	–	2.6	161.4
2015	C. Briseno-Vidrios	VLSI [83]	40	No	75	64.9	65.4	67.7	22.9	160.1
2015	T-K. Kao	VLSI [84]	16	No	39	67.7	–	72.1	12.4	162.7
2015	T. Kim	VLSI [85]	130	No	10	75.3	75.5	78.5	7.2	166.7
2015	S. Loeda	VLSI [86]	40	No	40	66.9	–	67.8	5.3	165.7

Table 1.1: Continued.

Design					Performance in Journal/Conference					
Year	First Author in Journal/Conference	Conference/Journal [Reference]	CMOS (nm)	MASH	BW (MHz)	SNDR (dB)	SNR (dB)	DR (dB)	P (mW)	FOM (dB)
2015	K. Reddy	VLSI [87]	65	No	50	71.5	71.7	72.0	54.0	161.2
2015	C. Ding	ESSCIRC [88]	130	No	20	66.4	66.7	74.6	5.1	162.3
2015	R. Ritter	ESSCIRC [89]	130	No	38.3	50.4	53.9	54.3	15.6	144.3
2015	C-H. Weng	A-SSCC [90]	90	No	13	68.0	69.1	72.3	5.1	162.1
2016	L. Breems	ISSCC [91]	65	No	25	77.0	77.0	77.0	41.4	164.8
2016	Y. Dong	ISSCC [92]	28	Yes	465	64.7	63.1	69.3	930.0	151.7
2016	B. Nowacki	ISSCC [93]	65	Yes	10	72.2	76.0	77.0	1.6	170.2
2016	B. Wu	ISSCC [94]	65	No	45	75.3	78.5	82.5	24.7	167.9
2016	**A. Edward**	**This Work**	**40**	**Yes**	**50.3**	**74.4**	**75.8**	**76.8**	**43.0**	**165.1**

architecture has recently gained popularity due to its wide bandwidth capability [92], low power potential [93], and capacity for integration in an LTE-A base-station transceiver [2]. Nevertheless, the single-loop CTΣΔM architecture is usually preferred over the MASH CTΣΔM architecture due to the problems of quantization noise leakage and non-ideal interstage interfacing. To enable the MASH CTΣΔM architecture to achieve its full potential, these problems need to be addressed.

1.2 Contribution

This dissertation presents system and circuit solutions for the MASH CTΣΔM architecture demonstrated in a prototype MASH 2-2 CTΣΔM chip. Fully integrated in 40 nm CMOS, it achieves 74.4 dB of signal-to-noise and distortion ratio (SNDR), 75.8 dB of signal-to-noise ratio (SNR), and 76.8 dB of dynamic range (DR) in 50.3 MHz of bandwidth at 1 GHz of sampling frequency (FS) with 43.0 mW of power consumption. As shown in Fig. 1.2, it currently has the best figure of merit (FOM), defined as FOM = SNDR + $10\log_{10}$(BW/P), compared to state-of-the-art designs with BW $\geq$ 50 MHz suitable for an LTE-A direct conversion receiver.

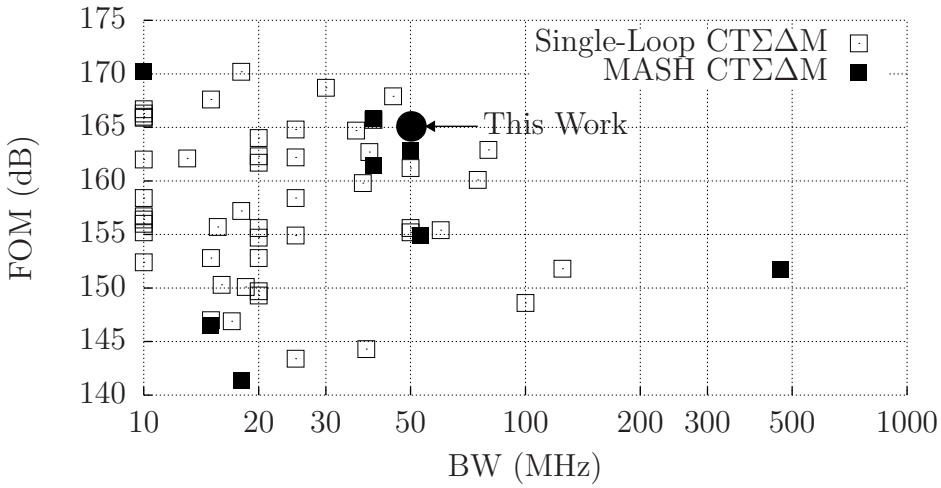


Figure 1.2: FOM vs BW for CMOS low-pass CTΣΔMs in Table 1.1.

1.3 Organization

This dissertation is organized as follows. Section 2 provides theoretical review. Section 3 describes architecture synthesis. Section 4 discusses circuit design. Section 5 reports experimental results. Section 6 presents conclusion.

2. THEORETICAL REVIEW

This section provides theoretical review necessary to understand the MASH CTΣΔM architecture. Signal processing operations behind a Nyquist ADC and a Nyquist digital-to-analog converter (DAC) are studied. General overview on single-loop and MASH ΣΔ modulator architectures is presented.

2.1 Nyquist ADC

Fig. 2.1 shows the time domain model of a Nyquist ADC which performs the sampling and the quantization operations. The analog signal $V(t)$ is sampled to the analog sequence $V[n]$ and quantized to the digital sequence $D[n]$.

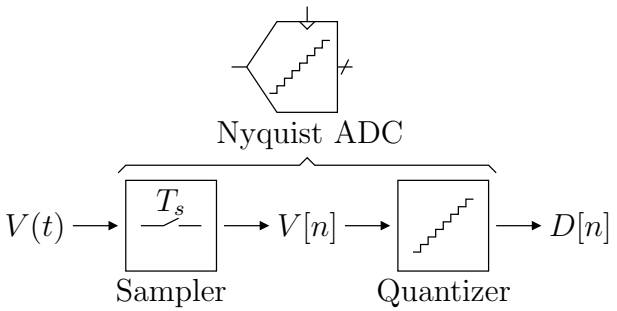


Figure 2.1: Time domain model of a Nyquist ADC.

2.1.1 Sampling

The sampling operation converts a signal $V(t)$ to a sequence $V[n]$ governed by the time domain sampling relationship as follows

$$V[n] = V(t)|_{t=nT_s} \tag{2.1}$$

where T_s is the sampling period.

The sampling operation can be decomposed as shown in Fig. 2.2. First, the signal $V(t)$ is multiplied or modulated by the Dirac delta impulse train $V_s(t)$. Next, the modulated signal $V(t)V_s(t)$ in the form of Dirac delta impulses is converted to have the form of Kronecker delta impulses.

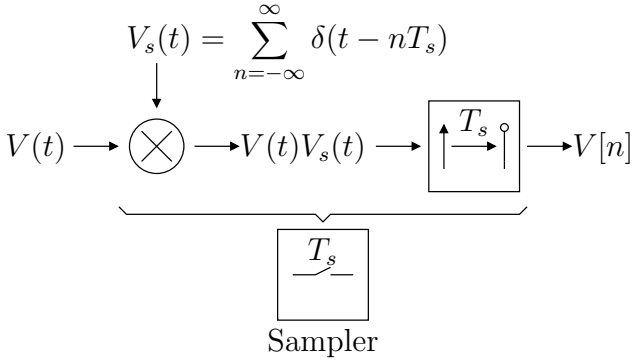


Figure 2.2: Time domain model of a sampler.

The frequency domain counterpart of this model can be derived using a continuous-time Fourier transform to obtain the modulated spectrum given by

$$\frac{1}{2\pi}V(j\omega) * V_s(j\omega) = \frac{1}{T_s}\sum_{k=-\infty}^{\infty} V\left(j\omega - j\frac{2\pi k}{T_s}\right) \tag{2.2}$$

where $V(j\omega)$ and $V_s(j\omega)$ are the spectrums of the signal $V(t)$ and the Dirac delta impulse train $V_s(t)$, respectively.

Note that the modulated spectrum in (2.2) is equal to the sampled spectrum only for aperiodic signals. For periodic signals, the sampled spectrum should be obtained by applying a discrete-time Fourier transform to the time domain sampling relationship in (2.1) instead.

2.1.1.1 Sampling Alias

In the sampling operation, a continuous-time spectrum has to be folded to fit into the limited bandwidth available in a discrete-time spectrum. The folded spectrum is then repeated to satisfy the periodicity property of a discrete-time spectrum. This spectrum folding and repetition describe the mathematical operation in (2.2).

The folding relationship between the angular frequency of a sampled sinusoid signal Ω and the normalized angular frequency of a sinusoid signal ωT_s is given by

$$\Omega = \left| \omega T_s - \left\lfloor \omega T_s + \frac{1}{2} \right\rfloor \right| \tag{2.3}$$

and plotted in Fig. 2.3. The triangular waveform represents the folding pattern in the frequency axis of a continuous-time spectrum. Since multiple sinusoid signals located at different frequencies are mapped to only one frequency after the sampling operation, these signals are the alias of each other. To avoid this interference, the bandwidth of a signal needs to be limited to half the sampling frequency, which is also referred as the Nyquist frequency, before it is sampled.

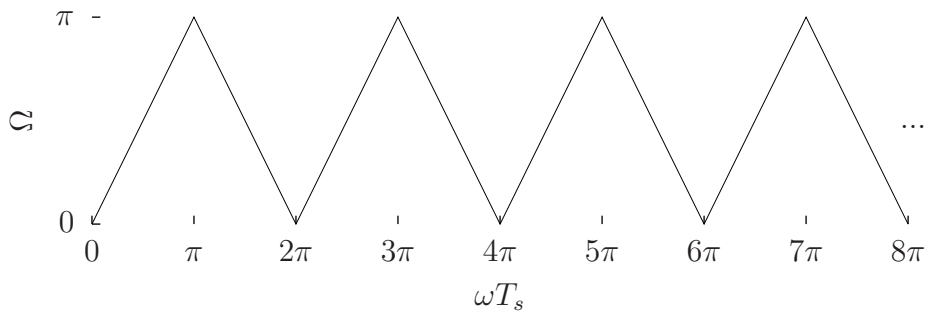


Figure 2.3: Ω vs ωT_s for the sampling operation of a sinusoid signal.

2.1.1.2 Sampling Noise

The understanding of sampling alias is relevant for the analysis of sampling noise. Noise residing outside the Nyquist band is folded inside during the sampling operation and increases the effective noise power spectral density (PSD). To accurately quantify this effect, knowledge of the time and the frequency domain sampling relationships for random signal is needed. They are given by

$$r[n] = r(t)|_{t=nT_s} \tag{2.4}$$

$$\Phi(e^{j\Omega}) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} \Phi\left(j\frac{\Omega}{T_s} - j\frac{2\pi k}{T_s}\right) \tag{2.5}$$

where $r[n]$ and $r(t)$ are the autocorrelation functions of the random sequence and signal, respectively. $\Phi(e^{j\Omega})$ and $\Phi(j\omega)$ are the discrete-time and the continuous-time PSDs of the random sequence and signal, respectively.

Based on these relationships, the sampled noise PSD $\Phi(e^{j\Omega})$ can be calculated if the noise PSD $\Phi(j\omega)$ is known. This calculation can performed with the help of Table A.1 derived in appendix A. If only the total noise power across the whole Nyquist band is of interest, it can be readily computed as follows

$$\overline{N^2} = \frac{1}{2\pi}\int_{-\infty}^{\infty} \Phi(j\omega)d\omega = \frac{1}{2\pi}\int_{-\pi}^{\pi} \Phi(e^{j\Omega})d\Omega \tag{2.6}$$

which is a consequence of the fact that the sampling operation preserves the total noise power in both the continuous-time and the discrete-time domains. A classic example is the kT/C noise. Another example is the notion that sampling white noise signal with infinite bandwidth yields infinite noise power.

2.1.1.3 Sampling Jitter

Jitter can be modelled as a discrete-time sequence $J[n]$ which quantifies the timing deviation of each sampling instance from its ideal position as shown in Fig. 2.4.

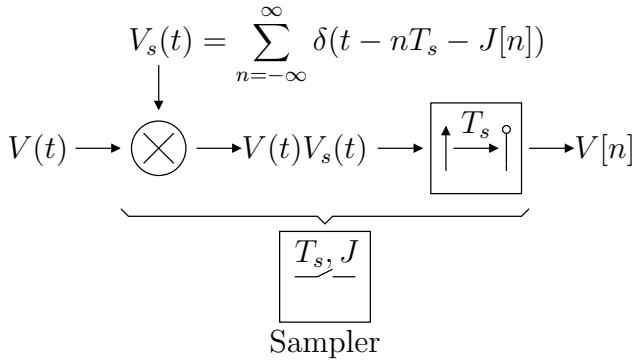


Figure 2.4: Time domain model of a sampler with jitter.

Assuming that the magnitude of the jitter sequence is relatively small compared to the clock period T_s, the sampled signal can be approximated as

$$V[n] \approx V(t)|_{t=nT_s} + J[n] \times \frac{dV(t)}{dt}\bigg|_{t=nT_s} \tag{2.7}$$

where the effect of jitter can be viewed as an additive noise which is equal to the jitter sequence multiplied by the sampled time derivative of the signal.

For a sinusoid signal with an angular frequency of ω_o and a white jitter sequence with a variance of $\overline{J^2}$, the signal-to-jitter-noise ratio (SJNR) is given by

$$\text{SJNR} = 10 \log_{10} \left(\frac{1}{\omega_o^2} \frac{T_s^2}{\overline{J^2}} \right) \tag{2.8}$$

which limits the achievable sampling accuracy, especially for a high frequency signal.

2.1.2 Quantization

The quantization operation converts an analog signal or sequence to a digital signal or sequence. Fig. 2.5 shows example transfer functions for a four-bit quantizer (Q). It shows the discrete output levels and the quantization error vs the continuous input level. The full-scale, denoted as V_{fs}, is defined as the maximum amplitude of a sinusoid input signal or sequence in which its corresponding quantization error remains bounded within half the quantization step size or least significant bit (LSB).

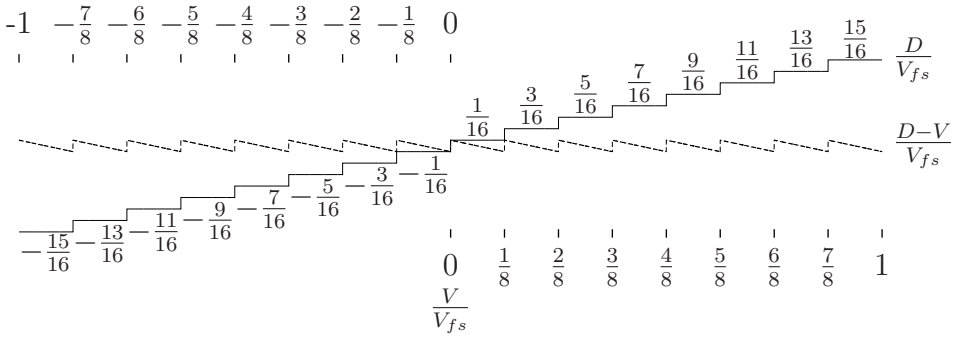


Figure 2.5: Example transfer functions for a four-bit quantizer.

The quantization error is a non-linear input-dependent function. Assuming that the quantizer input is a random signal, it can be modelled as an additive white noise with a uniform probability distribution function [95] as shown in Fig. 2.6. Using this model, the signal-to-quantization-noise ratio (SQNR) for the case of a sinusoid input signal or sequence is given by

$$\mathrm{SQNR} = 10\log_{10}\left(\frac{3}{2}\frac{A^2}{V_{fs}^2}2^{2B}\right) \tag{2.9}$$

where A is the amplitude of the sinusoid input signal or sequence, V_{fs} is the quantizer

full-scale, and B is the number of quantization bits. The SQNR increases by 6 dB every time the number of quantization bits is increased by one.

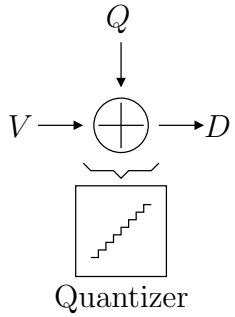


Figure 2.6: Additive white noise model of a quantizer.

Exact analyses on the spectrums of quantized signals are presented in appendix B. For the case of a uniformly quantized sinusoid signal, its spectrum consists of infinite tones located at the odd harmonics as exemplified in Fig. 2.7. The theoretical result in Fig. 2.7 has been validated by transient simulation. In practice, the presence of noise or deliberate dither signal whitens this spectrum and makes the additive white noise model practical to use.

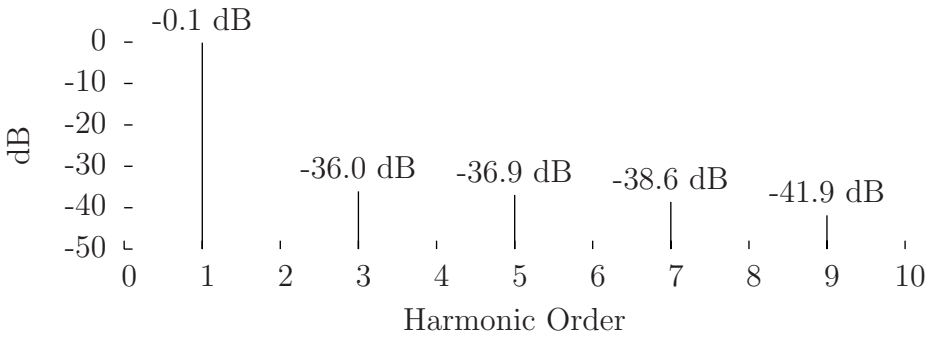


Figure 2.7: Amplitudes of the first five odd harmonic tones in a four-bit quantizer output spectrum processing a full-scale sinusoid input signal.

2.2 Nyquist DAC

Fig. 2.8 shows the time domain model of a Nyquist DAC which performs the requantization and the reconstruction operations. First, the digital sequence $D[n]$ is requantized to another digital sequence $V[n]$. Next, the requantized digital sequence $V[n]$ is reconstructed to the analog signal $V(t)$.

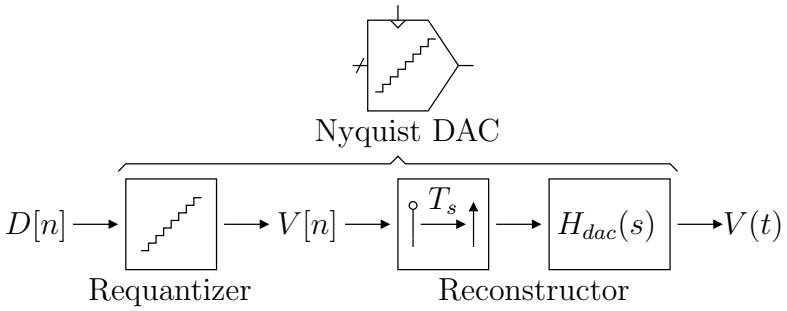


Figure 2.8: Time domain model of a Nyquist DAC.

2.2.1 Requantization

Requantization error or DAC error can be modelled as an additive error which is non-linear and input-dependent as shown in Fig. 2.9.

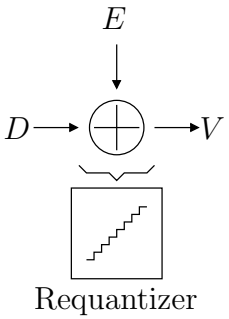


Figure 2.9: Additive DAC error model of a requantizer.

DAC error physically originates from device mismatches. Fig. 2.10 shows the time domain model of a requantizer with mismatch. It consists of $2^B - 1$ unit DAC cells where B is the number of quantization bits. Each unit DAC cell, indexed by the variable m, produces an output of $1 - M\{m\}$ or $1 + M\{m\}$ if the encoded sequence $D[n]\{m\}$ is -1 or $+1$, respectively, where $M\{m\}$ quantifies the normalized mismatch in the weight of the unit DAC cell from its ideal value.

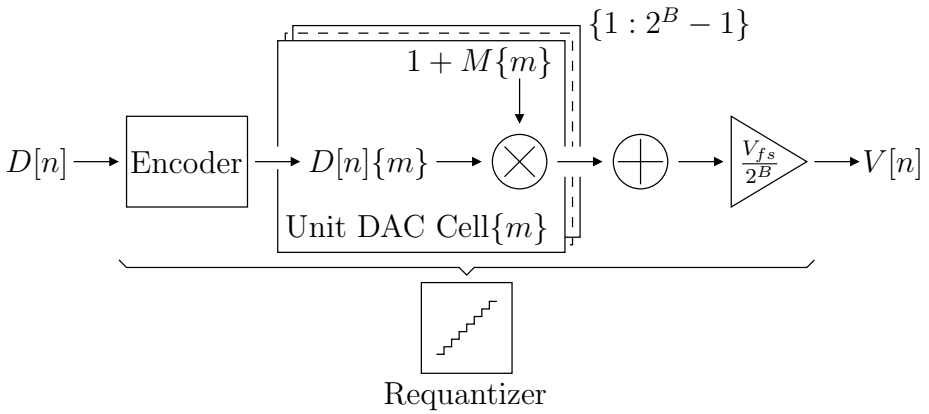


Figure 2.10: Time domain model of a requantizer with mismatch.

The DAC error sequence is given by

$$E[n] = \sum_{m=1}^{2^B-1} M\{m\}D[n]\{m\} \tag{2.10}$$

where the encoded sequence is given by

$$D[n]\{m\} \begin{cases} +1 & \text{if } D[n] > \dfrac{V_{fs}}{2^B}(2^B - 1 - 2m), \\ -1 & \text{if otherwise.} \end{cases} \tag{2.11}$$

Fig. 2.11 shows an example DAC error transfer function for a four-bit requan-

tizer. The mismatch variable $M\{m\}$ is modelled as an independent Gaussian random variable with a mean of zero and a variance of $\overline{M^2} = 1$.

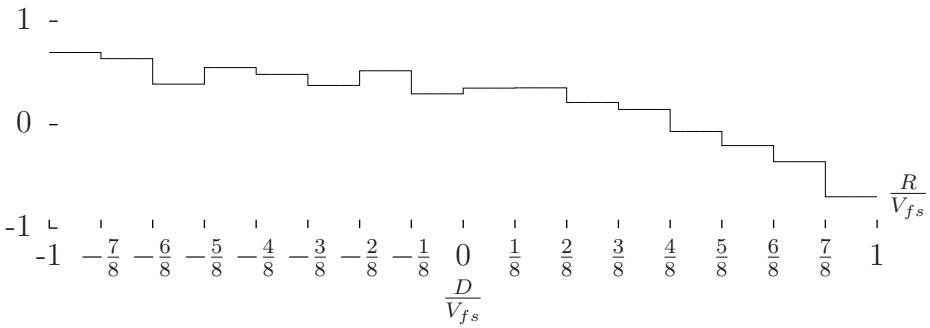


Figure 2.11: Example DAC error transfer function for a four-bit requantizer.

The requantization operation can be viewed as a quantization operation with a non-uniform output level distribution which is analyzed in appendix B. Since it is affected by a random process, the quantity of interest is the expected amplitudes of the harmonic tones in the DAC error spectrum as exemplified in Fig. 2.12. The theoretical result in Fig. 2.12 has been validated with Monte Carlo transient simulations.

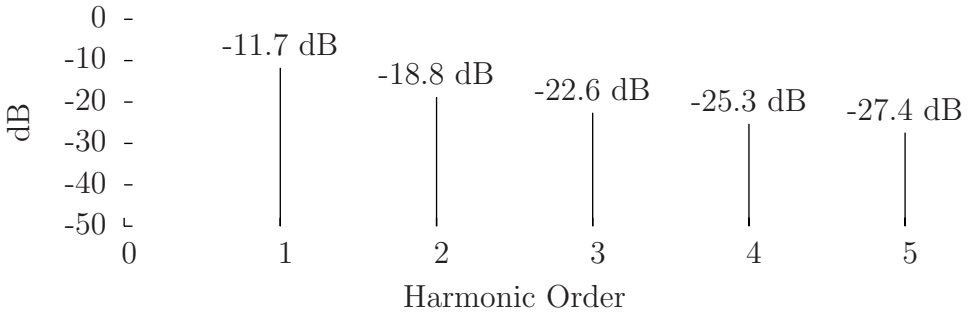


Figure 2.12: Expected amplitudes of the first five harmonic tones in a four-bit DAC error spectrum processing a full-scale sinusoid input sequence. $\overline{M^2} = 1$.

2.2.2 Reconstruction

The reconstruction operation can be decomposed as shown in Fig. 2.8. First, the requantized sequence $V[n]$ in the form of Kronecker delta impulses is converted to have the form of Dirac delta impulses. Next, the converted signal is convolved with the DAC impulse response $h_{dac}(t)$ to generate the reconstructed signal $V(t)$. This time domain reconstruction relationship can be written mathematically as

$$V(t) = \sum_{n=-\infty}^{\infty} V[n]\delta(t - nT_s) * h_{dac}(t) \tag{2.12}$$

The frequency domain reconstruction relationship can be obtained by applying a continuous-time Fourier transform to the time domain reconstruction relationship in (2.12). Similar to the procedure to obtain the frequency domain sampling relationship, one needs to be careful when applying a Fourier transform to a periodic signal or sequence whose Fourier transform does not converge. In this case, one can recall that the Fourier transform for a periodic signal or sequence is defined such that its inverse Fourier transform yields the Fourier series representation of the periodic signal or sequence itself.

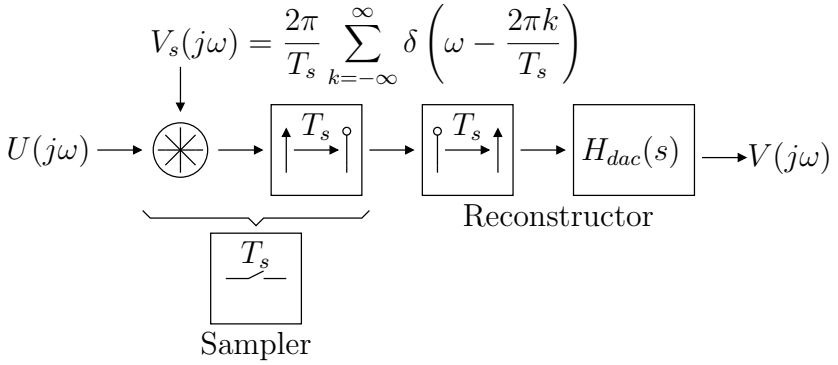


Figure 2.13: Frequency domain model of the cascade interconnection of a sampler followed by a reconstructor.

For a sequence that originates from the sampling operation of a signal, it is more convenient to relate the spectrum of the reconstructed signal $V(j\omega)$ with the spectrum of the signal before sampling $U(j\omega)$. Fig. 2.13 shows this situation modelled in the frequency domain where both the sampler and the reconstructor have the same sampling period of T_s. The reconstructed spectrum is given by

$$V(j\omega) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} U\left(j\omega - j\frac{2\pi k}{T_s}\right) H_{dac}(j\omega) \tag{2.13}$$

where $H_{dac}(j\omega)$ is the DAC transfer function.

In the next subsubsections, the problems of reconstruction alias, noise, and jitter are discussed.

2.2.2.1 Reconstruction Alias

A sinusoid sequence of the form $A\cos[\Omega n]$ has alias sequences of the form $A\cos[\Omega n + 2\pi kn]$ where k is an integer. These aliases are also reconstructed to the continuous-time domain and shaped by the DAC transfer function. Fig. 2.14 shows the normalized transfer function of a non-return-to-zero (NRZ) DAC as an example which provides suppressions for aliases near the integer multiples of the sampling frequency.

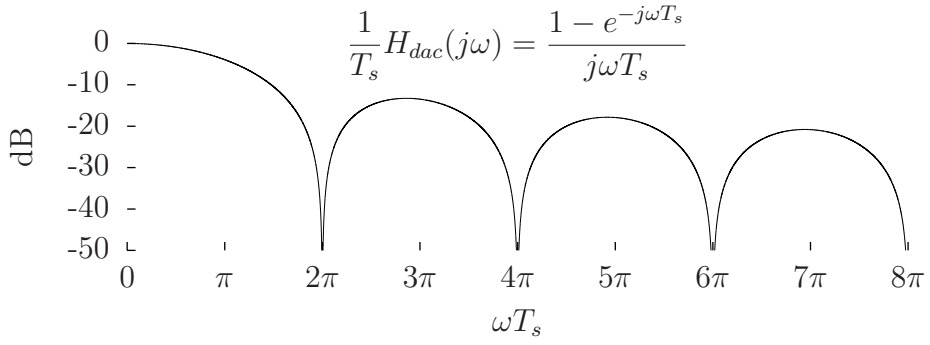


Figure 2.14: Normalized transfer function of an NRZ DAC.

2.2.2.2 Reconstruction Noise

The reconstruction operation also translates noise sequences such as the quantization error and the DAC error to the continuous-time domain. The time and frequency domain reconstruction relationships for a random sequence are given by

$$r(t) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} r[n]\delta(t - nT_s) * h_{dac}(t) * h_{dac}(-t) \tag{2.14}$$

$$\Phi(j\omega) = T_s \times \Phi(e^{j\Omega})|_{\Omega=\omega T_s} \times \frac{1}{T_s^2}|H_{dac}(j\omega)|^2 \tag{2.15}$$

where $r(t)$ and $r[n]$ are the autocorrelation functions of the random signal and sequence, respectively. $\Phi(j\omega)$ and $\Phi(e^{j\Omega})$ are the continuous-time and the discrete-time PSDs of the random signal and sequence, respectively. $h_{dac}(t)$ and $H_{dac}(j\omega)$ are the DAC impulse response and transfer function, respectively.

From (2.15), the reconstruction operation first scales the discrete-time noise PSD $\Phi(e^{j\Omega})$ by the factor T_s. This PSD scaling can be thought as the preservation of the total noise power in the discrete-time domain as the noise power in the continuous-time domain integrated over the Nyquist bandwidth. This can be mathematically written as follows

$$\overline{N^2} = \frac{1}{2\pi}\int_{-\pi}^{\pi} \Phi(e^{j\Omega})d\Omega = \frac{T_s}{2\pi}\int_{-\frac{\pi}{T_s}}^{\frac{\pi}{T_s}} \Phi(e^{j\Omega})|_{\Omega=\omega T_s} d\omega \tag{2.16}$$

Next, the scaled discrete-time noise PSD is shaped by the square magnitude of the normalized DAC transfer function to obtain the continuous-time noise PSD. As an example, the normalized NRZ DAC transfer function is plotted in Fig. 2.14 which has 0 dB of gain at low frequency.

2.2.2.3 Reconstruction Jitter

Analogous to sampling jitter, reconstruction jitter can be modelled as a discrete-time sequence $J[n]$ which quantifies the timing deviation of each reconstruction instance from its ideal position. As an example, the reconstructed signal for an NRZ DAC with jitter is given by

$$V(t) = \sum_{n=-\infty}^{\infty} (V[n] - V[n-1])u(t - nT_s - J[n]) \tag{2.17}$$

which is illustrated in Fig. 2.15 together with the additive jitter noise signal obtained by taking the difference between the reconstructed signal with jitter and the ideal reconstructed signal.

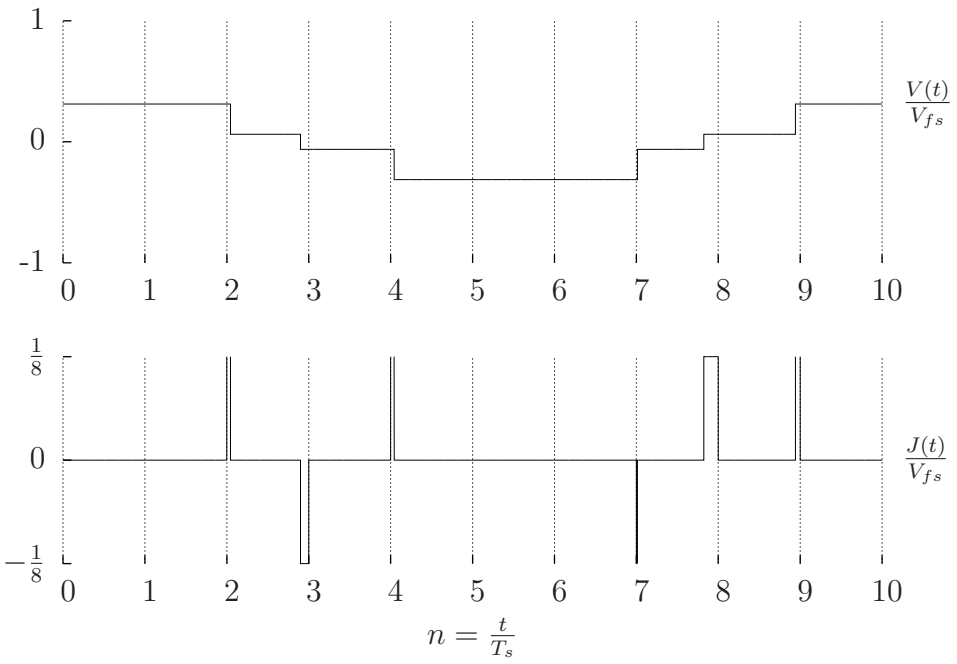


Figure 2.15: Example reconstructed signal with jitter and additive jitter noise signal.

In most practical situations, the NRZ DAC output is processed by a continuous-time linear time invariant (LTI) system as shown in Fig. 2.16. Therefore, the quantity of interest is the response of the continuous-time LTI system to the additive jitter noise signal. This response may also be sampled by the observer in other situations.

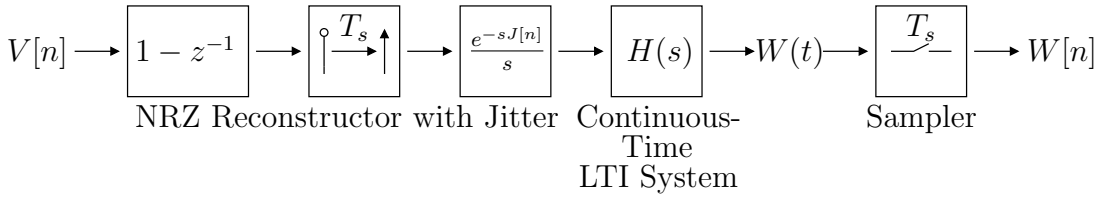


Figure 2.16: Time domain model of the cascade interconnection of a NRZ reconstructor with jitter followed by a continuous-time LTI system and a sampler.

Assuming that the magnitude of the jitter sequence is relatively small compared to the clock period, the reconstructed signal at the continuous-time LTI system output can be approximated using Taylor series expansion as

$$W(t) \approx \sum_{n=-\infty}^{\infty} (V[n] - V[n-1])u(t - nT_s) * h(t) + \sum_{n=-\infty}^{\infty} J[n](V[n] - V[n-1])\delta(t - nT_s) * h_j(t) \tag{2.18}$$

which consists of the ideal reconstructed signal and the continuous-time LTI system response to the additive jitter noise signal. This response is proportional to the jitter sequence $J[n]$ multiplied by the first-order discrete-time derivative of the requantized sequence $V[n] - V[n-1]$. It is also the result of a convolution operation with the jitter impulse response $h_j(t)$ of the system.

2.3 ΣΔ Modulator

In this section, an overview on the discrete-time and the continuous-time single-loop as well as MASH ΣΔ modulator architectures is presented.

2.3.1 DTΣΔM

Fig. 2.17 shows the time domain model of a discrete-time ΣΔ ADC, which was first introduced in [96]. It consists of a sampler, a discrete-time ΣΔ modulator (DTΣΔM), and a digital decimation filter. The DTΣΔM consists of a discrete-time loop filter, a Nyquist ADC, and a Nyquist DAC in a feedback loop configuration. The Nyquist ADC and the Nyquist DAC are typically of low resolution and referred as the quantizer and the feedback DAC, respectively.

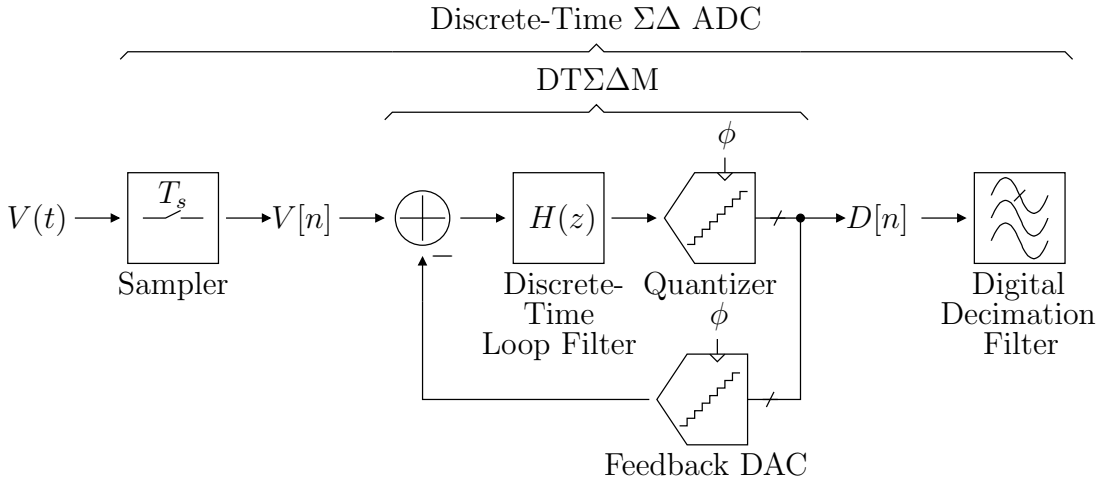


Figure 2.17: Time domain model of a discrete-time ΣΔ ADC.

The analysis of a DTΣΔM is performed by using the linearized model as shown in Fig. 2.18. In this model, the quantizer is replaced by an additive white noise and the feedback DAC is replaced by a direct connection. The detailed continuous-

time modelling of the Nyquist ADC and the Nyquist DAC presented in the previous sections can be omitted in this discrete-time model.

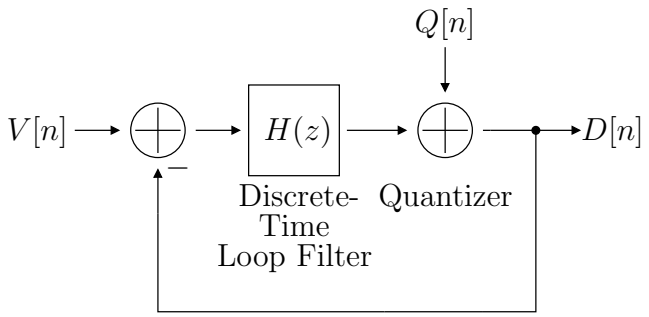


Figure 2.18: Time domain linearized model of a DTΣΔM.

The modulator output spectrum is given by

$$D(z) = \mathrm{STF}(z)V(z) + \mathrm{NTF}(z)Q(z) \tag{2.19}$$

where the signal transfer function (STF) and the noise transfer function (NTF) of the modulator are given by

$$\mathrm{STF}(z) = \frac{H(z)}{1 + H(z)} \tag{2.20}$$

$$\mathrm{NTF}(z) = \frac{1}{1 + H(z)} \tag{2.21}$$

Fig. 2.19 shows example STF and NTF of a fourth-order DTΣΔM. The order of the modulator refers to the number of zeros in the NTF, whose positions in this example are spread across the bandwidth of interest to minimize the quantization noise. Across the bandwidth of interest of $\pi/10$ in this example, the STF provides a unity gain and the NTF provides 47.6 dB of quantization noise suppression.

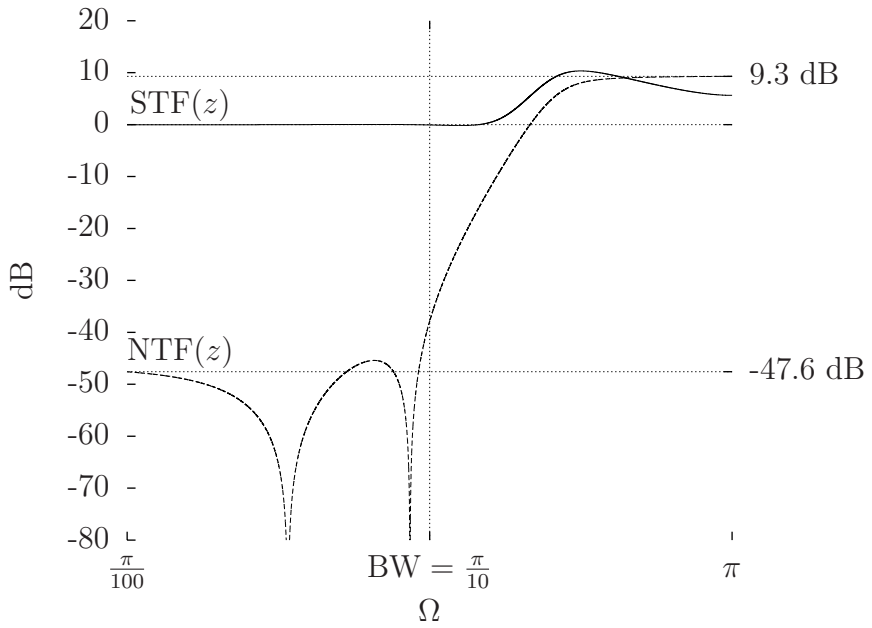


Figure 2.19: Example STF and NTF of a fourth-order DTΣΔM.

The ratio between the Nyquist frequency FS/2 and the bandwidth of interest BW is an important design parameter called the oversampling ratio (OSR). It is mathematically defined as follows

$$\text{OSR} = \frac{\text{FS}/2}{\text{BW}} \tag{2.22}$$

To relax the design of an anti alias filter, a Nyquist ADC is typically operated with an OSR > 1. Assuming that the quantization noise in a Nyquist ADC is spread uniformly across the Nyquist bandwidth, the quantization noise power normalized to the full-scale sinusoid input power or the quantization noise floor is given by

$$\overline{Q^2} = \frac{2}{3}\frac{1}{2^{2B}}\frac{1}{\text{OSR}} \tag{2.23}$$

where B is the number of quantization bits. For example, a four-bit Nyquist ADC with -25.8 dBFS of quantization noise floor over the Nyquist bandwidth has -35.8 dBFS of quantization noise floor with an OSR of 10. The quantization noise floor reduces by 10 dB every time the OSR is increased by ten times.

For a $\Sigma\Delta$ ADC, the quantization noise floor is given by

$$\overline{Q^2} = \frac{2}{3}\frac{1}{2^{2B}} \times \frac{1}{2\pi}\int_{-\frac{\pi}{\mathrm{OSR}}}^{\frac{\pi}{\mathrm{OSR}}} |\mathrm{NTF}(e^{j\Omega})|^2 d\Omega \tag{2.24}$$

For example, a $\Sigma\Delta$ ADC with a four-bit quantizer and an NTF as shown in Fig. 2.19 has -83.4 dBFS of quantization noise floor. The difference of 47.6 dB between the quantization noise floors of the example $\Sigma\Delta$ ADC and the example Nyquist ADC is attributed to the quantization noise suppression provided by the NTF of a $\Sigma\Delta$ ADC. This improvement comes at the cost of potential for feedback loop instability.

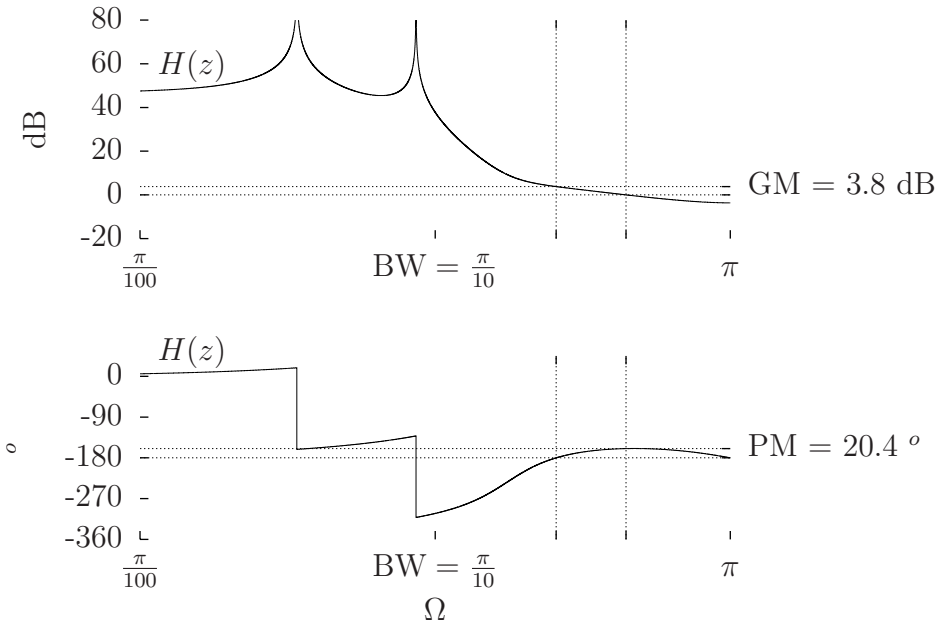


Figure 2.20: Example bode plot of a fourth-order discrete-time loop filter.

The stability of the feedback loop in a DTΣΔM can be assessed using linear analyses. Fig. 2.20 shows example bode plot of a fourth-order discrete-time loop filter. The phase margin (PM) and gain margin (GM) are 20.4 ^{o} and 3.8 dB, respectively, predicting that the modulator is stable.

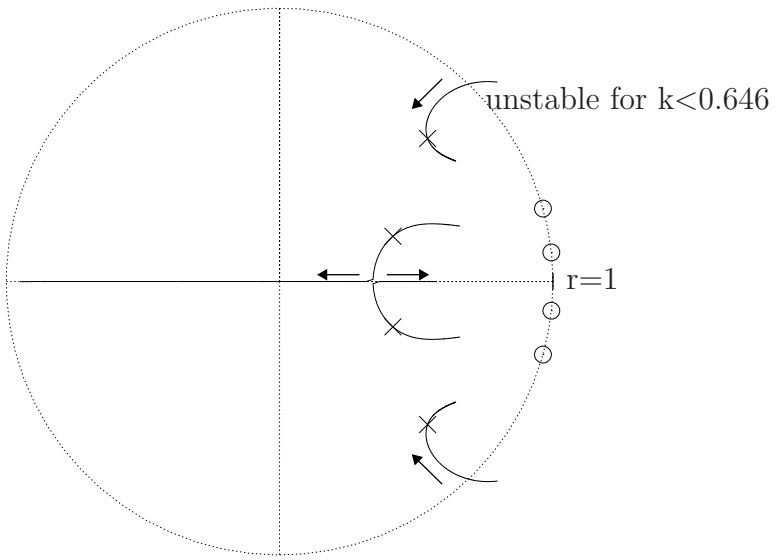


Figure 2.21: Example root locus plot of a fourth-order DTΣΔM vs quantizer gain k from 0.5 to 1.5.

Another tool to assess the stability of the feedback loop in a DTΣΔM is the root locus analysis. Fig. 2.21 shows an example root locus plot of a fourth-order DTΣΔM vs quantizer gain k from 0.5 to 1.5. The quantizer gain k can be modelled in Fig. 2.18 by modifying the discrete-time loop filter transfer function from $H(z)$ to $kH(z)$. Two poles of the NTF go outside the unit circle for $k < 0.646$, which corresponds to GM of 3.8 dB from the Bode plot analysis. The root locus analysis can be repeated for all modulator parameters to obtain their margins against variations.

To verify the results of linear analyses, transient simulation using a non-linear quantizer model is a must. Fig. 2.22 shows an example output sequence and a Fast Fourier Transform (FFT) spectrum of a fourth-order DTΣΔM. The input sequence is a sinusoid with an amplitude of −1.7 dBFS and a frequency of about one-fifth the bandwidth of the modulator. The SQNR is 82.0 dB. The quantization noise floor is −83.7 dBFS which is very close to the theoretical prediction of −83.4 dBFS.

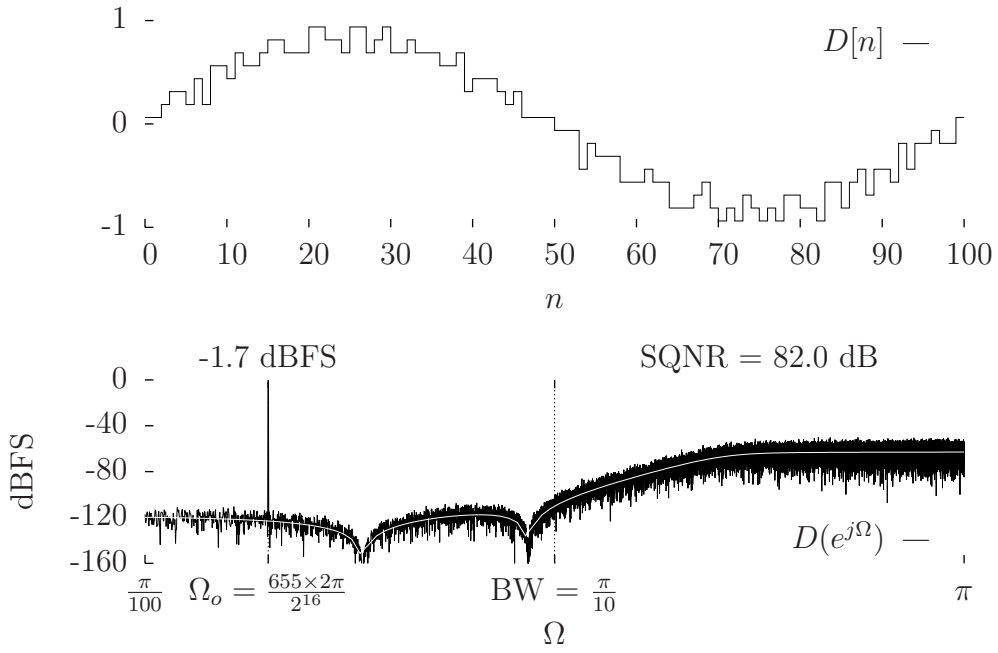


Figure 2.22: Example output sequence and FFT spectrum of a fourth-order DTΣΔM.

This simulation can be repeated for different amplitudes of the sinusoid input sequence to obtain the plot shown in Fig. 2.23. The DR, defined as the ratio between the maximum and minimum amplitude of the sinusoid input sequence which corresponds to SQNR > 0 dB, is 82.1 dB. The maximum stable amplitude (MSA) is −1.2 dBFS. For sinusoid input sequence with amplitude greater than the MSA, the

modulator overloads and exhibits negative SQNR.

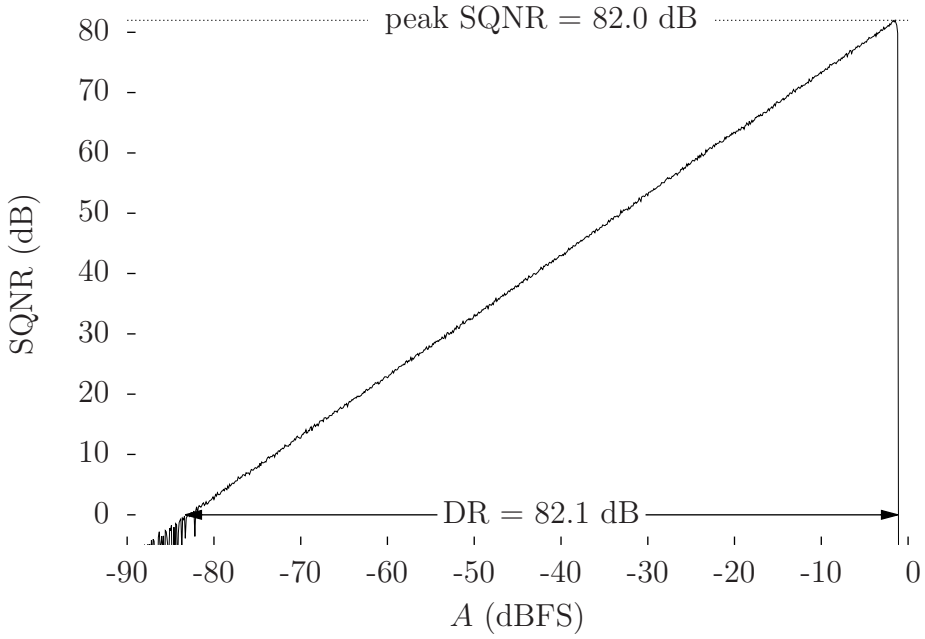


Figure 2.23: Example SQNR vs sinusoid input sequence amplitude of a 4^{th}-order DT$\Sigma\Delta$M.

To understand the modulator overload behaviour, one needs to recognize that the quantizer in a $\Sigma\Delta$ modulator processes both the input and the feedbacked quantization noise sequences. Using linear analysis, the feedbacked quantization noise floor at the quantizer input is given by

$$\text{feedbacked } \overline{Q^2} = \frac{2}{3}\frac{1}{2^{2B}} \times \frac{1}{2\pi}\int_{-\pi}^{\pi} |\text{NTF}(e^{j\Omega}) - 1|^2 d\Omega \tag{2.25}$$

which is amplified to -18.9 dBFS from -25.8 dBFS in this example. Assuming that the probability distribution function of the feedbacked quantization noise is also uniform, this corresponds to the feedbacked quantization noise level bounded

within $\pm 0.140\ V_{fs}$. Thus, the amplitude of the sinusoid input sequence should be limited to $0.860\ V_{fs}$ or -1.3 dBFS to ensure that the quantizer input level never exceeds full-scale. This theoretical prediction is very close to the simulated value of -1.2 dBFS. The MSA can therefore be estimated using the following formula

$$\frac{\text{MSA}}{V_{fs}} = 1 - \frac{1}{2^B}\sqrt{\frac{1}{2\pi}\int_{-\pi}^{\pi} |\text{NTF}(e^{j\Omega}) - 1|^2 d\Omega} \tag{2.26}$$

The MSA is improved by increasing the number of quantization levels and reducing the feedbacked quantization noise amplification factor. This amplification factor is correlated to the aggressiveness of the NTF, which is usually quantified by the peak NTF gain or the out-of-band NTF gain.

As the out-of-band NTF gain is increased, the quantization noise suppression of the modulator is also improved or becomes more aggressive. This fact is a consequence of the "waterbed effect" which states that if a disturbance in a feedback system is suppressed at some frequency range, it will be amplified at the other frequency range. The modulator also becomes less stable with reduced margin against variations independent from the number of quantization levels.

Reducing the out-of-band NTF gain to improve the modulator robustness is only recommended up to certain point in which the quantizer tonal behaviour manifests in the modulator output spectrum [97]. This can be explained as the strength of the dithering effect provided by feedbacked quantization noise at the quantizer input is reduced. Thus, the NTF is a very important parameter in a $\Sigma\Delta$ modulator design which should be carefully selected to balance the trade-off between the quantization noise suppression and the design complexity needed to keep variations under control.

2.3.2 CTΣΔM

Fig. 2.24 shows the time domain model of a continuous-time ΣΔ ADC. Compared to the discrete-time ΣΔ ADC in Fig. 2.17, the continuous-time ΣΔ ADC does not require a dedicated sampler at the ADC input since the loop filter directly processes the input signal. The sampling operation occurs inside the quantizer. The feedback DAC also plays a role to reconstruct the digital output sequence to its continuous-time counterpart for the feedback operation.

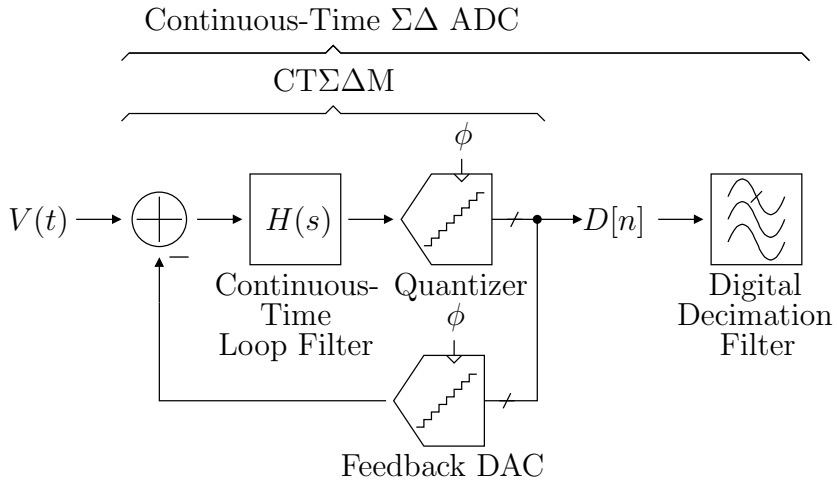


Figure 2.24: Time domain model of a continuous-time ΣΔ ADC.

The analysis of a CTΣΔM is performed by using the linearized model as shown in Fig. 2.25. In this model, the continuous-time loop filter is split into its feedforward and feedback parts which process the input signal and the output sequence, respectively. The feedback part together with the feedback DAC transfer function can be modelled in the discrete-time domain using impulse invariant analysis demonstrated in appendix C. Thus, the analyses presented in the previous subsection are also valid for a CTΣΔM.

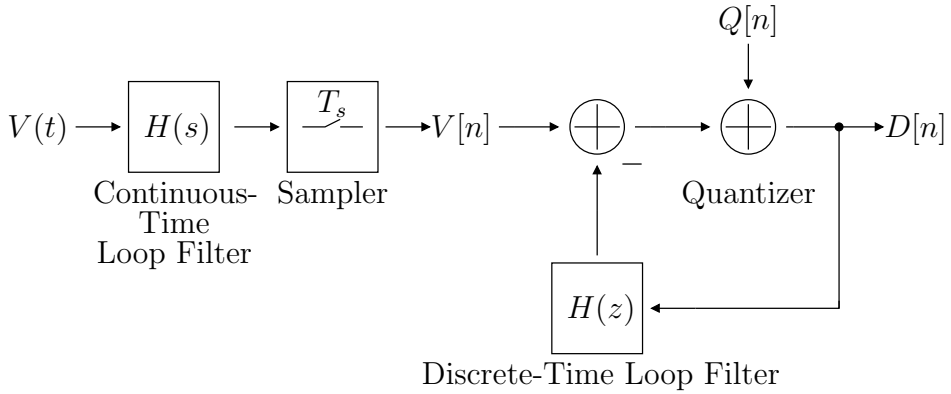


Figure 2.25: Time domain linearized model of a CTΣΔM.

Using a zero clock cycle delay NRZ feedback DAC as an example, a continuous-time loop filter can be synthesized with the help of Table C.1 in appendix C such that its pulse response matches with the impulse response of the original discrete-time loop filter at the quantizer sampling instances. This is shown in Fig. 2.26.

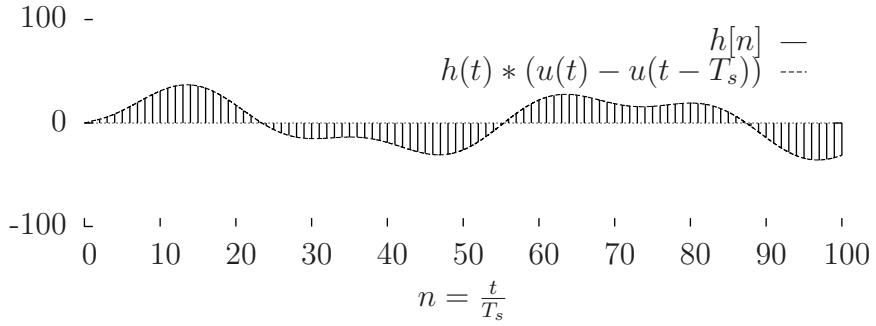


Figure 2.26: Example discrete-time loop filter impulse response and continuous-time loop filter pulse response of a fourth-order CTΣΔM.

The continuous-time transfer function of the cascade interconnection of a zero clock cycle delay NRZ feedback DAC followed by a continuous-time loop filter is compared with its discrete-time counterpart as shown in Fig. 2.27. Good matching

is observed in-band. However, they differ considerably out-of-band near their unity gain frequencies which can affect the result of linear stability analysis. This difference is caused by the transfer function folding experienced by the discrete-time loop filter transfer function as follows

$$H(e^{j\Omega}) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} H_{dac}(j\omega)H(j\omega)\Big|_{\omega=\frac{\Omega}{T_s}-\frac{2\pi k}{T_s}} \tag{2.27}$$

For example, the worst-case error in the magnitude of the continuous-time transfer function is reduced from 61 % to 20 % at the Nyquist frequency if just one folding $k = 1$ is taken into account. (2.27) is therefore practical to assist the stability analysis of a CTΣΔM using an AC simulation where an exact impulse invariant transform analysis is too complex to be performed.

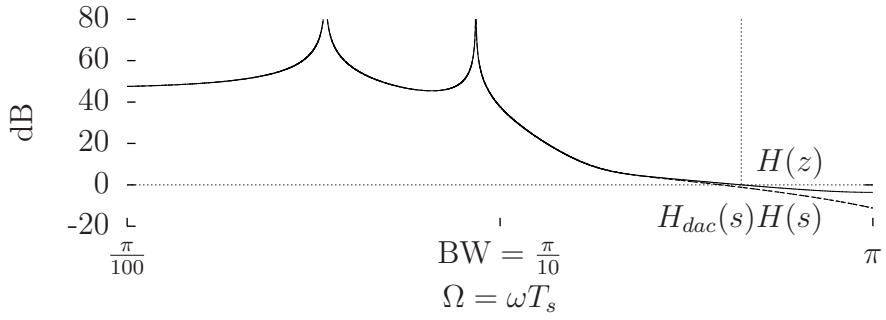


Figure 2.27: Example transfer functions of the cascade interconnection of a zero clock cycle delay NRZ feedback DAC followed by a continuous-time loop filter and the discrete-time loop filter of a fourth-order CTΣΔM.

The determination of an STF in a CTΣΔM is not as straightforward as that in a DTΣΔM as its input is still in the continuous-time domain. The modulator output

spectrum is given by

$$D(e^{j\Omega}) = \sum_{k=-\infty}^{\infty} \mathrm{STF}(j\omega)V(j\omega)|_{\omega=\frac{\Omega}{T_s}-\frac{2\pi k}{T_s}} + \mathrm{NTF}(e^{j\Omega})Q(e^{j\Omega}) \tag{2.28}$$

where the STF for a periodic input signal is given by

$$\mathrm{STF}(j\omega) = H(j\omega)\mathrm{NTF}(e^{j\omega T_s}) \tag{2.29}$$

Fig. 2.28 shows an example STF of a fourth-order CTΣΔM. Assuming that the input signal is a sinusoid, the x-axis corresponds to its normalized angular frequency ωT_s and the y-axis corresponds to the gain it experiences. The angular frequency of the sinusoid output sequence Ω can be determined using the folding relationship in (2.3). For an aperiodic input signal, the STF in (2.29) is scaled by the factor $1/T_s$.

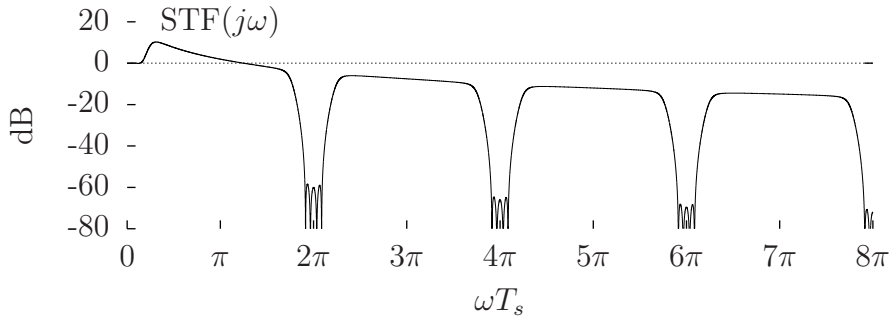


Figure 2.28: Example STF of a 4^{th}-order CTΣΔM.

The STF of a CTΣΔM provides a strong attenuation for alias input signals residing near the integer multiples of the sampling frequency. This rejection is commensurate with the degree of NTF suppression and the continuous-time loop filter out-of-band filtering. The alias rejection provided by the NTF can be understood

as a consequence of the fact that the sampling and the quantization operations in a CTΣΔM occur at the same place which is the quantizer. Thus, any error in the sampling operation is indistinguishable from the quantization noise.

The example STF in Fig. 2.28 exhibits out-of-band peaking for input signal located approximately between the modulator bandwidth and the Nyquist frequency. This peaking is undesired in wireless applications as strong out-of-band blocker can potentially overload the modulator. In a practical CTΣΔM implementation, the loop filter topology can be selected to provide independent control between the STF and the NTF in which out-of-band STF peaking can be eliminated in some topologies to provide an out-of-band blocker tolerance.

In addition to the advantages of an inherent alias rejection and a tolerance to out-of-band blocker, the CTΣΔM architecture is currently favored compared to the DTΣΔM architecture in wide bandwidth ΣΔ modulator implementations. The widest bandwidth attained by a CTΣΔM currently is 465 MHz [92] compared to the 40 MHz of bandwidth attained by a DTΣΔM [98]. This can be attributed to the superior power and noise efficiencies of continuous-time circuits compared to discrete-time circuits.

However, the design of a CTΣΔM has several challenging aspects to be tackled compared to the design of a DTΣΔM. Due to the higher speed of operation, excess loop delay (ELD) caused by the non-zero delay in the operations of the quantizer and the feedback DAC degrades stability and needs to be compensated by additional circuit complexities. Due to its continuous-time operation, timing error in the feedback DAC such as jitter, delay mismatch, and waveform asymmetry degrades the performance. These non-idealities will be studied in more details for the proposed architecture.

2.3.3 MASH ΣΔ Modulator

Fig. 2.29 shows the time domain model of a two-stage MASH DTΣΔM, which was first introduced in [99] in the three-stage version. Analysis are performed in the discrete-time domain for simplicity. Both stages consist of discrete-time loop filters, feedback DACs, and quantizers. Interstage connection is implemented by taking the difference between the input and the output of Q_1 using DAC_2. Therefore, the input of the second stage is simply the inverted first-stage quantization noise.

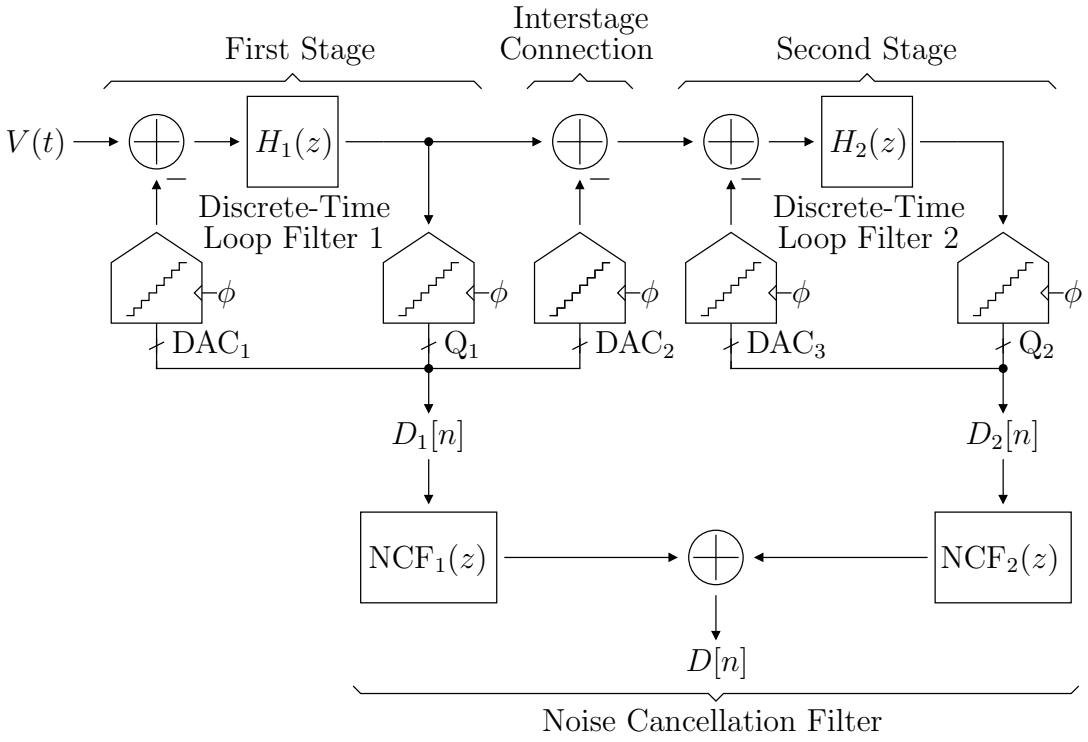


Figure 2.29: Time domain model of a two-stage MASH DTΣΔM.

The spectrum of the noise cancellation filter (NCF) output is given by

$$D(z) = \mathrm{STF}(z)V(z) + \mathrm{LTF}(z)Q_1(z) + \mathrm{NTF}(z)Q_2(z) \tag{2.30}$$

where the STF, leakage transfer function (LTF), and NTF are given by

$$\mathrm{STF}(z) = \frac{H_1(z)}{1 + H_1(z)}\mathrm{NCF}_1(z) \tag{2.31}$$

$$\mathrm{LTF}(z) = \frac{1}{1 + H_1(z)}\mathrm{NCF}_1(z) - \frac{H_2(z)}{1 + H_2(z)}\mathrm{NCF}_2(z) \tag{2.32}$$

$$\mathrm{NTF}(z) = \frac{1}{1 + H_2(z)}\mathrm{NCF}_2(z) \tag{2.33}$$

If the NCF transfer functions are selected as follows

$$\mathrm{NCF}_1(z) = \frac{H_2(z)}{1 + H_2(z)} \tag{2.34}$$

$$\mathrm{NCF}_2(z) = \frac{1}{1 + H_1(z)} \tag{2.35}$$

then the LTF and the NTF becomes

$$\mathrm{LTF}(z) = 0 \tag{2.36}$$

$$\mathrm{NTF}(z) = \frac{1}{1 + H_1(z)}\frac{1}{1 + H_2(z)} \tag{2.37}$$

In this case, the first-stage quantization noise is completely cancelled leaving the modulator output with the second-stage quantization noise suppressed by the NTFs of the first and the second stages and the input sequence shaped by the STF.

Fig. 2.30 shows an example fourth-order NTFs comparison with optimized and DC zeros. The fourth-order NTF with optimized zeros, which is used as an example in the previous subsections, has 47.6 dB of quantization noise suppresion for an OSR of 10 and 7.0 dB of feedbacked quantization noise amplification factor. The fourth-order NTF with DC zeros has 49.9 dB of quantization noise suppression for an OSR of 10. If the fourth-order NTF with DC zeros is implemented with a cascade of two

second-order ΣΔ modulator or a MASH 2-2 ΣΔ modulator, its stability is equivalent to a fourth-order NTF with optimized zeros since a second-order NTF with DC zeros also has 7.0 dB of feedbacked quantization noise amplification factor.

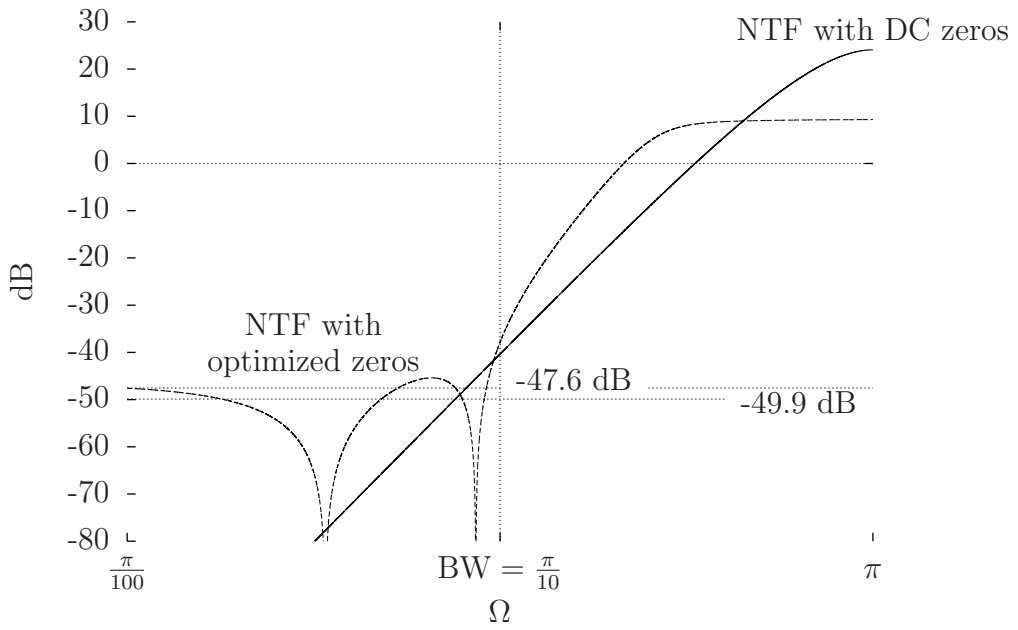


Figure 2.30: Example fourth-order NTFs comparison with optimized and DC zeros.

Besides the additional 2.3 dB of quantization noise suppression in this example, most MASH ΣΔ modulator architectures allow the use of interstage gain to further improve this specification. This can be modelled in Fig. 2.29 by amplifying the second-stage input and attenuating the second-stage output by the same factor. For example, an interstage gain of 2 V/V is popular as it can be realized efficiently on the digital domain. Higher interstage gain is possible but this might not be an efficient solution if the quantization noise performance starts to be limited by the leakage and the cost to implement this gain on the analog domain becomes prohibitive.

In addition, a MASH ΣΔ modulator has superior overload recovery compared to

a high-order single-loop ΣΔ modulator. In a high-order single-loop ΣΔ modulator, there is no guarantee that it will return to stable operation after a large input signal that overloads the modulator is removed. This situation is also applicable during startup, requiring reset and detection mechanisms if the modulator overloads. On the other hand, a first-order and a second-order ΣΔ modulators are guaranteed to be stable as long as the magnitude of the input signal is bounded [100].

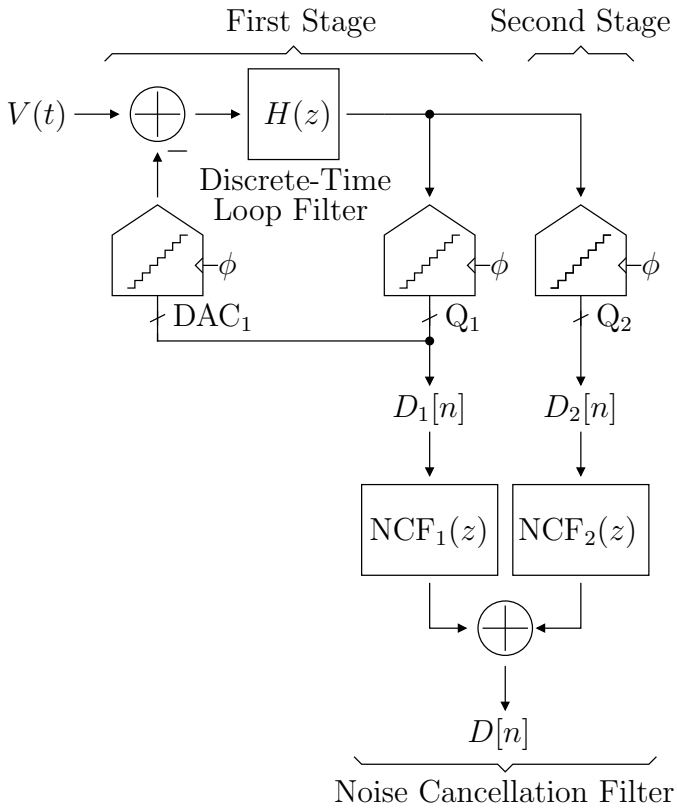


Figure 2.31: Time domain model of a MASH N-0 DTΣΔM.

Fig. 2.31 and 2.32 show the time domain models of a MASH N-0 and a MASH 0-N DTΣΔMs. These two architectures are special cases of the two-stage MASH DTΣΔM in which one of the stages is a Nyquist ADC. In the MASH N-0 ΣΔ

modulator architecture which was first introduced in [101], the second stage is implemented by a Nyquist ADC whose resolution needs to be higher than that of the first-stage quantizer. This architecture is attractive if a Nyquist ADC can be designed to be more power efficient than a $\Sigma\Delta$ modulator for the second stage with the same resolution in-band. In the MASH 0-N $\Sigma\Delta$ modulator architecture which was first introduced in [102], the first stage is implemented by a Nyquist ADC. This architecture relaxes the input signal swing processed by the second stage. However, the tonal behaviour of the first-stage quantizer and the gain matching accuracy limit its distortion performance.

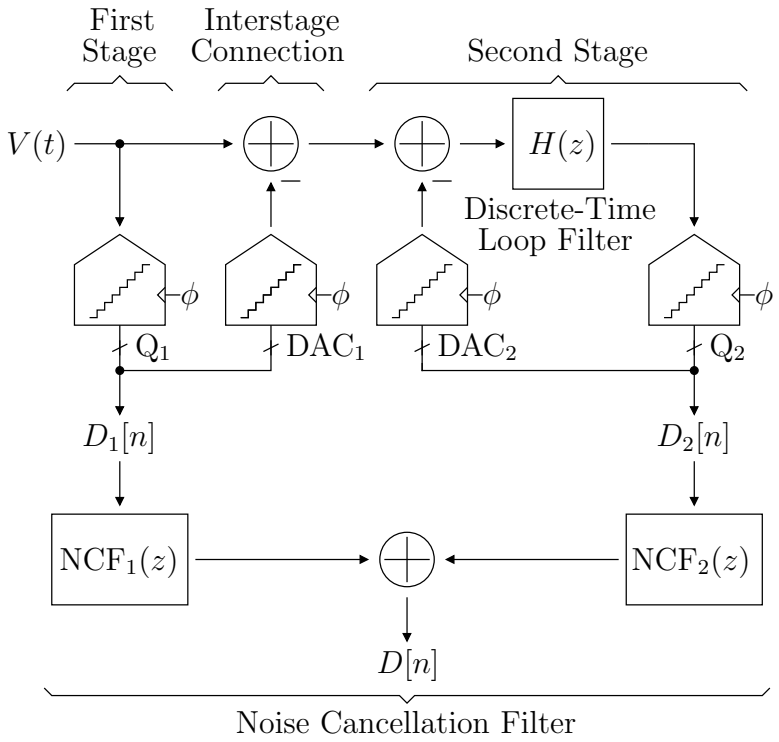


Figure 2.32: Time domain model of a MASH 0-N DT$\Sigma\Delta$M.

Another special case is the sturdy MASH (SMASH) $\Sigma\Delta$ modulator architecture

which was first introduced in [103]. Its time domain model is shown in Fig. 2.33. It is essentially a single-loop ΣΔ modulator with a MASH 0-N ΣΔ modulator as a quantizer. Thus, its robustness against quantization noise leakage is similar to that of a MASH 0-N ΣΔ modulator architecture. However, its stability is similar to that of a single-loop ΣΔ modulator architecture. Moreover, extra care is necessary to ensure that the out-of-band quantization noise from the MASH 0-N quantizer does not overload the main feedback loop.

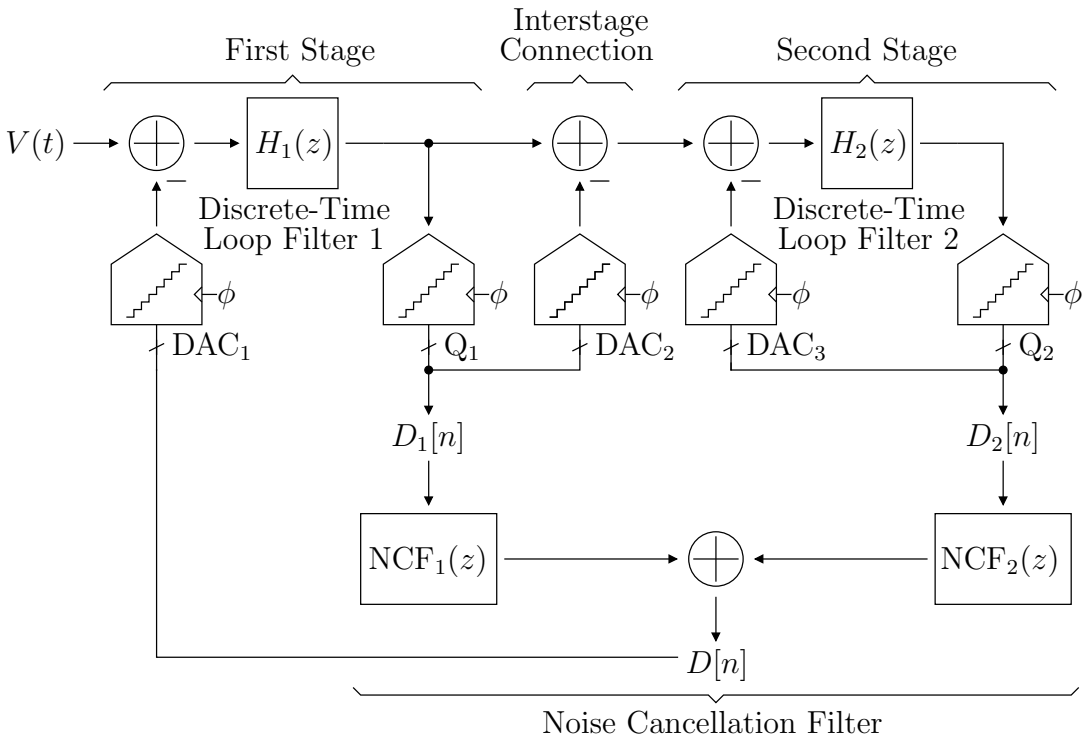


Figure 2.33: Time domain model of a SMASH DTΣΔM.

3. ARCHITECTURE SYNTHESIS

This section describes architecture synthesis of the proposed MASH 2-2 CTΣΔM. The architecture is first described and analyzed. Synthesis procedure which leads to the final design are discussed. Detailed analyses and simulation results on the effects of major non-idealities are presented.

3.1 Proposed Architecture

Fig. 3.1 shows the proposed MASH 2-2 CTΣΔM architecture. The modulator core consists of two single-loop CTΣΔM stages and an NCF. Each stage is comprised of two integrators, feedback DACs, and a quantizer. Bias and RC time constant calibration circuits provide support for each stage.

3.1.1 Proposed Single-Loop CTΣΔM Stage Architectures

Fig. 3.2 shows the first and the second stage architectures used in the proposed MASH 2-2 CTΣΔM architecture. Feedback topology is adopted to avoid out-of-band peaking of the input signal for the first stage and amplification of the first-stage quantization noise for the second stage. The loop filters are realized using an active-RC topology with digitally tunable capacitors. High gain multi-stage operational amplifiers (OAs) are implemented to satisfy both the loop filter linearity and quantization noise leakage specifications.

DAC_1 and DAC_6 provide the main feedback paths in the first and the second stages, respectively. The delay of DAC_1 is extended to two clock cycle to accomodate data weighted averaging (DWA) [104]. This extra delay is compensated by DAC_2 which also takes advantage of DWA. On the other hand, the delay of DAC_6 is kept to one clock cycle as it does not need DWA.

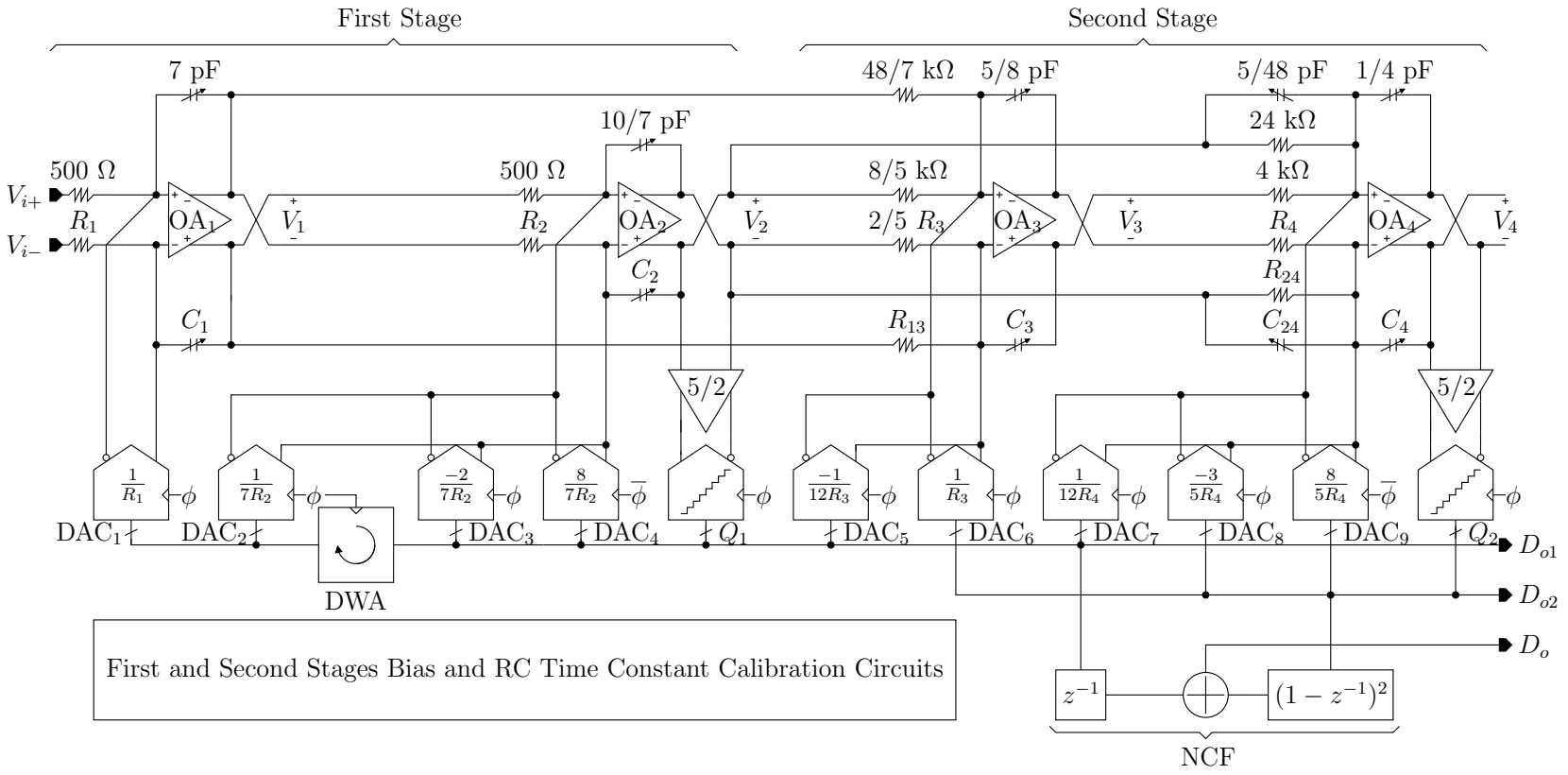
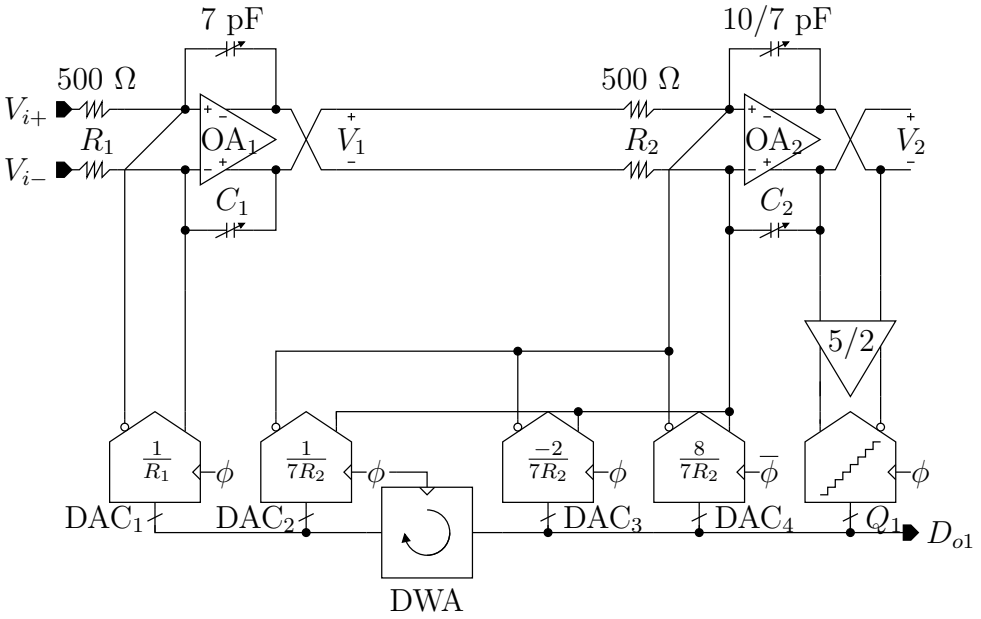
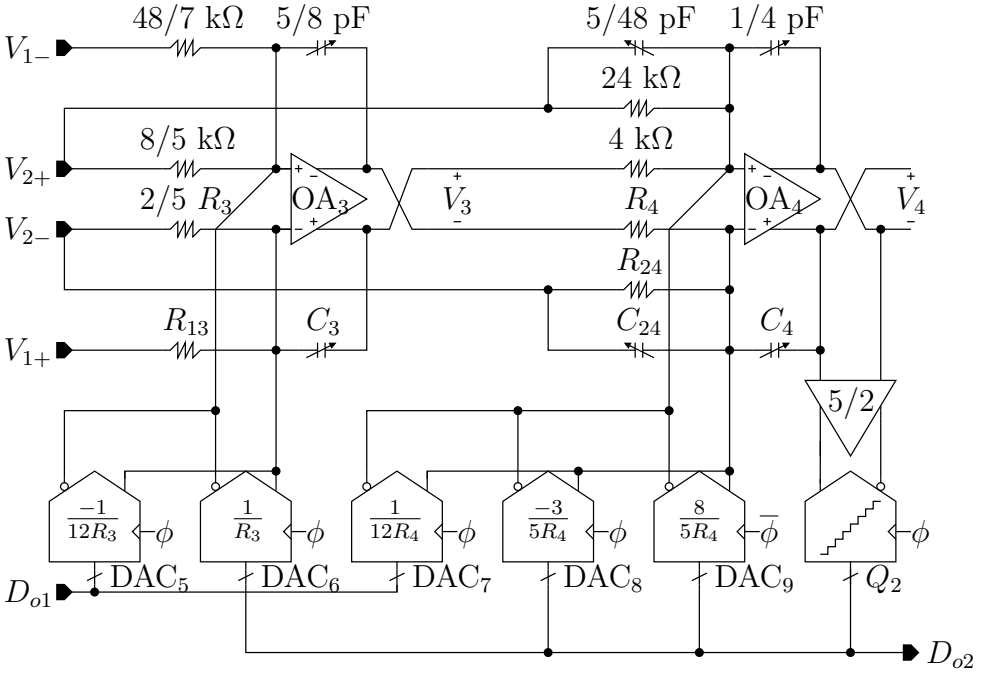


Figure 3.1: Proposed MASH 2-2 CTΣΔM architecture.



(a)



(b)

Figure 3.2: (a) First and (b) second stage architectures used in the proposed MASH 2-2 CTΣΔM architecture.

DAC_4 and DAC_3 provide the half and the one clock cycle delay feedback paths in the first stage, respectively. This ELD compensation scheme provides better power efficiency compared to using the zeroth-order feedback path [105, 106] and lower quantizer complexity compared to using the digital ELD compensation [107]. They resemble the differentiator DAC [11], but the main difference is that DAC_3 coefficient is reduced by four times which save area and power consumption. DAC_9 and DAC_8 fulfill the same roles as DAC_4 and DAC_3 in the second stage, respectively.

All DACs use the NRZ pulse shaping to reduce jitter sensitivity. Their bias currents are generated to have values inversely proportional to the values of the replica loop filter resistors to minimize quantization noise leakage.

Two four-bit flash quantizers provide an amplification factor of 2.5 V/V to reduce the signal swings and the bandwidths of the second and the fourth integrators by the same amount. This is achieved by reducing the quantizer full-scale with respect to that of the modulator [108]. Since the quantizer LSB is reduced by this technique, the offsets of the dynamic comparators used in the quantizer are calibrated to the reference voltages on startup to maintain accuracy. This also enables the quantizers to have zero analog power consumption.

3.1.2 Proposed MASH 2-2 CTΣΔM Architecture

The proposed MASH 2-2 CTΣΔM architecture relies on the accuracy of the RC time constant calibration circuits to minimize quantization noise leakage by tuning the analog loop filter transfer functions through the digitally tunable capacitors. Since an RC time constant in a modern CMOS process can vary by up to ±40 %, this type of analog calibration scheme is already a necessity for the single-loop CTΣΔM architecture to maintain stability over process corners. Therefore, it is implemented in this design with improved accuracy to also satisfy the quantization

noise leakage specification. The analog calibration scheme is preferred compared to the digital correction of modulator output [7, 92] which is too power hungry to implement at high sampling frequency. Compared to the analog calibration schemes used in prior designs [109, 28], the calibration algorithm used in this design is more power efficient, simple to implement, and compatible with background operation.

The interstage connection of the proposed MASH 2-2 CTΣΔM architecture is implemented by the main interstage path through R_3 and five additional feedforward interstage paths through R_{13}, R_{24}, C_{24}, DAC_5, and DAC_7. Without these additional paths, the second stage needs to process the input signal without any attenuation and the NCF needed to cancel the first-stage quantization noise is complex [28]. Even though the in-band input signal processed by the second stage can be cancelled using DAC_5 [7, 109], this leads to out-of-band peaking of the input signal and the first-stage quantization noise at the second-stage output. This out-of-band peaking can be solved by minimizing DAC_5 delay or implementing an analog delay in the main interstage path [69, 81, 92]. Compared to these solutions, the additional feedforward interstage paths reduce the input signal swings at the second-stage integrator outputs without any out-of-band peaking. Furthermore, these paths are relatively weak and do not load the second stage.

3.2 Analysis

Fig. 3.3 shows the proposed MASH 2-2 CTΣΔM time domain model as a starting point for analysis.

Table 3.1 shows the impulse invariant transform analyses of the loop gains of the first and the second stages used in the proposed MASH 2-2 CTΣΔM. The loop gain of each stage is a superposition of the loop gain of each cascade interconnection of a DAC and a part of the continuous-time loop filter.

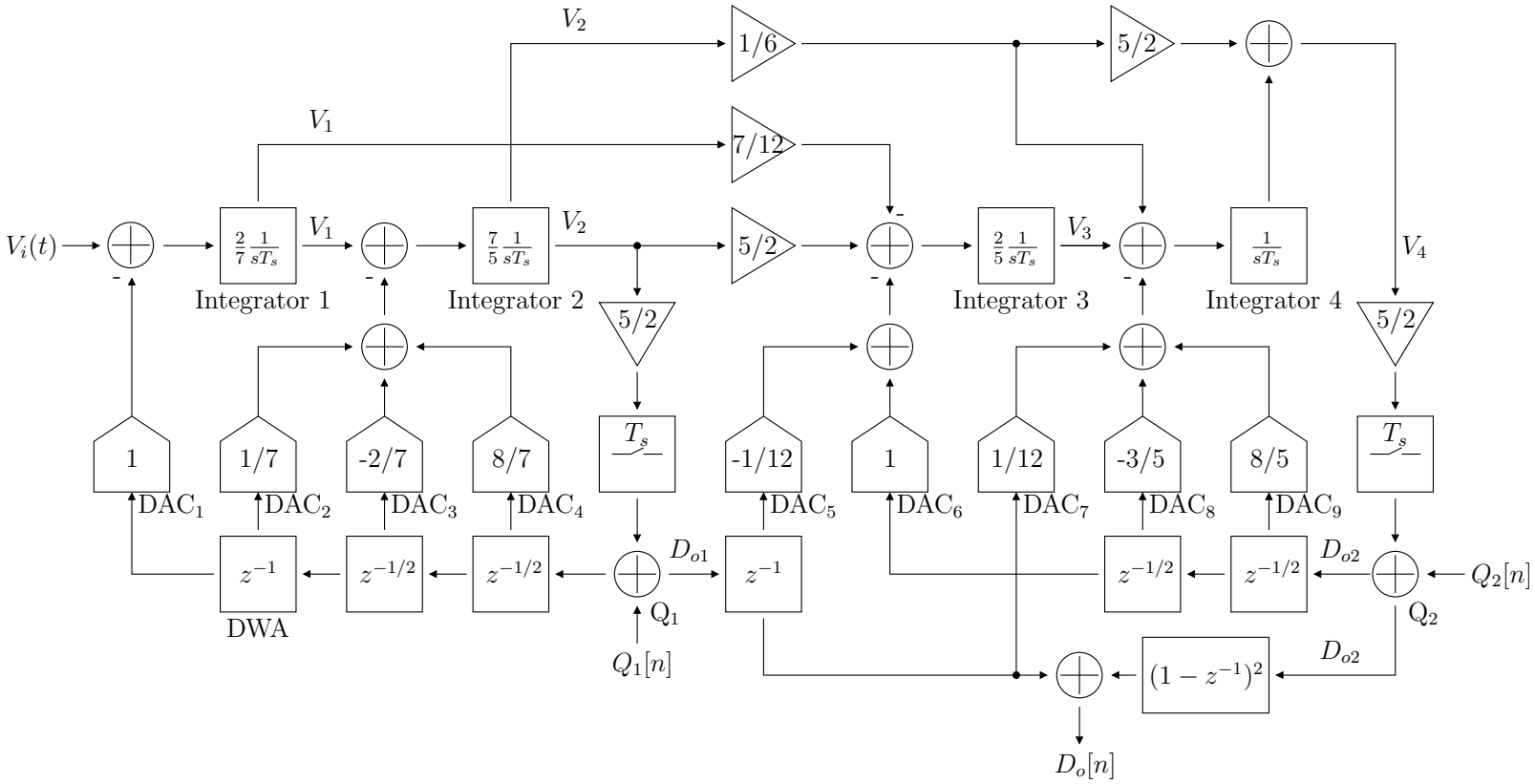


Figure 3.3: Proposed MASH 2-2 CTΣΔM time domain model.

Table 3.1: Impulse invariant transform analyses of the loop gains of the first and the second stages used in the proposed MASH 2-2 CTΣΔM.

DAC	z	$H(s)$	$H(z)$
DAC_1	z^{-2}	$\frac{1}{s^2T_s^2}$	$\frac{1}{2}\frac{z^{-3}+z^{-4}}{(1-z^{-1})^2}$
DAC_2	z^{-2}	$\frac{1}{2}\frac{1}{sT_s}$	$\frac{1}{2}\frac{z^{-3}}{1-z^{-1}}$
DAC_3	z^{-1}	$-\frac{1}{sT_s}$	$-\frac{z^{-2}}{1-z^{-1}}$
DAC_4	$z^{-1/2}$	$\frac{4}{sT_s}$	$\frac{2(z^{-1}+z^{-2})}{1-z^{-1}}$
$H_1(z)$ (Total)			$\frac{2z^{-1}-z^{-2}}{(1-z^{-1})^2}$

DAC	z	$H(s)$	$H(z)$
DAC_6	z^{-1}	$\frac{1}{s^2T_s^2}$	$\frac{1}{2}\frac{z^{-2}+z^{-3}}{(1-z^{-1})^2}$
DAC_8	z^{-1}	$-\frac{3}{2}\frac{1}{sT_s}$	$-\frac{3}{2}\frac{z^{-2}}{1-z^{-1}}$
DAC_9	$z^{-1/2}$	$\frac{4}{sT_s}$	$\frac{2(z^{-1}+z^{-2})}{1-z^{-1}}$
$H_2(z)$ (Total)			$\frac{2z^{-1}-z^{-2}}{(1-z^{-1})^2}$

Fig. 3.4 shows the bode plot of the first and the second stages used in the proposed MASH 2-2 CTΣΔM. Both stages implement a second-order NTF with DC zeros. The gain margin is -2.5 dB. The phase margin is 23.9 ^{o}.

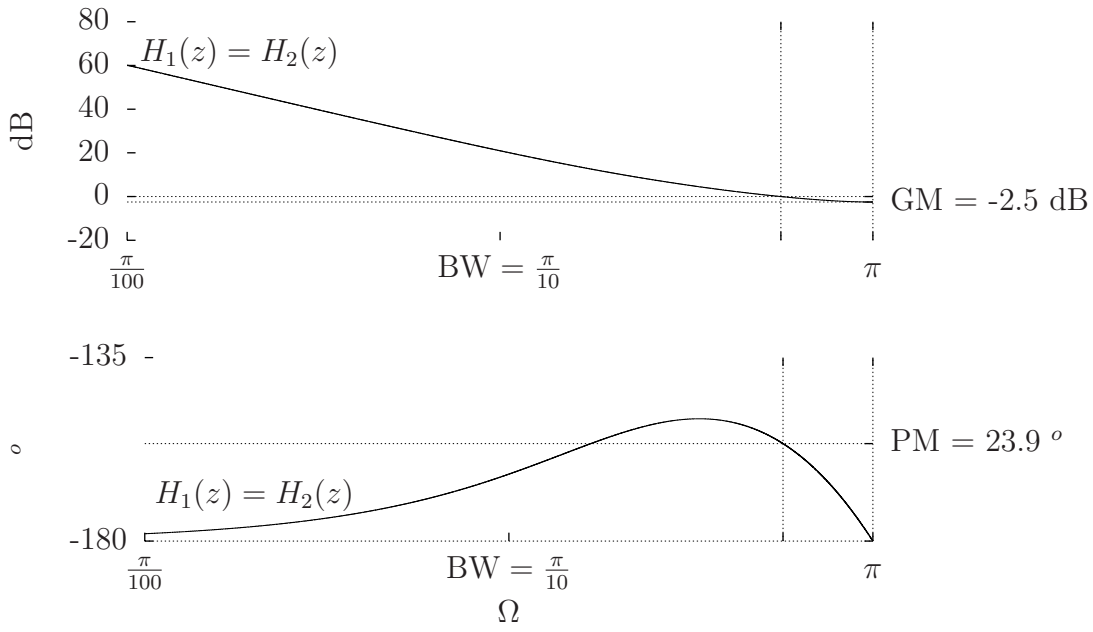


Figure 3.4: Bode plot of the first and the second stages used in the proposed MASH 2-2 CTΣΔM.

Fig. 3.5 shows the root locus plot of the first and the second stages used in the proposed MASH 2-2 CTΣΔM vs quantizer gain k from 1.25 to 3.75. The nominal quantizer gain is 2.5 V/V. One pole of the NTF goes outside the unit circle for $k > 3.335$ which corresponds to gain margin of -2.5 dB in Bode plot analysis.

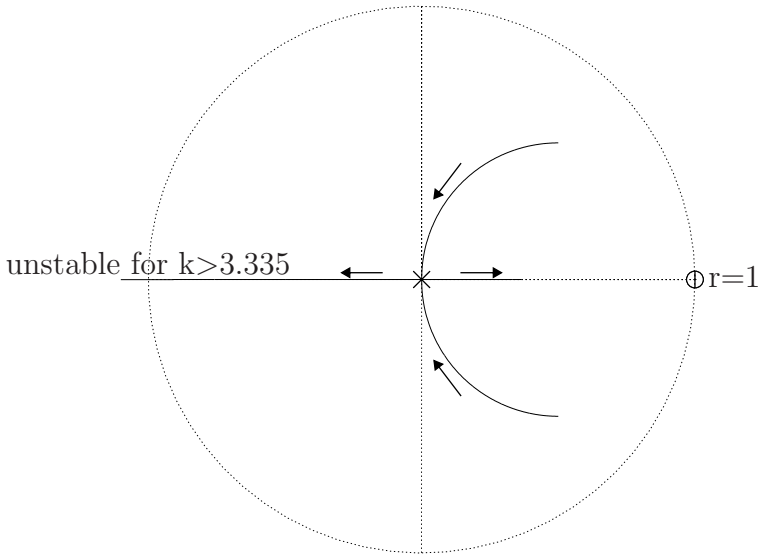


Figure 3.5: Root locus plot of the first and the second stages used in the proposed MASH 2-2 CTΣΔM vs quantizer gain k from 1.25 to 3.75.

Table 3.2 shows the impulse invariant transform analysis of the interstage loop gain of the proposed MASH 2-2 CTΣΔM. It derives the equivalent discrete-time open-loop loop filter transfer function $H_{12}(z)$ from the first-stage output D_{o1} to the second-stage output D_{o2}.

The results of impulse invariant transform analyses can be used to simplify the proposed MASH 2-2 CTΣΔM time domain model as shown in Fig. 3.6.

Table 3.2: Impulse invariant transform analysis of the interstage loop gain of the proposed MASH 2-2 CTΣΔM.

DAC	z	$H(s)$	$H(z)$
DAC_1	z^{-2}	$\frac{1}{s^4T_s^4} + \frac{5}{12}\frac{1}{s^2T_s^2}$	$\frac{1}{4}\frac{z^{-3}+z^{-4}+z^{-5}+z^{-6}}{(1-z^{-1})^4}$
DAC_2	z^{-2}	$\frac{1}{2}\frac{1}{s^3T_s^3} + \frac{1}{12}\frac{1}{s^2T_s^2} + \frac{5}{24}\frac{1}{sT_s}$	$\frac{1}{12}\frac{4z^{-3}-z^{-4}+3z^{-5}}{(1-z^{-1})^3}$
DAC_3	z^{-1}	$-\frac{1}{s^3T_s^3} - \frac{1}{6}\frac{1}{s^2T_s^2} - \frac{10}{24}\frac{1}{sT_s}$	$-\frac{1}{6}\frac{4z^{-2}-z^{-3}+3z^{-4}}{(1-z^{-1})^3}$
DAC_4	$z^{-1/2}$	$\frac{4}{s^3T_s^3} + \frac{2}{3}\frac{1}{s^2T_s^2} + \frac{5}{3}\frac{1}{sT_s}$	$\frac{1}{6}\frac{6z^{-1}+9z^{-2}+4z^{-3}+5z^{-4}}{(1-z^{-1})^3}$
DAC_5	z^{-1}	$-\frac{1}{12}\frac{1}{s^2T_s^2}$	$-\frac{1}{24}\frac{z^{-2}+z^{-3}}{(1-z^{-1})^2}$
DAC_7	z^{-1}	$\frac{5}{24}\frac{1}{sT_s}$	$\frac{5}{24}\frac{z^{-2}}{1-z^{-1}}$
$H_{12}(z)$ (Total)			$\frac{z^{-1}}{(1-z^{-1})^4}$

The STF, the LTF, and the NTF are given by

$$\mathrm{STF}(j\omega) = \left(\frac{1}{(j\omega T_s)^4} + \frac{5}{12}\frac{1}{(j\omega T_s)^2}\right) \times (1 - e^{j\omega T_s})^4 \tag{3.1}$$

$$\mathrm{LTF}(z) = 0 \tag{3.2}$$

$$\mathrm{NTF}(z) = (1 - z^{-1})^4 \tag{3.3}$$

whereas the STFs and the NTFs of the first and the second stages are given by

$$\mathrm{STF}_1(j\omega) = \frac{(1 - e^{j\omega T_s})^2}{(j\omega T_s)^2} \tag{3.4}$$

$$\mathrm{STF}_2(j\omega) = \left(\frac{1}{(j\omega T_s)^4} + \frac{5}{12}\frac{1}{(j\omega T_s)^2}\right) \times (1 - e^{j\omega T_s})^2 - \frac{e^{-j\omega T_s}}{(j\omega T_s)^2} \tag{3.5}$$

$$\mathrm{NTF}_1(z) = (1 - z^{-1})^2 \tag{3.6}$$

$$\mathrm{NTF}_2(z) = (1 - z^{-1})^2 \tag{3.7}$$

$$\mathrm{NTF}_{12}(z) = -z^{-1} \tag{3.8}$$

These equations show that the proposed MASH 2-2 CTΣΔM implement a fourth-order NTF with DC zeros. Systematic leakage of the first-stage quantization noise is

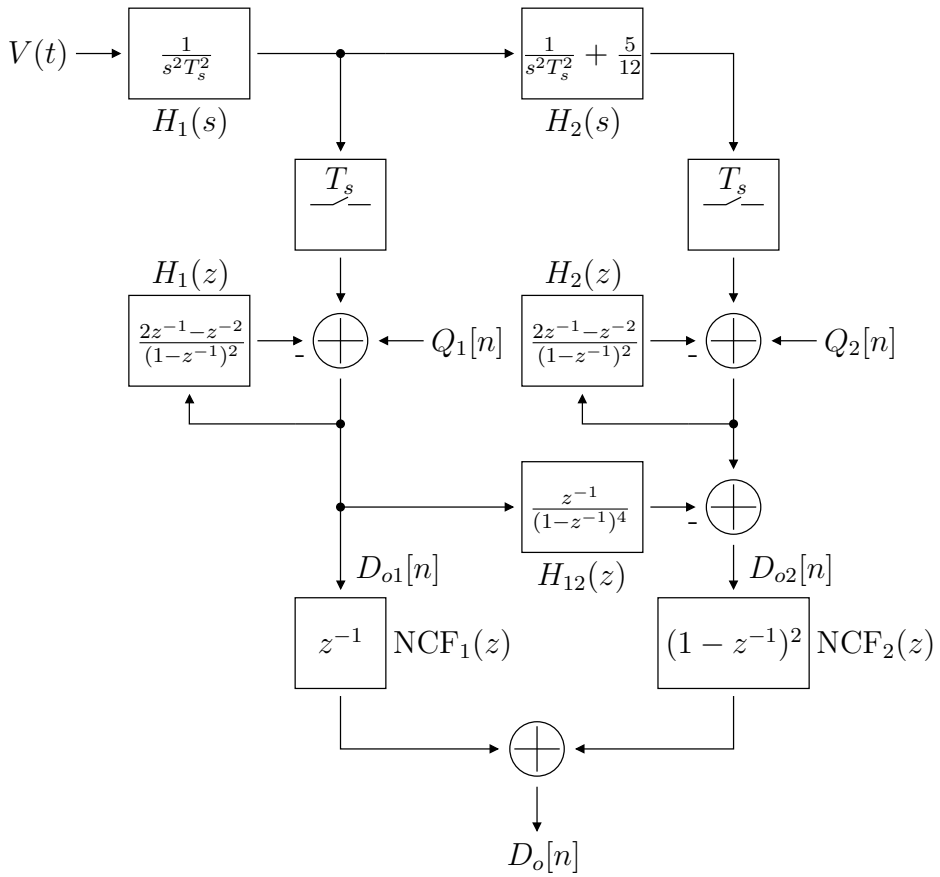
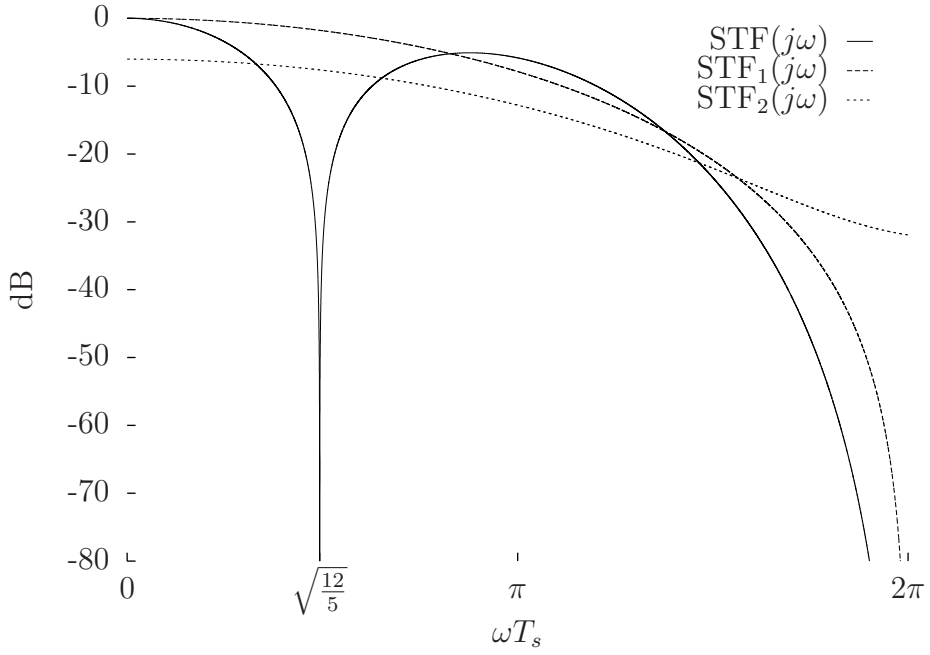


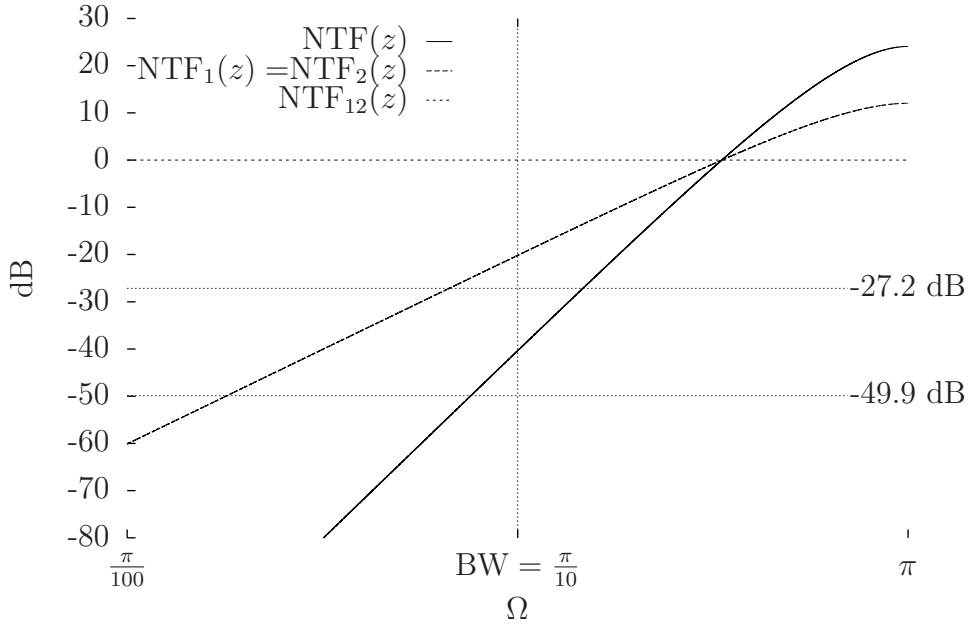
Figure 3.6: Proposed MASH 2-2 CTΣΔM simplified time domain model.

eliminated. Thanks to the additional feedforward interstage paths, the second stage simply processes the inverted delayed version of the first-stage quantization noise. They also greatly simplify the NCF transfer functions.

Fig. 3.7a shows the STFs of the proposed MASH 2-2 CTΣΔM. The STFs are free from out-of-band peaking. The modulator STF possesses a notch located at $\omega T_s = \sqrt{12/5}$ generated by the second-order feedforward interstage path through C_{24} and the cancellation of the third-order feedforward interstage paths through R_{13} and R_{24}. The input signal swing at the second-stage output is reduced by half compared to those in the first-stage and the modulator outputs.



(a)



(b)

Figure 3.7: (a) STFs and (b) NTFs of the proposed MASH 2-2 CTΣΔM.

Fig. 3.7b show the NTFs of the proposed MASH 2-2 CTΣΔM. The quantization noise suppressions provided by the second-order and the fourth-order NTFs with DC zeros are 27.2 dB and 49.9 dB, respectively, for an OSR of 10. With four-bit quantizers used in both stages, the quantization noise floors at the first-stage and the modulator outputs are −63.0 dBFS and −85.7 dBFS, respectively. The interstage NTF denoted as $\mathrm{NTF}_{12}(z)$, which is the transfer function from the first-stage quantization noise to the second-stage output, has a flat 0 dB of gain.

Fig. 3.8 show the SQNR vs sinusoid input signal amplitude of the proposed MASH 2-2 CTΣΔM. The DR is 85.5 dB. The quantization noise floor is −85.5 dBFS, which is very close to the theoretical quantization noise floor of −85.7 dBFS. The peak SQNR is 85.2 dB which occurs at an input amplitude of −0.7 dBFS. The MSA is −0.6 dBFS.

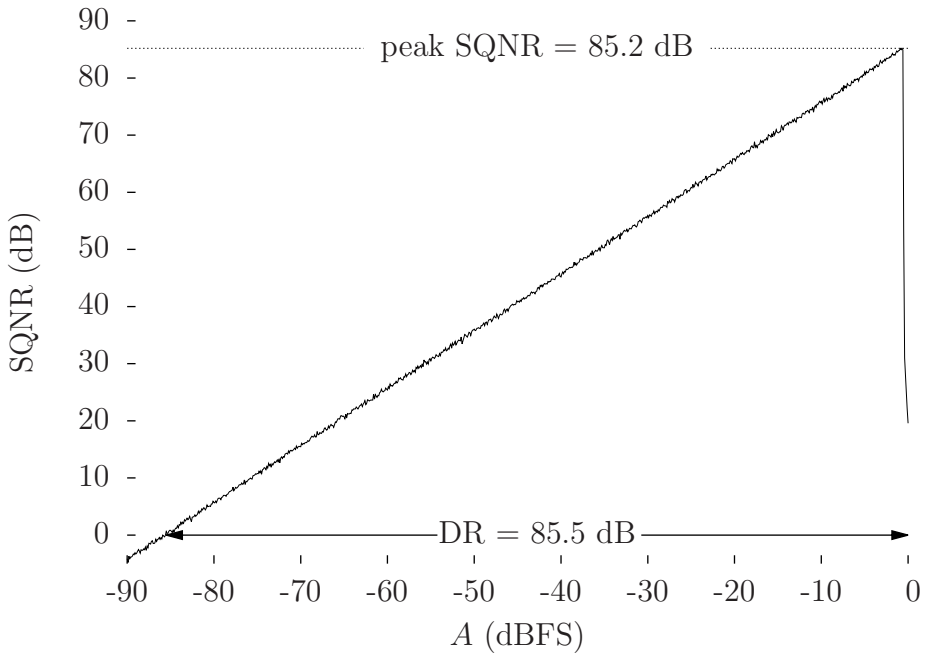


Figure 3.8: SQNR vs sinusoid input signal amplitude of the proposed MASH 2-2 CTΣΔM.

Fig. 3.9 shows the modulator output sequence and FFT spectrum of the proposed MASH 2-2 CTΣΔM at peak SQNR condition. The simulated quantization noise spectrum follows the fourth-order noise-shaping behaviour predicted by the theory in (3.3) and shown in Fig. 3.9 using a white line.

Fig. 3.10 shows the first and the second stages output sequences and FFT spectrums of the proposed MASH 2-2 CTΣΔM at peak SQNR condition. The SQNR at the first-stage output is 53.9 dB, which differs significantly compared to the predicted theoretical value of 62.3 dB. At close inspection, tones can be observed at the output spectrums of both stages since the first stage is very close to the overload condition at this input amplitude of −0.7 dBFS. Thanks to the second stage, these tones are cancelled and not visible at the modulator output. Quantization noise and distortion cancellation of 31.3 dB is observed.

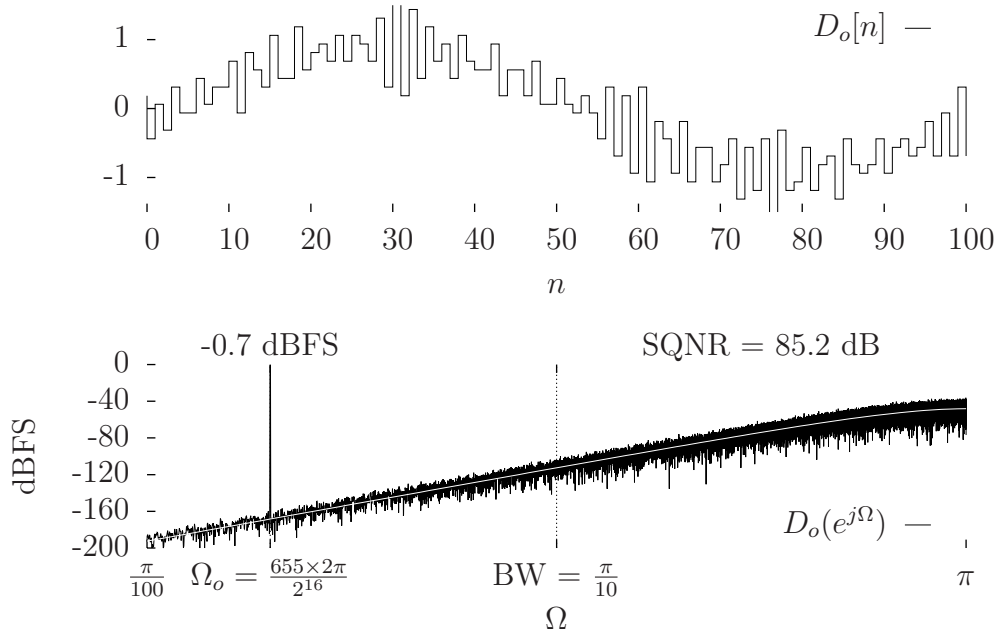


Figure 3.9: Modulator output sequence and FFT spectrum of the proposed MASH 2-2 CTΣΔM at peak SQNR condition.

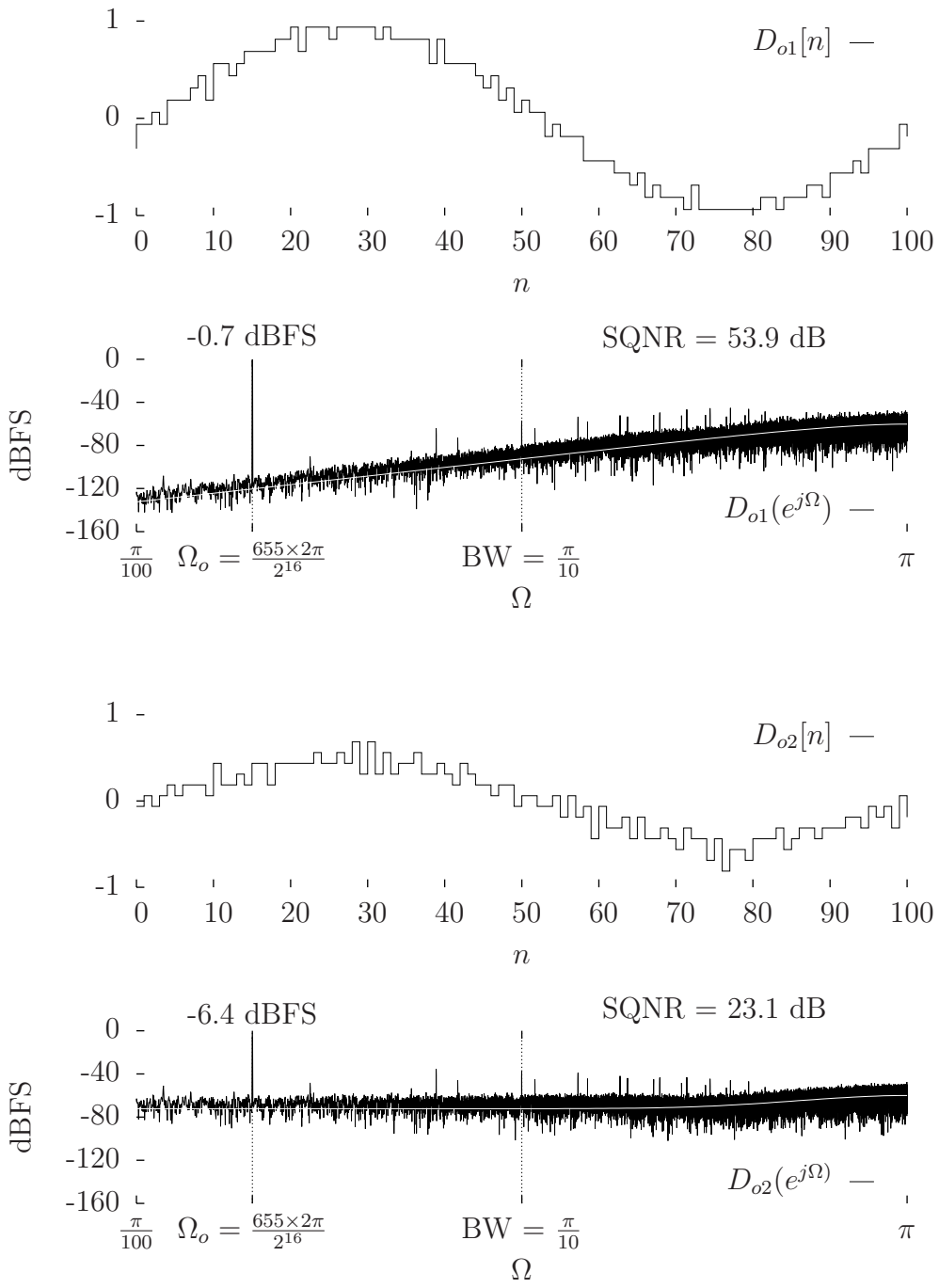


Figure 3.10: First and second stages output sequences and FFT spectrums of the proposed MASH 2-2 CTΣΔM at peak SQNR condition.

To analyze the signal swings at the integrator outputs, the following equations can be written by referring to the time domain model in Fig. 3.3.

$$V_1(j\omega) = \frac{2}{7}\frac{V_i(j\omega)}{j\omega T_s} - \frac{2}{7}e^{-2j\omega T_s}\frac{V_{o1}(j\omega)}{j\omega T_s} \tag{3.9}$$

$$V_2(j\omega) = \frac{7}{5}\frac{V_1(j\omega)}{j\omega T_s} - \frac{1}{5}\left(2e^{-2j\omega T_s} - 3e^{-j\omega T_s} + 8e^{-j\omega T_s/2}\right)\frac{V_{o1}(j\omega)}{j\omega T_s} \tag{3.10}$$

$$V_3(j\omega) = \frac{V_2(j\omega)}{j\omega T_s} - \frac{7}{30}\frac{V_1(j\omega)}{j\omega T_s} + \frac{1}{30}e^{-j\omega T_s}\frac{V_{o1}(j\omega)}{j\omega T_s} - \frac{2}{5}e^{-j\omega T_s}\frac{V_{o2}(j\omega)}{j\omega T_s} \tag{3.11}$$

$$\begin{aligned} V_4(j\omega) = {} & \frac{V_3(j\omega)}{j\omega T_s} + \frac{1}{6}\frac{V_2(j\omega)}{j\omega T_s} + \frac{5}{12}V_2(j\omega) - \frac{1}{12}e^{-j\omega T_s}\frac{V_{o1}(j\omega)}{j\omega T_s} \\ & - \frac{1}{5}\left(-3e^{-j\omega T_s} + 8e^{-j\omega T_s/2}\right)\frac{V_{o2}(j\omega)}{j\omega T_s} \end{aligned} \tag{3.12}$$

where $V_{o1}(j\omega)$ and $V_{o2}(j\omega)$ are the first-stage and the second-stage continuous-time output spectrums which are the results of reconstruction operations performed by the NRZ DACs.

The reconstructed input spectrum at the first-stage and the second-stage continuous-time outputs are given by

$$V_{o1}(j\omega)|_{Q_1=Q_2=0} = \frac{1-e^{-j\omega T_s}}{j\omega T_s}\sum_{k=-\infty}^{\infty}\mathrm{STF}_1\left(j\omega - j\frac{2\pi k}{T_s}\right)V_i\left(j\omega - j\frac{2\pi k}{T_s}\right) \tag{3.13}$$

$$V_{o2}(j\omega)|_{Q_1=Q_2=0} = \frac{1-e^{-j\omega T_s}}{j\omega T_s}\sum_{k=-\infty}^{\infty}\mathrm{STF}_2\left(j\omega - j\frac{2\pi k}{T_s}\right)V_i\left(j\omega - j\frac{2\pi k}{T_s}\right) \tag{3.14}$$

The reconstructed quantization noise PSD at the first-stage and the second-stage continuous-time outputs are given by

$$|V_{o1}(j\omega)|^2|_{V_i=0} = \overline{Q_1^2}T_s \times |\mathrm{NTF}_1(e^{j\omega T_s})|^2 \times \frac{1}{T_s^2}\left|\frac{1-e^{-j\omega T_s}}{j\omega}\right|^2 \tag{3.15}$$

$$\begin{aligned} |V_{o2}(j\omega)|^2|_{V_i=0} = {} & \left(\overline{Q_1^2}T_s \times |\mathrm{NTF}_{12}(e^{j\omega T_s})|^2 + \overline{Q_2^2}T_s \times |\mathrm{NTF}_2(e^{j\omega T_s})|^2\right) \\ & \times \frac{1}{T_s^2}\left|\frac{1-e^{-j\omega T_s}}{j\omega}\right|^2 \end{aligned} \tag{3.16}$$

The theoretical continuous-time spectrums at the integrator outputs can be plotted using (3.9) to (3.16). However, it is more convenient in simulation to obtain the discrete-time spectrums by applying FFTs at the sampled integrator outputs. Using impulse invariant transform analysis, the sampled integrator outputs are of the form

$$V_m(e^{j\Omega}) = \sum_{k=-\infty}^{\infty} \mathrm{ISTF}_m(j\omega)V_i(j\omega)|_{\omega=\frac{\Omega}{T_s}-\frac{2\pi k}{T_s}} + \mathrm{INTF}_{1m}(e^{j\Omega})Q_1(e^{j\Omega}) + \mathrm{INTF}_{2m}(e^{j\Omega})Q_2(e^{j\Omega}) \tag{3.17}$$

where m is the integrator index from one to four. The discrete-time integrator output spectrum contains the sampled input spectrum shaped by the integrator STF and the quantization noise spectrums shaped by the integrator NTFs.

The integrator STFs are given by

$$\mathrm{ISTF}_1(j\omega) = \frac{2}{7}\frac{1}{j\omega T_s} - \frac{2}{7}\frac{e^{-3j\omega T_s}}{1-e^{-j\omega T_s}}\mathrm{STF}_1(j\omega) \tag{3.18}$$

$$\mathrm{ISTF}_2(j\omega) = \frac{2}{5}\mathrm{STF}_1(j\omega) \tag{3.19}$$

$$\begin{aligned}\mathrm{ISTF}_3(j\omega) = {} & \frac{2}{5}\frac{1}{(j\omega T_s)^3} - \frac{1}{15}\frac{1}{(j\omega T_s)^2} \\ & - \frac{1}{30}\frac{6e^{-j\omega T_s}+23e^{-2j\omega T_s}-24e^{-3j\omega T_s}+7e^{-4j\omega T_s}}{(1-e^{-j\omega T_s})^3}\mathrm{STF}_1(j\omega) \\ & - \frac{2}{5}\frac{e^{-2j\omega T_s}}{(1-e^{-j\omega T_s})^2}\mathrm{STF}_2(j\omega)\end{aligned} \tag{3.20}$$

$$\mathrm{ISTF}_4(j\omega) = \frac{2}{5}\mathrm{STF}_2(j\omega) \tag{3.21}$$

Fig. 3.11 shows the simulated STFs and integrator STFs of the proposed MASH 2-2 CTΣΔM. Theoretical predictions are shown using white lines. The in-band input signal swings at the first through the fourth integrator outputs are 0 dB, −8 dB, −5.7 dB, and −14.0 dB, respectively. No out-of-band STF peaking is observed.

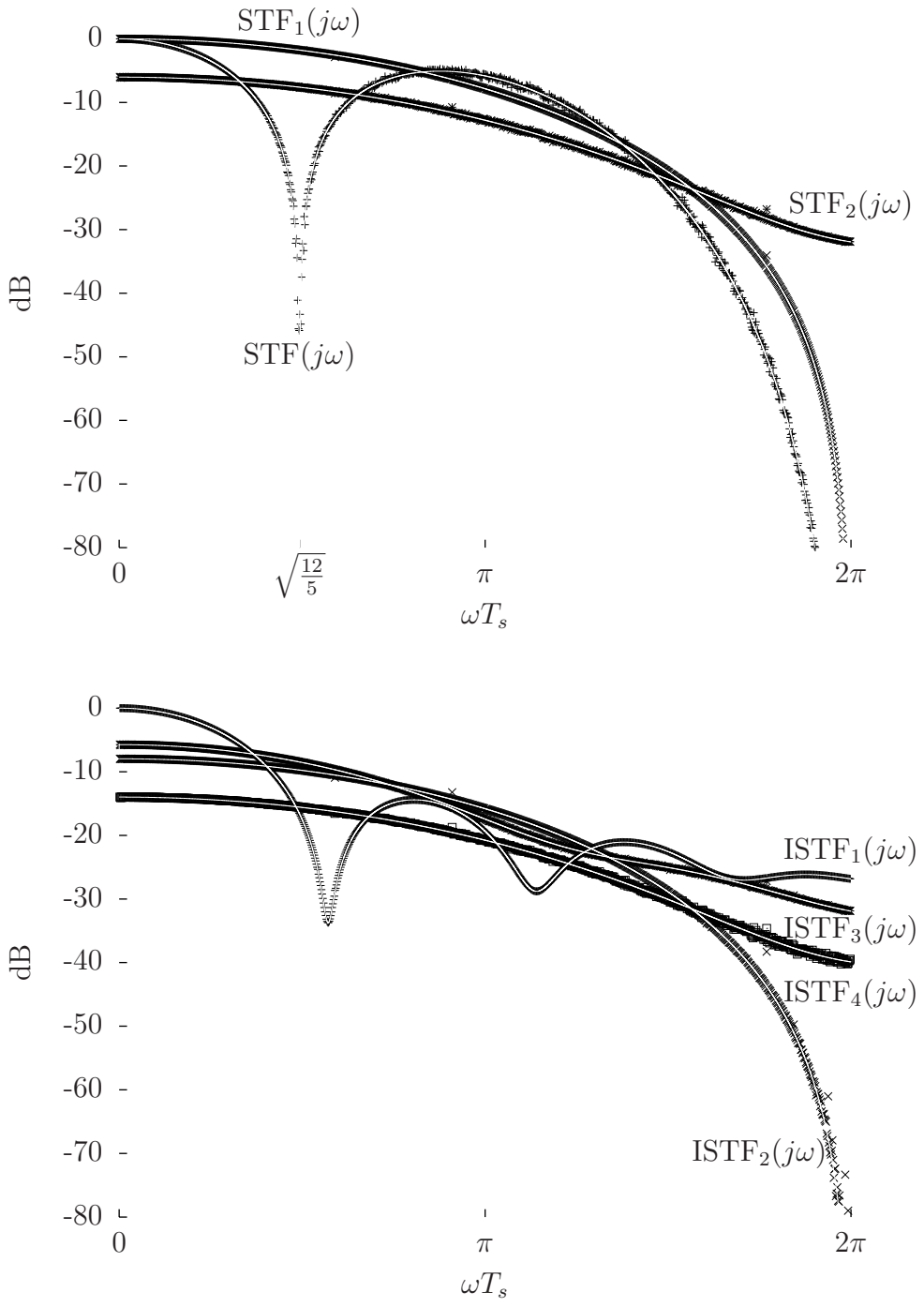


Figure 3.11: Simulated STFs and integrator STFs of the proposed MASH 2-2 CTΣΔM.

The integrator NTFs for the first-stage quantization noise are given by

$$\mathrm{INTF}_{11}(z) = -\frac{2}{7}\frac{z^{-3}}{1-z^{-1}}\mathrm{NTF}_1(z) \tag{3.22}$$

$$\mathrm{INTF}_{12}(z) = \frac{2}{5}\left(\mathrm{NTF}_1(z) - 1\right) \tag{3.23}$$

$$\begin{aligned}\mathrm{INTF}_{13}(z) = &-\frac{1}{60}\frac{12z^{-1}+43z^{-2}-42z^{-3}+11z^{-4}}{(1-z^{-1})^3}\mathrm{NTF}_1(z) \\ &-\frac{2}{5}\frac{z^{-2}}{(1-z^{-1})}\mathrm{NTF}_{12}(z)\end{aligned} \tag{3.24}$$

$$\mathrm{INTF}_{14}(z) = \frac{2}{5}\mathrm{NTF}_{12}(z) \tag{3.25}$$

The integrator NTFs for the second-stage quantization noise are given by

$$\mathrm{INTF}_{21}(z) = 0 \tag{3.26}$$

$$\mathrm{INTF}_{22}(z) = 0 \tag{3.27}$$

$$\mathrm{INTF}_{23}(z) = -\frac{2}{5}\frac{z^{-2}}{(1-z^{-1})}\mathrm{NTF}_2(z) \tag{3.28}$$

$$\mathrm{INTF}_{24}(z) = \frac{2}{5}\left(\mathrm{NTF}_2(z) - 1\right) \tag{3.29}$$

Fig. 3.12 and Fig. 3.13 show the first through the fourth integrator output sequences and FFT spectrums of the proposed MASH 2-2 CTΣΔM at peak SQNR condition. The integrator output signals are sampled at the same sampling instances of the quantizers which is the assumption behind the derivation of (3.17) to (3.29). The simulated quantization noise spectrums agree with the theoretical results derived in (3.22) to (3.29) and shown in Fig. 3.12 and Fig. 3.13 using white lines. No out-of-band quantization noise peaking is observed. The second-stage is not prone to overload from processing the first-stage quantization noise.

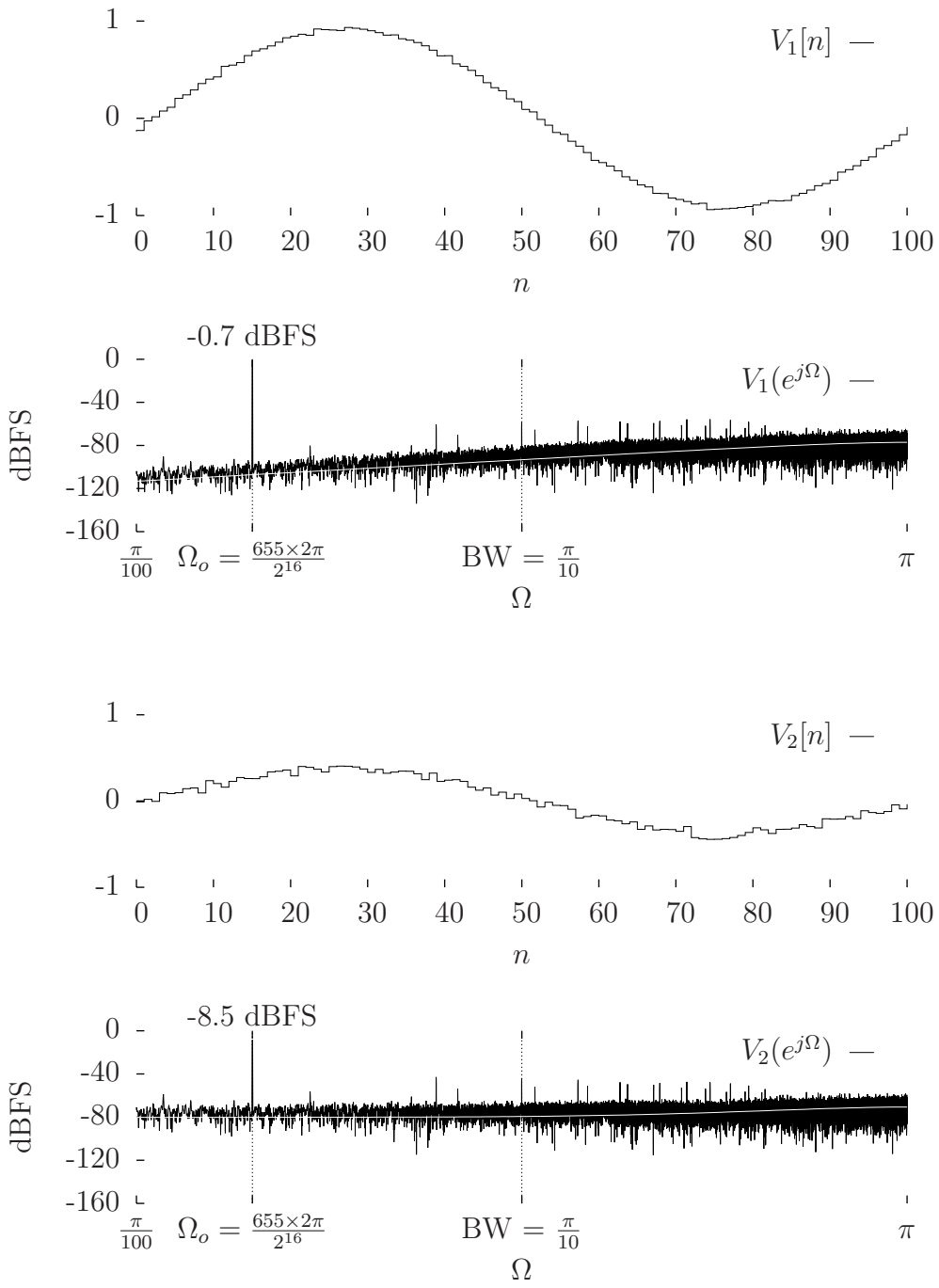


Figure 3.12: First and second integrator output sequences and FFT spectrums of the proposed MASH 2-2 CTΣΔM at peak SQNR condition.

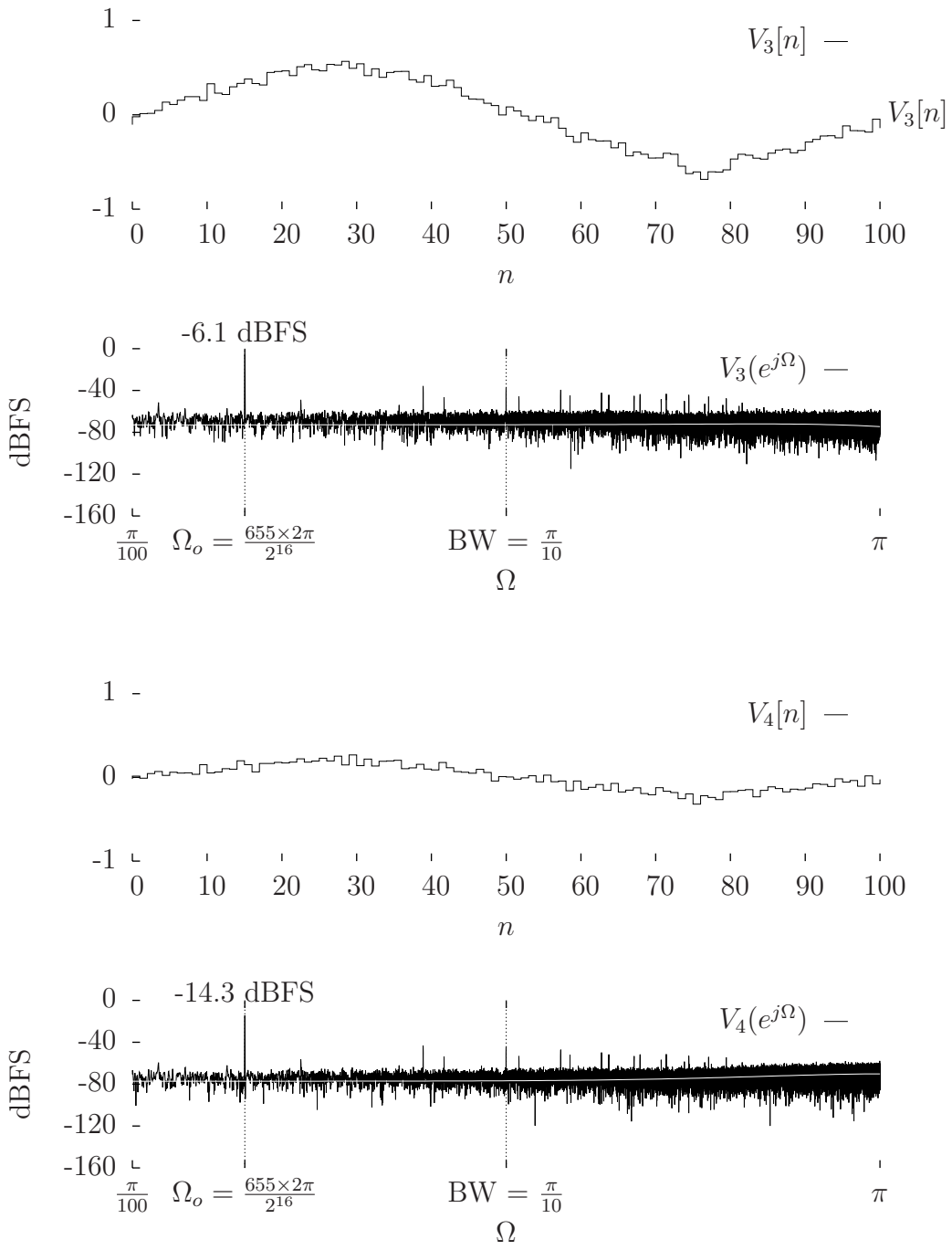


Figure 3.13: Third and fourth integrator output sequences and FFT spectrums of the proposed MASH 2-2 CTΣΔM at peak SQNR condition.

3.3 Synthesis Procedure

To arrive at the chosen feedforward interstage paths, various permutations of the MASH 2-2 CTΣΔM architecture were synthesized. The design options considered were: (i) four loop filter feedforward interstage paths, one of which is the unused resistive connection from the first-integrator output to the fourth-integrator input, (ii) two interstage DACs from the first-stage output to the second-stage integrator inputs with a one, a one and a half, or two clock cycle delays, and (iii) delay from the first-stage output to the modulator output of one or two clock cycles.

For every option, the feedforward interstage path coefficients were obtained using impulse invariant transform analysis to eliminate the systematic first-stage quantization noise leakage with simple NCF transfer functions. All of the candidates were analyzed and compared based on the input signal swings present at the second-stage integrator outputs and the value of the coefficients for ease of implementation.

The five additional feedforward interstage paths are necessary to constraint the NCF transfer functions. To add constraint for either or both the in-band input signal swings at the second-stage integrator outputs, up to two extra design variables are necessary. Unlike [110], this is not pursued further in this design due to the added design complexity and the lack of constraints on the out-of-band input signal swings.

An improved topology is obtained by adding a feedforward resistive path from the modulator input to the second-integrator input that cancels the second-order feedforward path through C_{24}. In this case, the in-band input signal swings at the third-integrator and the second-stage outputs are -20.0 dB and -21.6 dB, respectively. Thus, an interstage gain can be used to reduce the second-stage quantization noise floor. As this design allocates a quantization noise leakage budget for a safe measure, this modification is not necessary. It can be attractive for future designs.

3.4 Non-Idealities

In this section, the effects of non-idealities such as circuit thermal noise, DAC clock jitter, DAC mismatch, and process variations are analyzed. These non-idealities are important as they limit the performance of the proposed MASH 2-2 CTΣΔM.

3.4.1 Circuit Thermal Noise

Table 3.3 shows the impulse invariant transform analysis of circuit thermal noise of the proposed MASH 2-2 CTΣΔM. It derives the square magnitudes of the open-loop equivalent discrete-time NTFs from each integrator input to the second-stage output using Table A.1 in appendix A as a reference.

Table 3.3: Impulse invariant transform analysis of circuit thermal noise of the proposed MASH 2-2 CTΣΔM.

R	$H(s)$	$\lvert H(z)\rvert^2$
R_1	$\frac{1}{s^4T_s^4} + \frac{5}{12}\frac{1}{s^2T_s^2}$	$\frac{1091z^{-1}+5760z^{-2}+2421z^{-3}+11696z^{-4}+2421z^{-5}+5760z^{-6}+1091z^{-7}}{30240(1-z^{-1})^8}$
R_2	$\frac{7}{2}\frac{1}{s^3T_s^3} + \frac{7}{12}\frac{1}{s^2T_s^2} + \frac{35}{24}\frac{1}{sT_s}$	$-\frac{49}{8640}\frac{683z^{-1}-452z^{-2}+1698z^{-3}-452z^{-4}+683z^{-5}}{(1-z^{-1})^6}$
R_3	$\frac{5}{2}\frac{1}{s^2T_s^2}$	$\frac{25}{24}\frac{z^{-1}+4z^{-2}+z^{-3}}{(1-z^{-1})^4}$
R_4	$\frac{5}{2}\frac{1}{sT_s}$	$-\frac{25}{4}\frac{z^{-1}}{(1-z^{-1})^2}$

Fig. 3.14 shows the square magnitudes of the close-loop equivalent discrete-time NTFs from each integrator input to the modulator output of the proposed MASH 2-2 CTΣΔM. The suppressions for the input-referred thermal noise of the first through the fourth integrators are 0.2 dB, 4.2 dB, 19.3 dB, and 30.8 dB, respectively.

Fig. 3.15 shows the circuit thermal noise breakdown of the proposed MASH 2-2 CTΣΔM. The total circuit thermal noise floor of the modulator is −79.1 dBFS. The modulator full-scale is 687.5 mV.

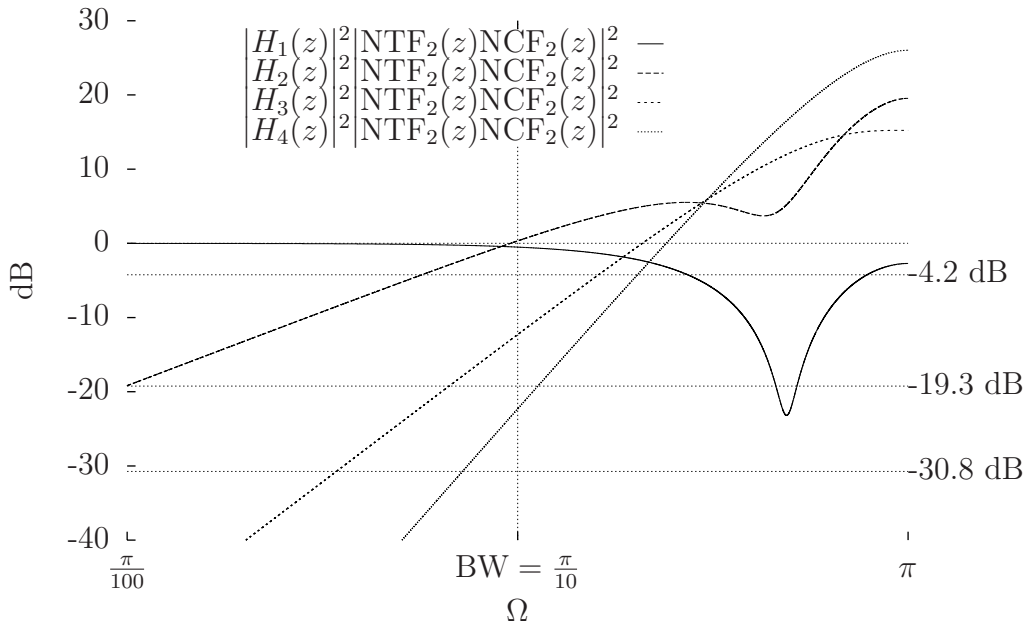


Figure 3.14: Square magnitudes of the close-loop equivalent discrete-time NTFs from each integrator input to the modulator output of the proposed MASH 2-2 CTΣΔM.

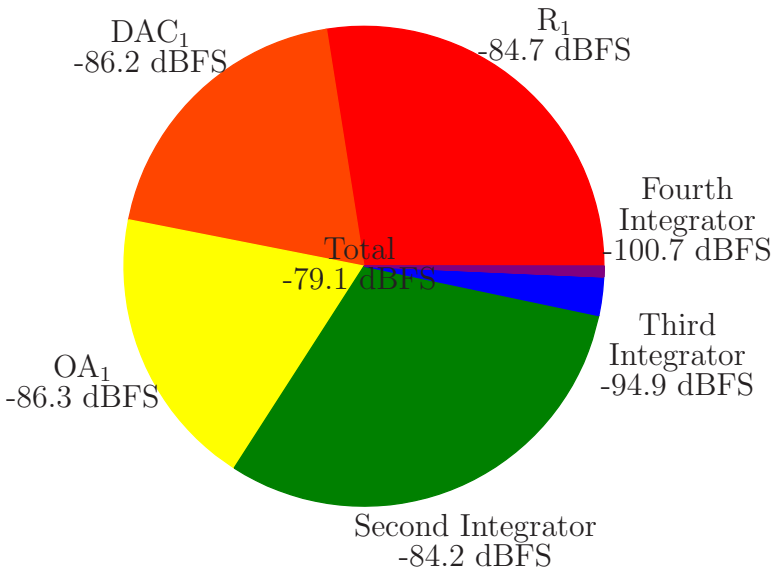


Figure 3.15: Circuit thermal noise breakdown of the proposed MASH 2-2 CTΣΔM.

3.4.2 DAC Clock Jitter

The prototype chip relies on the performance of an external clock source to minimize the effect of clock jitter to the modulator noise floor. Here the analysis in [111] is used to have an estimate on the modulator clock jitter sensitivity. In addition to the white clock jitter model, a low frequency clock spur can be used to model the clock phase noise near the carrier frequency assuming that this noise has a very narrow bandwidth compared to that of the modulator. The analysis here also assumes that the effect of clock jitter is dominated by that in DAC_1 for simplicity.

The approximate modulator noise floors due to a white clock jitter mixes with the first-stage quantization noise and the input signal are given by

$$\overline{N_{jq1}^2} \approx \frac{\overline{J^2}}{T_s^2} \times \overline{Q_1^2} \times \frac{1}{\mathrm{OSR}} \times \frac{1}{2\pi} \int_{-\pi}^{\pi} |\mathrm{NTF}_1(\Omega)(1 - e^{-j\Omega})|^2 d\Omega \tag{3.30}$$

$$\overline{N_{ji}^2} \approx \frac{\overline{J^2}}{T_s^2} \times \frac{A^2}{2} \times \frac{1}{\mathrm{OSR}} \times \mathrm{STF}_1(j\omega_o)(1 - e^{-j\omega_o T_s}) \tag{3.31}$$

The approximate modulator noise floors due to a low frequency clock spur mixes with the first-stage quantization noise and the input signal are given by

$$\overline{N_{sq1}^2} \approx \frac{1}{2}\frac{A_j^2}{T_s^2} \times \overline{Q_1^2} \times \frac{1}{2\pi} \int_{-\frac{\pi}{\mathrm{OSR}}}^{\frac{\pi}{\mathrm{OSR}}} |\mathrm{NTF}_1(\Omega)(1 - e^{-j\Omega})|^2 d\Omega \tag{3.32}$$

$$\overline{N_{si}^2} \approx \frac{1}{2}\frac{A_j^2}{T_s^2} \times \frac{A^2}{2} \times \mathrm{STF}_1(j\omega_o)(1 - e^{-j\omega_o T_s}) \left(u(\omega_o T_s) - u\left(\omega_o T_s - \frac{\pi}{\mathrm{OSR}}\right)\right) \tag{3.33}$$

where $\overline{J^2}$ is the white clock jitter variance, A_j is the clock spur amplitude, $\overline{Q_1^2}$ is the quantization noise floor of the first-stage quantizer, A is the sinusoid input signal amplitude, and ω_o is the sinusoid input signal angular frequency.

Fig. 3.16 shows the simulated noise floor of the proposed MASH 2-2 CTΣΔM for a white clock jitter and a low frequency clock spur models in all DACs.

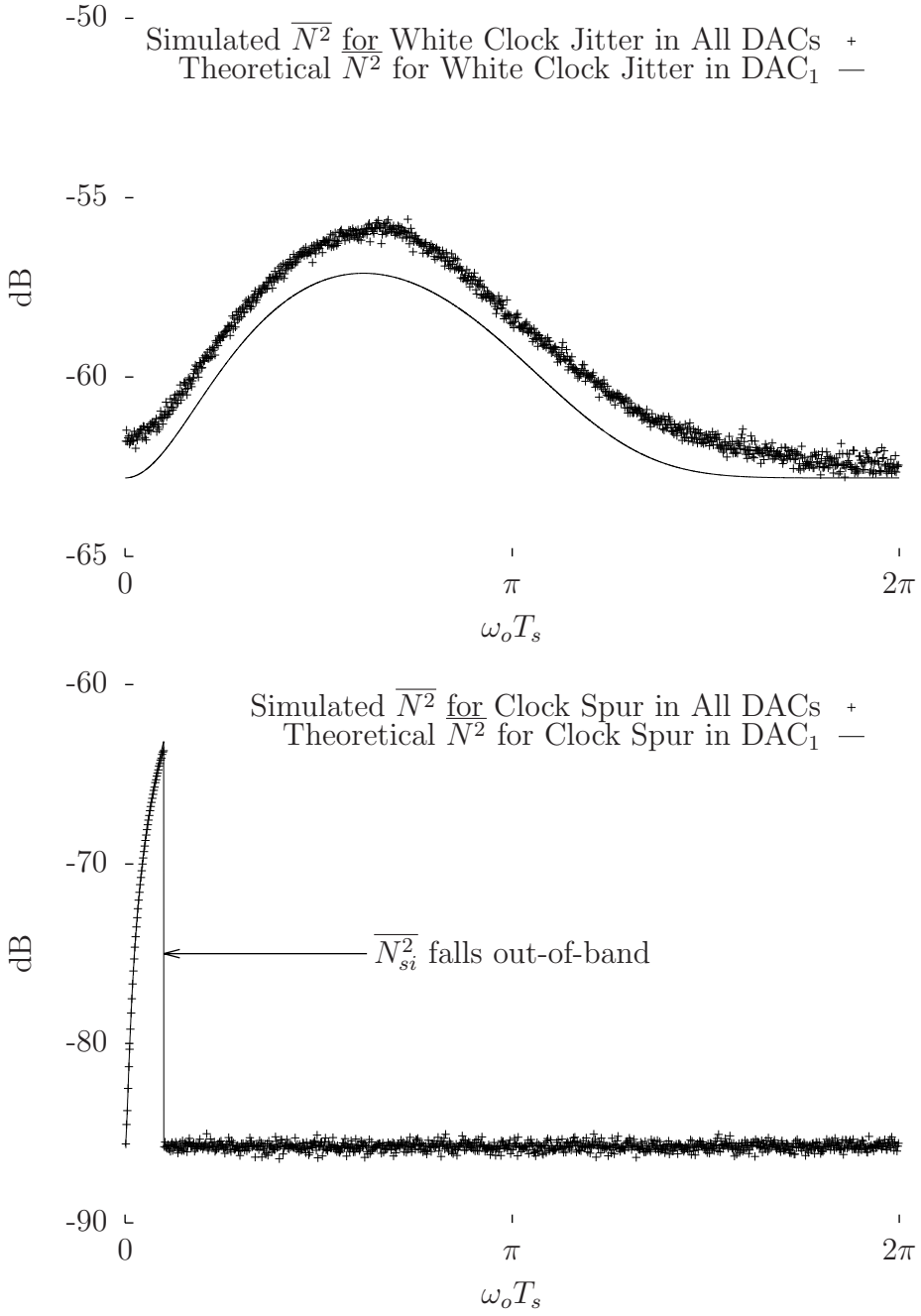


Figure 3.16: Simulated noise floor of the proposed MASH 2-2 CTΣΔM for a white clock jitter and a low frequency clock spur models in all DACs. $\overline{J^2}/T_s^2 = -40$ dB. $A_j/T_s = -40$ dB. $A = -10$ dBFS.

3.4.3 DAC Mismatch

DAC mismatch limits the distortion performance of a multi-bit ΣΔ modulator. Fig. 3.17 shows an example modulator output FFT spectrum of the proposed MASH 2-2 CTΣΔM with DAC mismatch variance $\overline{M^2}$ of 1 % for all DACs.

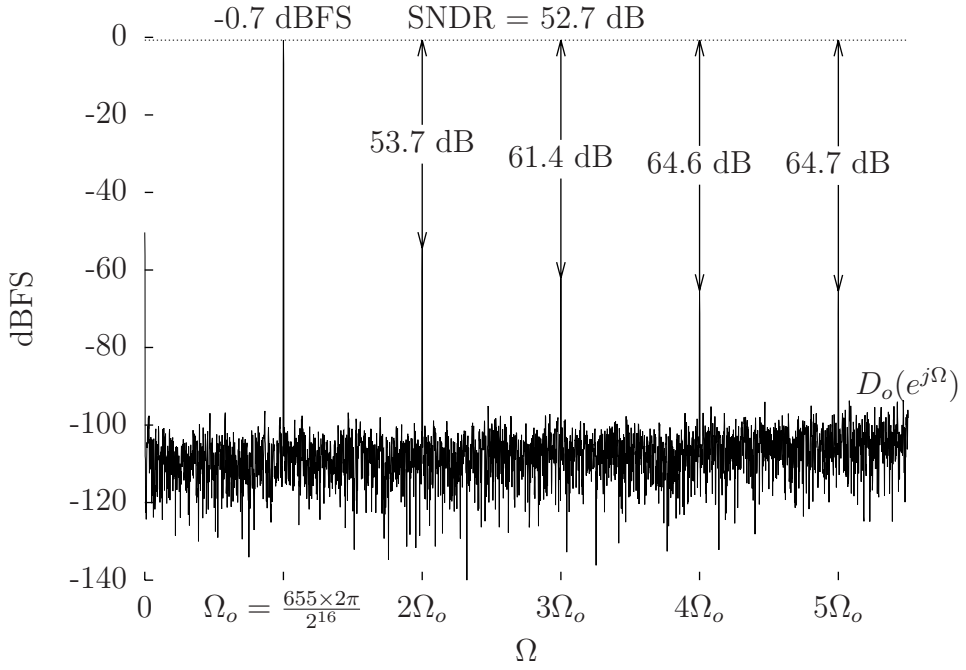


Figure 3.17: Example modulator output FFT spectrum of the proposed MASH 2-2 CTΣΔM with DAC mismatch variance $\overline{M^2}$ of 1 % for all DACs.

Table 3.4 shows the average harmonic tones amplitudes of the proposed MASH 2-2 CTΣΔM for 1000-run Monte Carlo simulations vs theoretical predictions. The theoretical predictions were obtained by substracting 40 dB from the expected amplitudes of the harmonic tones in the DAC error spectrum in Fig. 2.12.

The DACs in this design were budgeted to have 12-bit of linearity performance.

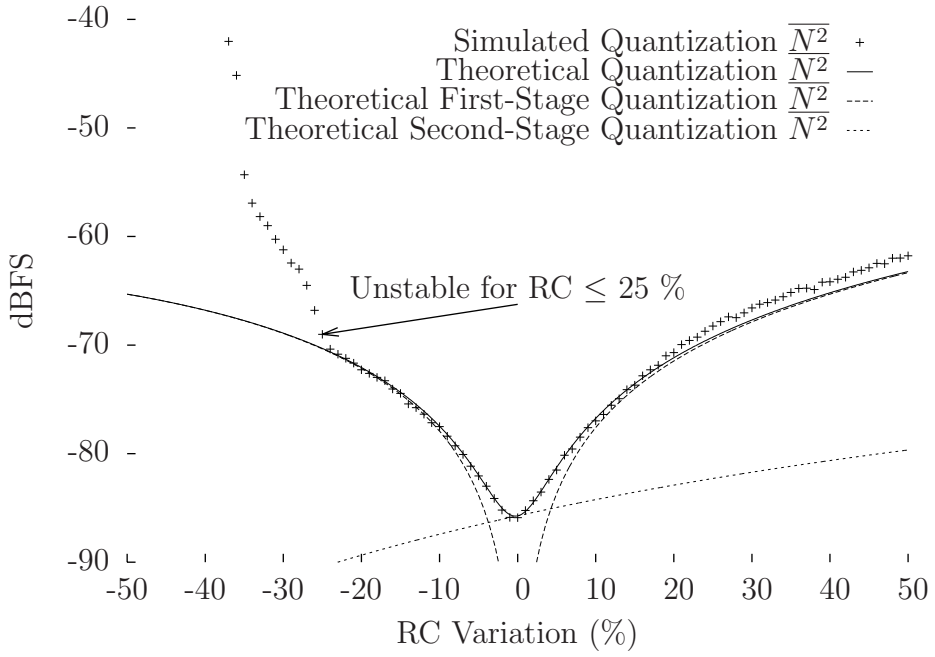
Table 3.4: Average harmonic tones amplitudes of the proposed MASH 2-2 CTΣΔM for 1000-run Monte Carlo simulations vs theoretical predictions.

Harmonic Order	Simulation	Theoretical
2	−58.4 dB	−58.8 dB
3	−61.7 dB	−62.6 dB
4	−63.5 dB	−65.3 dB
5	−65.3 dB	−67.4 dB

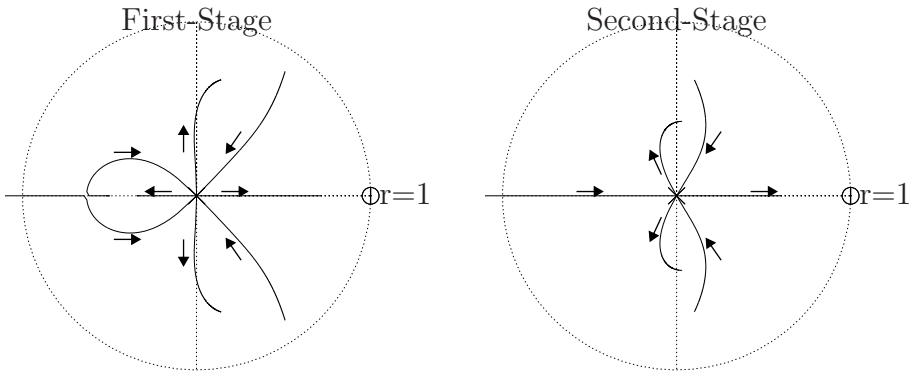
3.4.4 Process Variations

Fig. 3.18 shows the simulated noise floors and the root locus plots of the proposed MASH 2-2 CTΣΔM vs RC time constant variation. In this example, up to ±3 % of RC time constant variation can be tolerated for less than −83.5 dBFS of the quantization noise floor budget. Calibration is necessary since the expected worst-case variation of resistors or capacitors is ±20 % based on technology specifications.

Analyses were done for both the global and the local variations of resistors, capacitors, DAC coefficients, DAC delays, quantizer sampling instances, and quantizer gains with good agreement found between the theoretical and the simulation results. Besides RC time constant variation, DAC coefficient variations are also a contributor to the quantization noise leakage and minimized by proper biasing. The quantization noise floor of the design is not sensitive to DAC delays, quantizer sampling instances, quantizer gains, and feedforward interstage path coefficients variations.



(a)



(b)

Figure 3.18: (a) Simulated noise floors and (b) root locus plots of the proposed MASH 2-2 CTΣΔM vs RC time constant variation.

4. CIRCUIT DESIGN

This section discusses circuit design of OAs, bias circuits, digitally tunable capacitors, RC time constant calibration circuits, quantizers, and feedback DACs which are critical building blocks implementing the prototype MASH 2-2 CTΣΔM chip.

4.1 Operational Amplifier (OA)

Fig. 4.1 shows the OA schematic. The four-stage OA is compensated using the no capacitor feedforward (NCFF) scheme [112]. The fourth-order path consists of the transconductors G_{m1-4} which provide a high gain at low frequencies. At high frequencies, the first-order path through the transconductor G_{m14} dominates the OA frequency response to guarantee a close-loop stability. The second-order and the third-order paths through the transconductors G_{m12} and G_{m13}, respectively, provide a smooth transition for the OA frequency response at intermediate frequencies.

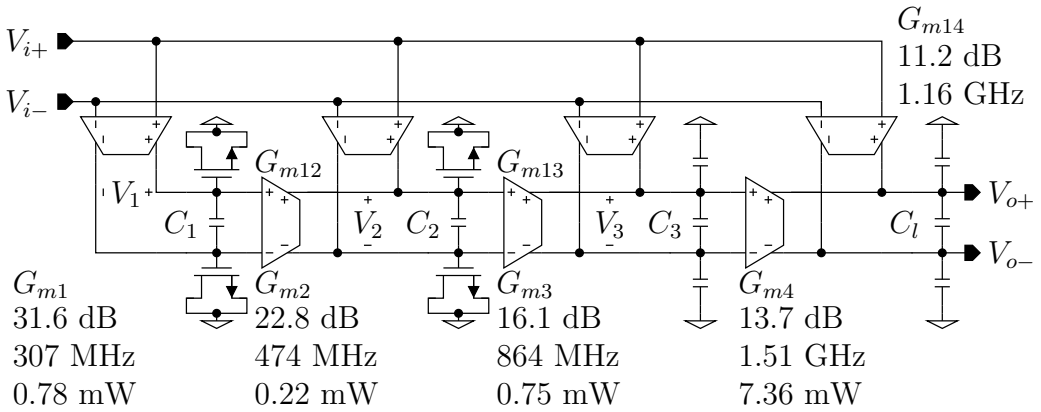


Figure 4.1: OA schematic annotated with OA_1 design parameters.

OA_1 design parameters are also annotated in Fig. 4.1 as an example. The band-

width of each stage is numerically optimized to provide a high gain up to the modulator bandwidth of 50 MHz while maintaining a good phase margin. Additional NMOS capacitors are added to the first-stage and the second-stage outputs to achieve the low bandwidth required for an optimal frequency response while maintaining a low noise performance. Their non-linearity is not a concern due to the small signal swings they experience. On the other hand, the third stage directly drives the parasitic input capacitances of the fourth stage to save power consumption.

The inputs, the outputs, and the internal voltages V_{1-3} of the OA can be shorted by switches to reset the modulator.

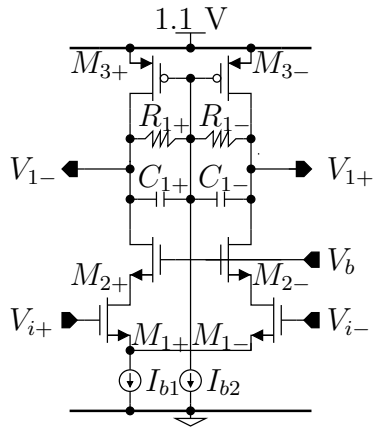


Figure 4.2: Transconductor G_{m1} schematic used in the OA.

Fig. 4.2 shows the transconductor G_{m1} schematic used in the OA. The input transistors M_1 are cascoded by the transistors M_2 to achieve a high gain, a high transconductance efficiency, and low input capacitances using small channel length transistors. Cascoding is not used for the load transistors M_3 as their large channel length provides a sufficiently high output resistance and their headroom needs to be large for a low noise operation. Self-biased common-mode feedback (CMFB) is im-

plemented by the resistors R_1 and the capacitors C_1. The current source I_{b2} is added to raise the transconductor output common-mode voltage. The transconductors G_{m2} and G_{m12} have an identical schematic to that of the transconductor G_{m1}, whereas the transconductors G_{m3} and G_{m13} have a slightly different schematic to that of the transconductor G_{m1} in which the current source I_{b2} is not used.

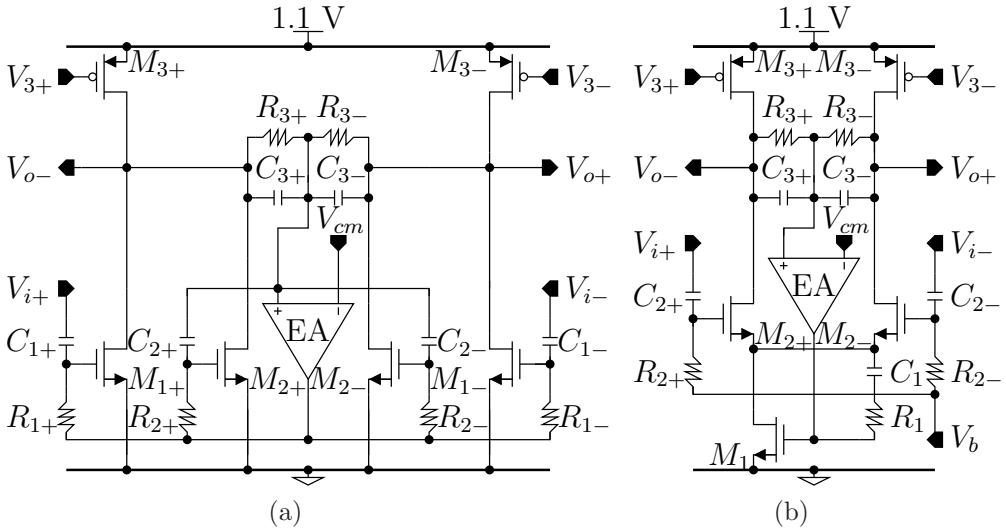


Figure 4.3: Transconductors G_{m4} and G_{m14} schematics used in (a) OA_1 and (b) OA_2.

Fig. 4.3a shows the transconductors G_{m4} and G_{m14} schematic used in OA_1. The transconductor G_{m4} is formed by the transistors M_3. The transconductor G_{m14} is formed by the transistors M_1 which are AC coupled to the OA input terminals using the resistors R_1 and the capacitors C_1. The AC coupling is designed to provide an in-band isolation between the gate to drain capacitances of M_1 and the digitally tunable capacitors of the integrators. A two-stage NCFF compensated CMFB loop is used. At low frequencies, the CMFB loop consists of the common-mode detector formed by resistors R_3 and capacitors C_3, an error amplifier (EA), transistors M_{1-2},

and resistors R_{1-2}. At high frequencies, capacitors C_2 and C_3 bypass the EA and the resistors R_{1-2}.

Fig. 4.3b shows the transconductors G_{m4} and G_{m14} schematic used in OA_2. As the input signal swings in the outputs of the second to the fourth integrators are reduced, the pseudo differential topology of the transconductor G_{m14} in OA_1 is replaced by its fully differential version. A two-stage Miller compensated CMFB loop with a nulling resistor is used. The transconductors G_{m4} and G_{m14} used in OA_{3-4} have a slightly different schematic to that in OA_2 in which the AC coupling is not used to save power consumption.

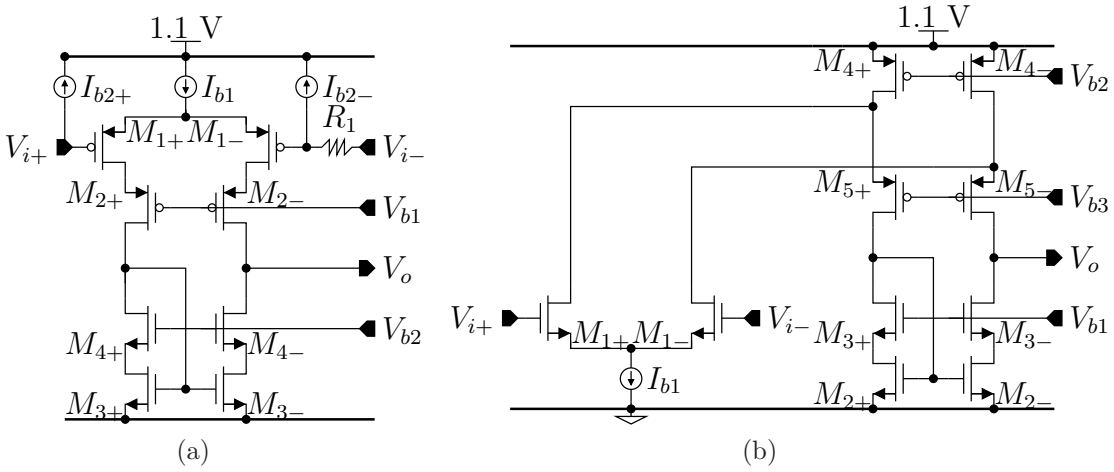


Figure 4.4: EA schematics used in (a) $OA_{1,3}$ and (b) $OA_{2,4}$.

Fig. 4.4a shows the EA schematic used in $OA_{1,3}$. It is a single-ended telescopic cascode amplifier with PMOS input transistors M_1. The current sources I_{b2} and the resistor R_1 are used to lower the input common-mode voltage of the EA. Fig. 4.4b shows the EA schematic used in $OA_{2,4}$. It is a single-ended folded cascode amplifier with NMOS input transistors M_1.

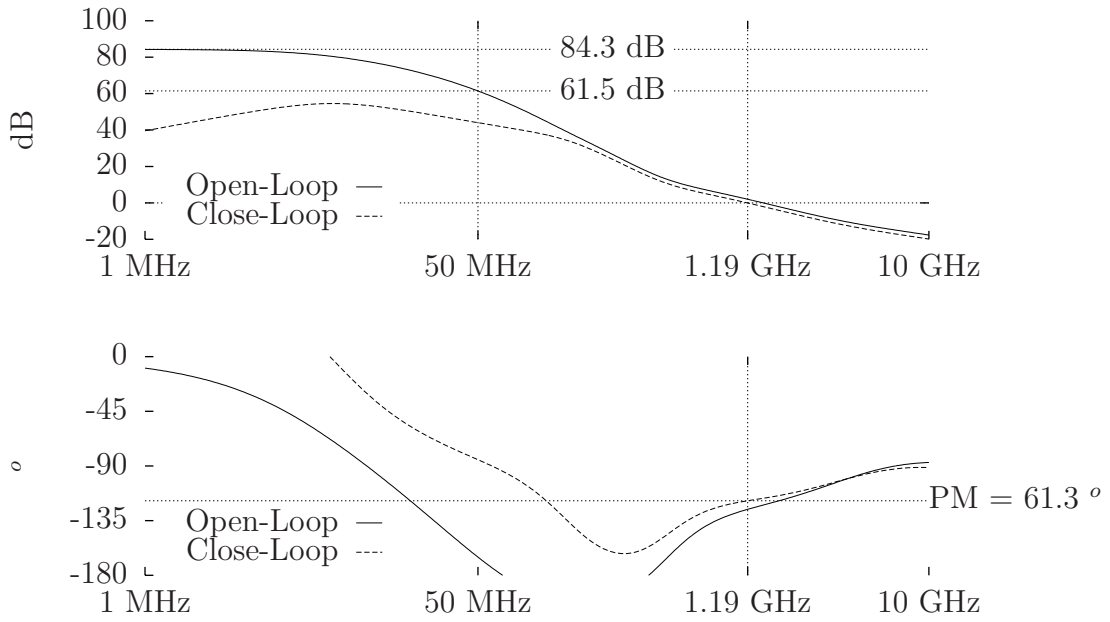


Figure 4.5: Simulated OA_1 postlayout bode plot.

Fig. 4.5 shows the simulated OA_1 postlayout bode plot as an example. The test-bench breaks the integrator feedback loop at the OA input terminals to measure the open-loop and the close-loop OA gains including all loadings. Table 4.1 summarizes the OAs postlayout simulation results. All OAs achieve greater than 60 dB of open-loop gain at a frequency of 50 MHz to satisfy both the linearity and quantization noise leakage specifications.

Table 4.1: OAs postlayout simulation results.

	A_{dc} (dB)	$A_{50\ MHz}$ (dB)	UGF (GHz)	PM (^{o})	P (mW)
OA_1	84.3	61.5	1.19	61.3	10.7
OA_2	85.0	63.2	1.20	67.8	6.6
OA_3	78.9	64.3	1.81	72.3	3.6
OA_4	80.0	65.4	0.96	65.3	3.5

4.2 Bias Circuit

Fig. 4.6a shows the bias circuit schematic. Each bias circuit provides bias currents proportional to V_{fs}/R_b to the DACs, the OAs, and the RC time constant calibration circuit of each stage, where V_{fs} is an external reference voltage of 687.5 mV which corresponds to the modulator full-scale and R_b is a replica loop filter resistor. The values of R_b for the first and the second stages bias circuits are 8 kΩ and 64 kΩ, respectively.

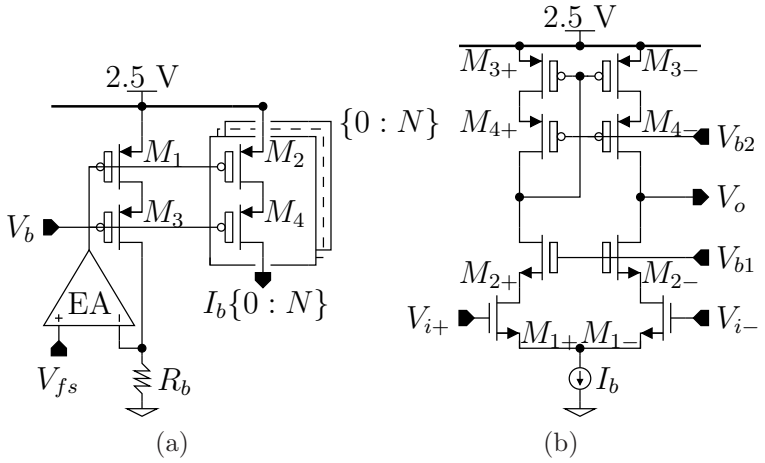


Figure 4.6: (a) Bias circuit schematic and (b) EA schematic used in the bias circuit.

Fig. 4.6b shows the EA schematic used in the bias circuit. The telescopic cascode EA consists of low mismatch NMOS input transistors M_1 and high output resistance 2.5 V thick oxide transistors M_{2-4} for the cascode and the load devices. Postlayout simulation results show that the EA achieves 839 μV of DC offset standard deviation and 90.7 dB of DC loop gain including the gain stage which consists of the transistors $M_{1,3}$ and the resistor R_b. The feedback loop is stable thanks to the parasitic capacitance at the EA output.

4.3 Digitally Tunable Capacitor

Fig. 4.7a shows the digitally tunable capacitor schematic. It is composed of multiple switchable capacitor unit cells in which each cell consists of a capacitor C in series with a 2.5 V thick oxide switch M and multiple fixed capacitor unit cells which is lumped in Fig. 4.7a as a single capacitor C_f.

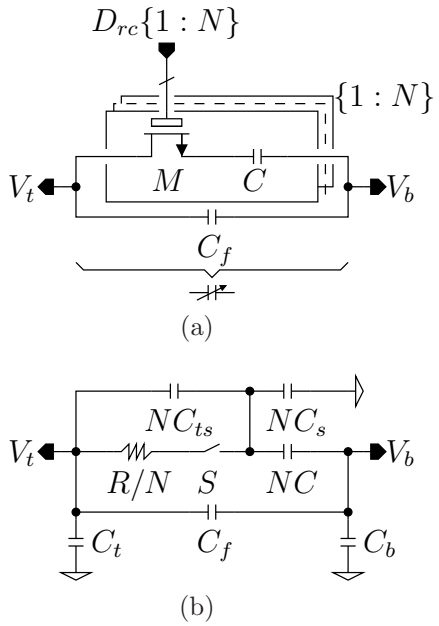


Figure 4.7: Digitally tunable capacitor (a) schematic and (b) small-signal model.

Table 4.2 shows the digitally tunable capacitors design parameters for the loop filter $C_{1-4,24}$ and the RC time constant calibration circuits C_{rc1-2}. The unit capacitance values are 1/56 pF and 1/96 pF for the first and the second stages digitally tunable capacitors, respectively. The numbers of unit cells used for the fixed and the switchable capacitors are selected such that the effective capacitances are 63.3 % and 163.3 % of the nominal capacitance value when all the switchable capacitor

unit cells are off and on, respectively. This design choice covers individual R and C variations of ±20 % or total RC variation from −36 % to 44 %.

Table 4.2: Digitally tunable capacitors design parameters.

Capacitor	Value (pF)	C_f (pF)	NC (pF)
C_1	7	248/56	392/56
C_2	10/7	51/56	80/56
C_{rc1}	7/2	124/56	196/56
C_3	5/8	38/96	60/96
C_4	1/4	15/96	24/96
C_{24}	5/48	6/96	10/96
C_{rc2}	5/2	152/96	240/96

The first and the second stages digitally tunable capacitors are controlled by 98-level and 120-level thermometer codes, respectively. The quantization noise leakage budget of ±3 % of RC time constant variation tolerates up to 2 LSBs and 4 LSBs of error in the first and the second stages RC time constant calibration codes, respectively. Thanks to the thermometer coding, the worst-case systematic mismatch between the digitally tunable capacitors C_1 and C_2 is minimized to less than 0.9 %.

Fig. 4.7b shows the digitally tunable capacitor small-signal model. The effective capacitances C_{off} and C_{on}, which correspond to the cases when all the switchable capacitor unit cells are off and on, respectively, are given by

$$C_{off} = C_f + \frac{NCC_{ts}}{C + C_{ts} + C_s} \tag{4.1}$$

$$C_{on} = C_f + NC \tag{4.2}$$

assuming that the digitally tunable capacitor is used in an active RC integrator.

(4.1) and (4.2) help a designer to tweak the unit capacitance values of the fixed

and the switchable capacitor cells during layout. The layout of the unit cells minimizes the parasitics top plate capacitor C_t, bottom plate capacitor C_b, and switch capacitance C_s as these capacitors load the OAs. Table 4.3 shows the digitally tunable capacitors simulation results for each stage where the ratios between the parasitic capacitances $C_{t,b,s}$ and the nominal capacitance values NC are tabulated. The switch on-resistance is chosen low enough to minimize the NTF out-of-band peaking but not too low in order to minimize the parasitics switch capacitances.

Table 4.3: Digitally tunable capacitors postlayout simulation results.

Stage	$C_t/(NC)$ (%)	$C_b/(NC)$ (%)	$C_s/(NC)$ (%)
1	8.2	11.1	9.3
2	7.5	19.8	6.4

4.4 RC Time Constant Calibration Circuit

Fig. 5.7 shows the RC time constant calibration circuit schematic. It consists of a one-bit DAC, an integrator formed by an OA and a digitally tunable capacitor C_{rc}, a comparator, and a finite state machine (FSM). It needs only one external reference voltage V_{fs} of 687.5 mV which corresponds to the modulator full-scale and a bias current I_{rc} generated by the bias circuit.

Fig. 4.9 shows the integrator output signal V_{ramp} during RC time constant calibration. Each ramp is generated by turning on the one-bit DAC which in turn sinks the current I_{rc} from the integrator input. If the integrator output signal V_{ramp} does not reach the reference voltage V_{fs} in a prescribed amount of ramp time, the RC time constant calibration code D_{rc} is decremented and the ramp is regenerated. Otherwise, this process is stopped and the RC time constant calibration code D_{rc} is saved

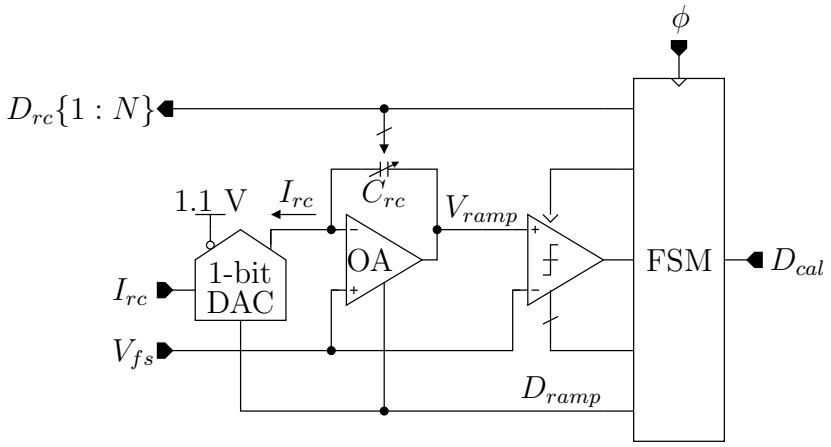


Figure 4.8: RC time constant calibration circuit schematic.

in the registers. The ramp time is set to be 196 and 160 times of the clock period for the first and the second stages RC time constant calibration circuits, respectively.

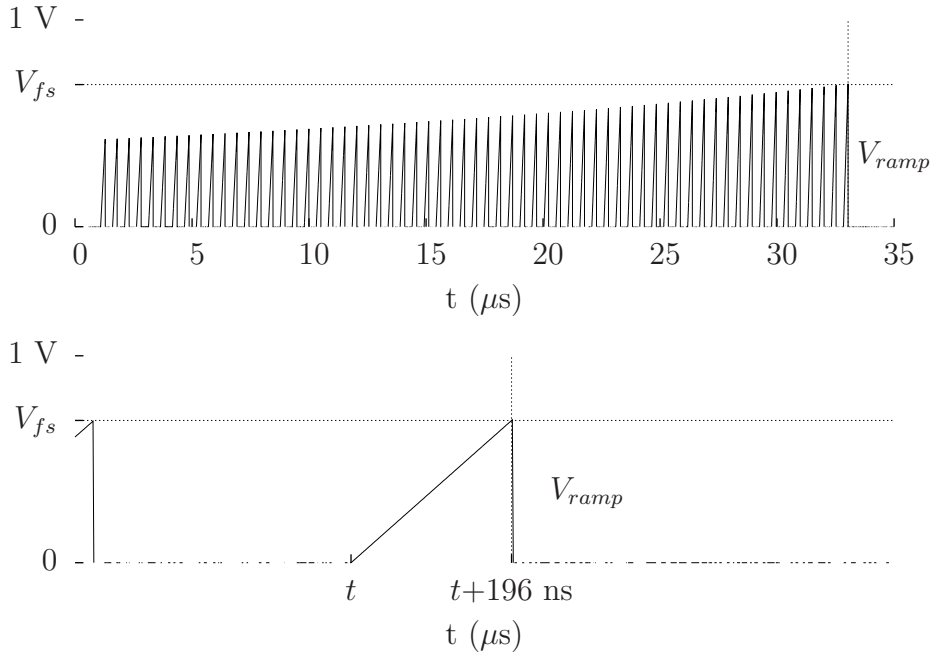


Figure 4.9: Integrator output signal V_{ramp} during RC time constant calibration.

Fig. 4.10 shows the integrator schematic used in the RC time constant calibration circuit. The two-stage uncompensated OA used in the integrator has auto-zero offset reduction and 0 V output voltage operation capabilities. The input stage is formed by the input transistors M_1, the cascoded load transistors M_{2-3}, and the current source I_{b1}. The output stage is formed by the transistor M_4, the current-steering cascode transistors M_5, the current source I_{b2}, the current-steering switches M_6, the reset transistor M_7, and the digital drivers. When the signal D_{ramp} is low, the integrator is configured as a unity gain follower charging the potential between the top and the bottom plates of the digitally tunable capacitor C_{rc} to the external reference voltage V_{fs}. When the signal D_{ramp} is high, the integrator generates a ramp at its output with 0 V of initial condition. The OA operates linearly as only the PMOS transistors M_4 and M_{5-} are connected to the output in this situation.

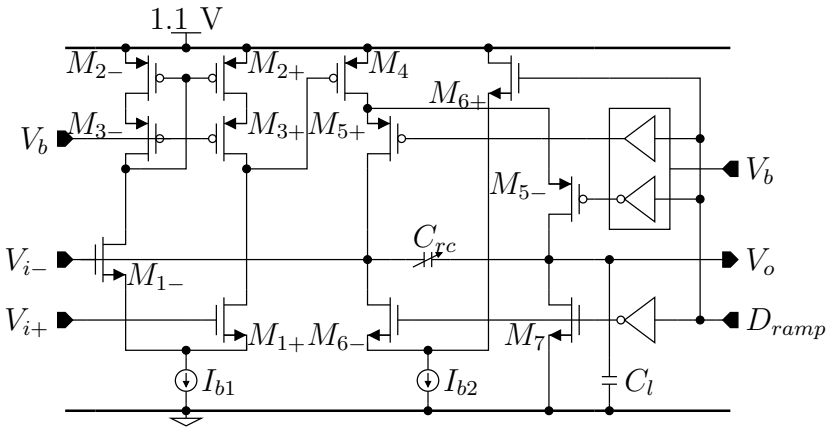


Figure 4.10: Integrator schematic used in the RC time constant calibration circuit.

Stability is ensured by placing the output pole of the input stage to be above the unity gain frequency (UGF) of the output stage and the fact that the output stage only carries a small current of approximately $I_{rc}\,(1 + C_l/C)$ to generate the ramp.

Setting the current source I_{b2} to this amount helps to reduce integrator delay as this is the initial condition of the OA output current when the ramp begins. Nevertheless, the integrator delay is not very critical as it can be compensated by delaying the comparator clock signal. On the other hand, it is important to have high OA gain to minimize error in the slope of the ramp. DC gain of 60 dB is achieved.

Fig. 4.11 shows the comparator schematic used in the RC time constant calibration circuit. It consists of a preamplifier, a DAC, a sense amplifier [113], and an SR latch [114]. The preamplifier is a differential pair with NMOS input transistors and resistive loads. Before RC time constant calibration begins, the offset and the hysteresis of the preamplifier is calibrated by shorting the preamplifier input terminals to the external reference voltage V_{fs} and sweeping the digital input codes of the seventeen-level current-steering DAC until the SR latch output signal flips.

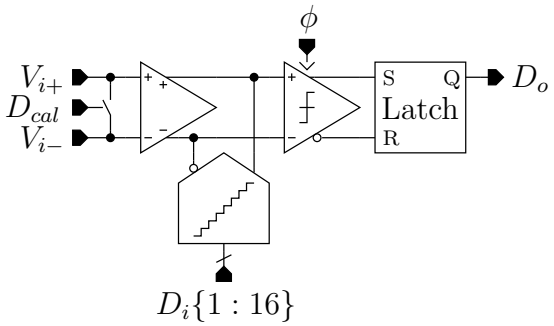


Figure 4.11: Comparator schematic used in the RC time constant calibration circuit.

The RC time constant variation over temperature is +0.15 % and +0.64 % at 125 ^{o}C and -40 ^{o}C, respectively, compared to the nominal RC time constant at 27 ^{o}C. Thanks to the low temperature coefficient of the passive components, startup RC time constant calibration is deemed sufficient.

4.5 Quantizer

Fig. 4.12 shows the quantizer schematic. The four-bit flash quantizer consists of fifteen comparators, a resistor ladder, a thermometer-to-binary encoder, and a DWA pointer calculator. The dynamic comparator has a digitally controlled offset voltage which is calibrated to the resistive ladder differential reference voltage during startup. After calibration, the resistive ladder can be turned off during normal operation to save power consumption. The thermometer-to-binary encoder is based on a Wallace-tree adder topology to minimize the effect of comparator metastability to the modulator performance.

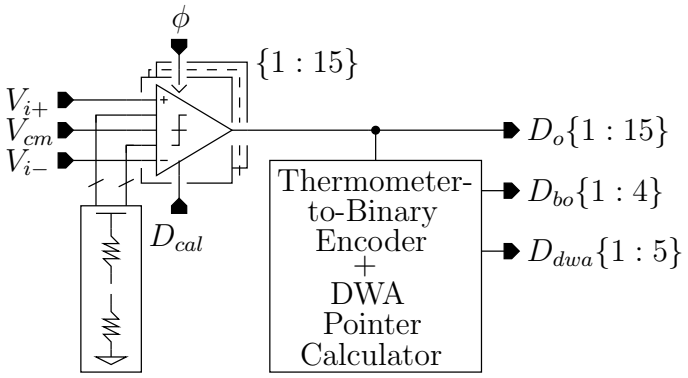


Figure 4.12: Quantizer schematic.

Fig. 4.13a shows the comparator schematic used in the quantizer. The comparator consists of a sense amplifier, an SR latch [114], an FSM, a switched-capacitor common-mode voltage level shifter, and a pair of input calibration switch. Calibration is performed by connecting the sense amplifier input terminals to the resistive ladder differential reference voltage V_r through the switched-capacitor common-mode voltage level shifter. The FSM sweeps the code controlling the sense amplifier off-

set voltage and monitors the SR latch output. The optimum sense amplifier offset calibration code is then saved in the registers.

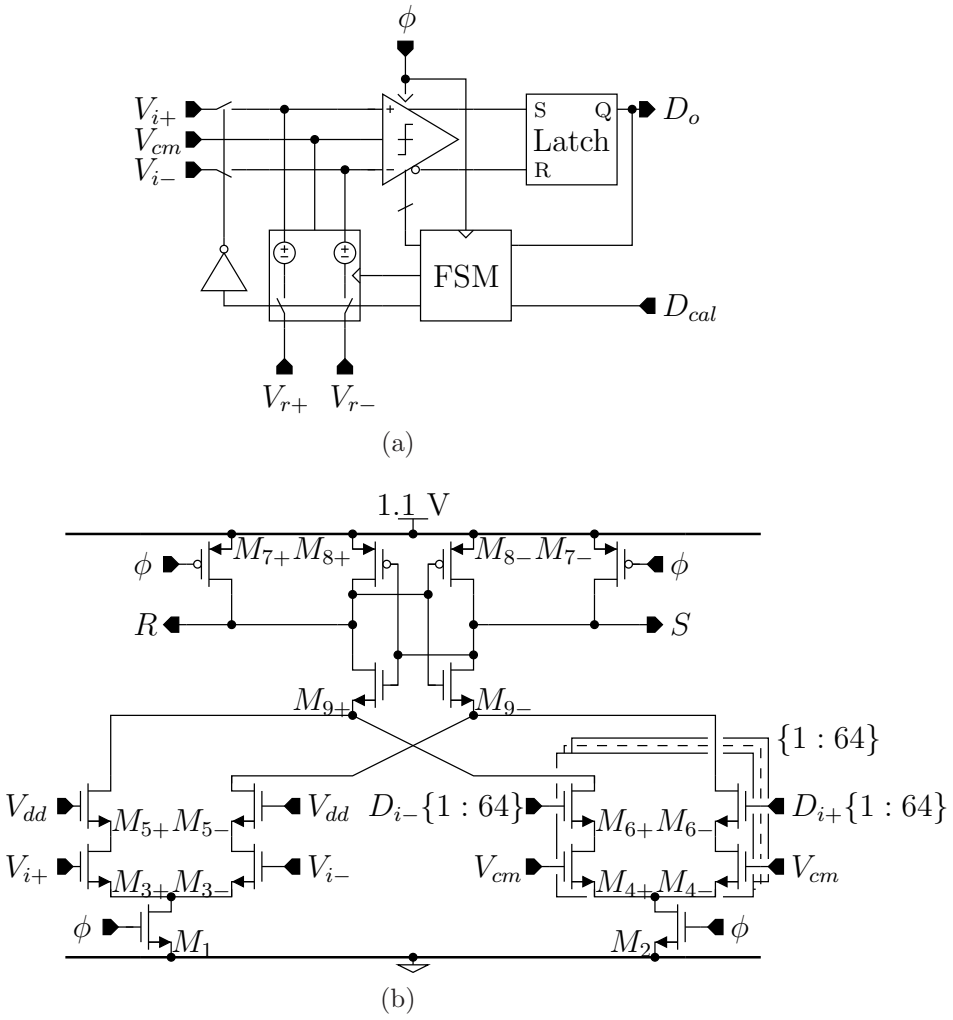


Figure 4.13: (a) Comparator schematic used in the quantizer and (b) sense amplifier schematic used in the comparator.

Fig. 4.13b shows the sense amplifier schematic used in the comparator. The topology in [113] is modified by adding sixty four cells of the reference transistors M_4 and the switches M_6 which are clocked by the transistor M_2. Sixteen of this cell

also form the the input transistors M_3. They are permanently enabled by connecting the gate of the transistors M_5 to the power supply voltage of 1.1 V.

Fig. 4.14 shows the postlayout corner simulation results of sense amplifier offset voltage vs calibration code. The effect of non-linearity on this curve is minimized by sweeping both the positive and negative sense amplifier offset calibration codes during calibration. At maximum sense amplifier offset calibration code, the sense amplifier offset voltage is greater than the desired maximum reference voltage for all corners to give some margin for random transistor mismatches.

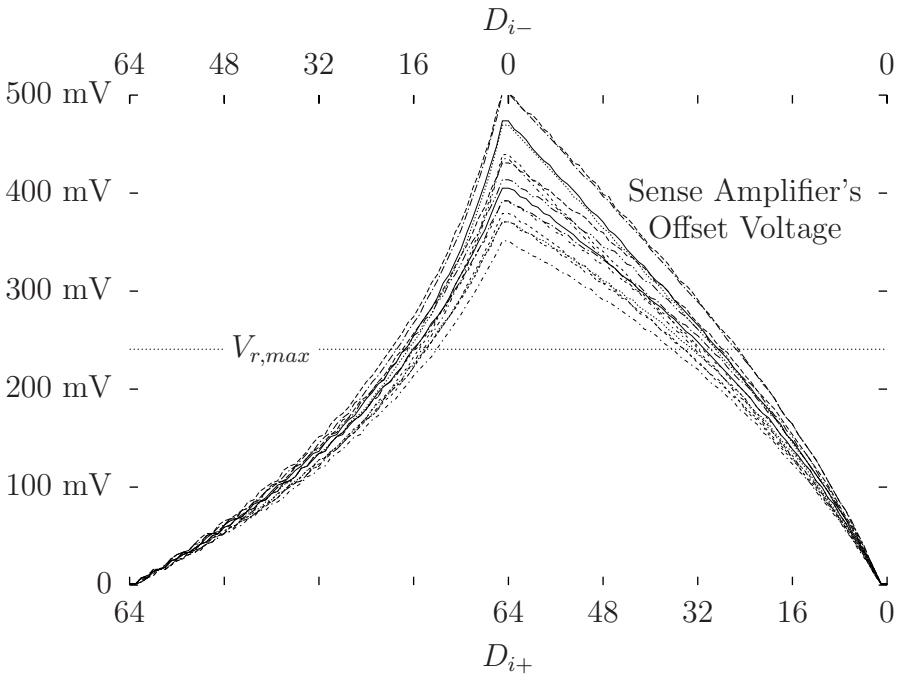


Figure 4.14: Postlayout corner simulation results of sense amplifier offset voltage vs calibration code.

The simulated nominal digital power consumption of the quantizer is 2.5 mW.

4.6 Feedback DAC

Fig. 4.15 show the PMOS and the NMOS DAC cells schematics. Each of the fifteen DAC cells consists of the current source transistor M_1, the cascode transistor M_2, the current switch transistors M_3, and the latch. The PMOS DAC cell uses a 2.5 V power supply voltage and a 2.5 V thick oxide current source transistor M_1, whose drain is biased at 1.1 V to provide the large headroom necessary for low noise and good matching performances.

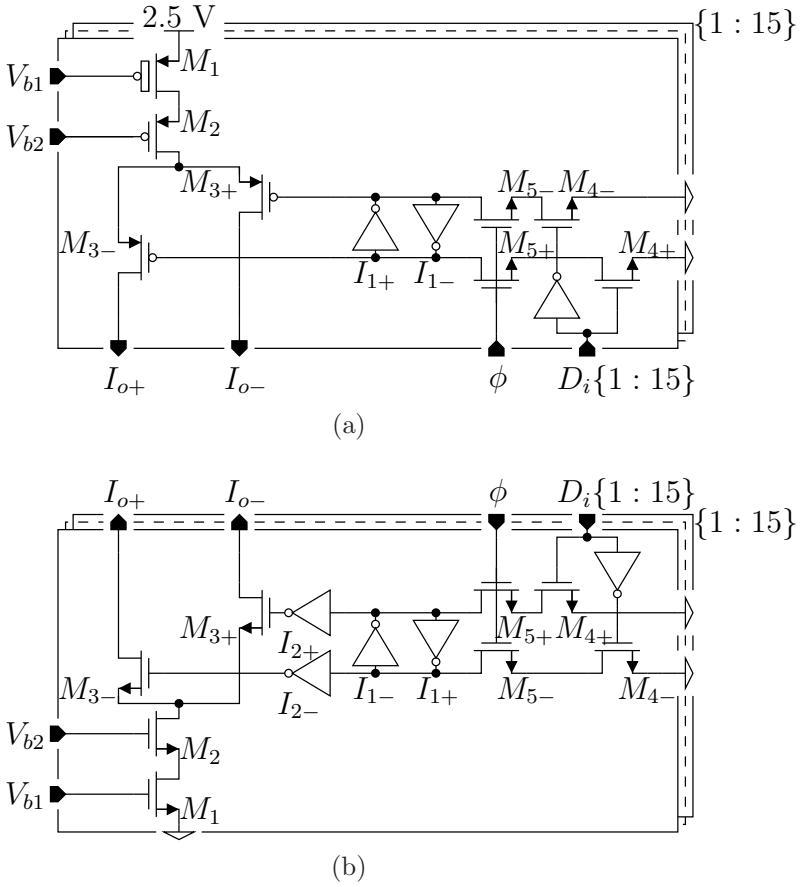


Figure 4.15: (a) PMOS and (b) NMOS DAC cells schematics.

The latch consists of the transistors M_{4-5} and the cross-coupled inverters I_1. The additional inverters I_2 are added at the output terminals of the latch used in the NMOS DAC cell to generate a high crossing-point switching. The number of inverter stages used to buffer the clock signal of each DAC is carefully selected to minimize ELD based on postlayout simulation results on the delays of the latch, the current switch transistors, and the quantizer clock buffer. The digital signal paths from the quantizer outputs to the DAC inputs are kept single-ended to minimize power consumption.

Each DAC cell carries a bias current whose value is given by $G_m V_{fs}/16$, where G_m is the DAC transconductance annotated in each DAC shown in Fig. 3.1 and V_{fs} is the external reference voltage of 687.5 mV which corresponds to the modulator full-scale. External capacitors are used to decouple DAC bias voltages V_{b1}. The PMOS DAC cell is used for DAC_1, DAC_4, DAC_6, and DAC_9 whereas the NMOS DAC cell is used for the rest of the DACs. The residual DAC common-mode bias currents help to increase the OA input common-mode voltages and provide bias currents to the OA output stages and the circuit driving the modulator input terminals.

The simulated nominal analog power consumptions of the first and the second stage DACs are 7.5 mW and 1.1 mW, respectively. The simulated nominal digital power consumptions of the first and the second stage DACs are 3.2 mW and 1.7 mW, respectively.

5. EXPERIMENTAL RESULTS

This section reports experimental results of the prototype MASH 2-2 CTΣΔM chip. The prototype chip and experimental setup are first described before the experimental results are finally reported.

5.1 Prototype Chip

The prototype chip was implemented in TSMC 40 nm CMOS mixed-signal/RF low power process. Fig. 5.1 shows the prototype chip microphotograph. The area occupied by the modulator core is 0.265 mm^2.

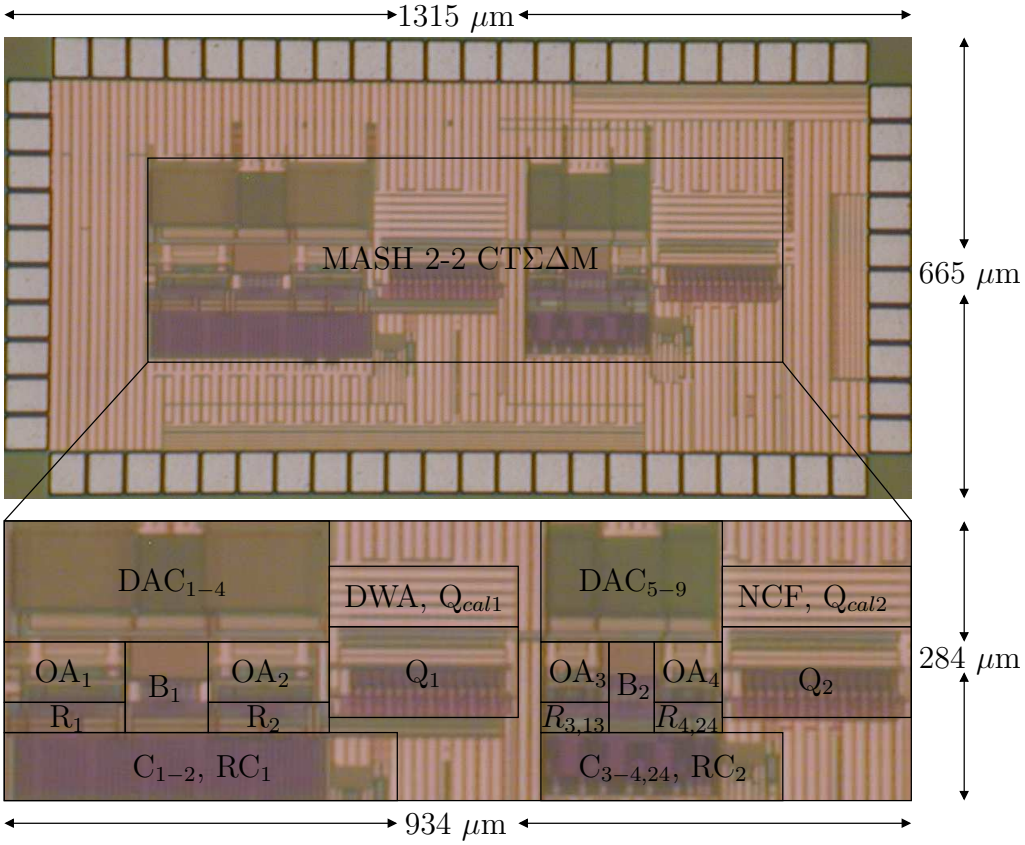


Figure 5.1: Prototype chip microphotograph.

Besides the modulator core, some additional circuitries are needed for testing purpose. Four channels of current mode logic buffer and two-to-one multiplexer are included to have the ability to observe either the seven-bit NCF output or two four-bit quantizer outputs using a four-channel oscilloscope. A clock generator converts a single-ended sinusoid clock signal with a frequency of 2 GHz off-chip into a single-ended square wave clock signal with a frequency of 1 GHz and a duty cycle of 50 % on-chip for the DACs and quantizers. An additional clock generator can be enabled to provide two separate delayed clock signals for the DACs and quantizers, respectively, if ELD is not optimum. Bias voltages of the DACs and OAs are taken off-chip to enable measurement of power consumption breakdown. Scan interface enables the read and write operations for the calibration and configuration registers. The leftover area is used for decoupling capacitors.

5.2 Experimental Setup

The prototype chip was bonded to a 56-pin quad flat no-leads (QFN) package and soldered to a custom printed circuit board (PCB) as shown in Fig. 5.2. The PCB includes adjustable low-dropout (LDO) regulators to provide power supply voltages, potentiometers to provide bias currents, and adjustable resistive dividers followed by unity gain buffers to override internal bias voltages. Debounced switches and Arduino UNO microcontroller were used to initiate calibrations, change modes of operation, and perform scan. The single-ended input signal was converted to differential using the two Mini-circuits ADT1-6T baluns in cascade mounted in a daughter PCB. Each single-ended sinusoid clock signal with a frequency of 2 GHz was filtered using the two Taiyo Yuden FAR-F6KA-2G0175-D4DR surface acoustic wave (SAW) filters in cascade mounted in a daughter PCB. The differential digital outputs are routed using 50 Ω coplanar waveguides to subminiature version A (SMA) connectors located at

the edge of the PCB. The positive digital outputs were taken to the oscilloscope inputs using 50 Ω SMA cables, whereas the negative digital outputs were terminated using 50 Ω SMA load terminations.

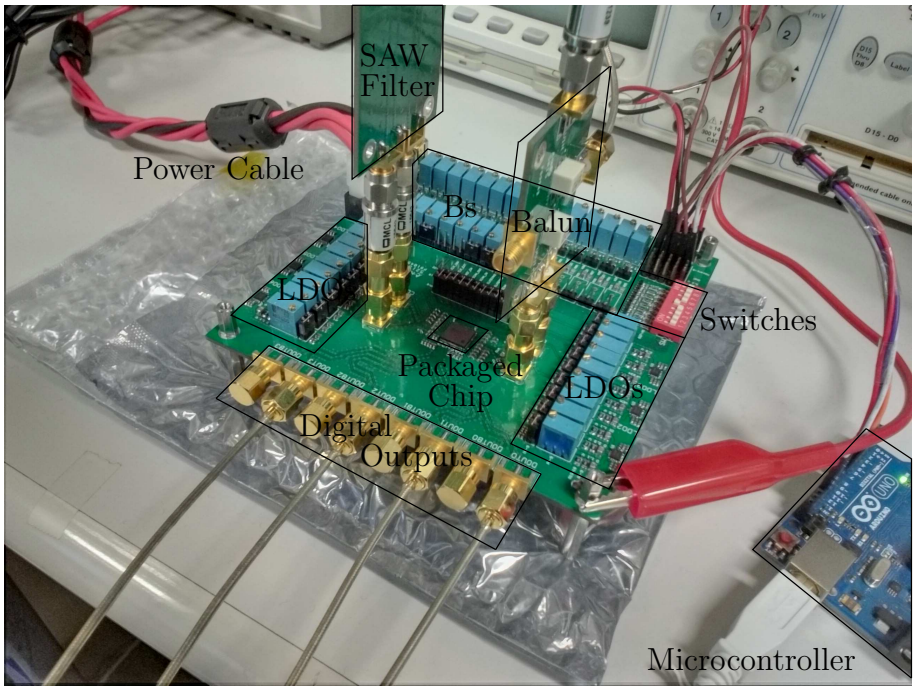


Figure 5.2: PCB photo.

Fig. 5.3 shows the experimental setup. The Agilent E3631A powered the PCB. For single-tone test, the Agilent E8267D provided the single-ended sinusoid input signal with a frequency of 10 MHz that was filtered by a Mini-circuits SLP-10.7+ low-pass filter, Mini-circuits SBP-10.7+ band-pass filter, and KR Electronics 2796-SMA band-pass filter with a 3 dB bandwidth of 400 kHz in cascade. For two-tone test, the Agilent E8267D and Agilent E4432B provided the single-ended sinusoid input signals with frequencies of 42 MHz and 38 MHz, respectively. The two signals were combined by a splitter and filtered by the KR Electronics 2510-SMA band pass

filter with a 3 dB bandwidth of 4 MHz. For STF measurement, the Mini-circuits TX-2-5-1+ balun was used for single-ended to differential input signal conversion.

The Agilent N5171B and Agilent E4432B provided the single-ended sinusoid clock signals with a frequency of 2 GHz to the main and secondary clock generators, respectively, through the SAW filters. As ELD was measured to be optimum, there was no need to provide two separate delayed clock signals for the DACs and quantizers. The secondary clock generator provides the clock signal to the RC time constant calibration circuits in this mode of operation. The Agilent DSA91304A oscilloscope captured the single-ended digital outputs. A laptop with a custom C program averaged the square magnitudes of 125 4096-point Hann-windowed FFTs spectrums of the captured data. All generators and the oscilloscope were synchronized using a reference signal with a frequency of 10 MHz generated from the Agilent E8267D.

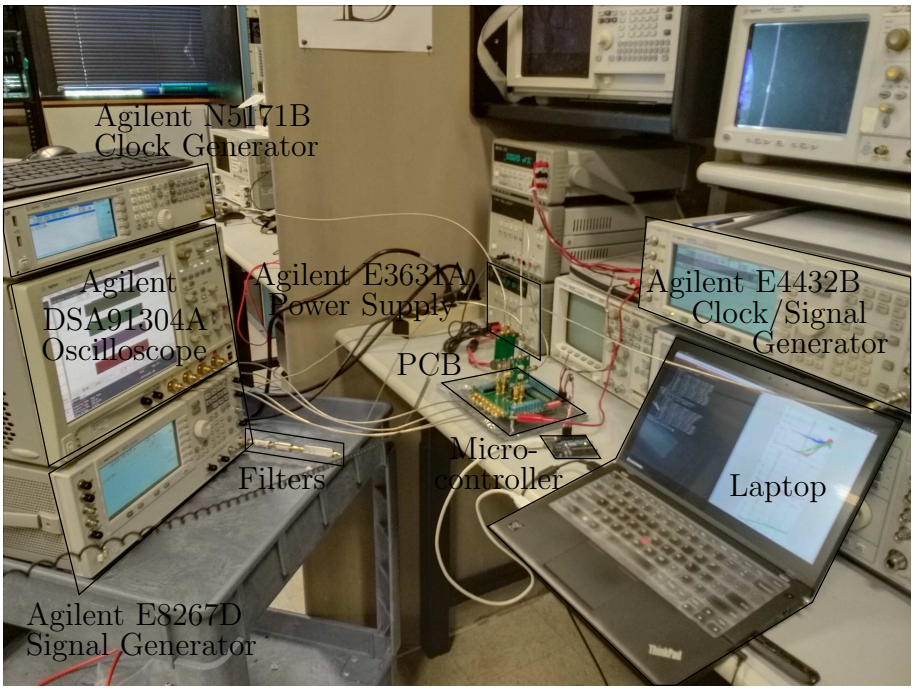


Figure 5.3: Experimental setup.

5.3 Experimental Results

Fig. 5.4 shows the measured SNDR and SNR vs the 10 MHz sinusoid input signal amplitude of the prototype MASH 2-2 CTΣΔM. The DR, defined as the ratio between the maximum and minimum input signal amplitudes where the SNDR > 0 dB, is 76.8 dB. The MSA is -0.7 dBFS. During measurement, the modulator always recovered from overload and startup conditions without a need for reset mechanisms.

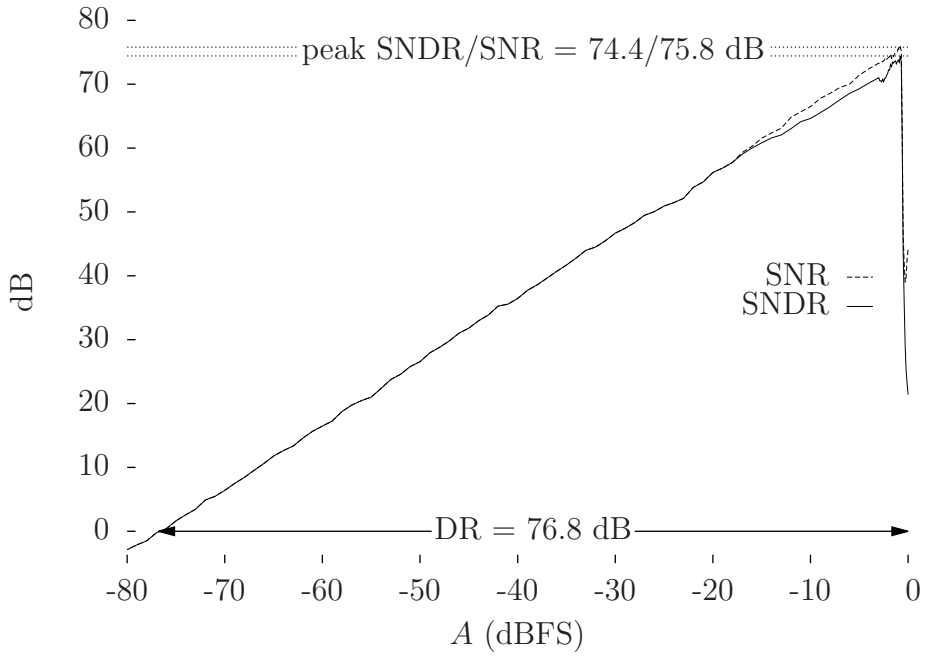


Figure 5.4: Measured SNDR and SNR vs the 10 MHz sinusoid input signal amplitude of the prototype MASH 2-2 CTΣΔM.

For increased visibility, measurement was performed by observing the two four-bit quantizer outputs and performing NCF function off-chip. No significant difference in the SNDR for this setup was found compared to the case when only the NCF output was observed. This observation confirms the functionality of the on-chip NCF.

Fig. 5.5 shows the measured single-tone FFT spectrum of the prototype MASH 2-2 CTΣΔM at peak SNDR condition. The peak SNDR, peak SNR, and spurious-free dynamic range (SFDR) are 74.4 dB, 75.8 dB, and 84.0 dB, respectively, for a sinusoid input signal with an amplitude of −0.8 dBFS and a frequency of 10 MHz. Noise and distortion cancellation of 20.0 dB was observed. The bandwidth of the modulator is 50.3 MHz to include the fifth-order harmonic in this measurement. The distortion is limited by intrinsic DAC matching as DWA was found to reduce the SFDR due to interaction between the parasitic DAC capacitances and the parasitic DAC routing resistances to the OA input terminals.

Fig. 5.6 shows the measured two-tone FFT spectrum of the prototype MASH 2-2 CTΣΔM. The sinusoid input signals are located at frequencies of 38 MHz and 42 MHz with an amplitude of −7.5 dBFS each. This condition represents the worst-case two-tone linearity test. The second- and third-order intermodulation distortion are 85.9 dB and 80.6 dB, respectively. Residual noise from the signal generators, which was filtered by the KR Electronics 2510-SMA band-pass filter, was observed from the 38 MHz to the 42 MHz band.

Fig. 5.7 shows the measured noise floor vs RC time constant calibration codes of the prototype MASH 2-2 CTΣΔM. The RC time constant calibration code for each stage was swept while keeping that for the other stage unchanged from its nominal value obtained from startup calibration. The codes obtained from startup calibration were found to be close to optimum. Compared to the nominal codes obtained from simulation, the measured codes differ by +2 and −1 LSBs for the first and second stages, respectively. Meanwhile, the measured value of the input resistors R_1 is 475 Ω, which is about 5 % less than its nominal value.

Fig. 5.8 shows the measured STF of the prototype MASH 2-2 CTΣΔM. The STF peaking is 4.1 dB at a frequency of 320 MHz. The alias suppresion is 52.4

dB at a frequency of 950 MHz. The STF peaking, degraded alias suppression, and shallow STF notch are attributed to poor matching at high frequency due to finite OA bandwidth, finite switch on-resistance, and component mismatch. Nevertheless, the increased dynamic range required by the STF peaking is safely accomodated by the NCF and the only peaking worth considering is the 2.1 dB of first-stage STF peaking at a frequency of 170 MHz. The reduction of in-band input signal swing at the second-stage output is degraded to 3.4 dB compared to the theoretical value of 6.0 dB due to quantizer gain error attributed from the switched-capacitor common-mode level shifter during quantizer calibration.

Fig. 5.9 shows the measured power consumption breakdown of the prototype MASH 2-2 CTΣΔM. The total power consumption is 43.0 mW composed of 30.6 mW and 12.4 mW of analog and digital power consumption, respectively.

Table 5.1 compares the performance of the proposed MASH 2-2 CTΣΔM to state-of-the-art CTΣΔMs with BW $\geq$ 50 MHz and DR $\geq$ 70 dB. The FOM, defined as $\text{FOM} = \text{SNDR} + 10\log_{10}(\text{BW/P})$, is 165.1 dB which is currently the best among all CTΣΔMs with BW $\geq$ 50 MHz. In addition, the modulator does not require external software calibration and possesses minimal out-of-band STF peaking.

Table 5.1: Comparison of CTΣΔMs with BW $\geq$ 50 MHz and DR $\geq$ 70 dB.

	This Work	[92]	[87]	[81]	[72]	[71]	[69]	[55]	[41]
FS (GHz)	**1.000**	6.000	1.200	1.800	1.280	2.184	3.200	4.000	4.000
BW (MHz)	**50.3**	350.0	50.0	50.0	50.0	80.0	53.3	150.0	125.0
DR (dB)	**76.8**	72.8	72.0	85.0	75.0	73.0	88.0	73.0	70.0
Peak SNR (dB)	**75.8**	66.8	71.7	76.8	71.0	70.0	83.1	71.0	65.5
Peak SNDR (dB)	**74.4**	64.8	71.5	74.9	64.0	67.5	71.4	N/A	65.0
P (mW)	**43.0**	756.0	54.0	80.4	38.0	23.0	235.0	750.0	260.0
FOM[a](dB)	**165.1**	151.5	161.2	162.8	155.2	162.9	154.9	N/A	151.8
FOM_S[b](dB)	**167.5**	159.5	161.7	172.9	166.2	168.4	171.5	156.0	156.8
FOM_W[c](fJ/step)	**99.8**	761.1	176.0	177.1	293.6	74.2	730.8	N/A	716.3
Area (mm^2)	**0.265**	1.400	0.500	0.337	0.490	0.100	0.900	5.500	0.880
Technology (nm)	**40**	28	65	28	65	20	28	65	45

$\text{FOM} = \text{SNDR} + 10\log_{10}\left(\frac{\text{BW}}{\text{P}}\right)$; $\text{FOM}_S = \text{DR} + 10\log_{10}\left(\frac{\text{BW}}{\text{P}}\right)$;
$\text{FOM}_W = \frac{\text{P}}{2\times\text{BW}\times\text{ENOB}}$; $\text{ENOB} = \frac{\text{SNDR}-10\log_{10}(1.5)}{20\log_{10}(2)}$

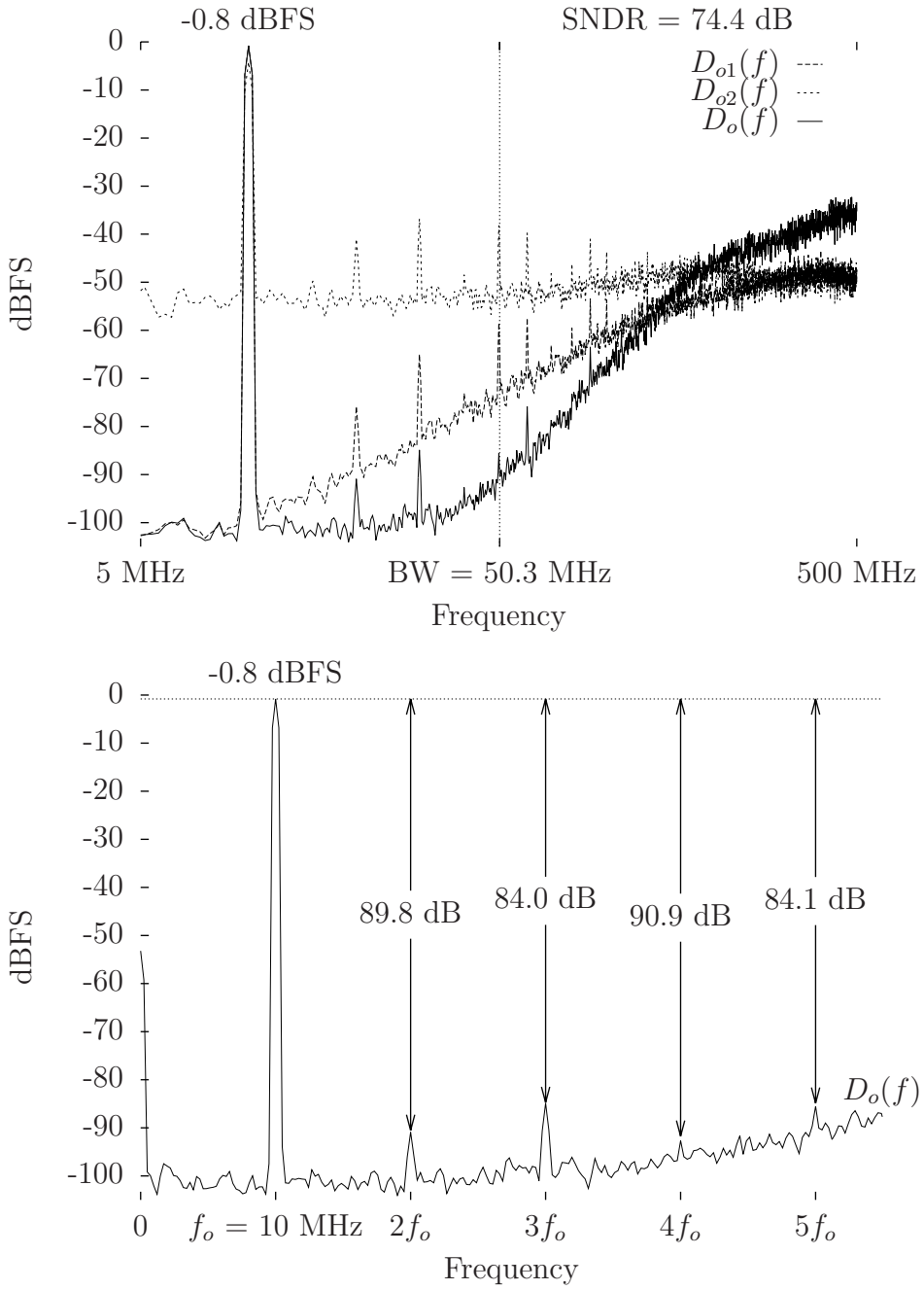


Figure 5.5: Measured single-tone FFT spectrum of the prototype MASH 2-2 CTΣΔM at peak SNDR condition.

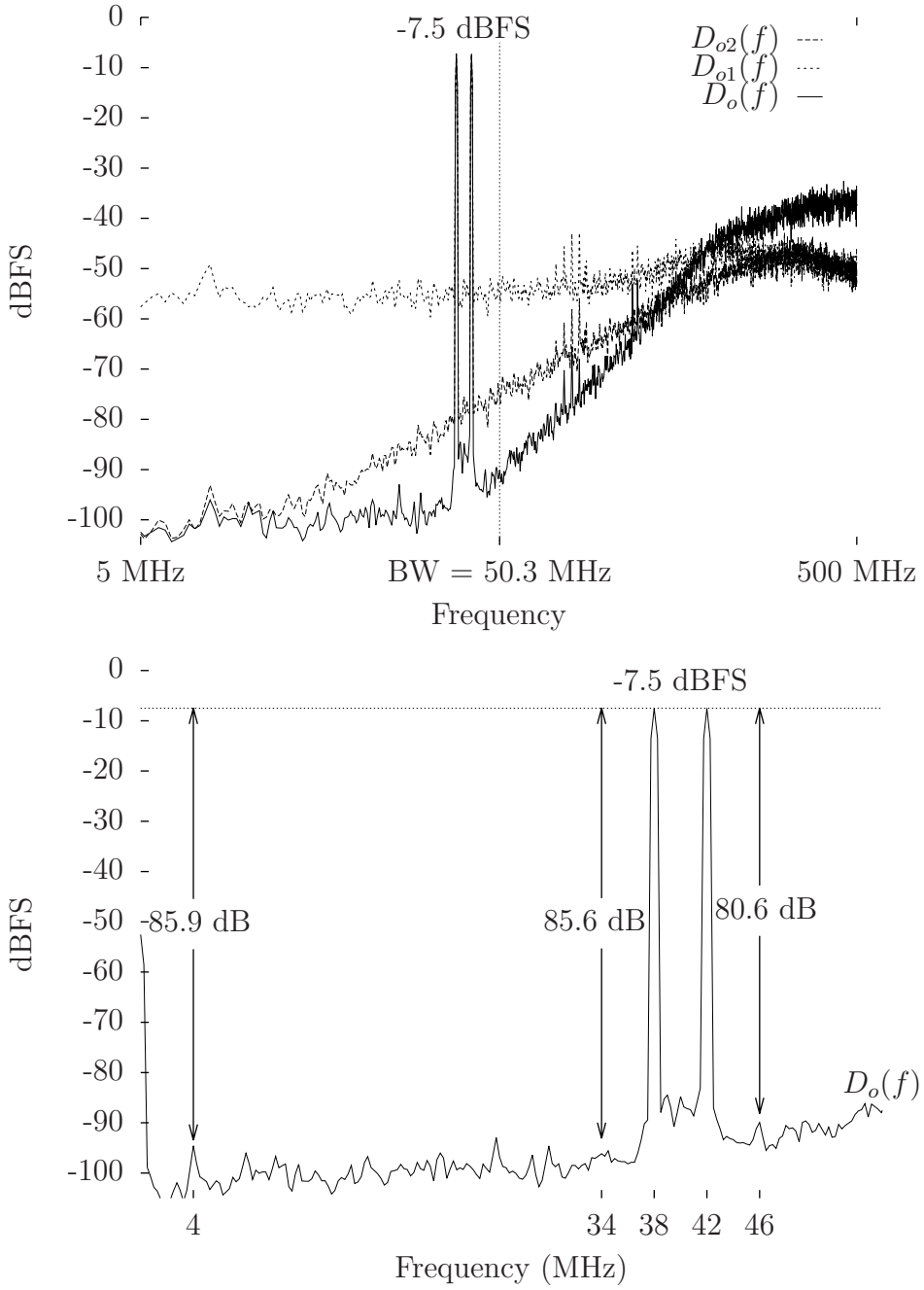


Figure 5.6: Measured two-tone FFT spectrum of the prototype MASH 2-2 CTΣΔM.

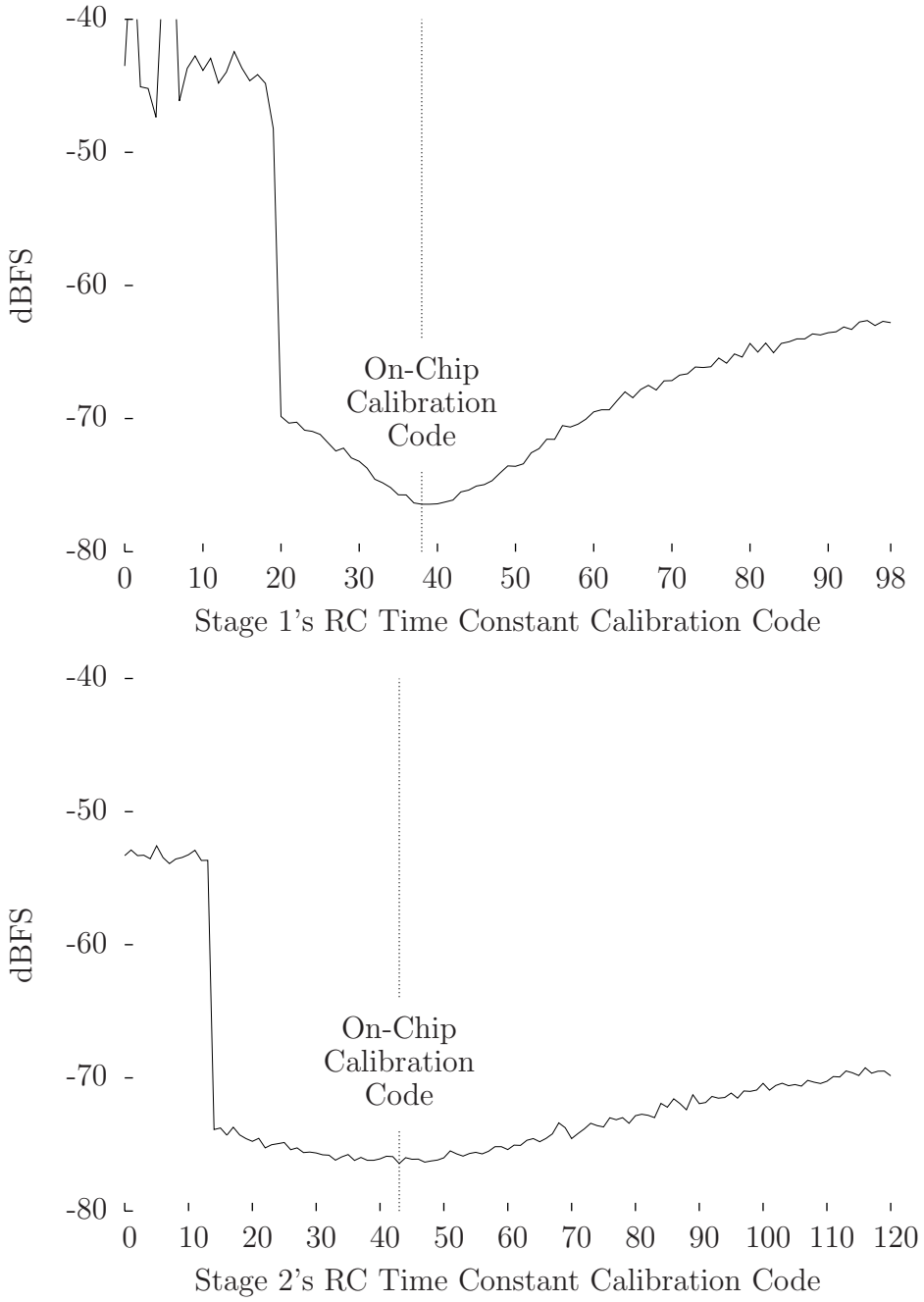


Figure 5.7: Measured noise floor vs RC time constant calibration codes of the prototype MASH 2-2 CTΣΔM.

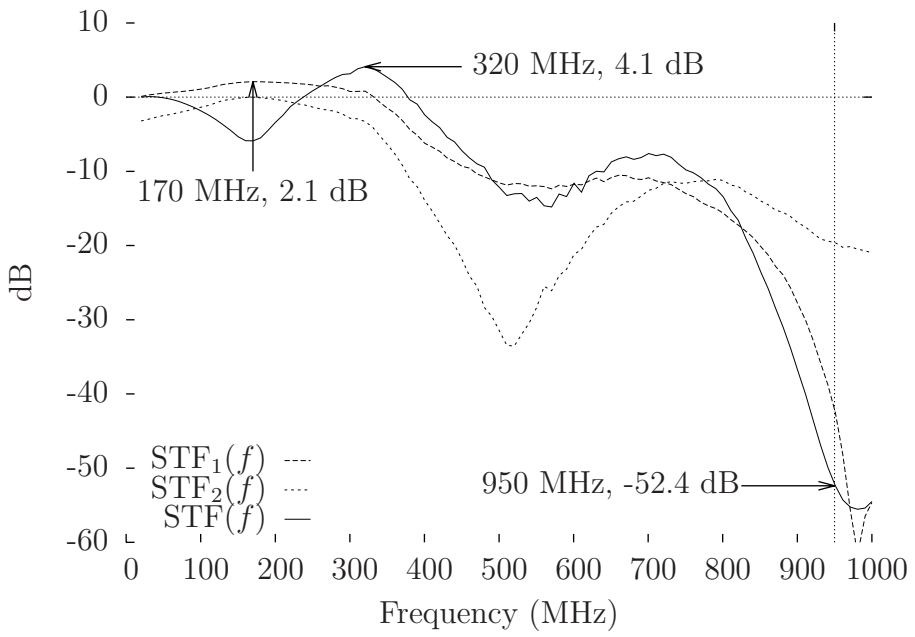


Figure 5.8: Measured STF of the prototype MASH 2-2 CTΣΔM.

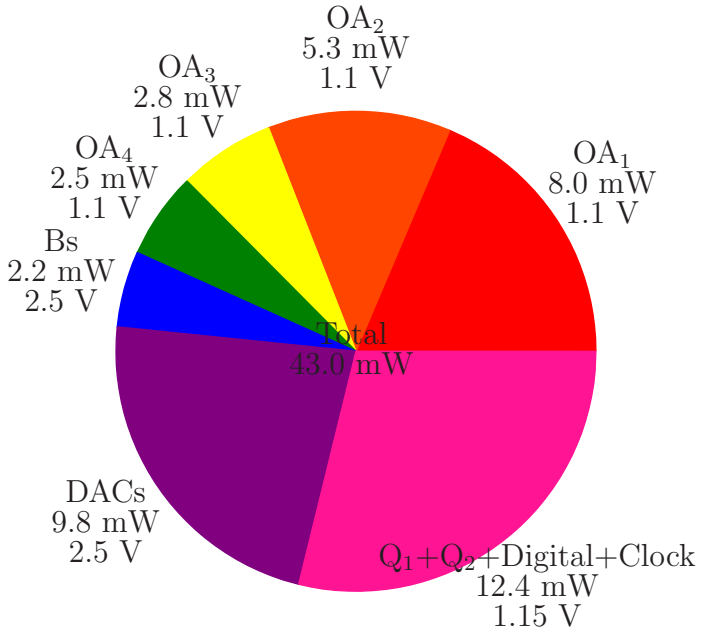


Figure 5.9: Measured power consumption breakdown of the prototype MASH 2-2 CTΣΔM.

6. CONCLUSION

The proposed MASH 2-2 CTΣΔM architecture, with on-chip RC time constant calibration circuits, multiple feedforward interstage paths, and a fully integrated NCF, provides solutions to the quantization noise leakage and non-ideal interstage connection problems in the MASH CTΣΔM architecture. The prototype chip fully integrated in 40 nm CMOS achieves 74.4 dB of SNDR, 75.8 dB of SNR, and 76.8 dB of DR in 50.3 MHz of bandwidth at 1 GHz of sampling frequency with a power consumption of only 43.0 mW. The figure-of-merit (FOM) of this design, defined as $\text{FOM} = \text{SNDR} + 10\log_{10}(\text{BW/P})$, is 165.1 dB which is currently the best among all CTΣΔMs with BW $\geq$ 50 MHz. In addition, the modulator does not require external software calibration and possesses minimal out-of-band STF peaking.

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APPENDIX A

SAMPLING OF RANDOM SIGNALS

This appendix aids the calculation of a sampled noise PSD for the cascade interconnection of a continuous-time LTI system followed by a sampler processing a white noise signal. By using the sampling relationships for random signals in (2.4) and (2.5), this system can be replaced by an equivalent discrete-time LTI system processing a white noise sequence as shown in Fig. A.1.

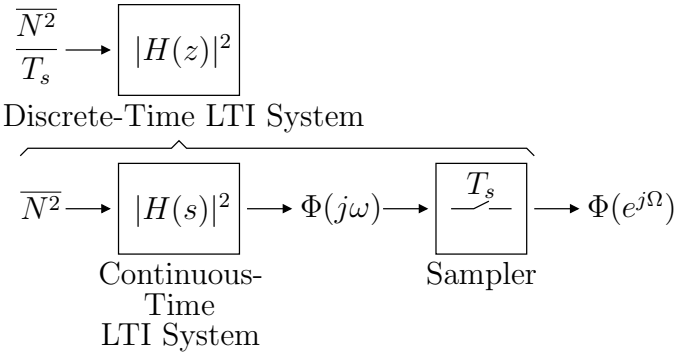

Figure A.1: Frequency domain model of the cascade interconnection of a continuous-time LTI system followed by a sampler processing a white noise signal.

The square magnitude of the equivalent discrete-time LTI system transfer function is given by

$$|H(z)|^2 = T_s \times \mathcal{Z}\left\{\mathcal{L}^{-1}\left\{|H(s)|^2\right\}|_{t=nT_s}\right\} \tag{A.1}$$

and calculated in Table A.1 for various continuous-time LTI system transfer functions.

Table A.1: $H(s)$ to $|H(z)|^2$ for the cascade interconnection of a continuous-time LTI system followed by a sampler processing a white noise signal.

$H(s)$	$\left\|H^+(z)\right\|^2$ [a,b,1,2]
1	∞
$\frac{1}{sT_s}$	$-\frac{1}{2}\frac{z^{-1}}{(1-z^{-1})^2}$
$\frac{1}{s^2T_s^2}$	$\frac{1}{12}\frac{z^{-1}+4z^{-2}+z^{-3}}{(1-z^{-1})^4}$
$\frac{1}{s^3T_s^3}$	$-\frac{1}{240}\frac{z^{-1}+26z^{-2}+66z^{-3}+26z^{-4}+z^{-5}}{(1-z^{-1})^6}$
$\frac{1}{s^4T_s^4}$	$\frac{1}{10080}\frac{z^{-1}+120z^{-2}+1191z^{-3}+2416z^{-4}+1191z^{-5}+120z^{-6}+z^{-7}}{(1-z^{-1})^8}$
$\frac{1}{1+s/\omega_p}$	$\frac{a}{2}\frac{1}{1-az^{-1}}-\frac{a}{4}$
$\frac{1}{1+s^2/\omega_o^2}$	$\frac{\theta_o}{4}\frac{(\sin(\theta_o)-\theta_o\cos(\theta_o))z^{-1}+2\theta_o z^{-2}-\theta_o\cos(\theta_o)z^{-3}}{1-2\cos(\theta_o)z^{-1}+z^{-2}}$
$\frac{s/\omega_o}{1+s^2/\omega_o^2}$	$\frac{\theta_o}{4}\frac{(-\sin(\theta_o)-\theta_o\cos(\theta_o))z^{-1}+2\theta_o z^{-2}-\theta_o\cos(\theta_o)z^{-3}}{1-2\cos(\theta_o)z^{-1}+z^{-2}}$
$\frac{1}{1+s/\omega_o/Q+s^2/\omega_o^2}$	$\frac{\theta_o Q}{2}\frac{1+r\cos(\theta_o)(\tan(\theta_o)\tan(\theta_Q)-1)z^{-1}}{1-2r\cos(\theta_o)z^{-1}+r^2z^{-2}}-\frac{\theta_o Q}{4}$
$\frac{s/\omega_o}{1+s/\omega_o/Q+s^2/\omega_o^2}$	$\frac{\theta_o Q}{2}\frac{1-r\cos(\theta_o)(\tan(\theta_o)\tan(\theta_Q)+1)z^{-1}}{1-2r\cos(\theta_o)z^{-1}+r^2z^{-2}}-\frac{\theta_o Q}{4}$

[a] $|H(z)|^2 = |H^+(z)|^2 + |H^-(z)|^2$.
[b] $|H^-(z)|^2 = |H^+(z^*)|^2$.
[1] $a = e^{-\omega_p T_s}$.
[2] $r = e^{-\frac{\omega_o T_s}{2Q}}$, $\theta_o = \omega_o T_s \cos(\theta_Q)$, and $\theta_Q = \operatorname{atan}\left(\frac{1}{\sqrt{4Q^2-1}}\right)$.

APPENDIX B

SPECTRUMS OF QUANTIZED SIGNALS

This appendix presents exact analyses on the spectrums of a quantized sinusoid signal, a white Gaussian noise signal, and their superposition. To simplify analysis, the quantization operation is assumed to be performed on continuous-time signals. Because the order of operations between sampling and quantization in a Nyquist ADC can be reversed, the continuous-time spectrums derived here can be converted to their discrete-time counterparts to take the sampling operation into account.

B.1 Spectrum of a Quantized Sinusoid Signal

The analysis on the spectrum of a quantized sinusoid signal presented here is based on the study in [115]. The output signal of a quantizer processing a sinusoid signal can be viewed as a superposition of periodic square waves.

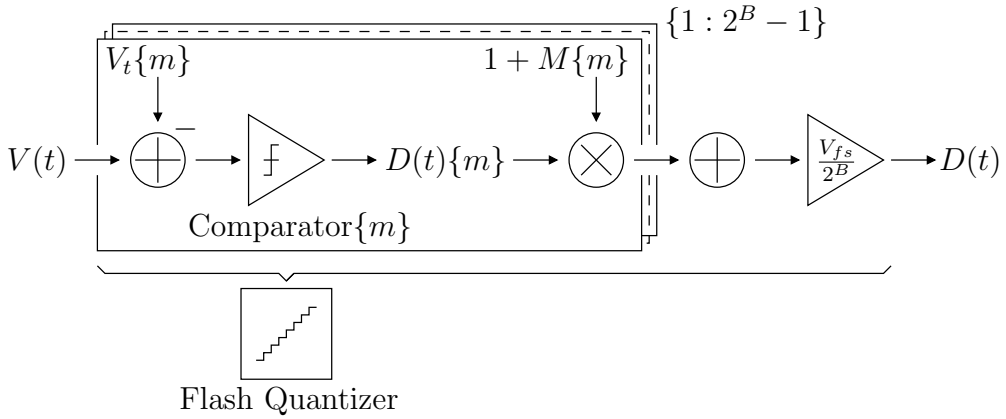

Figure B.1: Time domain model of a flash quantizer.

This observation leads to the model shown in Fig. B.1 which also describes the

operation of a flash quantizer. It consists of $2^B - 1$ comparators where B is the number of quantization bits. Each comparator, indexed by the variable m, produces an output signal $D(t)\{m\}$ of -1 if the input signal $V(t)$ is less than its threshold level $V_t\{m\}$ and $+1$ if otherwise.

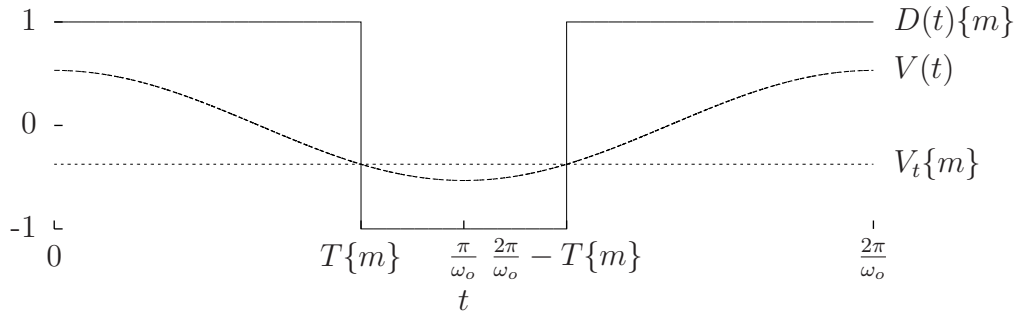

Figure B.2: Example of comparator input and output signals.

Fig. B.2 shows an example of comparator input and output signals. The comparator input signal $V(t)$ is a sinusoid of the form $A\cos(\omega_o t)$ where A and ω_o are its amplitude and angular frequency, respectively. The Fourier series representation of the comparator output signal is given by

$$D(t)\{m\} = C\{0, m\} + \sum_{k=1}^{\infty} C\{k, m\}\cos(k\omega_o t) \tag{B.1}$$

where the Fourier series coefficients $C\{0, m\}$ and $C\{k, m\}$ are given by

$$C\{0, m\} = \frac{2}{\pi}\omega_o T\{m\} - 1 \tag{B.2}$$

$$C\{k, m\} = \frac{4}{\pi k}\sin(k\omega_o T\{m\}) \tag{B.3}$$

and $T\{m\}$ is given by

$$T\{m\} = \frac{1}{\omega_o}\text{acos}\left(\max\left(\min\left(\frac{V_t\{m\}}{A}, +1\right), -1\right)\right) \tag{B.4}$$

Assuming a uniform output level distribution, the quantizer output signal is obtained by adding all the comparator output signals scaled by the factor $V_{fs}/2^B$ where V_{fs} is the quantizer full-scale. This can be mathematically written as

$$D(t) = \frac{V_{fs}}{2^B}\sum_{m=1}^{2^B-1} D(t)\{m\} \tag{B.5}$$

From (B.1) to (B.5), it can be deduced that the spectrum of a quantized sinusoid signal consists of a DC offset and infinite tones located at the harmonics of the angular frequency $k\omega_o$. The amplitudes of these harmonic tones decay in proportion to the harmonic order k.

The case of a non-uniform output level distribution is useful to analyze the DAC error spectrum in the presence of device mismatches. This is modelled in Fig. B.1 by adding the weight of each comparator output signal by a Gaussian random variable $M\{m\}$ with a mean of zero and a variance of $\overline{M^2}$. The DAC error signal is given by

$$E(t) = \frac{V_{fs}}{2^B}\sum_{m=1}^{2^B-1} M\{m\}D(t)\{m\} \tag{B.6}$$

The variance of the Fourier series coefficient of the DAC error signal is given by

$$E\left[\left(\sum_{m=1}^{2^B-1} M\{m\}C\{k,m\}\right)^2\right] = \overline{M^2}\sum_{m=1}^{2^B-1} C^2\{k,m\} \tag{B.7}$$

which is a useful quantity to calculate the expected amplitudes of the harmonic tones in the DAC error spectrum.

B.2 Spectrum of a Quantized White Gaussian Noise Signal

Suppose that the quantizer input signal is a white Gaussian noise signal with a mean of zero and a variance of $\overline{N^2}$. Fig. B.3 shows the probability density function of a white Gaussian noise signal.

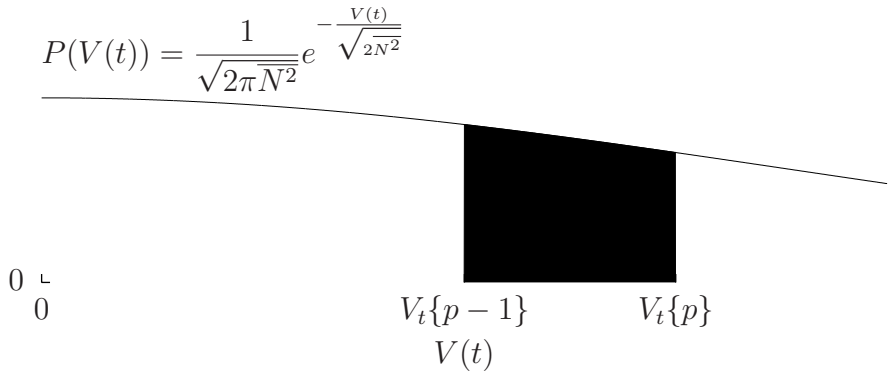

Figure B.3: Probability density function of a white Gaussian noise signal.

The autocorrelation function of the quantizer output signal is defined as

$$r(t) = E\left[D(\tau)D(\tau - t)\right] \tag{B.8}$$

The probability of the quantizer output signal to occupy a discrete output level is equal to the probability of the quantizer input signal to lie between two adjacent comparator threshold levels given by

$$P\left(D(t) = \frac{V_{fs}}{2^B}(2p - 2^B - 1)\right) = \frac{1}{2}\left(\text{erf}\left(\frac{V_t\{p\}}{\sqrt{2\overline{N^2}}}\right) - \text{erf}\left(\frac{V_t\{p-1\}}{\sqrt{2\overline{N^2}}}\right)\right) \tag{B.9}$$

which is illustrated in Fig. B.3 as the shaded region under the curve. The quantizer is assumed to have a uniform output level distribution. Two additional comparator

threshold levels of $V_t\{0\} = -\infty$ and $V_t\{2^B\} = \infty$ are needed in this derivation.

By using this information, the autocorrelation function of the quantizer output signal is given by

$$r(0) = \frac{V_{fs}^2}{2^{2B}} \sum_{p=1}^{2^B} (2p - 2^B - 1)^2 \times \frac{1}{2} \left(\text{erf}\left(\frac{V_t\{p\}}{\sqrt{2\overline{N^2}}} \right) - \text{erf}\left(\frac{V_t\{p-1\}}{\sqrt{2\overline{N^2}}} \right) \right) \tag{B.10}$$

$$\begin{aligned} r(t \neq 0) = \frac{V_{fs}^2}{2^{2B}} \sum_{p=1}^{2^B} \sum_{q=1}^{2^B} & (2p - 2^B - 1)(2q - 2^B - 1) \\ & \times \frac{1}{2} \left(\text{erf}\left(\frac{V_t\{p\}}{\sqrt{2\overline{N^2}}} \right) - \text{erf}\left(\frac{V_t\{p-1\}}{\sqrt{2\overline{N^2}}} \right) \right) \\ & \times \frac{1}{2} \left(\text{erf}\left(\frac{V_t\{q\}}{\sqrt{2\overline{N^2}}} \right) - \text{erf}\left(\frac{V_t\{q-1\}}{\sqrt{2\overline{N^2}}} \right) \right) \end{aligned} \tag{B.11}$$

At $t \neq 0$, the autocorrelation function of the quantizer output signal is simply a constant. Therefore, the spectrum of a quantized white Gaussian noise signal consists of a DC offset and a white Gaussian noise spectrum. Fig. B.4 shows an example of output vs input noise variance for a four-bit quantizer. The output noise variance increases to a certain limit dictated by the quantizer output clipping level as the input noise variance increases without bound.

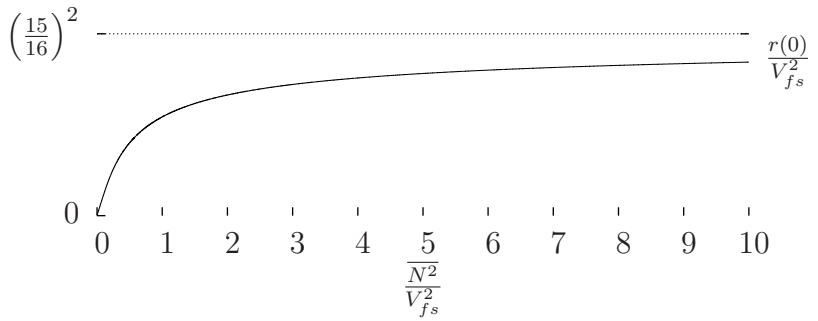

Figure B.4: Example of output vs input noise variance for a four-bit quantizer.

B.3 Spectrum of Quantized Sinusoid and White Gaussian Noise Signals

Suppose that the quantizer input signal is a superposition of a sinusoid signal and a white Gaussian noise signal with a mean of zero and a variance of $\overline{N^2}$. The input signal in this situation is equivalent to a white Gaussian noise signal with a time varying mean. The mean is equal to the sinusoid signal itself of the form $A\cos(\omega_o t)$ where A and ω_o are its amplitude and angular frequency, respectively. The probability of the quantizer output signal to occupy a discrete output level in (B.9) becomes periodic in time as follows

$$P\left(D(t) = \frac{V_{fs}}{2^B}(2p - 2^B - 1)\right) = \frac{1}{2}\left(\mathrm{erf}\left(\frac{V_t\{p\}}{\sqrt{2\overline{N^2}}}\right) - \mathrm{erf}\left(\frac{V_t\{p-1\}}{\sqrt{2\overline{N^2}}}\right)\right) + C\{0,p\} + \sum_{k=1}^{\infty} C\{k,p\}\cos(k\omega_o t) \tag{B.12}$$

The Fourier series coefficients $C\{0,p\}$ and $C\{k,p\}$ are given by

$$C\{0,p\} = \frac{1}{\sqrt{\pi}}\sum_{l=1}^{\infty}\sum_{m=l}^{\infty} B\{0,2l,2m+1,p\} \tag{B.13}$$

$$C\{k,p\}\begin{cases} \dfrac{2}{\sqrt{\pi}}\displaystyle\sum_{l=\frac{k+1}{2}}^{\infty}\sum_{m=l}^{\infty} B\{k,2l-1,2m+1,p\} \text{ if } k \text{ is odd,} \\ \dfrac{2}{\sqrt{\pi}}\displaystyle\sum_{l=\frac{k}{2}}^{\infty}\sum_{m=l}^{\infty} B\{k,2l,2m+1,p\} \text{ if } k \text{ is even.} \end{cases} \tag{B.14}$$

where $B\{k,l,m,p\}$ is given by

$$B\{k,l,m,p\} = \frac{(-1)^{\frac{m-1}{2}}}{2^l}\frac{(m-1)!}{(m-l)!\left(\frac{m-1}{2}\right)!\left(\frac{l+k}{2}\right)!\left(\frac{l-k}{2}\right)!} \times \frac{(V_t\{p\}^{m-l} - V_t\{p-1\}^{m-l})(-A)^l}{\left(2\overline{N^2}\right)^{\frac{m}{2}}} \tag{B.15}$$

The autocorrelation function of the quantizer output signal in (B.10) and (B.11)

becomes

$$r(0) = \frac{V_{fs}^2}{2^{2B}} \sum_{p=1}^{2^B} (2p - 2^B - 1)^2 \times \left(\frac{1}{2} \left(\operatorname{erf}\left(\frac{V_t\{p\}}{\sqrt{2\overline{N^2}}} \right) - \operatorname{erf}\left(\frac{V_t\{p-1\}}{\sqrt{2\overline{N^2}}} \right) \right) + C\{0,p\} \right) \tag{B.16}$$

$$r(t \neq 0) = \frac{V_{fs}^2}{2^{2B}} \sum_{p=1}^{2^B} \sum_{q=1}^{2^B} (2p - 2^B - 1)(2q - 2^B - 1) \times \left(\left(\frac{1}{2} \left(\operatorname{erf}\left(\frac{V_t\{p\}}{\sqrt{2\overline{N^2}}} \right) - \operatorname{erf}\left(\frac{V_t\{p-1\}}{\sqrt{2\overline{N^2}}} \right) \right) + C\{0,p\} \right) \times \left(\frac{1}{2} \left(\operatorname{erf}\left(\frac{V_t\{q\}}{\sqrt{2\overline{N^2}}} \right) - \operatorname{erf}\left(\frac{V_t\{q-1\}}{\sqrt{2\overline{N^2}}} \right) \right) + C\{0,q\} \right) + \frac{1}{2} \sum_{k=1}^{\infty} C\{k,p\} C\{k,q\} \cos(k\omega_o t) \right) \tag{B.17}$$

From (B.16) and (B.17), it can be deduced that the spectrum of quantized sinusoid and white Gaussian noise signals consists of a DC offset, infinite tones located at the harmonics of the angular frequency kω_o, and a white Gaussian noise spectrum. From (B.15), it can be deduced that the amplitudes of these tones is inversely proportional to the variance of the white Gaussian noise signal $\overline{N^2}$.

APPENDIX C

IMPULSE-INVARIANT TRANSFORM

This appendix shows how the feedback loop in a CTΣΔM can be modelled in the discrete-time domain. This equivalence was shown as early in [116] using time domain integral equations even before impulse-invariant transform was formally introduced in [117]. Table C.1 to C.3, derived in this appendix using impulse-invariant principle, help a designer to synthesize a CTΣΔM possessing a desired NTF or analyze the effects of some non-idealities to the modulator performance.

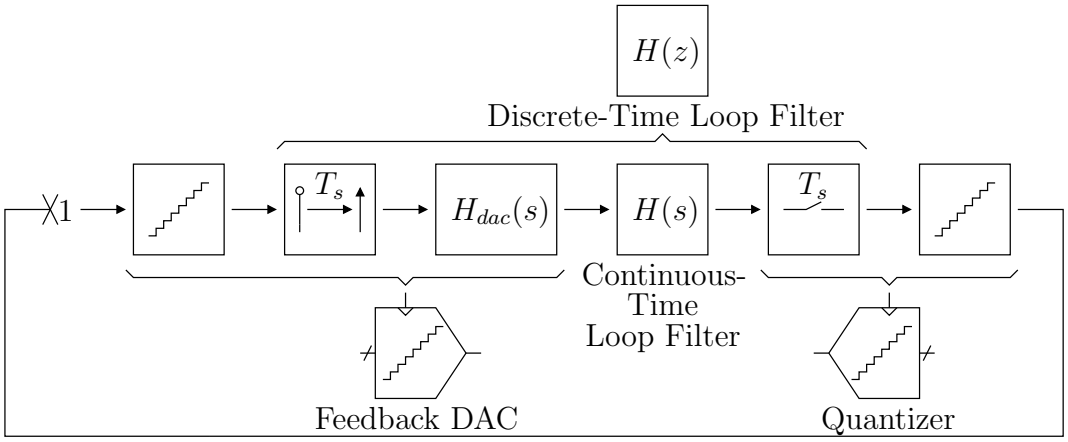

Figure C.1: Frequency domain model of an opened feedback loop in a CTΣΔM.

As shown in Fig. C.1, the feedback DAC, the continuous-time loop filter, and the sampler in the feedback loop of a CTΣΔM can be replaced by an equivalent discrete-time loop filter whose transfer function can be calculated as follows

$$H(z) = \mathcal{Z}\left\{\mathcal{L}^{-1}\left\{H_{dac}(s)H(s)\right\}|_{t=nT_s}\right\} \tag{C.1}$$

Table C.1: $H(s)$ to $H(z)$ for a CTΣΔM with a zero clock cycle delay NRZ feedback DAC. [(a)]

$H(s)$	$H(z)$ [(1,2)]
1	z^{-1}
$\frac{1}{sT_s}$	$\frac{z^{-1}}{1-z^{-1}}$
$\frac{1}{s^2T_s^2}$	$\frac{1}{2}\frac{z^{-1}+z^{-2}}{(1-z^{-1})^2}$
$\frac{1}{s^3T_s^3}$	$\frac{1}{6}\frac{z^{-1}+4z^{-2}+z^{-3}}{(1-z^{-1})^3}$
$\frac{1}{s^4T_s^4}$	$\frac{1}{24}\frac{z^{-1}+11z^{-2}+11z^{-3}+z^{-4}}{(1-z^{-1})^4}$
$\frac{1}{1+s/\omega_p}$	$z^{-1} - \frac{az^{-1}(1-z^{-1})}{1-az^{-1}}$
$\frac{1}{1+s^2/\omega_o^2}$	$z^{-1} - \frac{(\cos(\theta_o)z^{-1}-z^{-2})(1-z^{-1})}{1-2\cos(\theta_o)z^{-1}+z^{-2}}$
$\frac{s/\omega_o}{1+s^2/\omega_o^2}$	$\frac{\sin(\theta_o)z^{-1}(1-z^{-1})}{1-2\cos(\theta_o)z^{-1}+z^{-2}}$
$\frac{1}{1+s/\omega_o/Q+s^2/\omega_o^2}$	$z^{-1} - \frac{r\sec(\theta_Q)(\cos(\theta_o-\theta_Q)z^{-1}-r\cos(\theta_Q)z^{-2})(1-z^{-1})}{1-2r\cos(\theta_o)z^{-1}+r^2z^{-2}}$
$\frac{s/\omega_o}{1+s/\omega_o/Q+s^2/\omega_o^2}$	$\frac{r\sec(\theta_Q)\sin(\theta_o)z^{-1}(1-z^{-1})}{1-2r\cos(\theta_o)z^{-1}+r^2z^{-2}}$

[a] $H_{dac}(s) = \frac{1-e^{-sT_s}}{s}$.

[1] $a = e^{-\omega_p T_s}$.

[2] $r = e^{-\frac{\omega_o T_s}{2Q}}$, $\theta_o = \omega_o T_s \cos(\theta_Q)$, and $\theta_Q = \text{atan}\left(\frac{1}{\sqrt{4Q^2-1}}\right)$.

Table C.2: $H(s)$ to $H(z)$ for a CTΣΔM with a half clock cycle delay NRZ feedback DAC. [a]

$H(s)$	$H(z)$ [1,2]
1	z^{-1}
$\frac{1}{sT_s}$	$\frac{1}{2}\frac{z^{-1}+z^{-2}}{1-z^{-1}}$
$\frac{1}{s^2T_s^2}$	$\frac{1}{8}\frac{z^{-1}+6z^{-2}+z^{-3}}{(1-z^{-1})^2}$
$\frac{1}{s^3T_s^3}$	$\frac{1}{48}\frac{z^{-1}+23z^{-2}+23z^{-3}+z^{-4}}{(1-z^{-1})^3}$
$\frac{1}{s^4T_s^4}$	$\frac{1}{384}\frac{z^{-1}+76z^{-2}+230z^{-3}+76z^{-4}+z^{-5}}{(1-z^{-1})^4}$
$\frac{1}{1+s/\omega_p}$	$z^{-1} - \frac{\sqrt{a}z^{-1}(1-z^{-1})}{1-az^{-1}}$
$\frac{1}{1+s^2/\omega_o^2}$	$z^{-1} - \frac{\cos(\theta_o/2)(z^{-1}-z^{-2})(1-z^{-1})}{1-2\cos(\theta_o)z^{-1}+z^{-2}}$
$\frac{s/\omega_o}{1+s^2/\omega_o^2}$	$\frac{\sin(\theta_o/2)(z^{-1}+z^{-2})(1-z^{-1})}{1-2\cos(\theta_o)z^{-1}+z^{-2}}$
$\frac{1}{1+s/\omega_o/Q+s^2/\omega_o^2}$	$z^{-1} - \frac{\sqrt{r}\sec(\theta_Q)(\cos(\theta_o/2-\theta_Q)z^{-1}-r\cos(\theta_o/2+\theta_Q)z^{-2})(1-z^{-1})}{1-2r\cos(\theta_o)z^{-1}+r^2z^{-2}}$
$\frac{s/\omega_o}{1+s/\omega_o/Q+s^2/\omega_o^2}$	$\frac{\sqrt{r}\sec(\theta_Q)\sin(\theta_o/2)(z^{-1}+rz^{-2})(1-z^{-1})}{1-2r\cos(\theta_o)z^{-1}+r^2z^{-2}}$

[a] $H_{dac}(s) = \frac{e^{-sT_s/2}(1-e^{-sT_s})}{s}$.

[1] $a = e^{-\omega_p T_s}$.

[2] $r = e^{-\frac{\omega_o T_s}{2Q}}$, $\theta_o = \omega_o T_s \cos(\theta_Q)$, and $\theta_Q = \operatorname{atan}\left(\frac{1}{\sqrt{4Q^2-1}}\right)$.

Table C.3: $H(s)$ to $H(z)$ for a CTΣΔM with an arbitrary rectangular pulse feedback DAC. [a]

$H(s)$	$H(z,\alpha)^{(\mathrm{b,c,1,2})}$
1	$\frac{z^{-1}}{1-z^{-1}}$
$\frac{1}{sT_s}$	$\frac{z^{-1}}{(1-z^{-1})^2} - \frac{\alpha}{1}\frac{z^{-1}}{1-z^{-1}}$
$\frac{1}{s^2T_s^2}$	$\frac{1}{2}\frac{z^{-1}+z^{-2}}{(1-z^{-1})^3} - \frac{\alpha}{1}\frac{z^{-1}}{(1-z^{-1})^2} + \frac{\alpha^2}{2}\frac{z^{-1}}{1-z^{-1}}$
$\frac{1}{s^3T_s^3}$	$\frac{1}{6}\frac{z^{-1}+4z^{-2}+z^{-3}}{(1-z^{-1})^4} - \frac{\alpha}{2}\frac{z^{-1}+z^{-2}}{(1-z^{-1})^3} + \frac{\alpha^2}{2}\frac{z^{-1}}{(1-z^{-1})^2} - \frac{\alpha^3}{6}\frac{z^{-1}}{1-z^{-1}}$
$\frac{1}{s^4T_s^4}$	$\frac{1}{24}\frac{z^{-1}+11z^{-2}+11z^{-3}+z^{-4}}{(1-z^{-1})^5} - \frac{\alpha}{6}\frac{z^{-1}+4z^{-2}+z^{-3}}{(1-z^{-1})^4} + \frac{\alpha^2}{4}\frac{z^{-1}+z^{-2}}{(1-z^{-1})^3} - \frac{\alpha^3}{6}\frac{z^{-1}}{(1-z^{-1})^2} + \frac{\alpha^4}{24}\frac{z^{-1}}{1-z^{-1}}$
$\frac{1}{1+s/\omega_p}$	$\frac{z^{-1}}{1-z^{-1}} - \frac{a^{1-\alpha}z^{-1}}{1-az^{-1}}$
$\frac{1}{1+s^2/\omega_o^2}$	$\frac{z^{-1}}{1-z^{-1}} - \frac{\cos(\theta_o(1-\alpha))z^{-1}-\cos(\theta_o\alpha)z^{-2}}{1-2\cos(\theta_o)z^{-1}+z^{-2}}$
$\frac{s/\omega_o}{1+s^2/\omega_o^2}$	$\frac{\sin(\theta_o(1-\alpha))z^{-1}+\sin(\theta_o\alpha)z^{-2}}{1-2\cos(\theta_o)z^{-1}+z^{-2}}$
$\frac{1}{1+s/\omega_o/Q+s^2/\omega_o^2}$	$\frac{z^{-1}}{1-z^{-1}} - \frac{r^{1-\alpha}\sec(\theta_Q)(\cos(\theta_o(1-\alpha)-\theta_Q)z^{-1}-r\cos(\theta_o\alpha+\theta_Q)z^{-2})}{1-2r\cos(\theta_o)z^{-1}+r^2z^{-2}}$
$\frac{s/\omega_o}{1+s/\omega_o/Q+s^2/\omega_o^2}$	$\frac{r^{1-\alpha}\sec(\theta_Q)(\sin(\theta_o(1-\alpha))z^{-1}+r\sin(\theta_o\alpha)z^{-2})}{1-2r\cos(\theta_o)z^{-1}+r^2z^{-2}}$

[a] $H_{dac}(s) = \frac{e^{-s\alpha T_s}-e^{-s\beta T_s}}{s}$, $0 \le \alpha < 1$, and $0 < \beta - \alpha \le 1$.

[b] $H(z) = H(z,\alpha) - H(z,\beta)$.

[c] $H(z,\beta)\begin{cases} H(z,\alpha)|_{\alpha=\beta} & \text{if } 0 < \beta < 1, \\ z^{-1}H(z,\alpha)|_{\alpha=\beta-1} & \text{if } 1 \le \beta < 2. \end{cases}$

[1] $a = e^{-\omega_p T_s}$.

[2] $r = e^{-\frac{\omega_o T_s}{2Q}}$, $\theta_o = \omega_o T_s \cos(\theta_Q)$, and $\theta_Q = \operatorname{atan}\left(\frac{1}{\sqrt{4Q^2-1}}\right)$.