DESIGN OF A CLASS-AB AMPLIFIER FOR A 1.5 BIT MDAC OF A 12 BIT 100MSPS PIPELINE ADC

A Thesis

by

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ABSTRACT

The basic building block of a pipeline analog-to-digital converter (ADC) is the multiplying digital-to-analog converter (MDAC). The performance of the MDAC significantly depends on the performance of the operational amplifier and calibration techniques. To reduce the complexity of calibration, the operational amplifier needs to have high-linearity, high bandwidth and moderate gain.

In this work, the Op-amp specifications were derived from the pipeline ADC requirements. A novel class-AB bias scheme with feed-forward compensation, which provides high linearity and bandwidth consuming low power is proposed. The advantages of the new topology over Monticelli bias scheme and Miller's compensated amplifiers is explained. The amplifier is implemented in IBM 130nm technology and the MDAC design is used as a test bench to characterize the Op-amp performance. The proposed architecture performance is compared with class A and class-AB output stage amplifiers with Miller's compensation reported in literature. The proposed class-AB amplifier with feed forward compensation provides an open loop gain of 47dB, unit gain bandwidth of 1040 MHz and IM3 of 75dB consuming 3.88mA current. The amplifier provides the required linearity and bandwidth at much lower power consumption than the amplifiers using conventional class-AB bias schemes.

DEDICATION

To Mom, Dad, Manoj, Lakshmi & Guna

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1. INTRODUCTION

High-performance communication systems require Analog-to-Digital converters with high-resolution and bandwidth. For such applications, pipeline ADC architecture provides an optimal match for speed and power dissipations. The increasing focus on low power design has motivated a shift from using conventional class-A amplifiers to class-AB amplifiers to design the ADC. An important constrain in using a class-AB amplifier is the linearity and this thesis explores the issue in detail and presents a novel architecture for high performance class-AB amplifier with high linearity.

1.1 Motivation

Analog-to-digital converters (ADC) are important components of numerous systems which vary from digital radios, military and medical sensors to wired and wireless communications which require an interface between analog and digital domains. And with the rapid growth in speed and complexity of wireless communications, the performance expectance from data converters has also increased. There are varied ADC architectures based on conversion accuracy and speed, and no single architecture can be considered optimal for all applications and the selection of architecture can depend on resolution, speed, latency and power conversion. Figure 1 illustrates some of the architectures and their intended resolution

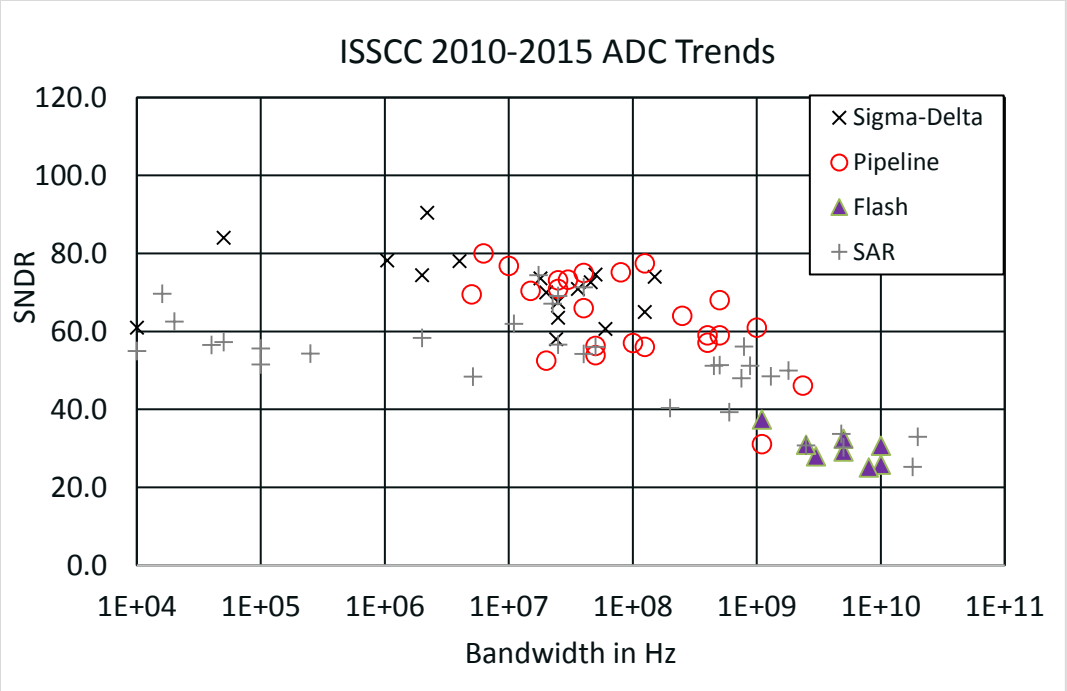

Figure 1: Types of ADC [1]

The focus of this thesis is on medium resolution and high speed pipeline ADC, specifically a 12 bit resolution and a sampling speed of 100 MSPS. [2-7] have shown resolutions of 12 bits and higher but the common factor among them is the high power consumption. The main contributors for power consumption in a pipeline ADC are the Op-amps and traditionally higher resolutions would require a high gain, high speed amplifiers which required huge currents. But as analyzed and proved in [8, 9, 10] digital calibration techniques can be used to relax the gain requirements of the amplifier and hence lower the power consumption. This thesis focuses in this research direction and proposes an architecture to achieve the required resolution using a low power Op-amp.

1.2 Thesis organization

Following the introduction, the next section focuses on presenting the basics of pipeline ADC, and highlights the requirements of the Op-amps used in a pipeline ADC

Section 3, introduces the existing architectures of class-AB amplifiers and their drawbacks and provides an in-depth analysis of the proposed amplifier topology and design procedure

Section 4, discusses the requirements and implementation of switches in the design of an MDAC, specifically the boot-strap implementation and design procedure

Section 5, provides the schematic simulation test-benches and results of the amplifier and the switch. The amplifier specifications are compared to various other amplifier architectures

Section 6 presents the conclusion of the thesis.

2. PIPELINE ADC BASICS

The function of an ADC is to convert a continuous time, continuous value signal into a discrete-time, discrete-value signal. The first conversion in the time domain is called sampling and the next conversion in the value is called signal-level-quantization or quantization.

Sampling can be explained using the simple circuit shown in Figure 2. While the switch is closed, the voltage on the capacitor tracks the input voltage and when the switch opens at $t = t_0$, the capacitor holds the value of the input at the switching instant.

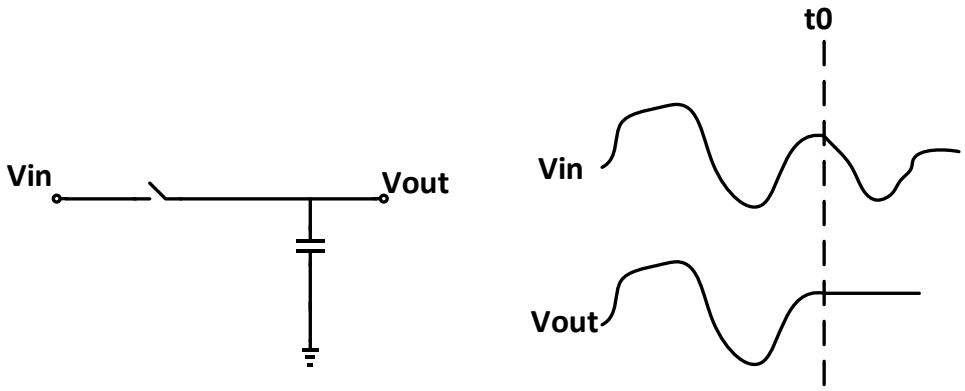

Figure 2: Sampling example

Quantization is converting the sampled analog value to a digital value by comparing the analog value to a reference level. A simple example would be a 1-bit quantization using reference level “0”, all positive sampled values will be “1” and all 0 and negative values will be “0”. As the resolution of digital value increases the number of reference levels also increases. The two basic implementations of quantization are serial and parallel quantization.

In a parallel quantization, the signal is compared with all the reference levels at once and the exact digital value of the signal is determined as in a Flash ADC. Consider the Flash ADC and the quantization error in Figure 3, as can be seen the quantization error

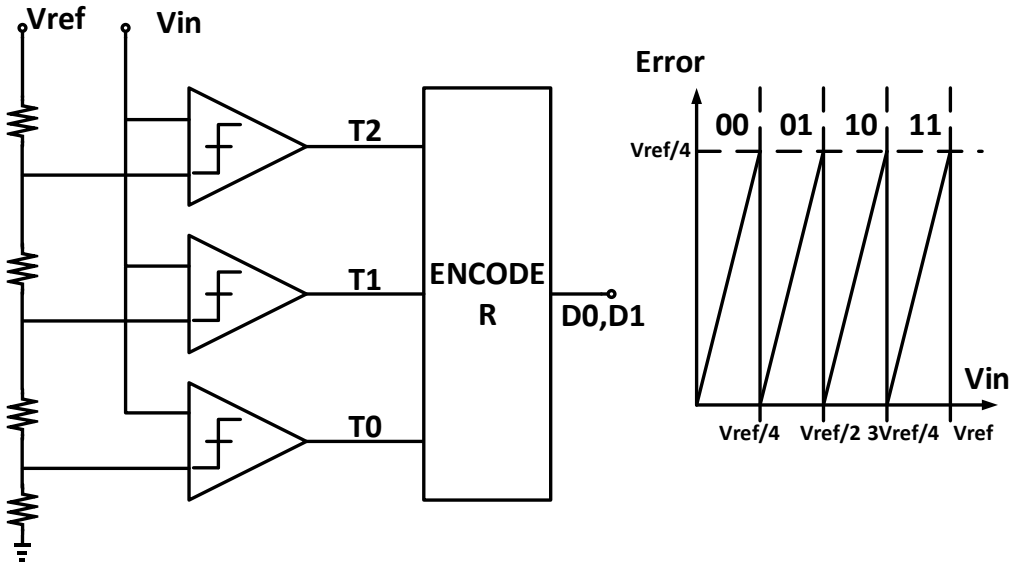

Figure 3: Flash ADC and the quantization error

it-self contains information about the input signal and if this error can be extracted and amplified, more bits can be resolved from the error; such an architecture is called Two-

Step ADC. To get the quantization error, the original input signal can be subtracted by the analog equivalent of the resolved digital bits. An amplifier is used to amplify the error value to the analog reference voltage as shown in Figure 4. The Two-step ADC can be further extended to multiple series stages and this forms the basis for a pipeline ADC.

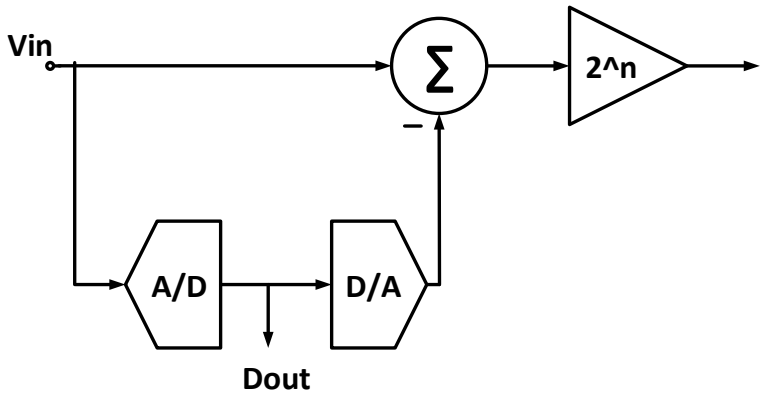

Figure 4: Quantization error signal generation and amplification

Figure 5 shows a block diagram of a pipelined ADC: the structure in Figure 4 is repeated multiple times to match the required resolution, and the last stage is generally a Flash ADC.

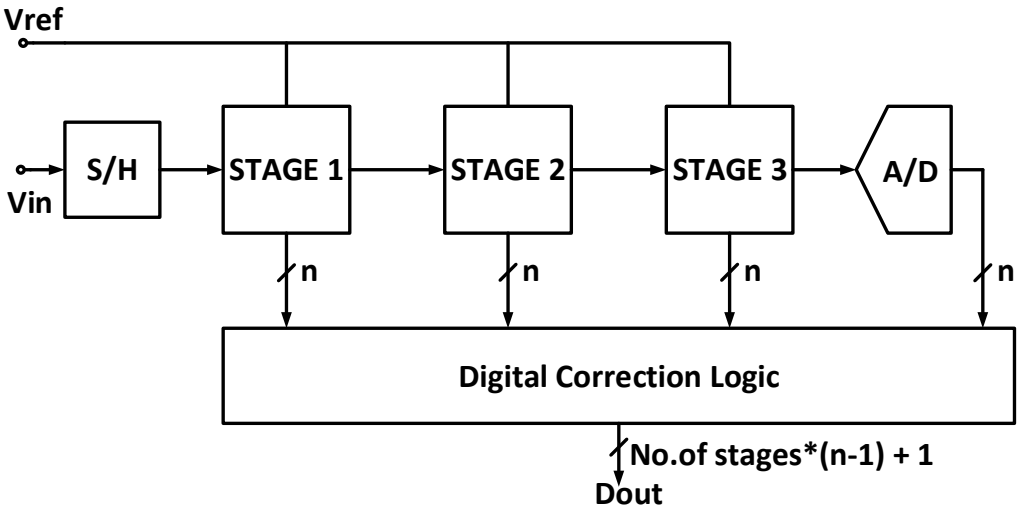

Figure 5: Pipelined ADC

Multiplying Digital-to-Analog Converters (MDAC) are the basic building blocks of pipeline ADC. MDAC's combine sample and hold, subtraction, DAC and gain operations shown in Figure 4 into a simple switched capacitor circuit to provide per-stage resolved digital output of an ADC. The basic block diagram of a single ended 1.5 bit MDAC is shown in Figure 6.

During the sampling phase Φ1 the input ('V_{in}') is sampled on the capacitors C_1 and C_2 and depending on the value of V_{in} the decoder selects the voltage to be applied to C_2 ('V_s') during hold stage Φ2

If $V_{in} < -V_R/4$, then $V_s = -V_R$ and bj = 00

If $-V_R/4 <= V_{in} <= V_R/4$, then $V_s = 0$ and bj = 01,

If $V_{in} > V_R/4$, then $V_s = V_R$ and bj = 10

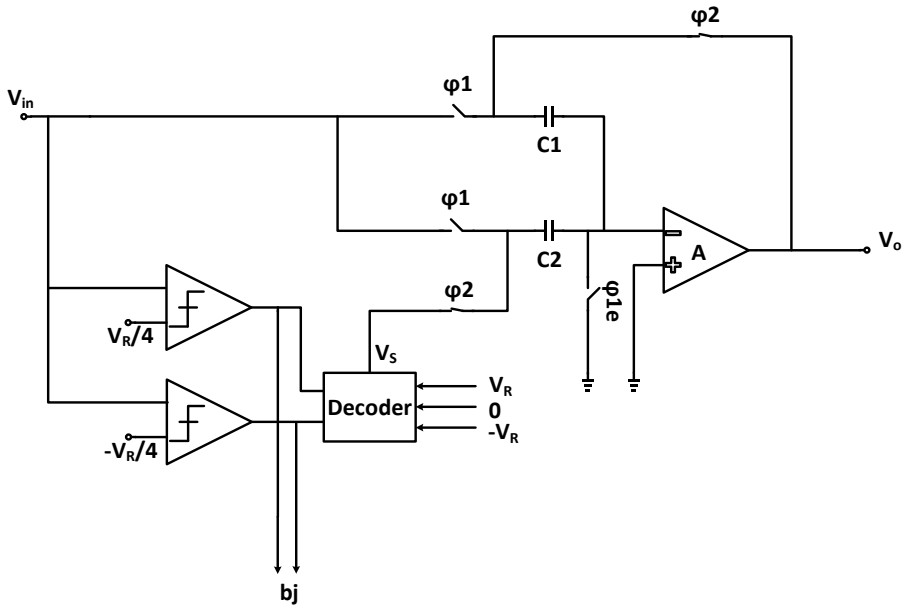

Figure 6: 1.5 bit MDAC

Based on the charge conservation principle, assuming ideal amplifier and capacitors the transfer function from input to the output can be calculated as and is shown in Figure 7.

$$V_o = 2V_{in} - (bj - 1)V_R \qquad 2.1$$

2.1 MDAC error sources

For calculating equation 2.1 we have assumed the Op-amp, Capacitors and Switches and the Comparators to be ideal but in reality this is not the case and this section explains the error sources in the MDAC and ways to overcome

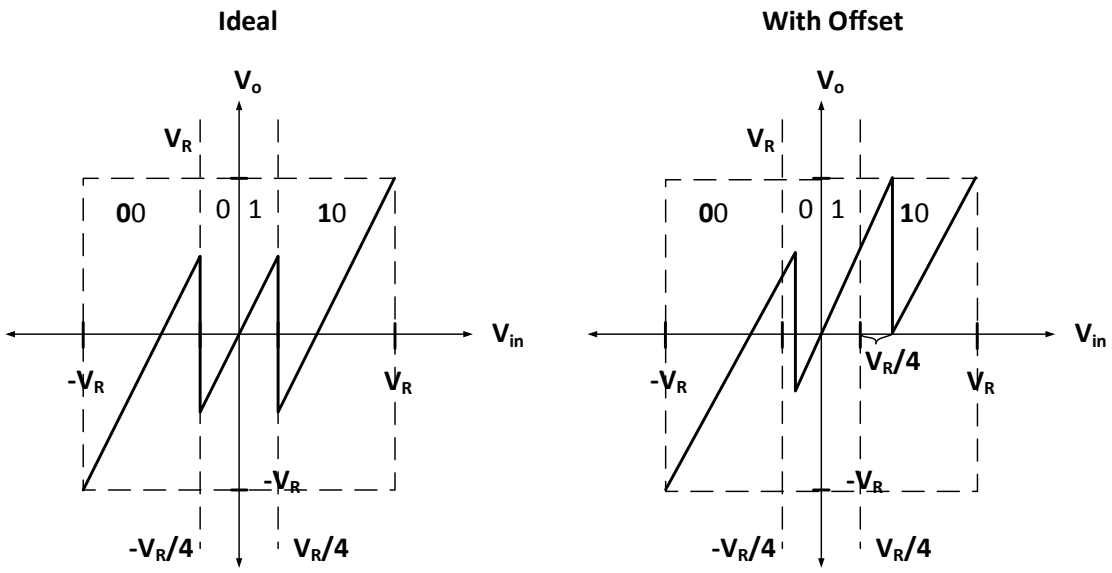

Figure 7: 1.5 bit MDAC transfer function

2.1.1 Offset error

The common sources of offset errors are charge injection, Op-amp offset, Comparator offset and the DAC offset

- Charge injection is generally due to the switches used in the design; when a switch is turned off there exists some charge in the channel, which is dumped on to the connected capacitor. If the capacitor is a sampling or feedback capacitor it alters the signal level. This can be reduced using techniques like early-clocking(used in this design), dummy switches and complimentary switches [11]
- Op-amp offset is generally caused by the mismatches in the transistors and can be reduced using proper layout techniques and also using the concept of offset storage. The offset voltage of the amplifier is sampled onto the capacitor during

one phase and then it is subtracted from the signal during the other phase with some processing as explained in [8].

- Due to the redundancy present in the MDAC, the comparator offset up to $V_R/4$ can be tolerated.
- DAC offset is not reflected in the digital output of the stage but does influence the analog output of the stage. Hence it cannot be corrected by the redundancy in the MDAC stages and careful design and layout techniques have to be used to reduce the offset.

2.1.2 Gain errors and non-linear errors

Gain error at the output of MDAC can be caused by the mismatch in the capacitor ratio, the finite gain of Op-amp and settling time. The linearity and finite gain of the Op-amp and the switch linearity effects the linearity of the MDAC.

- The transfer function of a 1.5 bit MDAC considering finite amplifier gain 'A', capacitor mismatch and amplifier offset is given by

$$V_o = \left(\frac{(C2+C1)}{C1+\frac{C2+C1}{A}}\right) * V_{in} - \left((bj-1) * \left(\frac{C2}{C1+\frac{C2+C1}{A}}\right)\right) * V_R + \left(\frac{(C2+C1)}{C1+\frac{C2+C1}{A}}\right) * V_{OS} \quad 2.2$$

And in-order to minimize the gain errors, we need good matching of the capacitors as well as a high open-loop gain for the amplifier, which could result in power hungry amplifiers. Instead error correction techniques (calibration) have been used [12-17] for high resolution ADC which significantly relaxes the gain requirements and enables power and area saving. Digital calibration is preferred over analog calibration due to higher robustness and accuracy.

Calibration of pipelined ADC can be classified into two operation modes: foreground and back-ground. In foreground calibration, the ADC conversion process is halted and a known test signal is applied and the calibration parameters are determined. Back-ground calibration does not interrupt the ADC conversion process and can be further split into two major types: a) channel error identification and b) correlation-based. In channel error identification an additional slow but accurate ADC acts as a reference and the output of the pipelined ADC is compared with the reference to determine the error function [12-15]. Correlation-based approach uses statistical estimation to determine the error function without necessitating an additional ADC [16-17].

- Although using low gain amplifiers digital calibration corrects for gain errors, low gain amplifiers can introduce significant harmonic distortion and non-linearity. There are techniques to calibrate non-linear errors, but they result in complex power hungry circuits [18] and consume significant time to identify the error function. Hence an amplifier to be used in digitally calibrated pipeline ADC will have high linearity and moderate gain, which is the primary focus of this thesis. Switch linearity can be

improved using boot-strapping techniques [19, 20] which can achieve up to 15 bit linearity.

2.2 Components specification

2.2.1 Sampling capacitors

The most dominating factor which impacts the resolution of a pipeline ADC is the noise in the circuit and the key contributors are KT/C thermal noise on the capacitors, active circuit noise and digital switching noise. Since thermal noise is inversely proportional to the value of the sampling capacitors, the larger the capacitors the smaller the noise and its value is based on the noise budget.

Since the ADC is a 12 bit, the output of the first MDAC(1.5bit) has to at least have a SNR of 11 bits. If the differential peak-peak swing at the output is 1.2V, based on the below calculation, the noise budge is

$$SNR = 6.02 * 11 + 1.76 = 68dB \quad (2.3)$$

$$SNR = 10 * 10^6 \quad (2.4)$$

The signal power at the output of the MDAC

$$S_p = \frac{0.6 * 0.6}{2} = 0.18 \quad (2.5)$$

$$Noise\_power = S_n = \frac{S_p}{SNR} = \frac{0.18}{6.31 * 10^6} = 1.8 * 10^{-8}V^2 \quad (2.6)$$

The total noise at the output of the differential MDAC is calculated in [21] and is given by [excluding the switch resistance]

$$N_o^2 = \frac{4KT}{C} + 2 * kT * UGB * R_{op} \quad (2.7)$$

Where C is the sampling capacitor (C1 and C2) and UGB is the Gain-bandwidth of the amplifier and R_{op} is the equivalent Op-amp noise resistance. From the architecture of the amplifier described in chapter 3, the noise significantly effects the power consumption. Hence, a large chunk of noise budget is left for the amplifier and the capacitor noise budget is taken to be 0.72*10^-8V^2. Based on the first term, the sampling capacitor values can be calculated to be 2.3pF.

2.2.2 Amplifier specification

Slew current:

To determine the slew current requirement of the amplifier, assume that the capacitors C1 and C2 initially sample Vin during the sampling stage and the load capacitor is charged to Vx. When the switches toggle, the MDAC gets to the hold phase as shown in Figure 8 and, because of charge redistribution

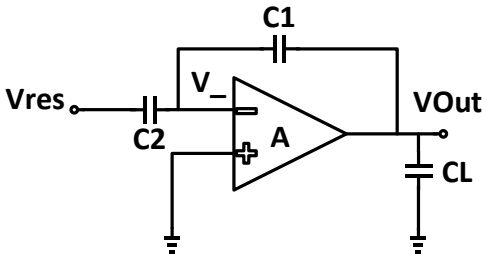

Figure 8: MDAC in hold state

At V_:

$$C2\big((Vres - V\_) - Vin\big) + C1\big((VOut - V\_) - Vin\big) = 0 \qquad 2.8$$

At VOut:

$$C1\big((VOut - V\_) - Vin\big) + CL(VOut - Vx) = 0. \quad (2.9)$$

On solving the equations we get

$$V\_initial = -Vin + \left(\frac{\Big(\big((C1 + CL) * C2 * Vres\big) + (CL * C1 * Vx)\Big)}{C1 * CL + C2 * CL + C1 * C2}\right) \quad (2.10)$$

$$VOutinitial = \left(\frac{\Big(\big((C1 + C2) * CL * Vx\big) + (C1 * C2 * Vres)\Big)}{C1 * CL + C2 * CL + C1 * C2}\right). \quad (2.11)$$

From these initial values, the V_ terminal slews till it reaches √2*Voverdrive and then the amplifier operates in linear region, and if we assume the slewing time to be 1ns, then the slewing current can be calculated using

$$VOutfinal = VOutinitial - \left(1 + \left(\frac{C2}{C1}\right)\right) * V_{initial} - \sqrt{2} * Voverdrive \quad (2.12)$$

$$I = \left(CL * \frac{(VOutfinal - VOutinitial)}{1ns}\right) - \left(C2 * \frac{(V_{initial} - sqrt(2) * Voverdrive)}{1ns}\right) \quad (2.13)$$

Using the values C2 = C1 = CL = 2.3pF, Voverdrive = 0.2V, Vin = 0.3, Vx = -0.3, 0 we get the slew-current to be 1.4mA and 690uA. Hence, the maximum current to be supplied by the output stage of the amplifier should be >= 1.4mA.

Gain-Bandwidth product:

If we assume the Op-amp to be a single pole system, then the closed loop settling error is given by

$$Error = Vin * \left(e^{-(\beta * UGB * t_{settle})}\right). \quad 2.14$$

The MDAC output has to settle to more than 11 bit accuracy in about 3ns and Vin = 1.2, β = 0.5. These values will give an open loop gain-bandwidth product of 810MHz.

Output swing, Gain and Noise:

Since we are targeting a differential input peak-peak signal of 1.2V, the output swing has to be 1.2V. As explained before, a moderate gain amplifier with a high linearity would be sufficient to attain the required resolution so, the targeted gain is 45dB. Based on the noise budget, the noise of the amplifier has to be less than $180uV^2$.

Linearity:

As explained in [9], a highly linear amplifier can decrease the required loop gain and as such, the open-loop gain of the amplifier. The closed loop non-linearity can be defined as

$$Closed\_loop\ IM3 = \frac{Open\_loop\ IM3}{(1 + loopgain)^3} \quad 2.15$$

Since we are targeting a lower loop gain, the open loop IM3 should be large and the value at the output of the MDAC should be at least 68dB, which is 11-bit resolution.

3. AMPLIFIER DESIGN

In section 2, the amplifier specifications required by the MDAC were calculated. In this section, the specifications are listed and the design of the amplifier is discussed in detail. Class-A and class-AB output stage based amplifiers are discussed, and various compensation schemes to improve the bandwidth are analyzed. A new class-AB bias scheme with feed forward compensation and source degenerated CMFB amplifier is proposed and discussed in-detail.

3.1 Amplifier specifications

Table 1 summarizes the design specifications required for the amplifier to be used for the MDAC

Table 1: Amplifier specifications

Parameter	Value
DC Gain	≥ 45 dB
Gain-bandwidth product	≥ 850MHz
Output linear range (fully-differential)	≥ 1.2V
Power	minimal
Squared Input referred noise in 900MHz	≤ 1.8e-08
Load	3.5 pF
Settling time	<=5ns
IM3 at 40MHz	>= 68 dB

3.2 Amplifier topology

As can be seen from the specifications, the required amplifier is a moderate gain, high bandwidth, highly linear amplifier with a capability to drive a huge capacitor. The moderate gain and high bandwidth requirement can be achieved by using a multi-stage amplifier, but as we increase the number of stages the power consumption increases. The linearity and power consumption of the amplifier significantly depends on the output stage linearity and the ability to drive a large capacitor. The type of compensation used to achieve stability provides a choice between Miller compensation and feed-forward compensation. Based on the trade-offs and the overall requirement of a low-power and highly linear amplifier, how the topology was selected is explained in the next few sub-sections.

3.2.1 Output stage

As explained in [9], for an amplifier with a moderate gain in the output stage, the change in the drain to source voltages of the transistors in the output stage is significant when compared with internal stages. Hence, the output stage contributes the most towards non-linearity. The output stage also has to supply sufficient current to charge/discharge the load during slewing. The two types of output stages studied were class-A and class-AB. Based on the power consumption, class-AB with a novel biasing scheme to improve linearity was chosen for the design.

Class-A output stage:

A class-A output stage is always ON for the entire signal cycle, and this is achieved by biasing the output transistor with a fixed current source. Figure 9 shows a simple class-A output stage and its small signal characteristics.

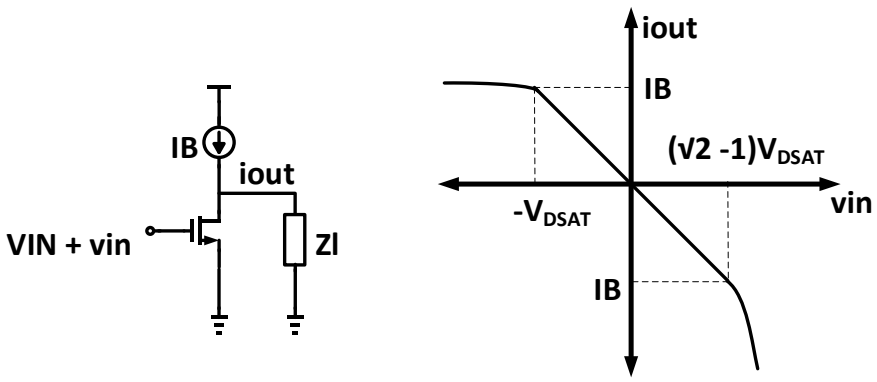

Figure 9: Class-A output stage and its I-V characteristics

The output current into the load is

$$iout = IB - IM1 \tag{3.1}$$

where IM1 is the transistor current. As vin increases from -∞, as long as vin < $-V_{DSAT}$ the transistor is cut off, and the complete bias current flows into the load capacitor. The capacitor charges at the rate

$$SR\_rise = \frac{IB}{CL} \tag{3.2}$$

When vin => $-V_{DSAT}$ and the transistor is expected to operate in saturation the output current is given by

$$iout = IB - K(V_{DSAT} + vin)^2 \quad 3.3$$

$$iout = -KV_{DSAT}vin - Kvin^2 \quad 3.4$$

$$K = \frac{u_n CoxW}{2 * L} \quad 3.5$$

From the above equation for smaller values of vin, the linear term dominates and the output current varies linearly with vin. And as vin increases the quadratic term starts dominating as can be seen in Figure 9.

When vin is small variation around $V_{DSAT} + Vth$ the output stage is highly linear and class-A is a popular choice for Op-amps that need to be linear [22, 23, 24], but the slew rate is limited by the bias current (For differential operation the quadratic term cancels out, but third order non-linearity exists). As discussed, for a 12-bit ADC the sampling capacitor of the first MDAC is very large. To support the required slew rate if class-A is used as the output stage the biasing current needs to be very large dissipating excessive power.

Class-AB output stage:

Class-AB stage consists of a PMOS and NMOS biased at a quiescent current and is theoretically capable of driving infinite current into the load. Figure 10 shows an ideal class-AB output stage, and the output current vs input voltage characteristics. When vin = 0, iout = 0 and the quiescent current I_Q flows through the PMOS and NMOS.

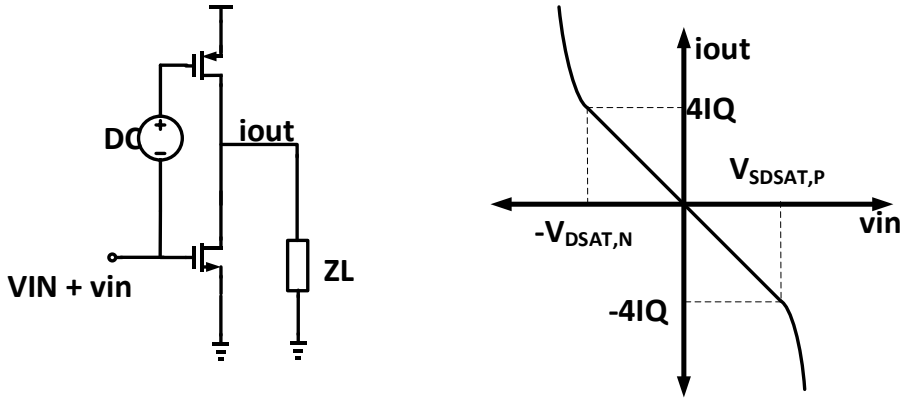

Figure 10: Class-AB output stage and its I-V characteristics

For the condition when $-V_{DSAT,N} <= vin <= V_{SDSAT,P}$, both the transistors are in saturation and

$$iout = ip - in. \tag{3.6}$$

Assuming $V_{DSAT,N} = V_{SDSAT,P}$ and $K_n = K_p$ we get

$$iout = K_p(V_{SDSAT} - vin)^2 - K_n(V_{DSSAT} + vin)^2 \tag{3.7}$$

$$iout = -4KV_{DSSAT}vin. \tag{3.8}$$

For the other cases $vin < -V_{DSAT,N}$, $vin > V_{DSAT,P}$ the NMOS and PMOS are cutoff respectively. The other MOSFET directly drives the output, and the current depends on the VGS of the MOSFET but not the quiescent current. The slew rate can be defined as

$$SR_{rise} = \frac{K_P\left(V_{SDSAT,P} - vin\right)^2}{C_L}; \tag{3.9}$$

$$SR_{fall} = -\frac{K_N\left(V_{DSAT,N} + vin\right)^2}{C_L} \quad 3.10$$

Hence, for smaller variations of vin around $V_{DSAT.N}/V_{DSAT,P}$ the class-AB stage is highly linear and the biasing power requirement during quiescent condition is much smaller than class-A stage. When there is a large capacitive load or a small resistive load at the output, class-AB stages can provide an optimum match for power vs linearity. And also, for a given current the small signal gain is higher for class-AB because both the transistors provide gain.

In the above discussion we conveniently assumed that the small signal 'vin' is transmitted from NMOS to PMOS without any variation, but in practical design there could be a slight variation. In case of variations the equations would become

$$iout = K_p(V_{SDSAT} - vinp)^2 - K_n(V_{DSSAT} + vinn)^2 \quad 3.11$$

$$iout = -2KV_{DSSAT}(vinp + vinn) + K(vinp^2 - vinn^2). \quad 3.12$$

This would result in a quadratic term in the current equation and there by introducing non-linearity at the output. Hence, to achieve a highly linear output stage the DC level shifter/biasing circuit used for class-AB needs to

1. Transmit same small signal 'vin' to NMOS and PMOS which means act as a short circuit for small signal.
2. Bias the NMOS and PMOS with a fixed quiescent current.
3. It should not impose a limit on the current that can be driven to the load.

Several class-AB schemes have been reported in the literature [25, 26, 27, 28] with the focus on implementation of the DC level shifter to efficiently support the three

functions mentioned earlier. Among them Monticelli bias [27] scheme is the most popular approach and is shown in Figure 11.

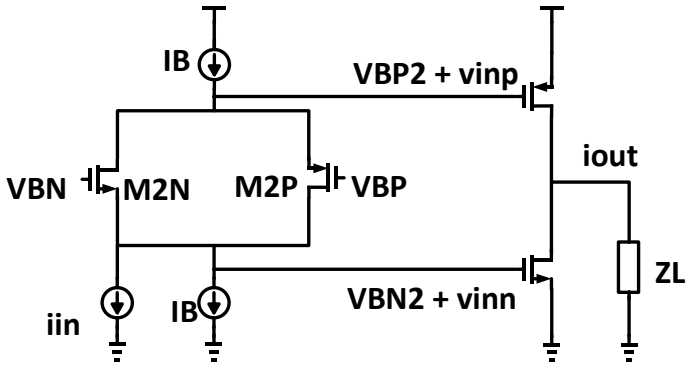

Figure 11: Class-AB output stage with Monticelli bias

Monticelli bias scheme is based on quadratic trans-linearity principle, and the transistors M2P and M2N act as the DC level shifters. In quiescent condition the current through each transistor is IB/2. When the previous stage in the Op-amp generates a small signal current iin, depending on the impedance at node vinn, the voltage vinn varies with iin. If iin increases, vinn decreases and the gate to source voltage of M2N increases, and the current flowing through M2N increases. Since, the small signal current circulates between M2N and M2P, the current through M2P decreases and the voltage at vinp decreases. Similarly when iin decreases vinn and vinp increase and the small signal transfer function between vinn and vinp is given by

$$\frac{vinp}{vinn} = \frac{gm_{M2N}Zout}{1 + gm_{M2P}Zout} \quad 3.13$$

Where gm_{M2N} and gm_{M2P} are the trans-conductance of M2N and M2P and Zout is the small signal impedance at the node vinp.

As can be seen from the above equation and explained in [29], the transfer function heavily depends on the trans-conductance of M2N and M2P, and this can add to the non-linearity in two aspects

a) Trans-conductance and impedance of the transistor is by itself non-linear and varies with the drain-to-source voltage.
b) As explained in equation 3.12, if the transfer function between vinp and vinn is not unity, the quadratic terms in the output current equation can cause non-linearity. And for the transfer function to be unity we need a good match between gm_{M2N} and gm_{M2P} which is not always possible in real implementation.
c) In addition Monticelli scheme also suffers from hard discontinuities in the transfer function when iin is very large and pushes either M2N or M2P into linear region[29]

3.2.2 Proposed DC-level shifter for class-AB stage

Since the focus is to have same small signal at the gate of NMOS and PMOS of the class-AB stage, a capacitor which acts as a short circuit at high frequencies can be used. Consider the circuit in Figure 12, the VBIASN is generated using common mode feedback to drive the required amount of quiescent current. Rb and Cp are the bias

generator resistance and capacitance. The transfer function from vinp to vinn can be written as

$$\frac{viin}{viip} = \frac{(Cb * Rb) * s}{(Cb * Rb + Cp * Rb) * s + 1} \quad 3.14$$

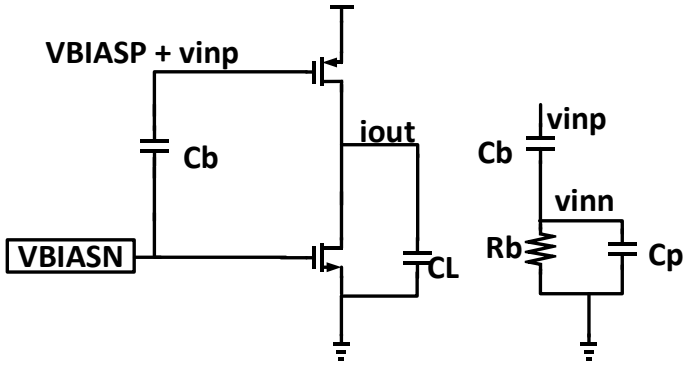

Figure 12: Level-shifter circuit and small signal equivalent circuit

If Cb >> Cp, at higher frequencies the transfer function becomes close to 1, but at lower frequencies there is a zero at origin and there will be a mismatch between vinp and vinn as can be seen in Figure 13. To reduce the mismatch a large resistor Rb is required.

Consider the circuit in Figure 14, a resistor is added in parallel to the Capacitor Cb

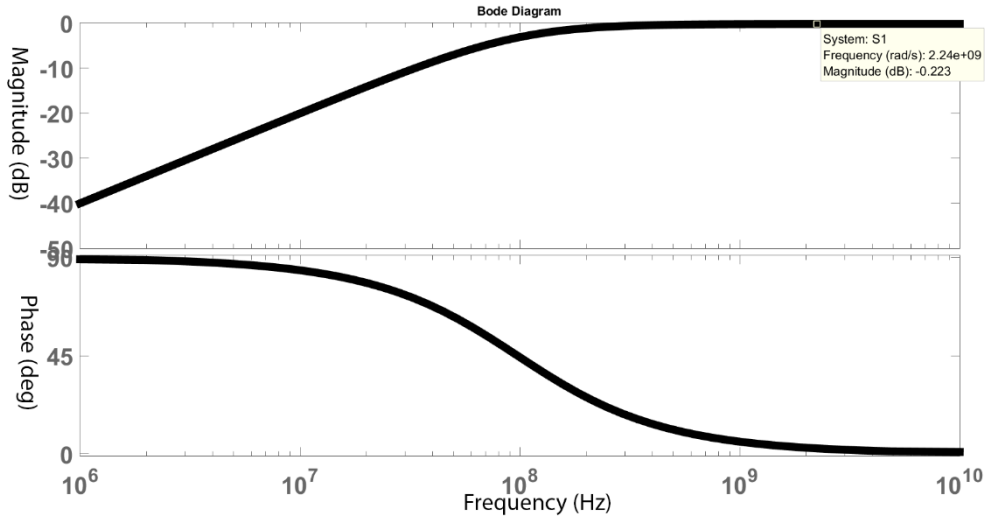

Figure 13: Transfer function of capacitor-only level shifter

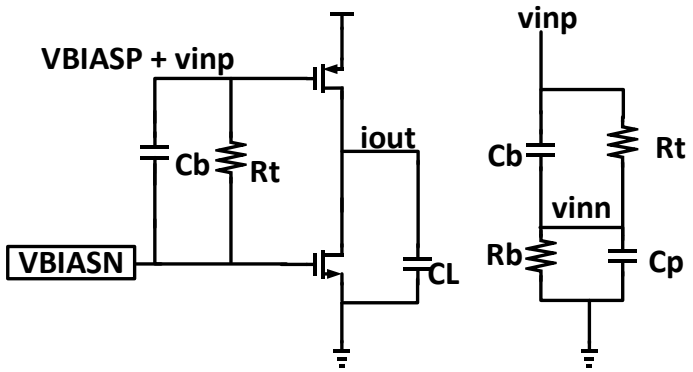

Figure 14: Level-shifter circuit with resistor and small signal equivalent circuit

Now the transfer function between vinp and vinn would be

$$\frac{viin}{vinp} = \frac{(Cb * Rb * Rt) * s + Rb}{(Cb * Rb * Rt + Cp * Rb * Rt) * s + Rb + Rt} \quad 3.15$$

The zero at origin has been moved to a higher frequency and depending on the values of [Cb >> Cp and Rb >> Rt] we can get a match between vinp and vinn even at lower frequencies as shown in Figure 15. It should be noted here that, at higher frequencies the transfer function reaches a value depending on the ratio of capacitors Cb and Cp and the

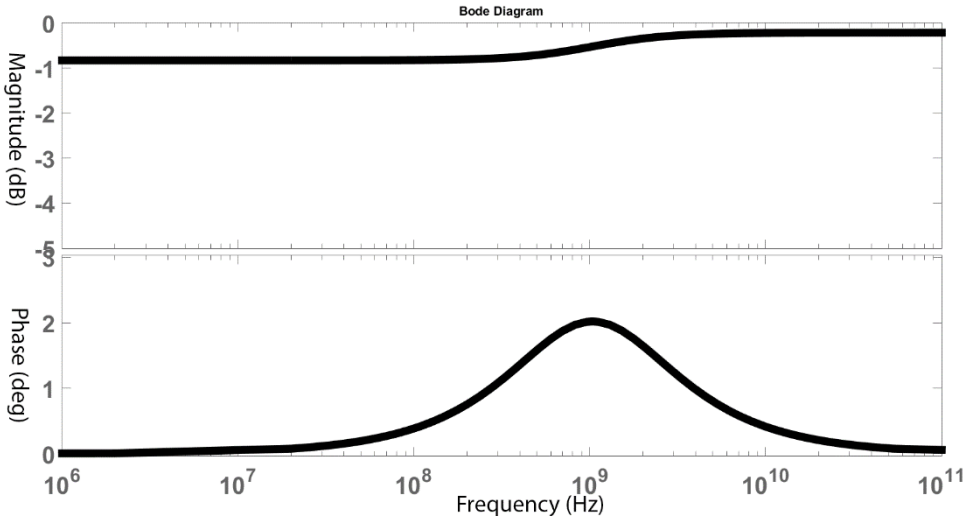

Figure 15: Transfer function of capacitor + resistor level shifter

slight variation from 1 can be adjusted in the Kp and Kn of PMOS and NMOS to get a good linearity. More importantly, since passive components are used to transmit the small signal to the gates of the output transistors the linearity improves significantly.

The resistor Rt is further useful to bias the output transistors as shown in Figure 16. The common mode feedback tracks the output common-mode and varies the current

through the MOSFET MB, which in turn varies the current flowing through Rt and that causes the required drop/increase in the biasing voltage of the NMOS.

3.2.3 Frequency compensation schemes

The most commonly used compensation scheme for amplifiers is Miller's compensation, which results in stability at the expense of bandwidth by lowering the dominant pole. Using Miller's compensation would require large power in both the stages

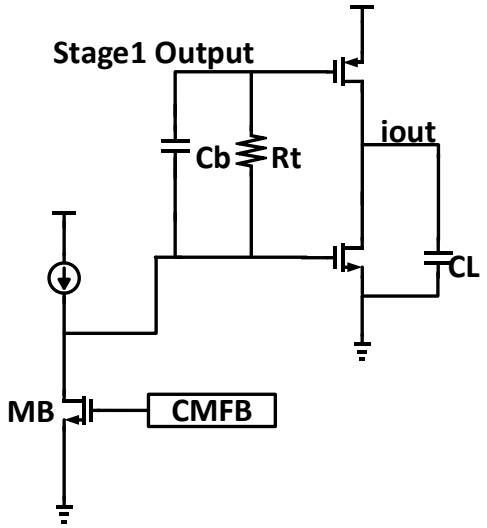

Figure 16: DC Level shifter for class-AB

of the amplifier, which we are trying to avoid. Hence for this design feed-forward compensation [30] was selected. The technique is explained briefly using Figure 17.

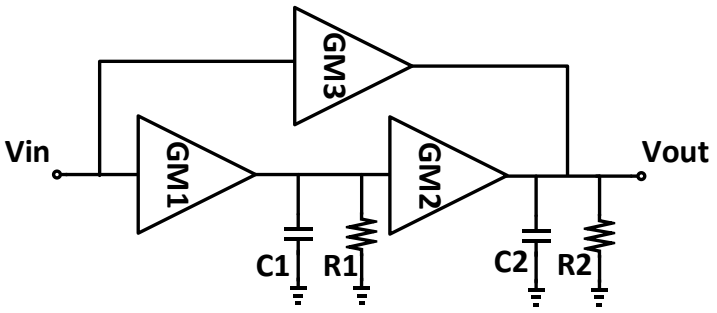

Figure 17: Feed-forward Gm compensation technique

The two gain stages with trans-conductance GM1 and GM2 are the two gain stages of the amplifier and GM3 is the feed forward stage which provides a fast path and adds a zero to the transfer function, which can be used to compensate for a pole. If A1 = GM1*R1, A2 = GM2*R2, A3 = GM3*R2, wp1 = 1/(R1*C1) and wp2 = 1/(R2*C2), the transfer function can be written as

$$\frac{A1 * A2}{\left(1 + \frac{s}{wp1}\right) * \left(1 + \frac{s}{wp2}\right)} + \frac{A3}{1 + \frac{s}{wp2}} \tag{3.16}$$

Which can be resolved to

$$(A1 * A2 + A3) * \frac{\left(1 + \frac{s}{wp1 * \frac{A1A2 + A3}{A3}}\right)}{\left(1 + \frac{s}{wp1}\right) * \left(1 + \frac{s}{wp2}\right)} \tag{3.17}$$

The frequency of zero thus generated is $wp1 * \frac{A1A2+A3}{A3}$, and it should be noted that the zero will always be greater than wp1. This condition on the zero generated results in

- To cancel/reduce the effect of one of the poles, the output pole has to be farther away from origin than the first stage pole. Which means wp1 < wz <= wp2.

But in our case since the sampling capacitors are huge and the gain requirement is high, we will most likely have the second pole as the dominating pole. Hence, the feed-forward technique mentioned above cannot be directly used.

3.2.4 Modified feed-forward compensation

In order to compensate the effect of a pole, let us first try to understand what happens around and after the pole frequency. Consider the simple circuit in Figure 18

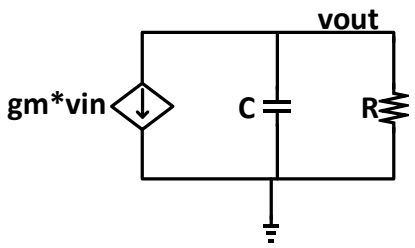

Figure 18: Small signal model of a simple amplifier

At DC all the small signal current flows through the resistor and the gain is –gm*R. As the pole approaches, the impedance of the capacitor starts decreasing and only a part of the current flows through the resistor [Net impedance decreases]. Hence, the gain of the

amplifier decreases. If there exists a path which supplies current in parallel to gm*vin at high frequencies (around and after the pole frequency), then it can reduce or even cancel the effect of the pole.

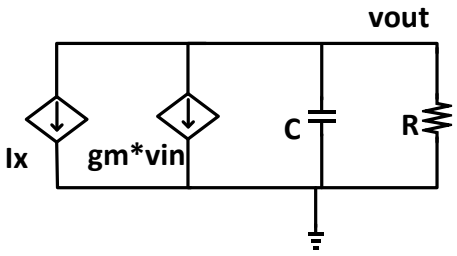

Figure 19: Small signal model of a simple amplifier for pole cancellation

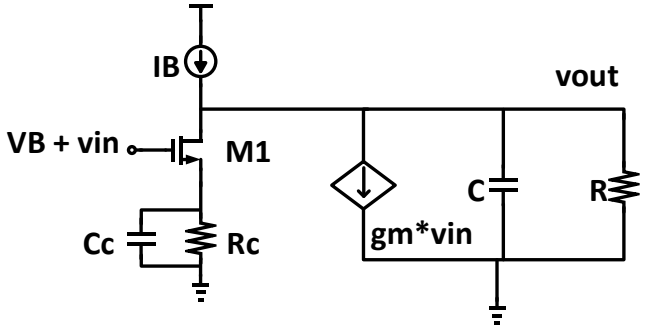

Figure 20: Ix implementation, the small signal model of amplifier is still considered

For the pole to be cancelled, vout = -gm*R*vin at all frequencies and will only happen when

$$Ix = gm * R * vin * s * C \quad (3.18)$$

This can be achieved using the circuit in Figure 20, but the circuit results in a high frequency pole given by gm1/(Cc).

If Rc is very large then

$$Ix = vin * s * Cc \quad (3.19)$$

and this can be used to reduce/cancel the effect of the pole.

3.2.5 Proposed amplifier architecture

Combining the DC level shifter circuit described in section 3.2.2 and the feed-forward compensation in section 3.2.3, the architecture in Figure 21 was used to design the amplifier with high linearity and a high bandwidth.

The small signal model of the first stage differential half circuit including the feed forward compensation and assuming that Cb forms a short between node X and node Y [Cb is large] is given in Figure 22

The poles and zeros of this system are

$$Frequency\ of\ Zero = \frac{R1 * Ra * gm1 + R1 * Rds3 * gm1 + R1 * Rds3 * gm3 + R1 * Ra * Rds3 * gm1 * gm3}{Ca * R1 * Ra * Rds3 * gm1 + Ca * R1 * Ra * Rds3 * gm3} \cong \frac{gm1 * gm3}{Ca * (gm1 + gm3)} \quad (3.20)$$

$$Frequency\ of\ First\ Pole = \frac{R1 + Ra + Rds3 + Ra * Rds3 * gm3}{C1 * R1 * Ra + C1 * R1 * Rds3 + Ca * R1 * Ra + Ca * Ra * Rds3 + C1 * R1 * Ra * Rds3 * gm3}$$

$$\cong \frac{1}{C1 * R1} \qquad 3.21$$

$$Frequency\ of\ Second\ Pole = \frac{gm3}{Ca}. \qquad 3.22$$

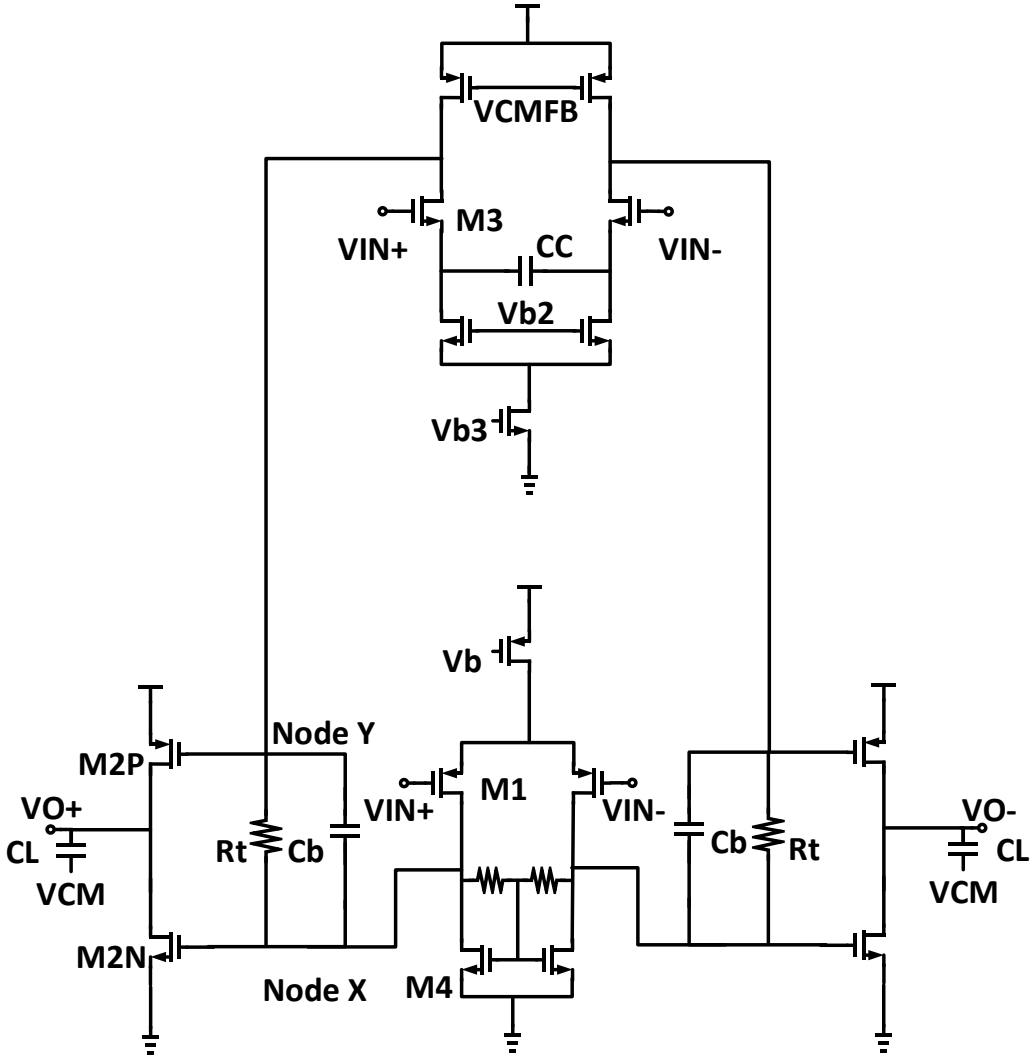

Figure 21: Two stage amplifier with DC level shifter and feed forward compensation

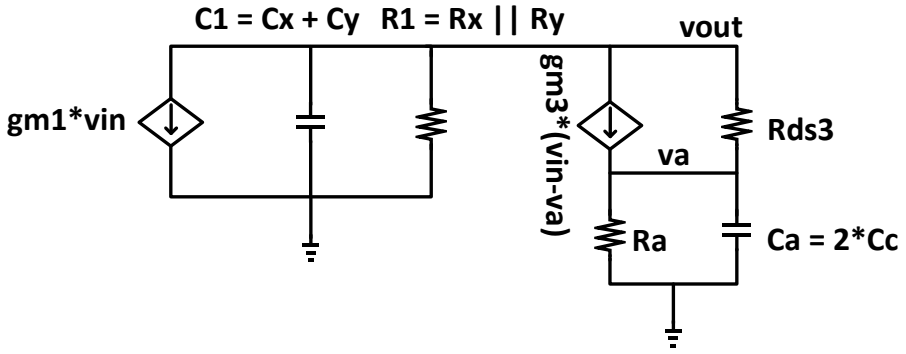

Figure 22: Small signal model of stage 1

Hence in-order to cancel the first stage pole and assuming gm3 > gm1 we get

$$\frac{gm1}{Ca} = \frac{1}{R1 * C1} \tag{3.23}$$

$$\frac{Ca}{C1} = gm1 * R1. \tag{3.24}$$

But, since the first stage pole is the non-dominant pole and we do not have to cancel it exactly to get the required phase margin, the ratio of Ca to C1 can be less than the gain of the first stage. With the feed-forward compensation the two stage amplifier parameters can be defined as

$$DCgain = \ gm1 * R1 * (gmp2 + gmn2) * Rout \tag{3.25}$$

$$Frequency\ of\ Dominant\ pole\ P1 = \frac{1}{Rout * Cl} \tag{3.26}$$

$$Frequency\ of\ Pole\ P2 = \frac{1}{R1 * C1} \quad 3.27$$

$$Frequency\ of\ Zero = gm1/Ca \quad 3.28$$

$$Frequency\ of\ Pole\ P3 = gm3/Ca \quad 3.29$$

In addition there will be a pole zero pair due to Cb and Rt.

Common-mode half circuit analysis for common mode feedback loop:

In this section we will look at the effect of the addition of Cb and Rt on the common mode feedback loop. Assuming the inputs are grounded, the small signal model is shown in Figure 23

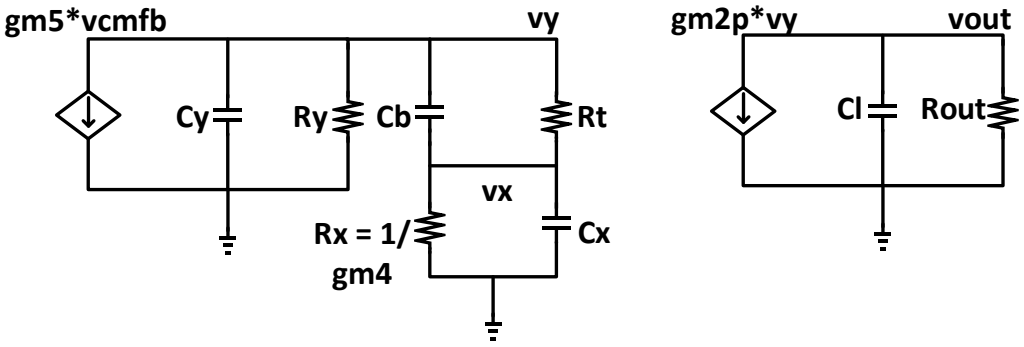

Figure 23: Small signal model of part of common mode feedback loop

Since the value of Rx << Rt and Cx << Cb, the voltage vx will be very small compared to vy and hence, the effect of it on the output common mode level through M2N is neglected. The poles and zeros of this system are

$$Frequency\ of\ Zero = \frac{Rt\ +\ Rx}{Cb * Rt * Rx\ +\ Cx * Rt * Rx} \cong \frac{1}{Cb * Rx} \tag{3.30}$$

$$Frequency\ of\ Output\ pole = \frac{1}{Cl * Rout} \tag{3.31}$$

$$Frequency\ of\ First\ stage\ pole1 = \frac{1}{Cb * \frac{Rt * (Rx + Ry)}{Rt + Rx + Ry}} \cong \frac{1}{Cb * Rt} \tag{3.32}$$

$$Frequency\ of\ First\ stage\ pole2 = \frac{1}{Rx * (Cx + Cy)} \tag{3.33}$$

Since, the output pole and First stage pole 1 are low frequency poles they have to be compensated to get a proper phase margin. First stage pole 2 will generally be a high frequency pole since Rx is small. To compensate for the two dominant poles, the CMFB amplifier (Figure 24) was designed to have source degeneration to add a zero to the path to cancel one of the dominant poles. The additional pole generated due to degeneration was cancelled using the zero generated due to Cb and Rt.

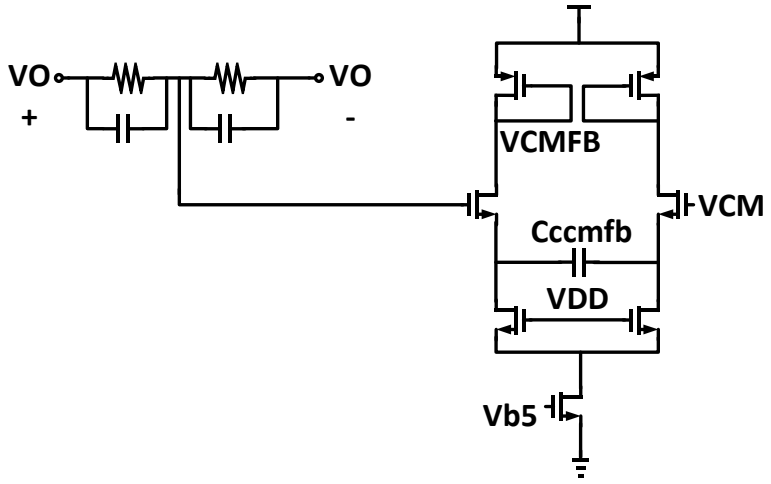

Figure 24: CMFB amplifier

The poles and zeros of the amplifier were placed as given below

$$Frequency\ of\ First\ stage\ pole\ 1 \cong \frac{1}{Rccmfb * 2 * Cccmfb} \tag{3.34}$$

$$Frequency\ of\ Zero \cong \frac{gmx}{2 * Cccmfb} \tag{3.35}$$

The second pole of the CMFB is a high frequency pole because of the diode connected load. The complete circuit is shown in Figure 25

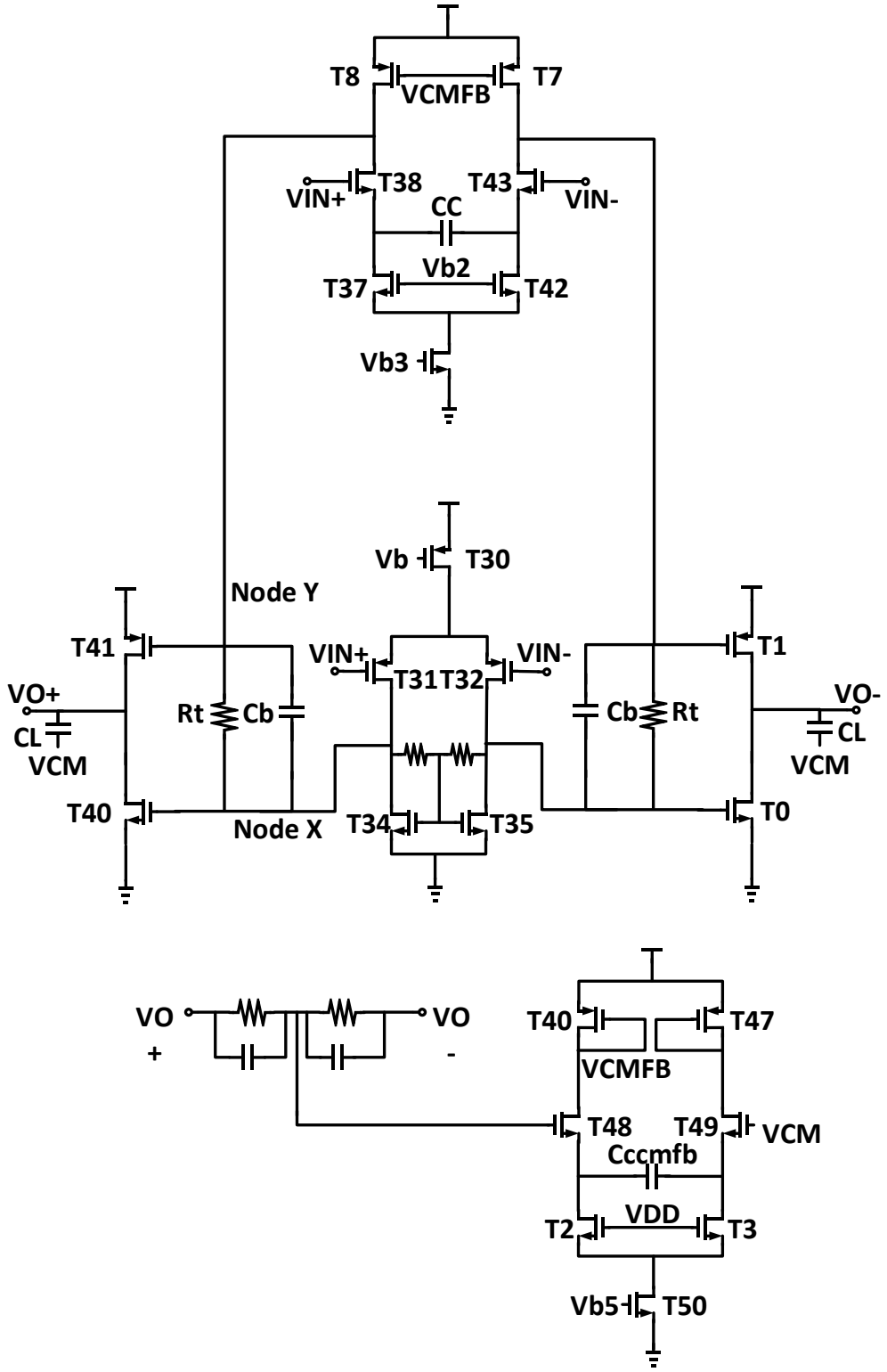

Figure 25: Two stage amplifier with class-AB output stage

3.2.6 Amplifier design procedure

The following steps provide an overview of the design procedure of the amplifier

1) Based on the load capacitance 'CL' and the slew time requirement determine the slew current. Since we are using a class-AB stage the quiescent current can be $1/4^{th}$ - $1/3^{rd}$ of the slew current.
2) Based on the settling time requirement and the feedback factor, calculate the UGB required for the amplifier. In ideal case, when the non-dominate pole is perfectly cancelled by the feed-forward zero, the UGB of the amplifier will be

$$UGB = \frac{gm31 * R1 * (gm41 + gm40)}{2 * pi * CL} \quad 3.36$$

   But since we may not have to exactly cancel the first stage pole, use a higher UGB value than required.
3) Based on the DC gain value, assuming a required gain for stage 1, and using the quiescent current and UGB calculate the required gm41/Iq and gm40/Iq and based on the gm/Id plots get the required (W/L), set the PMOS (W/L) slightly smaller to compensate for the mismatch in 'vx' and 'vy'
4) For the first stage, the value of input transistor 'gm' has to be determined from noise specification, using approximate value of the gain and the parasitic capacitance of stage 2 estimate the location of first stage pole.
5) Using Matlab determine the position of the zero required to get a proper phase margin. Based on the position of zero and input transistor gm, determine the value of CC in the feed forward transistor

6) The location of the second pole "gm38/(2*CC)" generated by the feed forward path has to beyond the UGB, based on the condition determine gm38 and using a high overdrive and gm/Id determine the current in the feed forward branch to achieve 'gm38'.
7) To determine the value of Rt calculate the maximum drop 'VD' required in the DC bias voltages across PVT and based on the below equation determine the value of Rt.

$$VD = Rt * \left(\frac{10\%\ of\ First\ stage\ Itail}{2}\right) \quad 3.37$$

8) Cb should be such that 1/(Rt*Cb) has to be smaller than the input signal frequency.
9) For the CMFB amplifier, based on Cb and Rt values and a nominal value of gm/Id determine the value of Cccmfb and adjust it depending on the requirement.

Based on the above method the dimensions of the transistors, capacitors and current values are provided in Table 2

Table 2: Amplifier dimensions

Transistor	**W/L**	**Overdrive (V)**	**Current (A)**
T30	1.0944m/240n	80m	700u
T31, T32	91.2u/240n	200m	350u
T34, T35	11.04u/240n	200m	350u
T1, T41	49.2u/240n	200m	460u
T0, T40	13.44u/240n	200m	460u
T8, T7	165.12u/240n	200m	900u
T38, T43	192u/130n	60m	900u
T37, T42	312u/240n	80m	900u
T4	624u/240n	80m	1.8m
T40, T47	38.88u/240n	200m	201u
T48, T49	52.8u/240n	80m	210u

Table 2: Continued

Transistor	W/L	Overdrive (V)	Current (A)
T2, T3	5.76u/240n	80m	210u
T50	105.6u/240n	80m	420u

Amp	Tail Current
First Stage	700u
Second Stage, each branch	460u
Feed-forward	1.8m
CMFB	420u

Cb	2pF
Cc	1pF
Ccmfb	1pF

4. SWITCH DESIGN

Consider the 1.5 bit MDAC shown in Figure 26, the switches S1, S1’ connect the input to the capacitors CH and CS during sampling and switches S3, S3’ connect to the output during hold. Hence, the output of the MDAC heavily depends on how the switches transmit a signal from one node to the other, which in-turn means the switch linearity.

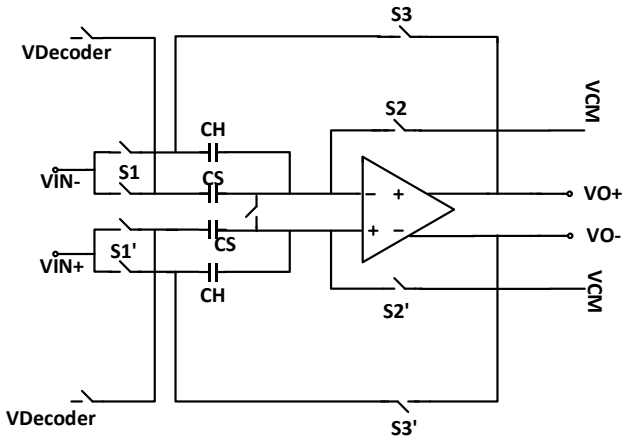

Figure 26: Structure of a 1.5 bit MDAC

The linearity requirement of the switch for the first MDAC in a pipeline ADC is determined by the overall resolution of the ADC. For a 12-bit ADC it is desirable that the linearity of the sampling switches is at least 13 bits, this would make noise of the circuits the dominant contributor for ENOB analysis.

A simple transistor can act as a switch with its gate voltage controlling the turning on and off of the switch. The resistance of a single MOSFET, assuming it's operating in linear region is given by

$$Ron = \frac{1}{\mu nCox\left(\frac{W}{L}\right)(V_{GS} - V_{TH})} \quad 4.1$$

As can be seen from the equation the on resistance is inversely proportional to the V_{GS} and if source is connected to the input and a capacitor to the output, as shown in Figure 27, the on-resistance change with the level of the input and the linearity is drastically affected. In order to keep the resistance constant for all inputs, the V_{GS} of the switch is

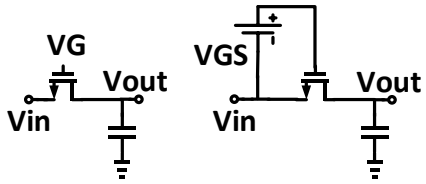

Figure 27: a. MOSFET switch b. MOSFET switch with boot-strapping

forced to be constant this is generally done by connecting a constant voltage source across the gate and source of the MOSFET as shown in the figure, this technique is called boot-strapping and one such implementation is provided in Figure 28 [31]. Using boot-strapping technique linearity of up to 15 bits has been reported. During ϕ_2 phase the

capacitor C_{offset} is charged to VDD which will be the V_{GS} voltage of the switch MNSW. During ϕ_1 as transistor MN1 closes, the voltage at B becomes VDD (some charge shared) + V_{in} and hence, the gate source voltage of MNSW remains constant at VDD. The dimensions of the transistors we calculated based on the below table 3

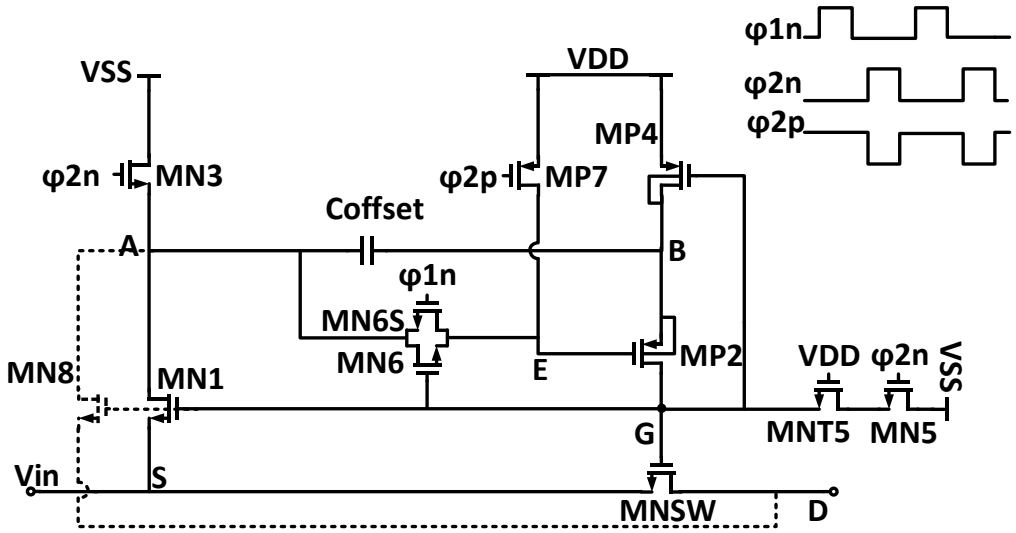

Figure 28: Boot-strapping switch [31]

Where Cs = Sampling Capacitance (2.3pF), Coffset = 2pF, Cp = (Coffset in series with C_G), C_G = Net parasitic capacitance at Node G, C_{g2} is the total parasitic capacitance at the gate of MP2 and Ts is the sampling time

Table 3: Switch design parameters

Transistor	**Load Capacitance**	**Time**	**Initial voltage VG, VS, VD**	**Final voltages VG, VS, VD**	**Slewing**	**Dimension is based on**
MNSW	Cs	Ts/5	0,0.6,0.6	(2.1,0.9,0.9)/ (1.5,0.3,0.3)	No	Linear Ron
Comments: Time = (Ts/2.5)/2, there will be another switch in series with the capacitor						
MN1/MN8	C_p	0.1* Ts/5	0,0.6,0	(2.1,0.9,0.9)/ (1.5,0.3,0.3)	No	Linear Ron
The settling accuracy can be 1%						
MP2	C_p	0.1* Ts/5	1.2,1.2,0	(0.9,2.1,2.1)/ (0.3,1.5,1.5)	Yes	Slewing Current
The drain has to slew from 0 to 0.9 + |Vthp|						
MN3	C_{Offset}	Ts/2.5	(0,0,0.3)/(0, 0,0.9)	1.2,0,0	No	Linear Ron
The settling accuracy can be 1%						
MP4	C_{Offset}	Ts/2.5	(1.5,1.2,1.5) /(2.1,1.2,2.1	0,1.2,1.2	No	Linear Ron
The settling accuracy can be 1%						
MN5/MNT5	C_G	0.1* Ts/5	(0,0,2.1)/ (0,0,1.5)	1.2,0,0	Yes	Slewing Current
The drain has to slew from 2.1 to 1.2 - Vthn						
MN6/MNS6	C_{g2}	0.1* Ts/5	(0,0,1.2)	(1.2/2.1,0.9,0 .9)/(1.2/1.5,0. 3,0.3)	Yes	Slewing Current
The drain has to slew from 1.2 to 1.2 - Vthn						
MP7	C_{g2}	Ts/2.5	(1.2,1.2,0.3) /(1.2,1.2,0.9	0,1.2,1.2	No	Linear Ron

Using the above table the dimensions of the transistors were calculated as (Table 4)

Table 4: Switch dimensions

Transistor	**W/L**
MNSW	10.24u/130n
MN1/MN8	3.2/240n
MP2	6.72u/240n

Table 4: Continued

Transistor	W/L
MN3	15.36u/240n
MP4	7.2u/240n
MN5/MNT5	4.8u/240n
MN6/MN6S	2.4u/240n
MP7	4.8u/240n

5. SIMULATION AND RESULTS

This section presents the simulation details and schematic level simulation results of the amplifier and the switch. The amplifier was characterized for its open loop and closed loop properties and the switch was characterized for its settling time and linearity.

5.1 Amplifier simulation and results

The below table summarizes the results achieved by the amplifier explained in Figure 28.

Table 5: Amplifier results

	This work [TT]
Technology	IBM 0.13um
VDD	1.2
ADC Resolution	12 bit
Sampling Frequency	100MHz
Vpp	1.2
Load	3.5pF
Amplifier type	Two stage
DC_gain	47dB
GBW	1040MHz
Current	3.88mA
Settling time	[11-bit] 3.881ns
IM3	75dB -6dBFS @(4.30MHz and 5.08MHz) 68.46dB -3.5dBFS@(4.30MHz and 5.08MHz)
Noise	62uV up to 50MHz
FOM1[MHz*pF/mA]	938
FOM2[(V/us)*(pF)/mA]	881
FOM3[(V/us)/mA] [Slewrate/Current]	251
FOM3[ns/mA]	1.01

Figure 29 shows the test-bench used to perform open loop simulations, the capacitor on the output node is the net capacitance (3.5pF) that node would see in a closed loop scenario.

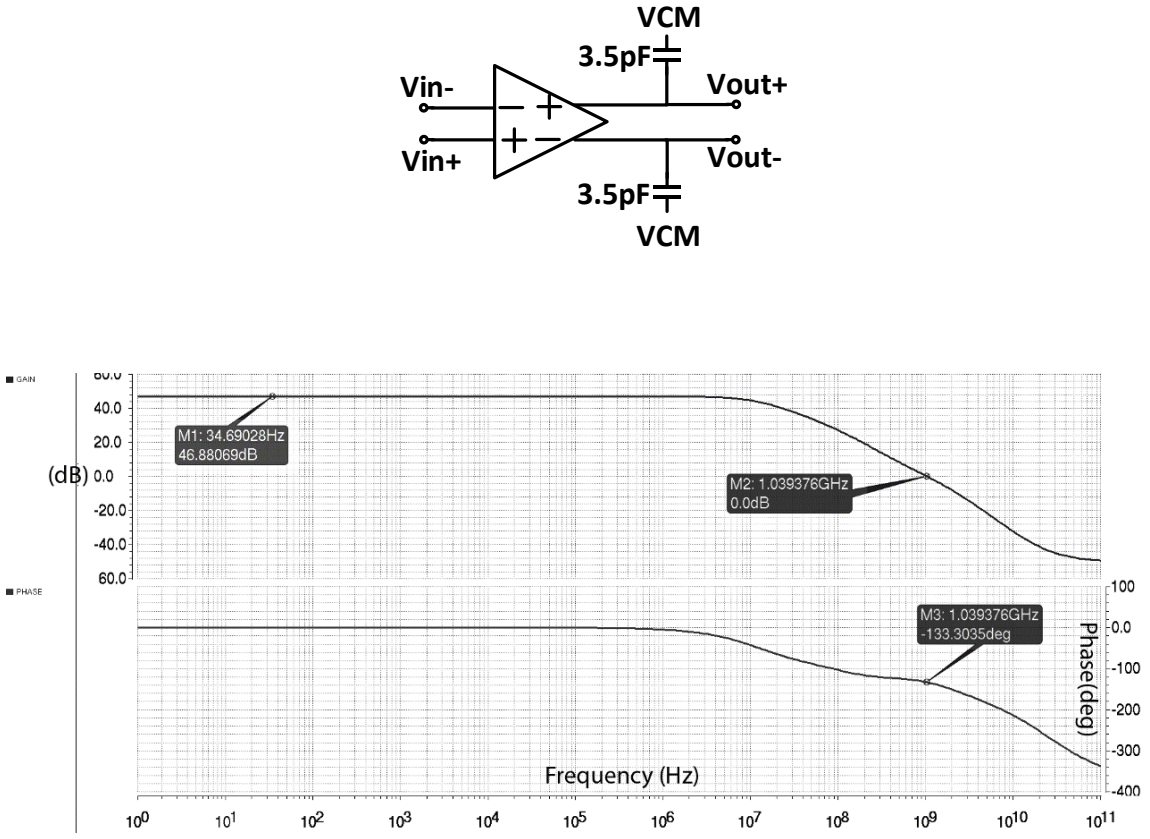

Figure 29: a. Open loop test-bench b. AC gain and phase

The AC analysis results in UGB of 1040MHz, DC gain of 47dB and a phase margin of 46.7 degrees as can be seen in Figure 29. The locations of poles and zeros are given in the Table 6.

Table 6: Poles and zeros of the amplifier

	Pole/Zero	Value	Description
1	Pole 1	12.1MHz	Output pole
2	Pole – Zero Pair	18.3MHz – 19.16 MHz	Due to Cb, Rt
3	Pole 2	165 MHz	First Stage Pole
4	Zero 1	378 MHz	From feed-forward path
5	Pole 3	1.94 GHz	From feed-forward path

As can be seen from Figure 29 and Table 6, the feed forward zero compensates for the first stage pole but since the cancellation is not exact, the output pole which determines the UGB had to be pushed forward. Also the addition of Cb, Rt and the feed-forward circuit introduces a pole zero pair.

Similarly for the common mode feedback loop, the gain is around 38dB, bandwidth 402MHz with a phase margin of 47.4 degrees. The location of poles and zeros is given in Table 7.

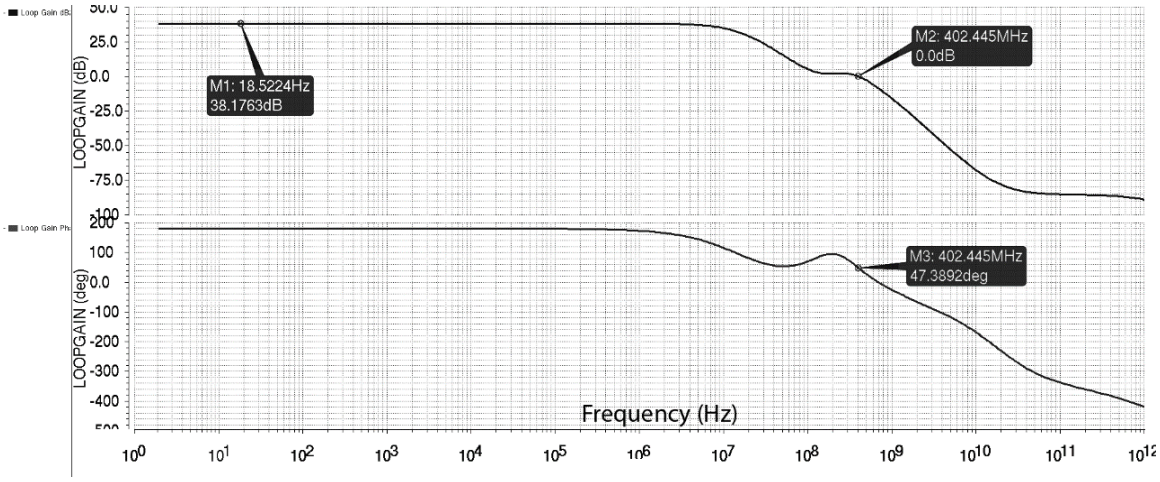

Figure 30: CMFB loop gain

Table 7: Poles and zeros of the CMFB loop

	Pole/Zero	Value	Description
1	Pole 1	11.6MHz	Output pole
2	Pole 2	23 MHz	Due to Cb, Rt
3	Zero 1	126 MHz	Zero from Cb and Rx
4	Zero 2	130 MHz	CMFB Amp zero
5	Pole 3	384 MHz	CMFB Amp pole 1
6	Pole 4	531 MHz	CMFB Amp Pole 2

The biasing circuit used in the first stage load introduces a pole zero pair, this can be eliminated by connecting a capacitor (~= Cgs T34) parallel to the resistors but this will decrease the location of the first pole. From the table it can be seen that Pole 2 and Pole 3 are compensated by Zero 1 and Zero 2 and the non-dominant pole is after the UGB.

Figure 31 shows the test-bench used to perform close loop simulations to estimate the settling behavior and linearity of the amplifier. Since the amplifier will be used in a discrete circuit, the test bench uses switches with resistance of 80 Ohms and non-overlapping clocks for sample and hold phases with a rise and fall time of about 125ps. During the sampling phase, the input is sampled on to the input capacitors and the amplifier is connected in unit gain feedback, the load and the feedback capacitors are connected to common mode. During the hold phase, the feedback capacitor is connected across the amplifier and the load is connected at the output and one end of the input capacitor is connected to common mode, this is similar to the operation of the MDAC.

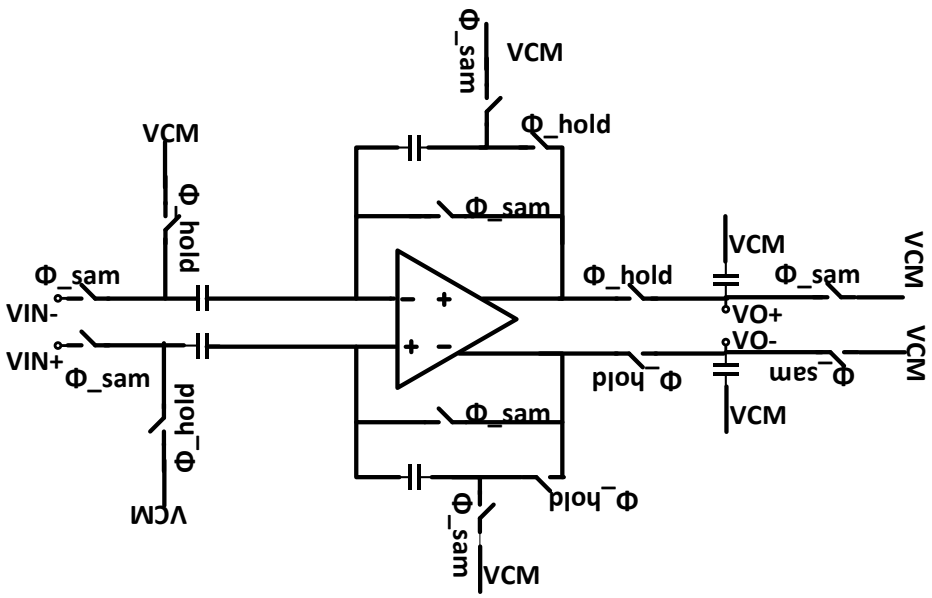

Figure 31: Closed loop test bench

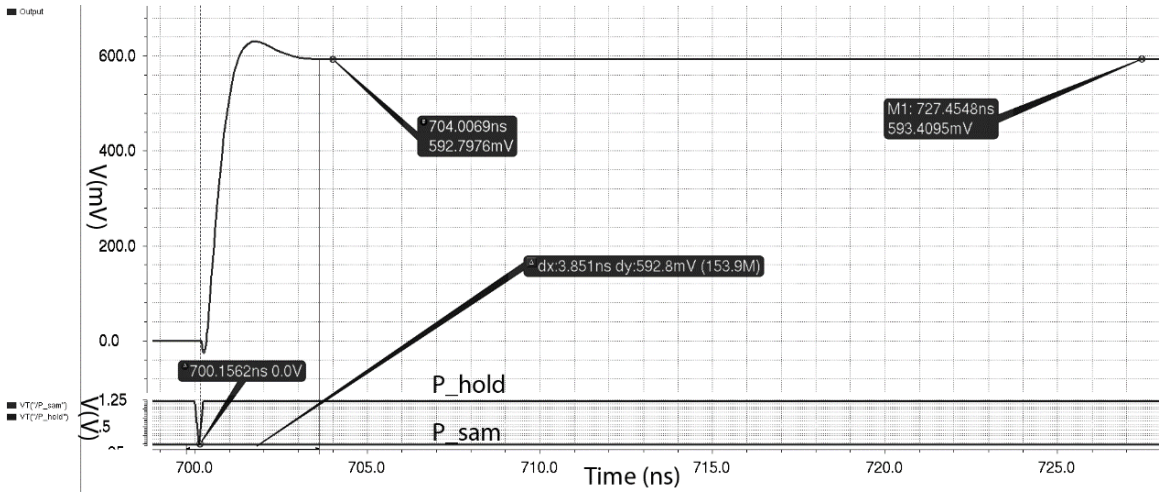

Figure 32: Settling time

The settling time was measured to the accuracy of 11bits, which is $\frac{1.187}{2^{11}} = 580uV$ and that is 0.097% settling error. The 11 bit settling time is 3.815ns which should be sufficient for non-overlapping clocks at 100MHz.

To measure the linearity of the amplifier, single tone tests at full scale amplitude, frequency of 39.45MHz and 93.36MHz and a sampling frequency of 100MHz and two tone tests at -6dBFS and -3.5dBFS (each) and frequencies 4.3MHz and 5.08MHz were performed. For each of the tests, 256 samples were considered for DFT and each sample was taken after 4.5ns in the hold phase. As can be seen in the Figures 33, 34 the HD3 of the single tone is about 72.66dB and since the IM3 non-linearity is not clearly visible at an amplitude of -6dBFS, the amplitude was increased to -3.5dBFS (each tone) and it can be seen in Figure 36, that the IM3 is 68.73dB.

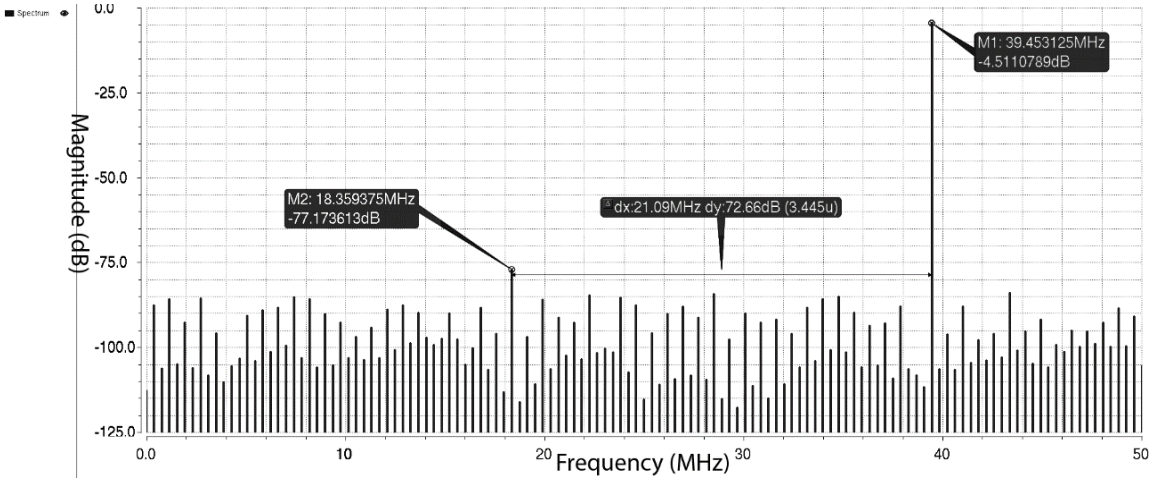

Figure 33: HD3 at 39.45MHz

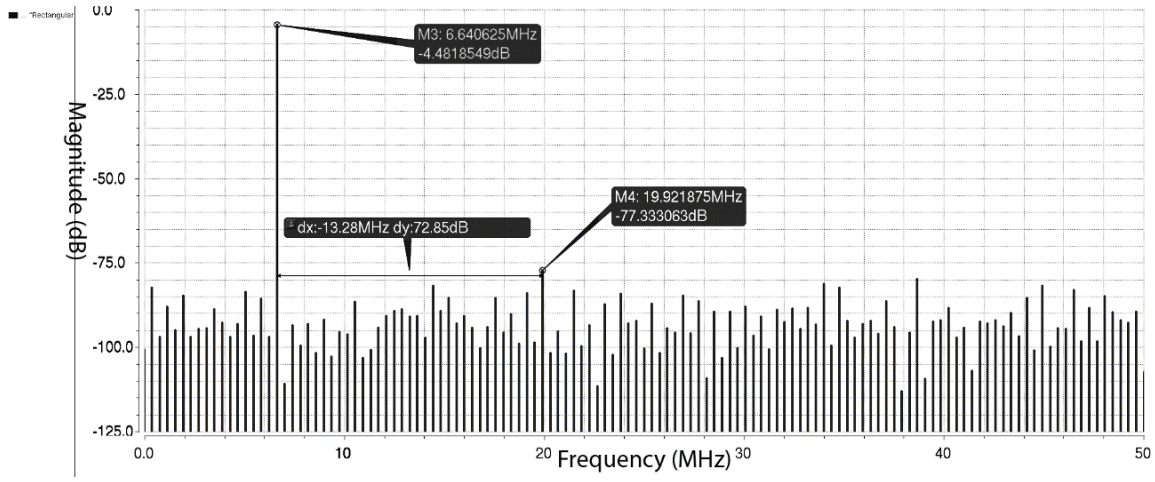

Figure 34: HD3 at 93.36MHz

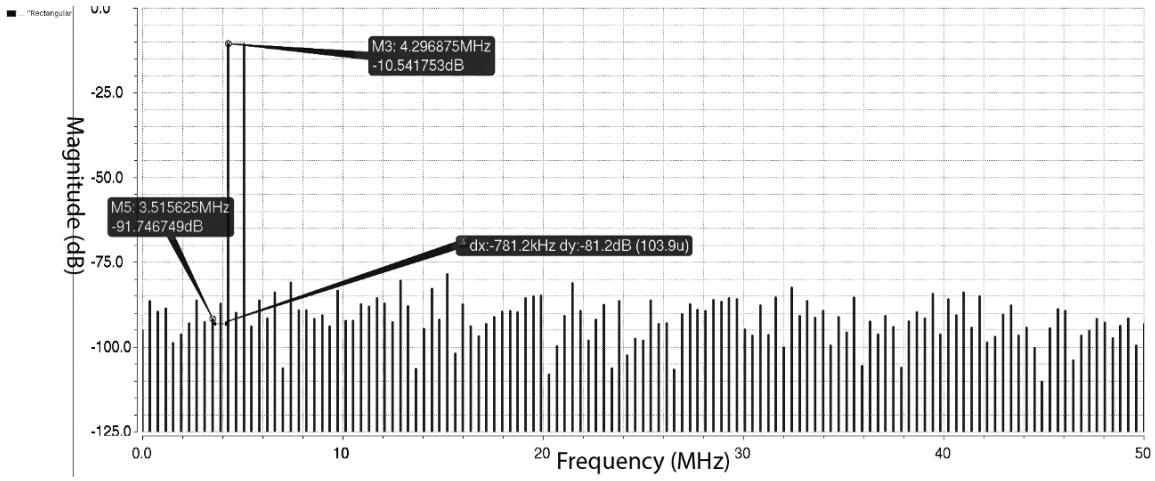

Figure 35: IM3 at -6dBFS (each tone)

The amplitudes of the tone were varied and the IM3 was plotted vs amplitude and can be seen in Figure 37. Differential full scale is 1.2 V and the peak amplitude of each

tone is 4*x. [The amplitude is higher than full scale so that the effect of IM3 can be properly seen]

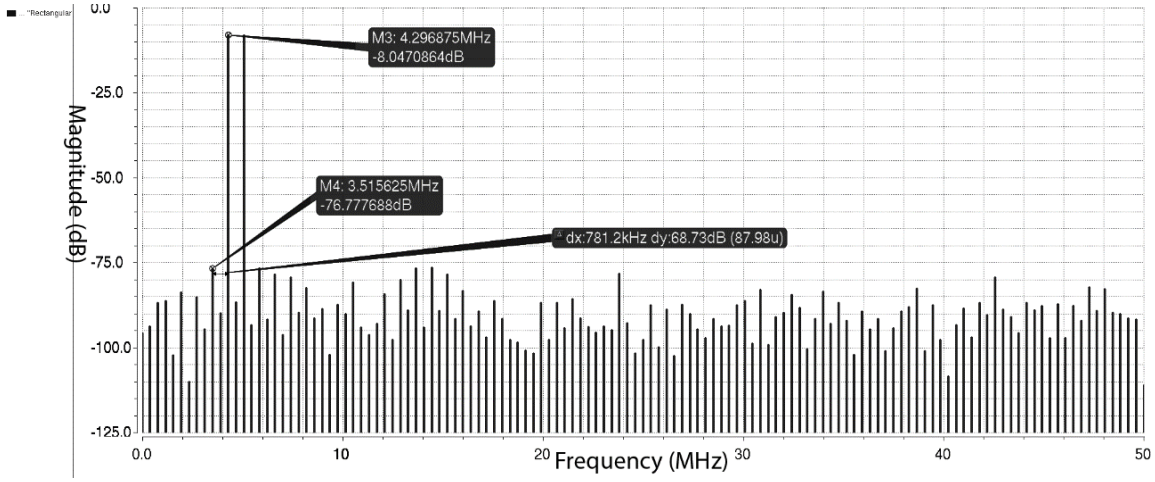

Figure 36: IM3 at -3.5dBFS (each tone)

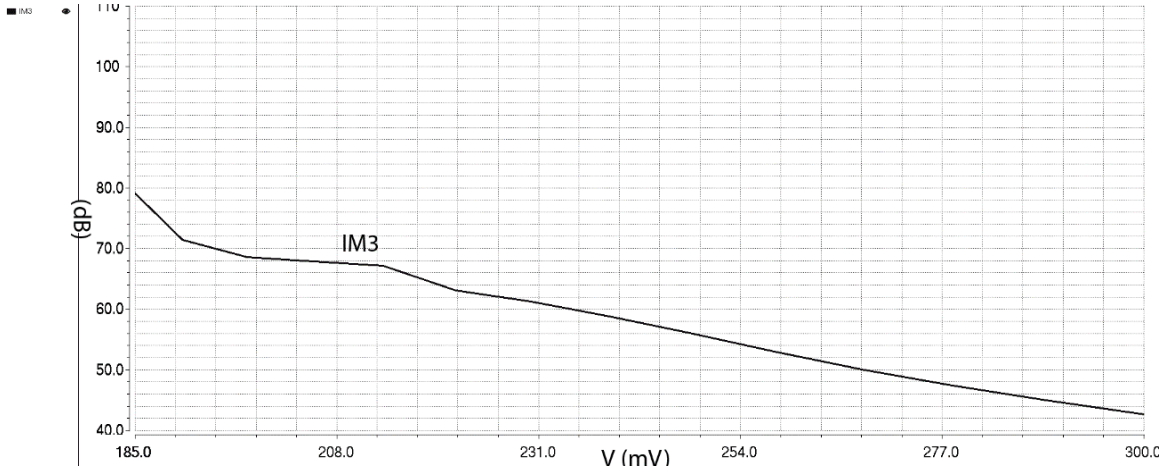

Figure 37: IM3 vs amplitude

The linearity of the amplifier was also characterized using continuous time test bench shown in Figure 38, the resistors at the input were large and provided DC biasing.

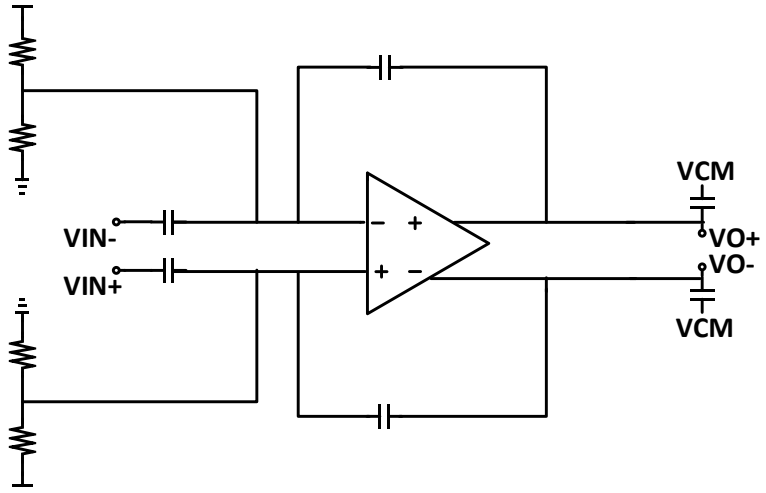

Figure 38: Continuous time test bench

From the plots the IIP3 value is 38.3dBm and the -1-dB compression is also at 11.36631dBm which is greater than the required value of 0dBm (1.2V peak-peak). As discussed in chapter 2, the linearity of the amplifier significantly depends on the linearity of the output stage. The linearity of the class-AB output stage depends on the overdrive of the transistors and the AC signal supplied to them. Since we are using feed-forward compensation and not Miller's compensation, the current and the trans-conductance

requirement in the output stage is low and this enables us to have a large overdrive for the output transistors. Also the DC-level shifter explained in section 3.2.2 provides a proper AC signal at the gates of NMOS and PMOS of the output stage using passive components which are more linear than the active level shifter used in the Monticelli scheme. For the current design the value of the signal can be seen in Figure 41.

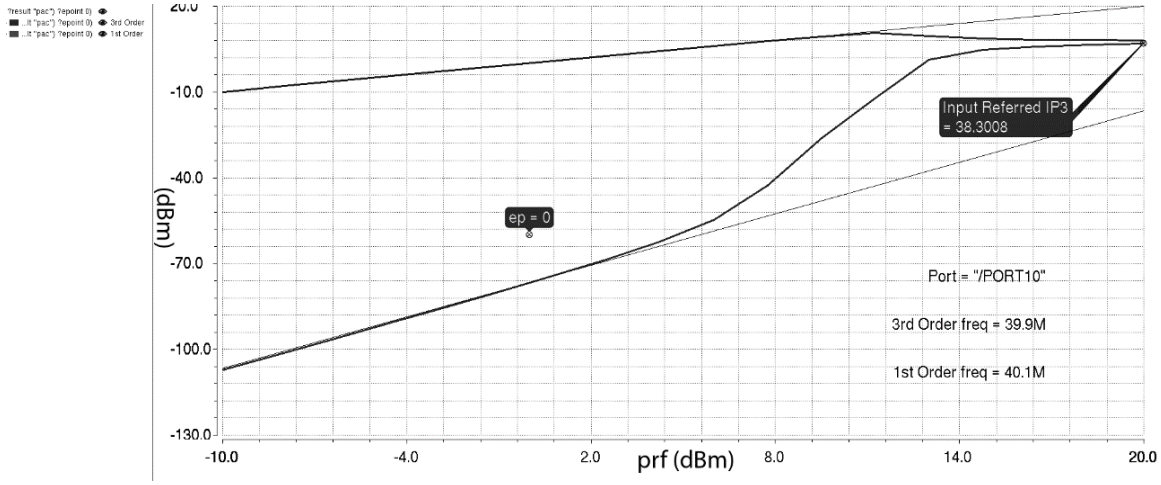

Figure 39: Closed-loop IIP3

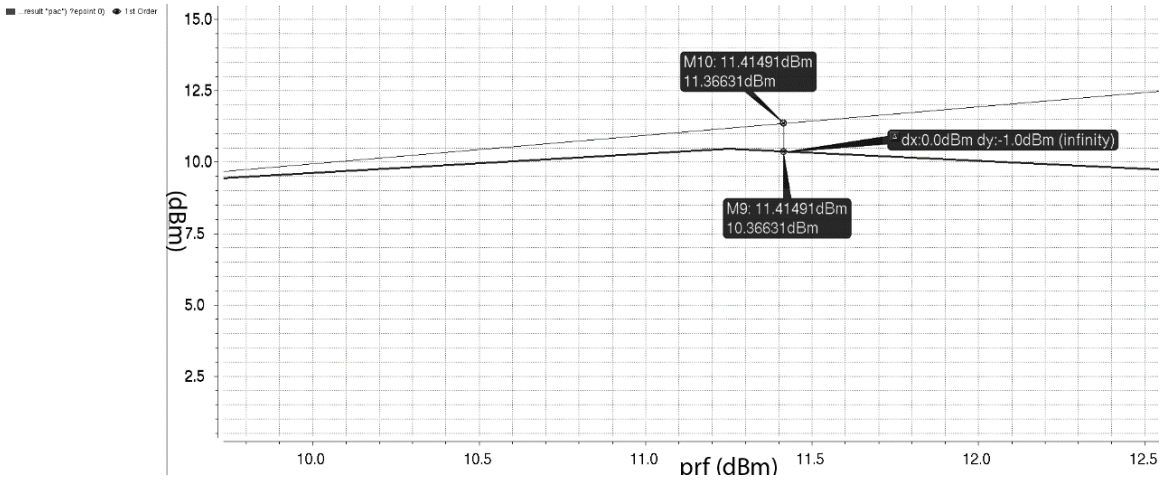

Figure 40: 1-dB compression

From Figure 41 it can be seen that the AC signal at the gates of output stage does not exactly match at low frequencies but at high frequencies it matches perfectly. Ideally the frequency where it starts to match should be less than the input signal frequency. Even though the value of the resistor "Rt" was selected based on this condition, the plots are not as expected. This can be explained based on Figure 42.

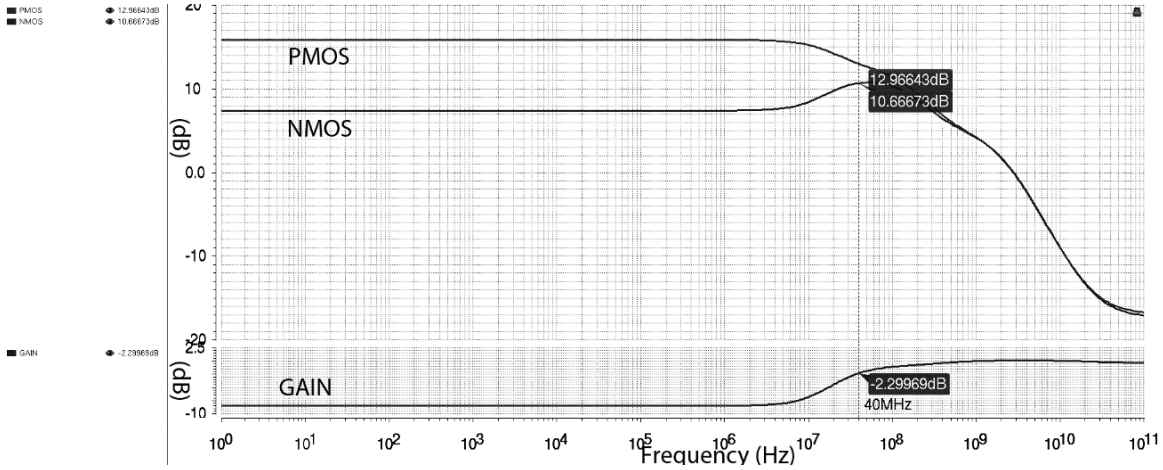

Figure 41: AC signals at the gates of the output stage

As calculated in section 3.2.2 the transfer function from vinp to vinn is given by

$$\frac{viin}{vinp} = \frac{(Cb * Rb * Rt) * s + Rb}{(Cb * Rb * Rt + Cp * Rb * Rt) * s + Rb + Rt} \quad 5.1$$

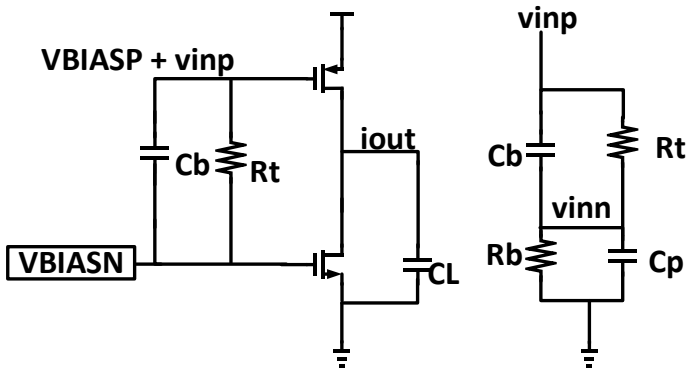

Figure 42: DC level shifter

-

Based on the transfer function, the pole is given by $-\frac{1}{(Cb+Cp)*(Rb||Rt)}$ and the zero by $-\frac{1}{Cb*Rt}$. If the value of Rb is not much greater than Rt, the location of the pole is pushed farther away from the zero, which is what is the case in this design. Since the current in the feedforward amplifier is very high, the net resistance at its output is small, which resulted in a pole farther away than expected. This can be eliminated by using cascaded load in the feed-forward stage as shown in Figure 43. Since the linearity requirement of the MDAC was satisfied, this circuit was not modified.

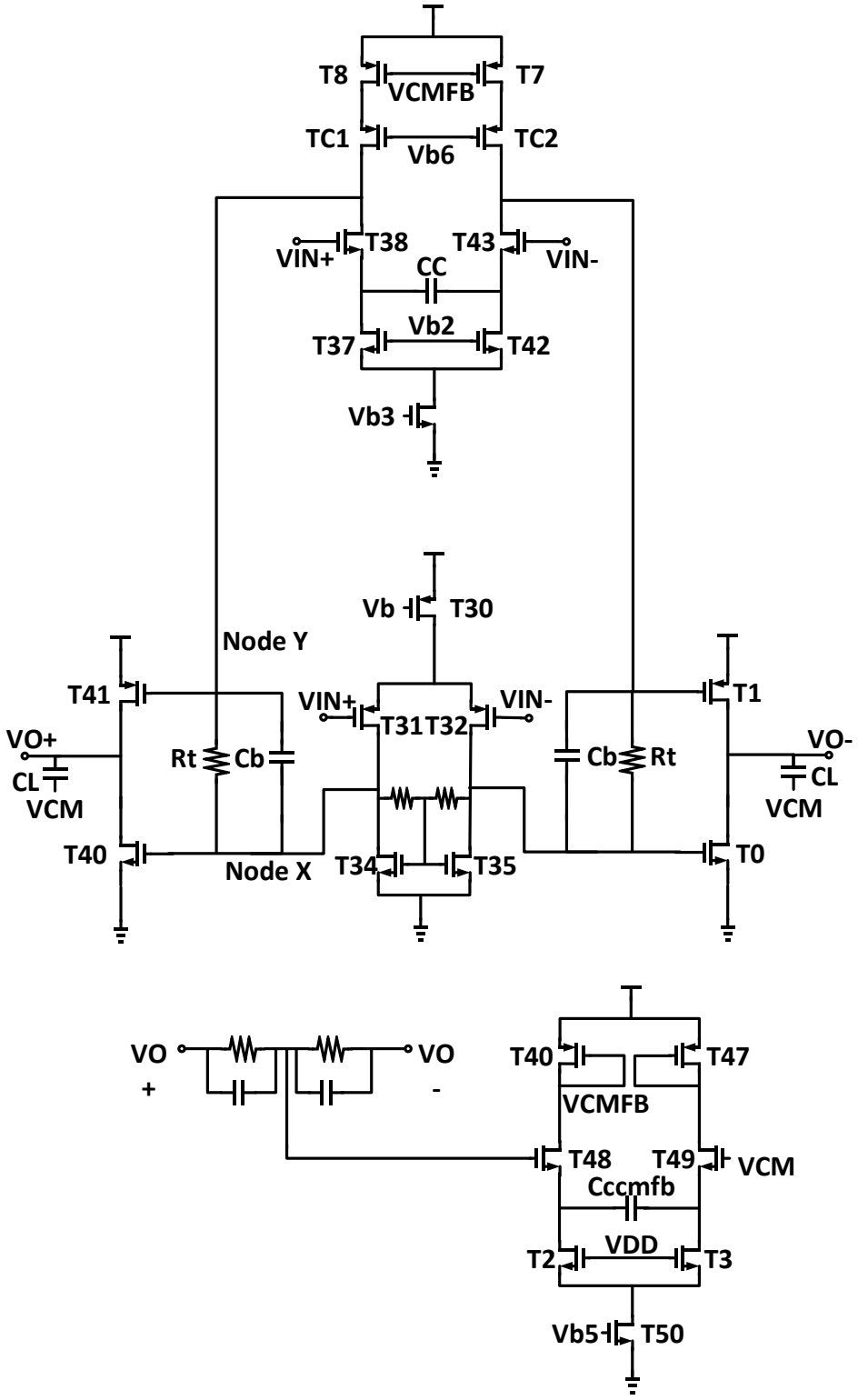

Figure 43: Modified amplifier

The noise simulation results are provided in Figure 44 and Table 8.

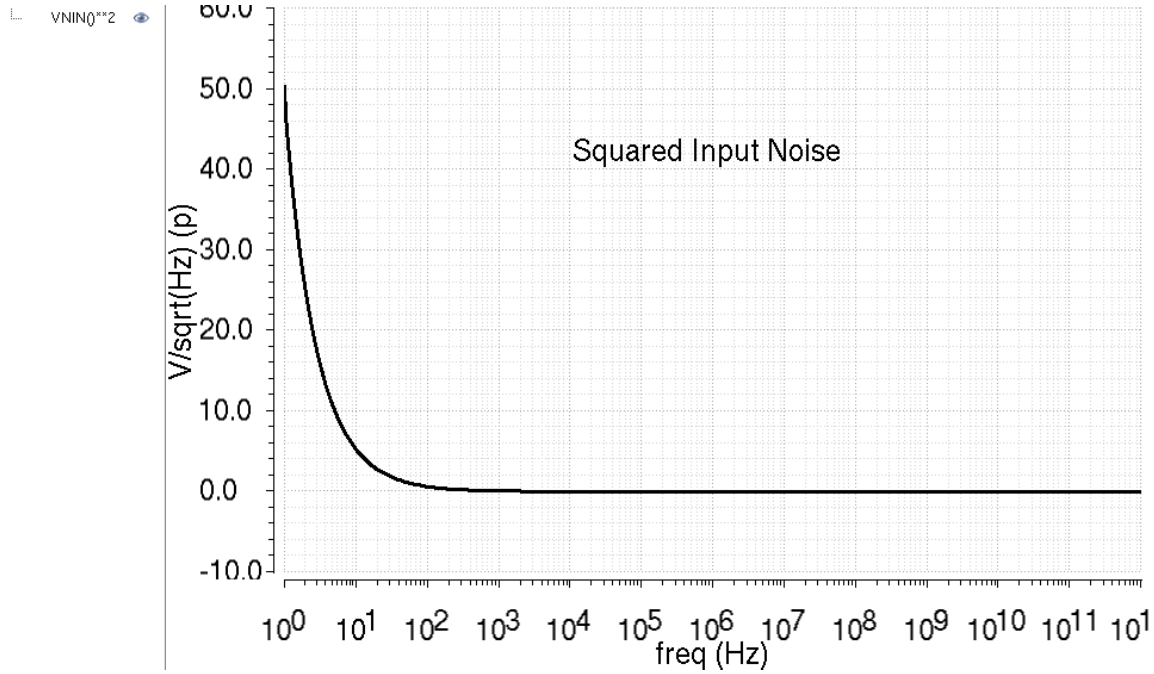

Figure 44: Squared input noise

Table 8: Device noise

Device	Param	Noise Contribution	% Of Total
/I50/T34	fn	0.00540816	25.96
/I50/T33	fn	0.00540816	25.96
/I50/T42	fn	0.00362858	11.69
/I50/T37	fn	0.00362858	11.69
/I50/T42	id	0.00253313	5.70
/I50/T37	id	0.00253313	5.70
/I50/T7	id	0.00159932	2.27
/I50/T6	id	0.00159932	2.27
/I50/T31	id	0.00124907	1.38
/I50/T32	id	0.00124907	1.38

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.0106143
Total Input Referred Noise = 6.26803e-05
The above noise summary info is for noise data

As can be seen, the major contributors of noise are the load transistors of stage 1. This is because the trans-conductance (overdrive) of these devices depends on the output stage NMOS. For good swing the overdrive of output stage NMOS cannot be increased, and so, the trans-conductance of the load devices tends to be large. PMOS input transistors were used to decrease the flicker noise and as per the noise introduced by the feed-forward stage. Since the input transistors are cascaded, they contribute almost no noise and the key contributors are the load PMOS and the source degenerating NMOS. The trans-conductance of these devices were reduced to decrease the noise. The measured noise is integrated up to the bandwidth of the amplifier because all the noise beyond sampling frequency will be folded back. The net noise of the amplifier is $14.6nV^2$ which is less than the required specification of the MDAC.

Also, it was mentioned in section 2.1.1 that most of the noise budget was dedicated for the Op-amp as it directly affects the power consumption. This is because, to have a lower noise the trans-conductance of input transistors has to be large and based on equation 3.28, to have a zero closer to the pole the capacitance of Ca has to be increased and this in turn would require a higher trans-conductance in the feed forward input amplifier to push the non-dominant pole beyond UGB. Hence, maximum noise budget was allotted to the amplifier to decrease the input trans conductance and power.

The amplifier was characterized for five corners and Table 9 shows the simulation results

Table 9: Corner simulations

Corner	TT	FF	SS	FS	SF	Change
UGB(MHz)	1040	1190	910	990	1067	27%
Settling time(ns) (11-bit)	3.881	2.929	4.803	3.417	3.125	48%
Slewrate (V/us)	977	1080	807	960	970	28%
HD3 1.2Vpp@(39.453Mhz) Sampling – 100Mhz	77.84	71.45	69.31	74.39(1.3Vpp)	74.39	11%
Noise(uV)	62	56	61	71	55	26%
Current (mA)	3.83	4.03	3.64	3.77	3.84	10.2%

As can be seen, the Slow-Slow corner has the highest settling time which can be attributed to the decrease in slew rate and the gain bandwidth. The settling time and linearity requirement are satisfied at all corners.

5.2 Switch simulation and results

The linearity and settling time of the switch designed in section 3 was measured using the test-bench in Figure 45. C11 and C46 are the sampling capacitors (2.3pF) and they are connected to the common mode level through a simple MOSFET switch, similar to the sampling phase of the MDAC. The ϕ1n clock of boot-strap is controlled by S1 and

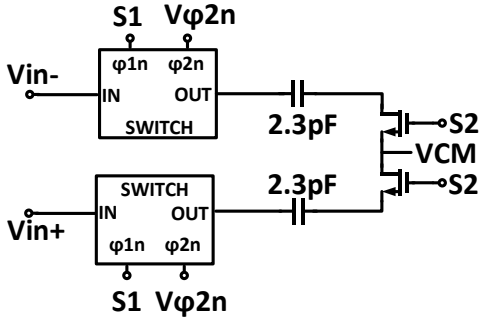

Figure 45: Switch test bench

the S2 is early clocked to prevent charge injection from the switch onto the sampling capacitor. To measure the linearity, the voltage across the two capacitors was taken and subtracted to get the net differential voltage sampled and 256 samples were taken after the output settled after S1 fell and 256 point DFT was performed.

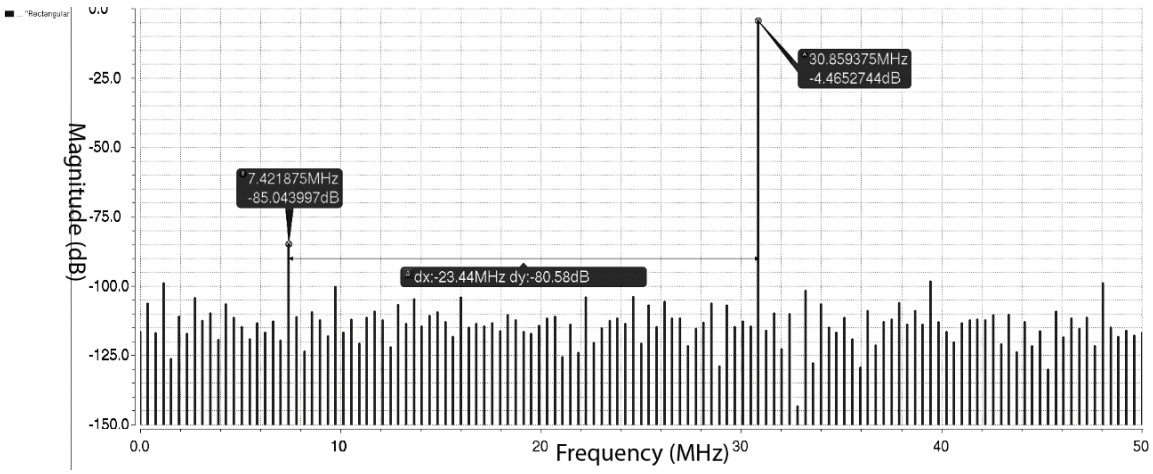

Figure 46: Switch spectrum

Figure 46 shows the spectrum of the switch, and the linearity is above 13 bits as required by the MDAC specification. Another parameter to be observed is the magnitude of the fundamental, it has slightly dropped from the ideal value and this can also be seen in the tracking and settling behavior in Figure 47 and Figure 48 respectively. In Figure 47, immediately after S1 goes to zero the voltage across the capacitor drops slightly, this is due to charge sharing across parasitic capacitors. A similar phenomenon occurs when a pulse is applied at the input. Since this drop in the charge across the capacitors is not impacting the frequency response, it has to be varying linearly with the input magnitude.

This was verified by varying the input step size and checking the final settled value and the response can be seen in Figure 49: it varies linearly with the input step magnitude. This can be easily corrected either by digital post processing or calibration.

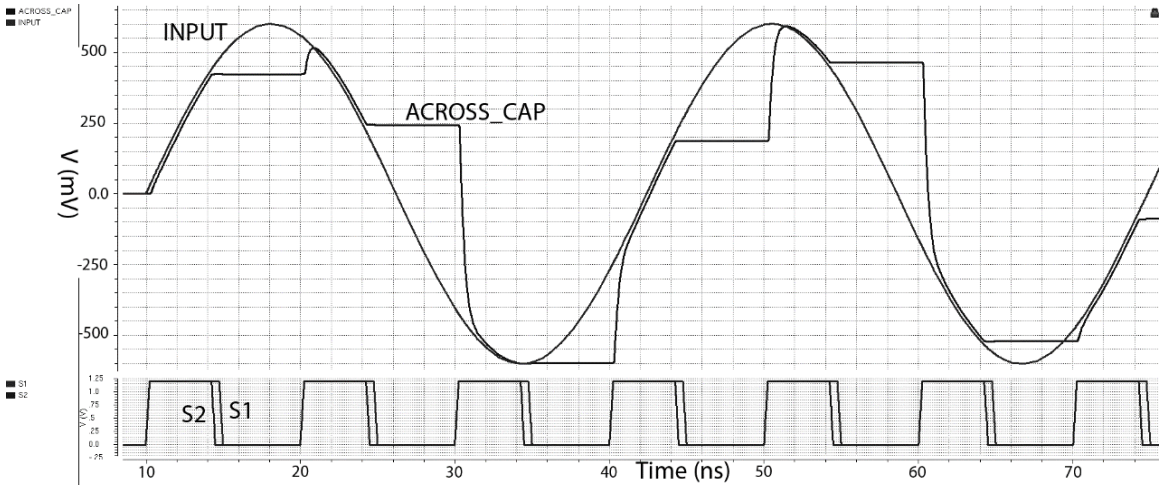

Figure 47: Switch transient behavior

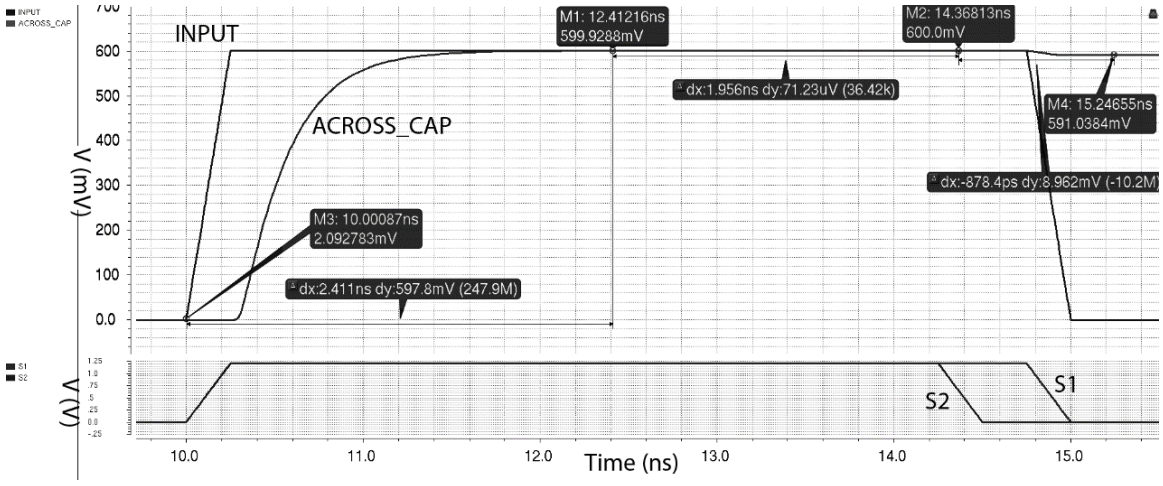

Figure 48: Switch pulse input

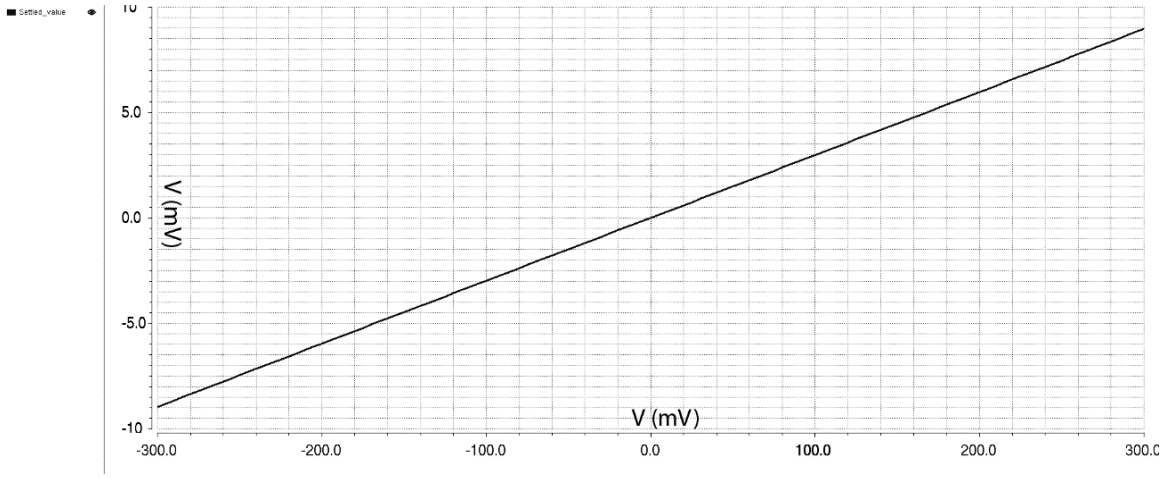

Figure 49: Drop in the voltage across capacitor vs input magnitude (single ended)

5.3 Summary of results and comparisons

In this section the amplifier specifications are compared in-detail with the amplifier used in [32] for the design of a 1.5 bit MDAC for a 14 bit ADC working at a sampling rate of 100MHz, and the advantages and disadvantages of the proposed architecture are highlighted. The amplifier is further compared with other architectures mentioned in literature.

The amplifier used in [32] is a single stage telescopic amplifier with gain boosting. Table 10 provides the specification comparison

Table 10: Comparison 1

	This work [TT]	**[32]**
Technology	IBM 0.13um	TSMC 0.13um
VDD	1.2	2
ADC Resolution	12 bit	14 bit
Sampling Frequency	100MHz	100Mhz
Vpp	1.2	2
Load	3.5pF	3pF
Amplifier type	Two stage	Single stage
DC_gain	47dB	80dB
GBW	1040MHz	1100MHz
Current	3.88mA	8.4m
Settling time	[11-bit] 3.881	Required [> 13-bit in < 5ns]
IM3	75dB -6dBFS @(4.3MHz and 5.08 MHz) 68.46dB -3.5dBFS@(4.3MHz and 5.08 MHz)	68dB -6.48dBFS @(4.75MHz and 5.25MHz)
Noise	62uV up to 50MHz	18uV up to 50MHz
FOM1[MHz*pF/mA]	938	392
FOM2[(V/us)*(pF)/mA]	881	654
FOM3[(V/us)/mA]	251	218
FOM3[ns/mA]	1.01	

Since gain boosting with telescopic architecture was used, the DC gain of the amplifier in [32] is very high, but as VDD decreases using telescopic architecture is generally not optimal and when calibration techniques are used for the ADC a very high gain is not a necessary requirement. The current consumption in [32] is much higher because higher the load capacitance higher is the current required to maintain slew rate. Whereas, a class-AB output stage slew current is independent of the quiescent biasing current and as can be seen in Figure 50, the slew current increases up to 6 times the quiescent current.

Also, the UGB specification is [32] is defined by $\frac{gm}{CL}$ which is again dependent on the load and would require higher trans-conductance and thereby higher current consumption. Whereas, in the proposed architecture if the pole-zero cancellation is exact, the UGB can be given as $A1 * \frac{gm}{CL}$, where A1 is the stage 1 gain. And hence the gm requirement of the second stage is reduced. From the table it can be seen the linearity of the current architecture is better and this can be attributed to the higher overdrive voltages of the output stage transistors (lower gm) and the capacitive short circuit path at high frequencies for the class-AB output NMOS and PMOS transistors.

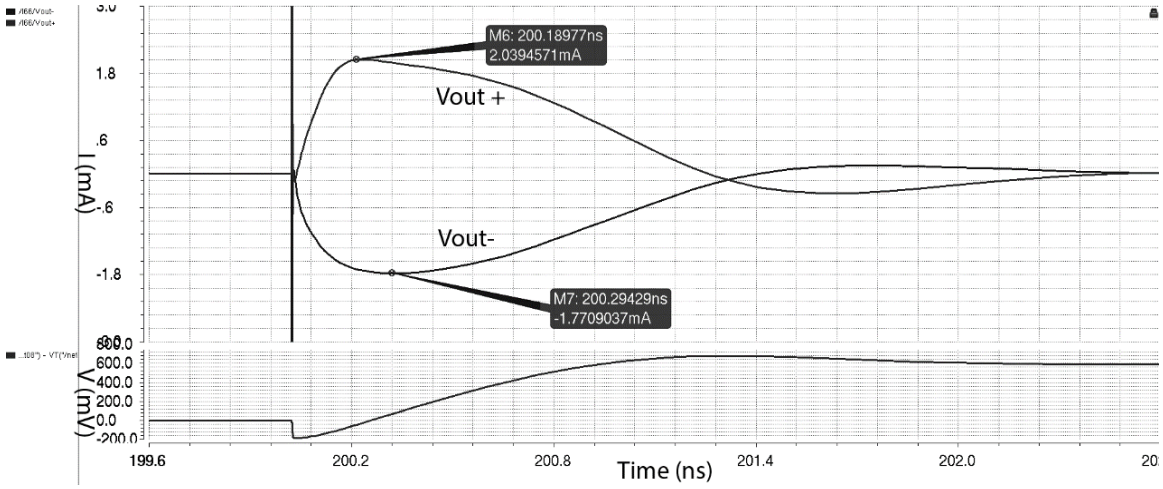

Figure 50: Slew current for class-AB output stage

As discussed in the previous sections, noise specification of the amplifier in the current architecture has a significant impact on the power consumption. To lower the noise the trans-conductance of the input pair has to be increased, which in-turn will increase the

capacitor required to compensate the pole. And this will result in an increase in the feed forward path current. Since the ADC is 12 bit, the current design satisfies the noise requirement.

The amplifiers are compared using the following Figure of Merits

$$FOM1 = \frac{GBW(in\ MHz) * Cload(in\ pF)}{Itotal(in\ mA)} \quad 5.2$$

$$FOM2 = \frac{Slew\_rate(in\ V/us) * Cload(in\ pF)}{Itotal(in\ mA)} \quad 5.3$$

$$FOM3 = \frac{Slew\_rate(in\ \frac{V}{us})}{Itotal(in\ mA)} \quad 5.4$$

$$FOM4 = \frac{Settling\_time(in\ ns)}{Itotal(in\ mA)} \quad 5.5$$

As can be seen from the table the current architecture provides a better figure of merit in terms of FOM1, FOM2 and FOM3. The amplifier is further compared (Table 11) with the sample and hold amplifier used in [33], 10-bit 160MHz pipeline ADC. The amplifier architecture used is Recycling Folded Cascode with gain boosting. Since the feedback factors of the MDAC and the sample and hold amplifier are different only FOM1 can be used for comparison and the current architecture has a better FOM1.

Finally the amplifier is compared with amplifiers form the literature and Table 12 shows the comparison. The amplifier in [34] uses a telescopic cascade architecture with gain boosting and has similar disadvantages to the one in [32] as discussed above. The amplifier in [35] uses a two stage architecture with a telescopic cascade stage 1 and a

Table 11: Comparison 2

	This work [TT]	**[33] [Sample and hold]**
Technology	IBM 0.13um	SMIC 0.18um
VDD	1.2	1.2
ADC Resolution	12 bit	10 bit
Sampling Frequency	100MHz	160MHz
Vpp	1.2	1
Load	3.5pF	1.4pF
Amplifier type	Two stage	Single stage
DC_gain	47dB	90dB
GBW	1040MHz	935MHz
Current	3.88mA	2.6m
HD3	1.2Vpp @ 39.45MHz (100Mhz sampling rate) = 73.45dB	1Vpp @ 90MHz (200MHz sampling rate) = 57.32dB
Noise	62uV upto 50MHz	
FOM1[MHz*pF/mA]	938	503

class A stage with cascade compensation. The cascade compensation can provide a better bandwidth than a simple Miller compensation but it still lowers the dominant pole and stability is attained sacrificing the bandwidth. The amplifier in [36] uses two stage architecture with feed forward compensation thereby overcoming the shortcoming of Miller's compensation but uses a Class A output stage, which even though provides a good linearity results in a large DC current. The amplifier in [37] is a simple two stage miller compensated amplifier and as can be seen from the table even though it is very fast and has a moderate linearity the current consumption is extremely high owing to large load capacitance. Finally the amplifier in [38] uses class-AB (class A biased

Table 12: Comparison 3

	This	**[34]**	**[35]**	**[36]**	**[18]**	**[39]**
Technolog	0.13um	0.35um	0.25um	40nm	90-nm	90-nm
VDD	1.2	3.3	2.5	1.1		
Current	3.88m	4.8m	1m	12m	160m	34m
Vp-p	1.2			1.4		
Load [pF]	3.5	1.4	0.4	2	6	3
DC Gain	47	85.4	88.4	44	28	74
GBW [MHz]	1040	570	320	3000	2860	1000
Phase Margin	47	85.6	62.6	69.4		
Settling (ns)	[11-bit] 3.881	[0.012%] 8.6	[0.1%] 11.3		[13-bit] 1	
HD3	1.2Vpp @ 39.45MHz (100Mhz sampling rate) = 73.45dB			1.4Vpp@ 25MHz (200 Mhz sampling rate) = 64dB	@100Mhz (200 Mhz sampling rate) 57dB	1.5Vpp(160 Mhz sampling rate)-75dB
FOM1[MHz*pF/m	938	166.25	200.16	500	107.25	88
FOM2[(V/us)*(pF)/	881	242.6	128			

invertor) output stage using a switched capacitor level shifter and Miller's compensation. Over-all if the FOM are compared the current architecture because of class-AB output stage and the modified feed forward compensation provides a power efficient architecture for high linearity and moderate gain amplifiers generally required by calibrated pipelined ADC.

6. CONCLUSION

In this thesis, a class-AB amplifier using a novel DC-level shifter and a feed-forward compensation architecture has been proposed for the design of a 1.5 bit MDAC of a 12-bit pipeline ADC. The need for a moderate gain, high speed and high linearity requirements for an ADC was discussed and the design specifications were calculated from the performance requirements of the MDAC in a top-down fashion. An improved DC-level shifting scheme for class-AB amplifiers has been proposed and compared with existing schemes in terms of linearity improvement. A feed-forward compensation technique that can be used in parallel with the level shifter has been proposed and the amplifier design based on the new architecture showed a good linearity at low power consumption. A boot-strap switch design procedure was also explained and the linearity and settling time of the switch were tested. The implementation has been carried out in IBM 130nm.

REFERENCES

[1] B. Murmann, "ADC Performance Survey 1997-2015," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

[2] E. Siragusa and I. Galton, “A digitally enhanced 1.8V 15b 40MS/s CMOS pipelinedADC," in IEEE International Solid-State Circuits Conference, Digest of Technical Papers, February 2004, vol. 1, pp. 452-453.

[3] H. Liu, Z. Lee, and J. Wu, “A 15b 20MS/s CMOS pipelined ADC with digital background calibration," in IEEE International Solid-State Circuits Conference, Digest of Technical Papers, February 2004, vol. 1, pp. 454-455.

[4] K. Nair and R. Harjani, “A 96dB SFDR 50MS/s digitally enhanced CMOS pipeline A/D converter," in IEEE International Solid-State Circuits Conference, Digest of Technical Papers, February 2004, vol. 1, pp. 456-457.

[5] H. Lee, M. Miyahara and A. Matsuzawa, "A 12-bit interpolated pipeline ADC using body voltage controlled amplifier," New Circuits and Systems Conference (NEWCAS), 2013 IEEE 11th International, Paris, 2013, pp. 1-4.

[6] H. C. Choi , Y. J. Kim , G. C. Ahn and S. H. Lee, "A 1.2-V 12-b 120-MS/s SHA-free dual-channel Nyquist ADC based on midcode calibration", IEEE Trans. Circuits Syst. I, vol. 56, no. 5, pp. 894-901, 2009

[7] T. Leichti, A. Tajalli, O. Can, Z. Toprak, and Y. Leblebici. A 1.8V 12-bit 230-MS/s Pipeline ADC in 0.18μm CMOS Technology. IEEE Asia-Pacific Conference on Circuits and Systems 2008, Macao, China.

[8] B. Razavi and B. Wooley, “Design techniques for high-speed, high-resolution comparators," IEEE Journal of Solid-State Circuits, vol. 27, no. 12, pp. 1916-1926,December 1992.

[9] H. Adel, M.-M. Louerat, and M. Sabut, “Design considerations for low gain amplifier in the MDAC of digitally calibrated pipelined ADCs,” in Proc. IFIP/IEEE Int. Conf. Very Large Scale Integr. (VLSI-SOC 2013), 2013.

[10] A. Verma and B. Razavi, “A 10-Bit 500-MS/s 55-mW CMOS ADC,” IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 3039–3050, Nov. 2009

[11] D. Johns and K. Martin, Analog Integrated Circuit Design, John Wiley and Sons, Inc., 1997.

[12] K.C. Dyer, D. Fu, S.H. Lewis, P.J. Hurst, “An Analog Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters”, IEEE J. Solid-State Circuits, vol. 33, no. 12, pp. 1912-1919, Dec. 1998

[13] S.R. Sonkusale, J. Van der Spiegel, K. Nagaraj, “Background Digital Error Correction Technique for Pipelined Analog-Digital Converters”, IEEE Int. Sym. on Cir. and Systems, pp. 408-411, 2001

[14] A.J. Gines, E.J. Peralias, A. Rueda, “Digital Background Calibration Technique for Pipeline ADCs with Multi-Bit Stages”, IEEE Int. Symp. Circuits Syst., pp. 317-322, Sept. 2003

[15] Y. Chiu, C.W. Tsang, B. Nikolic, P.R. Gray, "Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters", IEEE Trans. on Circuits Syst. I, vol. 51, no. 1, pp. 38-46, Jan. 2004

[16] J.P. Keane, P.J. Hurst, S.H. Lewis, “Background Interstage Gain Calibration Technique for Pipelined ADCs”, IEEE Trans. on Circuits Syst. I, vol. 52, no. 1, pp. 32-43, Jan. 2005

[17] H. Van de Vel, B.A.J. Buter, H. van der Ploeg, M. Vertregt, G.J.G.M. Geelen, E.J.F. Paulus, "A 1.2-V 250-mW 14-b 100-MS/s Digitally Calibrated Pipeline ADC in 90-nm CMOS", IEEE J. Solid-State Circuits, vol. 44, no. 4, pp. 1047-1056, April 2009

[18] B. D. Sahoo and B. Razavi, “A 12-bit 200-MHz CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2366–2380, Sep. 2009.

[19] M. Dessouky and A. Kaiser, “Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch boot-strapping," IEEE Journal of Solid-State Circuits, vol. 36, no. 3, pp. 349-355, March 2001.

[20] A. Abo and P. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," IEEE Journal of Solid-State Circuits, vol. 34, no. 5, pp. 599-606, May 1999.

[21] M.Y. Azizi, A. Saeedfar, H.Z. Hoseini, and O. Shoaei, “Thermal noise analysis of multi-bit SC gain-stages for low-voltage high-resolution pipeline ADC design,” In Signals, Circuits and Systems, 2003. SCS 2003. International Symposium on, volume 2, pages 581 –584 vol.2, 2003.

[22] C. Y. Lu et al., "A 25 MHz bandwidth 5th-order continuous-time low-pass sigma-delta modulator with 67.7 dB SNDR using time-domain quantization and feedback," IEEE J. Solid-State Circuits, vol. 45, no. 9, pp. 1795-1808, Sep. 2010.

[23] V. Dhanasekaran et al., “A 20MHz BW 68dB DR CT $\Delta\sum$ ADC based on a multi-bit time-domain quantizer and feedback element,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2009, pp. 174-175.

[24] L. J. Breems, R. Rutten, R. van Veldhoven, G. van der Weide, and H. Termeer, “A 56mW CT quadrature cascaded $\sum\Delta$ modulator with 77dB DR in a near zero-IF 20MHz band,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2007, pp. 238-239.

[25] V. Peluso, P. Vancorenland, M. Steyaert, and W. Sansen, ”900mW differential class-AB OTA for switched Op-amp applications,” *Electron. Lett.*, vol. 33, no. 17, pp. 1445-1456, Aug. 1997.

[26] F. You, S. H. K. Embabi, and E. Sanchez-Sinencio, ”Low-voltage class-AB buffers with quiescent current control,” *IEEE J. Solid-State Circuits*, vol. 33, no. 6, pp. 915-920, Jun. 1998.

[27] D. M. Monticelli, “A quad CMOS single-supply op amp with rail-to-rail output swing,” *IEEE J. Solid-state Circuits*, vol. SC-21, no. 6, pp. 1026-1034, Dec. 1986.

[28] K. de Langen and J. H. Huijsing, ”Compact low-voltage power-efficient operational amplifier cells for VLSI,” *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1482-1496, Oct. 1998

[29] Krishnan, Lakshminarasimhan (2011). High Performance Class-AB Output Stage Operational Amplifiers for Continuous-time Sigma-delta ADC. Master's thesis, Texas A&M University. Available electronically from http://hdl.handle.net/1969.1/ETD-TAMU-2011-08-9896

[30] B. K. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller Capacitors," IEEE J. Solid-State Circuits, vol. 38, no. 2, pp. 237-243, Feb. 2003.

[31] M. Dessouky, M. -M. Louerat, A. Kaiser, "Switch Sizing for Very Low-Voltage Switched-Capacitor Circuits", IEEE, 2001, pp. 1549-1552;

[32] Larsson, Andreas 1978- (2012). Nyquist-Rate Switched-Capacitor Analog-to-Digital Converters. Doctoral dissertation, Texas A&M University. Available electronically from http : / /hdl .handle .net /1969 .1 /148307.

[33] Assaad, R. S. (2009). Design Techniques for High Speed Low Voltage and Low Power Non-Calibrated Pipeline Analog to Digital Converters (Doctoral dissertation, Texas A&M University).

[34] J. A. Diaz-Madrid, H. Neubauer, H. Hauer, G. Domenech-Asensi and R. Ruiz-Merino, "Power reduction of a 12-bit 40-MS/s pipeline ADC exploiting partial amplifier sharing," Design, Automation & Test in Europe Conference & Exhibition, 2009. DATE '09., Nice, 2009, pp. 369-373.

[35] S. Q. Liang, Y. S. Yin, H. H. Deng, Y. K. Song and M. L. Gao, "A low power consumption, high speed Op-amp for a 10-bit 100MSPS parallel pipeline ADC," Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference on, Macao, 2008, pp. 818-821.

[36] H. Adel, M. Sabut and M. M. Louerat, "1.1-V 200 MS/s 12-bit digitally calibrated pipeline ADC in 40 nm CMOS," Circuits and Systems (ISCAS), 2015 IEEE International Symposium on, Lisbon, 2015, pp. 2281-2284.

[37] K.C. Dyer, D. Fu, S.H. Lewis, P.J. Hurst, "An Analog Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters", IEEE J. Solid-State Circuits, vol. 33, no. 12, pp. 1912-1919, Dec. 1998

[38] S.R. Sonkusale, J. Van der Spiegel, K. Nagaraj, “Background Digital Error Correction Technique for Pipelined Analog-Digital Converters”, IEEE Int. Sym. on Cir. and Systems, pp. 408-411, 2001

[39] Huber D J, Chandler R J. A 10 b 160 MS/s 84 mW 1 V subranging ADC in 90 nm CMOS. ISSCC Dig Tech Papers, 2007:455