CLASS-AB AMPLIFIER WITH THIRD ORDER NONLINEARITY CANCELLATION

A Thesis

by

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Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

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August 2016

Major Subject: Electrical Engineering

ABSTRACT

Class-AB amplifiers have better power efficiency than class-A amplifiers, which makes them a suitable choice for pipeline ADCs where low power, high performance opamps are desired. However, class-AB amplifiers have significantly lower linearity compared to class-A amplifiers due to the problem of cross-over distortion.

In this work, the problem of designing power efficient, high linearity class-AB amplifiers is addressed. The Monticelli bias scheme, which is the most popular class-AB bias scheme today, is analyzed. A new class-AB bias scheme, which is highly robust to process variations and achieves better linearity than the Monticelli bias scheme, is proposed. The problem of "cross-over distortion" in the class-AB amplifier is addressed and a solution is proposed. The idea behind this method is that the third order nonlinearity in the class-AB amplifier can be reduced or eliminated by matching the output stage NMOS and PMOS transistor transconductance across the input signal range, ensuring a constant transconductance at the output, improving linearity performance. To ensure good matching across process, voltage and temperature variations (P.V.T), a feedback calibration scheme is proposed.

DEDICATION

To my parents.

ACKNOWLEDGEMENTS

I am deeply indebted towards my advisor, Dr. Silva-Martinez for his great support and guidance. When I first met Dr. Silva, I was a transfer student at Texas A&M University and was very new to analog circuit design. During the summer of 2014, I got the opportunity to start my thesis work with him as my advisor on a very interesting idea for nonlinearity cancellation in the class-AB amplifier. I had long discussions with him that really enhanced my interest and passion for this subject and improved my fundamental understanding. Dr. Silva has always been very patient in explaining concepts, however fundamental they were and I feel really honored to have worked with him these last two years.

I am also grateful towards Dr. Karsilayan for closely working with me on my project during the initial period and for his valuable suggestions on my work. The graduate course, which I studied with him, "VLSI Circuit Design" really helped develop my basic analog design skills. I would like to thank Dr. Sam Palermo for teaching me his course, "High Speed Links Circuits and Systems", which introduced me to mixed signal design. I would like to thank my other committee members, Dr. Hu and Dr. Jo for their guidance and support throughout the course of this research. I would like to thank Dr. Srinivas Shakkottai for kindly consenting to attend my thesis defense as a substitute examiner. I would also like to thank the ECE department and staff, Tammy Carda, Jeanie Marshall and Melissa Sheldon for helping with me all administrative tasks.

I would also like to thank my friends, colleagues and mentors, Anand, Francy, Rajiv, Naveen, Arihant and Srivatsa without whose help and encouragement, I would not have finished my thesis. Finally, thanks to my parents for everything.

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1. INTRODUCTION

1.1. Motivation

The ever growing demand for portable battery operated consumer electronics such as mobile phones and digital cameras have put greater performance requirements on analog to digital converters (ADCs). Good power efficient ADC architectures are a necessity to extend the battery life of these electronic gadgets. The pipeline ADC is a good candidate to meet such requirements being able to support high sampling rates as well as moderate resolution (8-14 bits) [1, 2, 3, 4, 5]. Pipeline ADCs are mainly driven, nowadays by sensors used in portable electronics and high speed instrumentation. A few applications exist in the military where high performance is the major concern. Figure 1 shows an application, digital photography for the pipeline ADC. Currently, many of the functions that were previously implemented in analog are now being moved to the digital domain. As CMOS technology keeps advancing, they bring in greater digital signal processing power. This has caused the ADC to become the bottleneck for achieving high performance and power efficiency in the system. The research on pipeline ADCs is focused in the direction of maximizing both performance and power efficiency.

Figure 1 Digital photography

Incorporating digital calibration into pipeline ADCs has helped in greatly relaxing the requirements on analog circuitry such as fast settling and high gain [6, 7, 8, 9]. Digital circuitry are much more robust to process, voltage and temperature variations than analog circuitry. It is easier to implement complex functions in digital logic than in analog. In pipeline ADCs, digital calibration is utilized to correct for errors between the real analog signal and the sampled signal. Such digitally assisted analog systems can help achieve large resolution in pipeline ADCs.

The pipeline ADC consists of several stages cascaded together. Each stage in a pipeline ADC converts the analog signal into a digital code at a much lower resolution than the total resolution of the entire ADC. The error between the real signal and the sampled signal that is obtained at each stage is called the residue. This residue is then amplified and sent to the next pipeline stage. The main power hungry block in the pipeline ADC is the residue amplifier accounting for as much as half of the total power in some cases. These amplifiers also require fast settling within one LSB (Least Significant Bit).

These requirements motivate us to consider using class-AB amplifiers as opposed to the conventional class-A amplifiers in these residue stages. The class-AB output stage is an ideal candidate for high performance opamps which require large open loop gain and fast settling properties without having large power consumptions. The class-AB amplifier

can be designed to consume a very low static power, while providing large currents during large signal operation without slewing. The slew rate is not determined by its bias current. In contrast, class-A amplifiers have their slew rates limited by the bias current, representing a power-performance tradeoff.

In this thesis, the existing Monticelli level shifter that is the state of the art for class-AB amplifiers is studied and its drawbacks are analyzed. A new class-AB output stage is proposed that is more suitable for applications which require high linearity. Further, we also attempt to solve a problem inherent in class-AB amplifiers-"cross-over distortion". The cross-over distortion, which is a problem for class-B amplifiers when the signal switches from one transistor to another also affects class-AB amplifiers. We first analyze this problem theoretically, and propose a solution.

1.2 Thesis organization

This thesis covers the design and implementation of class-AB amplifiers as well as the problem of their inherent nonlinearity.

Section 2 introduces and compares the class-A and class-AB amplifiers. We discuss various class-AB implementations in literature, primarily focusing on the Monticelli level shifter which is the most widely used design in industry today. We also discuss some drawbacks of this architecture. To address these drawbacks, namely the linearity, a new class-AB output stage is proposed and a class-AB amplifier is designed based on this output stage.

Section 3 discusses the issue of nonlinearity in class-AB amplifiers. It addresses it from a theoretical perspective as well as discusses a method to cancel nonlinearity in the class-AB amplifier. Finally the limitations of this technique and future work that can be undertaken in this direction are described.

Section 4 shows the simulation results for the two class-AB amplifiers described in section 2.

2. CLASS-AB AMPLIFIER DESIGN

This section describes the working principle of the class-A, class-B and class-AB output stages. It also discusses the architecture and implementation of the conventional class-AB amplifier, which is based on the Monticelli level shifter. Finally, we propose a new class-AB output stage that addresses some of the drawbacks of the conventional architecture, and its implementation in an amplifier.

2.1 Class-A output stage

The class-A output stage is preferred in opamps where good linearity is critical. The peak AC current that the class-A output stage can supply is not more than the quiescent current or the bias current. The slew rate of the class-A output stage is dependent on the bias current. This makes it very power inefficient.

In the class-A output stage, one of the transistors is turned ON during the entire operation. The fixed current source used here determines the bias currents under DC condition. A simple class-A output stage is shown in Figure 2 below.

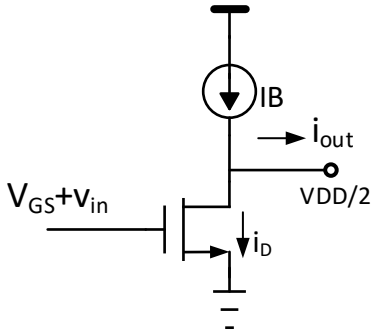

Figure 2 Class-A output stage

The small –signal characteristics of the class-A output stage is plotted in Figure 3. It is seen that the output current of the amplifier saturates to the bias current when large signals are applied. This leads to clipping which causes large-signal distortion in the amplifier.

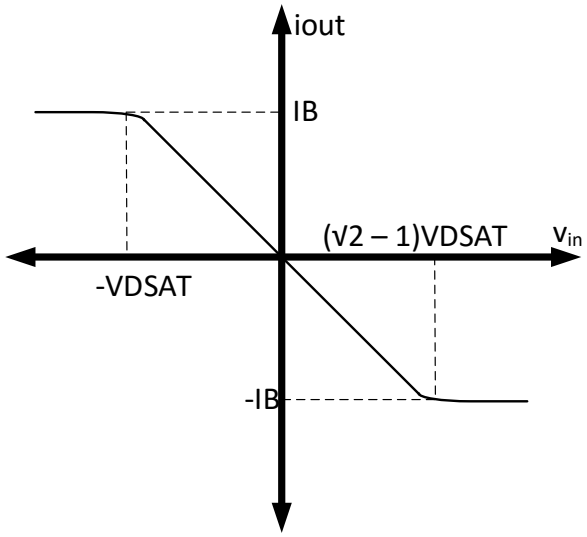

Figure 3 Class-A I-V characteristics

The output current in the class-A output stage can be expressed as,

$$\mathrm{i_{OUT}} = \mathrm{IB} - \mathrm{i_D} \tag{2.1}$$

The transistor is in saturation when $\mathrm{v_{in}} \geq -\mathrm{V_{DSAT}}$ and the drain-source voltage, $V_{DS} \geq V_{GS} - V_T$, equation (2.1) can be rewritten as

$$\mathrm{i_{out}} = IB - K(V_{GS} - V_T + v_{in})^2$$

$$\mathrm{i_{out}} = IB - K(V_{DSAT} + v_{in})^2$$

$$\mathrm{V_{DSAT}} = \mathrm{V_{GS}} - \mathrm{V_T}; \mathrm{K} = \frac{\mathrm{Kn'(W/L)}}{2}$$

Since $IB = K(V_{DSAT})^2$ under DC bias condition,

$$i_{out} = -KV_{DSAT}v_{in} - Kv_{in}^2 \tag{2.2}$$

The above equation shows that the class-A amplifier is linear as long as signal amplitude is small. At large signal amplitudes, the quadratic term introduces nonlinearity.

Further when the signal, $V_{in}$is so large that the NMOS transistor turns OFF,

$$\mathrm{i_{OUT}} = \mathrm{IB} \tag{2.3}$$

Thus the output current saturates to IB and causes hard nonlinearity.

Hence this region needs to be avoided in the operational range to achieve good linearity. Another advantage of the class-A amplifier is that the bias current is typically implemented using a current mirror that copies a reference current, which makes it P.V.T insensitive. The class-A amplifier is commonly used in the differential pair where good

linearity can be achieved as long as the input differential signal does not exceed $\sqrt{2}$ times the V_{DSAT} of the input transistors, leading to one of them turning off.

The observation that the peak output current achieved under large signal operation is limited to IB, brings us to expect the slew rate is also limited to it. The slew rate for a given load depends on the peak current that can be supplied to the load.

$$SR+= \frac{IB}{C_L} \tag{2.4}$$

This shows that the class-A Amplifier is power inefficient for applications where large slew rate is critical such as modern A/D converters.

2.2. Class-B output stage

In the class-B amplifier, the conduction angle is 180 degrees, which implies that the output stage transistors are turned ON only for half the signal period. The idea is that static power can be conserved by turning OFF the transistors when there is no signal amplification. Each of the transistors in the output stage are active and they conduct during alternate cycles, which leads to a push-pull effect. Thus, the power efficiency of the class-B amplifier is much higher than the class-A amplifier. The theoretical efficiency of the class-B amplifier is 78.5% [10].

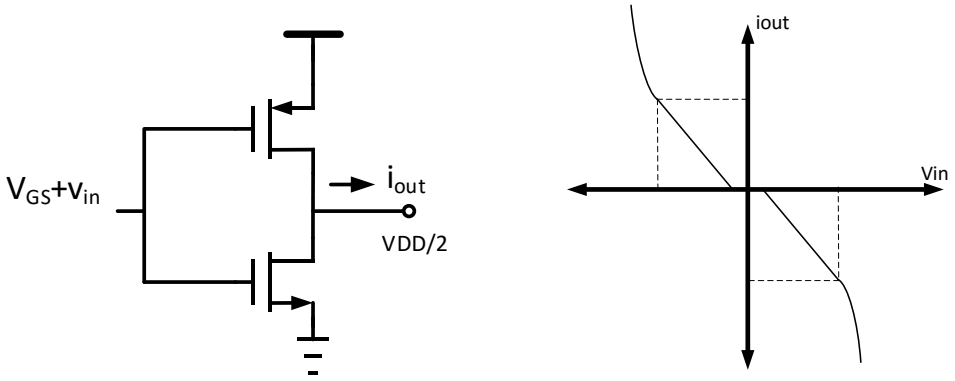

Figure 4 Class-B output stage and its I-V characteristics

The I-V characteristics of the class-B amplifier [11] are shown in Figure 4. Ideally, operating regions of the NMOS and PMOS transistors should cover the full range of the signal. However the characteristics indicate the existence of a dead-band around the DC bias point where neither transistor is conducting nor there is any AC current. This phenomenon, called "cross-over distortion" is a severe cause of nonlinearity in the class-B output Stage. This distortion exists mainly for small signal amplitudes around the DC bias point. As the signal becomes very large, it saturates and hard nonlinearity will be observed.

2.3 Class-AB output stage

In the class-AB output stage, a small quiescent current exists even when there is no signal to eliminate the dead-band. This makes the amplifier less power efficient compared to the class-B amplifier, as there is a finite static power dissipation.

It should be noted that the difference between the class-B output stage and the class-AB output stage is the region where the output stage transistors are biased. Both the class-B and class-AB output stages contain active transistors. For good power efficiency, the quiescent current with which the output stage is biased should be much smaller than the peak AC current. It is common to use a ratio of 3-4 for the peak AC current to the quiescent current or DC current.

The peak current in a class-AB output stage can theoretically be infinite. This makes the class-AB output stage a good choice for driving large capacitive loads. The I-V characteristics for the class-AB Output stage are given in Figure 5.

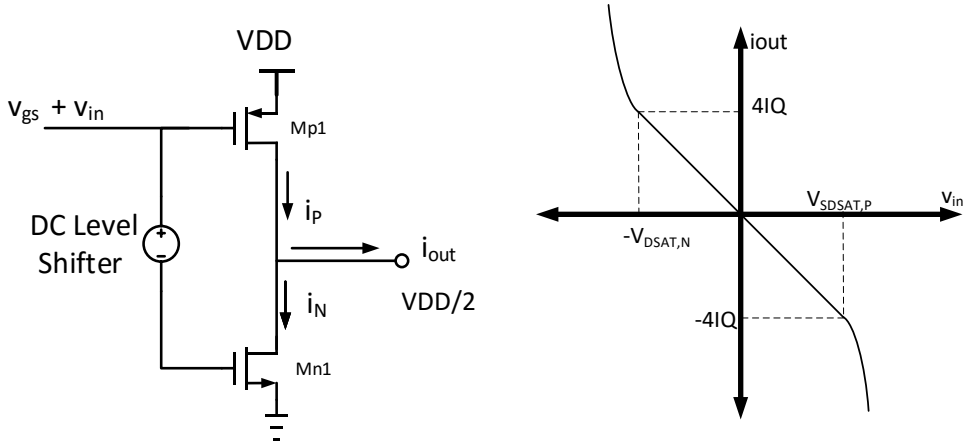

Figure 5 Class-AB output stage and I-V characteristics

The output current in the class-AB output stage shown in Figure 5 is given by:

$$i_{OUT} = i_p - i_n$$

where $i_p \; and \; i_n$are the drain currents of the NMOS and PMOS transistors.

$$i_{OUT} = K_p\left(V_{SDSAT,P} - v_{in}\right)^2 - K_n\left(V_{DSAT,N} + v_{in}\right)^2; \text{for } -V_{DSAT,N} < v_{in} < V_{SDSAT,P}$$

$$V_{DSAT,N} = V_{GS,N} - V_{T_N} \quad ; \; K_N = \mu_N C_{ox}\left(\frac{W}{L}\right)_N$$

$$V_{SDSAT,P} = V_{SG,P} - |V_{T_P}| \quad ; \; K_P = \mu_P C_{ox}\left(\frac{W}{L}\right)_P$$

If $V_{DSAT,N} = V_{DSAT,P}$ and $K_N = K_P = K$

$$i_{OUT} = -4KV_{DSAT}v_{in}; \text{ for } -V_{DSAT,N} < v_{in} < V_{SDSAT,P} \tag{2.5}$$

$$i_{OUT} = -K_N\left(V_{DSAT,N} - v_{in}\right)^2 ; \text{ for } v_{in} \geq V_{SDSAT,P} \tag{2.6}$$

$$i_{OUT} = K_P\left(V_{SDSAT,P} - v_{in}\right)^2 ; \text{ for } v_{in} \leq -V_{DSAT,N} \tag{2.7}$$

From the above equations, it can be concluded that there are 3 regions of operation for the class-AB output stage-

(1) PMOS transistor is OFF when $v_{in} < V_{SDSAT,P}$. In this region, the NMOS transistor sinks all the current from the load.

(2) NMOS transistor is OFF when $v_{in} > -V_{DSAT,N}$. In this region, the PMOS transistor sources all the current to the load.

(3) Both the NMOS and PMOS transistors are ON and in saturation when $V_{DSAT,N} < v_{in} < V_{SDSAT,P}$

It is seen that in the third region, if the V_{DSAT} and K_N and K_P of the NMOS and PMOS transistors in the output stage are matched, the output current is linearly dependent

on the signal voltage. Thus, cross over distortion is observed in the class-AB output stage if the signal is larger than the V_{DSAT} of the output stage transistors.

The other advantage of the class-AB amplifier is the absence of any slew rate limitation. The slew rate is independent of the bias current, so there is no tradeoff here with the power consumption. The ability of the class-AB output stage to instantaneously supply or sink large currents without slewing makes it a good candidate for the high performance opamps used in A/D converters.

The slew rate of the class-AB amplifier is given by,

$$SR+= \frac{K\left(V_{DSAT,P} - v_{in}\right)^2}{C_L} \tag{2.8}$$

To bias the transistors with a low quiescent current, a DC level shifter is required as demonstrated conceptually in the Figure 6.

Some of the properties of a good Level shifter are detailed below.

The DC Level shifter needs to accurately control the output stage quiescent currents, independent of the supply voltage across different process corners. It needs to transfer the AC signal without any attenuation. It should not reduce the DC gain of the amplifier.

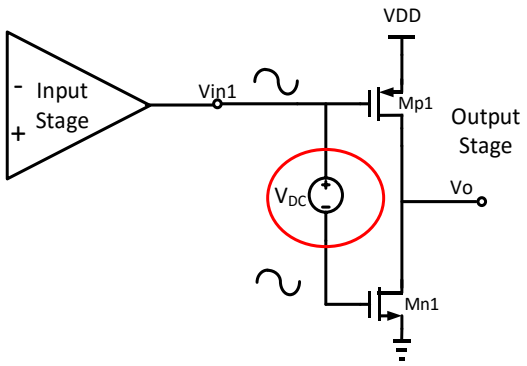

Figure 6 Class-AB level shifter

The level shifter design is undoubtedly, the most challenging aspect of the class-AB amplifier design. Several level shifter designs exist in literature. A simple complementary source follower level shifter is shown in Figure 7 [10]. It provides good control over the quiescent current and also has good frequency domain characteristics. The circuit has ease of implementation. However it has drawbacks such as a low output impedance and poor output swing; the maximum and minimum values of the output is given by $V_{DD} - V_{SDSAT,P3} - V_{GS,N1}$ and $V_{DSAT_{N3}} + V_{SG,P1}$. To solve the problem of swing limitation, the output stage is designed using transistors operating in common source configuration.

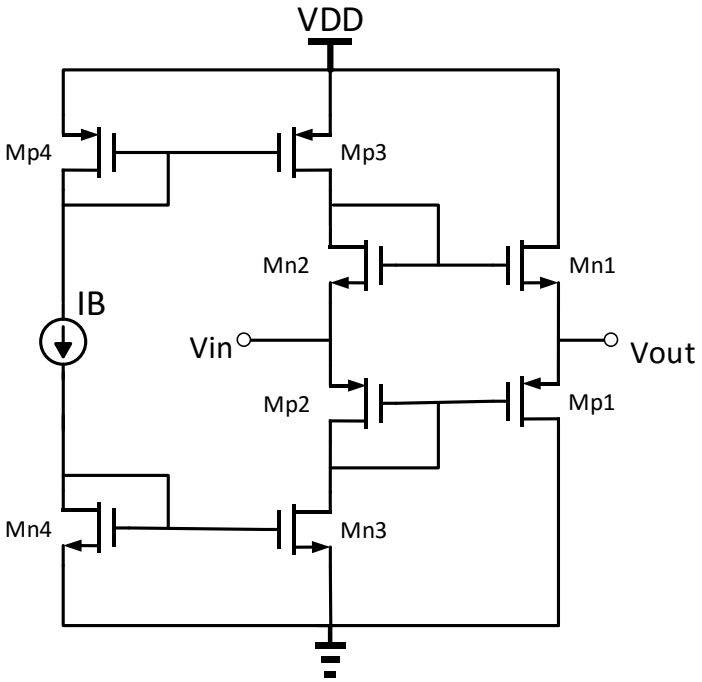

Figure 7 Complementary source follower level shifter

2.3.1 Monticelli level shifter

The Monticelli level shifter [12] is a very popular biasing scheme for the class-AB output stage. It achieves an accurate control of the quiescent control using the quadratic trans-linearity principle [13]. The output stage transistors' biasing is achieved by two trans-linear loops.

The basic principle of this level shifter is that the sum of the currents through the floating transistors M_{2N} and M_{2P} is fixed by the top and bottom current sources, M_{4P} and M_{4N}. The sum of the currents through these two transistors cannot exceed the top and bottom current sources in accordance with KCL. The gates of the output stage transistors

are low impedance nodes since they are connected to the source nodes of transistors M_{2N} and M_{2P}. Any signal applied at these nodes are used to bias the output stage transistors and cannot leak to the ground.

At equilibrium the currents through M_{2N} or M_{2P} are kept almost equal to allow V_X and V_Y to swing symmetrically in positive and negative directions.

When a positive signal is applied at V_Y i.e. the source of $M_{2N,}$ its V_{GS} decreases, thereby reducing its drain current. However, since the sum of the drain currents of M_{2N} and M_{2P} are fixed by IB, the V_{SG} of M_{2P} increases so as to increase its corresponding drain current. This causes the node V_X to effectively track the node, V_Y and the signal is transferred.

Similarly, when a negative signal is applied at V_Y, the V_{GS} of M_{2N} increases, causing its drain current to increase, and the drain current of M_{2P} to decrease and hence V_X is forced to track V_Y.

This represents a clever way to perform the level shift operation. The operation is also quite robust across P.V.T. variations as the nodes V_X and V_Y are low impedance nodes. Further the currents in the two transistors, M_{2N} and M_{2P}, can tolerate small amount of mismatch, they need not be exactly equal to each other as long as the sum is fixed.

The Monticelli Level shifter, shown in Figure 8, however suffers from some problems as detailed below.

The control transistors M_{2N} and M_{2P} are biased using diode connected transistors in this implementation. Thus it is evident that this level shifter is not suited for very low supply voltages (less than 1.8V).

The circuit also suffers from hard nonlinearity when a large signal is applied at either of the nodes V_X or V_Y . This can be understood by looking at the small signal equivalents of the circuit.

In Figure 9, I_{in} is the injected current generated by the first transconductance stage. Iin is converted into a voltage V_Y, by the impedance Z_1. As the equilibrium current in the control transistors, M_{2N} and M_{2P} is equal to half the current in the current sources, IB, the circuit can only track AC currents that are less than IB/2.

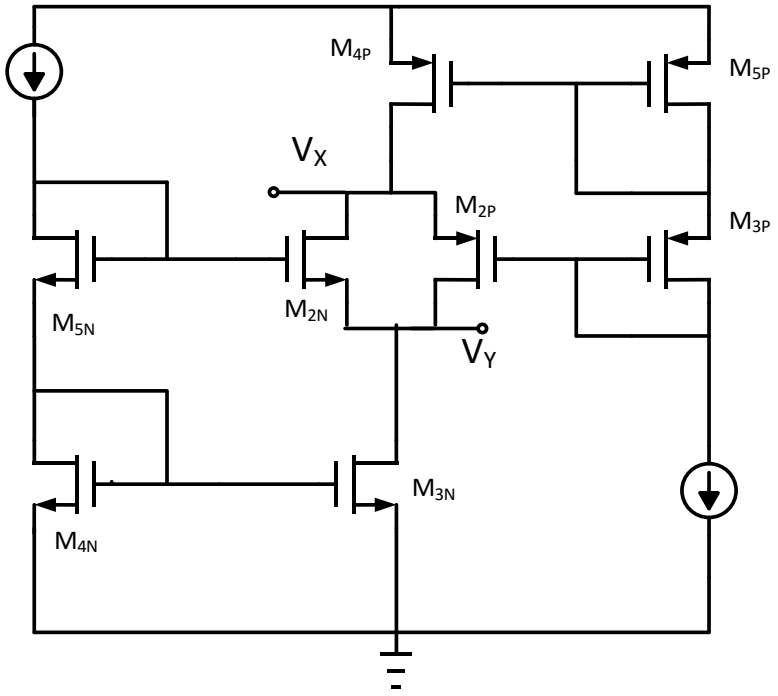

Figure 8 Monticelli level shifter

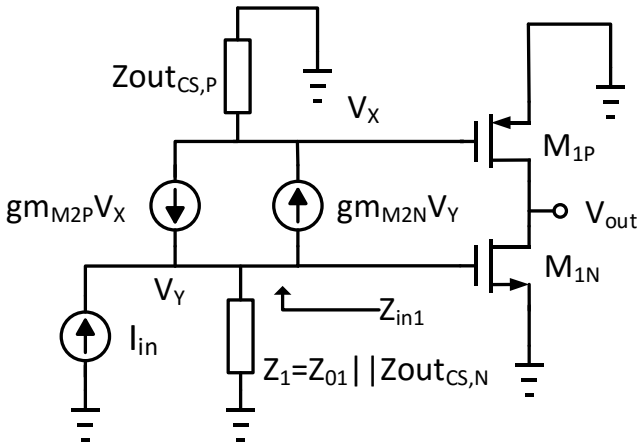

Figure 9 Monticelli small signal equivalent network, adapted from [14]

$$Z_{in1} = 1 + \frac{gm_{M2P}Zout_{CS},P}{gm_{M2N}}$$

$$V_Y = I_{in}(Z_1||Z_{in1}) = \frac{i_{in}Z_1\left(1 + gm_{M2P}Zout_{CS,P}\right)}{1 + gm_{M2P}Zout_{CS,P} + gm_{M2N}Z1}$$

$$V_X = V_Y\left(\frac{Zout_{CS,P}}{Zin1}\right) = I_{in}\frac{Z_1\left(gm_{M2N}Zout_{CS,P}\right)}{1 + gm_{M2P}Zout_{CS,P} + gm_{M2N}Z_1}$$

$$\frac{V_X}{V_Y} = \frac{gm_{M2N}Zout_{CS,P}}{1 + gm_{M2P}Zout_{CS,P}} \quad (2.9)$$

When a large signal is applied at either of the nodes, V_X or V_Y, such as a current that is larger than the bias current is injected, the circuit suffers from distortion. This is because, one of the control transistors, M_{2N} or M_{2P} turns off and all the current is passed through the other. When a positive swing is applied at the source of M_{2P}, such that it turns

off, then M_{2N} conducts all the current. Under this condition, M_{2P} acts merely as a cascade device, and the voltage swing at node V_X gets clipped as shown in Figure 10, [14].

$$V_Y = I_{in}\frac{Z_1\left(gm_{M2P}ro_{,M2P}Zout_{CSP}\right)}{gm_{M2P}ro_{M2,P}Zout_{CS,P} + Z_1}$$

$$V_X = I_{in}\frac{Z_1 Zout_{CSP}}{gm_{M2P}ro_{M2,P}Zout_{CS,P} + Z_1}$$

$$\frac{V_X}{V_Y} = \frac{1}{gm_{M2P}ro_{M2P}} \tag{2.10}$$

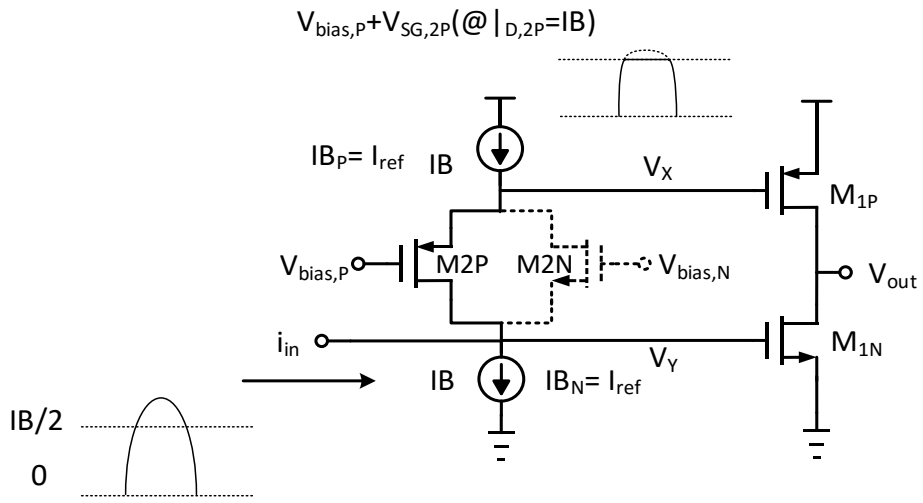

Figure 10 Large signal distortion in the Monticelli scheme (a), adapted from [14]

Similarly, when a large negative signal is applied at the source of M_{2N}, such that the current injected I_{in} is larger than the bias current, IB, the entire current provided by

the top current source is conducted through M_{2N}. M_{2P}, which is now current starved, goes into cut-off. This scenario is pictured in Figure 11.

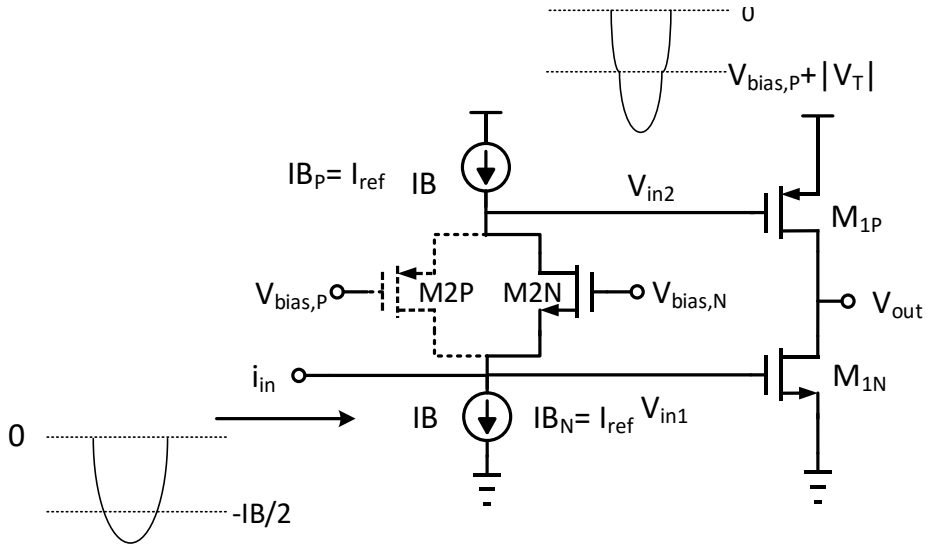

Figure 11 Large signal distortion in the Monticelli scheme (b), adapted from [14]

Now, the M_{2N} transistor simply acts as a common-gate amplifier as the signal is injected at its source. As the voltage swing at V_Y increases further in the negative direction, eventually the transistor M_{2N} enters triode region as its V_{DS} exceeds its overdrive.

$$V_Y = I_{in}\frac{Z_1}{1 + gm_{M2N}Z_1}$$

$$V_X = I_{in}\frac{gm_{M2N}Z_1 Zout_{CSP}}{1 + gm_{M2N}Z_1}$$

$$\frac{V_X}{V_Y} = gm_{M2N}Zout_{CSP} \tag{2.11}$$

The hard discontinuities in the transfer function as evidenced by the above equations causes the earlier mentioned large signal nonlinearity. The transfer function plot below in Figure 12, with the input ac current on the X-axis, illustrates these discontinuities.

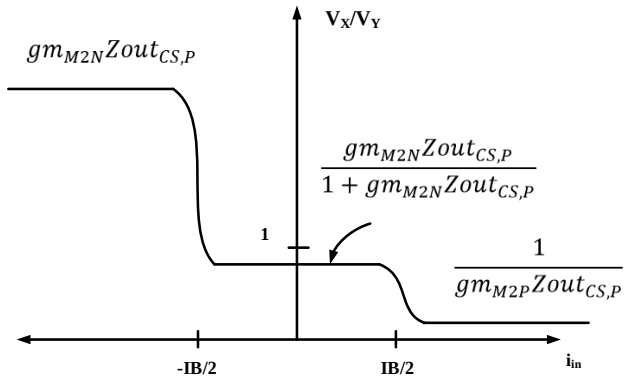

Figure 12 Monticelli transfer function, adapted from [14]

The ideal gain of a level shifter for AC signals should be unity. From the equation above, it is implied that the product, $gm_{M2P}Zout_{CS,P}$ should be much larger than one and that gm_{M2N} should be approximately equal to $gm_{M2P.}$ To maximize the product $gm_{M2P}Zout_{CS,P}$, we can reduce the bias current, as the product is inversely proportional to the square root of the bias current or increase $Zout_{CS,P}$ by cascoding, which would further reduce the headroom available. Reducing the bias current is not a good option since its limit is determined by the peak AC current of the previous stage. Matching the gm_{M2P} and gm_{M2N} quantities are difficult under P.V.T. variations. Thus the level shifter transfer function may never reach unity, which implies that the signal swings at the output stage NMOS and PMOS transistors are unequal. This can introduce nonlinearity in the output stage as the quadratic terms in equation (2.5) do not cancel out.

2.3.2 Implementation of the Monticelli based class-AB amplifier

To understand the working of a level shifter better and its intrinsic nonlinearity, a class-AB amplifier was implemented based on the Monti-celli Level shifter scheme. The schematic of this amplifier is shown in Figure 15.

2.3.2.1 Input stage

The Input stage is a simple differential pair with Local Common Mode Feedback (LCFB) as shown in Figure 13. Since the output of the first stage is a high resistance node, it requires common Mode feedback to define its common mode level under P.V.T. variations. The LCFB circuit consists of using two large resistors (greater than $rds_{M_{P1,2}}$), to define the output common mode levels of the first stage. These resistors are connected between the gate and drain of the PMOS current source transistors. For differential signals, these resistors appear in parallel to the $rds_{MP_{3,4}}$ since the center node, V_z is a virtual ground. For common mode signals they act as a short and the input stage behaves similar to a diode connected differential pair.

The advantage of LCFB, apart from defining the output common mode is that the parasitic capacitances C_{GS} of the current source transistors, $M_{p1,2}$ do not contribute to the total parasitic capacitance of the first stage as the gate node, Vz is an AC ground. This helps improve the frequency response. An additional advantage of this technique is slew rate enhancement [15].

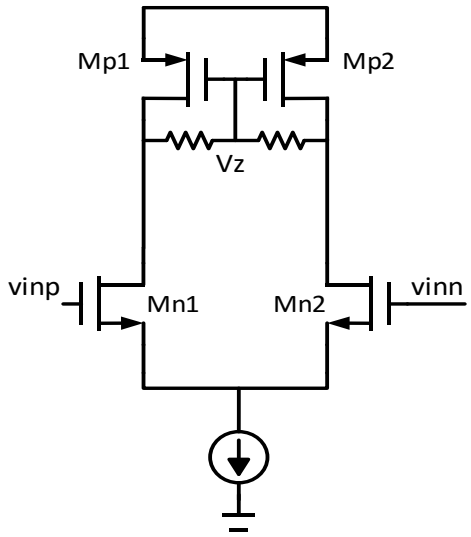

Figure 13 Input stage

2.3.2.2 Monti Celli level shifter implementation

In the design depicted in Figure 14, the Monticelli Level shifter is implemented with the output of the first stage connected to the PMOS source transistor, M_{P8} . The total output resistance at the first stage is given by the contributions of the first stage r_{ds} and the top current source of the Monticelli stage, M_{p4}.

The local common mode feedback resistor's contribution is neglected as it is large.

$$Rout_1 = r_{ds,n2} \left|\left| r_{ds,p2} \right|\right| r_{ds,p4}$$

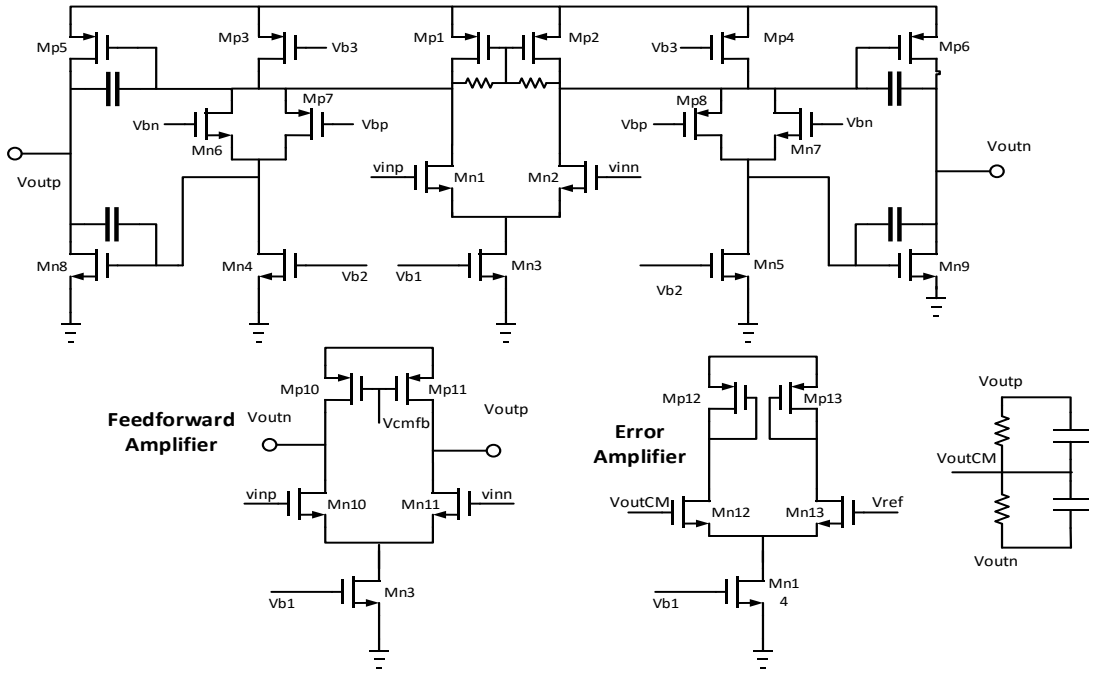

Figure 14 Class-AB implementation using Monticelli bias scheme

Gain of the first stage $= gm1Rout1$

It is observed in our design that the gain of the first stage is relatively low, as the output resistance is degraded by the parallel combination of several resistances.

2.4 Feedforward compensation

A feedforward compensation scheme is more efficient than the traditional Miller compensation scheme which requires higher power for the same Gain Bandwidth product (GBW). This is because the feedforward compensation scheme does not move the dominant pole towards the origin unlike, the Miller compensation scheme that splits the

poles and reduces the w_{3dB} bandwidth of the opamp. Another disadvantage of the Miller compensation scheme is the existence of a RHP zero which needs to be cancelled using a nulling resistor [16].

The basic principle of the feedforward compensation scheme is to introduce an LHP zero through an additional path, and use its positive phase shift to compensate for the negative phase shift produced by the two dominant poles of the amplifier [17].

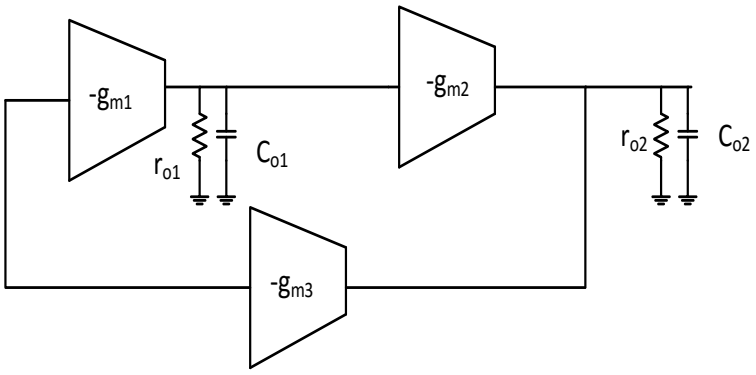

Figure 15 Feedforward compensation

Figure 15 shows the block diagram of the feedforward compensation scheme. The transfer function is given by

$$\frac{Vout(s)}{Vin(s)} = \frac{(A_{v1}A_{v2} + A_{v3})\left(1 + \frac{A_{v3}s}{(A_{v1}A_{v2} + A_{v3})w_{p1}}\right)}{\left(1 + \frac{s}{w_{p1}}\right)\left(1 + \frac{s}{w_{p2}}\right)} \qquad (2.12)$$

Here A_{v1}, A_{v2}, A_{v3} are the low-frequency gains of the first stage, second stage and the feedforward stage are given by

$$A_{v1} = -gm_1 ro_1$$

$$A_{v2} = -gm_2 ro_2$$

$$A_{v3} = -gm_3 ro_3$$

w_{p1} is the pole at the output of the first stage and is given by $\frac{1}{\mathrm{ro_1 C_{01}}}$ while w_{p2} is the shared pole of the second and third stage and is given by $\frac{1}{\mathrm{ro_2 C_{02}}}$

The feedforward stage introduces a zero which is given by:

$$z_k = \left(1 + \frac{A_{v1}A_{v2}}{A_{v3}}\right) w_{p1} \tag{2.13}$$

A perfect cancellation of the non-dominant pole using the zero would attain single stage opamp frequency response. However, in the presence of imperfect cancellation, a pole-zero doublet is formed [18] which can dominate the settling time. Hence the poles and zeroes needs to be placed carefully in order to attain a fast transient response.

$$1/(ro_2 Co_2) = -\left(1 + \frac{A_{v1}A_{v2}}{A_{v3}}\right) w_{p1} \tag{2.14}$$

The basic assumption behind the feedforward compensation is that the first stage output pole is dominant. In [17], the first stage gain is kept high by using a telescopic cascade. However, in our design, since the first stage output resistance is comparatively low, the pole at the output of the first stage output is nondominant. A simple solution to

this problem is to connect a small Miller capacitor (50fF) between the first stage and the second stage output node. The purpose of this capacitor is to bring the first stage output pole to a lower frequency, making it dominant. Since the capacitor is very small, pole splitting occurs to a very small degree. It was also observed that the RHP zero does not appear before the GBW. Figure 16 shows the closed loop simulation test bench for the amplifier.

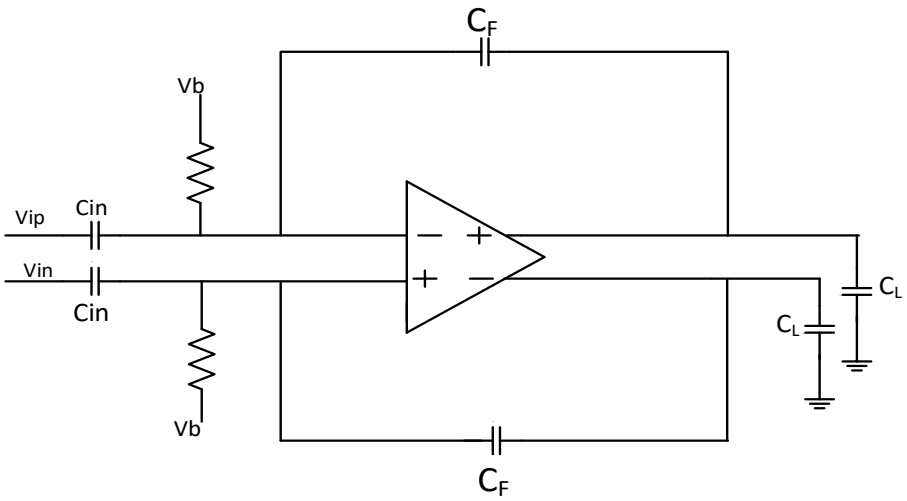

Figure 16 Closed loop simulation test bench

2.5. Proposed class-AB output stage

We first examine the benefits and drawbacks of a source-follower level shifter as shown in Figure 17 [9]. The source follower shifts the DC level between its input and output by its gate to source voltage, V_{gs}. The V_{gs} drop provided by the source follower acts as the necessary level DC shift which can be set using a bias current source as follows,

For large-signals, $V_i = V_o + V_{gs} = V_o + V_t + V_{dsat}$

$$V_{gs} = V_t + \sqrt{\frac{2I_b}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} \tag{2.14}$$

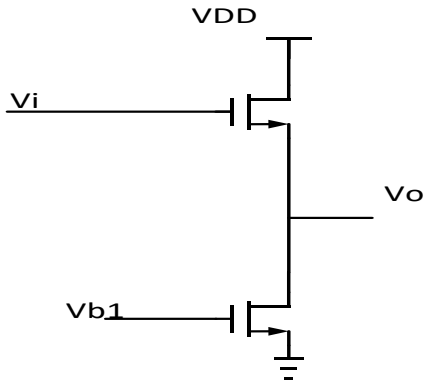

Figure 17 Source follower

For AC signals, the gain of this level shifter is given by,

$$V_{o=}\frac{g_{ds}}{g_{ds}+\frac{1}{gm}}V_i \tag{2.15}$$

where $g_{ds} = g_{ds1} + g_{ds2} = \left(\frac{1}{ro_1}\right) + \left(\frac{1}{ro_2}\right)$

As seen in the above equation, the AC gain of this level shifter is close to unity, which is the case when g_{ds} is much larger compared to $\frac{1}{\text{gm}}$.

The problem with this simple level shifter is that, the quantity V_{gs} is susceptible to variations across process corners and temperatures which makes the level shift value

subject to P.V.T variations. V_{gs} is directly dependent on V_T which is a function of temperature and process parameters as seen in Figure 18.

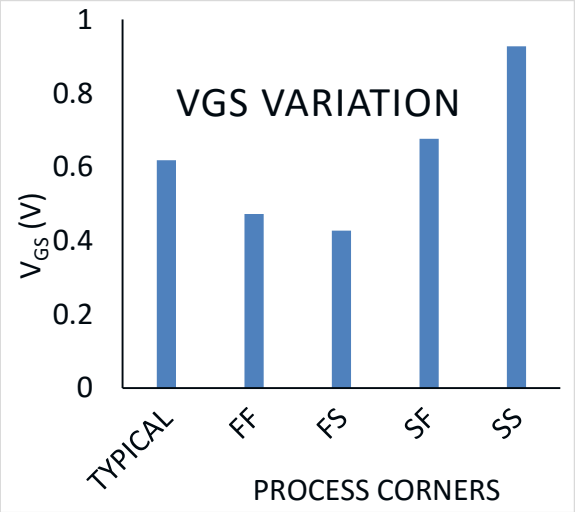

Figure 18 V_{GS} variation under corners

To compensate for these variations, a negative feedback loop needs to be implemented. A common mode feedback loop can serve this function, in addition to setting the output common voltage for the fully differential output stage.

The role of the CMFB loop here is to make sure that the DC bias conditions of the NMOS and PMOS transistors of the output stage is set such that the output currents are balanced. This is done by measuring the output common mode and comparing with a reference voltage. The error is suppressed by the loop.

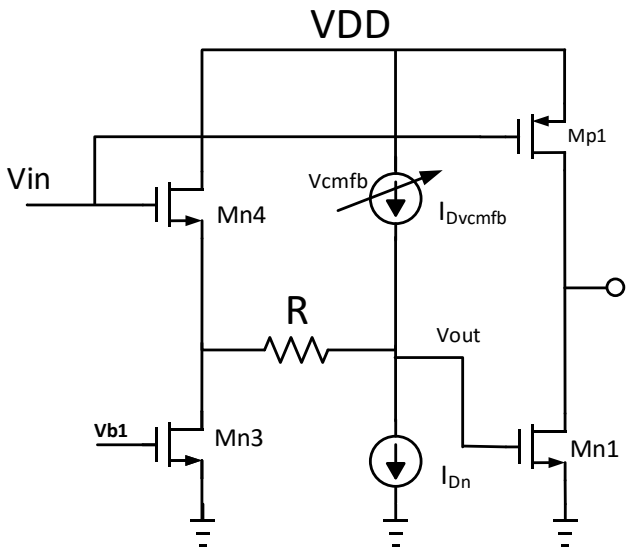

Figure 19 Proposed level shifter

To ensure that the DC level shift is compensated for any variations, it is necessary to introduce a variable DC drop in addition to the fixed drop provided by the source follower. The drop is provided by introducing a variable current which is controlled by the CMFB loop, across a small resistor as shown in Figure 19. Thus the total level shift can be visualized as large or coarse voltage drop along with a smaller or finer drop that can be tuned by the loop. The amount of tuning that can be achieved or the variation that can be suppressed depends on the gain of the loop.

The variable current source is implemented using a PMOS transistor whose gate node is controlled by the error amplifier output voltage. This implies that the dc drop across the resistor is always positive; the tuning can only compensate for a source follower V_{GS} that is smaller than its typical corner or room temperature value. This means that we

wouldn't be able to compensate for a process corner variation where the source follower V_{GS} is higher than the nominal value.

A simple solution to this problem is to have a fixed current sink, I_{DN} as shown in Figure 19.

The nodal equations for the Level shifter are given by,

$$V_{in} = V_{gs} + \frac{V_x - V_{out}}{R}$$

$$\frac{V_x - V_{out}}{R} = I_{Dvctrl} - I_{Dn}$$

$$\frac{V_x - V_{out}}{R} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{DD} - Vctrl - |V_{Tp}|\right)^2 - \frac{1}{2}\mu_n C_{ox}(V_b - V_{Tn})^2 \quad (2.16)$$

where V_{ctrl} is the control voltage of the common mode feedback loop.

This can be simplified to

$$V_{in} - Vout = \quad V_{gs} \quad + [I_{Dvctrl} - I_{Dn}]R$$

The working of the loop can be explained as below under various P.V.T. conditions

At typical condition, sizes are adjusted such that $I_{Dvctrl} = I_{Dn}$

1) Negative V_{gs} variation under P.V.T.

   The loop adjusts the V_{ctrl} so that I_{Dvctrl} exceeds I_{Dn} and Vin-Vout remains constant.

2) Positive V_{gs} variation under P.V.T.

The loop adjusts the V_{ctrl} so that I_{Dvctrl} becomes lesser than I_{Dn} and V_{in}-V_{out} remains constant. In the extreme case, I_{Dvctrl} becomes zero and the maximum drop becomes equal to$-I_{Dn}R$.

The drawback of this method of tuning is that the amount of process variation tolerable depends on the magnitude of $[I_{Dvctrl} - I_{Dn}]R$. The product should be maximized to be able to accommodate the full range of expected P.V.T. variations. There are two ways to do this, increase I_{Dvctrl} and I_{Dn} or increase resistance.

There is a tradeoff here. It may appear that increasing the resistance, R is better than increasing the currents which would increase the power. However, the resistance along with the parasitic capacitances at that node contributes towards a pole which can attenuate the AC signal flowing into the NMOS gate at high frequencies as shown in Figure 20. This results in unequal signal swings at the NMOS and PMOS gates and can contribute towards nonlinearity as mentioned earlier. To push the pole to very high frequencies, it is necessary to reduce the value of R and instead increase the bias current towards the extent possible without increasing power consumption more than the budgeted amount.

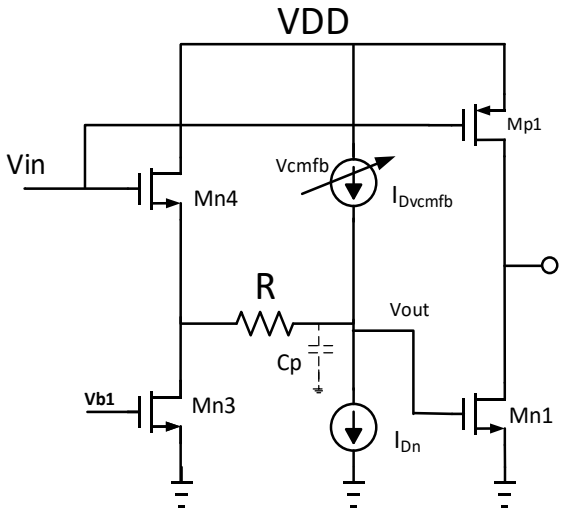

Figure 20 Parasitic pole in the proposed level shifter

These factors, R and the bias currents also determine the CMFB loop gain. The CMFB loop should have a large gain to suppress the variations in common mode. However being a negative feedback loop, its stability also needs to be considered.

The CMFB loop gain is given by

$$\text{Gain} = -A_2 * A_v * gm_{vctrl} * Ro_{Ls}$$

where Ro_{LS} is the impedance at the NMOS gate node shown in Figure 21.It is given by

$$Ro_{LS} = Z_1 || (R + Z_2)$$

$$Z_1 = ro_{vctrl} || ro_n$$

$$Z_2 = \frac{1}{gm} || ro_2 || ro_3$$

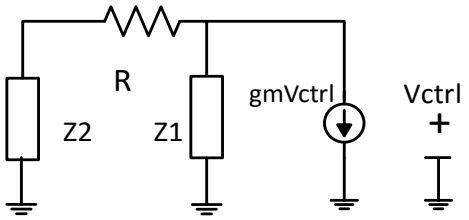

Figure 21 Impedance seen at the NMOS gate node of the proposed level shifter

Since R is chosen much smaller than the transistor r_{ds}, it dominates the net impedance. The loop has two dominant poles, the output stage pole which lies at low frequency and the pole at the NMOS gate terminal. It must be ensured that the pole at the NMOS gate lies at a sufficient high frequency so that the loop is stable.

The error amplifier is implemented using a simple diode connected differential pair. Since the loop already has sufficient gain, it is not necessary to implement a high gain error amplifier, which would create an additional pole. Further having a high bandwidth error amplifier is desirable to enable the CMFB loop to react to fast differential inputs.

This level shifter suffers from the drawback of having a gain slightly less than unity for AC signals. Since the source follower implemented suffers from body effect, it is not possible to realize a unity transfer function even with ideal transistors.

This drawback needs to be addressed by sizing the output stage NMOS transistor accordingly to increase its gm.

The AC current conducted by the NMOS and PMOS transistors in the output stage are given by

$$i_{dn} = gm_n v_{gsn} = i_{dp} = gm_p v_{gsp}$$

Since $v_{gsn} < v_{gsp}$, it is necessary to size the output stage transistors such that $gm_n > gm_p$.

2.6 Improved input stage

In the input stage used in the Monticelli based class-AB amplifier, it was observed that the AC gain is comparatively small due to the effect of the low gds of the input NMOS transistor. As the input transistor is optimized to achieve high GBW, its drain resistance suffers which limits the overall stage gain. It is always desirable to obtain large gain in the first stage of the opamp and high swing in the second stage. Having a small output resistance for the first stage could push its pole to a higher frequency than the output stage pole. To rectify this issue, it is necessary to increase the output resistance of the first stage without cascoding.

We utilize a negative resistance [19] to cancel out the smaller value of the NMOS resistance and improve the overall first stage output resistance. The negative impedance that is realized under the configuration in Figure 22 is a function of $\frac{N}{gm_p}$ where N is a factor dependent on the values of R1, R2 and R3. This negative resistance can be used to cancel out the NMOS transistor's gds and enhance the net output impedance.

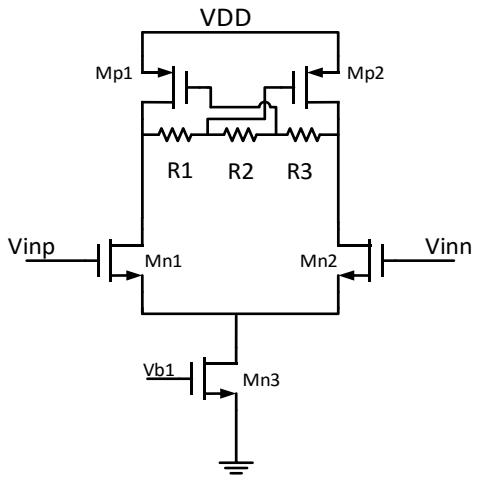

Figure 22 Proposed input stage

Table 1 Device dimensions

Device	Dimensions	Device	Dimensions
Mn1	6u/0.18u	Mp3	24u/0.18u
Mn2	54u/0.4u	Mp4	4u/0.18u
Mn3	8u/0.18u	IB1	300u
Mn4	12u/0.18u	IB2	140u
Mp1	24u/0.18u	IB3	300u
Mp2	8u/0.18u	IB4	300u

An amplifier was designed based on the class-AB output stage just described as shown in Figure 23. Table 1 displays all the device dimensions.

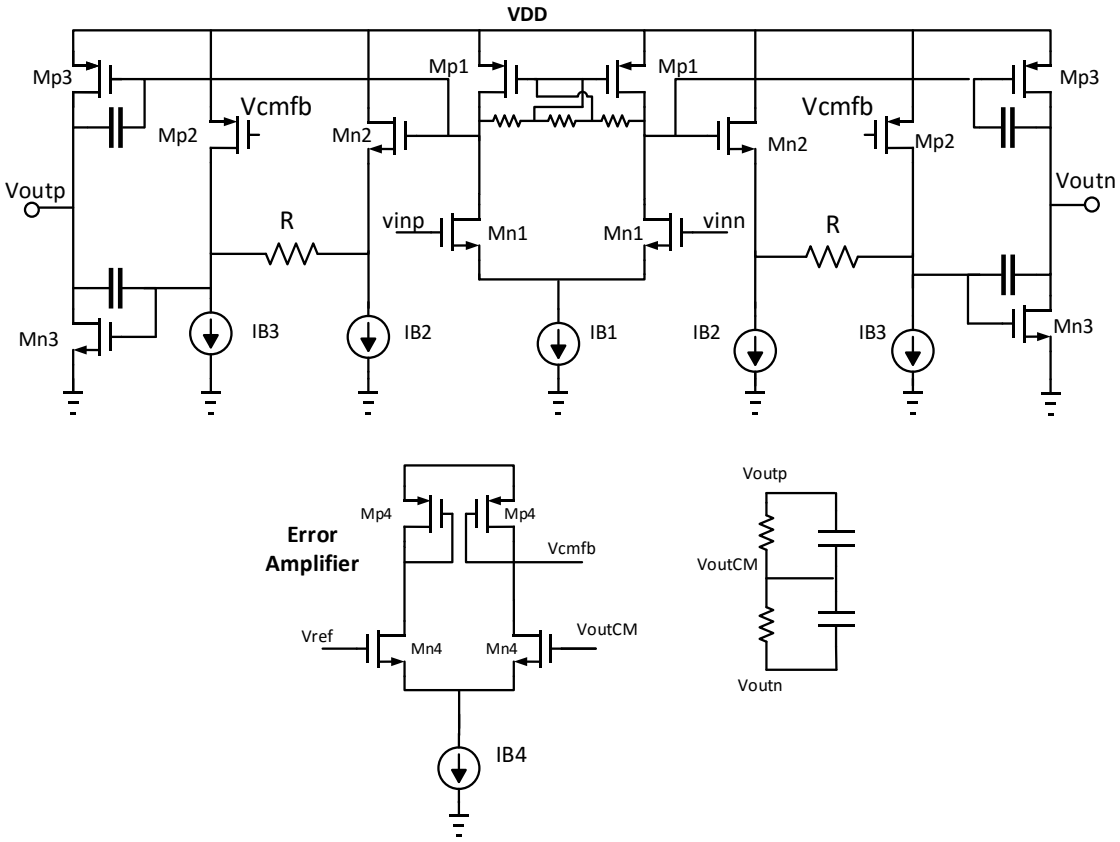

Figure 23 Class-AB amplifier based on the proposed level shifter and improved input stage

3. CLASS-AB NONLINEARITY

3.1 Distortion

Distortion or nonlinearity can be defined as the deviation of the output waveform from a desired linear characteristic. Soft nonlinearity occurs when the signal is small and the deviation is not too large. An amplifier in closed loop that produces distorted square waveforms under ideal square wave input, can be considering as suffering from soft-nonlinearity [20]. An example of hard nonlinearity is the amplifier suffering from slew rate limitations. In this scenario, an amplifier subjected to an input sinusoid whose frequency is so high that the amplifier cannot track its changes starts changing it output at a constant rate. Another example of hard nonlinearity is the transistor turning off when the signal swing is larger than it's V_{DSAT}.

In general, the nonlinearity of an amplifier [21] can be expressed as

$$V_o = A_{nl}V_i = a_0 + a_1V_i + a_2V_i^2 + a_3V_i^3 + \cdots \quad (3.1)$$

The coefficient a_0 represents the DC component of the output signal, V_0, a_1 represents the linear gain of the amplifier, a_2, a_3,.., represents the nonlinear components of the open loop gain of the amplifier.

Supposed V_i is a pure sinusoidal tone, given by $V_i = V\cos(wt)$, then

The output voltage can be expressed as

$$V_o = u_0 + u_1\cos(wt) + u_2\cos(2wt) + u_3\cos(3wt) \quad (3.2)$$

The terms u_0, u_1, u_2, u_3 are given by

$$u_0 = a_0 + \frac{a_2}{2}V^2$$

$$u_1 = a_1 V_i + \frac{3}{4}a_3 V^3$$

$$u_2 = \frac{a_2}{2}V^2$$

$$u_3 = \frac{a_3}{4}V^3$$

$$HD_2 = \frac{u_2}{u_1} = \frac{1a_2}{2a_1^2}V$$

$$HD_3 = \frac{1a_3}{4a_1}V^2$$

The IM3 is another metric used for measuring distortion, which is defined as the ratio of the third harmonic component at the output normalized to the fundamental component. As the system is fully differential, the second harmonic component is cancelled and the third harmonic component is the primary factor contributing towards the distortion. An advantage of the IM3 metric over the HD3 is that it characterizes distortion at the frequency of operation while the HD3 metric measures the third harmonic component at three times the fundamental frequency, which could artificially yield a good value due to high frequency attenuation.

In the following analysis, a relation between the closed loop IM3 and open loop IM3 is determined. Higher order terms are neglected for ease of analysis.

The closed loop gain of the amplifier in feedback can be represented as,

$$\frac{Vo}{Vin} = \frac{A}{1 + A\beta}$$

where β is the feedback factor,

$$\beta = \frac{Z_1}{Z_1 + Z_f}$$

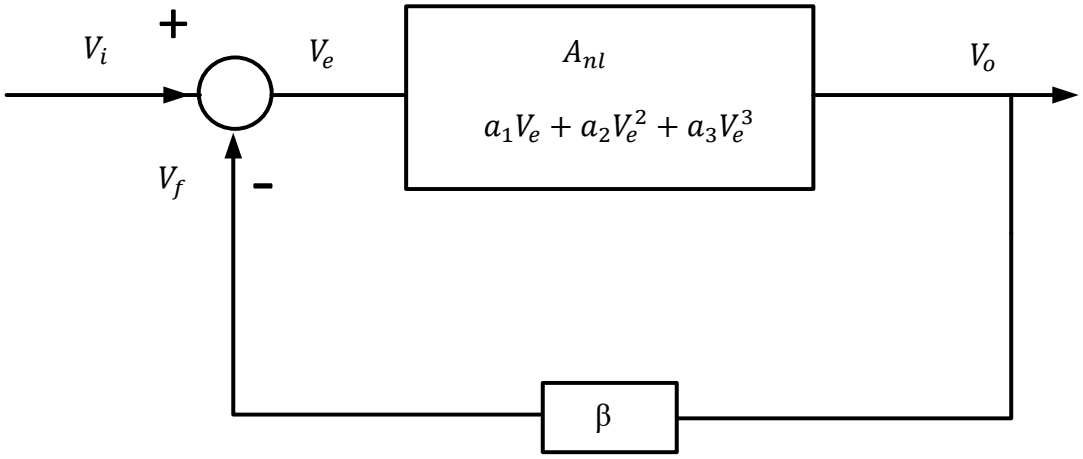

Figure 24 Amplifier in feedback, adapted from [22]

The nonlinearity of the closed loop amplifier, shown in Figure 24, can be expressed as,

$$V_o = a_1V_e + a_2V_e^2 + a_3V_e^3$$

The output signal can be expressed in terms of the input V_i as

$$V_o = b_1V_i + b_2V_i^2 + b_3V_i^3$$

The coefficients b_1, b_2 and b_3 that are obtained from [21] are given by,

$$b_1 = \frac{a_1}{1 + A\beta}$$

$$b_2 = \frac{a_2}{(1 + A\beta)^3}$$

$$b_3 = \frac{a_3(a + A\beta) - 2a_2^2\beta}{(1 + A\beta)^5}$$

Assuming that $2a_2^2\beta << a_3(a + A\beta)$, then we can rewrite the above equation as

$$b_3 = \frac{a_3}{(1 + A\beta)^4}$$

The expression for the IM3 of the amplifier in closed loop, from [23], is given by

$$\text{IM3} = \frac{3}{4}\frac{b_3}{b_1}V_i^2$$

$$\text{IM3} = \frac{\frac{3}{4}\frac{a_3}{a_1}V_i^2}{(1 + A\beta)^3}$$

Thus in general, we can generalize a relation between the closed loop IM3 and the open loop IM3 by,

$$\text{Closed Loop IM3} = \frac{\text{Open loop IM3}}{(1 + \text{Loop gain})^3} \tag{3.3}$$

3.2. Class-AB output stage nonlinearity

The ideal class-AB stage generates only second order nonlinearity as can be observed in equation (2.5). However the effect of channel length modulation, dependence of the mobility, μ, on the vertical and horizontal electric fields and various other second order effects generate higher order distortion terms. Generally, the main sources of nonlinearity in the output stage are the nonlinear transconductance (gm) and the nonlinear output resistance. The main scope of this work is the characterization and measurement of the transconductance nonlinearity.

Assuming the signal is not too large, and ignoring the effect of the nonlinearities from the parasitic capacitors and output resistances, the drain current of a MOS transistor can be expressed as

$$i_D = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \ldots\ldots\ldots\ldots \tag{3.4}$$

where g_i is the t^{th} – order distortion coefficient of the transistor obtained by differentiating the drain current i_D with respect to the gate-source voltage v_{gs} at the quiescent condition [24]. The coefficient of v_{gs} which is termed the gm, corresponds to the small signal transconductance.

$$g_1 = \left(\frac{\partial i_D}{\partial v_{gs}}\right)_Q, \qquad g_2 = \left(\frac{\partial^2 i_D}{2!\,\partial v_{gs}^2}\right)_Q, \qquad g_3 = \left(\frac{\partial^3 i_D}{3!\partial v_{gs}^3}\right)_Q$$

For the ideal class-AB output stage shown in Figure 25,

$$i_{OUT} = i_P - i_N$$

$$= (g_{1P} v_{sg} + g_{2P} v_{sg}^2 + g_{3P} v_{sg}^3 + \cdots \ldots\ldots) - (g_{1N} v_{gs} + g_{2N} v_{gs}^2 + g_{3N} v_{gs}^3 + \cdots)$$

$$=(g_{1N} + g_{1P}) v_{gs} + (g_{2N} - g_{2P}) v_{gs}^2 + (g_{3N} + g_{3P}) v_{gs}^3 + \cdots \ldots\ldots\ldots$$

$$i_{OUT} = g_{1out} v_{gs} + g_{2out} v_{gs}^2 + g_{3out} v_{gs}^3 + \cdots \ldots\ldots\ldots\ldots \tag{3.5}$$

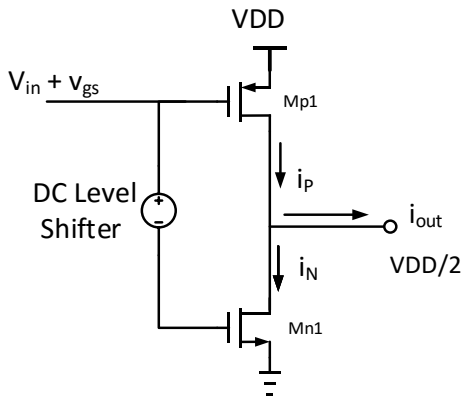

Figure 25 Ideal class-AB output stage

where g_{iout} is the i[th]- order distortion coefficient of the output stage obtained by differentiating the output current i_D with respect to the gate-source voltage v_{gs} at the quiescent condition and g_{iP} and g_{iN} correspond to the distortion coefficients for the PMOS and NMOS transistors.

For the square law current equation model, assuming that the NMOS and PMOS parameters are perfectly matched ($K_n = K_p$ and $V_{DSAT,N} = V_{DSAT,P}$) and the signal does not exceed the V_{DSAT} of either transistor, these higher order coefficients can be neglected and the output current can be reduced to equation (2.5) as described in the previous section.

If $K_n = K_p$ and $V_{DSAT,N} = V_{DSAT,P}$

$$i_{OUT} = -4KV_{DSAT}v_{in} \quad ; \text{for } -V_{DSAT,N} < v_{in} < V_{DSAT,P} \tag{3.6}$$

In Figure 26, the currents in the class-AB output stage are plotted against the $v_{gs,}$ the small signal input. It can be seen that the bias currents are very small compared to the peak AC currents, demonstrating the class-AB operation. Further the output current is

much more linear compared to the NMOS and PMOS currents. In this characterization, the drain terminal of the NMOS and PMOS transistors are fixed at $\frac{VDD}{2}$

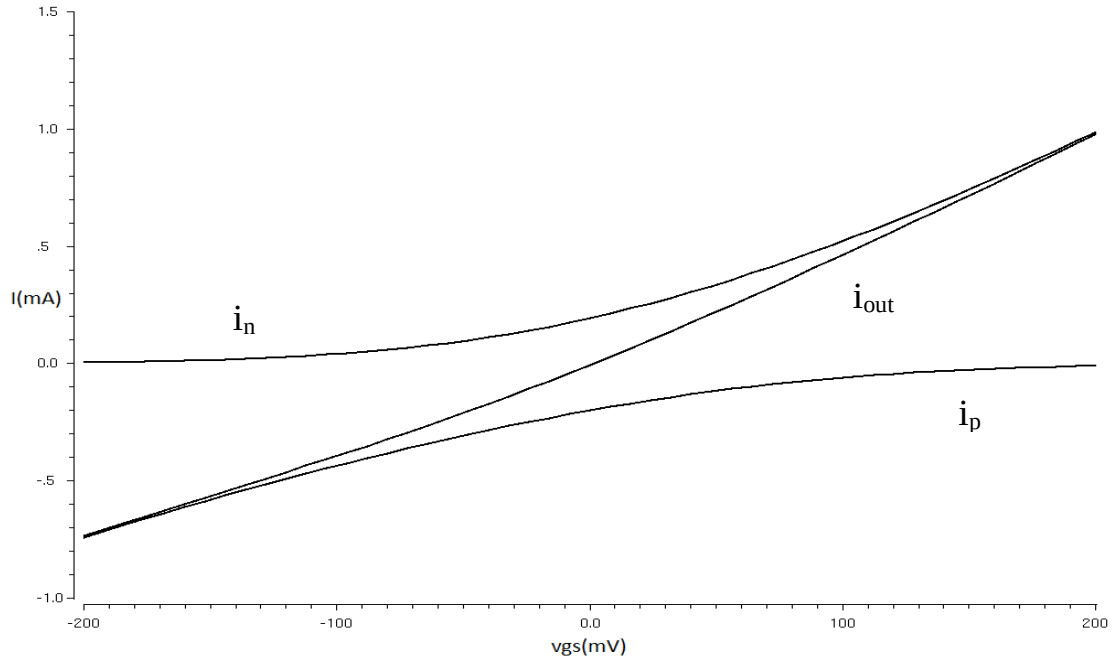

Figure 26 Class-AB output stage currents

as we are interested in the output current.

Figures 27-29 show the NMOS, PMOS and Output Gm variation against the input v_{gs}. In these plots, the three regions of class-AB operation can be observed. In region (1), the signal is smaller than either of the NMOS or PMOS V_{DSAT}, both the NMOS and PMOS transistors contribute towards the total Gm. In region (2), the PMOS Gm is very small as the signal swing is large in the positive direction and the NMOS transistor has a greater contribution towards the total Gm. Further increase in the signal can turn off the PMOS

transistor. Finally, in region (3), the PMOS transistor Gm is much larger than the NMOS Gm.

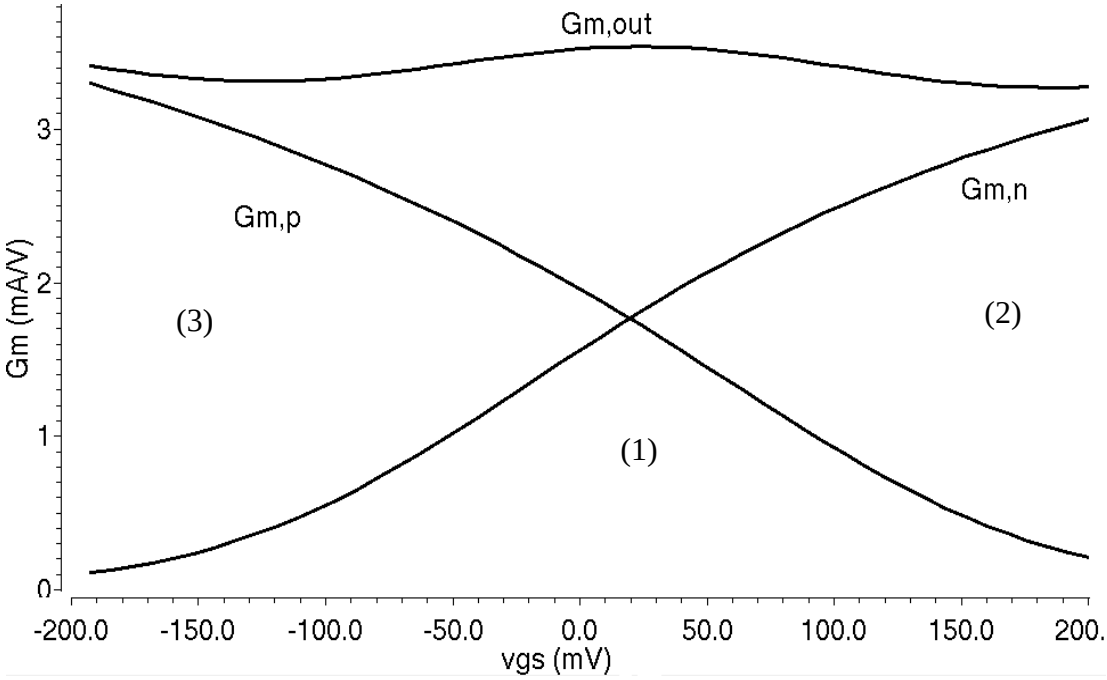

Figure 27 Gm vs vgs when NMOS and PMOS are matched

In Figure 27, it can be seen that the total Gm is constant. This is due to the good matching of NMOS AND PMOS parameters.

Under the matched condition, from equation (3.6),

$$i_{OUT} = -4KV_{DSAT}v_{in} \qquad ; \text{for } -V_{DSAT,N} < v_{in} < V_{DSAT,P}$$

Since ,

$$Gm_{out} = \frac{\partial i_{out}}{\partial V_{in}}$$

$$Gm_{out} = -4KV_{DSAT} \tag{3.7}$$

which is a constant independent of the input signal. In Figures 28 and 29, however the total Gm is not constant due to improper matching between the NMOS and PMOS transistor properties. In Figure 28 the NMOS Gm is more dominant than the PMOS Gm whereas in Figure 29, the PMOS Gm dominates over the NMOS Gm.

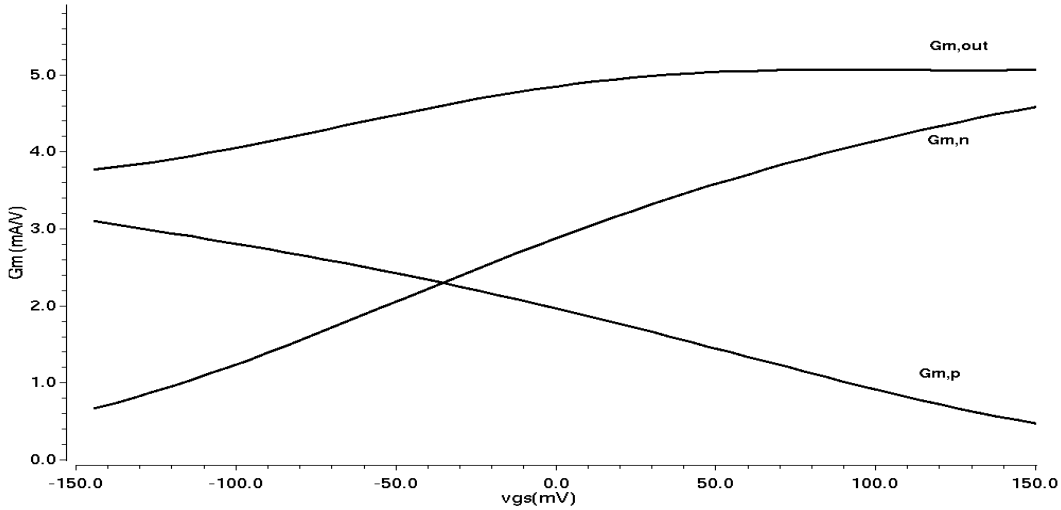

Figure 28 Gm vs vgs when NMOS is dominant over the PMOS

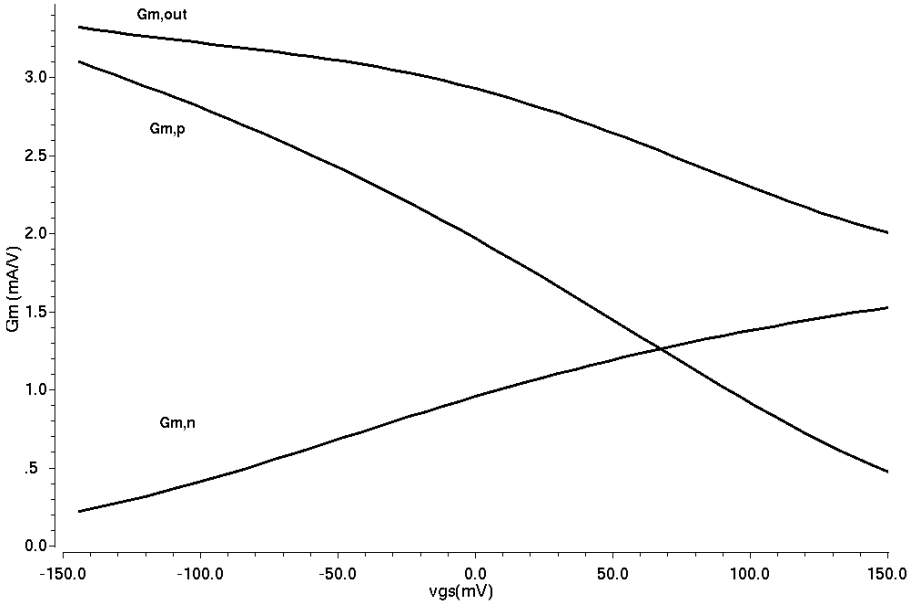

Figure 29 Gm vs vgs when PMOS is dominant over the NMOS

3.3. Gm nonlinearity cancellation procedure

We are primarily interested in the distortion arising in the output stage. It is proposed that with good matching, the output Gm can be made constant or a linear function of the input signal, which would cancel or reduce the third harmonic component, g_3. The second harmonic component is cancelled out inherently by having fully differential operation. We perform a characterization to understand for what particular output stage transistor properites the Gm is flat as shown in Figure 30.The PMOS size is fixed and the output transconductance is plotted against the input v_{gs} for various NMOS sizes. Since the parameter K_n is directly related to the size of the NMOS transistor, for a

particular size we can match the NMOS K_n with the PMOS K_p, resulting in lower distortion.

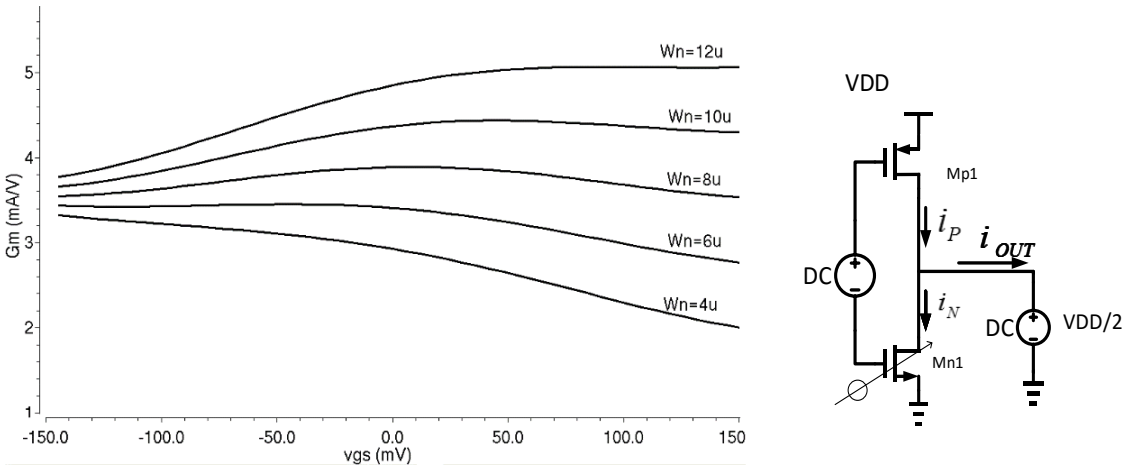

Figure 30 (a) Gm vs vgs with NMOS size as parameter (b) Test bench for characterization: the size of the PMOS transistor, Mp1 is fixed and the size of the NMOS transistor, Mn1 is swept as a parameter.

Figure 30(a) shows the output Gm plotted for various NMOS sizes with a fixed PMOS size as depicted in Figure 30(b). It can be seen that the output Gm is approximately constant for the case of NMOS size, Wn = 8u for the PMOS size, Wn= 24u. Both the transistors are biased with a quiescent current of 200uA with a V_{DSAT} of 130mV.

To verify the claim that the linearity is improved through matching the NMOS and PMOS paramters, we again characterize the Gm for a fully differential ideal class-AB stage shown in Figure 31 using the same procedure . It is important that the circuit is differential, to cancel out the second order nonlinearity. Common mode feedback is implemented so that the output common mode voltage is fixed by a reference. Here we

implemented ideal Common Mode feedback using a voltage controlled voltage source as error amplifier.

The common mode sensing resistors, Rcm here are very small (100 Ohm) so that the output impedance nonlinearity effects are ignored temporarily. These sensing resistors do not affect the common mode gain.

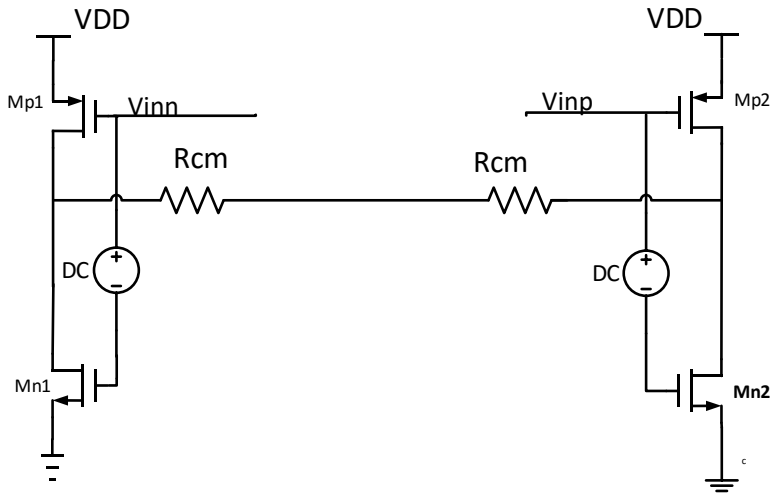

Figure 31 Differential ideal class-AB output stage

Figure 32 shows the total Gm variation plotted against the input differential signal,vgs for various NMOS sizes. It is observed that the Gm plots are symmetrical due to the differential nature of the circuit. The output Gm variation with the input differential signal is lowest for the case Wn = 5u which is the optimal condition expected to give the best linearity. The linearity is characterized by measuring the IM3 using a two-tone test at 10MHz frequency. Figure 33 shows the results of the two tone test for the differential class-AB output stage. It shows the plots of the IM3 vs the NMOS size, Wn (u) for

different input amplitudes. It can be seen that the linearity is significantly improved for Wn=5u, agreeing with the Gm characterization in the previous Figure.

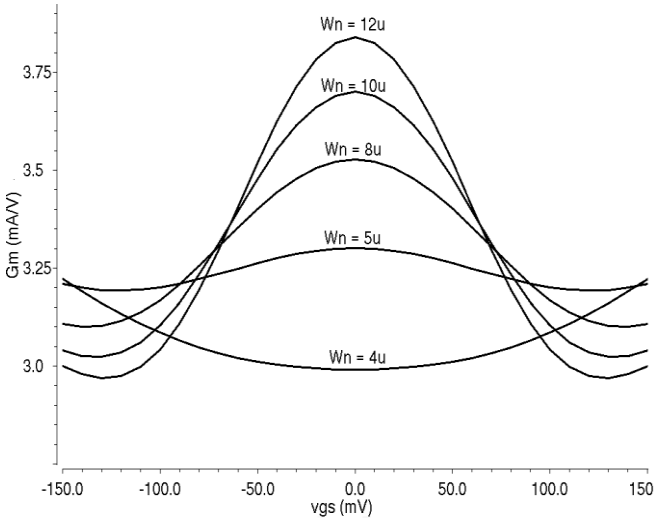

Figure 32 Gm vs differential input

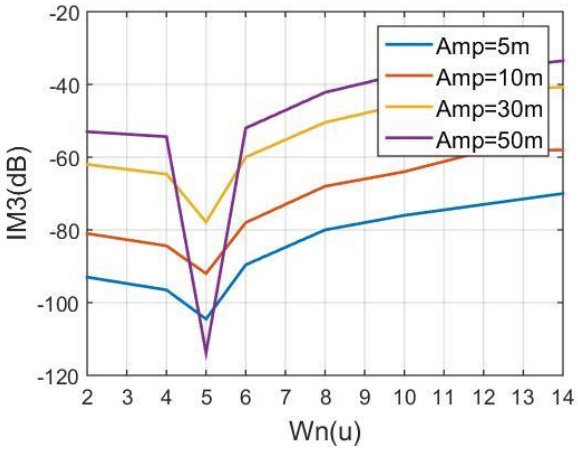

Figure 33 IM3 vs NMOS Size

3.3.1 Amplifier Gm characterizations neglecting effect of output resistance

In the next step, the same characterization was repeated for the complete two stage class-AB amplifier described in the last section. Initially we perform the characterization with a small output resistance to neglect the effects of the transistor output resistance (r_{ds}) nonlinearity. Further the assumption here is that the input stage is linear and the characterization is done to improve the linearity of just the output stage.

Generally, for two-stage amplifiers, the output stage linearity determines the total linearity [25].

$$\frac{1}{IIP3} = \frac{1}{IIP3_{,1}} + \frac{A_{v1}}{IIP3_{,2}} \tag{3.8}$$

where $IIP3_{,1}$ and $IIP3_{,2}$ are the input referred intercept points of the first and second stage respectively and A_{v1} is the gain of the first stage. Since the IIP3 of the second stage is scaled by its gain, the nonlinearity of the second stage becomes more critical.

To measure the Gm, a small AC signal, was applied across the inputs, as shown in Figure 34. The ratio of change in the output current by the input signal swing gives the total Gm of the amplifier. The current is measured across the common mode sensing resistors, Rcm. To neglect the effects of the output resistance, small common mode sensing resistors were used (Rcm = 100). Figure 35 shows the class-AB output stage currents. To obtain the Gm vs differential input plot in Figure 36, a differential ramp was generated at the input of the amplifier by sweeping the DC parameter vdiff $= V_{inp} - V_{in}$

over the desired input range [-10m, 10m] and the small signal Gm was plotted along the Y-axis. The choice of the input range was made such that the output current exceeds the bias current by 2-3 times for the peak vdiff value. A second criteria is that the output swing should not be too large so that the output stage transistors go into triode region.

The output Gm plots show that the optimal size for which the output stage NMOS and PMOS properties are matched is Wn=11u.

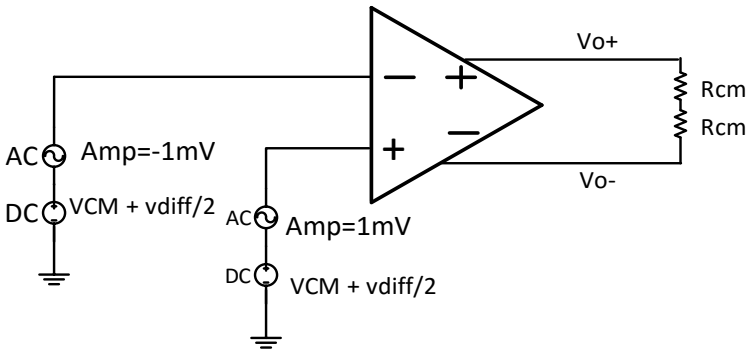

Figure 34 Test bench for Gm characterization

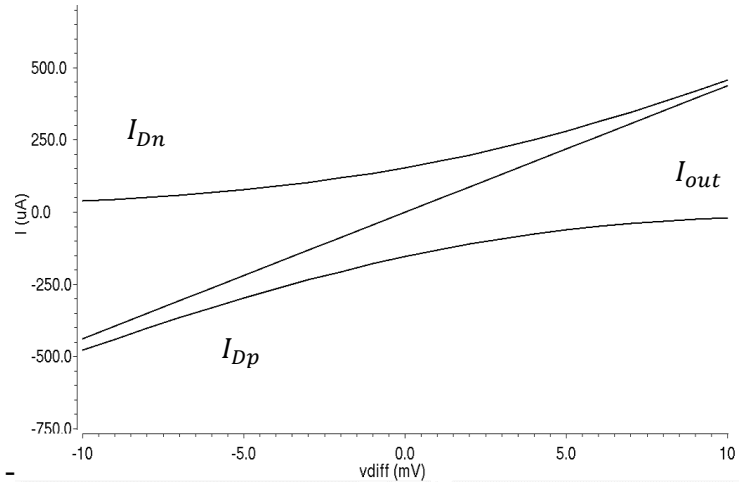

Figure 35 Currents in class-AB output stage

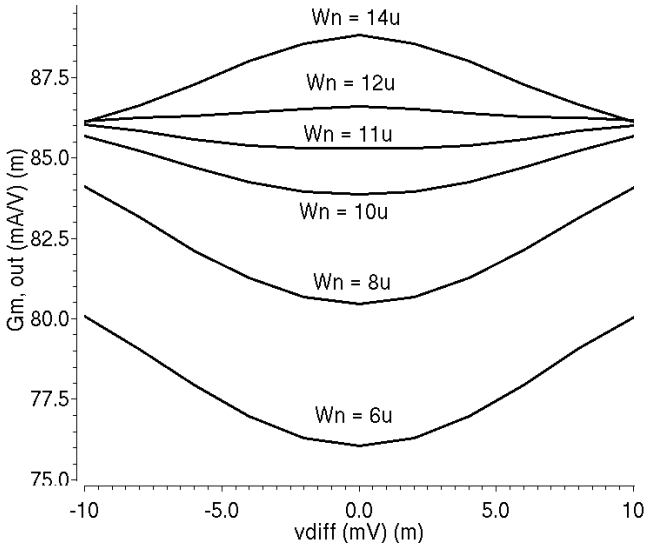

Figure 36 Gm vs differential input for Rcm = 100 Ohm

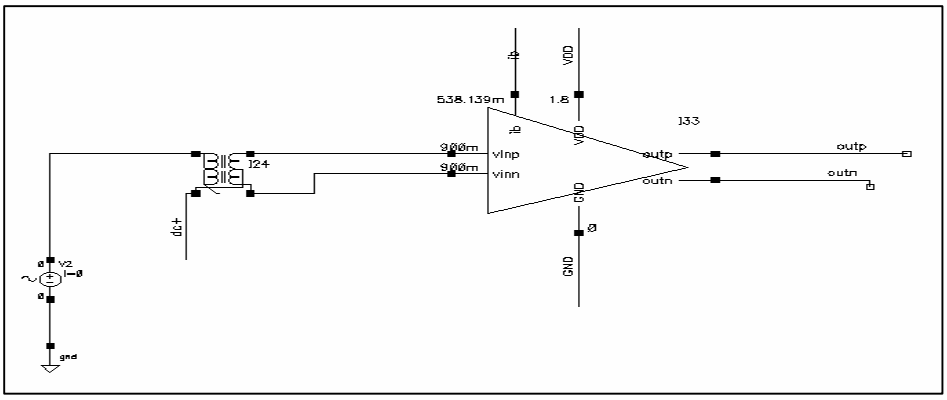

Figure 37 Test bench for characterizing IM3

Figure 38 shows the closed loop IM3 plotted against the NMOS size, for different input signal amplitudes. The open loop characterization test bench is shown in Figure 37. It can be observed that the IM3 has a local minima for Wn=11u, which is the size for which the Gm is constant over the input range as seen in Figure 36, for small amplitudes.

As the amplitude increases, large signal distortion dominates the linearity and we do not achieve the optimal linearity condition.

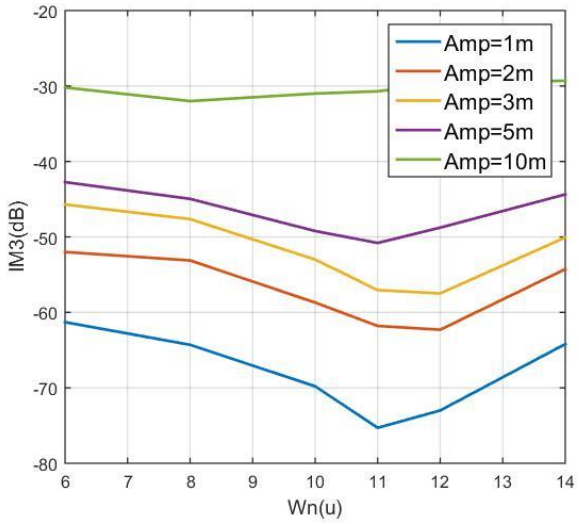

Figure 38 IM3 vs NMOS size for Rcm =100 Ohm

3.3.2 Effect of output resistance

As the amplifier in a real application cannot be loaded with a small output resistance, we need to characterize the Gm nonlinearity in the presence of a large output resistance. This is done by increasing the output common mode resistance value, Rcm to 6K Ohm which is equal to total output resistance contributed by the transistor r_{ds} . When a signal is applied at the input, the output current gets equally divided between the transistor r_{ds} and Rcm since they are of equal resistance. Hence the quantity on the Y-axis in Figure 39, which is the ratio of the peak to peak current in Rcm to the input voltage,

cannot be denoted as the output transconductance. We define it as the transconductance, Rcm. Figure 39 shows its variation with the differential input.

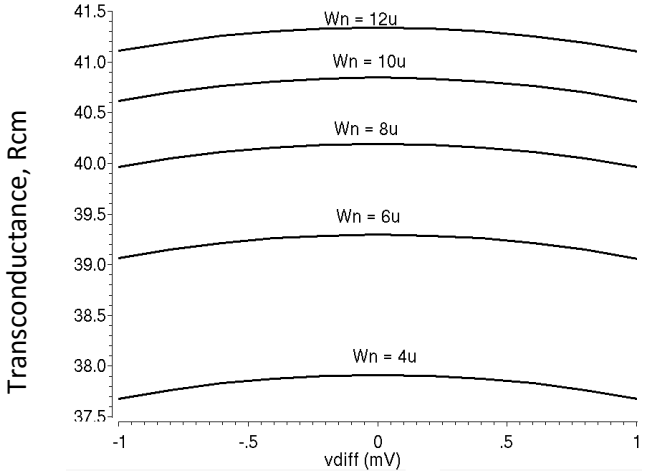

Figure 39 Ratio of peak to peak current in Rcm by input voltage vs differential input for Rcm=6K Ohm

It is seen that the transconductance, Rcm plots for all the NMOS sizes have a similar shape and do not indicate a matched condition as shown in Figure 39.

We further characterize the linearity using a two tone test for the amplifier in closed loop. Figure 40 shows the test bench for the closed loop simulations.

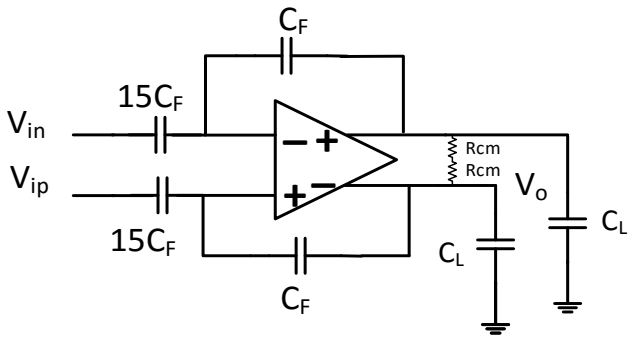

Figure 40 Closed loop test bench

As can be seen from the IM3 simulation results in Figure 41, no improvement in the linearity is obtained by matching the NMOS and PMOS transistor properties.

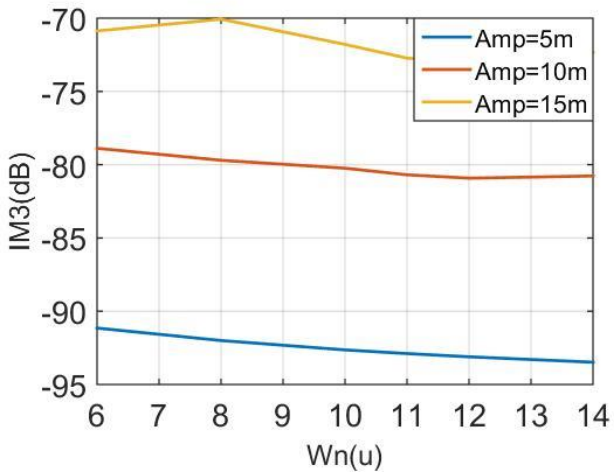

Figure 41 IM3 vs NMOS size for Rcm =6K Ohm

Table 2 Closed loop input and output amplitudes

Input Amplitude	**Output Amplitude**
A = 5mV	70.5mV
A = 10m	140mV
A = 20m	270mV

Table 2 shows the various output swings obtained for the applied input Amplitude tones.

These results indicate that the nonlinear transistor r_{ds} is dominating the linearity. In the previous section, we considered only the Gm-nonlinearity, modelled in Figure 42, ignoring the nonlinearity in the I-V conversion. The Gm nonlinearity cancellation method

that we described does not improve the linearity when we have a large nonlinear output resistance due to its dominating effect on the overall linearity.

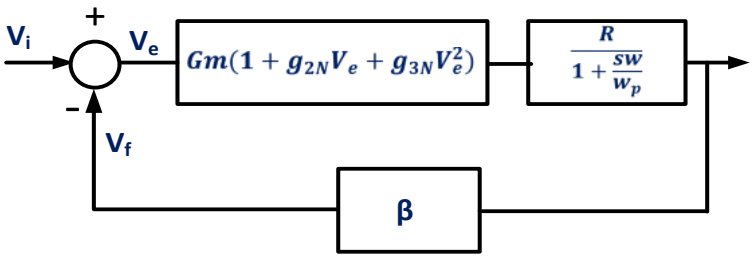

Figure 42 Gm nonlinearity model, adapted from [26]

The nonlinear output resistance for an amplifier can be described by

$$i_R = \frac{1}{R}(v_{out} + a_{2N,out}vout + a_{3N,out}v_{out}^3) \tag{3.9}$$

where a_{2N}, out and $a_{3N,out}$ are the nonlinear coefficients related to the output resistance [26]. It is more convenient to express the nonlinearity in the output resistance in the form of admittance.

The total output resistance of the output stage as shown in Figure 43, can be expressed as

$$\frac{1}{Z_{out}} = \frac{1}{Z_{nl}} + \frac{1}{R_{CM}}$$

where Z_{nl} is the nonlinear component of the output resistance, contributed by the transistor r_{ds} and R_{CM} is the output common mode resistance.

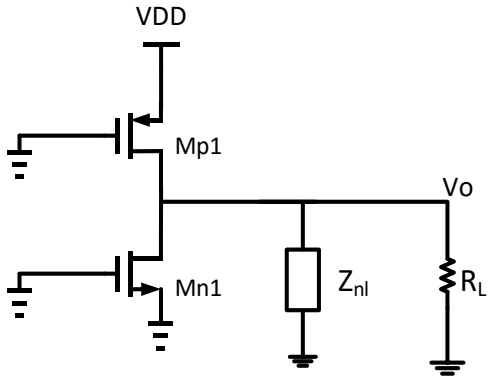

Figure 43 Output stage nonlinearity model

The admittance, $Y_{out} = \frac{1}{Z_{out}} = \frac{i_{out}}{v_o}$ can be expressed as

$$Y_{out} = Y_{nl} + Y_{CM}$$

where Y_{CM} is the inverse of the common mode sensing resistance and was chosen to be much smaller than Y_0. Y_{nl} is the nonlinear admittance, contributed by the transistor r_{ds} which can be expressed by,

$$Y_{nl} = Y_0 + Y_1 v_o + Y_2 v_o^2 + Y_3 v_o^3 + \cdots ...$$

Here Y_0 is the linear coefficient of the admittance, and Y_1,Y_2,Y_3 are the distortion coefficients of the output stage evaluated by differentiating the output current i_{out} with respect to the output voltage v_o at the operating point or quiescent condition.

$$Y_0 = \left(\frac{\partial i_{out}}{\partial V_o}\right)_Q, Y_1 = \left(\frac{\partial^2 i_{out}}{2!\,\partial V_o^2}\right)_Q, Y_2 = \left(\frac{\partial^3 i_{out}}{3!\,\partial V_o^3}\right)_Q$$

The total output admittance is then described by

$$Y_{out} = Y_{CM} + Y_0 + Y_1 v_o + Y_2 v_o^2 + Y_3 v_o^3 + \cdots .... \quad (3.10)$$

Normalizing the total output admittance by the linear component, Y_0 and Y_{CM} we obtain

$$\frac{Y_{out}}{Y_{CM}+Y_0} = 1 + \frac{Y_1}{Y_{CM}+Y_0} v_o + \frac{Y_2}{Y_{CM}+Y_0} v_o^2 + \frac{Y_3}{Y_{CM}+Y_0} v_o^3 + \ldots. \quad (3.11)$$

To understand the dependence and behavior of the nonlinear output resistance better, we measure the values of Y_1 and Y_2, the output admittance distortion coefficients for the four cases and tabulate them in Table 3. Table 4 compares the output currents and swings for all the cases. In the first 3 cases, we scale up the channel lengths of the output stage transistors while maintaining constant (W/L) ratio, output bias current and transconductances.

Table 3 Output admittance distortion coefficients

Cases	$\boldsymbol{Y_0}$	$\boldsymbol{Y_1}$	$\boldsymbol{Y_2}$
1)L=180n, IB=150u	134.018E-6	-7.5098E-6	9.37467E-6
2)L=360n, IB=150u	55.8425E-6	-0.5951E-6	5.30443E-6
3)L=600n, IB=150u	34.7805E-6	-0.984675E-6	3.04125E-6
4)L=600n, IB=37u	16.195E-6	-0.24617E-6	0.760295E-6

In the fourth case, the length is increased without scaling up the widths, having the effect of reducing the bias current, IB and transconductance by the same factor. The overdrive voltage, V_{DSAT} remains unaffected.

Table 4 Comparison of cases

Cases	**Input Swing(peak)**	**Output Swing(peak)**	**Output current(peak)**
1)L=180n, IB=150u	25mV	351mV	56uA
2)L=360n, IB=150u	25mV	356mV	57uA
3)L=600n, IB=150u	25mV	358mV	60uA
4)L=600n, IB=37u	25mV	305mV	55uA

It is observed that the values of the distortion coefficients reduce as the output stage transistor channel lengths are increased. The best improvement is observed for the fourth case where the channel length is increased without scaling up the transistor widths, causing the bias current to decrease. The effect of channel lengths on the distortion coefficients can be explained by examining the underlying causes of nonlinearity in r_{ds}, channel length

modulation. The channel length modulation parameter, λ is a factor responsible for VDS nonlinearity in the ideal square law equation.

$$i_d = 0.5\mu_n Cox\left(\frac{W}{L}\right)(V_{DSAT} - V_T)^2(1 + \lambda V_{DS}).$$

The channel length modulation parameter, λ , can be defined by

$$\lambda = \frac{\left(L - L_{effective}\right)}{L}$$

where $L - L_{effective}$ is the pinched off length of the channel.

It can be seen that by increasing the channel length, L the channel length modulation effect is suppressed.

We characterize and measure the variation of the third order intermodulation products at the output of the open loop amplifier. This is done by applying two signal tones at the output of the amplifier and measuring the resulting intermodulation products in the output current. Figure 44 shows the test bench for characterizing the output resistance. The input signals to the amplifier are grounded and an AC signal is applied at the output node, through a coupling capacitor. Figure 45 shows a plot of the output IM3 against the output voltage swing for the four cases in Table 3. It is observed that the IM3 reduces for increasing channel lengths.

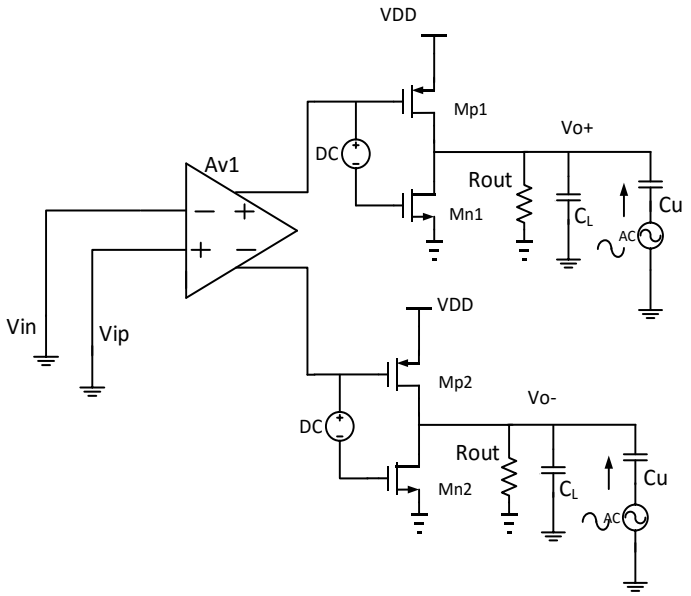

Figure 44 Test bench for output impedance characterization

Intuitively, we also expect the harmonic distortion due to the nonlinear output impedance to decrease at higher frequencies. As seen in Figure 44, the output impedance is the parallel combination of the load capacitor and the nonlinear output resistance. At higher frequencies, the relatively linear impedance of the load capacitor dominates and more current flows through it to ground. As smaller currents flow through the nonlinear r_{ds}, the overall distortion decreases. The same conclusions are supported by the data in [27], for a single stage amplifier model. It should be noted that channel length modulation is only one of the factors responsible for causing nonlinearity in the output resistance.Several other factors exist, such as the increased dependence of V_{th} on the channel length and drain voltage as the channel length reduces(short channel effect), velocity saturation, drain induced barrier lowering (DIBL), which are beyond the scope of this work.

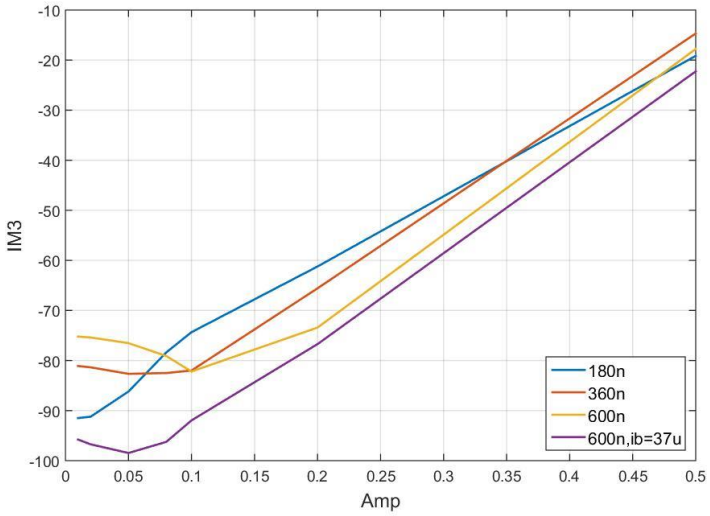

Figure 45 IM3 vs voltage signal amplitude applied at the output of the amplifier

For a better understanding of these effects, one needs to consult the relevent technolgy model. A few papers, [27] and [28] have modeled the nonlinearities in the output resistance arising from these effects.

Based on our output resistance characterization results, we increased the channel length of the output stage transistors. We plot the variation of transconductance, Rcm defined by the ratio of the peak to peak output current through the output common mode sensing resistor, Rcm by the input voltage swing, against the differential input in Figure 46. Consider cases 3 and 4 from Table 3 in this characterization. It is observed that in case 3, where the widths and the lengths of the output stage transistors are both scaled together, the Gm plots have a similar shape and do not indicate an optimal condition. However in

case 4, it is evident that an optimal linearity point exists for NMOS size, Wn=8u. In Figure 47, the variation of IM3 with the NMOS size for cases 3 and 4 from Table 3 is shown.

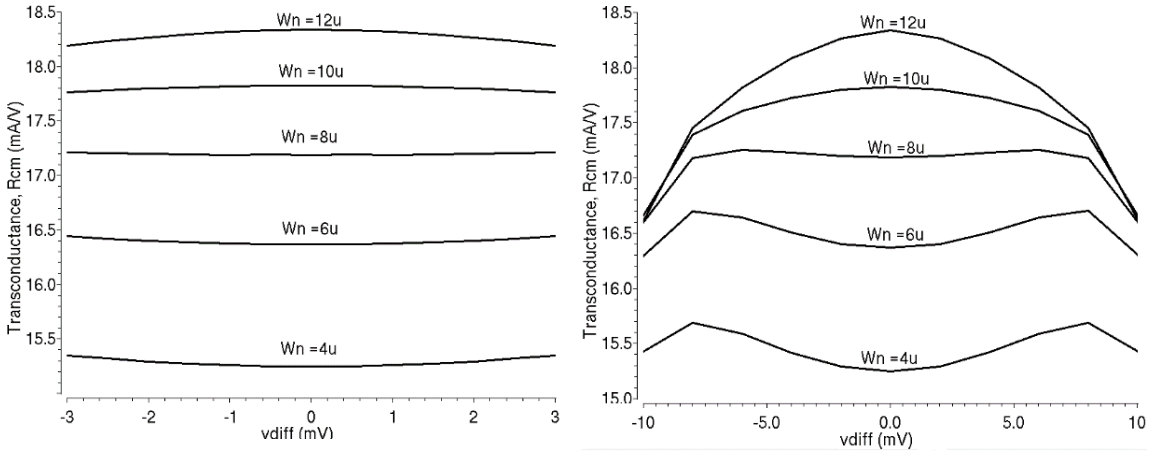

Figure 46 Transconductance, Rcm vs differential input for (a) L=600n, IB =150u (b) L=600n, IB =37u

It is observed that in case 4 the IM3 values show an optimal condition for linearity for Wn =8u agreeing with the Gm characterization plot in Figure 46b. However, for case 3, there is no observed optimal condition indicating that the output impedance nonlinearity is dominating over the Gm nonlinearity.

The same trend was observed for all the other cases in Table 3. The divergence for case 4 can be explained by observing that it has the lowest output admittance distortion coefficients, which implies that the output resistance nonlinearity is less dominant than in the previous cases.

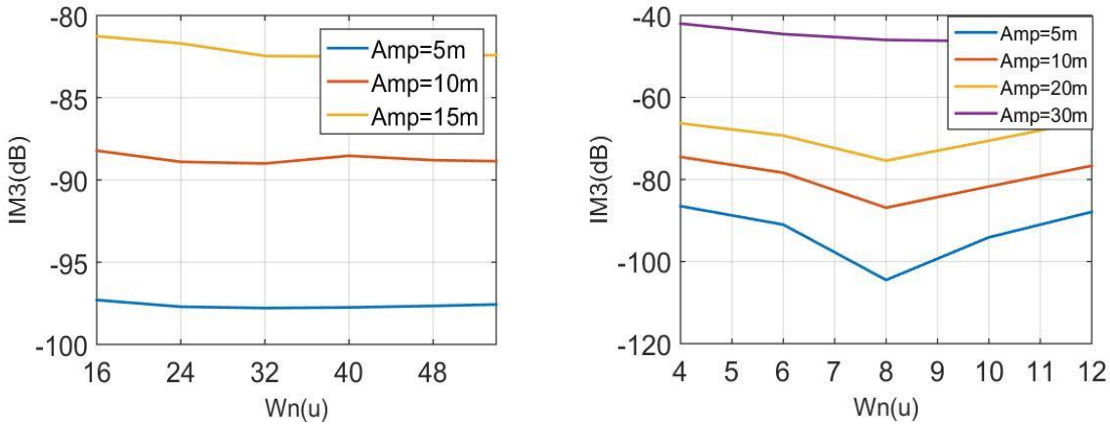

Figure 47 IM3 vs NMOS Size for a) L=600n, IB =150u (b) L=600n, IB =37u

3.4. Effect of P.V.T. variations

The optimal condition for case 4 in Figure 47(b), where the linearity is improved, is found to depend on the process, voltage and temperature. The NMOS and PMOS transistor matching depends on properties like the mobility (μ) and V_{DSAT} which are P.V.T variant. To understand the effect of P.V.T. variations on this method, we repeat the Gm characterization procedure and IM3 simulations under four different process corners, NMOS Fast PMOS Fast, NMOS Slow PMOS Fast, NMOS Fast PMOS Slow and NMOS Slow PMOS Slow.

1) NMOS Fast PMOS Fast

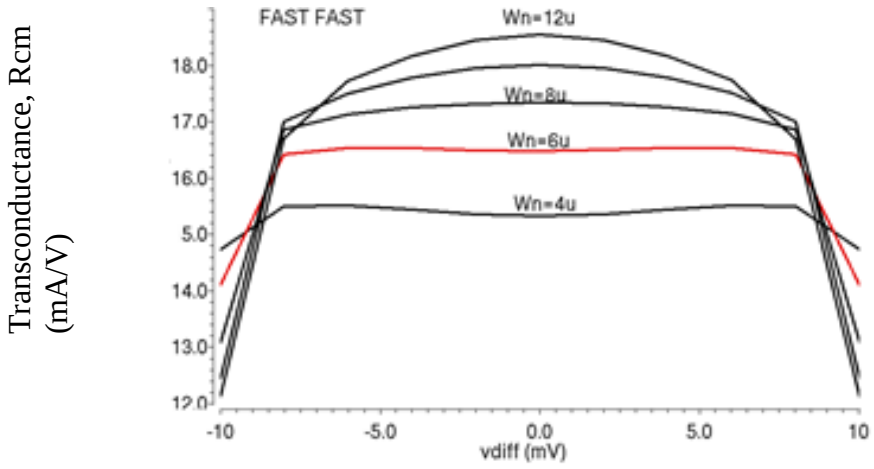

Figure 48 Transconductance, Rcm vs differential input in Fast Fast corner

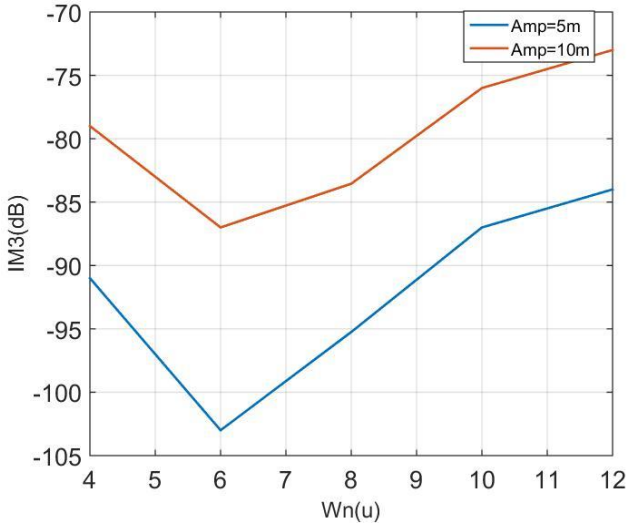

Figure 49 IM3 vs NMOS size in Fast Fast corner

It is observed from Figure 48 that the matched condition occurs for NMOS size, Wn=6u which is validated by the IM3 vs NMOS size plot shown in Figure 49.

2) NMOS Slow PMOS Fast

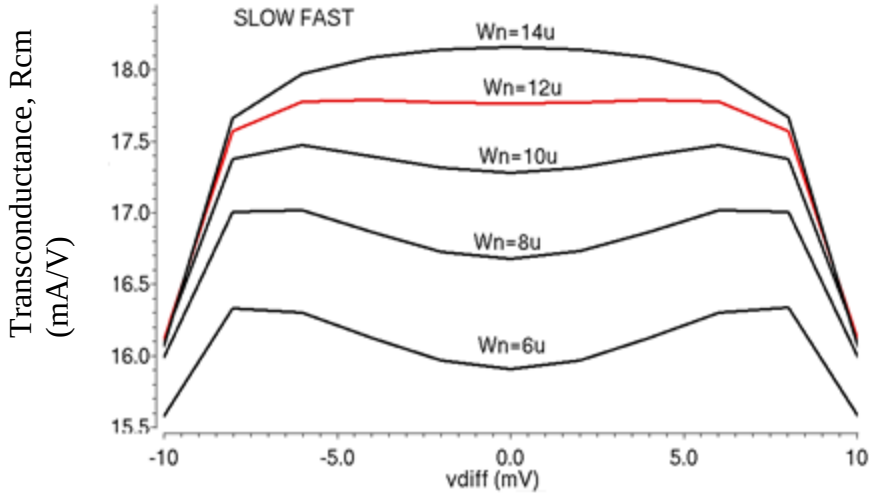

Figure 50 Transconductance, Rcm vs differential input in Slow Fast corner

It is observed from Figure 50 that the matched condition in the Slow Fast Corner occurs for the NMOS size, Wn=12u which can be verified by the IM3 vs NMOS size plot shown in Figure 51.

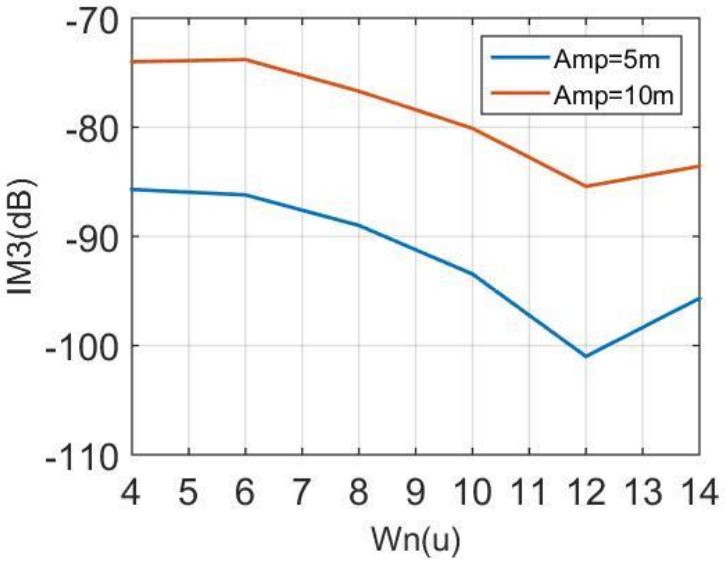

Figure 51 IM3 vs NMOS size in Slow Fast corner

3) NMOS Fast PMOS Slow

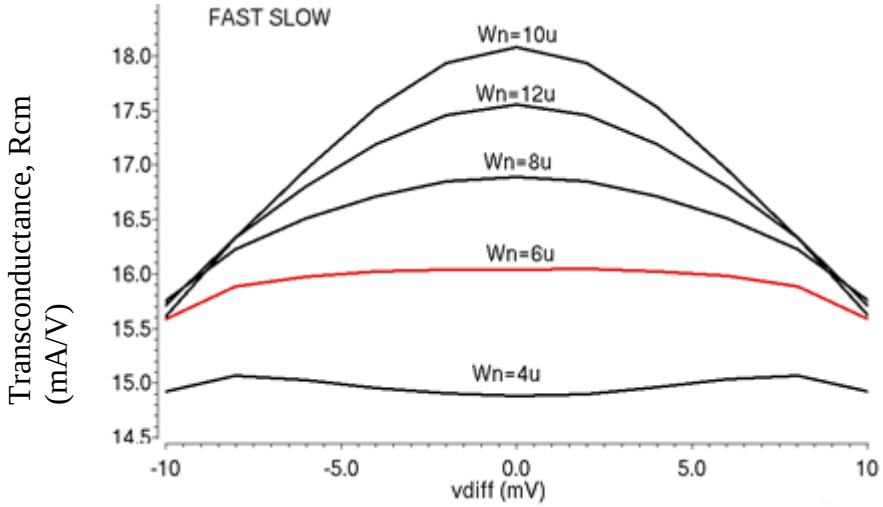

Figure 52 Transconductance, Rcm vs differential input in Fast Slow corner

It is observed from Figure 52 that the matched condition in the Fast Slow corner occurs for NMOS size, Wn=6u which can be verified by the IM3 vs NMOS size plot shown in Figure 53.

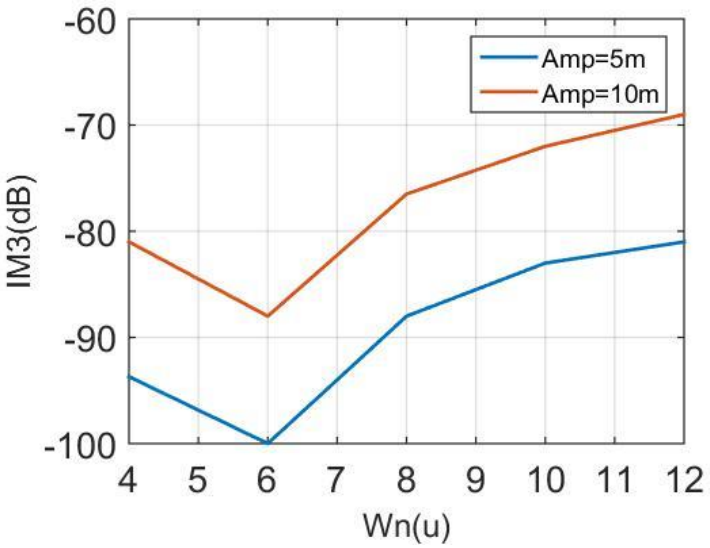

Figure 53 IM3 vs NMOS size in Fast Slow corner

4) NMOS Slow PMOS Slow

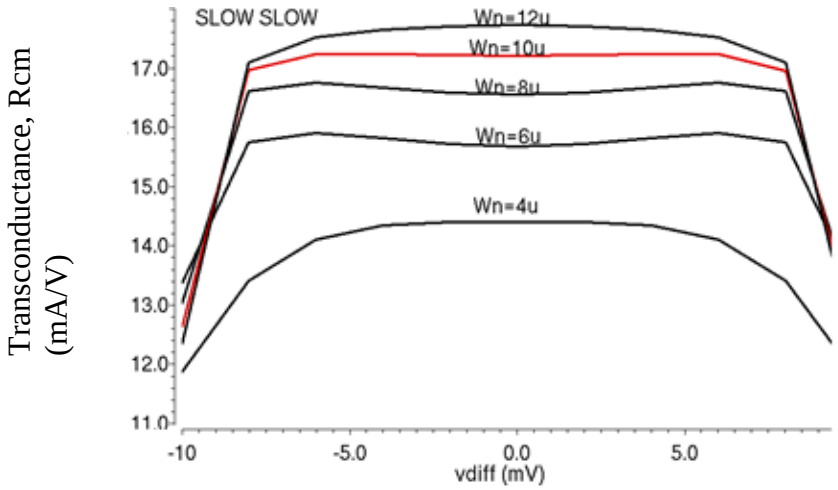

Figure 54 Transconductance, Rcm vs differential input in Slow Slow corner

It is observed from Figure 54 that the matched condition in the Slow Slow corner occurs for NMOS size, Wn=10u which can be verified by the IM3 vs NMOS size plot in Figure 55.

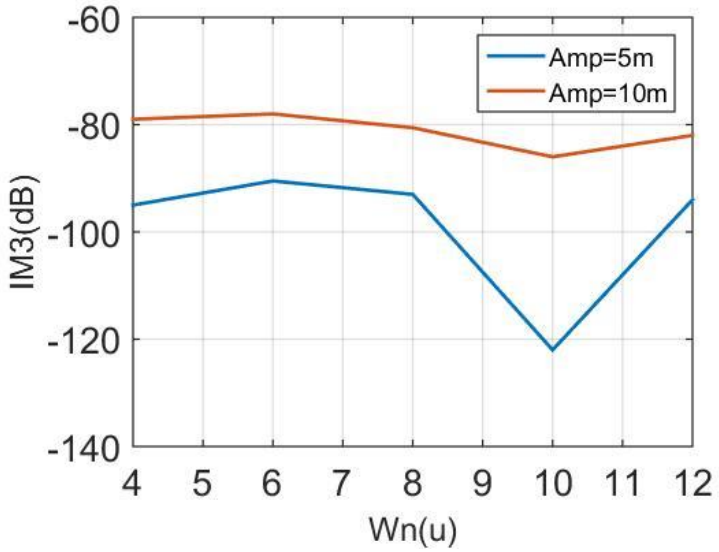

Figure 55 IM3 vs NMOS size in Slow Slow corner

It is observed that the optimal condition changes in different corners. Thus it is necessary to have a procedure to compensate for the different P.V.T. variations and always choose the optimal size.

3.5. Future work

To compensate for P.V.T. variations, it is necessary to have a system that can detect P.V.T. variations in the matched condition and compensate for them. This system can be implemented in the digital domain, due to the robustness of digital logic over analog

systems against noise, mismatch and other factors. This system needs to continuously operate, at very low frequency, at detect and tune for P.V.T. variations. Frequently, these kind of systems are used in I/O drivers to compensate for slew rate variations and mismatch sensitive analog circuits. For example, [29] describes a PLL based digital system to compensate for slew rate variations under P.V.T. variations.

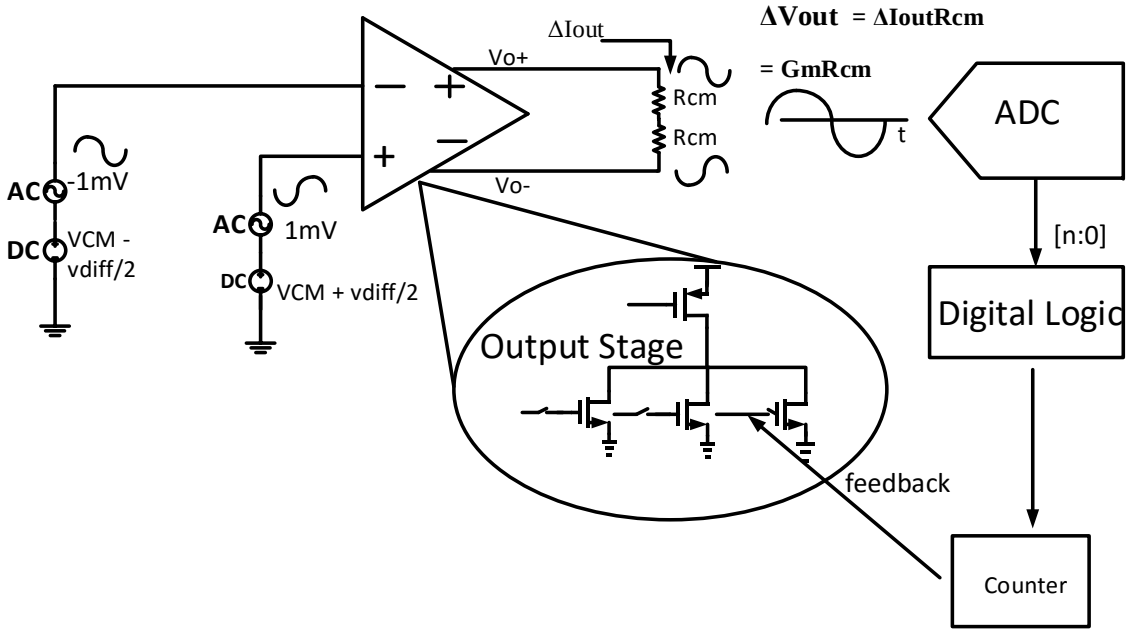

Figure 56 Digital system to tune for P.V.T. variations

There are several ways to implement this system. We propose an algorithm which is illustrated in Figure 56. The algorithm has 5 steps.

1) Measure Gm1 using a small AC signal applied at the input

2) Change the value of vdiff to one extreme and repeat (1) to obtain Gm2

3) Convert the two values of Gm to a digital code using an ADC.

4) Compare the two values of Gm measured and compare the difference.

5) If the values of Gm1 and Gm2 are different, update counter, which will activate the transistor bank at the NMOS of the output stage and change its size.

The Gm measurement procedure is implemented by applying a small AC signal, v_{in} at the input and measuring the change in output voltage across the common mode sensing resistors. The voltage across the resistors is given by,

$$\Delta V_{out} = \Delta \mathrm{I}_{\mathrm{out}} Rcm$$

$$\Delta V_{out} = \Delta \mathrm{Gm}\ \mathrm{v}_{\mathrm{in}} \Delta \mathrm{Rcm}$$

It can be seen that the voltage drop across the resistors is proportional to the Gm.

In the first step, a value for Gm is obtained at DC for vdiff =0, which is the region where both the NMOS and PMOS contributes almost equally to the output Gm. In the next step, this value needs to be compared with another value for Gm obtained at an extreme value for vdiff, where either the NMOS or PMOS transistor dominates the total Gm.

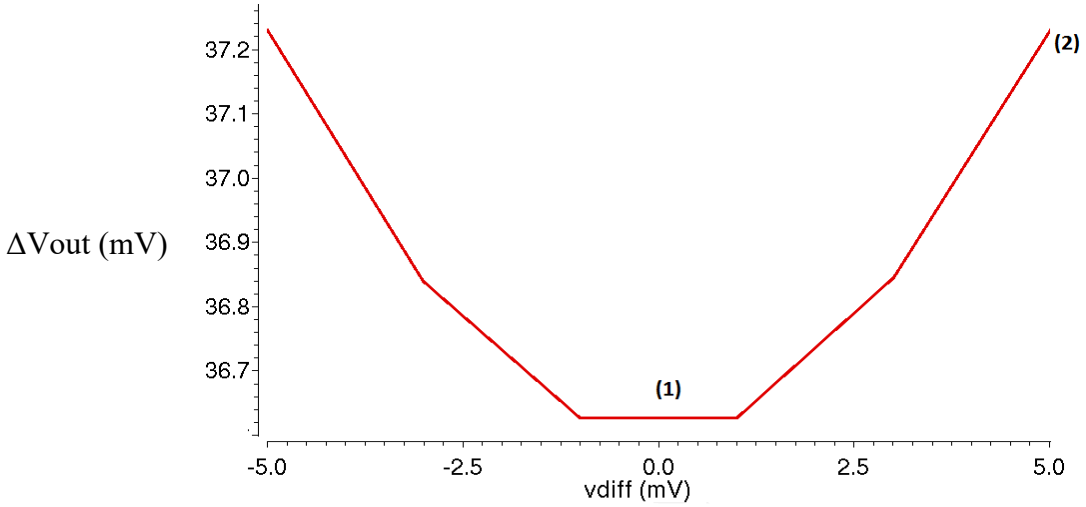

Figure 57 Voltage drop across resistor, Rcm

The two values are converted to digital codes by an ADC and compared using digital logic. The procedure is illustrated in Figure 57. If the values do not match or if the difference between them is too large, then a counter is updated, which would change the size of the NMOS transistor using switches. The NMOS transistor needs to be implemented as a bank of transistors, with each finger being controlled by a switch as illustrated in Figure 56. This enables the system to continuously tune the output stage so that it is always biased in the optimal condition for linearity.

4. SIMULATION RESULTS

This section details the simulation results of the amplifier with the Monticelli class-AB output stage and the amplifier with the proposed class-AB output stage. Table 5 summarizes and compares the performance specifications of the two amplifiers.

4.1 Comparison of amplifier parameters

The basic amplifier parameters such as DC gain, current consumption, settling time and linearity are summarized in Table 5. Figure 58 shows the frequency response of the amplifier based on the Monticelli based class-AB bias scheme and the amplifier based on the proposed class-AB bias scheme.

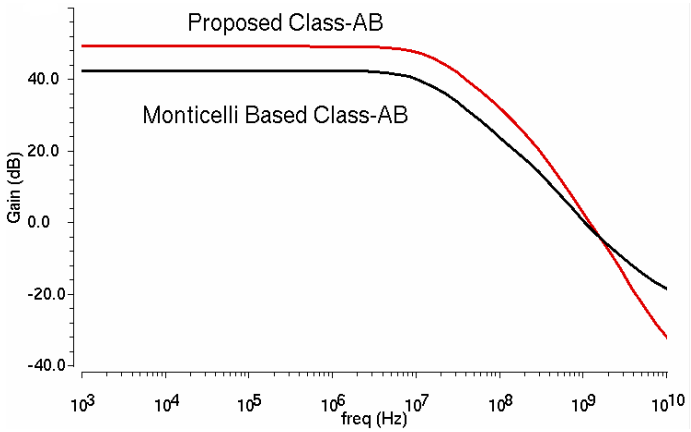

Figure 58 Frequency response of the Monticelli based class-AB amplifier and the amplifier based on proposed class-AB scheme.

It is observed that the new amplifier has a higher DC gain due its improved input stage. It has a DC gain of 49dB and a w_{3dB} cutoff of 20MHz. Figure 59 shows the test bench used for running closed loop simulations on the two amplifiers. The ideal closed loop gain is given by the ratio of the input capacitor and the feedback capacitor, which is 15.

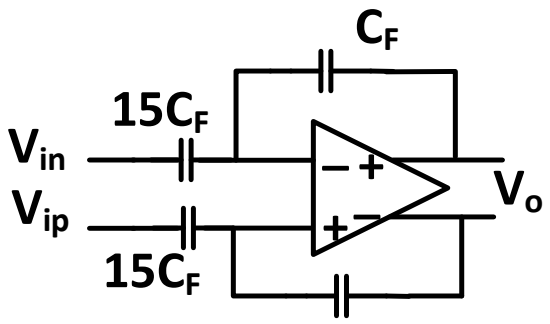

Figure 59 Closed loop test bench of the amplifier

Figure 60 shows the loop gain responses of the amplifiers based on the Monticelli class-AB bias scheme and the proposed class-AB bias scheme. The loop gain is higher for the new amplifier due to its higher DC gain.

Figures 61 and 62 show the transient responses of the amplifiers based on the Monticelli class-AB bias scheme and the proposed class-AB bias scheme, with a square wave of amplitude 20mV as the input. The 0.1% settling time is observed to be 6.54ns and 5.8ns respectively. To compare the linearity of the two amplifiers, we plot their respective IPN curves in Figure 63 and 64. As can be seen, the proposed class-AB amplifier has higher IIP3 indicating that it has higher linearity.

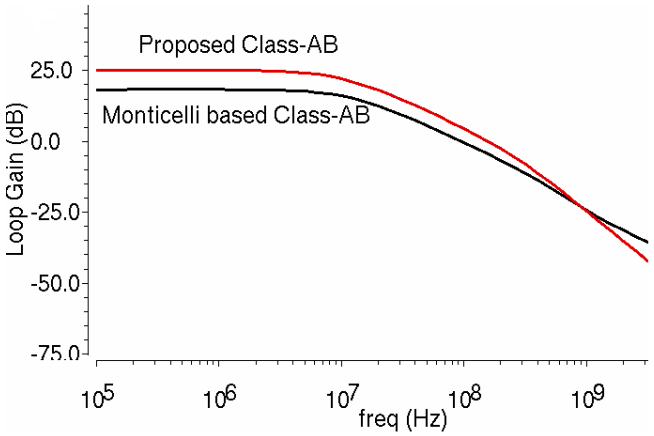

Figure 60 Loop gain frequency response for the Monticelli based class-AB amplifier and the amplifier based on proposed class-AB scheme.

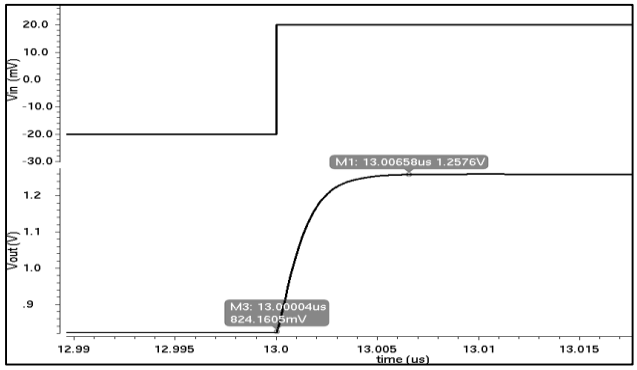

Figure 61 Step response of the Monticelli based class-AB amplifier

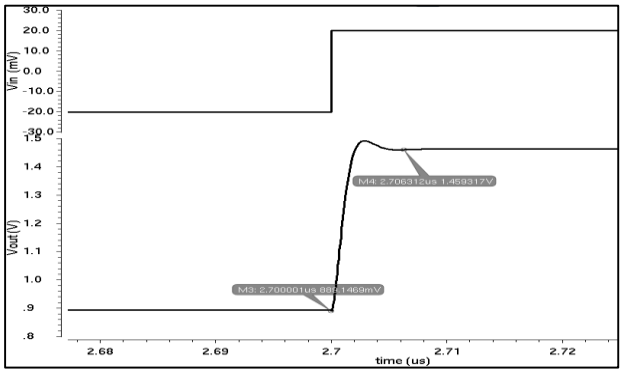

Figure 62 Step response of the amplifier based on proposed class-AB scheme.

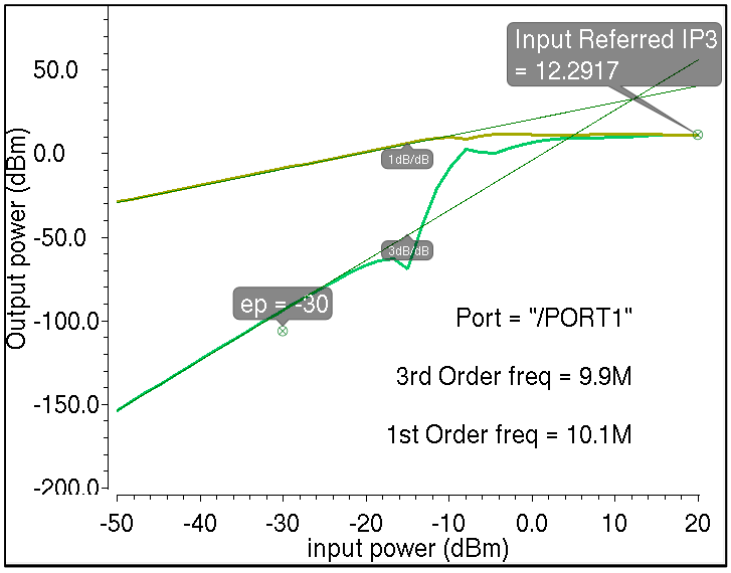

Figure 63 IPN curves of the amplifier using output stage based on Monticelli bias scheme

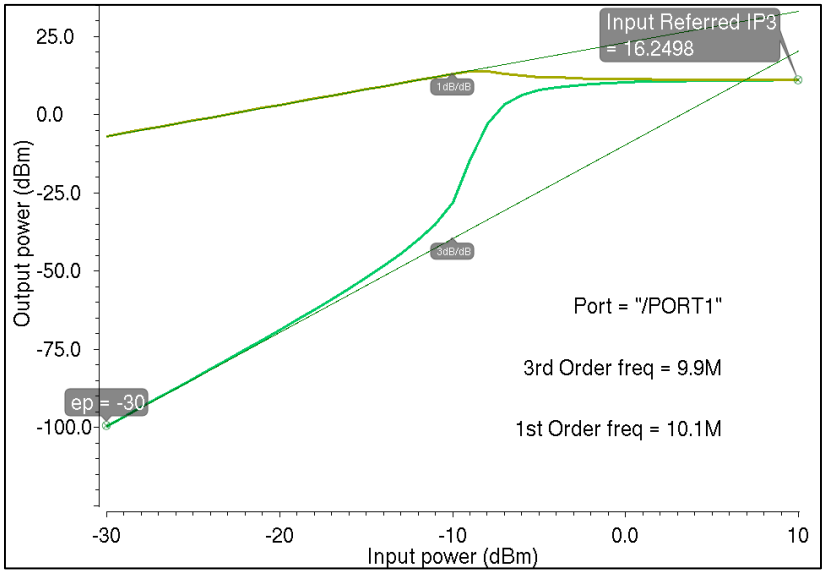

Figure 64 IPN curves of the amplifier using proposed class-AB output stage

In a second design for the amplifier with the proposed class-AB output stage, the output stage transistors' channel lengths were increased to twice the minimum length in this technology. Table 5 compares the parameters of all three amplifiers.

4.2 Analysis of results

From Table 5, it is observed that the proposed amplifier exceeds the specifications of the Monticelli level shifter based Class-AB amplifier with respect to power and settling time. The new amplifier is also found to have better linearity than the Monticelli level shifter based architecture due to its improved DC level shifter.

The IIP3 values are found to be dependent on the closed loop gain, which is 15 for both the amplifiers. The second design of the proposed amplifier, with twice the minimum length output stage transistors was found to have achieve better linearity. This is because having higher channel length output stage transistors reduces the output resistance distortion as discussed in the previous section. The amplifier also has higher open loop gain which reduces the closed loop distortion. However, this amplifier suffers with respect to the settling time, since the parasitic capacitances increase as the channel length increases.

Finally to verify the nonlinearity cancellation method described in the last section, we compare the IPN curves of the proposed class-AB amplifier for two NMOS sizes, corresponding to matched and unmatched conditions.

Table 5 Comparison of results

Parameter	**Conventional Class-AB Amplifier with Monticelli Bias scheme**	**Proposed Class-AB Amplifier (With Minimum length Output stage)**	**Proposed Class-AB Amplifier (With 360nm length output stage)**
Amplifier DC Gain	42 dB	48.5 dB	51.45 dB
feedback factor	1/16	1/16	1/16
Total Current Consumption	2.22mA	2mA	2mA
Output Stage Current	130uA	150uA	150uA
0.1% Settling Time	6.54ns	5.8ns	8.7ns
IIP3	12.29	16.25	19.63
Load	300f	300f	300f
Technology	Jazz 0.18um	Jazz 0.18um	Jazz 0.18um
Supply	1.8	1.8	1.8

In both cases, the output stage transistor channel lengths are increased to 600nm (to reduce the effect of nonlinear output resistance). In Figure 65, we have the IPN curves for the bias conditions corresponding to case 3 in Table 3(the output stage transistor widths are scaled along with the length, keeping the bias current constant). In Figure 66, the IPN curves corresponding to case 4 in Table 3 are shown (the output stage transistor widths are not scaled along with the length, changing the bias current).

For the IPN curves plotted for case 3 in Table 3, in Figure 65, we observe that the matched and unmatched cases have identical third order derivatives. This shows that Gm nonlinearity cancellation does not improve linearity in the matched condition which implies that the transistor r_{ds} is the dominant factor here determining the linearity.

For the case 4 simulation results shown in Figure 66, it is observed that the design with the matched NMOS and PMOS properties shows improved values for IIP3, supporting the conclusion that third order nonlinearity is cancelled using this procedure.

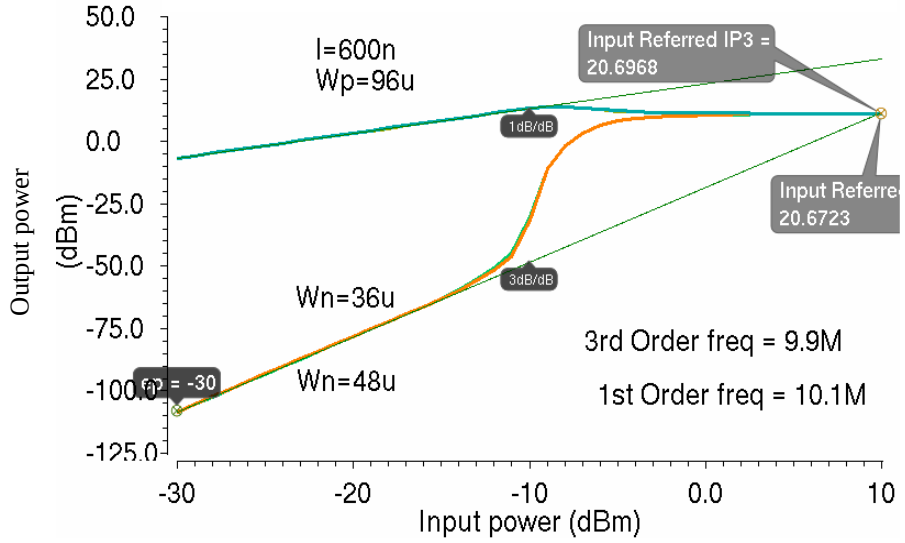

Figure 65 IPN curves for the proposed amplifier with output stage transistor L=600n, IB = 150uA for the matched (Wn=36u) and un-matched (Wn=48u) condition.

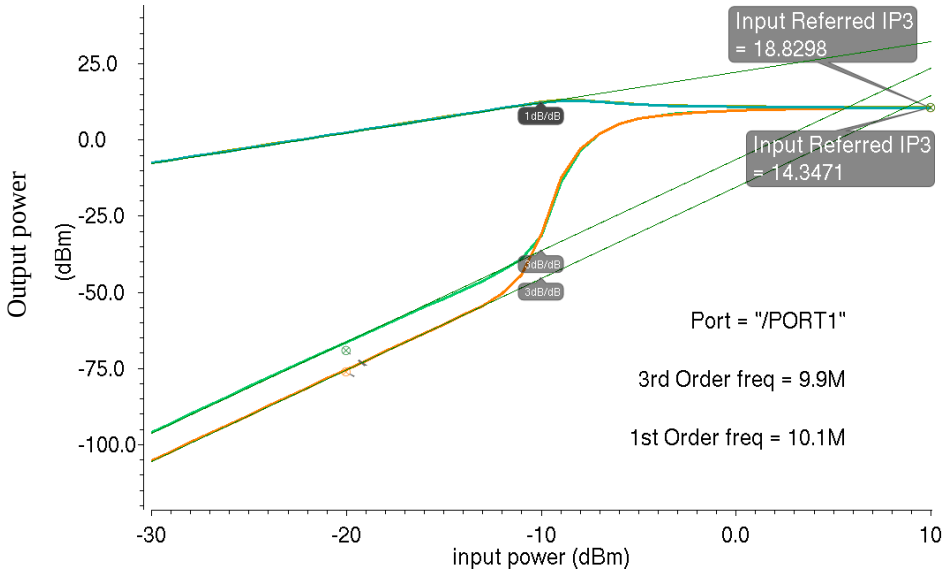

Figure 66 IPN curves for the proposed amplifier with output stage transistor L=600n, IB=37uA for the matched (Wn=8u) and un-matched (Wn=12u) condition.

These observations lead us to conclude that the transistor r_{ds} is an important factor influencing the total linearity of the amplifier apart from the output stage Gm, and cannot be ignored as explained in the previous section. The output stage in case 4, having lower resistance distortion coefficients than case 3, sees an improvement in linearity through Gm nonlinearity cancellation.

To show the effect of the output resistance nonlinearity for case 4 in Table 3, we increase the output common mode sensing resistance from 6K Ohm to 100K Ohm and plot the IPN curves in Figure 67. It is observed that the IIP3 value has increased, because the higher output resistance improves the open loop gain which increases the closed loop linearity. However, both the matched and unmatched cases have similar third derivative curves showing that when the effect of nonlinear r_{ds} was increased, the Gm nonlinearity cancellation is no longer effective.

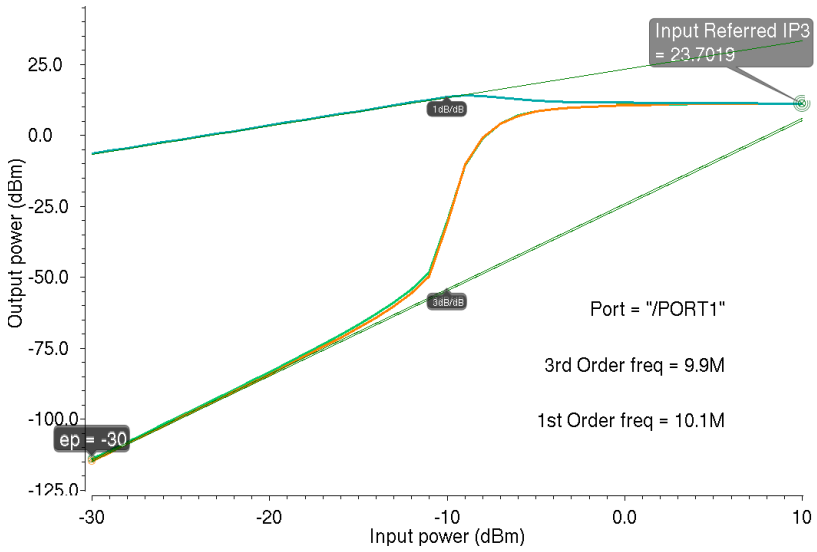

Figure 67 IPN curves for the proposed amplifier with output stage transistor L=600n, IB=37uA, Rcm = 100K Ohm for the matched and un-matched condition

5. CONCLUSION

The requirement of pipeline ADCs to achieve both high performance and power efficiency has led to the suggestion of the class-AB amplifier as a substitute for the conventional class-A amplifier. The class-AB amplifier was studied and its design considerations were put forward. The state of the art with respect to class-AB level shifters, the Monticelli output stage was analyzed and its shortcomings were analyzed. To improve the Monticelli level shifter, a new class-AB output stage was proposed and designed. The new class-AB output stage was found to exceed the performance, power and linearity of the conventional class-AB amplifier.

The problem of nonlinearity in the class-AB amplifier was discussed and solutions were put forward. Our proposed technique aims to cancel the distortion in the output stage, arising from cross-over distortion, which is a problem associated with the class-AB amplifier. The proposed technique was however found to when the nonlinearity of the output resistance becomes dominant. To understand the nonlinearity of the output resistance, we characterize it for various output stage transistors' channel lengths. It was observed that its effect over the transconductance nonlinearity can be reduced under certain conditions. Finally we examine the effect of process, voltage, temperature variations on our proposed nonlinearity cancellation method and propose an algorithm to compensate for them.

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