WIRELESSLY-POWERED CMOS FRONT END FOR LOCOMOTIVE IC APPLICATIONS

A Thesis

by

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ABSTRACT

The steady leaps in miniaturization made in the realm of integrated circuit (IC) design has opened up prospects for a vast number of interesting possibilities. One of the possibilities is the idea of a locomotive integrated circuit. Unlike a typical IC that is soldered on a printed circuit board (PCB), locomotive ICs can be untethered and free to move around its environment. Recent research has demonstrated locomotive ICs that can potentially be used for non-invasive medical procedures including precise drug delivery targeted to specific problematic region of the body

Recent research has demonstrated locomotion using a variety of schemes including using electrolytic bubbles and manipulation of Lorentz force in a uniform magnetic field. In this work a wireless front end for a locomotive IC that relies on surface acoustic wave (SAW) devices is explored. A SAW device is a piezoelectric material that converts electrical stimulus into mechanical vibrations. For this work, the SAW device has been designed specifically to enable the mechanical vibration generated by electrical stimulation at 177MHz to potentially actuate motion.

This work demonstrates a complementary metal-oxide semiconductor (CMOS) front end IC implemented in 180nm process that can potentially be used for locomotion by means of electrical excitation of a SAW device with an on-chip PLL frequency synthesizer. The energy required to power the IC is obtained through resonant wireless power transfer between a pair of PCB inductor coils. The IC also contains power conditioning blocks that rectify the alternating voltage across the receiver inductor coil and generates a regulated DC voltage that powers the PLL frequency synthesizer. The entire proposed locomotive system consisting of PCB receiver coil, CMOS IC and SAW device fits inside an area of 1.5cmX1.9cm.

DEDICATION

To my parents and my little sister, for all their love and prayers.

ACKNOWLEDGEMENTS

I express my sincere gratitude to my advisor Dr. Sam Palermo, who has been constantly motivating me in my research and has been a source of inspiration for me. I would like to thank him for his excellent ideas and for being patient with me throughout this project providing me guidance and strong support in my endeavors.

I am also grateful to Dr. Jun Kameoka for serving on my committee as well as for supporting the pursuit of a SAW device based locomotion. Special gratitude goes to Dr. Edgar Sanchez-Sinencio and Dr. Darren Hartl for taking time out of their busy schedules to serve on my committee.

I would like to acknowledge the contribution of Sina Kordmahale who went out of his way to support this project. On more than one occasion, he spent late nights in the laboratory preparing the SAW device and working on the wirebonding machine to ensure that this project remains on track.

My peers- Osama El-Hadidy, Ayman Shafik and Ehsan Zhian Tabasy deserve thanks for their timely and helpful advice with laboratory measurements. Additionally, I would like to thank Francy Varghese, Srikanth Nagaraja and Naveen Thomas for their suggestions and for continued support in many of the courses at A&M.

I am deeply indebted to my parents for all their support throughout my graduate studies. It was a very tough time for our family and through all the personal struggles, my parents never waivered in their emotional support for my endeavors.

NOMENCLATURE

CMOS	Complementary Metal Oxide Semiconductor
IC	Integrated Circuits
IDT	Inter Digitated Transducers
LIC	Locomotive Integrated Circuits
LDO	Low Drop Out
MHD	Magneto Hydro Dynamics
PCB	Printed Circuit Board
PLL	Phase Locked Loop
SAW	Surface Acoustic Wave
WPT	Wireless Power Transfer

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1. INTRODUCTION

1.1 Overview of Locomotive ICs

The steady leaps in miniaturization made in the realm of IC design has opened up prospects for a vast number of interesting possibilities. In 1959, at a lecture in CalTech, the physicist Dr. Richard Feynman presented the wild idea that with miniaturization, we will be able to, in a sense, swallow the surgeon [1]. His vision consisted of an extremely small mechanical contraption that goes into the blood vessel, navigates its way into the heart, looks around and operates on a faulty valve, instead of a surgeon operating on the same valve by means of an open heart surgery. While this vision of a completely autonomous surgeon is still in the realm of a fantastic fiction, the tools to make such a machine are now well within our grasp.

Recent research has already demonstrated implantable biomedical ICs [2]. A key component to realizing a completely autonomous implantable biomedical IC is the ability for that IC to move around. Recent research has demonstrated a variety of propulsion schemes for ICs or miniature micro-systems that enables locomotion. For example, [3] demonstrates a mm-sized wirelessly powered locomotive implant for biomedical applications. The authors have envisioned applications involving non-invasive medical procedures including precise drug delivery targeted to specific problematic region of the body. This research demonstrated locomotion by manipulating the Lorentz forces on current carrying wires. This approach required the use of external magnets to provide a uniform static magnetic field and demonstrated two mechanisms for generating propulsion- one based on magnetohydrodynamics (MHD) and the other based on asymmetries in fluid drag forces experienced by a structures oscillating due to alternating currents flowing through a loop of wire. Despite demon-

strating a novel scheme for IC locomotion, the research had some key limitations both of which severely compromises the scope for miniaturization. Firstly, this implementation required powerful external magnetic field, which will necessitate the use of big external magnets. Secondly, this scheme required external antenna to harvest electro-magnetic energy, which makes the overall system bigger than it needs to be. Despite these serious limitations, the research demonstrated a wirelessly powered locomotive IC capable of controlled motion in water.

[4] presented a controlled drug delivery system on a chip using electrolysis. The scheme controlled drug delivery by using the force of bubbles generated during electrolysis to open reservoirs and release drugs. While this system was not locomotive, the idea of using bubbles to generate generate force was further refined in [5] and proposed as a locomotive IC. In [5] [6], the authors demonstrated a locomotive IC that utilizes electrolytic bubbles for motion. Bubbles generated by on-chip electrolysis created the counterforce that propelled the IC. Unlike the work described in [3], this work did not require any external magnets. Moreover, [5] demonstrated locomotion using on-chip coils for wireless power transfer. The use of on-chip coils, while reducing the efficiency of WPT, leads to a more miniaturized system. Additionally, the research demonstrated controlled motion by sending control signals by amplitude modulating the carrier/power signal. These control signals are demodulated on-chip and used to control the direction of motion by selecting one of the various electrolysis systems. The authors imagine using their system in applications like tumor biopsy and abdominal dialysis, in which the controllable nature of their locomotive IC enables precise orientation and stabilization of their system to achieve the required application.

A few other potential locomotive schemes have been demonstrated in literature especially in the field of capsule endoscopy. For example, [7] describes a locomotive

mechanism that was inspired from the locomotion principles of inchworms. This mechanism employed shape memory alloy (SMA) wires to close and open "legs" on a microcapsule with which the microcapsule can anchor or crawl along the inside walls of the intestine. A similar mechanism, also using SMA, was proposed in [8]. A good summary of the wide variety of locomotive schemes proposed for capsule endoscopy can be found in [2].

1.2 Organization

This chapter continues with the discussion of SAW device as a potential actuator that can enable a miniaturized locomotive system. In the second chapter some system level considerations for locomotive IC are discussed. Next, since locomotive systems typically involve wireless power delivery, a simple analysis scheme to compare the nature of resonance in a two coil near field wireless power transfer system is presented in the third chapter. Following the discussion on wireless power transfer, the individual circuits used in CMOS front end for a potential locomotive system using SAW device is presented in chapter four. Next, in chapter five, silicon measurement results are presented that shows the correct operation of the CMOS front end.

1.3 SAW Transducers

In this work, a CMOS front end for a potential locomotive system using surface acoustic waves is explored. SAW devices are piezoelectric, which means these devices convert electrical stimuli into mechanical vibrations and vice versa. The key idea in using a SAW based locomotive scheme is that by fabricating a suitable SAW device and exciting it electrically at its resonant frequency, the resulting mechanical vibrations will actuate motion. While SAW device has been used as a locomotive scheme in [9], the system presented in that work was not miniature since the SAW

device was excited by electrical power from an external amplifier delivered to the SAW device through a pair of wires. This thesis describes the electrical circuits involved in realizing a locomotive IC that uses a SAW device as an actuator. The CMOS front end proposed in this work is used to excite a single SAW device. The locomotive system realized using this architecture has only one degree of freedom. That is, the SAW device either turned "ON" propelling the system in one direction or turned "OFF" whereby the system comes to a stop. The activation of SAW mechanism is done by means of an external power (WPT into the receiver coil) switched on and off. A more advanced system will have, for example, amplitude modulated (on-off keying) signal on the carrier used for WPT. This modulation scheme will provide control signals to control multiple actuators by which controlled locomotion along multiple degrees of freedom can be achieved.

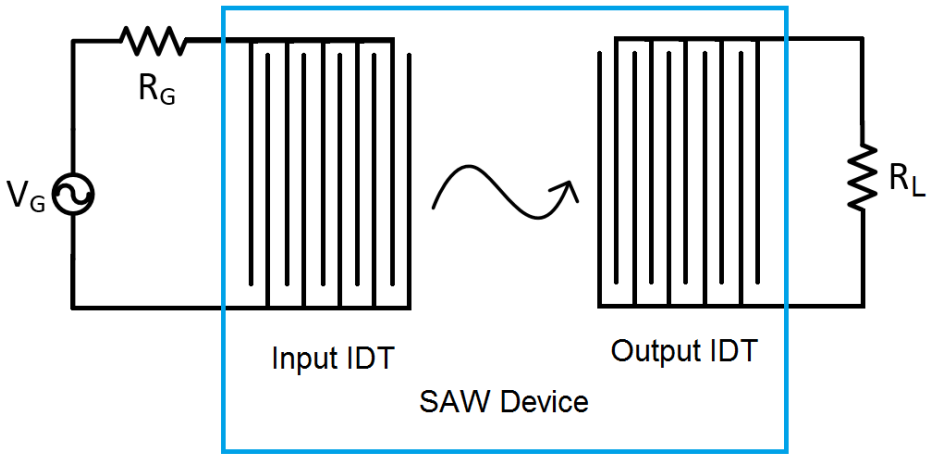

Figure 1.1: Typical SAW device in use

Electrical excitation of the piezoelectric substrate of the SAW device is done by utilizing comb-like metal structures called IDTs (Inter Digitated Transducers) as shown in Fig. 1.2. Lithium niobate ($LiNbO_3$) and zinc oxide (ZnO) are very popular piezoelectric substrate found in literature. For this work, aluminium metal was used to form IDT on lithium niobate substrate. The role of the IDT is to convert electrical energy to mechanical energy and vice versa. In a typical application, a pair of these IDT structures separated by a short distance forms a SAW device as shown in Fig. 1.1. At the input IDT, the electrical stimulus generates surface acoustic waves. These mechanical waves travel through the surface of the substrate to the output IDT where the mechanical energy in the waves is converted back into electrical energy.

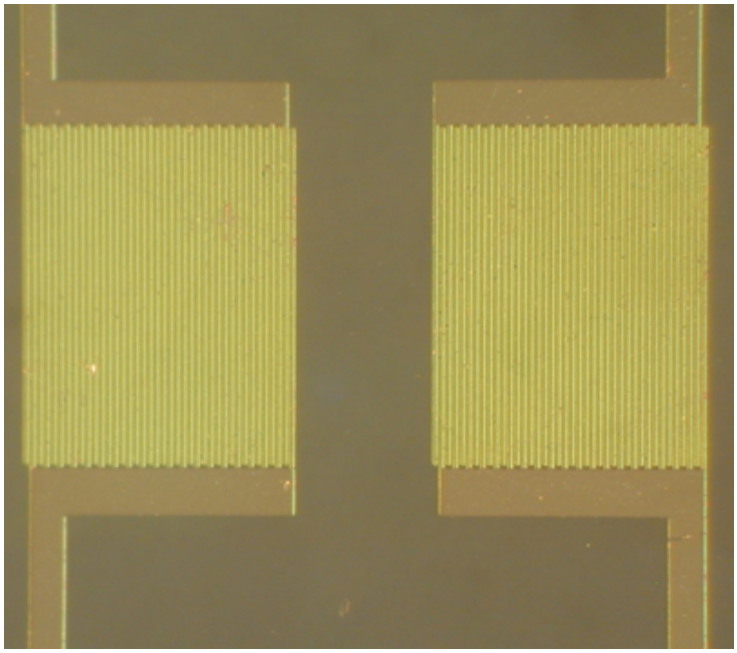

Figure 1.2: IDT structures formed by depositing Al on a $LiNb0_3$ substrate

An important property of the IDT that is that the mechanical response of the SAW device is highly band selective in nature. The resonant frequency f_0 of the SAW device is related to the speed of sound through subtrate (ν) and the periodicity of the lattice l as $f_0 = \frac{\nu}{l}$. Then the wavelength of surface acoustic wave is l. As a result of this resonant response, SAW devices find applications as band select filters in RF microelectronics. As the surface waves traverse from the input IDT to the output IDT, it experiences a delay. The nature of the delay can be a function of the medium surrounding the surface. This is because surface acoustic waves have a horizontal and vertical shear component that can couple with the medium in contact with the surface of the SAW device. This property of SAW devices have been exploited for making sensors used to detect chemicals, humidity and vibrations [10], [11], [12].

In recent years surface acoustic waves have been used to drive microfluidics. Consider a drop of liquid placed near an IDT. As the IDT is driven by a sinusoidal input at its resonant frequency, surface waves are generated. As these waves come into contact with the drop, the acoustic energy refracts into the drop because of the difference in the velocity of sound between the substrate and liquid. The resulting energy transfer causes recirculation of liquid which was demonstrated in [13] as shown in Fig. 1.3. This phenomenon has been demonstrated in [9] as a propulsion scheme for a locomotive system. At slightly higher SAW energy, there is also a horizontal component to the energy transfer that results in a net force to the entire drop in the direction of propagation of the surface wave. This was demonstrated in [14] as shown in Fig. 1.4. The use of even higher SAW power facilitates acoustic streaming to have sufficient energy to bring about microfluidic jetting and eventually atomization as shown in Fig. 1.5

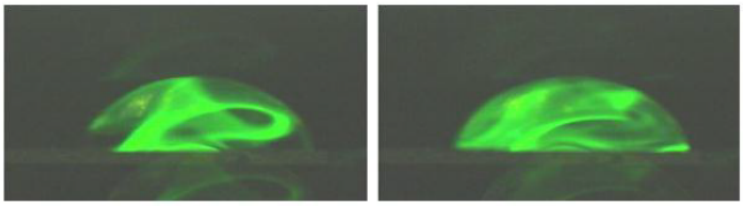

Figure 1.3: Mixing of a fluorescent dye in a water droplet due to agitation by SAW [13]

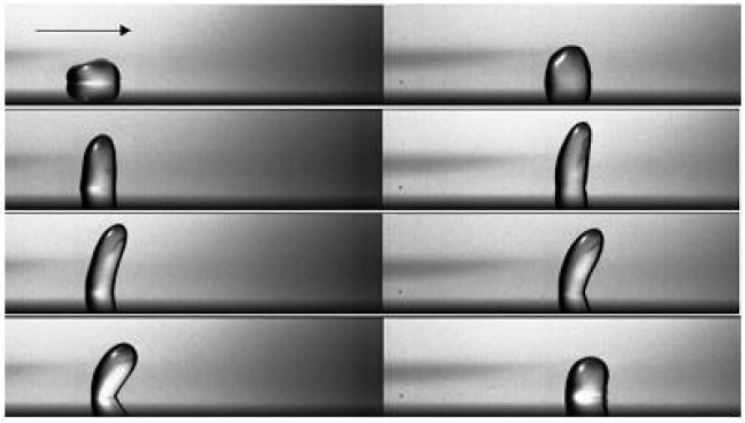

Figure 1.4: Acoustic streaming of droplet in the direction of surface acoustic waves [14]

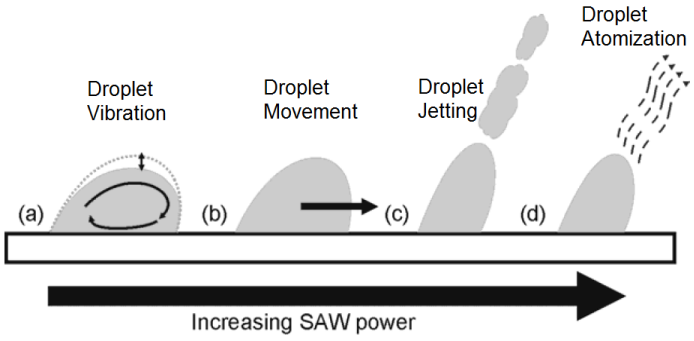

Figure 1.5: Transition from vibration to atomization in droplet as SAW power is increased [15]: (a) Vibration (b) Actuation or streaming (c) Jetting and (d) Atomization

Modelling of SAW device has been covered in detail in [16]. As shown in Fig. 1.6 shows a simple analytical model of the SAW device. The electrical equivalent circuit of the an IDT is a parallel resonance circuit consisting of capacitances C_T and a complex admittance $Y_a(f)$. The capacitance C_T has nothing to do with surface waves and is due to charge density along the IDT when a voltage is applied across the electrodes. The admittance $Y_a(f)$ arises because of the interaction of the IDT with the surface waves generated by it. $Y_a(f)$ consists of a real part $G_a(f)$ called radiation conductance and an imaginary part $B_a(f)$ called radiation susceptance. Therefore the total electrical admittance offered by the IDT to the electrical source driving it is given by

$$Y_{total}(f) = G_a(f) + j(B_a(f) + 2\pi f C_T). \tag{1.1}$$

It can be shown that $B_a(f)$ and $G_a(f)$ are Hilbert transform of each other. [16] develops a transmitter response function μ which depends on frequency f and metallization ratio η.

$$G_a(f) = 2|\mu|^2 y_O \frac{W}{\lambda}, \tag{1.2}$$

where y_O is equal to 0.21mmho for $LiNbO_3$. Additionally,

$$B_a(f) = G_a(f)(\frac{sin(2x) - 2x}{2x^2}), \tag{1.3}$$

where $x = \dfrac{N\pi(f - f_o)}{f_o}$. For a metallization ratio of $\eta = 0.5$, it can be shown that

$$\mu = 0.75K^2N \frac{sin(N\pi \dfrac{f - f_o}{f_o})}{N\pi \dfrac{f - f_o}{f_o}} \tag{1.4}$$

around the resonant frequency f_o of IDT. The constant K^2 is equal to 4.6% for y-cut $LiNb0_3$ wafer. Using this information, $G_a(f)$ and therefore $B_a(f)$ can be calculated. The capacitance C_T can be calculated using the relation, $C_T = NC_SW$ where N is the number of electrode pairs used in IDT, C_S is 4.6pF/cm for y cut $LiNbO_3$ wafer and W is the beam width of IDT. For the SAW device used in this project, N is 10, W is 980μm and f_o is 177MHz and the S_{11} can be simulated in MATLAB as shown in Fig. 1.7 using the equivalent circuit shown in Fig. 1.6.

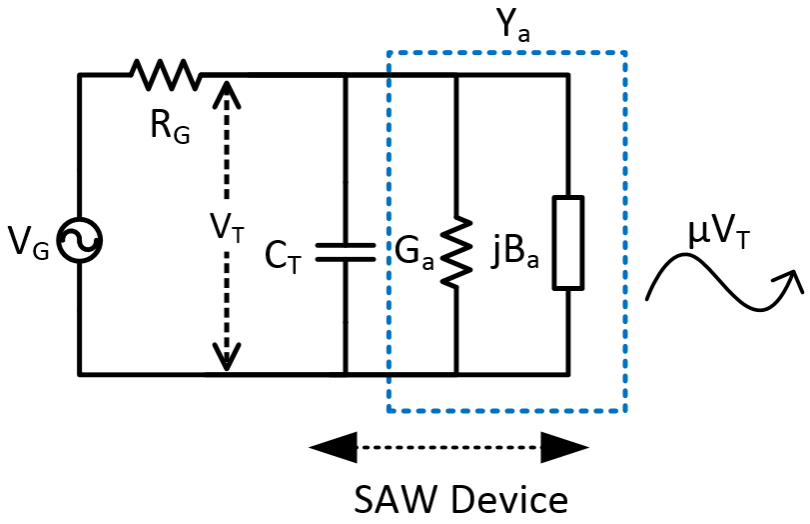

Figure 1.6: Electrical equivalent circuit for SAW IDT

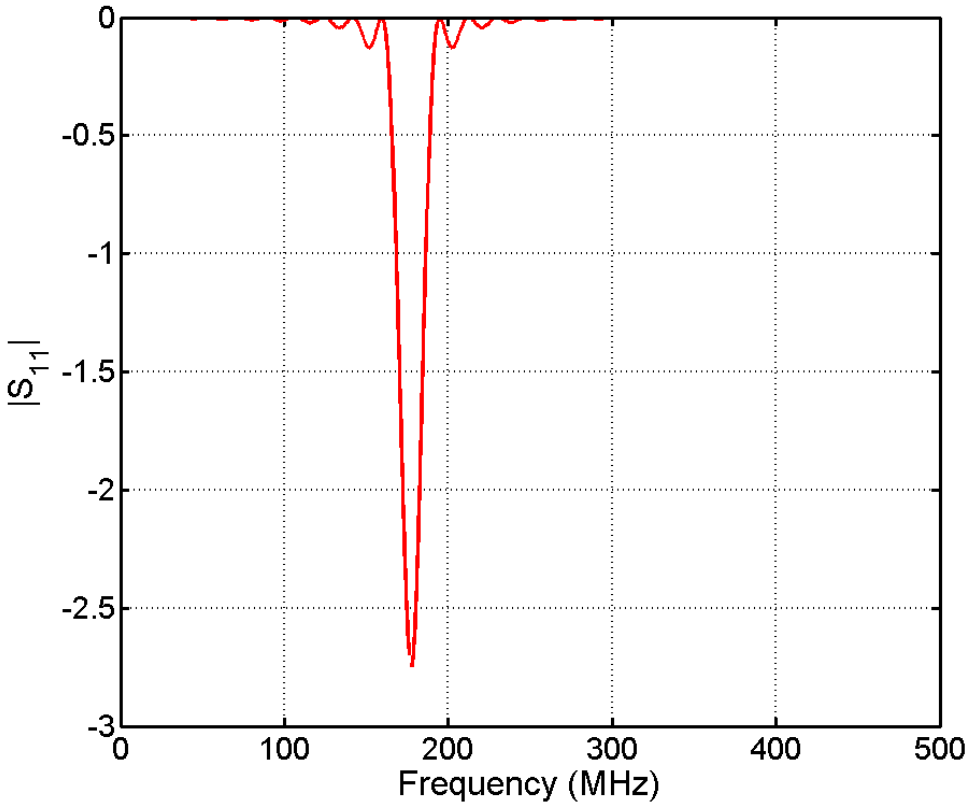

Figure 1.7: S11 for IDT modelled using the electrical equivalent circuit shown in 1.6

While this simple model can give some intuition regarding the operation of SAW device, this model does not consider effects such as reflections and echo of the acoustic waves and the effect of the finite mass and stiffness of the IDT. More realistic models can be formulated utilizing finite element modelling softwares like ANSYS or COMSOL Multiphysics. A setup for modelling two port SAW device is shown in Fig. 1.8 [17]. In addition to the electromechanical modelling at the interface between the driver circuit and the IDT, for locomotion, the interaction between the surface waves and the medium surrounding it should also be modelled to quantify the coupling efficiency of the device. Modelling of SAW device and its mechanical coupling is beyond the scope of this work.

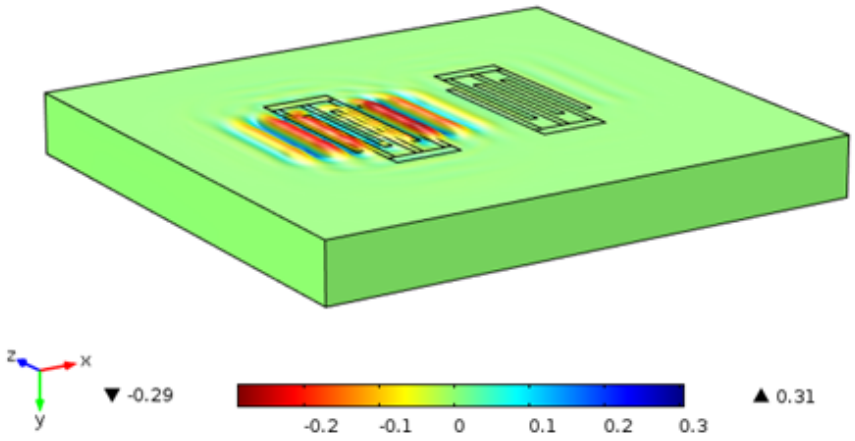

Figure 1.8: Modelling SAW device in COMSOL [17]. Color gradient shows the displacement in nm along the y direction when the transmitter IDT is excited by a sinusoidal voltage.

2. SYSTEM CONSIDERATIONS FOR LOCOMOTIVE IC

While the locomotive ICs described in [3] and [5], demonstrated very different locomotion mechanism, both had a few similarities in their underlying system architectures. In this chapter, the various design considerations to architect a locomotive system are discussed.

2.1 Powering Locomotive ICs

In the design of a locomotive IC (LIC), one of the first items to consider is the choice of power supply for such LICs. Unlike a typical IC, which is soldered on to a PCB, an LIC by its very nature is untethered. As such, a reliable mechanism to power the LIC is a primary consideration. An obvious choice is to use a battery cell to power the LIC. Unfortunately, the use of a battery restricts the miniaturization of the system. With batteries, there is an inherent trade-off between the size and storage capacity, both of which are critical parameters in an application like implantable biomedical devices. Both the works described in [3] and [5] relies on external magnetic/electromagnetic fields to power their devices. While near field WPT offer high efficiencies, such systems have limited range. Radiative WPT on the other hand have longer range but suffers from lower efficiency. As of now, near field WPT is the more prevalent choice for WPT to implantable biomedical devices. Alternatively, energy harvesting circuits can be potentially used. For example, a biomedical implant can be potentially powered by vibration [18].

Extensive literature is available that describes the effective wireless power transfer through biological tissue as depicted in Fig. 2.1. [19] shows that using a lower frequency of 4MHz for inductive wireless power transfer through biological medium results in very little tissue loss. [20] concludes that for a cortical implant electromag-

netic energy transfer is optimum at 20MHz. More recently, [21] and [22] presents the analysis techniques for radiative power transfer into biomedical implants and concludes that the optimum frequency is from sub-GHz to low-GHz range depending on the dimensions of the transmit antenna. [23] generalizes the results of other works and presents a closed form analytical solution to analyse efficiency of near field/inductive wireless power transfer through any medium. Additionally, [23], [24] discusses various cases involving wireless power transfer between planar PCB transmitter coil and PCB as well as on-chip planar receiver coils in the presence of biological medium as well as air and shows that the optimum coils for biological and on-chip applications tend to have only two or fewer number of turns and the optimum frequency for on-chip receiver is close to 100MHz.

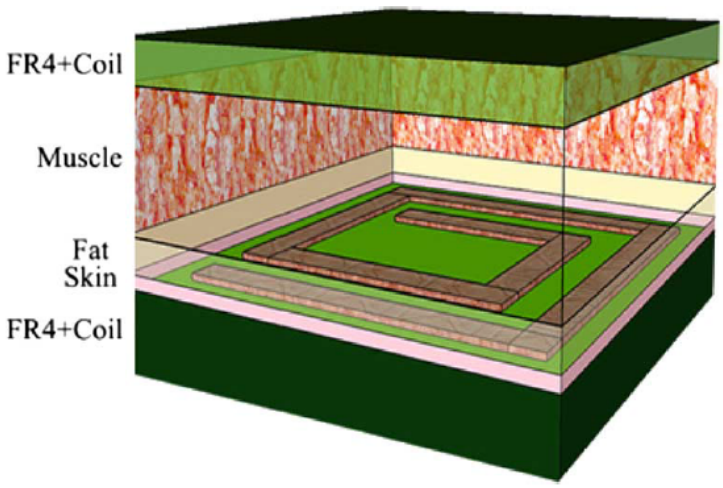

Figure 2.1: Biological medium between two coils [23]

The radiative WPT system demonstrated in [3] achieved an efficiency of -36dB at 5cm separation between transmitter and receiver antenna. This means that if 2W of power is transmitted, 500μ W will be received. With a rectifier efficiency of 55%, this translates to a usable power of close to 250μW for the locomotive implant. The near field/inductive WPT system demonstrated in [5] on the other hand showed an efficiency that decreased as distance between transmitter and receiver coils were swept from 0.5cm to 2.5cm as shown in Fig. 2.2. At 0.5cm, the measured efficiency of WPT was 15%. This means that for a transmitter power of 2W, 300mW of power is available at the receiver. From these numbers, it is evident that radiative WPT systems offer better range than inductive WPT. But unfortunately, the usable voltage generated across the receiver antenna in a radiative WPT scheme is considerably lower than in an inductive WPT and therefore requires a more complex charge pump based rectifier topology as shown in Fig. 2.3(b). Dickson chargepump based rectfier topologies have been proposed in [25] and [26]. [3] used a multistage rectifier topology as shown in Fig. 2.3(c). A similar circuit design was also adopted in [33]

It can be seen from Fig. 2.2, the measured efficiency 15% is significantly lower than the simulated efficiency of 26%. This was because [5] relied on on-chip receiver coil which has significantly lower Q (quality factor). The measured Q was only half that of the simulated Q for the on-chip receiver coil. Based on simulations, it was evident that using an on-chip receiver coil may not be the best solution of delivering large receiver power. On the other hand, with a larger area for flux coupling and very high Q, PCB based receiver coils are better suited for WPT. Therefore, for this project a PCB based receiver coil was employed to power the locomotive system.

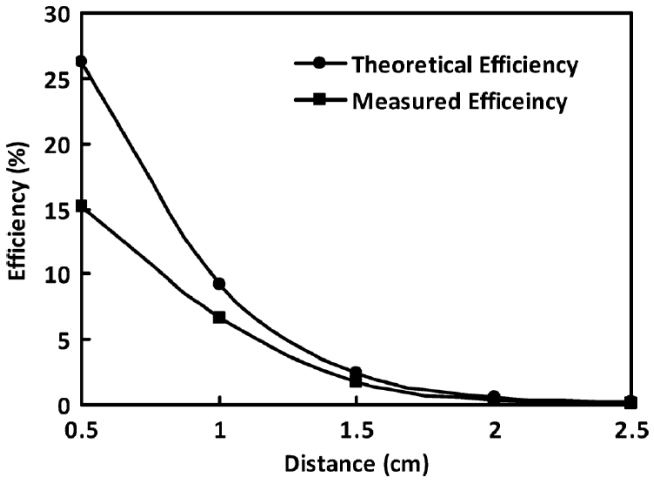

Figure 2.2: Efficieny of WPT as a function of the distance between coils [5]

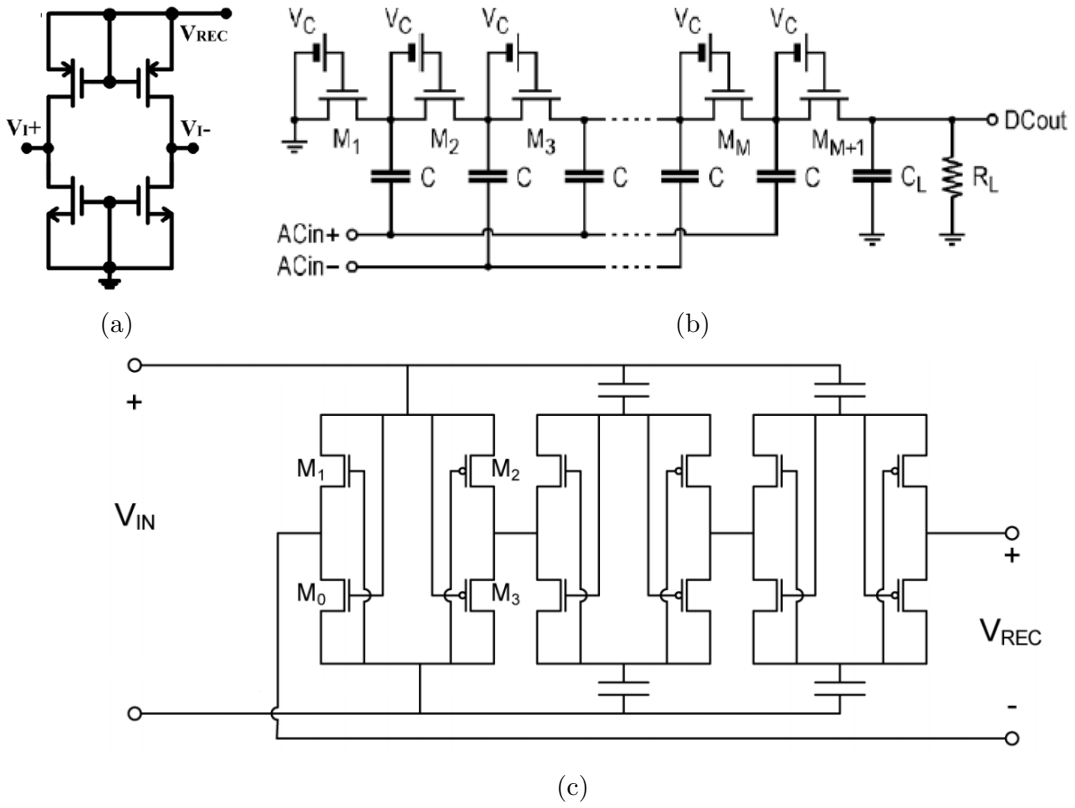

Figure 2.3: (a) Diode connected CMOS rectifier used in [5] (b) Dickson chargepump based rectifier with threshold compensation shown conceptually (c) Synchronous self driven rectifier used in [3]

2.2 System Architecture

A typical locomotive system architecture is shown in Fig. 2.4. A receiver coil is employed for harvesting magnetic/non radiative energy transmitted by an external transmitter coil. The AC voltage across this receiver coil is then converted to a DC voltage using a rectifier. This rectified output voltage is an unregulated supply since it is a function of the distance between the transmitter and receiver coils. A reference circuit (usually a bandgap circuit) generates a supply independent reference voltage that can then be used to generate a regulated supply, using a regulator circuit, which power the rest of the IC including the propulsion mechanism.

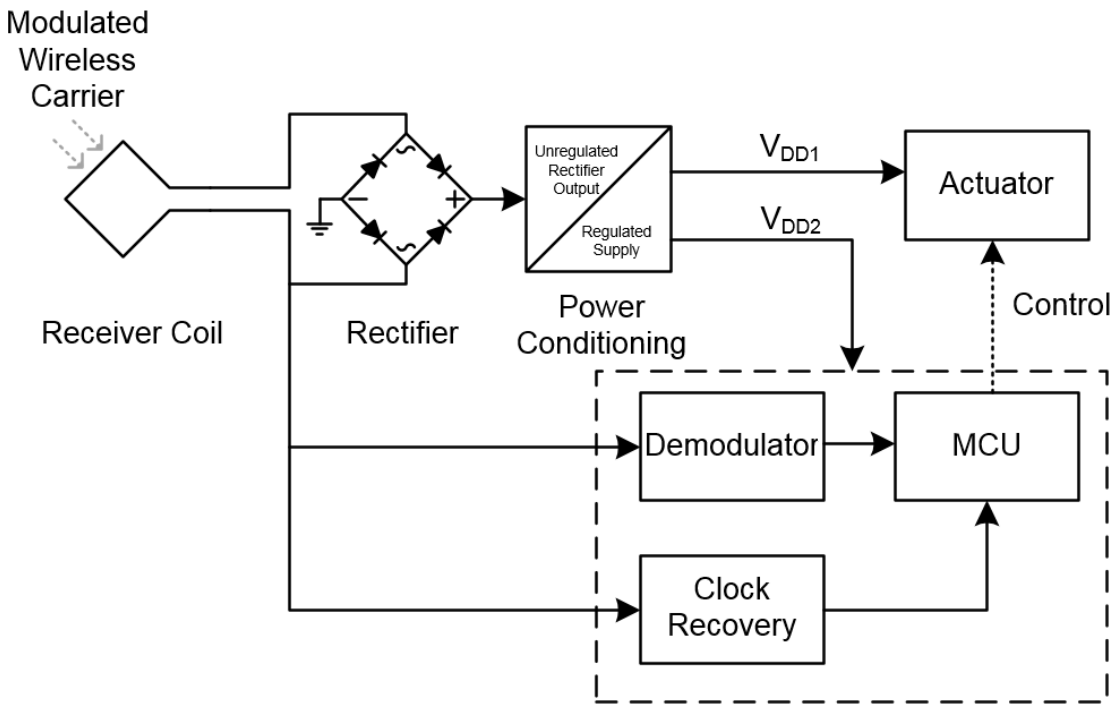

Figure 2.4: System Architecture for a typical LIC

2.3 Direction Control and Communication

Both the locomotive systems presented in [3] and [5] employed mechanisms to control direction. For example, [5] which employed electrolytic bubble based propulsion, had four electrodes along the four edges of the IC. By selectively activating one or more of the electrodes, controlled navigation along all directions in two dimensions can be achieved. Since the system is completely isolated except for the WPT signal, some form of wireless communication scheme needs to be implemented that can be used to send control signals to the locomotive system. This is accomplished by modulating the carrier signal used for WPT. By recovering the modulating signal from the carrier using a demodulator circuit, the bits for navigation control can be recovered.

Due to the constrained dimensions of the overall system, no energy storage elements can be used to store power in the LIC. As a result, the LIC will have to continuously harvest wireless energy in real time. This means that communication scheme employed, which typically uses the same link for data and power transfer, should not impact the power transfer efficiency at any time. In the context, phase and frequency modulation schemes looks attractive since both of them operate with a constant carrier amplitude and hence do not impact the power transfer efficiency. Unfortunately, these modulation schemes requires circuits like phase/frequency locked loop in the receiver, which increases the power consumption considerably. This is a problem in locomotive systems that are powered wirelessly. On the other hand, even though amplitude modulation results in degradation of carrier power, it does not require any clock synchronisation at the receiver and so the demodulator circuit consumes less power. The impact on duty cycle is minimized by employing a low modulation depth. [5] employed a simple amplitude shift keying scheme with modulation depth

of 15%. As shown in Fig. 2.5, the demodulator consisting of an envelope detector, a low pass filter and a cascaded limiting amplifiers realized from inverters did not require a biasing circuit, thereby reducing the system complexity. [3] employed an amplitude shift keying with a minimum of 9% modulation depth and also used pulse width encoding to further reduce impact on carrier power.

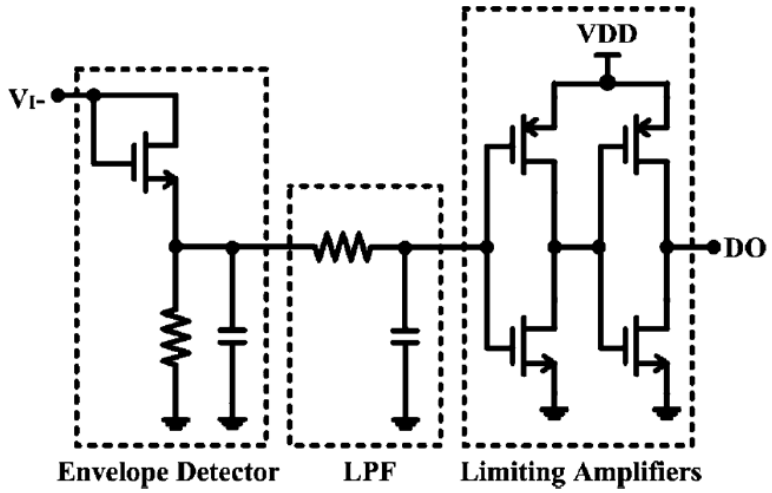

Figure 2.5: Demodulator used in [5]

3. WIRELESS POWER TRANSFER *

In this chapter, the need for resonant coupled magnetic power transfer is motivated and the optimum type of resonance in the transmitter and receiver coils that provides maximum efficiency of power transfer are discussed.

3.1 Introduction

Any change in the magnetic flux through a coil of wire induces a voltage across it. The simplest WPT scheme consists of two coils as shown in Fig. 3.1(a). The source V_G sets up an alternating current through the transmitter coil (inductance) L_T which in turn creates a time varying magnetic field around it. A portion of this magnetic flux is coupled into the receiver coil L_R which is in the vicinity of the transmitter coil. This coupled flux induces a voltage across the receiver coil and delivers power to the load R_L. In principle, such a scheme closely resembles a transformer with a key difference that the coupling efficiency between coils is quite low in a WPT system owing to the larger distance separating the two coils.

Using Biot-Savart law, it can be shown that the magnetic field at a distance z along the centre line of a coil of radius R carrying a current I is described by

$$B_z = \frac{\mu_0}{4\pi} \frac{2\pi R^2 I}{(z^2 + R^2)^{3/2}} \tag{3.1}$$

From this expression, it is evident that in order to maximize magnetic field generated by a given coil at a given distance, the current through the coil needs to be maximized.

Now consider the WPT system shown in Fig. 3.1(a). Assuming weak coupling

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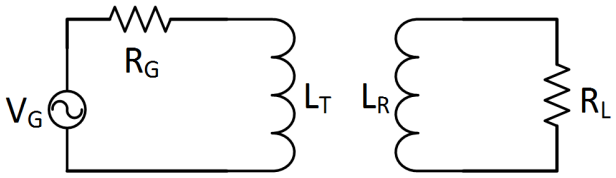
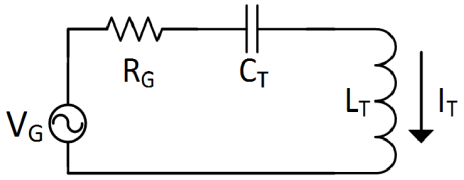


(a)



(b)

Figure 3.1: (a) A simple two-coil WPT system (R_G models the source impedance) (b) Transmitter coil in resonance

between the two coils, the current through the transmitter coil can be given by

$$I_T = \frac{V_G}{R_G + Z_T}, \tag{3.2}$$

where Z_T is the impedance offered by transmitter coil. Z_T can be modelled as a coil inductance $j\omega L_T$ in series with an equivalent series resistance (ESR) of the coil, R_T. Therefore, the current through the transmitter coil is

$$I_T = \frac{V_G}{R_G + R_T + j\omega L_T}. \tag{3.3}$$

In Fig. 3.1(a) the transmitter coil current, and hence the magnetic flux generated by the transmitter coil, is dependant on the impedance (and ESR) of the coil at the frequency of operation of the WPT system. This dependence of the magnetic flux generated by the transmitter coil (and so, of the WPT efficiency) on the coil impedance can be easily removed by introducing resonance. Consider a capacitor in

series with the transmitter coil as shown in Fig. 3.1(b). Then, the current through the coil becomes

$$I_T = \frac{V_G}{R_G + R_T + j\omega L_T - \frac{j}{\omega C_T}}. \tag{3.4}$$

Now, if the source frequency is chosen to be $\omega_0 = \frac{1}{\sqrt{L_T C_T}}$, then the inductive and capacitive reactances cancel out, maximizing the magnitude of current I_T as

$$I_{T,max} = \frac{V_G}{R_G + R_T};\ if\ \omega_0 = \frac{1}{\sqrt{L_T C_T}}. \tag{3.5}$$

This, in turn, maximizes the magnetic field generated by the coil and hence the efficiency of coupling as well.

Having established the motivation to have the transmitter coil in resonance, the next logical step is to enquire if resonance in the receiver coil can benefit the WPT system. Moreover, the possibility of employing a parallel resonance (capacitor in shunt with the coil) in place of the series resonance described above can be investigated. The aim of the following analysis will be to determine whether one resonance configuration is better than the other for a given pair of coils.

3.2 Analysis of Coil Coupling in a WPT system

In the following subsections, a comparison of the WPT performance with series and parallel resonances at transmitter and receiver coils is made. A coil is said to be in series resonance when the capacitor resonating with the coil is in series with it. Similarly, for the coil to be in parallel resonance, the capacitor is in shunt with it. In a real WPT system, the transmitter coil will see an additional load because of the load R_L connected to the receiver coil. Thus the load the the receiver is "reflected" onto the transmitter coil. This reflected load can be shown in series with the transmitter coil and so can be bracketed with R_T shown in Fig. 3.2. In this analysis, a source V_G

driving the transmitter coil is considered to have a source impedance R_G. Assuming Q_T to be the quality factor of the transmitter coil, the ESR of the transmitter coils is $R_T = Q_T \omega L_T$.

3.2.1 Series Versus Parallel Resonance at Transmitter

The transmitter coil can be configured with series or shunt capacitors as shown in Fig. 3.2(a) and Fig. 3.2(b) respectively. From the previous section it was concluded that efficiency of WPT can be maximized for a given transmitter coil and a given distance of seperation between the coils by maximizing the magnitude of alternating current through the coil.

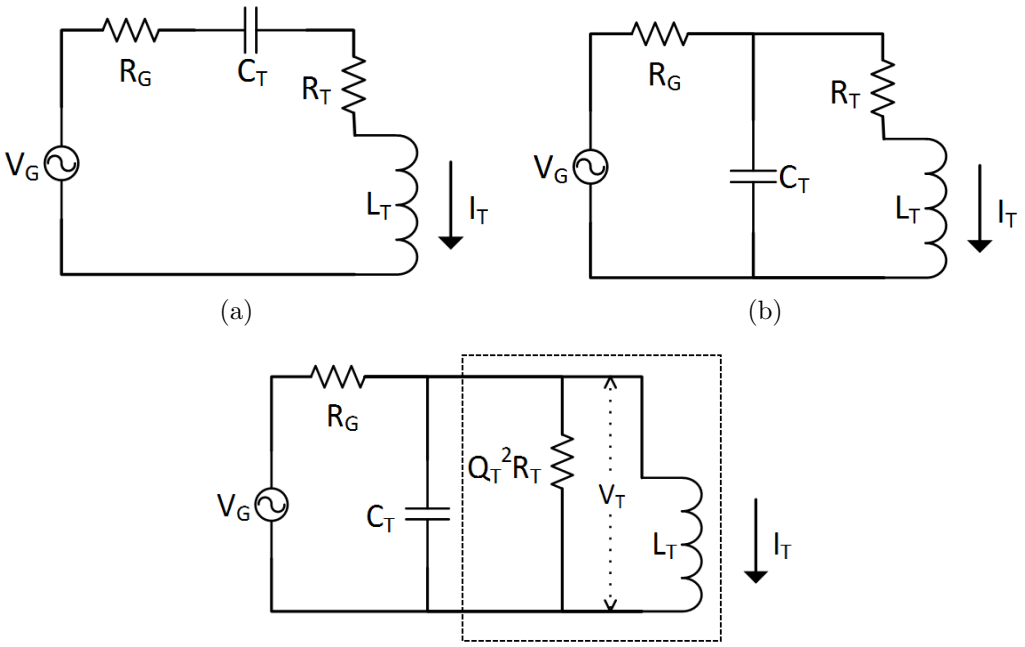


Figure 3.2: Transmitter coil in (a) series resonance and (b) parallel resonance. (c) depicts the circuit in (b) after narrowband impedance transformation.

In the series resonance configuration shown in Fig. 3.2(a), the current through the coil is given by (3.5) as derived in the previous section. Now, if the transmitter coil was considered to be high-Q, then the ESR of the coil will be very small and the current through the coil can be approximated as

$$I_{Tseries} \approx \frac{V_G}{R_G};\ if\ R_G \gg R_T. \tag{3.6}$$

To analyse the parallel resonance configuration shown in Fig. 3.2(b), a narrowband impedance transformation can be applied as shown in Fig. 3.2(c). This transformation of the circuit is justified since the source V_G is driving the circuit at frequency ω_0. For this circuit, at resonance, the admittances of the capacitance C_T and the inductance L_T together add up to zero. That means that the effective impedance seen by the driver consists of just the resistance $Q_T^2 R_T$. So at resonance, the voltage across this resistance $Q_T^2 R_T$ can be derived as

$$V_T = \frac{Q_T^2 R_T}{R_G + Q_T^2 R_T} V_G \approx V_G;\ if\ R_G \ll Q_T^2 R_T. \tag{3.7}$$

If the transmitter coil was considered to have very high-Q, then $Q_T^2 R_T$ will be much larger than the driver impedance R_G. Then the current through the coil can be written as

$$I_{Tparallel} = \frac{V_T}{j\omega_0 L} \approx \frac{V_G}{j\omega_0 L};\ if\ R_G \ll Q_T^2 R_T \tag{3.8}$$

From equations (3.6) and (3.8), it can be observed that the expression for current through the coil at resonance is different for series and parallel resonance configurations. For a given high-Q coil, if the source resistance R_G is greater than the coil impedance $\omega_0 L$, then the magnitude of $I_{Tseries}$ will be smaller than the magnitude of $I_{Tparallel}$ and so the parallel configuration is preferred. On the other hand, if the

source resistance R_G is lower than the coil impedance $\omega_0 L$, then $I_{Tseries}$ will have a larger magnitude than $I_{Tparallel}$ and using series configuration is more efficient for WPT.

Note that the assumption of a high-Q transmitter coil was invoked in the above derivation. As typical biomedical applications employ a PCB transmitter coils which can provide very high Q, this assumption is justified. Generally, reflected load seen at the transmitter coil due to the load R_L at receiver can be approximated as $k^2 \frac{L_T}{L_R} R_L$ [27]. Since the coupling coefficient $k \ll 1$, and assuming moderate to low load R_L at the receiver, this reflected load at the transmitter can be neglected.

3.2.2 Series Versus Parallel Resonance at Receiver

The two resonance configurations at the receiver coil is compared in this section. The voltage that couples into the receiver coil can be modelled as a voltage source V_I in series with the receiver coil. The following analysis compares the power delivered to the load R_L connected at the receiver coil for a given induced voltage V_I at the receiver coil, for the two configurations shown in Fig. 3.3(a) and Fig. 3.3(b). The equivalent series resistance of the receiver coil is represented by the resistance R_R in Fig. 3.3.

Consider the series resonance configuration as shown in Fig. 3.3(a). The current through the load R_L is given by

$$I_{Lseries} = \frac{V_I}{R_L + R_R + j\omega L_R - \frac{j}{\omega C_R}} \tag{3.9a}$$

$$\implies I_{Lseries} = \frac{V_I}{R_L + R_R};\ if\ \omega_0 = \frac{1}{\sqrt{L_R C_R}}. \tag{3.9b}$$

Now, consider the parallel resonance configuration as shown in Fig. 3.3(b). At

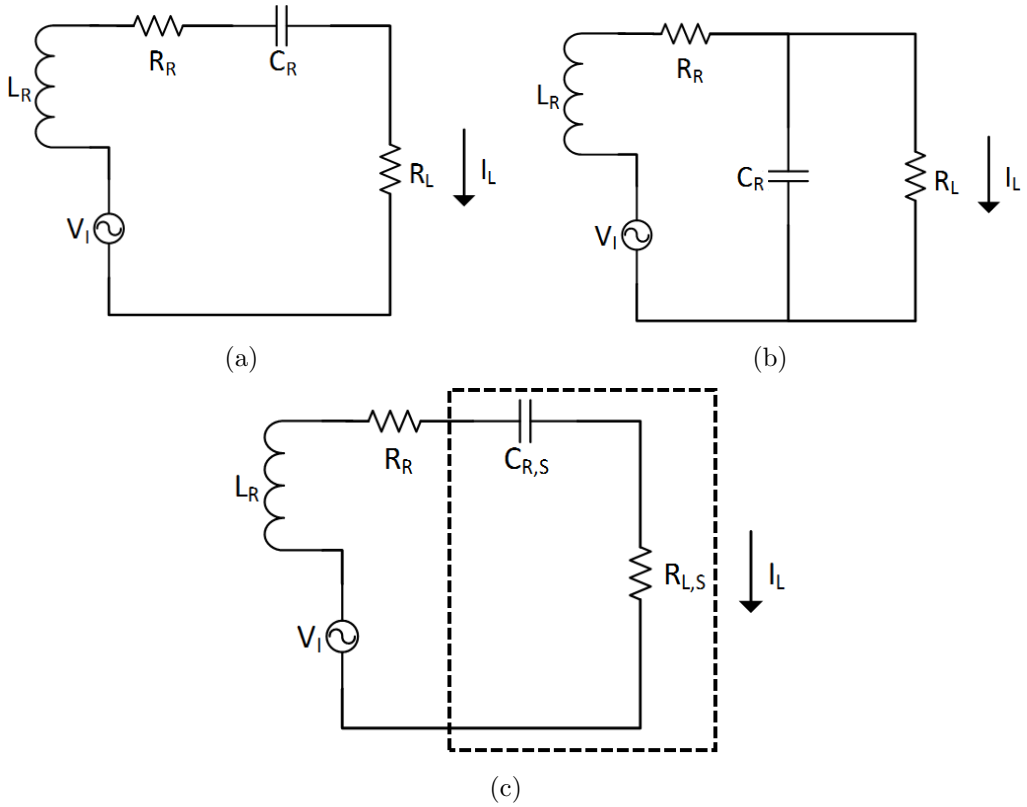


Figure 3.3: Receiver coil in (a) series resonance and (b) parallel resonance. (c) depicts the circuit in (b) after narrowband impedance transformation.

resonance frequency ω_0, a quality factor Q_R is defined as

$$Q_R = \omega_0 C_R R_L. \tag{3.10}$$

Q_R helps transform the parallel impedances of R_L and C_R shown in Fig. 3.3(b) to a series arrangement of $R_{L,S}$ and $C_{R,S}$ as shown in Fig. 3.3(c) through a narrowband impedance transformation. The equivalent series capacitance $C_{R,S}$ and the equivalent load resistance $R_{L,S}$ in Fig. 3.3(c) is related to C_R and R_L in Fig. 3.3(b) by

$$C_{R,S} = \frac{Q_R^2 + 1}{Q_R^2} C_R, \ \& \tag{3.11a}$$

$$R_{L,S} = \frac{R_L}{Q_R^2 + 1}. \tag{3.11b}$$

Note that the effective load seen by the coil has now decreased by a factor of $Q_R^2 + 1$ when compared to the series resonance configuration. For this transformed circuit, the current through the equivalent load $R_{L,S}$ is

$$I_{Lparallel} = \frac{V_I}{R_{L,S} + R_R + j\omega L_R - \dfrac{j}{\omega C_{R,S}}}, \tag{3.12a}$$

$$\implies I_{Lparallel} = \frac{V_I}{R_{L,S} + R_R};\ if\ \omega_0 = \frac{1}{\sqrt{L_R C_{R,S}}}. \tag{3.12b}$$

Notice that the resonance frequency ω_0 is not exactly the same as the condition derived in (3.9b) for the series resonance configuration. The resonance frequencies in these two cases are equal only if $Q_R \gg 1$. But unlike the assumption made on the quality factor Q_T of the transmitter coil, Q_R may not always be greater than 1.

The power delivered to the load at resonance in the two configurations are

$$P_{series} = I_{Lseries}^2 R_L \tag{3.13a}$$

$$P_{parallel} = I_{Lparallel}^2 R_{L,S} \tag{3.13b}$$

Assuming the receiver coil to be high-Q (not to be confused with Q_R of considered in the derivation of $I_{Lparallel}$) then, the ESR of the receiver coil is much smaller than the load. That is, $R_R \ll R_L$ and $R_R \ll R_{L,S}$. Under this condition, substituting for currents in expressions (3.13) from (3.9b) and (3.12b), the power delivered to the load in the two configurations are

$$P_{series} = \frac{V_I^2}{R_L} \tag{3.14a}$$

$$P_{Parallel} = \frac{V_I^2}{R_{L,S}}. \tag{3.14b}$$

Since $R_{L,S} < R_L$, the power delivered will be more in the parallel resonance configuration.

Revisiting the expressions for load current in series and parallel resonances ((3.9a) and (3.12a)), it can be observed that if the load resistances $R_L \gg \omega L$, then there is no benefit of having a capacitance cancel out the $j\omega L$ term. This is because the magnitude of the load current is going to be dominated by R_L. Typically, in any application, the load R_L is usually a rectifier circuit which can be modelled as a resistance and a capacitance in series. Hence even in the absence of an explicit capacitance C_R in Fig. 3.3(a), it is still possible to have cancellation of $j\omega L$ term. It may be possible that the $\frac{-j}{\omega C}$ term introduced by the rectifier load can dominate over $j\omega L$ of the coil. In such a case, the WPT system is best served by redesigning the coil such that $j\omega L$ term matches $\frac{-j}{\omega C}$ at $\omega = \omega_0$.

In a typical application in biomedical implants, the receiver coil can be an on-chip integrated inductor. The Q of such on-chip inductor is significantly lower than the Q of a PCB inductor. In this case, the optimum resonance configuration is determined by the relative values of $R_{L,S}$, R_L and R_R.

3.3 Experimental Results

To explore the analysis made in the previous section, a WPT system involving a PCB coil transmitting power to an on-chip integrated coil was considered. Coil dimensions from [23], summarized in Table 3.1, were utilized with a 5mm separation in air. Fig. 3.5 shows the setup in ANSYS HFSS used to simulate coupling between a PCB based transmitter coil and an on-chip receiver coil. A two-port model of the coil coupling was obtained from HFSS, which was then plugged into a circuit simulator (Cadence Virtuoso) as shown in Fig. 3.6 to simulate the various resonance configurations discussed in the previous section. Choosing the resonant frequency to be 100MHz and based on the inductance of the coils extracted from HFSS simulations, the resonance capacitances C_T and C_R were chosen to be 204pF and 265pF respectively. Fig. 3.4 shows the on-chip coil structure used in HFSS simulation.

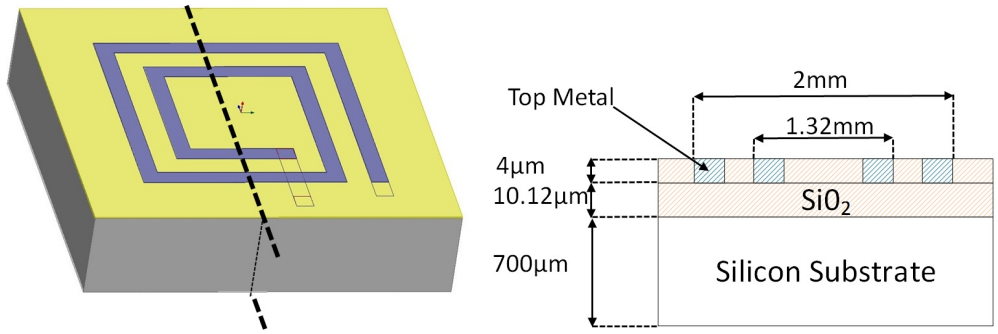


Figure 3.4: (a) Integrated (on-chip) coil model used in HFSS. (b) shows the cross section of (a) along the dotted line

The transmitting PCB coil was simulated to have a quality factor of close to 167 and gives the R_T of around 50mΩ. Now, setting up the on-chip receiver coil with parallel resonance and a load $R_L = 1\text{k}\Omega$, and driving the transmitter through

Table 3.1: Details of the coils

	PCB Coil	On-Chip Coil
Turns	1	2
Outer Diameter (mm)	14	2
Trace Width (μm)	3500	140
Trace Spacing (μm)	500	200
Substrate	1-oz FR-4	0.18μm CMOS
Inductance(nH)	12	9.4
$\|\omega L\|$ (ohm, at 100MHz)	7.5	5.9
Q of coil	167	8
ESR of coil	0.045	0.74
Capacitance(pF)	204	265

R_G= 100mΩ, it can be seen from the plots in Fig. 3.7(a) that series or parallel resonance gives about the same efficiency of around -20dB at 100MHz. On the other hand, when transmitter coil is driven through an R_G= 50Ω, the analysis in the previous section predicts that for the transmitter coil, $I_{Tparallel} \approx \frac{V_G}{j7.5\Omega}$ is greater than $I_{Tseries} = \frac{V_T}{50}$. Therefore the coupling in parallel resonance is expected to be higher than in series resonance configuration. And indeed, it can seen from the simulation plots in Fig. 3.7(b) that parallel resonance offers close to 25dB higher efficiency than series resonance at 100MHz.

Since in any WPT system, the receiver coil generally drives a rectifier, a simple gate-cross coupled rectifier was designed in 0.18 μm CMOS as shown in Fig. 3.8(a) and the resonance configurations at the receiver coil was contrasted with this circuit driving 1kΩ as load. With the transmitter in parallel resonance configuration with $R_G = 50\Omega$, it can be seen from the plots in Fig. 3.8(b) that parallel resonance configuration at the receiver offers close to 20dB higher efficiency at 100MHz when compared to series resonance configuration. This observation is also in concordance

with the predictions made in the analysis presented in the previous section.

To validate the predictions in a real-world setting, a pair of PCB coils described in Table 3.1 was fabricated and WPT efficiencies were measured using a network analyser ($R_G = R_L = 50\Omega$) for cases involving series and parallel resonances at transmitter and receiver coils. From the analysis in the previous section, for the transmitter coil, $I_{Tparallel} \approx \frac{V_G}{j7.5\Omega}$ is greater than $I_{Tseries} = \frac{V_T}{50}$. Therefore parallel resonance is predicted to be better at transmitter coil. Moreover, it was concluded from the analysis that parallel resonance is better at receiver coil as well. As shown in Fig. 3.9, in both transmitter and receiver coils, parallel resonance offers close to 10dB higher performance.

3.4 Summary of Coupling Analysis

Various combinations of resonance configurations can be employed in a inductive WPT system with two coils. The analysis presented in this section shows that in a system with a high-Q transmitter coil driven by a source with significant source impedance, a parallel resonance configuration is preferred at the transmitter coil. Moreover, for a typical system, parallel resonance seems to be more efficient at the receiver coil as well. With the right configuration, the efficiency of WPT can improve by as much as 20dB. Though the analysis neglected the loading seen by the transmitter coil due to the receiver, the trend predicted by the analysis was validated with laboratory measurements on PCB based WPT system.

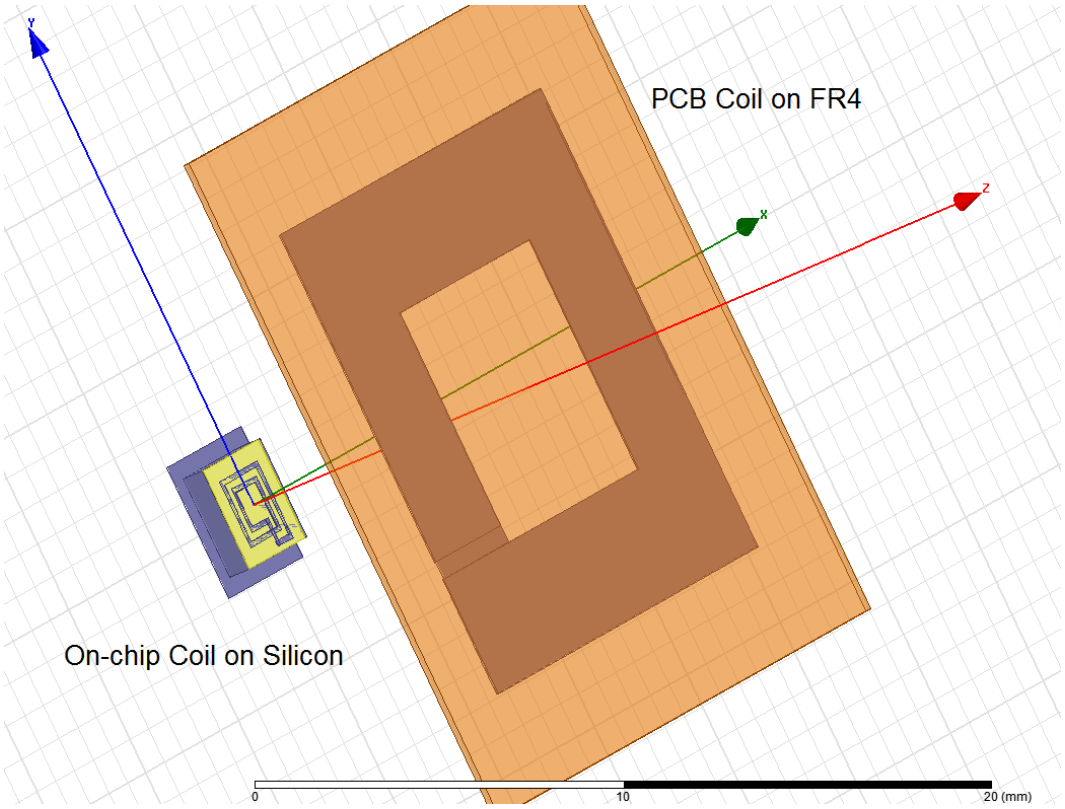


Figure 3.5: Setup in ANSYS HFSS

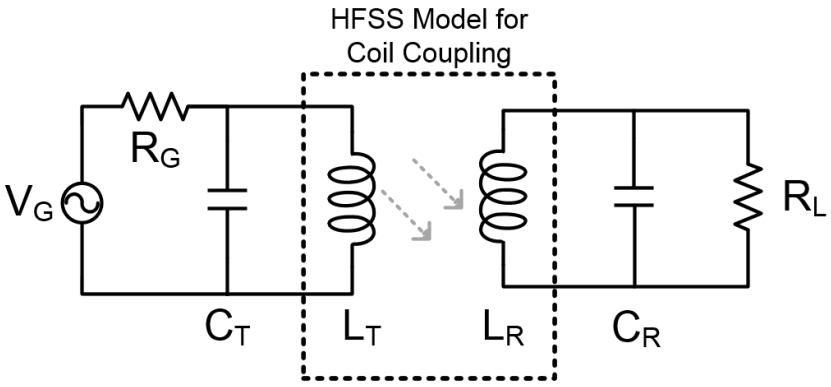
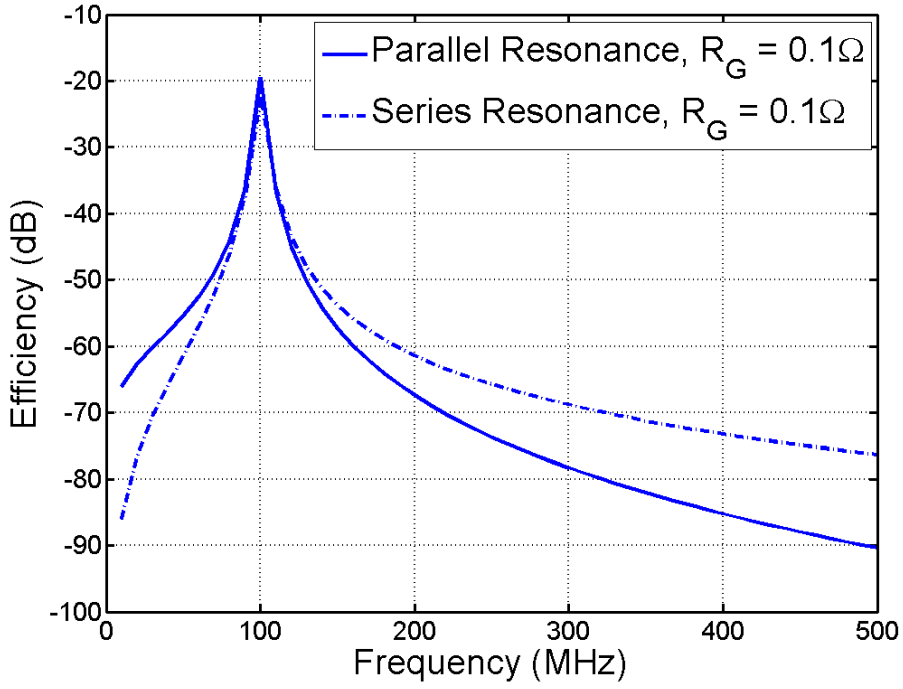
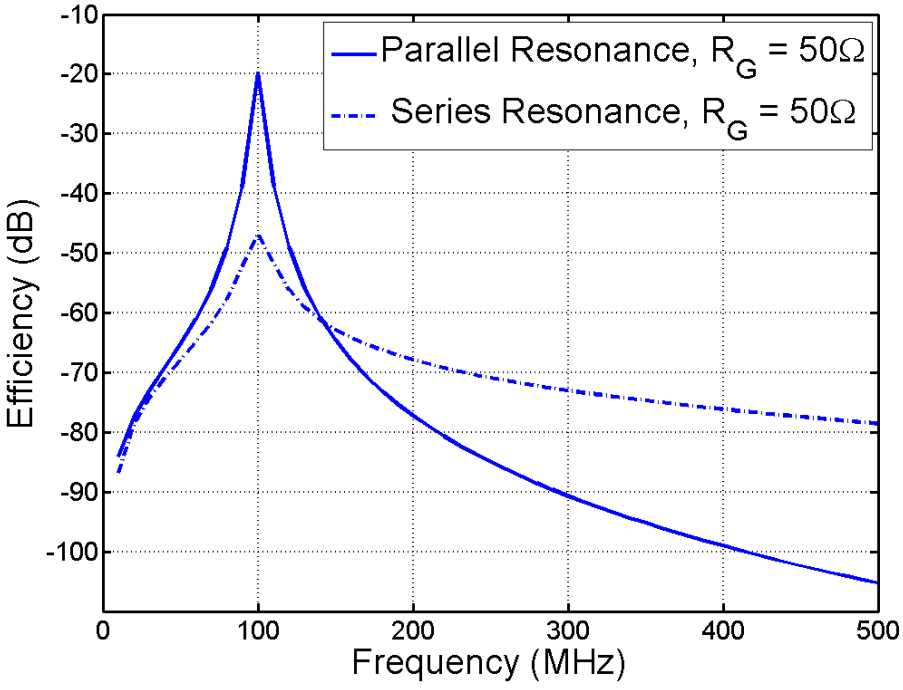


Figure 3.6: Simulation setup for measuring WPT efficency

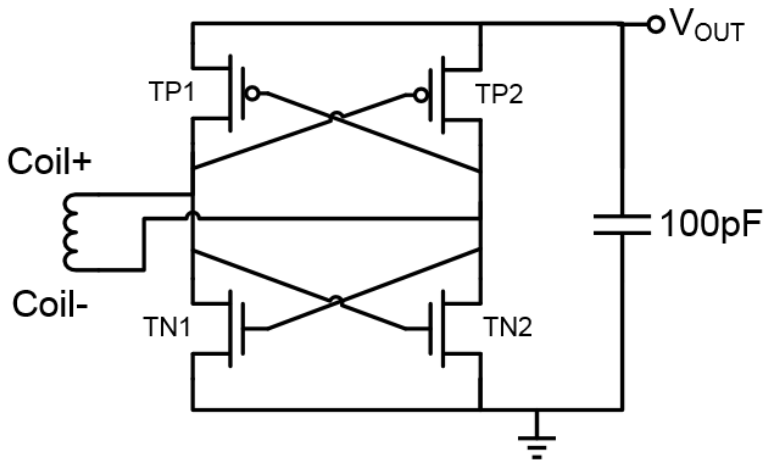


(a)

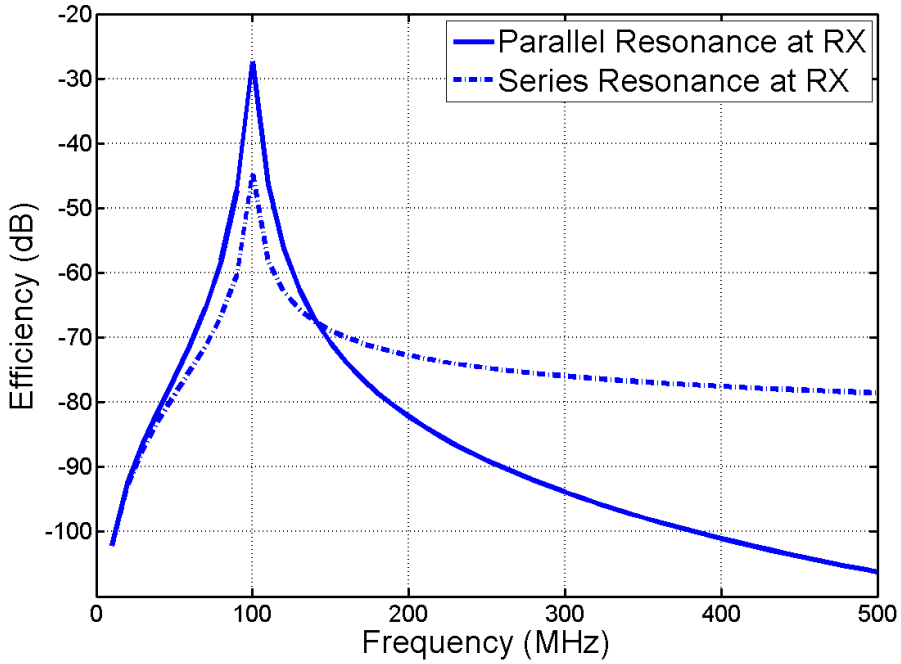


(b)

Figure 3.7: Coupling efficiency with parallel resonance at on-chip receiver coil with R_L= 1kΩ when transmitter coil is driven through (a) $R_G = 100m\Omega$ and (b) $R_G = 50\Omega$.

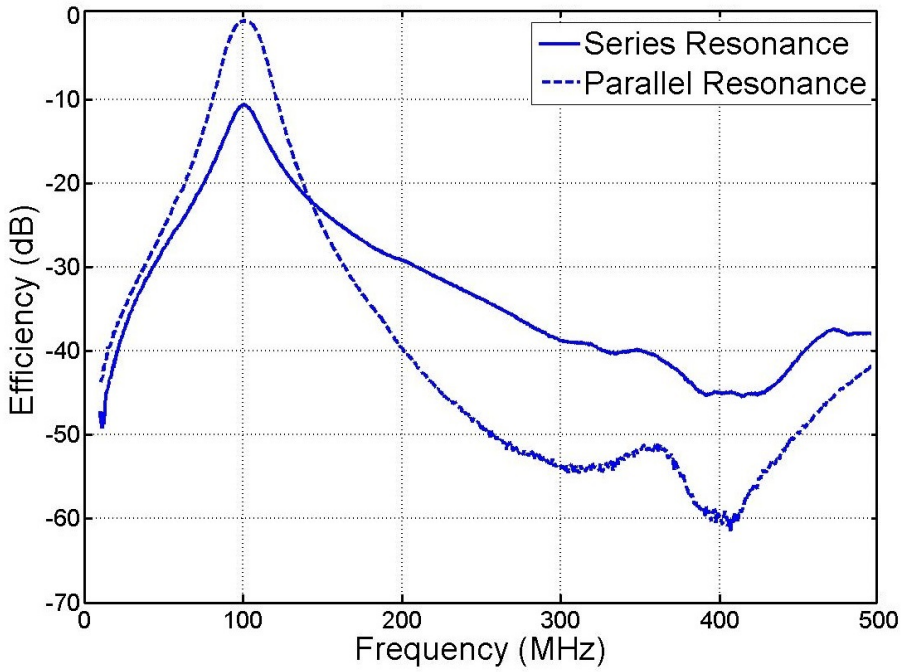


(a)

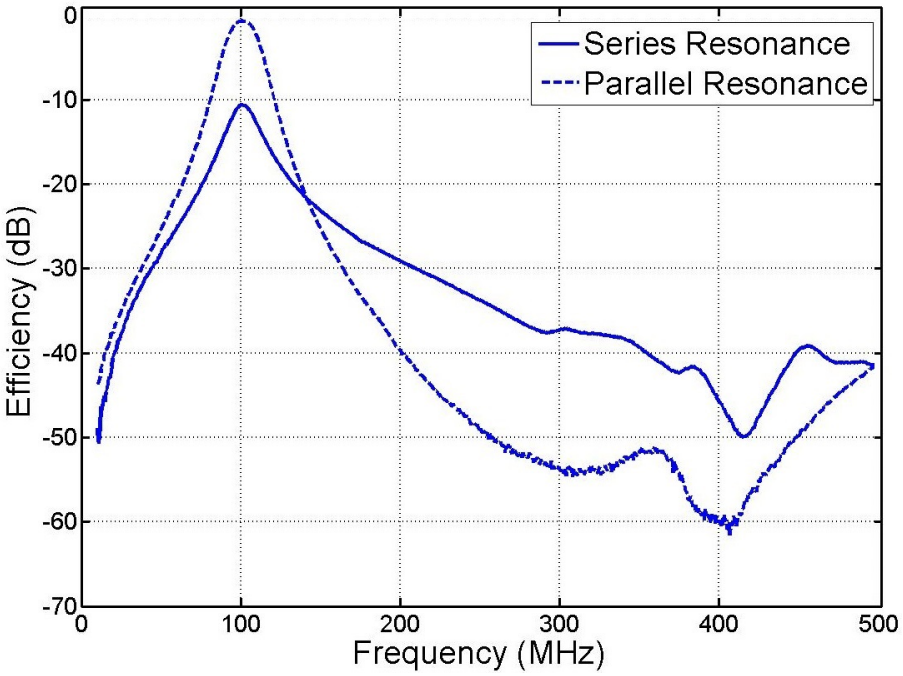


(b)

Figure 3.8: (a) Rectifier Circuit (b) Coupling efficiency with the on-chip receiver coil driving the rectifier.



(a)



(b)

Figure 3.9: Measurement results for PCB based transmitter and receiver coil pair (a) Series versus parallel resonance at transmitter with receiver coil in parallel resonance, and (b) Series versus parallel resonance at receiver with transmitter coil in parallel resonance.

4. BUILDING BLOCKS FOR LOCOMOTIVE IC

In this chapter, the various circuits required to build a wirelessly powered locomotive IC are explored. Fig. 4.1 shows the system block diagram for the locomotive IC system described in this work. As explained in the first chapter, this project focusses on driving a SAW device with a wirelessly powered CMOS front end for potential locomotion. Wireless power delivery is accomplished by means of a pair of PCB based transmitter and receiver coils. A PLL is used to generate the signal to drive the SAW device.

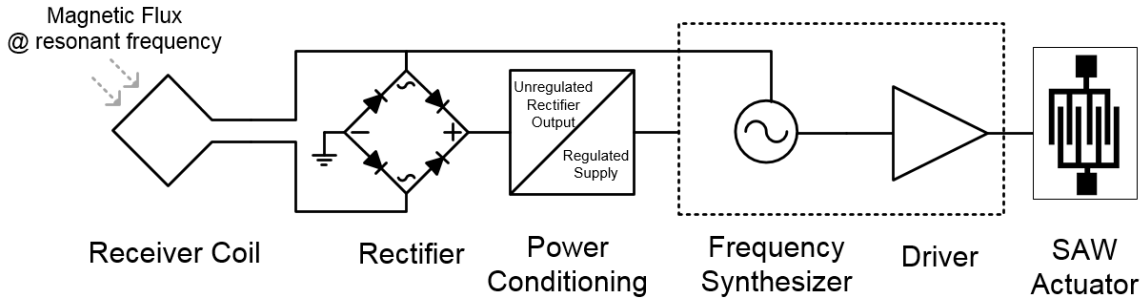


Figure 4.1: LIC System Architecture

One of the most important design constraint for this project is to minimize the power consumption of all circuit blocks in the system. Additionally, since the rectifier output drops as the distance between the transmitter and receiver coils increases,in order to maximize the range of operation for the wireless power transfer, the circuits need to operate at low supply voltages.

4.1 Power Conditioning Blocks

Wireless power delivered to a reciever coil needs to be recfified and a regulated supply generated to power the PLL frequency synthesizer. The power conditioning signal chain includes a rectifier circuit, a reference generation circuit and a regulator circuit.

4.1.1 Rectifier

The role of the rectifier is to generate the unregulated supply that powers the proposed locomotive system from the alternating voltage across the receiver coil. The simplest form of the full wave rectifier is shown in Fig. 4.2(a). As shown in Fig. 4.2(b), in each of the half cycle, two of the four diodes in the bridge conducts charging the capacitance C_L.

In a typical CMOS process, the diodes can be realized by a diode connected NMOS and PMOS transistors as shown in Fig. 4.3(a). The minimum input swing required in this case is equal to $\Delta V_{min} = V_{th,nmos} + V_{th,pmos}$. The efficiency of such an arrangement is mostly limited by the forward drop offered by the NMOS and PMOS transistors that are conducting in each half cycle. Consequently, the rectified output DC voltage is less from the AC amplitude by atleast $V_{drop} = V_{th,nmos} + V_{th,pmos}$. The V_{drop} can be quite large for low alternating voltage across the input of the rectifier and can contribute to lower efficiency.

One easy way to get around this problem is by replacing the diode connected NMOS and PMOS topologies with a cross coupled CMOS topology as shown in Fig. 4.3(b). While the minimum input swing required in for this circuit is still equal to $\Delta V_{min} = V_{th,nmos} + V_{th,pmos}$, the forward drop is only $\Delta V_{min} = V_{DS,nmos} + V_{SD,pmos}$, which is considerably less compared to the previous circuit.

Unfortunately, this topology suffers from reduced efficincy due to reverse currents.

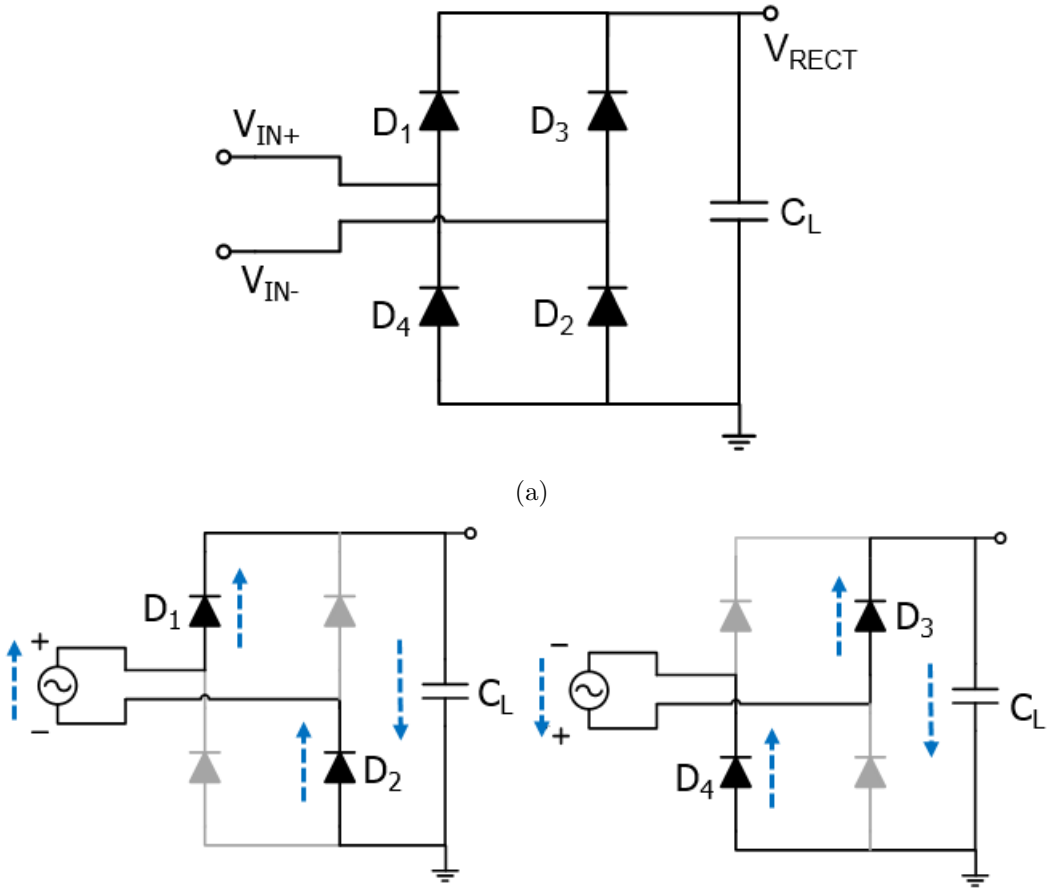


Figure 4.2: (a) Simple full wave rectifier (b) Operation of a full wave rectifier. The dotted blue arrows indicates the direction of current

Consider an input voltage ΔV_{IN} is applied to the input of the gate cross coupled CMOS rectifier shown in Fig. 4.3(b). When ΔV_{IN} is very high, gate induced drain leakage (GIDL) can occur which results in the capacitance C_L losing its charge and thus lowering rectifier efficiency. GIDL occurs when a large gate to drain voltage exists in a transistor which is OFF.

When ΔV_{IN} is small, there is another mechanism by which the load capacitor can discharge. Consider a sinusoid input to the rectifier with a swing of amplitude

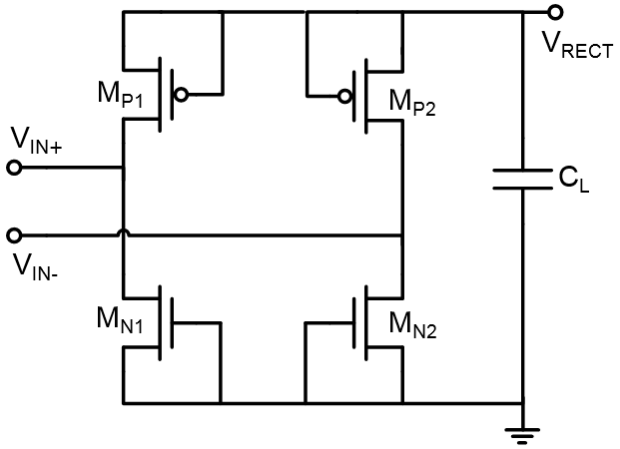
$\Delta V_{IN} = V_{IN+} - V_{IN-} = 1V$. Consider that the rectifier output is 0.8V obtained by one of the PMOS and one of NMOS transistors turning ON in each half cycle. As shown in Fig. 4.4(a), under normal operations, as the input swings from one extreme of amplitude to the other polarity one of the transistors M_{P1} and M_{P2} is conducting and the other is OFF. Now as the input swings, there is a phase when ΔV_{IN} is momentarily zero. Then, as shown in Fig. 4.4(b), the role of source and drain reverses and the transistors turn ON, leading to the capacitance C_L discharging thus reducing the efficiency.

Various techniques have been proposed in literature to improve rectifier efficiency. These techniques includes using active diodes that provide current direction control as demonstrated in [28] and [29] or using bootstrapped capacitances to cancel V_{th} of the transistors as demonstrated in [30] and [31]. While active diodes serves to improve efficiency for low frequencies (less than 40MHz), at higher frequencies, bootstrapping techniques are preferred. This is because at higher frequencies, the efficiency of the rectifier is limited by the delay in the active diode comparator. [32] gives a good summary of all the various techniques to improve the efficiency of the rectifier.

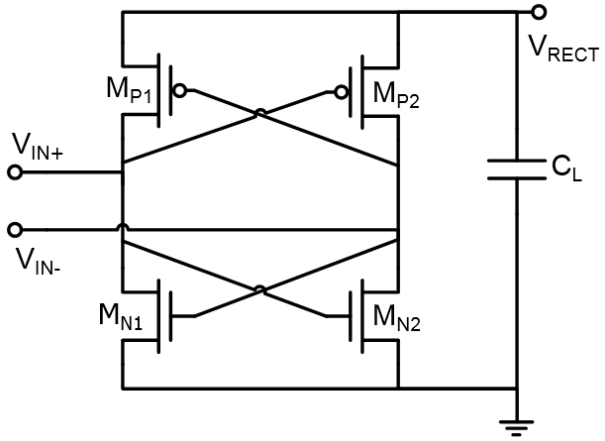
In this project, a simple gate cross coupled CMOS rectifier as shown in Fig. 4.3(b) was implemented. The table 4.6 shows the dimensions of the transistors used in the rectifier. The load capacitance was chosen to minimize the ripple observed on the rectifier output while driving a load resistance. Ideally, a large load capacitance benefits from reduced ripple, but in this project the use of an integrated capacitance means that the maximum capacitance that can be used was restricted by the area available in the layout budgeted for the rectifier circuit.

Table 4.1: Sizing of transistors for rectifier

Reference Designator	W	L	Fingers
M_{P1}, M_{P2}	15μ m	180nm	48
M_{P1}, M_{P2}	6μ m	180nm	48

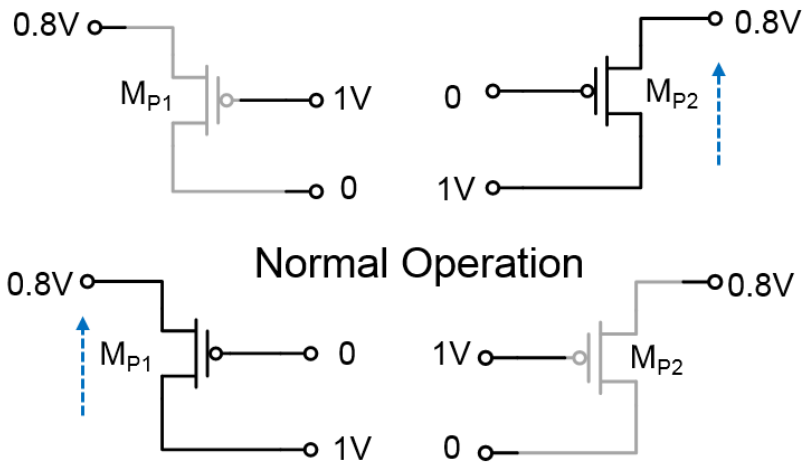


(a)

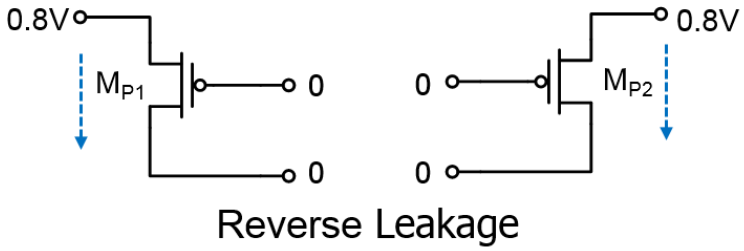


(b)

Figure 4.3: (a) CMOS rectifier realized using diode connected transistors (b) Gate cross-coupled CMOS rectifier



(a)



(b)

Figure 4.4: Operation of PMOS transistors in gate cross coupled CMOS rectifier with 1V sinusoid input and 0.8V rectified output (a) at extremes of input swings (b) when input polarity shifts (Note:dotted blue arrow indicates the direction of current)

4.1.2 Regulator

Since the rectifier output is unregulated and depends on the distance between the coils used for wireless power delivery, there should be a circuit that provides a steady power supply to guarantee the performance of the PLL frequency synthesizer. This requirement is achieved in this project by means of a LDO as shown in figure 4.5. The LDO circuit operates by using negative feedback to fix the potential across the resistor R_2 as equal to a potential V_{REF} so that the current through that resistance is $I = \frac{V_{REF}}{R_2}$. Now by Kirchoff's current law, the current through the resistance R_1 and R_2 are equal. Therefore the potential drop across the resistance R_1 is equal to $R_1 \times I$ or $R_1 \frac{V_{REF}}{R_2}$. Therefore, the output potential is

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) V_{REF}. \tag{4.1}$$

Tables 4.2 and 4.3 shows the details of the transistors and passives used in this circuit. The single stage amplifiers used in the regulator circuit was designed for a tail current of 5.2μA to obtain a gain of 35dB with a power supply of 1.1V. The DC loop gain of the regulator was 55dB with a dominant pole compensation at the V_{REG} output node. The phase margin for regulator is 55^o from simulations for the minimum supply of 1.1V.

Fig. 4.7 shows the power supply ripple rejection performance of the regulator circuit with a supply of 1.2V and with a load $R_L = 1k\Omega$. As shown in the figure, the ripple rejection if -14dB at 100MHz and -17dB at 200MHz. This rejection is important because unless a large off-chip capacitance is used at the output of the recifier, there will be ripple at the rectfier output. Therefore, the supply ripple rejection is an important parameter for the circuits that uses the rectifier output as its supply. Eventhough the supply rejection is bad at lower frequencies, this is not

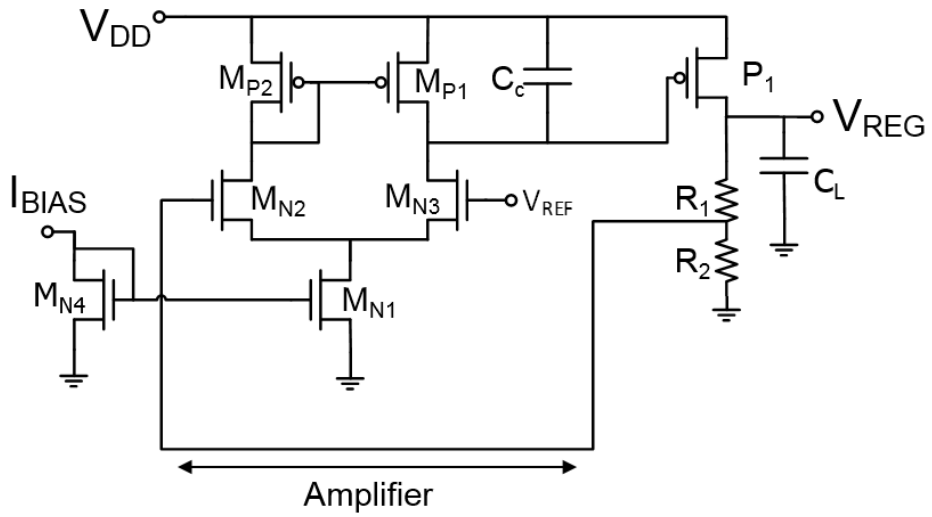


Figure 4.5: Regulator circuit used in this work

a problem for the locomotive system because for this system, the ripple frequency at the output of the rectifier is at the frequency of wireless power transfer (which is 100MHz) and its harmonics. Therefore, the rejection at 100MHz is the specification that the designer should consider. From 4.13, it can be seen that the rectifier output has a ripple (peak to peak) of around to 100mV. This translated to a ripple (peak to peak) of 14mV at the output of the regulator which is acceptable for the circuits used in this project.

Table 4.2: Sizing of transistors for regulator circuit

Reference Designator	W	L	Fingers
M_{P1}, M_{P2}, M_{N1}	1μm	2μm	4
M_{N2}, M_{N3}, M_{N4}	1μm	2μm	2
P_1	30μm	180nm	40

Table 4.3: Passives used in regulator circuit

Reference Designator	Value	W	L	Series Bars
C_C, C_L	$11pF$	50μ m	50μ m	-
R_1, R_2	26kΩ/bar	0.35μm	6μm	8,22

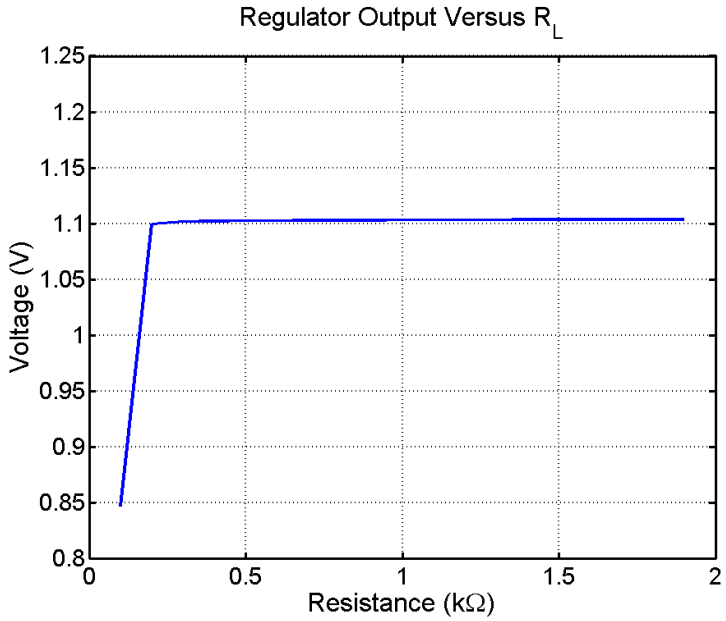


Figure 4.6: Load regulation of regulator circuit

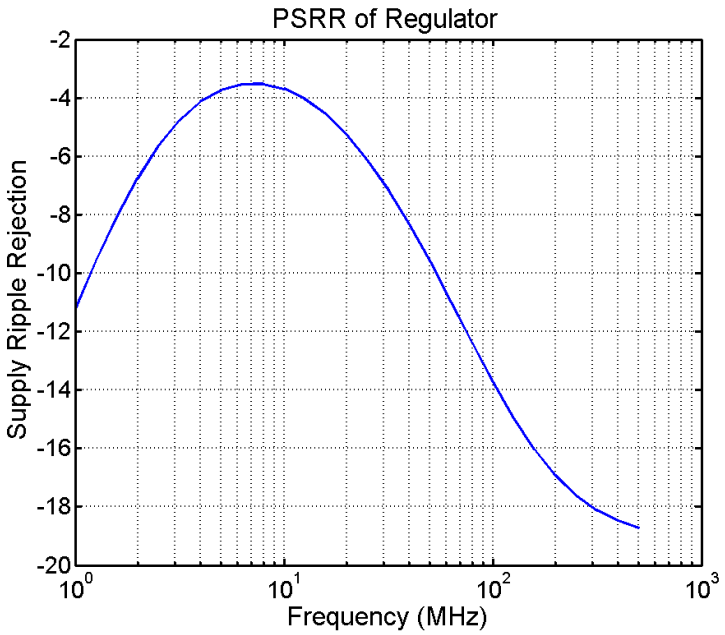


Figure 4.7: PSRR of regulator circuit

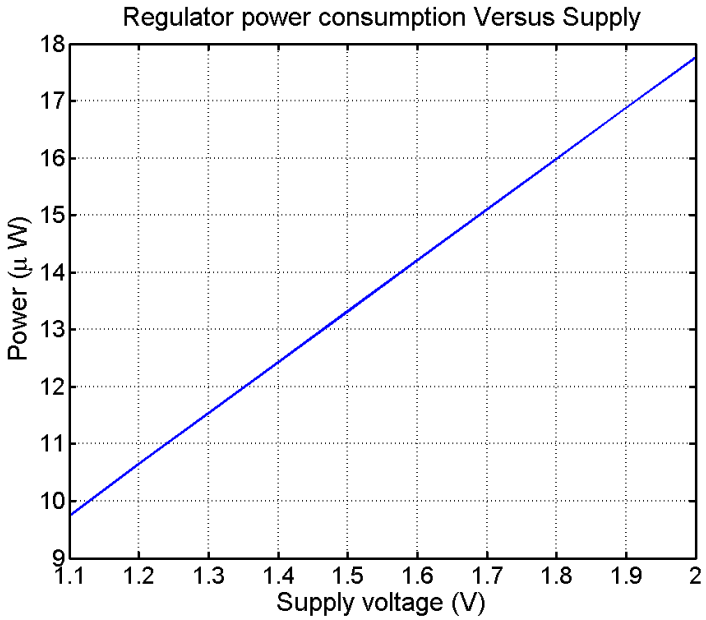


Figure 4.8: Power consumption of regulator circuit as supply is swept

4.1.3 Reference Generator

The reference voltage V_{REF} required by the regulator is generated using a reference circuit shown in Fig. 4.9. This circuit also generates the bias currents required else where in the IC like in the amplifier of the regulator and the VCO and charge pump in the PLL synthesizer. In the 180nm CMOS process in which this project was taped out allowed the realization of forward biased pn junctions in the form of PNP transistors whose base and collector are tied to ground as shown in Fig. 4.9.

The circuit works by employing negative feedback to force potentials V_A and V_B shown in Fig. 4.9 to the same value. Then the V_A is the forward conduction voltage of the diode D_2, V_{EB2}. This means that the voltage drop across reistance R_1 is the difference in forward drop for D_1 and D_2, $\Delta V_{EB} = V_{EB2} - V_{EB1}$. If the diodes D_1 and D_2 are sized in a ration n:1, then $\Delta V_{EB} = V_T ln(n)$ which is PTAT (Proportional To Absolute Temperature). Addionally, the potential V_{EB1} is CTAT (Complementary To Absolute Temperature) [34]. Therefore the potential V_B is a summation of the drop across R_1(PTAT) and D_1 (CTAT). The current through $T_{P1} - T_{P4}$ can be shown to be

$$I_{REF} = \frac{\Delta V_{EB}}{R_1} + \frac{V_{EB2}}{R_2}, \tag{4.2}$$

if R_2, R_3 are identical.

The reference voltage can be shown to be

$$V_{REF} = I_{REF} \times R_4 = \frac{R_4}{R_1}\Delta V_{EB} + \frac{R_4}{R_2}V_{EB2}. \tag{4.3}$$

By suitably scaling the resistor ratios, one can potentially make the reference voltage independant of temperature by cancelling the positive and negative temperature coefficients of the PTAT and CTAT terms. For the application presented in

this work, the primary requirement calls for a supply independant reference voltage and so, for the design of this circuit, cancellation of temperature coefficient was not pursued. Tables 4.4 and 4.5 shows the details of the transistors, diodes and passives used in this circuit. A single stage amplifier designed for a gain of 35dB with a power supply of 1.1V and a tail current of 5.2μA was used to set the negative feedback in the reference circuit.

One of the important design metric for the reference generation circuit is that the output voltage should vary very little with supply voltage. Fig. 4.10(a) shows the power supply ripple rejection of this circuit across the frequency of ripple in a AC simulation. As seen from this plot, at the frequency of wireless power transfer of 100MHz, the ripple rejection is less than -32.5dB. Fig. 4.11(a) and 4.11(b) shows the variation of reference voltage and current outputs as the supply voltage is varied. As can be seen from these plots, the variation of voltage and current outputs are respectively 0.4% and 0.97%. The minimum supply voltage to ensure all transistors are in saturation was 1.2V. At this supply, the circuit consumed 17.7μW of power as shown in Fig. 4.10(b).

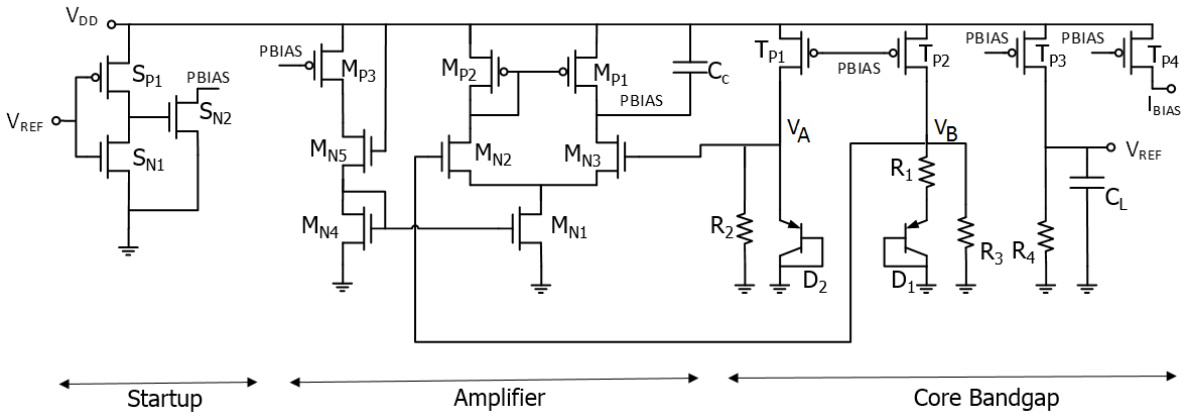


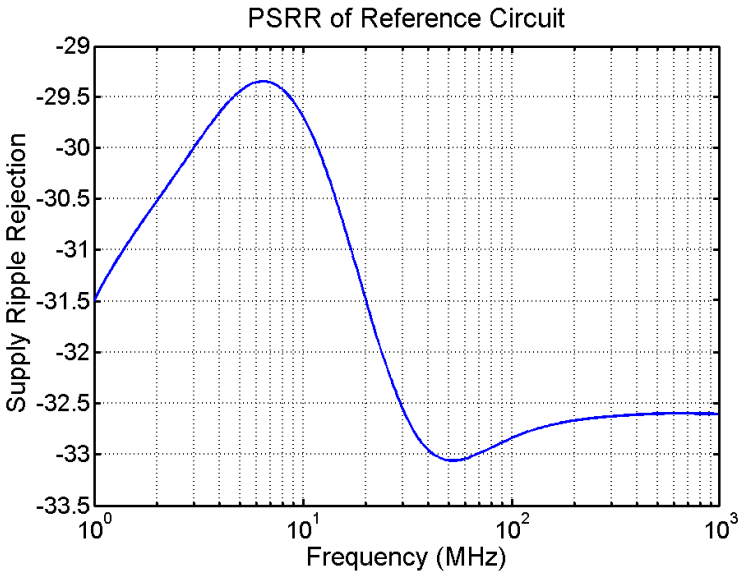
Figure 4.9: Reference generator circuit used in this work

Table 4.4: Sizing of transistors and diodes for reference circuit

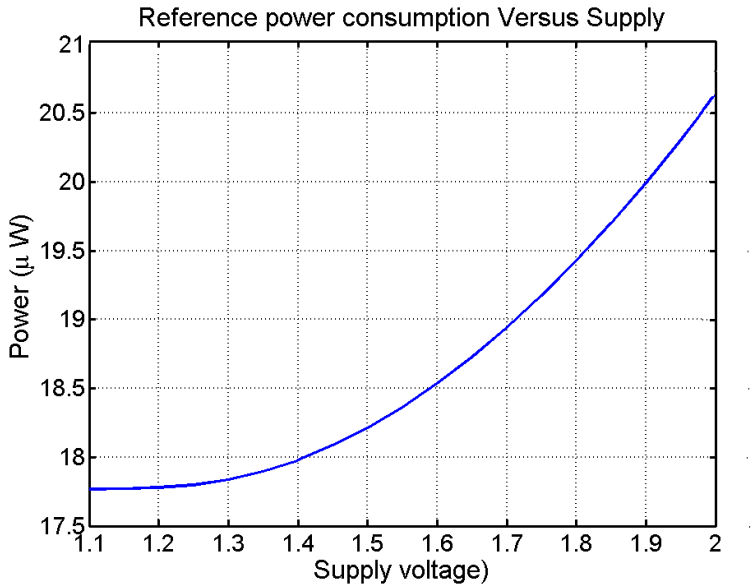
Reference Designator	W	L	Fingers
T_{P1}, T_{P2}, T_{P3}, T_{P4}, M_{P1}, M_{P2}, M_{P3}, M_{N1}, M_{N5}	1μm	2μm	4
M_{N2}, M_{N3}, M_{N4}	1μm	2μm	2
D_1, D_2 (Emitter Area)	1.2μm	3μm	1, 8

Table 4.5: Passives used in reference circuit

Reference Designator	Value	W	L	Series Bars
C_C, C_L	$1pF$	12μm	12μm	-
R_1	52.5$k\Omega$	0.35μm	6μm	2
R_2,R_3	472.4$k\Omega$	0.35μm	6μm	18
R_4	314.9$k\Omega$	0.35μm	6μm	12

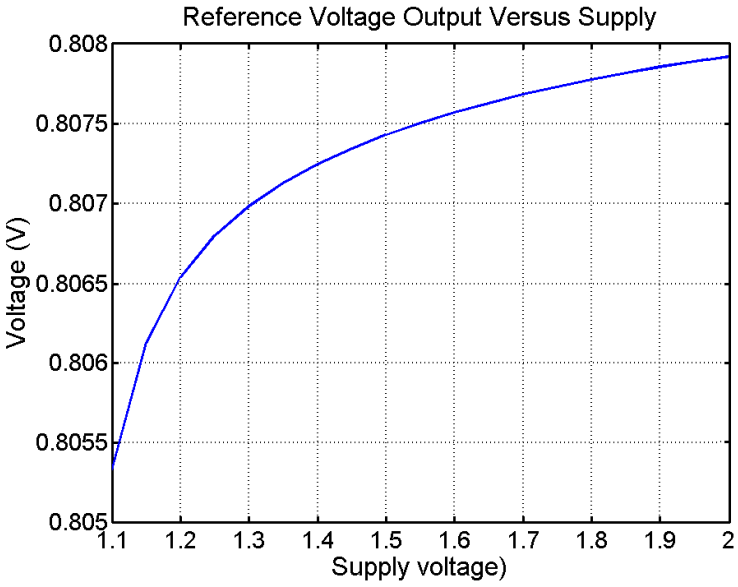


(a)

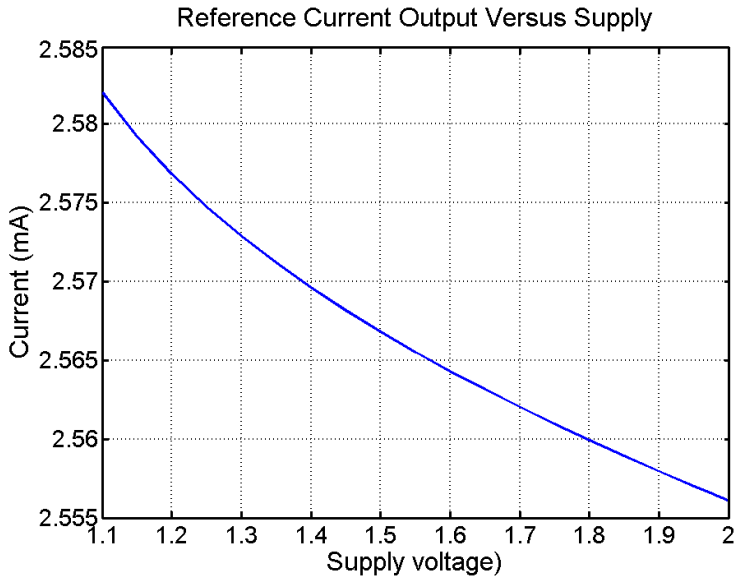


(b)

Figure 4.10: (a) PSRR of reference generator circuit (b) Power consumption of reference generator circuit as supply is swept



(a)



(b)

Figure 4.11: Variation of (a) Voltage output and (b) Current output, as supply voltage of reference generator circuit is swept

4.2 Simulation of Power Conditioning Blocks

The reference block was designed to generate an output voltage of 0.81V and an output current of 2.6μA. The regulator output was designed to be 1.1V and works with a minimum rectified output of 1.25V. To simulate the power conditioning blocks a test bench was setup as shown in Fig. 4.12. Wireless power delivery was simulated using a two port model for the coupling between a pair of PCB based coils as described in a previous chapter. The rectifier was driven by the receiver coil in the WPT system as shown in 4.13. The output of the rectifier was used to power the reference and regulator blocks. The regulator was setup to drive a 1kΩ load as is typical in the system proposed in this work. Fig. 4.14 shows the operation of reference and regulator circuits under these conditions. Based on this simulation, the rectifier outputs an average voltage of 1.35V for a 2.1V peak amplitude at its input. Therefore the simulated efficiency of rectifier is 65%.

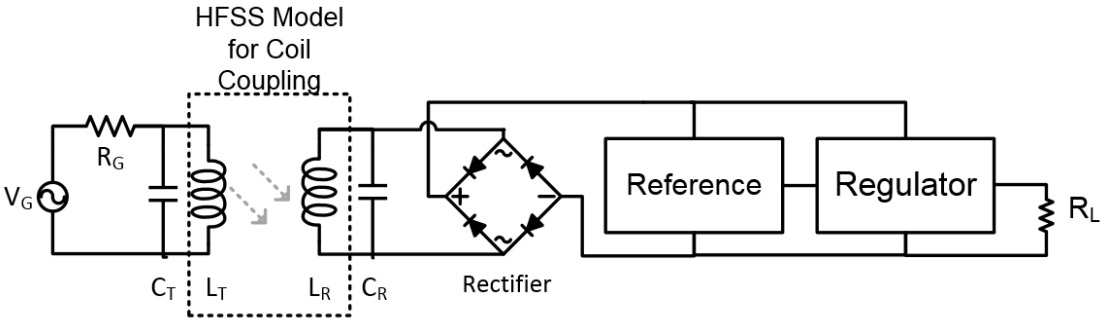


Figure 4.12: Testbench for simulating the operation of power conditioning blocks

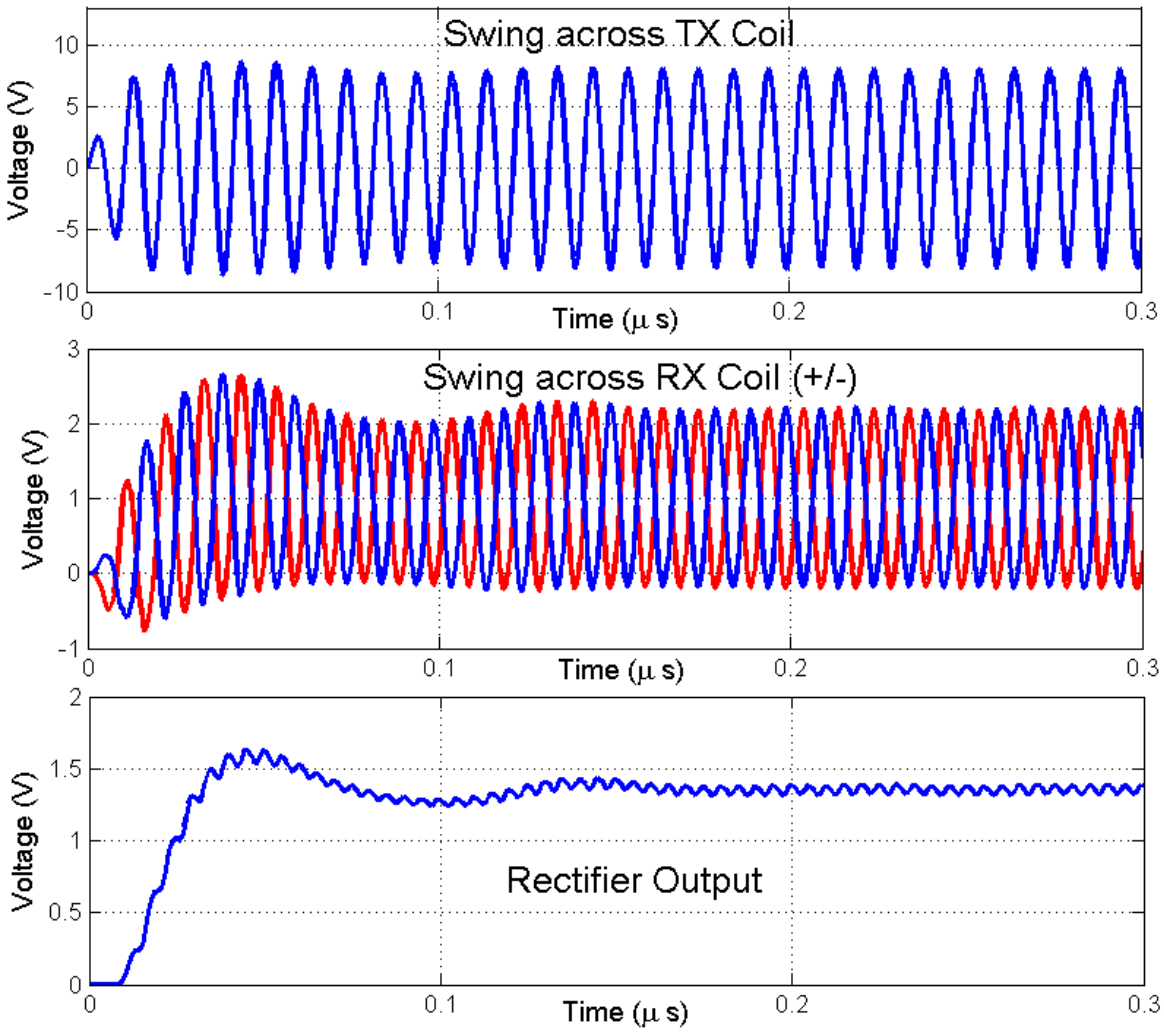


Figure 4.13: Waveforms at the input and output of rectifier

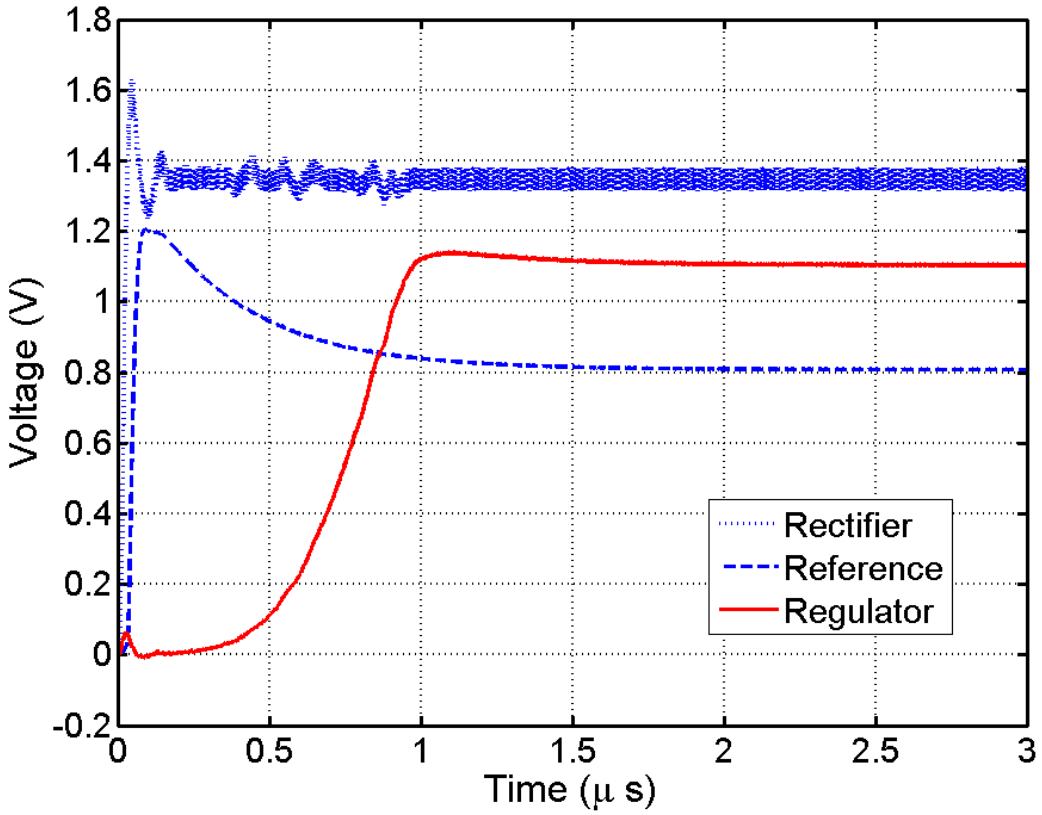


Figure 4.14: Waveforms at reference and regulator outputs

4.3 PLL Frequency Synthesizer

PLL based frequency synthesizers have been discussed in lenght in literature [35], [36]. For this work, the frequency synthesizer was implemented using a third order charge pump PLL as shown in Fig. 4.15. The SAW device specification required the output frequency of the synthesizer to cover the range 165MHz to 195MHz in steps of 3MHz. This means the reference of the PLL f_{REF} should be 3MHz and the feedback divider needs to be programmed for a division ratio between $N = 55$ to $N = 65$ to cover the required range of frequency.

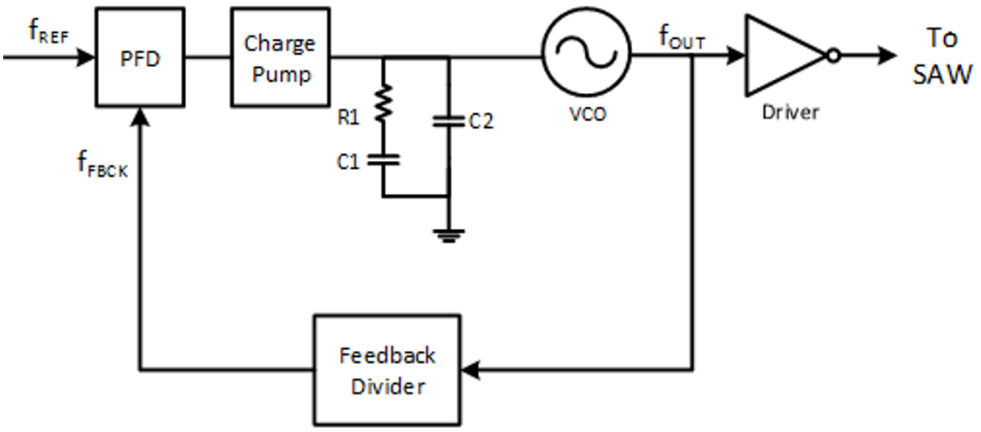


Figure 4.15: Block diagram of PLL Frequency Synthesizer

4.3.1 Reference Clock for PLL Synthesizer

For this project, the entire system containing CMOS IC and SAW device is completely isolated. The only external signal available to the system is the alternating voltage generated by the wireless power delivered to the receiver coil. Therefore, we use this alternating voltage to generate the reference clock for the PLL. This is done

as shown in Fig. 4.16. The clock waveform across the rectifier input is sensed by means of inverter based buffer and then divided by means of a reference divider. In this project, wireless power transfer was done at 100MHz frequency. Therefore, a reference clock for PLL of 3.125MHz can be generated from this 100MHz by employing a divider of $M = 32$.

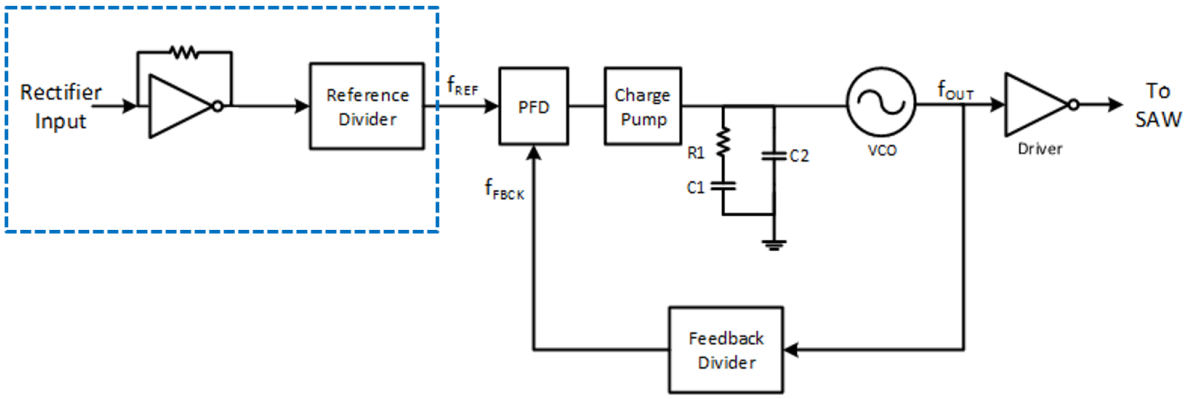


Figure 4.16: Reference clock generation for PLL frequency synthesizer

Such an arrangement provides flexibility in synthesizing frequencies outside the specifications provided. This flexibility was important in this project because at the time of circuit design and tape out, data from SAW devices were not available and there was a possibility that once fabricated the SAW devices might show a resonant frequency different from the specifications worked out and hence would require a different frequency synthesizer output frequency. By changing both the frequency of wireless power transfer and the divide ratio, any frequency can be synthesized.

Thus, the synthesized frequency f_{OUT} can be written as $f_{OUT} = N\frac{f_{WPT}}{M}$, where, f_{WPT} is the frequency of wireless power transfer and, M and N are respectively the reference clock divider and feedback divider ratios respectively.

4.3.2 Phase Detector, Charge Pump and Loop Filter

A standard phase detector circuit was shown in Fig. 4.17 was employed for this project. Spur rejection was not very critical for this project since the load (SAW device) inherently has a frequency selective response. Therefore a simple charge pump circuit used as shown in Fig. 4.18. The charge pump current was designed to be $20\mu A$. The loop filter components were chosen as $R_1 = 11k\Omega$, $C_1 = 117pF$ and $C_2 = 5.8pF(= C_1/16)$. With these values, the loop bandwidth of the PLL can be calculated as $\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NC_1}}$. For $N = 60$ and $f_{OUT} = 180$MHz bandwidth can be calculated to be $f_n = 68kHz$. The damping factor for the PLL can be calculated as $\zeta = \frac{\omega_n R_1 C_1}{2} \approx 0.7$. The bias current for the chargepump was mirrored from the current output of the reference generator circuit.

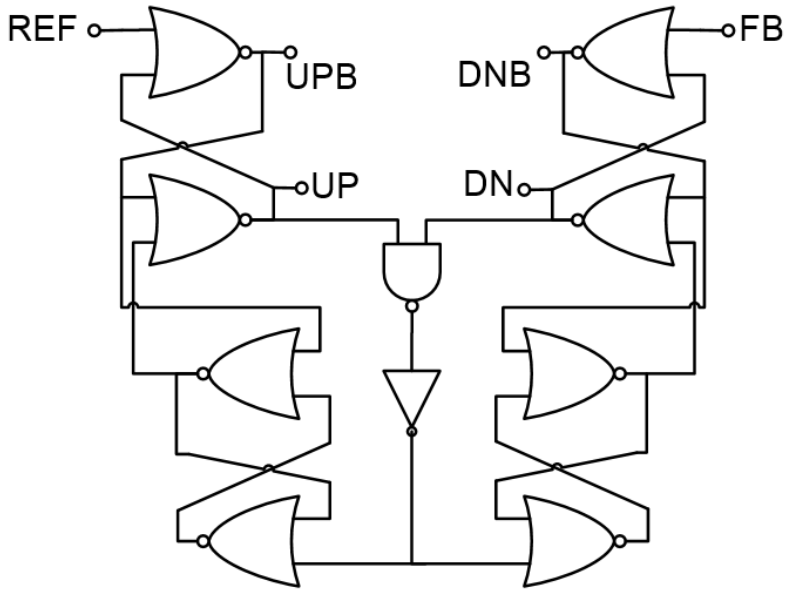


Figure 4.17: Phase frequency detector circuit used in this work

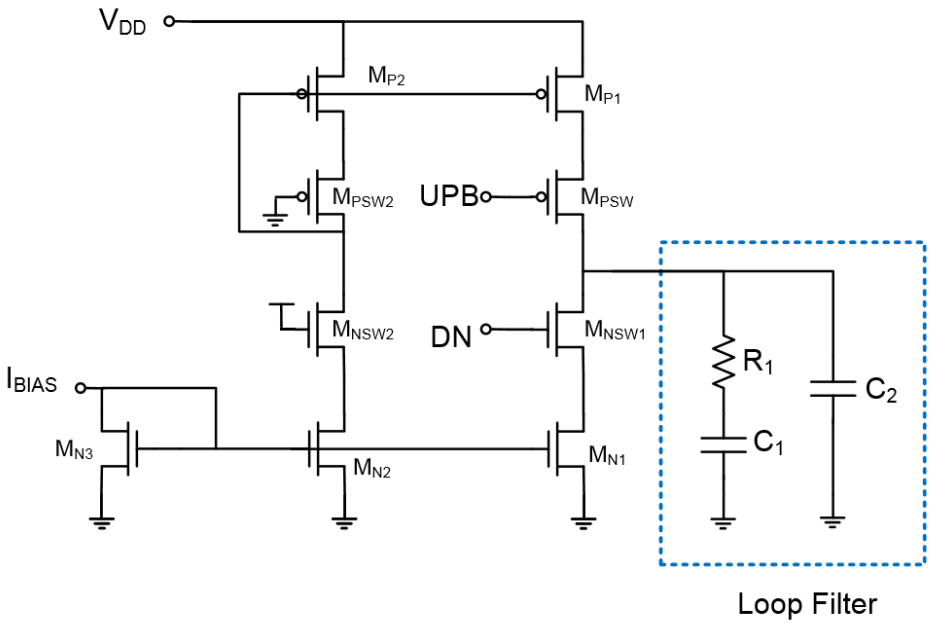


Figure 4.18: Charge pump circuit used in this work

Table 4.6: Sizing of transistors for charge pump

Reference Designator	W	L	Fingers
M_{N1}, M_{N2},M_{N3}	1μm	2μm	16,2,2
M_{NSW1}, M_{NSW2}	0.5μ m	0.18μm	16,2
M_{P1}, M_{P2}	4μ m	2μm	16,2
M_{PSW1}, M_{PSW2}	0.5μ m	0.18μm	16,2

4.3.3 Voltage Controlled Oscillator

The VCO was implemented as a three stage CML based ring oscillator as shown in Fig. 4.19. Each delay cell used in the ring oscillator was implemented as shown in Fig. 4.20. The VCO was designed to meet the range of frequency from 130MHz to 210MHz which is more than the specification of the synthesizer output frequencies with a gain $K_{VCO} = 300MHz/V$. As shown in Fig. 4.20 varactor (transistors M_{C1} and M_{C2}) based frequency tuning was employed in place of the more popular resistor tuning. While resistor based tuning offers a wider tuning range, it also results in swing variation with frequency (for a constant tail current). Typically, an amplitude control loop is employed to vary the tail current as the resistive load is tuned so that the over all swing remains unchanged. The use of this amplitude control loop would involve burning additional power. Since power was a critical parameter in the wirelessly powered system considered in this work and since varactor based tuning was sufficient to cover the required range of frequencies, the VCO was implented with varactor based tuning for the delay cell. Fig. 4.21 shows the buffer circuit employed to generate CMOS compatible output swing from the CML output of VCO. This is required since a CMOS divider circuit is employed in the PLL which requires CMOS levels at its input. The bias currents for the VCO and buffer were mirrored from the current output of the reference generator circuit. Fig. 4.22 shows the transient simulation output waveforms at the VCO output and at the buffer outputs. The swing at the VCO output is 300mV peak and at the buffer output is 1.1V peak. Table 4.8 summarizes the dimensions of the transistors used in the VCO design.

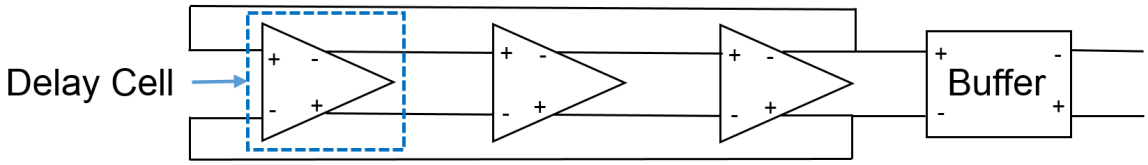


Figure 4.19: Three stage ring oscillator used in the PLL Frequency Synthesizer

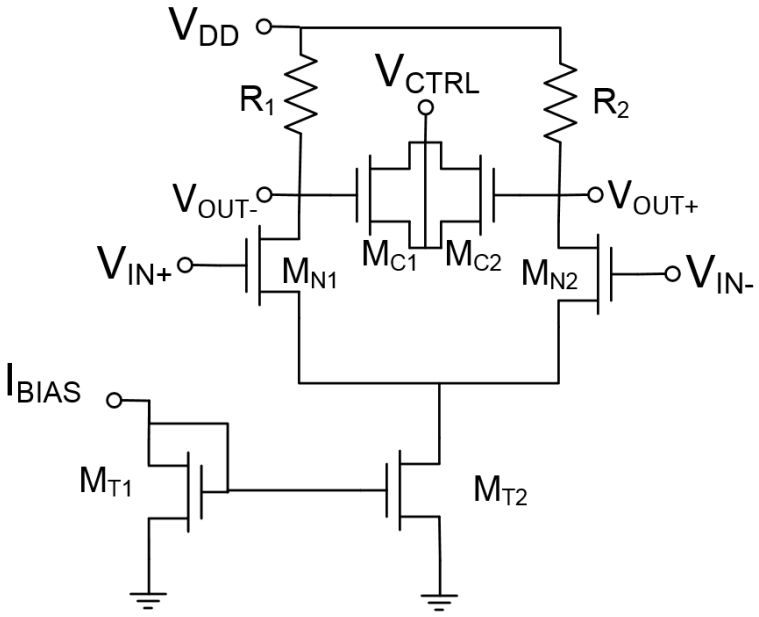


Figure 4.20: Delay cell used in ring oscillator

Table 4.7: Sizing of resistors used in VCO

Reference Designator	Value	W	L	Series Bars
R_1, R_2	11.7kΩ/bar	0.35μm	3.1μm	4

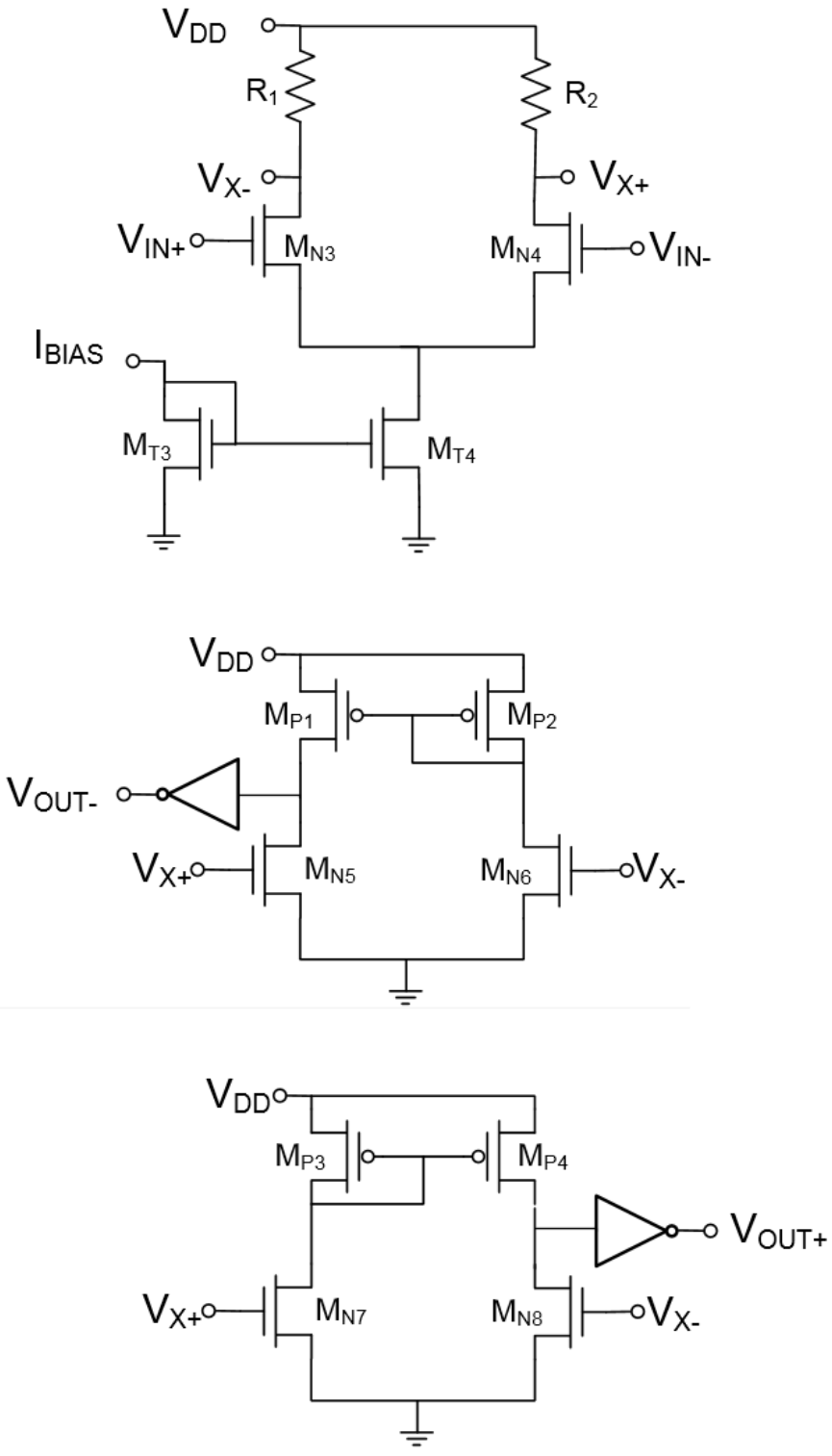


Figure 4.21: VCO buffer circuit

Table 4.8: Sizing of transistors used in VCO

Reference Designator	W	L	Fingers
M_{C1}, M_{C2}	0.7μm	1μm	4
M_{N1}, M_{N2}, M_{N3}, M_{N4}	0.8μm	0.8μm	2
M_{N5}, M_{N6}, M_{N7}, M_{N8}	0.5μm	1.5μm	2
M_{P1}, M_{P2}, M_{P3}, M_{P4}	4μm	1.5μm	4
M_{SW1}, M_{SW2}	3μm	0.18μm	2
M_{T1}, M_{T2}	1.2μm	2μm	2,10
M_{T3}, M_{T4}	1μm	2μm	2,12

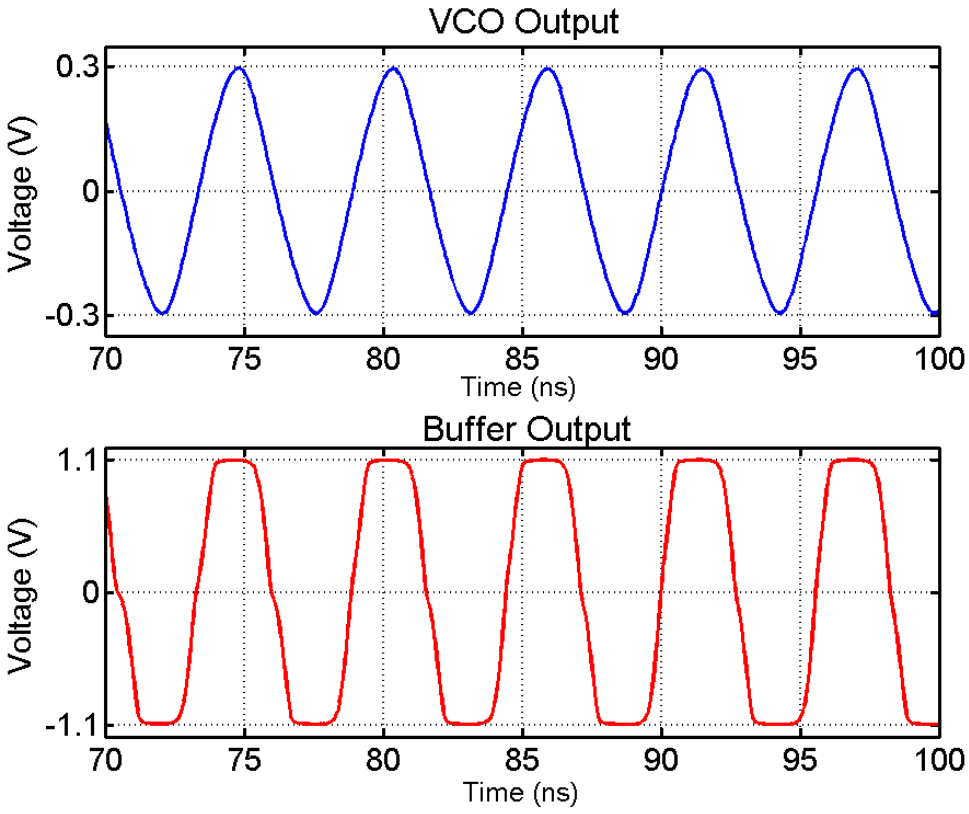


Figure 4.22: Transient simulations showing the differential outputs at the VCO and Buffer for 180MHz VCO operation

4.3.4 Divider

The architecture employed in this work called for the use of two dividers in the PLL - one for the reference clock and the other for the feedback clock. Since the synthesized output frequency range is from 165MHz to 195MHz with a reference of 3MHz, this meant that the divider ratio should be programmable from $N = 55$ to $N = 65$. This was accomplished using a cascade of $\div 2/\div 3$ cells (shown in 4.24) as shown in Fig. 4.23. It can be shown that with "n'' stages cascaded, divide ratio can be programmed from $N = 2^n$ when all CON signals are 'zero' to $N = 2^{n+1}$ when all CON signals are 'one'. With $n = 5$, divide ratio can be programmed from $N = 32to63$ and with $n = 6$ divide ratio can be programmed from $N = 64$ to $N = 127$. Based on the topology descibed in [37] the implentation shown in 4.25 can be programmed from $N = 32$ to $N = 127$ based on seven control bits. Table 4.9 shows how the seven control bits can be selected to obtain particular divide ratio. Figures 4.26 and 4.27 shows some typical divider waveforms encountered in the synthesizer. At the reference clock divider, an input frequency of 100MHz is divider by 32 to obtain output frequency of 3.125MHz. Similarly at the feedback divider, an input frequency of 175MHz from the VCO is divided by 56 to obtain output frequency of 3.125MHz. Clearly, in the second case, the output duty cycle is not 50%. Fortunately, the duty cycle at the output of divider need not be 50% since the divider output is fed into the phase detector which is edge triggered and therefore insenstive to duty cycle.

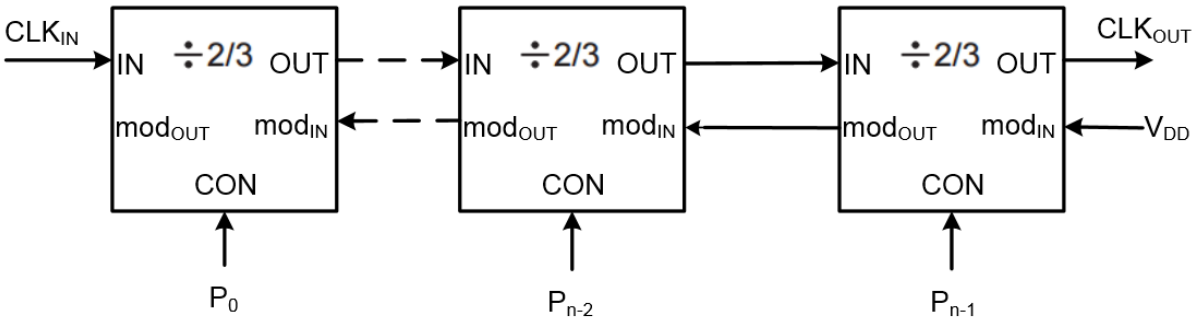


Figure 4.23: Programmable divider using cascade of $\div 2/\div 3$ cells

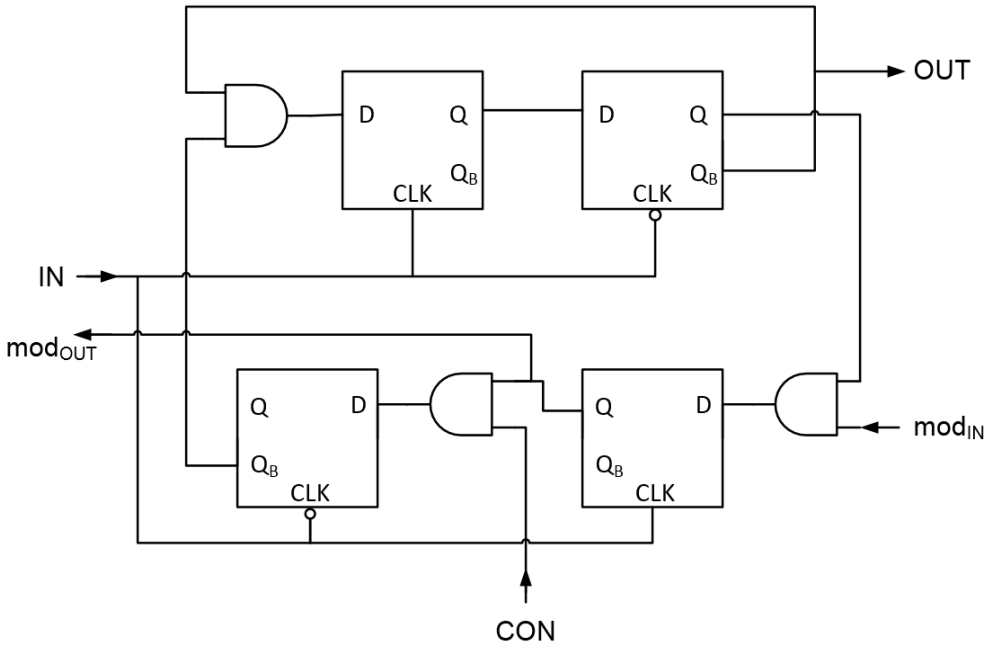


Figure 4.24: A single $\div 2/\div 3$ cells: if $CON = 0$ then the circuit divides by 2 and if $CON = 1$ then the circuit divides by 3

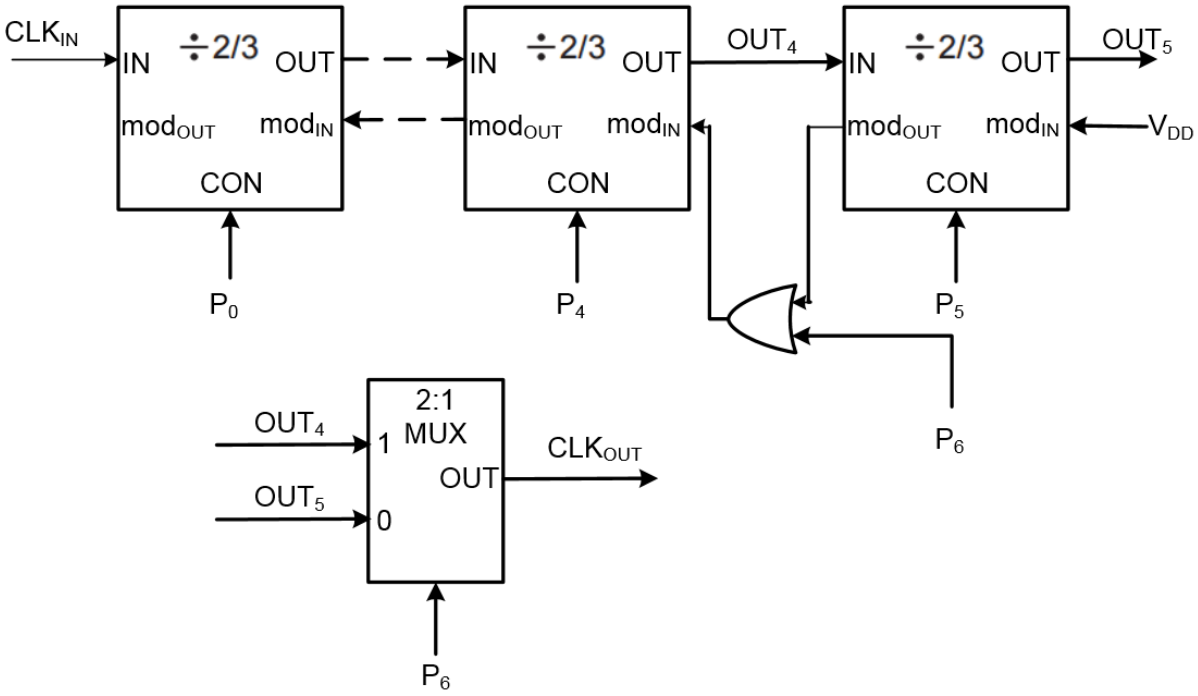


Figure 4.25: Programmable divider used in this work that can be programmed to divide from $N = 32$ to $N = 127$ with bits $P_6 - P_0$

Table 4.9: Progammable divider

MSB						LSB	Divide ratio (N)
P6	P5	P4	P3	P2	P1	P0	
1	X	0	0	0	0	0	32
1	X	.	.	.	.	.	.
1	X	.	.	.	.	.	.
1	X	1	1	1	1	1	63
0	0	0	0	0	0	0	64
0	.	.	.	.	.	.	.
0	.	.	.	.	.	.	.
0	1	1	1	1	1	1	127

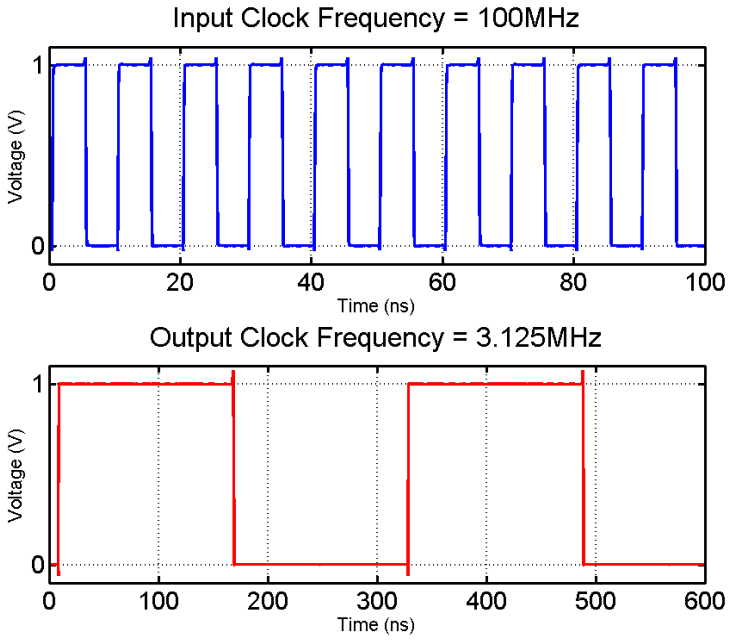


Figure 4.26: Divide by 32 operation of the programmable divider to obtain 3.125MHz output

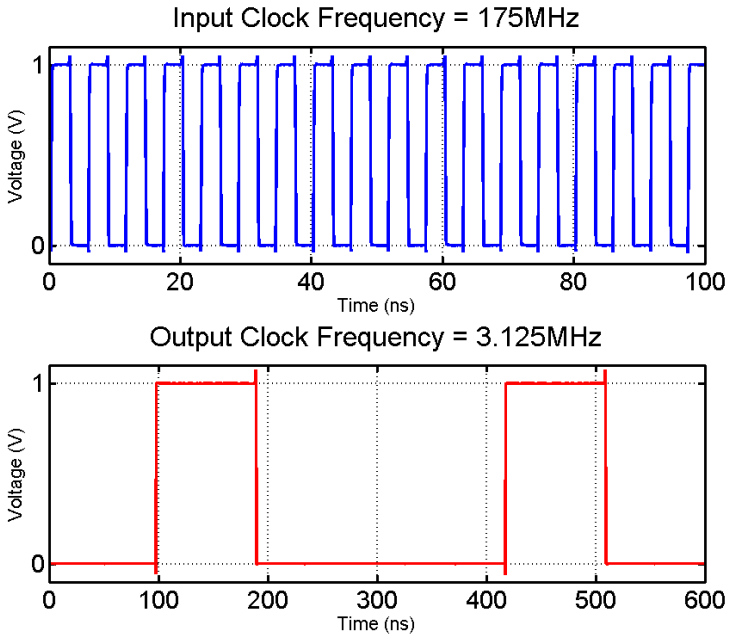


Figure 4.27: Divide by 56 operation of the programmable divider to obtain 3.125MHz output

4.4 Simulation of PLL

Fig. 4.28 shows the control voltage of the PLL as the PLL locks. The simulation setup involved post layout extracted cells for the VCO, loop filter and charge pump, and schematic level PFD and dividers. The reference clock for the PLL was generated from a f_{WPT} =100MHz input across the coil. Using a reference divider of $M = 32$ results in $f_{REF} = 3.125MHz$ and with feedback divider of $N = 56$, output frequency f_{OUT} =175MHz can be synthesized. As can be seen, the PLL control voltage output settles to the final value of 382mV within 15μs.

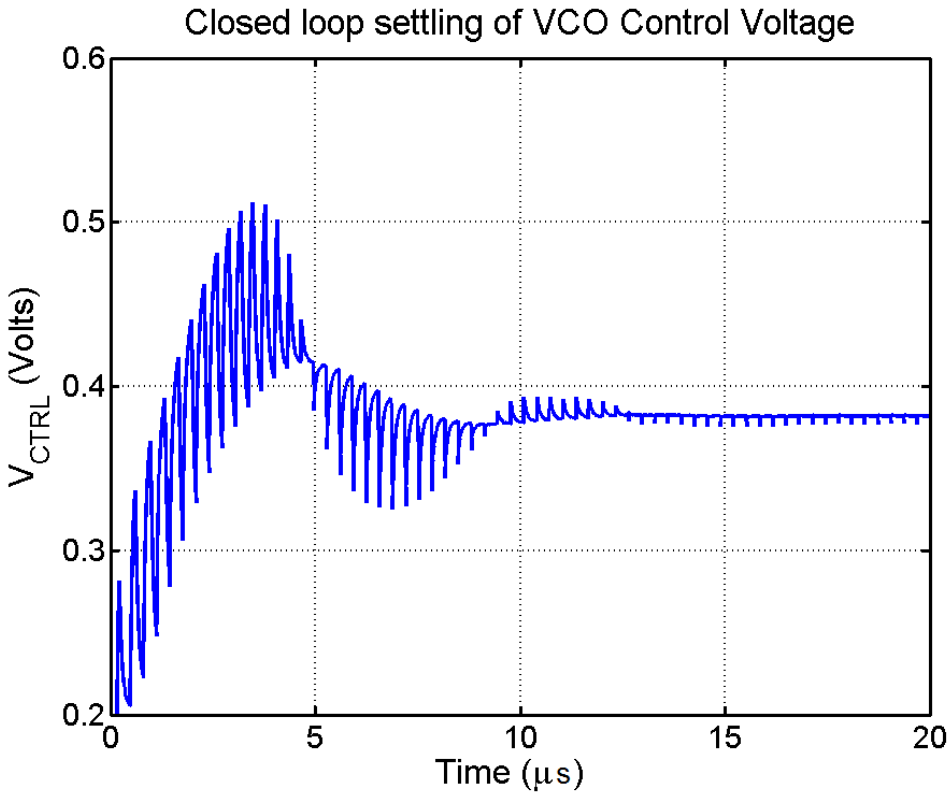


Figure 4.28: Control voltage settling in closed loop PLL

4.5 Driver Circuit

The clock waveform synthesized by the PLL is used to drive the SAW device. A pair of CMOS inverters were employed as driver circuits for this purpose as shown in Fig. 4.29. The transistors in the driver circuit were sized so as to deliver a short circuit current of 485mA. Because the SAW devices were unavailable at the time of tape out, the driver impedance could not be matched to the SAW device at the resonance frequency of the SAW device. This implied that an external impedance matching network be employed off-chip as shown in Fig. 4.29.

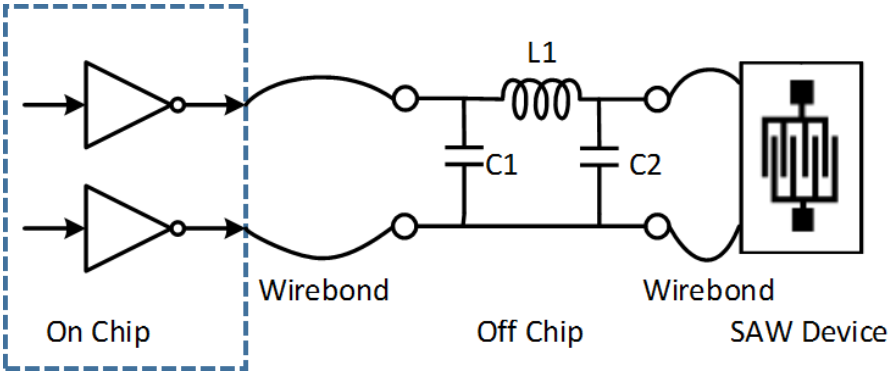


Figure 4.29: Driver circuit with off-chip matching network

4.6 SAW Actuator

The proposed locomotive system employs only one SAW device. This means that the system can move only in one direction along a straight line. Even though [9] had demonstrated SAW based locomotion, the size of the SAW device employed in that work was much larger with the finger length of approximately 1.5cm. The device was powered by an amplifier supplying 1.7W of power trough a pair of wires at the SAW resonant frequency of around 11MHz. While [9] demonstrated a novel tunable surface

acoustic wave device that enabled control of direction by changing the frequency of excitation of SAW device, the power requirement and larger size makes it unsuitable to be used in a miniature locomotive system driven by a wirelessly powered CMOS front end.

For this work, a smaller SAW device was fabricated. As the pitch between fingers is reduced, the resonance frequency of the SAW device increases. A very high resonance frequency creates difficulty in the design of the CMOS front end. This is because generating a larger frequency using a PLL inside the CMOS front end results in larger power consumption in it. This in turn limits the power available for locomotion and consequently the range of operation of the wirelessly powered locomotive system will be reduced.

4.7 Summary

In this chapter the various circuits required to implement a CMOS front end to drive a wirelessly SAW based locomotive IC were discussed. Since the wireless power harvested is limited, minimizing the power consumption of the circuits is the most important design criteria for this project. Table 4.10 shows the simulated post layout power consumption of individual blocks in a typical use case whereby the rectifier output is 1.25V and the reference clock obtained from the wireless power transfer at 100MHz is used to synthesize 177MHz. The total simulated power consumption was 529μW. Though this is almost twice the power consumption reported in other locomotive systems found in [3] and [5], the higher power consumption is due to the higher resonant frequency of SAW device which requires a frequency of close to 200MHz to be synthesized on chip. This requirement inherently puts a minimum bound on the power consumption of the CMOS front end because of the higher switching in the internal nodes in the PLL. In comparison, neither of the two refer-

ences involved any such high frequency switching node inside their respective signal chain. The clock recovery, demodulator and MCU used in [5] is operated at very low switching speed of 1Mbps. Similarly, the maximum data rate employed by [3] was only 25Mbps. Eventhough the carrier frequency (=1.86GHz) in [3] was much higher, this signal was observed only at the input of the rectifier circuit and so did not increase power consumption of other blocks in the signal chain.

Table 4.10: Power consumption of circuit

Block	Power Consumption (μW)
Reference	18
Regulator	11
Reference Clock Divider	100
Feedback Clock Divider	120
Chargepump	15
Phase Detector	80
VCO	170
Bias	15
Total	529

5. MEASUREMENT RESULTS

5.1 Silicon Versions and Measurement Setup

The proposed locomotive system containing the receiver coil, CMOS IC and SAW device all on a single PCB is completely isolated except for the wireless power being transferred to the receiver coil. Consequently, setting the control bits for the two programmable dividers requires attention. Moreover, in order to validate the correct operation of individual blocks in the CMOS IC, a few of the internal nodes should be accessible for observing with an oscilloscope. Based on these considerations, two versions of the CMOS ICs were fabricated- Version 1, which was meant for validating the circuit blocks, and Version 2 which was meant for the attempted demonstration of locomotion.

Fig. 5.1 shows the silicon die for Version 1. This silicon was packaged in a 36 pin QFN package and soldered on to a regular PCB with the intention of characterizing the operation and performance of individual circuit blocks. To achieve this, the internal nodes, which are the outputs of various blocks in the signal chain, were buffered and brought out as pins for observability. For ease of debug, the power conditioning block and PLL frequency synthesizer were separated out and powered by different supply pins. Additionally, the buffers used with the internal nodes utilized a separate power supply as well, to ensure that the switching noise of the buffers do not couple on to the analog blocks. Additionally, this version also included a scan chain programming for setting the control bits of the programmable dividers.

Fig. 5.2 shows the silicon die for Version 2 which was used as an unpackaged die to demonstrate locomotion. The locomotive system consisted of a PCB containing the receiver coil as well as the CMOS die and SAW device wirebonded on it. The

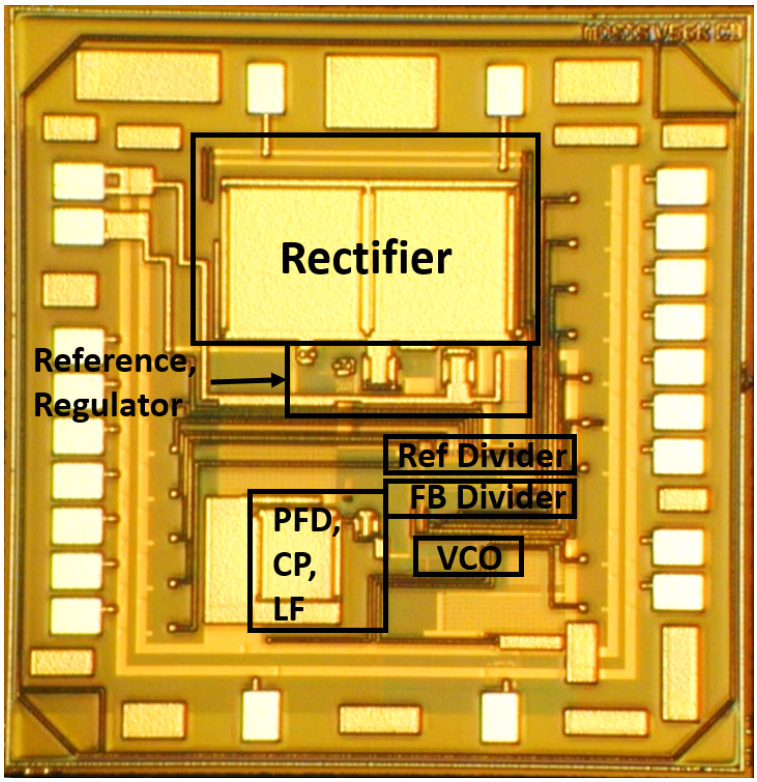


Figure 5.1: Die for Version 1 used in the locomotive system

VDD/VSS (regulator output and ground) nets inside the CMOS die is wirebonded to traces on the PCB. These PCB traces are then used to select the control bits of the dividers as shown in Fig. 5.3 by means of wirebonding. Also included on the PCB is the π matching network to match the impedance offered by the SAW device at its resonance frequency to the output impedance of the driver. As shown in figures 5.3(a) and 5.3(b), the receiver coil used for harvesting wireless power is on one side of the PCB and the CMOS die and SAW devices are wirebonded on the other side. For demonstration of locomotion, the side with the SAW device will be immersed in water with the receiver coil on the top, facing up and away from the water. When wireless power is provided to the receiver coil by means of a transmitter coil, the rectifier, reference and regulator circuits wakes up and generates a regulated

power supply for the PLL frequency synthesizer which in turn generates the electrical excitation to the SAW device which propels the PCB forward. The SAW device is immersed in water to enable this propulsion scheme. Careful attention was given to keep the complete PCB based system as small as possible to facilitate effective motion. The dimensions of the PCB which includes the receiver coil, the CMOS die, the off-chip matching network and the SAW device is 1.5cmX1.9cm.

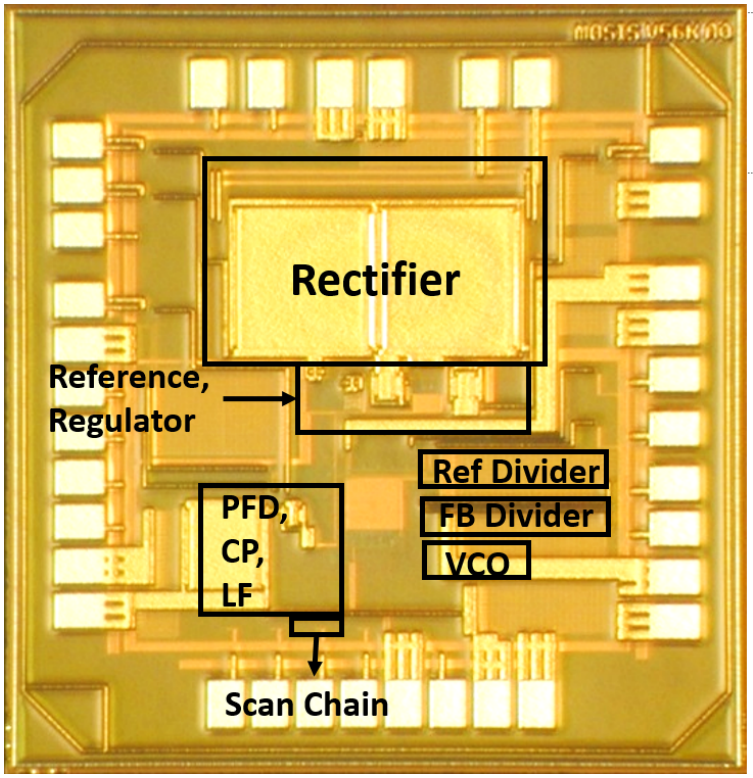


Figure 5.2: Die for Version 2 used for debug

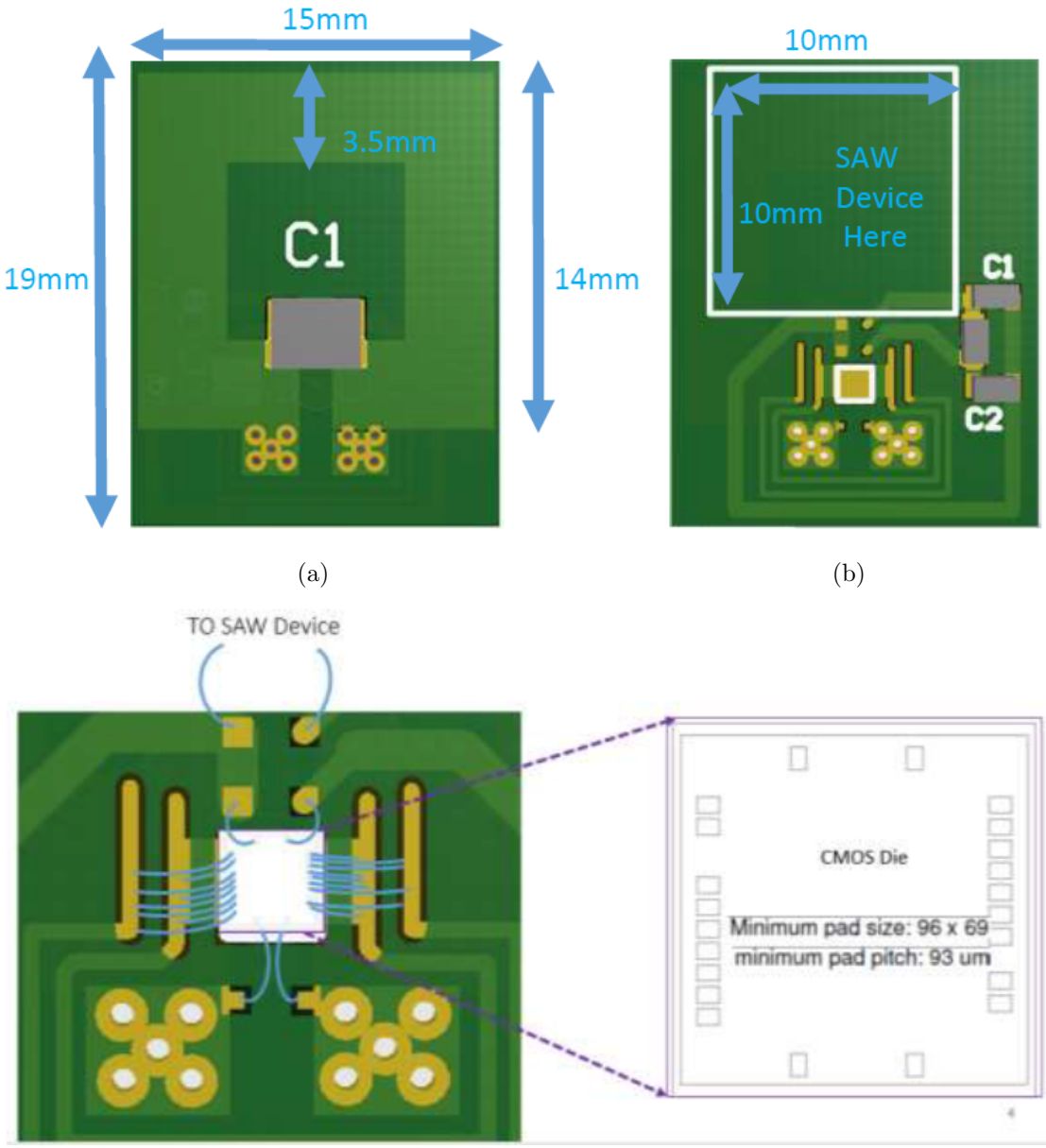


Figure 5.3: PCB used to demonstrate locomotion (a) Top view depicting receiver coil used to harvest wireless power and the capacitance in resonance with it (b) Bottom view of the PCB on which CMOS die and SAW devices are wirebonded (c) Wirebonding from pads on CMOS die to PCB- the pads on the bottom and top are respectively input to rectifier and driver output while pads on left and right are used to short control bits to VDD/VSS

5.2 Measurements on WPT

Fig. 5.4 shows the variation of wireless power transfer efficiency as measured using a network analyzer. Both the transmitter and receiver coils were PCB based coils whose dimensions are summarized in Table 5.1. Wireless power transfer efficiency was 80% at 5mm separation and decreased to 25% at 1cm separation. As mentioned in the first chapter, the efficiency of wireless power transfer using on-chip receiver coil demonstrated by [5] was 15% at 5mm separation between transmitter and receiver coils. It is evident from these measurements that WPT utilizing PCB based receiver coil offers better efficiency.

Table 5.1: Details of TX and RX coils used in WPT

Parameter	Value
Turns	1
Outer Diameter (mm)	14
Trace Width (μm)	3500
Trace Spacing (μm)	500
Substrate	1-oz FR-4
Inductance(nH)	12
Q	167

5.3 Measurements on Silicon

The power conditioning blocks and PLL were separately characterized with silicon from Version 1. With the transmitter and receiver coils separated by a distance of 5mm, the input power to the transmitter coil was varied and the rectifier, reference and regulator outputs were observed. Fig. 5.5 shows the resulting variation as a function of input power to the transmitter coil. As can be seen from this plot, the

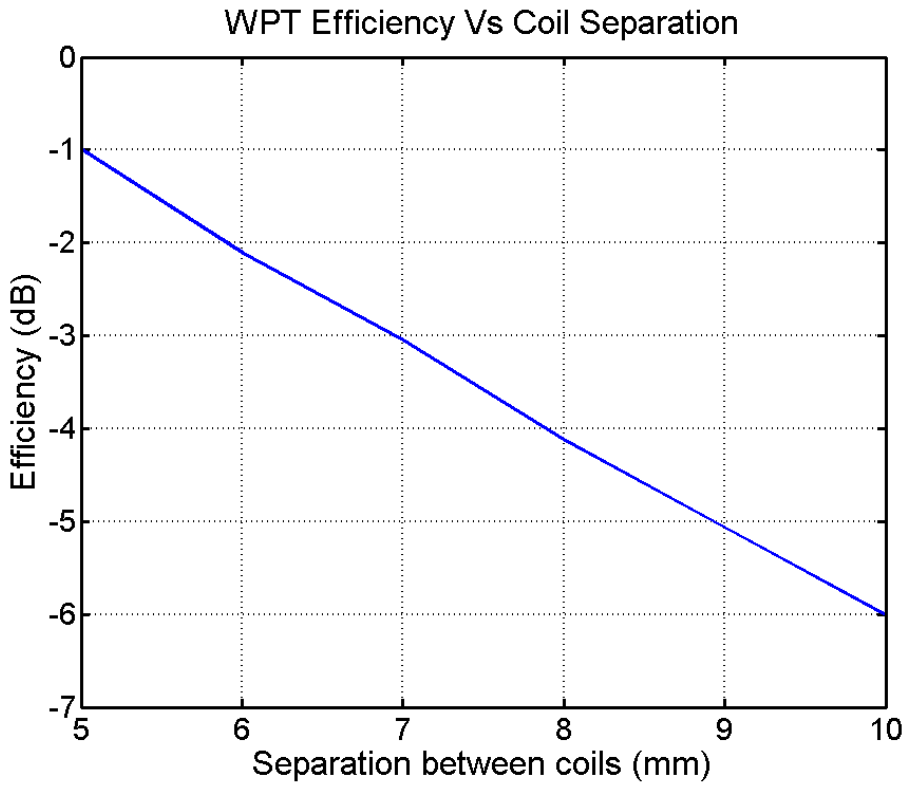


Figure 5.4: Wireless power transfer efficiency variation with separation between TX and RX coils

reference wakes up and regulator provides regulated supply for a minimum input power of 8dBm. The efficiency of rectifier was 60% when loaded by reference and regulator circuits which offered an equivalent load of 33kΩ to the rectifier.

Fig. 5.6 shows the frequency characteristics of the VCO as its control voltage is swept. Fig. 5.7 shows the outputs of reference divider and feedback divider in lock and VCO output at 177MHz. As can be seen from this figure, the PLL is in lock since all three waveforms are triggered together.

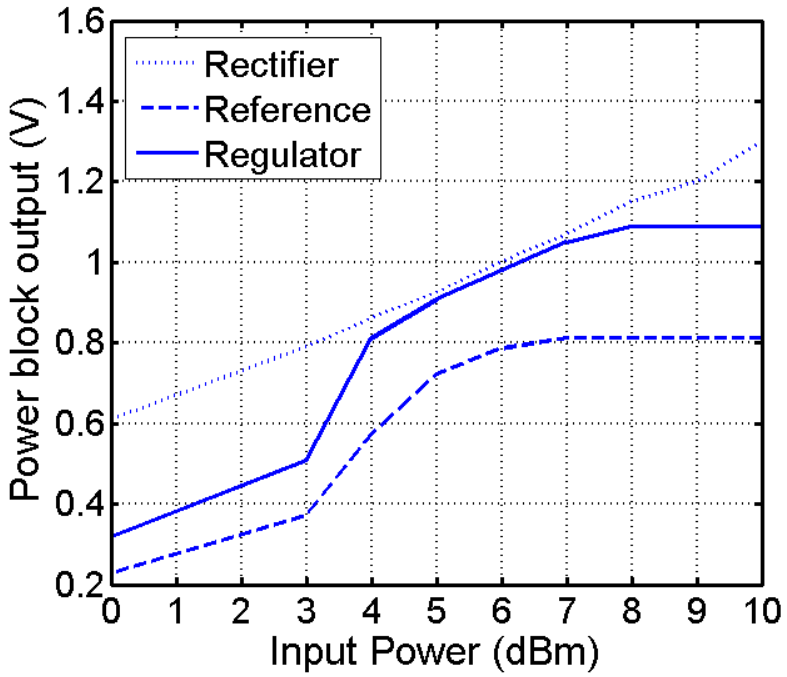


Figure 5.5: Output of power conditioning blocks as input power to the transmitter coil is varied

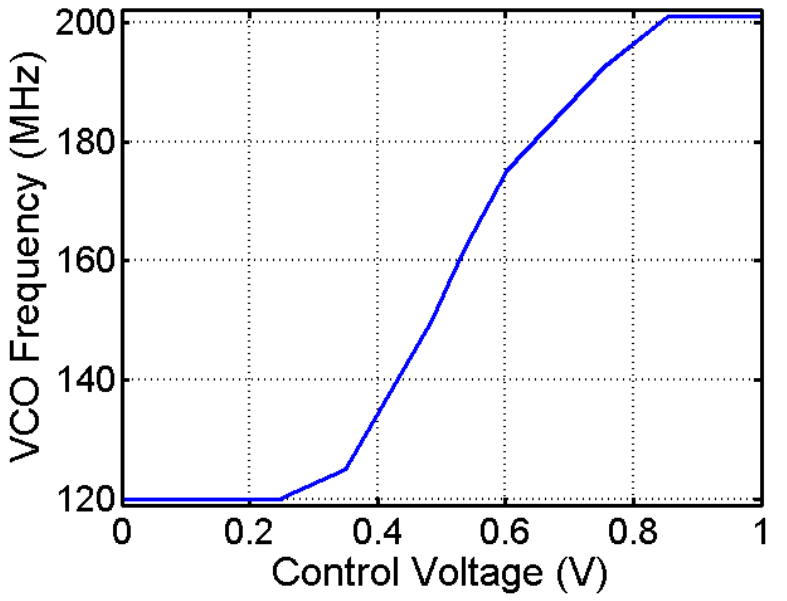


Figure 5.6: Measured frequency characteristics of the VCO

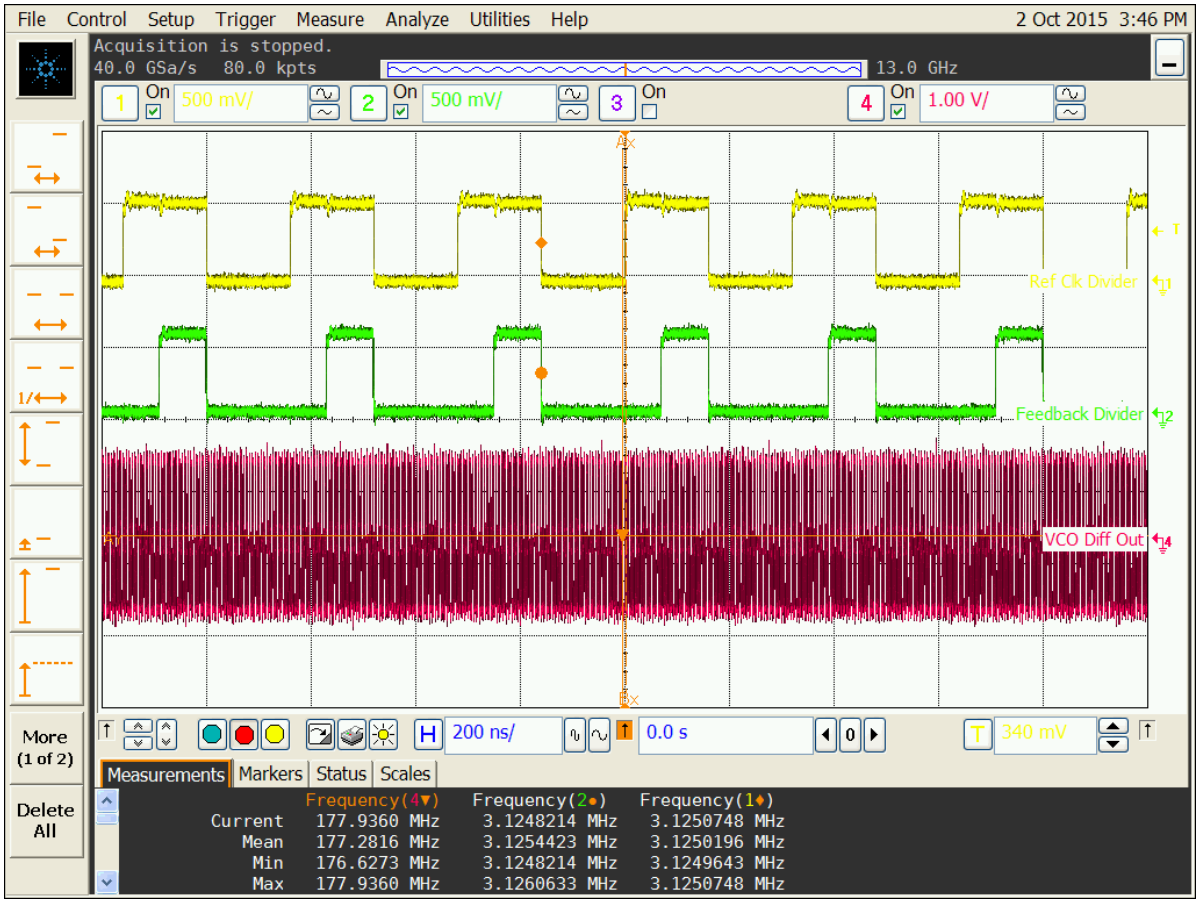


Figure 5.7: Transient waveforms showing frequency locking in PLL

5.4 Measurements on SAW Device

As explained in the previous chapter, the impedance of SAW device was not available at the time of tapeout. As a result, the opportunity to optimize the driver impedance was lost. Instead, an off-chip π matching network was employed to match the impedance of the SAW device at resonance to that of the driver. To design the matching network, the SAW device was first characterized using a network analyzer as shown in Fig. 5.8. As seen from this plot, the SAW device has a resonance at 177MHz which is within the predicted range of 165MHz to 195MHz. Though the measured S_{11} has a resonance at 177MHz, it is still very different from the S_{11} simulated using the equivalent circuit model in Chapter 1. This is because the equivalent circuit model does not take into account acoustic reflections and echo and also the impact of the mass and stiffness of the metal IDT on the generation of surface waves. The values of series inductor and shunt capacitances of the matching network can be obtained using simulations as $C_1 = 5.8$pF and $L_1 = 150$nH. Based on commercially available inductor datasheets, an equivalent series resistance (ESR) of 2Ω was assumed for the inductor resulting in a reasonable $Q \approx 30$. As shown in Fig. 5.9, the peak power delivered to the SAW device from the output driver increases from 0.05mW when driven directly to around 0.5mW when driven through the matching network. In both the cases, a pair of bond wire inductances were assumed to connect to SAW devices and CMOS driver output pads. Each of the bond wire were assumed to be an inductance of 3nH with a ESR of 1Ω (with $Q \approx 2$). From these simulations, it is evident that the use of matching network has increased the power delivered to the SAW device by a factor of 10.

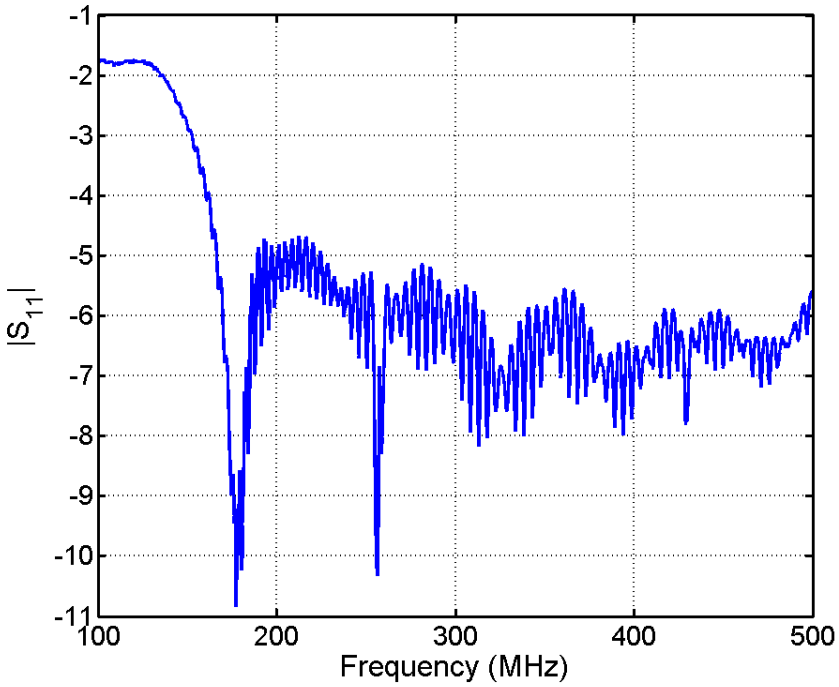


Figure 5.8: $|S_{11}|$ of the SAW device as characterized using a network analyzer

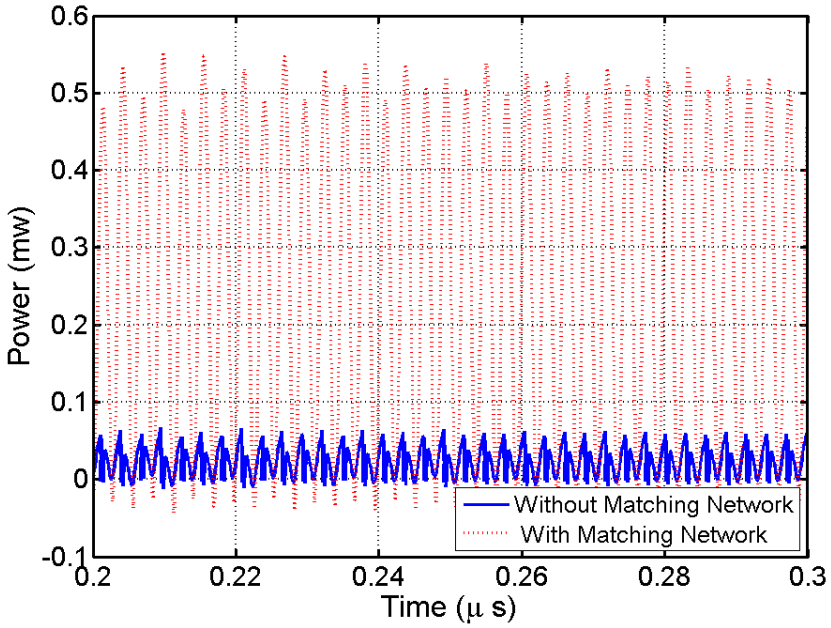


Figure 5.9: Power delivered to the SAW device with and without impedance matching network

5.5 Summary

Table 5.2 summarizes the key metrics of the locomotive system proposed in this work and compares it to the locomotive systems presented in [3] and [5]. As summarized in the table, the power consumption of this project is quite high. While the novelty of this work was to propose a complete locomotive system that uses SAW based propulsion scheme, the fact that the SAW device require electrical excitation at a frequency between 165MHz and 195MHz meant that there were multiple blocks including the VCO and divider that consumed switching power. Moreover, using the WPT frequency of 100MHz meant that a second reference clock divider was employed which further increased power consumption. Additionally, this work employed external components including an off-chip impedance matching network and a PCB based receiver coil, which limits the overall size of the system. While [5] demonstrated a smaller locomotive system, their first prototype presented in [6] utilized a system on a PCB that enclosed a circular area of 5cm diameter. The work presented here is smaller than that. Moreover, [3] requires an external magnetic field to enable propulsion using Lorentz force. This in turn meant the use of larger external magnets which in turn makes the overall size of the system much larger. Both [3] and [5] utilized a communication scheme that enabled digital information to be transmitted to the locomotive system that can be used to control direction of motion. Both these references employed a form of on amplitude modulation scheme on the carrier used to power these systems wirelessly to achieve this communication. Since the work presented here employed a single SAW device, there was no scope for direction control and hence there was no requirement for a communication scheme.

Table 5.2: Summary of locomotive system

Specification	This Work	[3]	[5]
Technology	180nm CMOS	350nm CMOS	65nm CMOS
Supply	1.1V	2V/1.3V	0.7V
Battery	No	No	No
Propulsion	SAW	Electrolytic	Lorentz
Scheme		bubbles	force
RF Carrier Frequency	100MHz (Power)	10MHz (Power & Communication)	1.86GHz (Power & Communication)
Total Power Consumption	550μW (CMOS) + 500μW (SAW)	207μW/ 180μW	267μW
Size	1.5cm X 1.9cm (RX coil) 1.5mm X 1.5mm (Die) 1cm X 1cm (SAW device)	4.6mm X 4.6mm	2mm X 2mm
External Components	Yes (PCB coil, matching network)	No	Yes (PCB antenna, Magnet)

6. CONCLUSION

With higher levels of integration possible, locomotive ICs are becoming popular topic for research. Since locomotive systems typically employ wireless power harvesting, resonant magnetic coupling was analysed in a typical two coil near field wireless power transfer system. It was shown that using a simple rearrangement of circuit components, the efficiency of wireless power transfer can be improved significantly. The analysis was validated by measurement results that showed up to 10dB improvement in wireless power transfer by changing the nature of resonance from series to parallel in both transmitter and receiver coils.

This work implemented the CMOS building blocks for a SAW transducer based locomotive IC. The CMOS IC included a PLL that provides the electrical excitation for the SAW device and power conditioning blocks including a rectifier that generates a DC voltage from the receiver coil in a wireless power transfer system, a reference generator circuit and a regulator that provides a regulated power supply for the PLL. Silicon measurements were made on the fabricated CMOS front end and it was shown that the front end functions as expected and consume 529μW of power. Addionally wireless power transfer was demonstrated with a pair of PCB based coils that can deliver power to the CMOS front end with efficiency of close to 80% at 5mm and 25% at 1cm

6.1 Future Work

This project utilized PCB based receiver coil for harvesting inductive/near field wireless power. The dimensions of the coil limited the overall dimensions of the system. The system can be further miniaturized by use of on-chip receiver coils. Additionally, the output impedance of the driver can be designed to match the

impedance of the SAW device. This will remove the need for the off-chip impedance matching network that also limits miniaturization of the system.

The challenge in employing on-chip coils is that wireless power transfer efficiency is reduced. This is the result of low Q and lower area of flux coupling offered by a smaller on-chip coil. Consequently, rectifier efficiency can be improved by using more advanced circuit topologies. The overall power requirements can be reduced by using new architecture in place of PLL to excite SAW transducer. One possibility is to use the SAW device itself as a resonant structure as in a LC tank VCO. Such a circuit will employ a negative resistance to create oscillations at the resonant frequency of the SAW device. As a result, such a structure will be inherently self-tuned and will not require a PLL loop and reference clock to tune it, thus saving power consumed by those blocks.

As the next step after demonstrating locomotion using a SAW device powered by the CMOS front end presented in this work, a locomotive system with multiple SAW devices can be pursued. Unlike the work presented here, such a system will have ability to move in multiple directions. Similar to the work presented in [5], a communication scheme that can be implemented as an amplitude modulation of the carrier used for wireless power transfer. Using a on-chip demodulator, the communicated bit stream can be decoded and by enabling or disabling one or more of the SAW devices, the direction of motion can be selected.

REFERENCES

[1] R. Feynman, "There's Plenty of Room at the Bottom", (Accessed:12-10-2015). [Online]. Available: http://www.zyvex.com/nanotech/feynman.html,

[2] G. Ciuti, A. Menciassi, and P. Dario, "Capsule Endoscopy: From Current Achievements to Open Challenges," *IEEE Reviews in Biomedical Engineering*, vol. 4, pp. 59–72, 2011.

[3] D. Pivonka, A. Yakovlev, A. Poon, and T. Meng, "A mm-Sized Wirelessly Powered and Remotely Controlled Locomotive Implant," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, no. 6, pp. 523–532, Dec 2012.

[4] P.-L. Huang, P.-H. Kuo, Y.-J. Huang, H.-H. Liao, Y.-J. Yang, T. Wang, Y.-H. Wang, and S.-S. Lu, "A Controlled-Release Drug Delivery System on a Chip Using Electrolysis," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 3, pp. 1578–1587, March 2012.

[5] J.-Y. Hsieh, P.-H. Kuo, Y.-C. Huang, Y.-J. Huang, R.-D. Tsai, T. Wang, H.-W. Chiu, Y.-H. Wang, and S.-S. Lu, "A Remotely-Controlled Locomotive IC Driven by Electrolytic Bubbles and Wireless Powering," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 6, pp. 787–798, Dec 2014.

[6] P.-H. Kuo, J.-Y. Hsieh, Y.-C. Huang, Y.-J. Huang, R.-D. Tsai, T. Wang, H.-W. Chiu, and S.-S. Lu, "18.7 A Remotely Controlled Locomotive IC Driven by Electrolytic Bubbles and Wireless Powering," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC),*, 2014, pp. 322–323.

[7] M. Karagozler, E. Cheung, J. Kwon, and M. Sitti, "Miniature Endoscopic Capsule Robot using Biomimetic Micro-Patterned Adhesives," in *The First IEEE/RAS-EMBS International Conference on Biomedical Robotics and Biomechatronics, 2006. BioRob 2006.*, Feb 2006, pp. 105–111.

[8] B. Kim, S. Lee, J. H. Park, and J.-O. Park, "Design and Fabrication of a Locomotive Mechanism for Capsule-type Endoscopes using Shape Memory Alloys (SMAs)," *IEEE/ASME Transactions on Mechatronics*, vol. 10, no. 1, pp. 77–86, Feb 2005.

[9] Y. P. J. Bourquin, "Shaping Surface Waves for Diagnostics," Ph.D. dissertation, University of Glasgow, 2012.

[10] L. Reindl, A. Pohl, G. Scholl, and R. Weigel, "SAW-based radio sensor systems," *IEEE Sensors Journal*, vol. 1, no. 1, pp. 69–78, June 2001.

[11] U. Wolff, F. Dickert, G. Fischerauer, W. Greibl, and C. Ruppel, "SAW sensors for harsh environments," *IEEE Sensors Journal*, vol. 1, no. 1, pp. 4–13, June 2001.

[12] Y. Zhu, Y. Zheng, Y. Gao, D. Made, C. Sun, M. Je, and A. Gu, "An Energy Autonomous 400 MHz Active Wireless SAW Temperature Sensor Powered by Vibration Energy Harvesting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 4, pp. 976–985, April 2015.

[13] A. Wixforth, "Acoustically Driven Programmable Microfluidics for Biological and Chemical Applications," *Journal of the Association for Laboratory Automation*, vol. 11, no. 6, pp. 399–405, 2006.

[14] P. Brunet, M. Baudoin, O. B. Matar, and F. Zoueshtiagh, "Droplet Displacements and Oscillations induced by Ultrasonic Surface Acoustic Waves: A Quan-

titative Study," *Physical Review E*, vol. 81, no. 3, p. 036315, 2010.

[15] T. D. Luong and N. T. Nguyen, "Surface Acoustic Wave Driven Microfluidics-A Review," *Micro and Nanosystems*, vol. 2, no. 3, pp. 217–225, 2010.

[16] S. Datta, "Surface Acoustic Wave Devices". Prentice Hall, 1986.

[17] COMSOL, "Two-port Piezoelectric SAW Device", (Accessed:12-10-2015). [Online]. Available: http://www.comsol.com/model/two-port-piezoelectric-saw-device-19155,

[18] E. Koukharenko, S. P. Beeby, M. J. Tudor, N. M. White, T. O'Donnell, C. Saha, S. Kulkarni, and S. Roy, "Microelectromechanical Systems Vibration Powered Electromagnetic Generator for Wireless Sensor Applications," *Microsyst. Technol.*, vol. 12, no. 10, pp. 1071–1077, Aug. 2006.

[19] C. Sauer, M. Stanacevic, G. Cauwenberghs, and N. Thakor, "Power harvesting and telemetry in CMOS for implanted devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 12, pp. 2605–2613, Dec 2005.

[20] P. Vaillancourt, A. Djemouai, J. Harvey, and M. Sawan, "EM radiation behavior upon biological tissues in a radio-frequency power transfer link for a cortical visual implant," in *Proceedings of the 19th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, 1997.* , vol. 6, Oct 1997, pp. 2499–2502 vol.6.

[21] A. Yakovlev, S. Kim, and A. Poon, "Implantable biomedical devices: Wireless powering and communication," *IEEE Communications Magazine*, vol. 50, no. 4, pp. 152–159, April 2012.

[22] A. Poon, S. O'Driscoll, and T. Meng, "Optimal Operating Frequency in Wireless Power Transmission for Implantable Devices," in *29th Annual International*

Conference of the IEEE Engineering in Medicine and Biology Society, 2007. EMBS 2007. , Aug 2007, pp. 5673–5678.

[23] M. Zargham and P. Gulak, "Maximum Achievable Efficiency in Near-Field Coupled Power-Transfer Systems," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, no. 3, pp. 228–245, June 2012.

[24] M. Zargham and P. Gulak, "Integrated CMOS wireless power transfer for neural implants," in *2011 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Nov 2011, pp. 165–168.

[25] L. Xia, J. Cheng, N. Glover, and P. Chiang, "0.56 V, -20 dBm RF-Powered, Multi-Node Wireless Body Area Network System-on-a-Chip With Harvesting-Efficiency Tracking Loop," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 6, pp. 1345–1355, June 2014.

[26] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS Threshold-Compensated RF Energy Harvester," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, Sept 2011.

[27] R. Harrison, "Designing Efficient Inductive Power Links for Implantable Devices," in *Proceedings IEEE International Symposium on Circuits and Systems*, May 2007, pp. 2080–2083.

[28] C. Peters, J. Handwerker, D. Maurath, and Y. Manoli, "A Sub-500 mV Highly Efficient Active Rectifier for Energy Harvesting Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 7, pp. 1542–1550, July 2011.

[29] Y. Lu and W.-H. Ki, "A 13.56 MHz CMOS Active Rectifier With Switched-Offset and Compensated Biasing for Biomedical Wireless Power Transfer Sys-

tems," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 3, pp. 334–344, June 2014.

[30] S. Hashemi, M. Sawan, and Y. Savaria, "A High-Efficiency Low-Voltage CMOS Rectifier for Harvesting Energy in Implantable Devices," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, no. 4, pp. 326–335, Aug 2012.

[31] Q. Li, R. Zhang, Z. Huang, and Y. Inoue, "A Low Voltage CMOS Rectifier for Wirelessly Powered Devices," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2010, pp. 873–876.

[32] J. Wardlaw and A. Karsilayan, "Self-Powered Rectifier for Energy Harvesting Applications," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 3, pp. 308–320, Sept 2011.

[33] S. Mandal and R. Sarpeshkar, "Low-Power CMOS Rectifier Design for RFID Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 6, pp. 1177–1188, June 2007.

[34] B. Razavi, "Design of Analog CMOS Integrated Circuits",1st ed., Tata McGraw-Hill, 2002.

[35] M. Mansuri, "Low-Power Low-Jitter On-Chip Clock Generation," Ph.D. dissertation, University of California, Los Angeles, 2003.

[36] B. Razavi, "Design of Integrated Circuits for Optical Communications", 1st ed. McGraw-Hill, Inc., 2003.

[37] C. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35μm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, July 2000.