POWER ELECTRONIC SOLUTIONS FOR INTERFACING OFFSHORE WIND

TURBINE GENERATORS TO MEDIUM VOLTAGE DC COLLECTION GRIDS

A Dissertation

by

MICHAEL T DANIEL

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Chair of Committee,	Prasad Enjeti
Committee Members,	Le Xie
	Shankar Bhattacharyya
	Won-jong Kim
Head of Department,	Miroslav Begovic

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ABSTRACT

Here in the early 21st century humanity is continuing to seek improved quality of life for citizens throughout the world. This global advancement is providing more people than ever with access to state-of-the-art services in areas such as transportation, entertainment, computing, communication, and so on. Providing these services to an ever-growing population while considering the constraints levied by continuing climate change will require new frontiers of clean energy to be developed. At the time of this writing, offshore wind has been proven as both a politically and economically agreeable source of clean, sustainable energy by northern European nations with many wind farms deployed in the North, Baltic, and Irish Seas.

Modern offshore wind farms are equipped with an electrical system within the farm itself to aggregate the energy from all turbines in the farm before it is transmitted to shore. This collection grid is traditionally a 3-phase medium voltage alternating current (MVAC) system. Due to reactive power and other practical constraints, it is preferable to use a medium voltage direct current (MVDC) collection grid when siting farms >150 km from shore. To date, no offshore wind farm features an MVDC collection grid. However, MVDC collection grids are expected to be deployed with future offshore wind farms as they are sited further out to sea.

In this work it is assumed that many future offshore wind farms may utilize an MVDC collection grid to aggregate electrical energy generated by individual wind turbines. As such, this work presents both per-phase and per-pole power electronic

converter systems suitable for interfacing individual wind turbines to such an MVDC collection grid. Both interfaces are shown to provide high input power factor at the wind turbine while providing DC output current to the MVDC grid. Common mode voltage stress and circulating currents are investigated, and mitigation strategies are provided for both interfaces. A power sharing scheme for connecting multiple wind turbines in series to allow for a higher MVDC grid voltage is also proposed and analyzed. The overall results show that the proposed per-pole approach yields key advantages in areas of common mode voltage stress, circulating current, and DC link capacitance, making it the more appropriate choice of the two proposed interfaces for this application.

For my family.

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1. INTRODUCTION AND LITERATURE REVIEW

This work presents two novel power electronic methods for interfacing offshore wind turbine generators (WTGs) to medium voltage DC (MVDC) collection grids. The location of the proposed power electronic interfaces can be observed in Figure 1-1. The power electronic interfaces investigated in this work are proposed for WTGs rated for > 5 MW located in wind farms > 50 km from shore. While no offshore wind farms currently incorporate an MVDC collection grid, this work anticipates the necessity of such a topology based on the increasing trend in inter-turbine spacing and distance from shore.

The key elements that are addressed by this work include the important features that must be included in a power electronic interface for such an application, as well as its design, electrical behavior, and performance under various operating conditions.
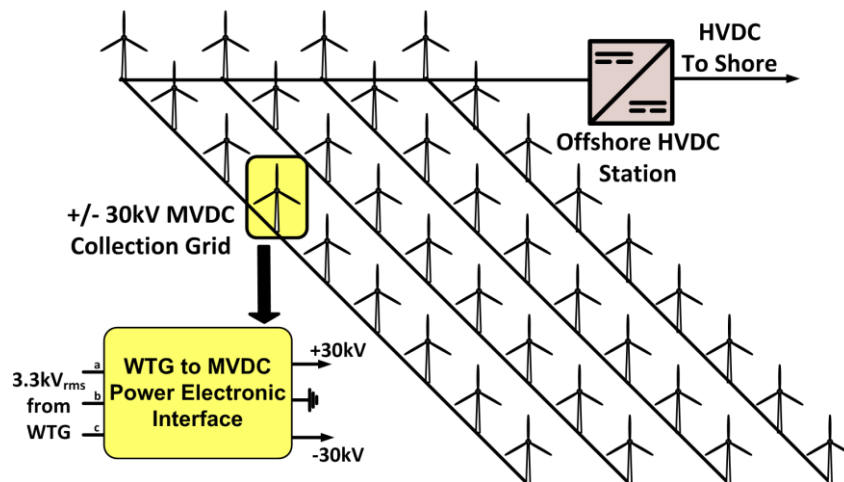
Figure 1-1: Offshore wind farm with MVDC collection grid.

Considering the superposition of projected global energy supply and demand in Figure 1-2 it is clear that new energy resources must be developed to prevent a global energy shortfall [1]

Due to the constraints placed on energy development by policy designed to prevent global climate change, many nations are seeking to develop alternative energy resources that are both environmentally acceptable and economically viable [2].

As such, many nations for which it is a practical option have begun aggressively developing their offshore wind energy resources in an effort to secure reasonably priced and reliable energy while limiting climatological impact, improving energy security, and reducing dependence on less attractive alternatives like large nuclear or hydroelectric power facilities [3]-[5].
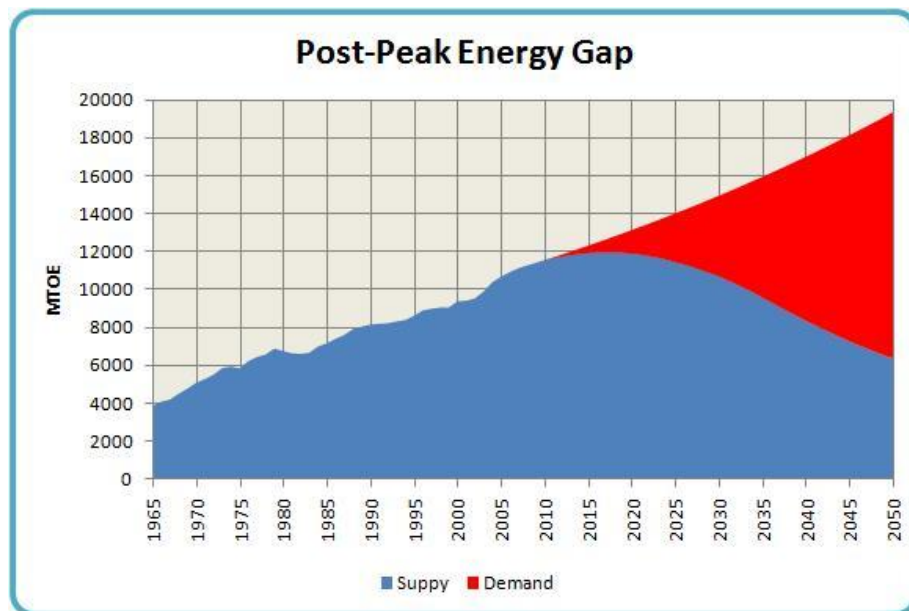
Figure 1-2: Illustration of projected global energy shortfall. Source: Paul Chefurka, 2008 [1]. *Reused with courtesy of Paul Chefurka*.

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With a single 5 MW turbine capable of powering 3500 homes while eliminating 7200 tons of carbon dioxide and 160 tons of sulfur dioxide annually, offshore wind is an attractive alternative energy resource [6].

While much of the wind energy development projected by Figure 1-3 [7] is on land, there remains tremendous growth potential for offshore wind energy development as reinforced by Figure 1-4 [8] and recent growth shown in Figure 1-5 [9]
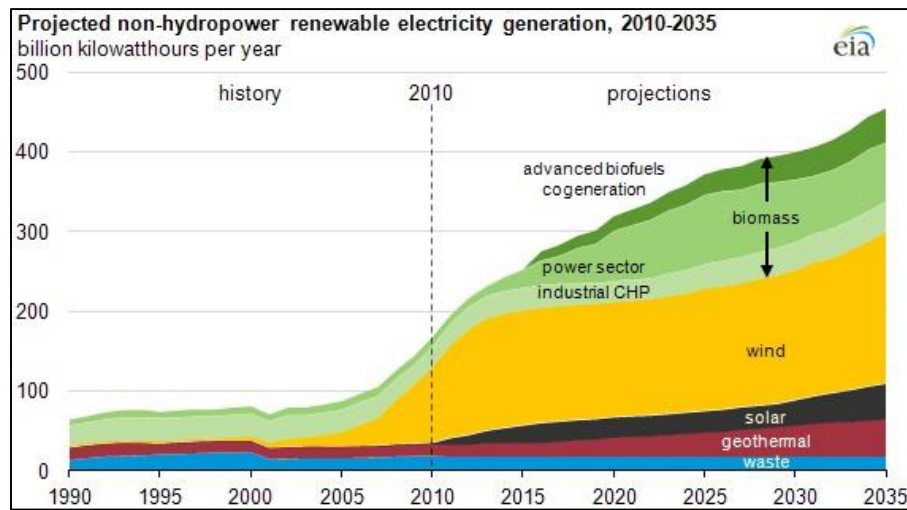
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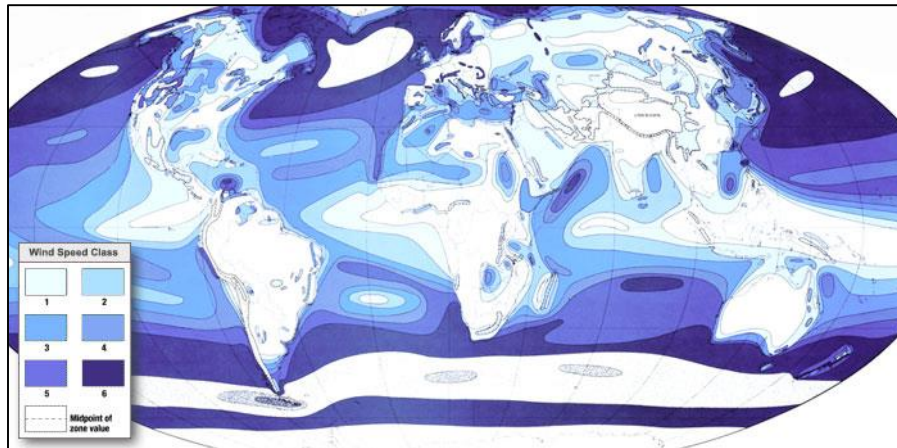
Figure 1-4: Estimate of global wind energy resources. Source: U.S. Department of Energy, 1980 [8]. *Reused with courtesy of the U.S. Department of Energy.*
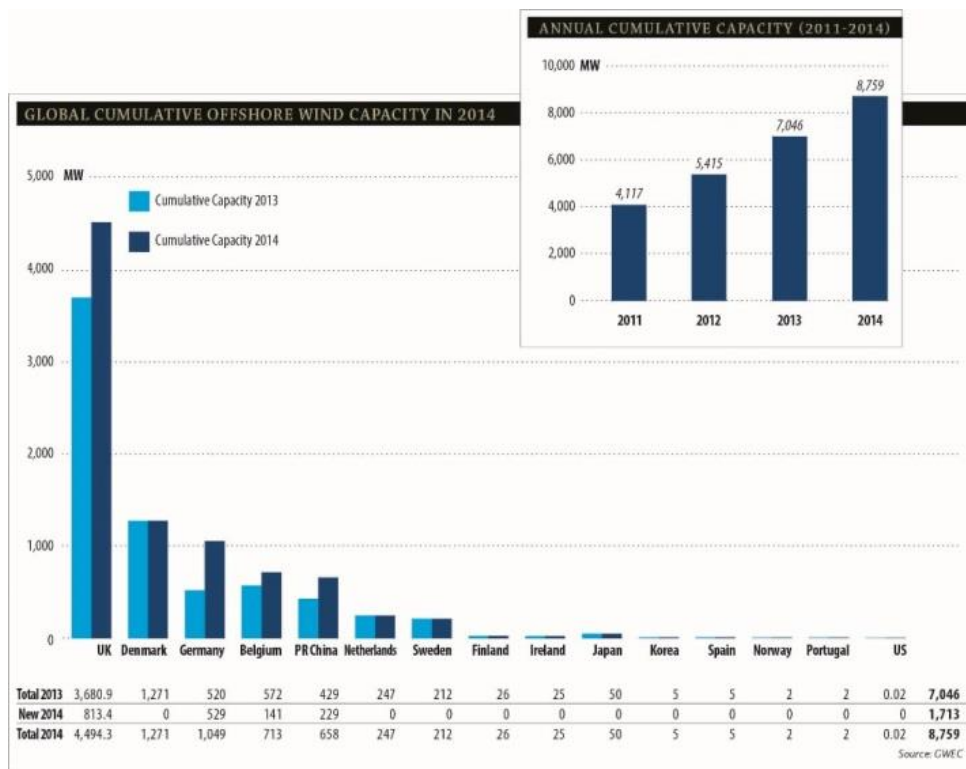
Figure 1-5: Recent development of offshore wind energy resources. Source: Global Wind Energy Council, 2015 [9]. *Reused with courtesy of the Global Wind Energy Council.*

One of the key differentiators between offshore wind and other competing renewable energy resources is its dependability. For example, solar photovoltaic (PV) installations by their very nature must have practically zero output for nearly half of every day, and can suffer dramatic changes from near zero to full power as clouds interfere with the incident solar radiation. These characteristics are obvious in Figure 1-6 [10]. Offshore wind farms are even superior to their onshore counterparts in terms of intermittency. Figure 1-7 shows the wind speed over a 24-hour period at the 576 MW Altamont Pass wind farm in Livermore, CA dropping well below the typical WTG cut-in speed of 3.5 m/s for much of the day which[11]. The wind speed for a 24-hour period near Germany's 288 MW Meerwind Ost/Sud offshore wind farm, shown in Figure 1-8, only varies from 8 to 12 m/s, corresponding to an approximately 50% variation in WTG output power, far better than the 100% variation observed in Figures 1-6 and 1-7 [12].
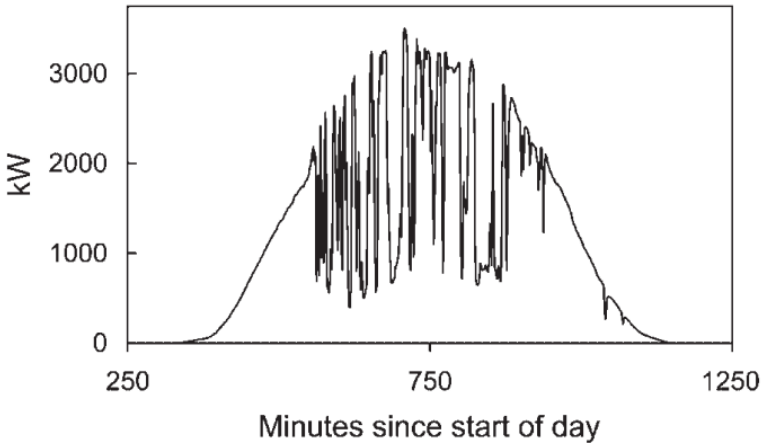
Figure 1-6: Power production at TEP Springerville PV station. Source: Curtright & Apt, 2007 [10]. *Reused with courtesy of John Wiley & Sons.*
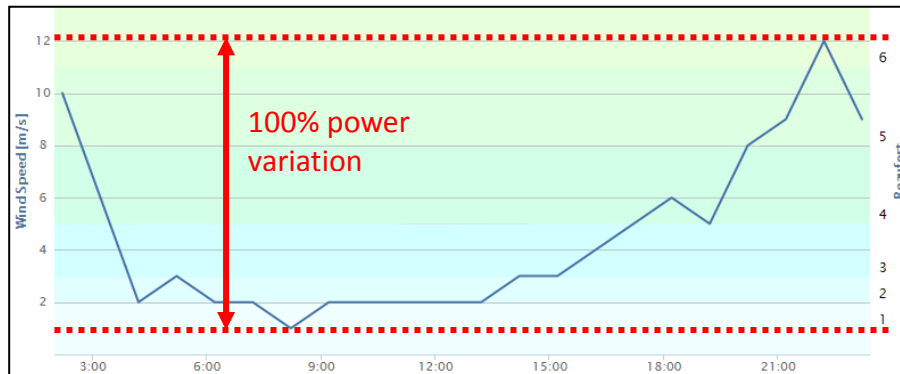
Figure 1-7: Altamont Pass wind speed on 18 April 2015. Source: WindFinder, 2015 [11]. *Adapted with permission of WindFinder.*
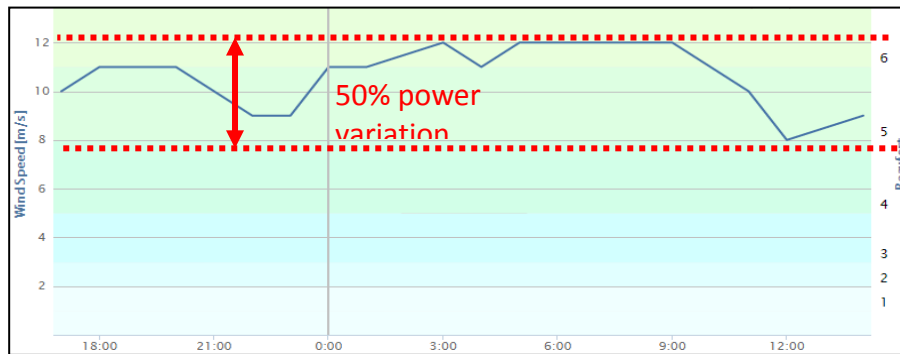
Figure 1-8: Wind speed near Meerwind Ost/Sud on 21/22 April 2015. Source: WindFinder, 2015 [12]. *Adapted with permission of WindFinder.*

Considering the tremendous recent growth and future potential outlined by Figures 1-4 and 1-5 it is important to consider the direction of that growth as outlined by Figure 1-9 [13],[14] to gain insight into the characteristics of future offshore wind farms [15]. While current wind farms like Global Tech I and BARD Offshore I are only designed to provide 200-400 MW and are sited about 100 km from shore, future projects several times that power are to be sited more than twice the distance from shore.

Due to the large distance to shore of current wind farms, high voltage direct current (HVDC) is used to transport electrical energy to shore [16]. There is also a collection grid within the wind farm to aggregate the energy from each WTG before conversion to HVDC and transit to shore. Figure 1-10 shows the Riffgat wind farm.
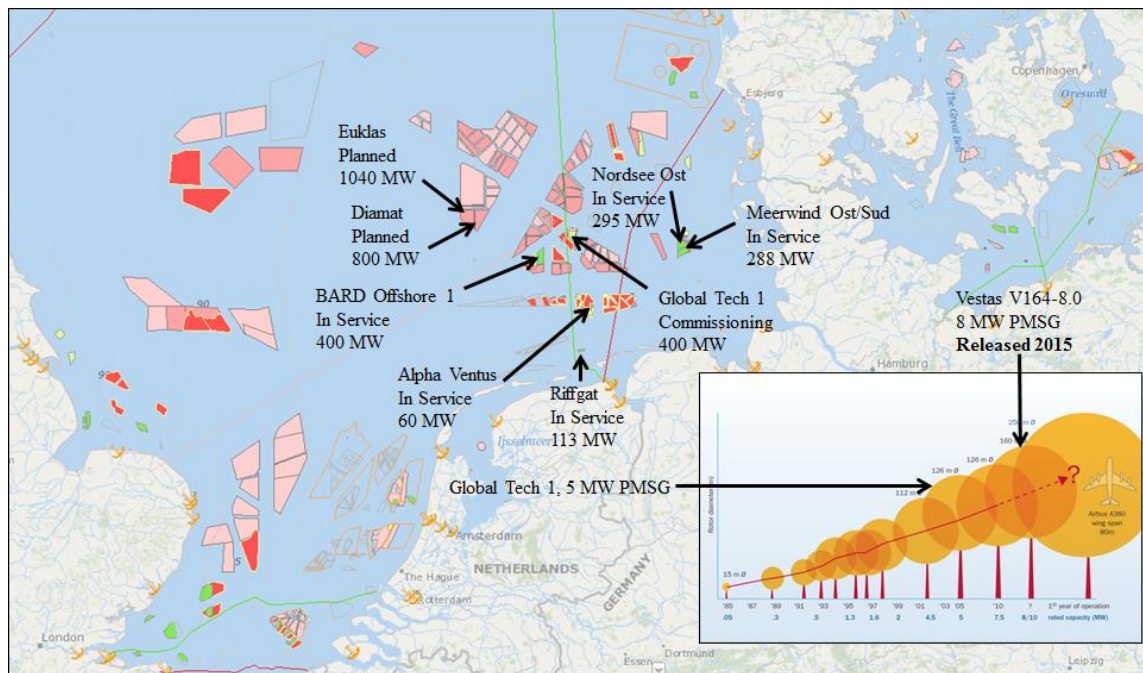
Figure 1-9: Large offshore wind farms of the future will be sited further to sea and require more space between individual turbines. Background image source: 4COffshore, 2015 [14]. *Adapted with permission of 4COffshore.* Inset image source: European Wind Energy Administration 2011 [13]. *Adapted with permission of the European Wind Energy Administration.*

Current offshore wind farm collection grids are 3-phase medium voltage AC (MVAC) with a rated voltage of 33 kV, as shown in Figure 1-11. With HVDC already being used to transmit the energy to shore and inter-turbine spacing of nearly 1 km [17], an MVDC collection grid may be more suitable for use in future offshore wind farms.

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Figure 1-10 Riffgat offshore wind farm and offshore substation. Photo: Siemens AG 2013 [18]. *Reused with courtesy of Siemens AG.*
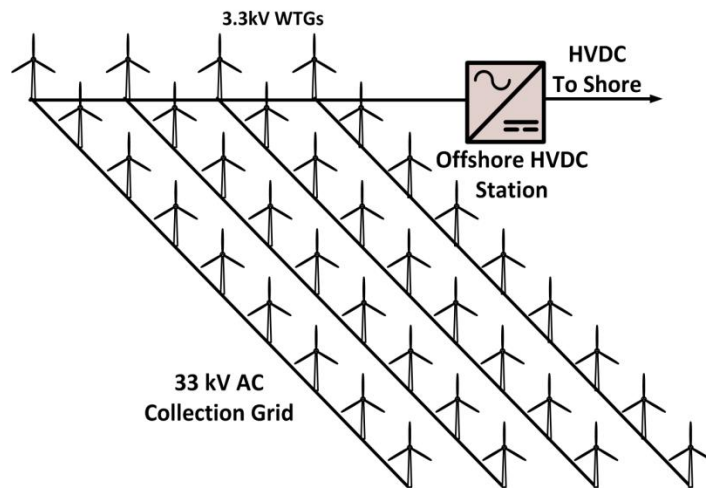
Figure 1-11: Offshore wind farm with 33 kV 3-phase MVAC collection grid.

Figure 1-12: Example of an offshore HVDC converter station. Photo: Siemens AG 2014 [19]. *Reused with courtesy of Siemens AG.*

A practical example of the MVAC to HVDC converter described as "Offshore HVDC Station" in Figure 1-11 is shown in Figure 1-12. The structure of an offshore wind farm utilizing an MVDC collection grid is shown in Figure 1-13.
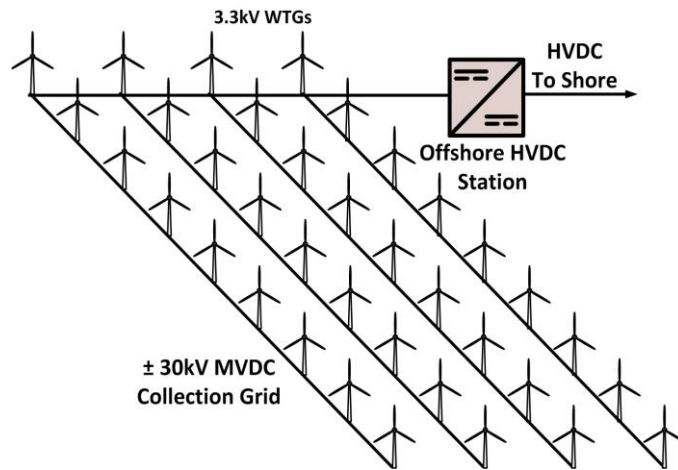
Figure 1-13: Offshore wind farm with ±30 kV MVDC collection grid.

Compared to the traditional MVAC collection grid the proposed MVDC alternative exhibits the advantages and disadvantages outlined in Table 1-1 [20].

Table 1-1: Outline of advantages and disadvantages of MVDC collection grids.

MVDC Advantages	MVDC Disadvantages
• No line frequency transformers present • Fewer undersea cables • More power flow control options • HVDC station interface is simplified • Cable current & insulation ratings more effectively used	• Addition of converter cost • Addition of converter losses • Electromagnetic interference • Circulation currents & common mode voltage stress • Protection and control complexity

The net result of the advantages and disadvantages outlined in Table 1 is that MVDC collection grids are better suited than MVAC collection grids for aggregated energy in large wind farms distant from shore, whereas MVAC grids may be better suited for use in small, dense wind farms only a few kilometers from shore.

Considering the future direction of offshore wind development described by Figure 1-9 it appears that MVDC collection grids may be a necessity for development of the next generation of offshore wind farms.

As such, this work proposes two candidate power electronic interfaces suitable for interfacing WTGs to an MVDC grid as described in Figure 1-1. The electrical behavior, control, and other salient characteristics of each approach are analyzed.

Several other power electronic approaches have been proposed for use as an interface between an offshore WTG and MVDC collection grid [21]-[29]. The previously proposed approaches can be divided into two broad groups: those that feature galvanic isolation and those that do not.

The first approach considered is proposed by Chen et al. [21]. This approach features a resonant topology that can provide high DC/DC gain, and thus is only proposed as the DC/DC stage in the WTG-to-MVDC interface as shown in Figure 1-14. Note that numerous active switches and tuned passive components are required.
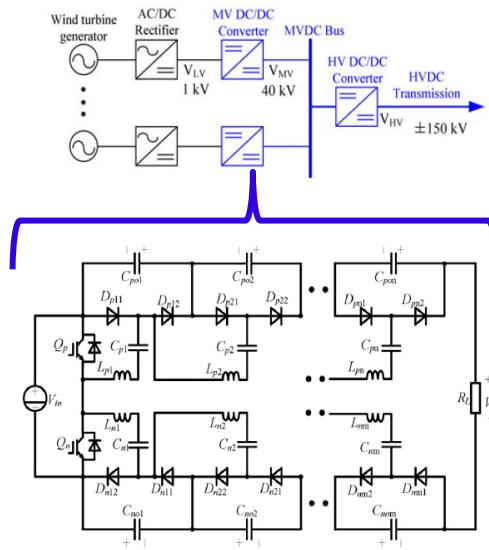
Figure 1-14: Resonant interface proposed by Chen et al. © 2013 IEEE [21]. *Adapted with permission of the IEEE.*
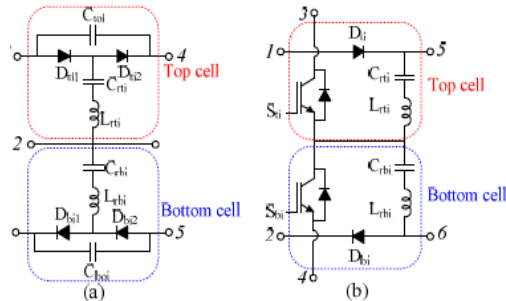
Structure of module #i. (a) SL-based module. (b) DS-based module.
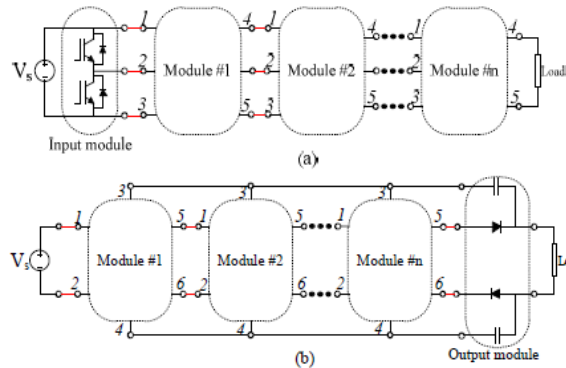
Figure 1-15: Modular resonant DC/DC proposed by Parastar et al. © 2014 IEEE [22]. *Adapted with permission of the IEEE.*

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The second non-isolated approach to consider is that proposed by Parastar et al. [22] in which they describe a modular resonant converter suitable for the DC/DC stage of the WTG-t-MVDC interface as shown in Figure 1-15. Similar to the approach proposed by Chen et al. this topology requires numerous active switches and tightly tuned passive elements to achieve high DC/DC voltage gain.

A third non-isolated approach relevant to this work is Jovcic's capacitive-coupled topology shown in Figure 1-16 [23]. Note the high peak-to-average current at the output capacitor in this approach.

While non-isolated topologies may be suitable for the DC/DC gain stage alone, the need to provide galvanic isolation is present in this application. Therefore, others have proposed both DC/DC and end-to-end approaches that include galvanic isolation.
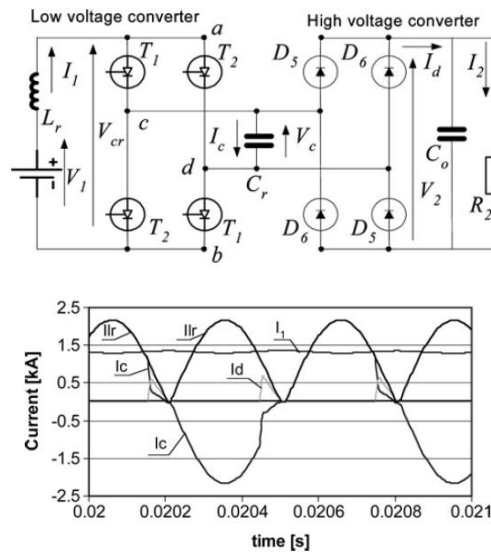
Figure 1-16: Capacitive coupled approach proposed by Jovcic. © 2009 IET [23]. *Adapted with permission of the IET.*

The approach proposed by Lam et al. [24] considers a soft-switching converter and diode rectifier output, shown in Figure 1-17. The input side of this approach requires numerous series-connected capacitors that must be balanced, and the output capacitor lacks the ability to be series connected with other WTGs in the offshore wind farm.
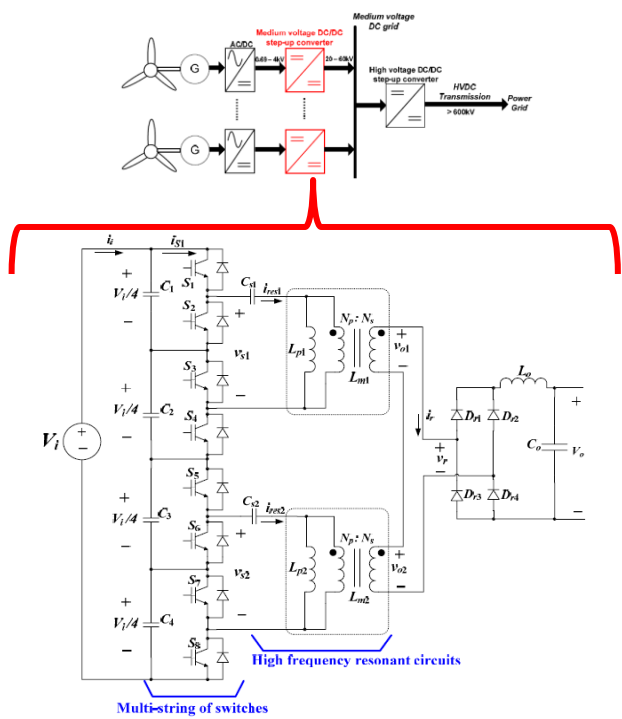
Figure 1-17: Isolated DC/DC approach proposed by Lam et al. © 2014 IEEE [24]. *Adapted with permission of the IEEE.*

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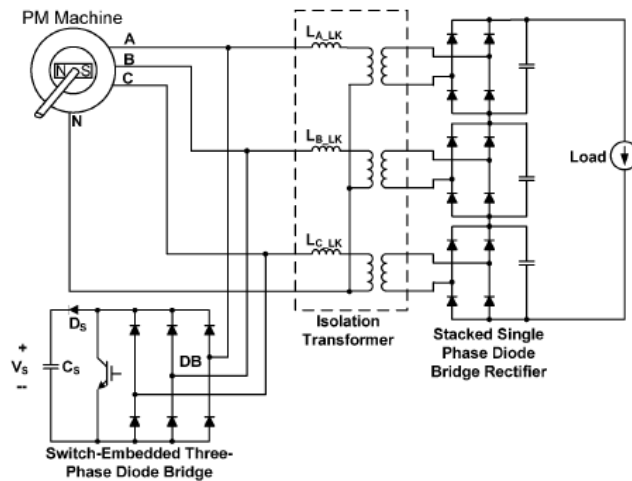
Figure 1-18: Medium frequency generator approach proposed by Prasai et al. © 2008 IEEE [25].
Adapted with permission of the IEEE.

The approach proposed by Prasai et al. [25], shown in Figure 1-18, assumes a medium frequency generator operating at approximately 1200 Hz to allow a medium frequency transformer to be used without then need for frequency conversion power electronics at the front-end. While this approach does feature a compact medium frequency transformer and only a single active switch, the medium frequency generator would require either a large number of poles or a large gearbox to yield the desired medium frequency from the low frequency turbine. Also note the proposed output voltage is only a few kV, necessitating another voltage boosting stage before the final interface with the MVDC grid.

Previous work has not only shown the necessity of using a DC grid to collect wind turbine energy, but has investigated several power conversion and control

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strategies for wind turbines in general [30]-[56]. This work provides a basis for the power electronic interface approaches proposed in this work.

In this work we address the problem of how to connect each turbine to an MVDC collection grid. Each WTG must be connected to the MVDC grid safely, reliably, and efficiently in order to build a wind farm more than 150 km from shore that can harvest the best wind energy resources with less visual and environmental impact.

The problem is that modern wind turbines output their energy at 3,300 volts AC, but the DC grid must be at least 30,000 volts DC. So the turbines can't be directly connected to the DC grid; they need some sort of interface to take the power from the turbine, process it, and then inject it into the DC grid.

This work presents two novel power electronic interfaces suitable for integrating state-of-the-art offshore wind turbine generators (WTGs) with medium voltage DC (MVDC) collection grids. The first interface is based on three end-to-end power electronic modules, one per WTG phase, hence it is considered a "per-phase" interface. The second interface is based on the same end-to-end module structure with a three-phase input rectifier at the module front-end and one module per MVDC pole, hence it is considered a "per-pole" interface. Both interfaces utilize a high frequency transformer (HFT) to provide galvanic isolation while reducing interface mass and volume. Module design, steady-state and dynamic electrical behavior, and practical control strategies are developed for both interfaces.

Sections 2 through 5 describe the results and impacts of this research in detail. Each section focuses on a unique component of the overall research.

Section 2, *A New Wind Turbine Interface to MVDC Collection Grid with High Frequency Isolation and Input Current Shaping*, describes the design, analysis, and key features of a new per-phase approach for connecting individual offshore wind turbines to a medium voltage DC collection Grid. Simulation and experimental results demonstrate the desired high displacement power factor at the WTG terminals

Section 3, *An Improved Offshore Wind Turbine to MVDC Grid Interface using High Frequency Resonant Isolation and Input Power Factor Control*, outlines an advanced per-pole approach for the wind turbine to MVDC grid interface which requires less DC link capacitance and the potential for improved common mode voltage balancing among high frequency transformers.

Section 4, *Exploring Common Mode Voltage Stress and Circulating Currents in Offshore Wind Turbine to MVDC Collection Grid Interfaces*, investigates common mode voltage stress and circulating currents in both per-phase and per-pole interfaces proposed in the previous sections. This section also proposes and analyzes a circulating current mitigation strategy that reduces ground current returning to the WTG neutral in both proposed interfaces.

Section 5, *A Power Sharing Scheme for Series Connected Offshore Wind Turbines in a Medium Voltage DC Collection Grid*, analyzes how power electronic converter blocks from the proposed interfaces in previous sections can be combined with a power sharing converter to allow pairs of series connected WTGs to be interfaced to an MVDC collection grid. Simulation results demonstrate operation in power sharing mode with a power unbalance of 1:2 between series connected WTGs.

2. A NEW WIND TURBINE INTERFACE TO MVDC COLLECTION GRID WITH HIGH FREQUENCY ISOLATION AND INPUT CURRENT SHAPING[*]

A new power electronic interface suitable for the integration of next-generation offshore wind turbines with medium voltage DC (MVDC) collection grids is introduced in this work. A practical design case study provides guidance for further development of the proposed interface. Detailed simulations show acceptable operation of the proposed approach from 25% to 100% rated power, including step changes in WTG input power. Simulation results demonstrate >0.95 displacement power factor magnitude, near sinusoidal WTG current, continuous output current, stiff DC link voltages, and inverter zero-current switching (ZCS). Preliminary hardware results from a 250 V_{dc}, 700 W lab-scale prototype are introduced, demonstrating input rectifier boost characteristic with a dominant input current fundamental and >0.95 displacement power factor magnitude. The DC link current has a large peak-to-average ratio as expected, and DC link capacitor voltage balance is achieved via adjustment of relative duty cycles between high- and low-side active rectifier switches.

2.1 Introduction

As people around the globe continue to achieve higher standards of living and economic power, humanity must continually develop new energy resources to sustain

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the ever-growing demand for services such as transportation, communication, computing, entertainment, etc[2]. To simultaneously satisfy the constraints placed on energy production by anticipated climate change, many nations are seeking to develop offshore wind energy as an environmentally and economically acceptable source of sustainable energy for the future[3]-[5].

Offshore wind farms are being sited further from shore than ever before[13], with Germany's Global Tech 1 farm, completed in 2014 and currently undergoing commissioning, constructed nearly 100 km out to sea[57]. In addition, state-of-the-art WTGs are available at 5 MW at 3.3 kV requiring nearly 1 km of inter-turbine spacing, as in the case of Germany's Alpha Ventus farm[17]. With 8 and 10 MW WTGs likely entering service in the near future [15], turbine spacing in excess of 1 km may be necessary for efficient operation.

The great distance to shore has made high voltage direct current (HVDC) a necessity in transporting offshore wind energy to customers on shore to eliminate reactive power requirements and reduce cabling cost and complexity[16].

The growing inter-turbine spacing, combined with the necessity of using an HVDC link to shore makes the use of an MVDC collection grid architecture more suitable for aggregating WTG energy within the farm than the traditional MVAC alternative. Several architectures have been proposed for interfacing MVDC collection grids to the HVDC link to shore [21],[24],[26],[27]. Figure 2-1 illustrates an MVDC collection grid architecture with two possible approaches for interfacing the MVDC grid to the offshore HVDC converter station.

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Compared to a traditional MVAC collection grid [26], the MVDC option has the advantages and disadvantages listed in Table 2-1, making the MVDC option a net disadvantage for small, dense wind farms close to shore, and a net advantage for large, distant wind farms.
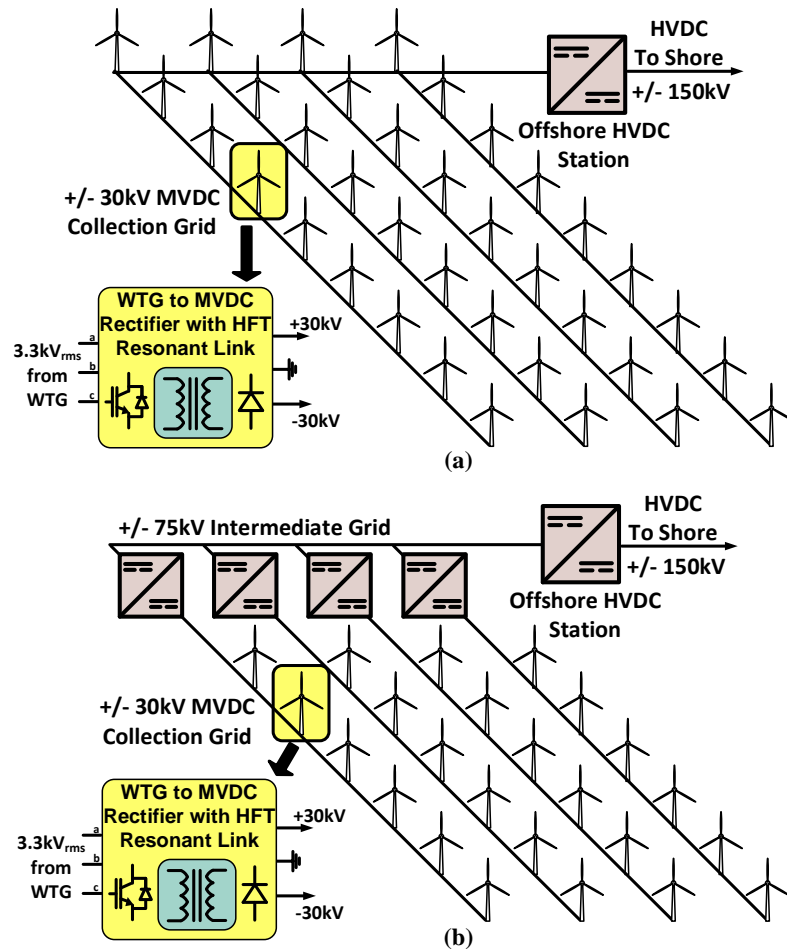
Figure 2-1: Example of offshore wind farm with WTG to ±30 kV MVDC collection grid interface. The MVDC grid can then be (a) interfaced directly to the offshore HVDC converter station [21], [24] or (b) boosted to an intermediate voltage level before conversion to HVDC for transmission to shore as proposed in [26], [27].

Table 2-1: Advantages and disadvantages of MVDC vs MVAC collection grid

MVDC Advantages	MVDC Disadvantages
• Elimination of line frequency transformers. • Simplification of collection grid undersea cabling. • Mitigation of inter-turbine power flow issues. • Simplification of HVDC converter station interface. • More effective use of cable current & insulation ratings.	• Added cost of converter • Added losses of converter • Electromagnetic interference • Common mode voltage stress and circulating ground currents • Complexity of protection, control, and circuit breaking schemes.

This work focuses on a new approach to interfacing individual WTGs to the MVDC collection grid. Several methods have been proposed for this interface. A non-isolated resonant switched capacitor (RSC) topology is proposed in [21] that utilizes cascaded RSC modules to achieve significant voltage gain, while the authors of [24] propose a modular multilevel inverter utilizing resonant ZVS to achieve voltage gain and isolation. In [26] and [27] multiple converter stages are proposed between the WTG and the HVDC link to shore, potentially requiring additional offshore platforms. Medium frequency generators have been proposed as the basis for WTGs interfacing to an MVDC grid via a simple diode rectifier in [25], although this alternative generator may be too large for a WTG due to requiring a large number of poles or gearbox to attain medium frequency operation. A modular multilevel converter architecture is proposed in [28] although it requires a four- armature machine to achieve substantial DC output voltage and does not provide galvanic isolation. A bridgeless PFC input scheme is proposed in [29], along with a complicated transformer connection to provide isolation. Parastar and Seok [22] propose a modular RSC approach lacking isolation, similar to the approach in [21]. Jovcic [23] proposed a non-isolated capacitive-coupled inverter

topology with applications in MW-scale DC/DC conversion; however the lack of isolation and large peak-to-average ratio of the output capacitor current make this converter unsuitable to the application proposed in this paper. A multilevel active neutral point clamped (NPC) approach is proposed in [58], while a single-stage non-isolated resonant approach is considered in [59]. Deng and Chen [60] propose an NPC-based isolated approach utilizing a passive filter on the medium frequency transformer primary.

This work proposes a per-phase approach utilizing high frequency resonant isolation while providing output current control to the MVDC bus and input current shaping for PFC at the WTG [61]. A per-pole version of the proposed approach is presented in [62]. Compared to [21]-[29],[58]-[60] the proposed approach has the following advantages:

1) Provides "end-to-end" conversion interface from WTG to MVDC grid

2) Provides galvanic isolation

3) High output diode rectifier device rating utilization

4) Fewer inverter input capacitor voltage levels to balance

5) Uses conventional direct-drive synchronous generator.

6) Compact high frequency transformer.

7) Resonant link allows ZCS, which more suited to IGBTs than ZVS [63].

8) Input current shaping capability for PFC.

9) Large generator inductance an advantage for multilevel rectifier boost PFC operation.

2.2 Proposed Approach

Figure 2-2 provides a high-level illustration of the proposed approach, while Figure 2-3 details a single end-to-end phase module including the two control schemes. For the proposed approach a direct-drive permanent magnet synchronous generator (DD-PMSG) is assumed. This type of machine has a synchronous reactance of approximately 0.6 per-unit, which is inversely proportional to machine volume [64], [65]. The MVDC voltage is considered to be fixed by the HVDC converter, necessitating current control at the converter output. Hence black-start from a de-energized state is achieved by first energizing the offshore HVDC station and MVDC grid from the shore-based HVDC converter station, which is similar to how a traditional VSC HVDC would be energized.
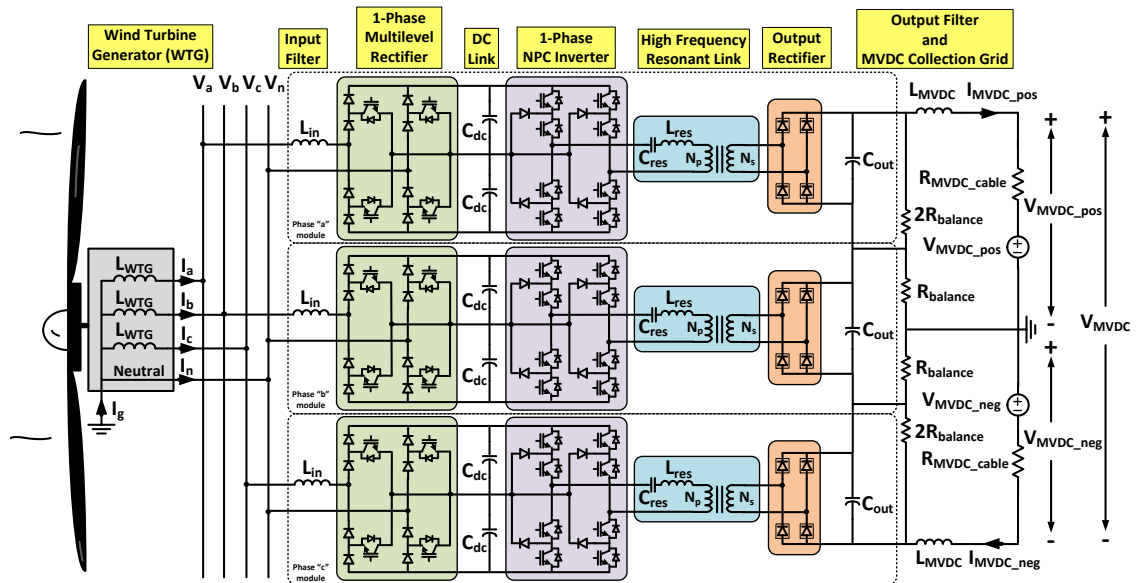
Figure 2-2: The proposed converter interface between WTG and MVDC collection grid using multilevel input rectifier, NPC inverter and high frequency resonant AC link.

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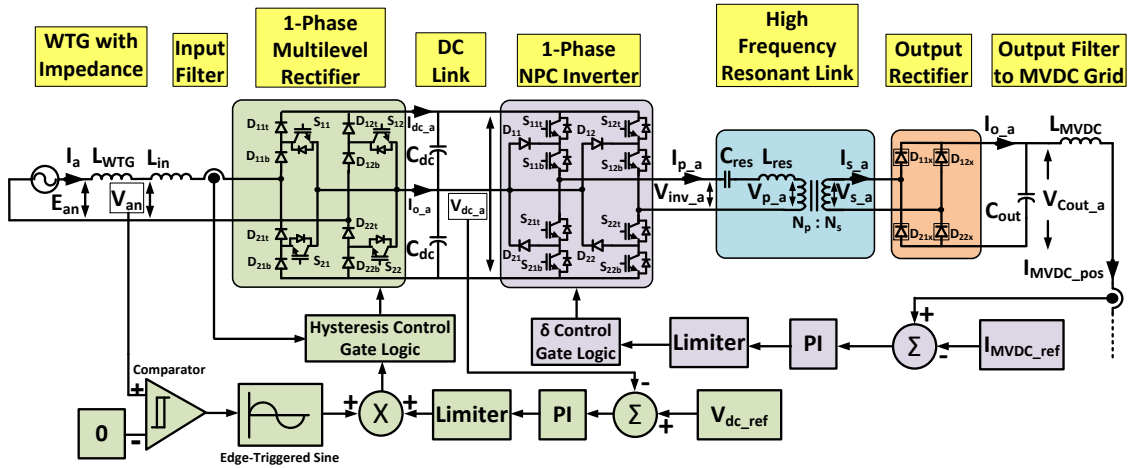
Figure 2-3: End-to-end detail of phase "a" converter module showing output current control scheme and DC link voltage control scheme. The DC link control also implements boost PFC functionality through input current shaping.

Once the MVDC collection grid is energized to the appropriate MVDC voltage individual WTGs may begin injecting power to the MVDC collection grid.

2.2.1 Front-end Multilevel Rectifier

Due to the large generator impedance a boost-type input rectifier is desirable. The proposed single phase multilevel rectifier adapted from [66] satisfies this requirement while also providing input current shaping capability and a DC bus neutral point which allows each semiconductor device to only block half the DC bus voltage. Note that the DC bus voltage must be chosen to be greater than the peak of the internal WTG voltage for boost operation. The DC link capacitor C_{dc} must be designed to suppress the second harmonic of the input current according to (2.1) to achieve a stiff DC bus voltage. A suitable design margin must be added to the results of (2.1), (2.5), and (2.7) to sufficiently suppress the desired frequency.

$$C_{dc} = \frac{1}{2} \left[\frac{1}{\omega_{WTG}} \right] \left[\frac{I_{dc}}{RF_{V_{dc}} V_{dc}} \right] \tag{2.1}$$

The input inductance L_{in} is chosen to be small compared to L_{WTG} and allows for a voltage sensing point separated from the switching at the input terminals of the multilevel rectifier.

2.2.2 HF Inverter and Resonant AC Link

The NPC inverter, dual of the proposed multilevel rectifier, also allows the DC bus voltage to be shared between its component semiconductor devices. This approach uses quasi-square wave switching with free-wheeling zero states provided by closing either both positive or negative pole pairs of IGBTs.

The resonant filter is designed via (2.2), (2.3), and (2.4) to limit the distortion of the primary transformer current and voltage by designing for a maximum allowable third harmonic voltage at the transformer primary winding as described in [67]. The HF transformer turns ratio must be designed to allow the output current controller to boost the DC link voltage to 1/3 the bipolar MVDC voltage with an acceptable duty cycle.

$$Q_{res} = \sqrt{\frac{\frac{v_{inv,3}^2}{v_{p,3}^2} - 1}{2.67^2}} \tag{2.2}$$

$$L_{res} = \left[\frac{Q_{res}}{\omega_{res}} \right] \left[\frac{N_p}{N_s} \right]^2 \left[\frac{V_{MVDC}^2}{9P_{WTG}} \right] - L_{leak} \tag{2.3}$$

$$C_{res} = \frac{1}{Q_{res}\omega_{res} \left[\frac{N_p}{N_s} \right]^2 \left[\frac{V_{MVDC}^2}{9P_{WTG}} \right]} \tag{2.4}$$

The inverter switching frequency was selected by performing a high level trade study of the effects of WTG voltage and switching frequency on the overall volume of the proposed power electronic interface at a given power level of 8 MW and MVDC grid

voltage of ±30 kV. For this analysis the volume of the output diode rectifier was considered fixed as it is determined primarily by the output power and MVDC voltage. The input rectifier and inverter volumes were scaled linearly with the number of devices, taken to be the 5SNA 1500E330305 IGBT [68] and 5SDF 20L4521 diode [69], required for sufficient voltage blocking and current conduction since additional gate drives, snubbers, balancing networks, busbars, etc., are required for each additional device. Total heatsink volume in each converter was scaled linearly with total converter losses to reflect that heatsink surface area must increase linearly with losses to achieve the same thermal resistance [70], and hence the same junction temperature, at the higher level of losses. Since most heatsinks are composed of thin fins, an increase in surface area (i.e. adding fins) yields the same proportion increase in heatsink volume, meaning that it is appropriate to scale heatsink volume linearly with losses. The device losses themselves are considered to scale with the square of the device current (conduction losses) and linearly with switching frequency (switching losses). The transformer volume is taken to scale linearly with the number of turns necessary to achieve the required primary volt-seconds at a given DC link voltage and switching frequency; hence the transformer volume scales linearly with voltage at a given frequency and by the inverse square root of frequency at a given voltage. This is expected since inductance, and hence turns^2, must scale proportionally with volt-seconds, meaning a transformer operating at a 10x higher frequency only requires 1/10 the applied volt-seconds per cycle and hence only 1/√10 as many turns. Once the relative volume of each component was calculated across the range of WTG voltages and inverter frequencies each point was normalized against

the 500 V_{rms} WTG, 1 kHz inverter case, given the volume distribution summarized in Table 2-2 for the overall system at that point [71]. The resulting surface representing normalized converter interface volume over a range of WTG voltages and inverter frequencies is given in Figure 2-4. Note that at while the volume due to power electronics increases at both high voltage and high current the result of a reduction in transformer size at higher frequencies yields an overall lower volume solution across all voltage levels studied. Hence the design proposed in this work operates at 10 kHz as it provides a minimum volume for the given conditions. While implementing a 2-3 MVA, 10 kHz transformer may seem impractical, recent work [72], [73] has shown that 1-2 MVA can be processed by transformers operating from 15-20 kHz. From these promising results we can infer that the technical barriers to constructing the proposed HFT can be overcome.

Table 2-2: Volume distribution of normalizing point in volume trade study.

Volume Component	Contribution to Total System Volume
Input Rectifier	25%
DC Link Capacitor	25%
HF Inverter	25%
HF Transformer	25%
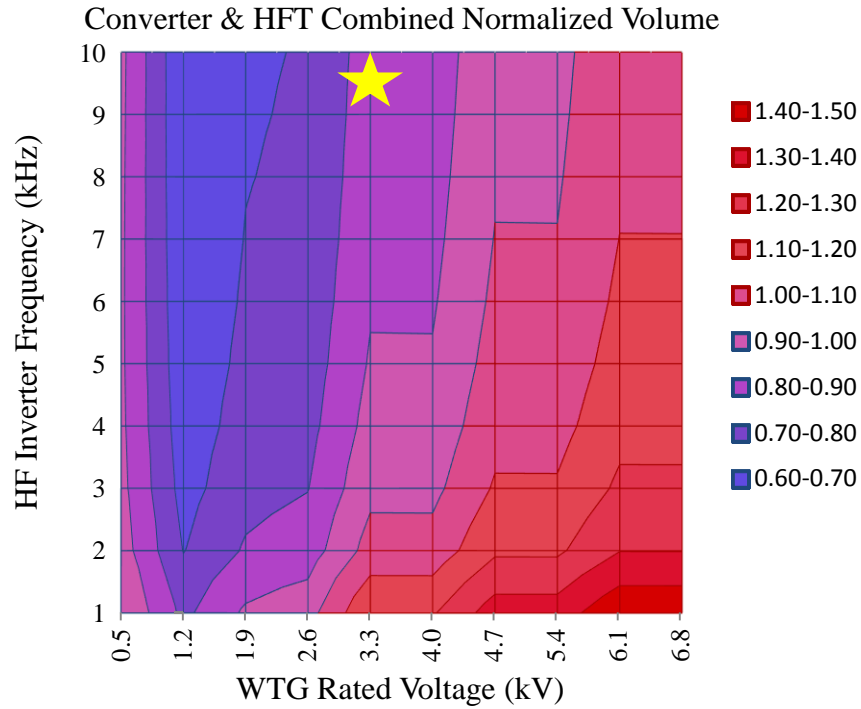
Figure 2-4: Surface describing normalized volume of proposed approach at various WTG voltages and inverter frequencies. The star indicates the chosen operating point studied in this work. The inverse square root effect of transformer volume scaling, as well as discontinuities when devices are added, can be clearly observed.

2.2.3 Output Rectifier to MVDC Grid

Note the need for each diode in the output rectifier to block 1/3 of the MVDC pole-to-pole voltage, which will require multiple series devices as indicated by the box drawn around each individual device in the output rectifiers of Figure 2-2 and Figure 2-3. The output filter is designed according to (2.5) and (2.7) to suppress $2\omega_{res}$ voltage ripple from the output rectifier and maintain constant output current with acceptable ripple. Note that to design C_{out}, the RMS AC component of I_o must first be determined from (2.6). From Figure 2-2 it is clear that I_{MVDC} must flow through each output diode

rectifier in series since it cannot pass through the output capacitors; therefore, each phase module must equally process 1/3 of the total WTG power otherwise I_{MVDC}, and hence output power, will be limited by the module supplying the least current. This creates a strong requirement that the input power from the WTG be balanced. Although unusual, severe unbalance in the WTG could be handled by either adjusting the DC link voltage of the modules such that equal power is drawn from each phase even though unequal current is drawn, or by addition of a power sharing converter similar to [74] between each output rectifier that can source or sink the difference in current between each phase module.

$$L_{MVDC} = \left[\frac{1}{\omega_{res}}\right] \left[\frac{RF_{V_{MVDC}} \frac{V_{MVDC}}{3}}{RF_{I_{MVDC}} I_{MVDC}}\right] \qquad (2.5)$$

$$i_o = \sqrt{\left[\frac{\frac{P_{WTG}}{3}}{\frac{2\sqrt{2}V_{dc}}{\pi}}\right]^2 - I_{MVDC}^2} \qquad (2.6)$$

$$C_{out} = \left[\frac{1}{\omega_{res}}\right] \left[\frac{\sqrt{2}i_o - RF_{I_{MVDC}} I_{MVDC}}{RF_{V_{MVDC}} \frac{V_{MVDC}}{3}}\right] \qquad (2.7)$$

2.2.4 Control Strategies

Two independent closed-loop controllers are implemented with this approach as seen in Figure 2-3. The slower output current controller dictates how much power is drawn through the converter by determining output current while the faster DC link controller maintains V_{dc} as output power varies while also shaping WTG current.

The current controller applies PI control to I_{MVDC} error to generate a phase delay δ which is applied to the NPC inverter switches via gate logic. The two pairs of switches in

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each inverter leg have complementary switching functions and the gate logic applies δ phase delay to the S12/S22 leg relative to the S11/S21 leg. Larger δ decreases the duty cycle of inverter quasi-square wave output with $\delta = \pi$ yielding $V_{inv} = 0V$ and $\delta = 0$ yielding full square wave output.

The DC link controller applies PI control to V_{dc} error to generate a scaling factor which is multiplied by a sinusoid in-phase with the WTG terminal voltage. This sinusoid is triggered each WTG cycle to maintain phase lock with WTG as wind speed varies. Gate logic is then used to generate WTG current hysteresis bands from the scaled sinusoid and apply hysteresis control to the multilevel rectifier for WTG current shaping. To increase WTG current all four rectifier switches are closed; WTG current is allowed to decay through the diodes to the DC bus when all four switches are opened.

2.3 Case Study and Simulation Results

For a practical design example of the proposed approach an 8 MW, 3.3 $kV_{LL,rms}$ DD-PMSG-based WTG is assumed with the characteristics described in Table 2-3. The resulting design is described in Table 2-4. The pole-to-pole MVDC voltage is assumed to fixed by the HVDC station at 60 kV with each pole 30 kV to either side of ground. Acceptable voltage and current ripples are specified as ripple factors, where an RF of 0.1 would correspond to a ripple of +/-10% of the DC value.

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Table 2-3: Case study input parameters

Input Parameter	Value
P_{WTG}	8 MW
V_{WTG}	3.3 $kV_{LL,rms}$
X_{WTG}	0.625 p.u.
f_{WTG}	60 Hz
|Disp. PF_{WTG}|	> 0.9
V_{MVDC}	± 30 kV (60 kV)
L_{leak}	0.05 p.u.
RF_{VMVDC}	0.05
RF_{IMVDC}	0.1
RF_{VDC}	0.05

Once the initial design parameters are fixed the DC link voltage must be selected to be greater than the peak line-to-neutral internal WTG voltage which is higher than the WTG terminal voltage under load and is a function of WTG power output. At rated load and terminal voltage this peak internal voltage was determined to be 3.86 kV, hence the DC link voltage was selected to be 4 kV.

Applying the DC link voltage and P_{WTG} to (2.1) along with a sufficient design margin results in a C_{dc} value of 50 mF, which is large due to the single phase nature of each input rectifier. Use of three-phase multilevel input rectifiers for each converter module would reduce the DC link capacitor size at the expense of adding more semiconductor devices.

The WTG current hysteresis bands are selected to be +/-10% of the reference current to achieve <<10 kHz switching in the multilevel rectifier while maintaining sufficient current shaping capability to achieve acceptable WTG displacement power factor.

Based on the DC link voltage, MVDC voltage, rectifier and inverter switching frequencies, and converter current ratings, the ABB 5SNA 1500E330305 IBGT and ABB 5SDF 20L4521 diode were selected to provide realistic loss parameters for simulation.

The minimum ratio of $N_p:N_s$ is the ratio of $V_{dc}:(V_{MVDC}/3)$, which would produce sufficient output voltage at V_{Cout} given full square wave switching at the inverter and no losses. The transformer turn ratio of $N_p:N_s = 1:8$ was selected to allow a moderate inverter duty cycle while accounting for losses. The transformer leakage inductance was calculated by taking the fundamental of the inverter full square wave, $P_{WTG}/3$, and ω_{res} as per-unit base values for the transformer. This leakage inductance combines with L_{res} to achieve full resonance at ω_{res}.

The resonant filter was designed to limit the third harmonic of V_p to 17.5% of the third harmonic of V_{inv}, meaning most high order harmonics of V_{inv} are rejected by the resonant filter. Applying this criteria to (2.2) results in a Q_{res} of 0.608 which in turn yields $L_{res} = 18.8$ µH and $C_{res} = 11.2$ µF.

Applying (2.6) and the other design parameters to (2.5) and (2.7) with a sufficient design margin yields $L_{MVDC} = 500$ mH and $C_{out} = 500$ µF. The output voltage balancing network was designed to account for less than 0.01% loss in the system. Therefore $R_{balance}$ was chosen to be 1 MΩ to only reduce efficiency by 0.0075%.

Table 2-4: Case study output parameters

Output Parameter	Value
L_{WTG}	2.26 mH
L_{in}	10 μH
V_{dc}	4 kV
C_{dc}	50 mF
f_{res}	10 kHz
C_{res}	11.2 μF
L_{res}	18.8 μH
$N_p:N_s$	1:8
L_{leak}	3.85 μH
C_{out}	500 μF
L_{MVDC}	500 mH
R_{MVDC}	200 mΩ
$R_{balance}$	1 MΩ

The MVDC cable resistance is determined by selecting an appropriate submarine cable rated for 80 kV pole-to-pole voltage such as those used in ABB HVDC Light applications [75]. Such a cable has a conductor area of 95 mm^2, or approximately 4/0 AWG, which has a DC resistance of 276 mΩ/mile [76]. Accounting for tower height, water depth, and turbine spacing, 200 mΩ per conductor to the nearest fixed MVDC source is assumed.

To evaluate the performance of the proposed approach, both steady-state and transient response simulations were carried out in PSIM 9.1.3. To add to the validity of the simulation all inductors were considered to have an ωL:R ratio of 200:1 and resulting inductor resistances were included. In addition capacitor ESRs were accounted for by introducing a series resistor across which 0.1% of each capacitor voltage was dropped. Diode and IGBT on-state voltages of 2.65 V and 3.1 V, respectively, were included based on the data sheets for the devices selected in the preceding design example.

2.3.1 Steady State Operation

Steady-state simulation results at rated WTG power, voltage, and frequency are shown in Figure 2-5 – Figure 2-10. The expected MVDC output current of 133 A is shown to be within the specified ripple of ±10% in Figure 2-5, while the ripple on the MVDC bus due to cable resistance is negligible compared to the MVDC source voltage and within the specified tolerance of ±5% .
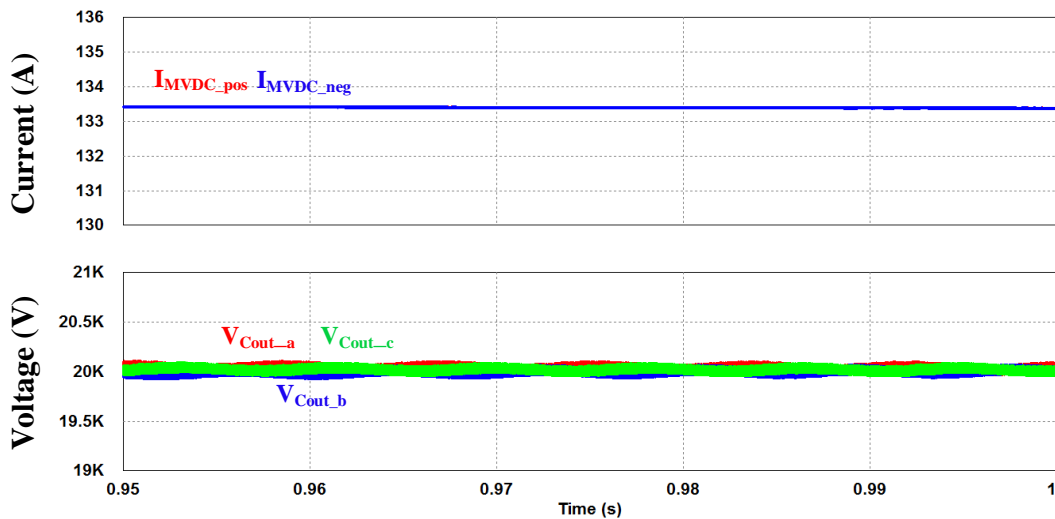
Figure 2-5: Output MVDC current is shown in the top plot while MVDC grid voltage and output capacitor voltages are shown at bottom. Full MVDC pole voltages are not shown as they are simply fixed DC sources at ±30 kV.
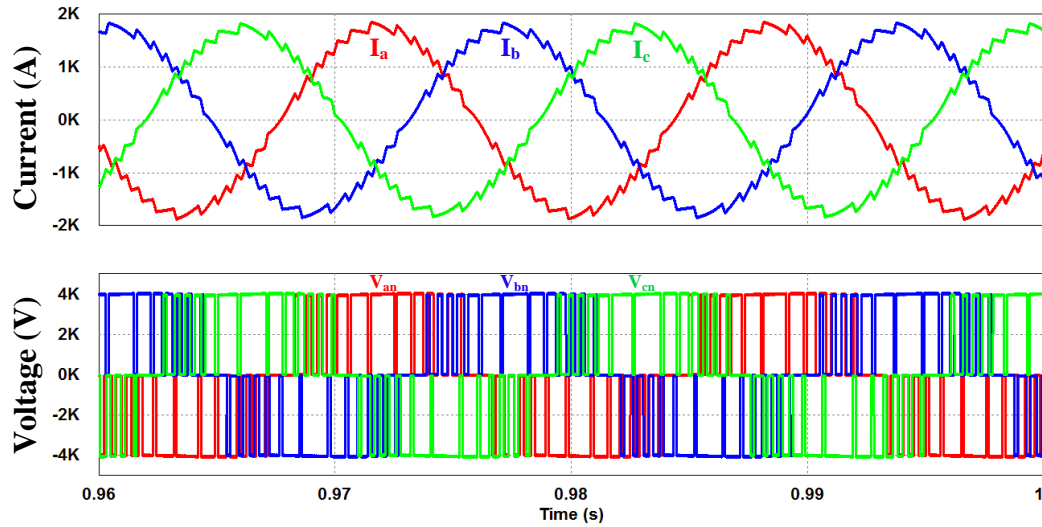
Figure 2-6: WTG currents are shown top while WTG terminal voltages are shown at bottom. Hysteresis control yields and effective input switching frequency of approximately 1.5 kHz.
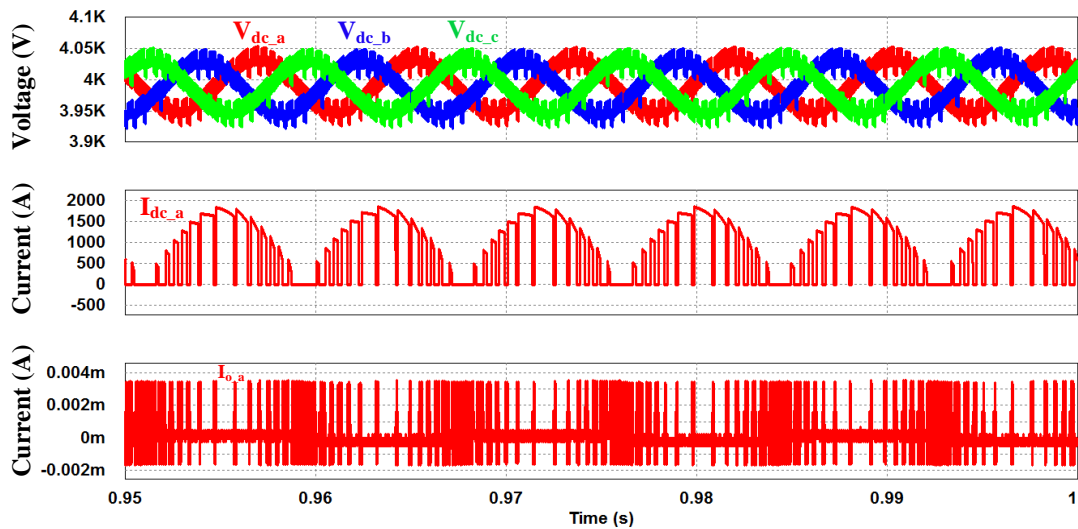
Figure 2-7: WTG phase "a" terminal voltage and current, as well as WTG internal voltage. Input current charging occurs while the corresponding WTG terminal is shorted by the rectifier input, while discharging occurs when the WTG terminal is clamped to the DC link through the outer rectifier diodes. Note V_{an} and I_a are in phase and both lag E_{an}.
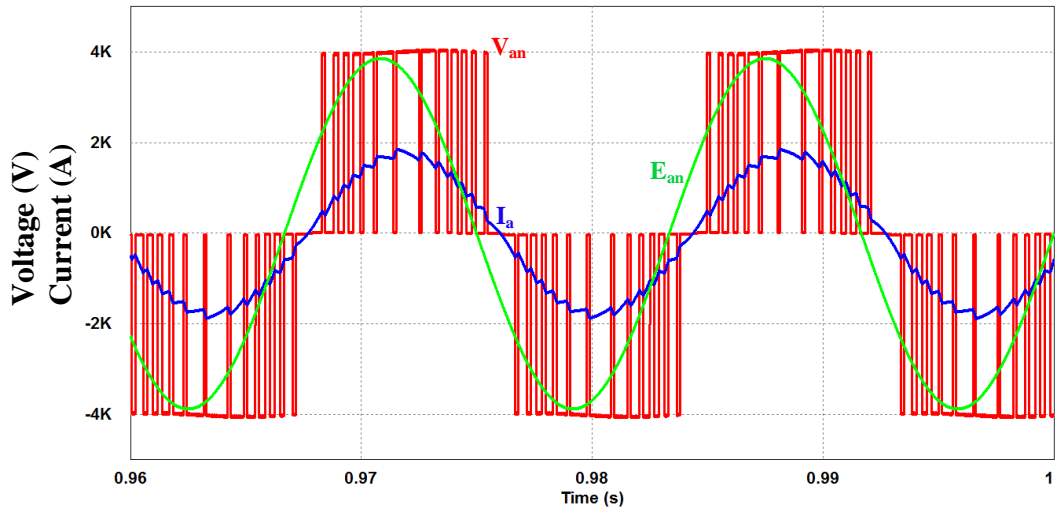
Figure 2-8: Steady-state DC link voltage is shown top while phase "a" DC link current and DC link balancing current are show middle and bottom, respectively. DC link current is composed of decaying portions of WTG current only, which is characteristic of boost converter diode current. The balance current is very small due to the perfectly matched capacitors used in simulation.
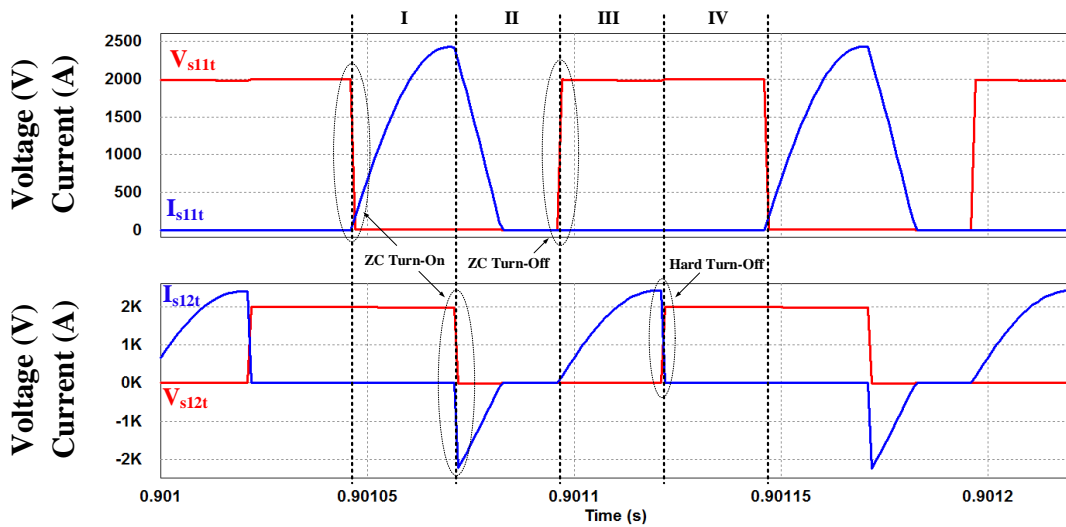
Figure 2-9: Top plot shows inverter output voltage (red), transformer primary voltage (blue), and primary current (green). Transformer current resonates to its peak before zero voltage is applied and current is allowed to freewheel back to zero before next half-cycle. Once I_p freewheels to zero V_p becomes $-V_{Cres}$ as no voltage is present across the resonant inductor when $I_p = 0$. Regions I-IV correspond to states described in Figure 2-11.

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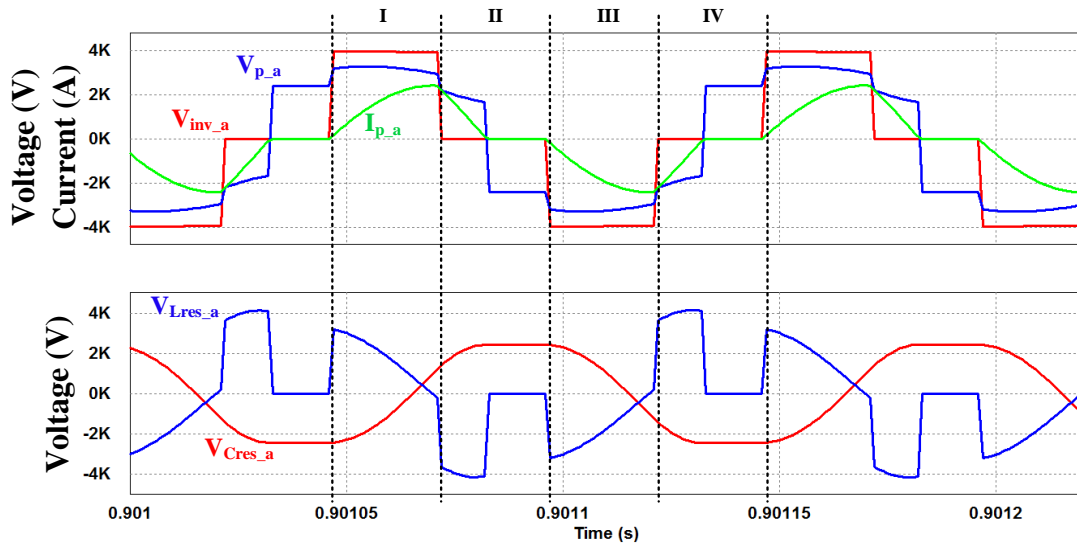
Figure 2-10: Inverter switch voltage and current waveforms for S11t & S12t from Figure 2-3. Both "t" and "b" switches in each pair operate simultaneously. S21 waveforms are S11 waveforms shifted 180°; same relationship holds between S12 & S22. I-IV correspond to Figure. 2-11.
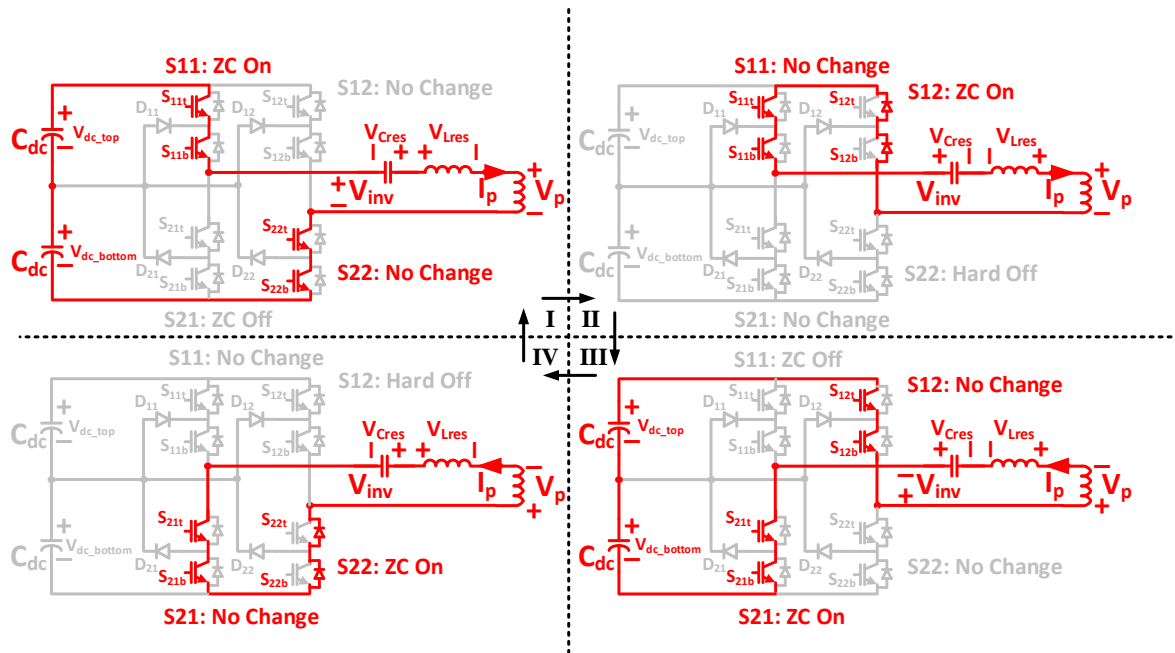
Figure 2-11. Summary of inverter switching states showing conducting paths in red. Inverter continually steps through states I-IV and adjusts the amount of time spent in zero voltage freewheeling states II & IV to control power transfer through transformer. Polarity of V_{Lres} and V_p in states II & IV are shown during current freewheeling before $I_p = 0$.

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The WTG terminal waveforms are shown in Figure 2-6 where balanced terminal voltage and current can be observed. In addition to balanced operation, note that the WTG current is properly shaped by the multilevel rectifier hysteresis control and is in-phase with the terminal voltages. Figure 2-7 shows WTG phase A voltage and current in detail. The multilevel rectifier achieves displacement power factor magnitude of >0.95, measured by estimating the time between input voltage and current fundamental component zero crossings. Also observe that a voltage divider between L_{WTG} and L_{in} forms when rectifier switches are closed resulting in the chopped WTG terminal voltage of Figure 2-7. The multilevel rectifier switching frequency is indirectly controlled by the width of the hysteresis bands and is found to be approximately 1.5 kHz from Figure 2-7, which is far enough from f_{res} to reduce switching interaction between the converters.

The DC link voltages and currents are featured in Figure 2-8. DC link voltages are within specified ripple tolerance of ±5% and the DC link current I_{DC_A} has a typical boost diode characteristic, conducting during switch off time when the input current must decay to the DC bus. Figure 2-9 demonstrates how resonant circuit allows current to build to a maximum when $\pm V_{dc}$ is applied and freewheel back to zero when zero voltage is applied before the next half-cycle, allowing full ZCS in the S11/S21 leg and ZC turn-on in the S12/S22 leg. Figure 2-10 shows ZCS switching in detail with switch voltages and currents. Considering the S11 in the top plot, one observes that the current is initially zero and begins to build only after the switch has closed. Still considering S11, note that the resonant current through the switch decays to zero before the switch turns off. In the case of S12 in the bottom plot, it turns on while current is freewheeling through its anti-

parallel diode, hence it experiences ZC turn-on. However, it experiences hard turn-off near the peak of the resonant current. The circuit switching states for ZCS are summarized in Figure 2-11.

2.3.2 *Transient Response*

Transient simulations were carried out under a step change in wind velocity from 12 m/s to 6 m/s at t = 1.1s given the WTG characteristics of [77]; WTG voltage and frequency reduce to ½ and output power will reduce to ¼ of rated values given a 50% reduction in wind speed.
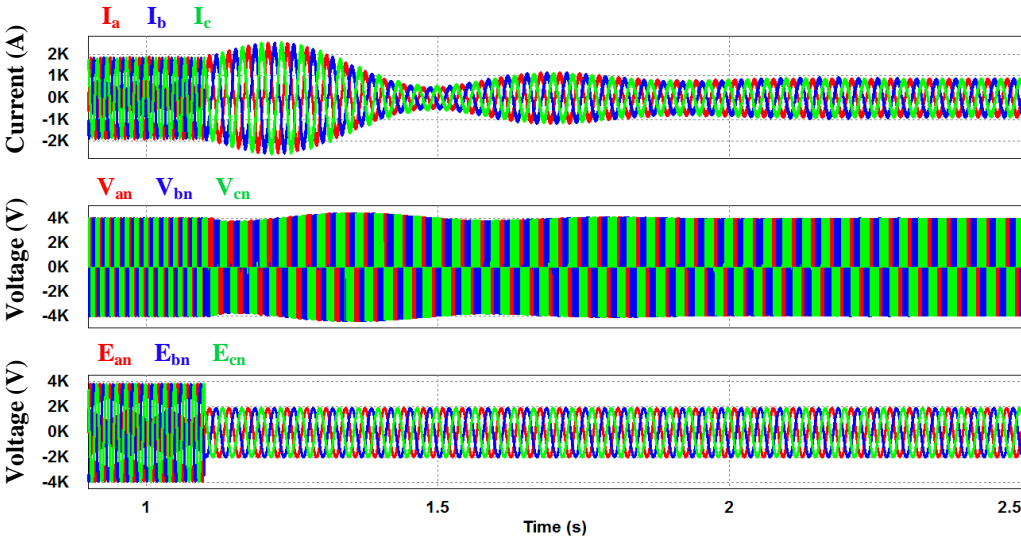
Figure 2-12: WTG current (top), terminal voltage (middle), and internal voltage (bottom) all reduce in frequency post transient, but terminal voltage continues to clamp to 4 kV DC bus.
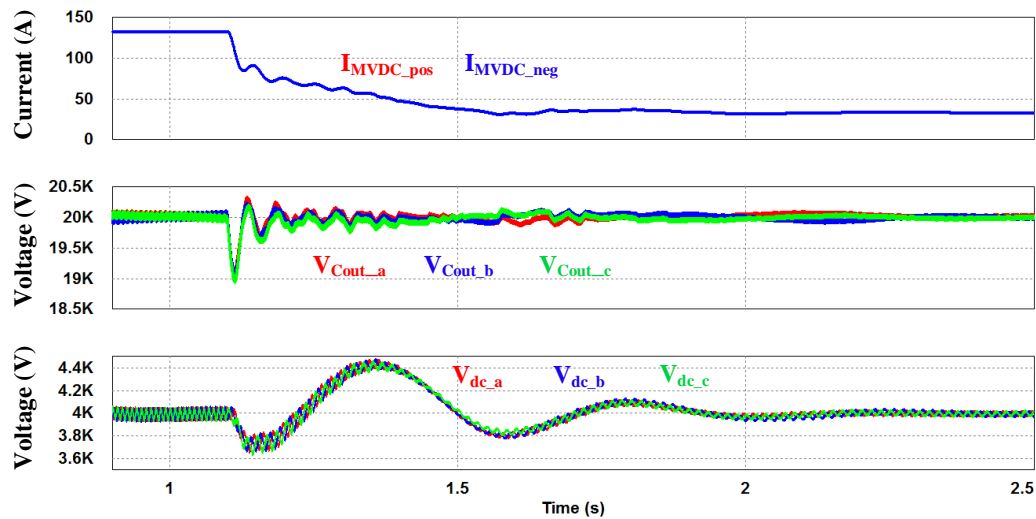
Figure 2-13: The inverter controller stabilizes the output MVDC current within 1 second post-transient. Note output capacitors rapidly rebalance and DC link controller stabilizes balanced DC link voltages within 1 second post-transient.

The WTG current and voltage are shown to both reduce in frequency post-transient, as expected, in Figure 2-12. Note the WTG voltage maintains the same amplitude due to the fixed DC bus even though internal machine voltages have dropped. Figure 2-13 features the output MVDC current which settles to the new output level of 33 A after approximately 1 second. The oscillation of the output current is due to the low damping provided by the active MVDC source at the output. An equivalent resistive load mitigates this oscillation by providing increased damping to the LC output filter. The DC link voltage is shown to settle to within 1 second post-transient in Figure 2-13 while the transformer current reduces to half its original peak value.

2.4 Experimental Results

To validate key simulation results a lab-scale prototype of the input active multilevel rectifier stage was constructed with the parameters described in Table 2-5

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with the remaining sections of the phase module represented by an equivalent resistive load. The prototype uses Infineon BSM 150GB 60DLC IGBTs [78] and International Rectifier IRK D196-16 diodes [79]. While this is a single-phase prototype of a proposed three-phase approach, the per-phase nature of the proposed approach makes investigation of a single-phase prototype suitable as each phase module is quite decoupled from the others. Future investigation of unbalanced operation will require a three-phase prototype.

Table 2-5: Lab-scale prototype hardware parameters

Prototype Parameter	Value
P_{WTG}	700 W
E_{WTG}	165 V_{rms}
L_{WTG}	15.8 mH
V_{DC}	250 V_{dc}
f_{WTG}	60 Hz
$f_{rectifier}$	1.5 kHz
$|Disp. PF_{WTG}|$	>0.95
C_{DC}	1.30 mF
R_{Load}	88.5 Ω
IGBT	BSM 150GB 60DLC
Diode	IRK D196-16

Unlike the identical DC link capacitors of the simulation, the lack of perfectly matching capacitors in the hardware prototype requires a methodology for equally balancing the DC link voltage between the top and bottom capacitors. While in the ideal case all four active switches of the input rectifier are closed and opened simultaneously to boost the input voltage to the DC link, capacitor voltage balancing can be achieved by adding a slight differential in the duty cycles of switch pairs S11/S12 and S21/S22 as

described in Figure 2-14. This provides a simpler capacitor voltage balancing implementation compared to other balancing schemes, such as that proposed in [66].

(a) $V_{dc\_top} > V_{dc\_bottom}$

(b) $V_{dc\_bottom} > V_{dc\_top}$
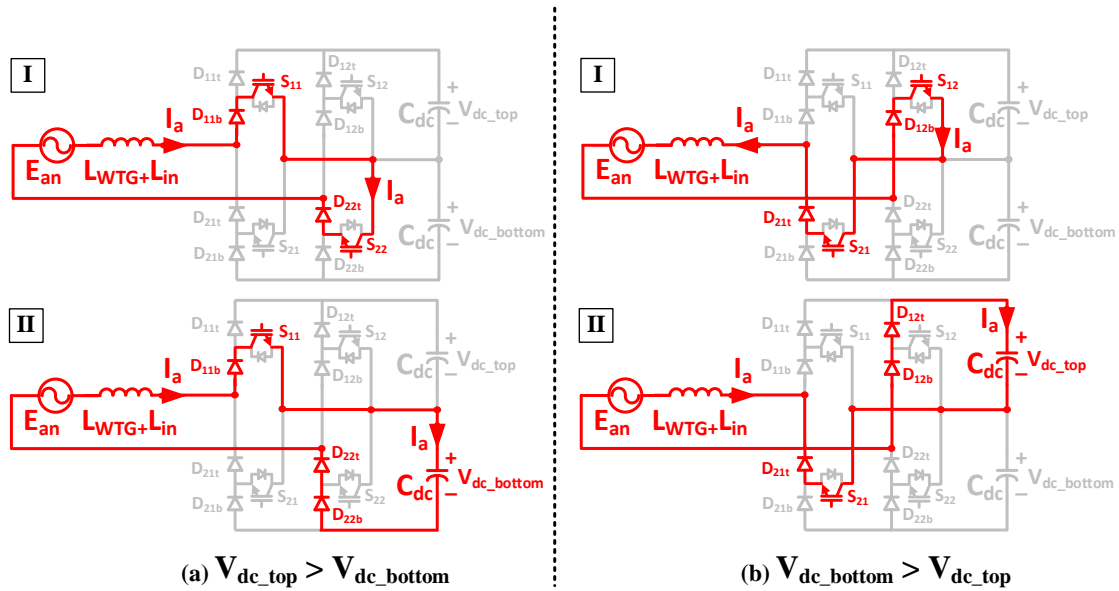
Figure 2-14: Switching methodology for capacitor voltage balancing. When top capacitor has greater voltage as in (a) I_a can be shunted to the bottom capacitor by allowing the duty cycle of S21 & S22 to be slightly lower than S11 & S12. When top capacitor has lower voltage as in (b) I_a can be shunted to the top capacitor by allowing the duty cycle of S21 & S22 to be slightly higher than S11 & S12.

The prototype is energized with 165 V_{rms} from a programmable electronic supply and boosts the input voltage to a 250 V_{dc} bus supplying a 700 W resistive load. The input AC waveforms and the total DC link voltage are shown in Figure 2-15 and closely match simulation results. As with the simulation results, the switching nature of the input voltage and current necessitate that the displacement power factor be measured by estimating the minimum time envelope surrounding the input voltage zero crossing that also contains the zero crossing of the fundamental current component, as demonstrated

in Figure 2-16. In this case the minimum time envelope that contains both input voltage and current fundamental zero crossing is ±0.8 ms, which yields a maximum phase displacement of 17.28° at 60 Hz, indicating a displacement power factor magnitude of at least 0.95. As expected from simulation results in Figure 2-7 the WTG current is shaped to be in phase with the WTG terminal voltage V_{WTG} and both I_{WTG} and V_{WTG} lag behind the internal machine voltage E_{WTG}.
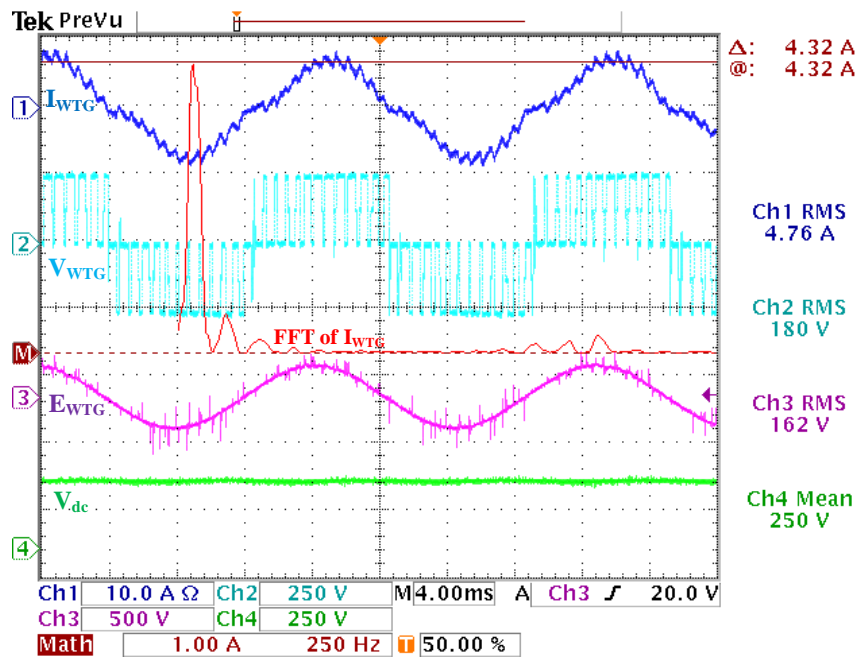
Figure 2-15: Active rectifier stage AC input waveforms and total DC output voltage. WTG internal voltage (Ch.3, purple) is measured as 162 V_{rms} at 60 Hz, while WTG terminal voltage (Ch2, light blue) has a higher RMS value due to switching harmonics as expected from simulation results in Figure 2-7. WTG current (Ch.1, dark blue) shows low phase displacement from WTG terminal voltage and the expected switching action from Figure 2-7. Output DC link voltage (Ch.4, green) is steady at 250 V_{dc}. Note the fundamental component of the input current (Ch. Math, red) is 4.32 A_{rms} and accounts for most of the 4.76 A_{rms} of input current.

The relevant output DC waveforms of the prototype active rectifier stage are illustrated in Figure 2-17 and match simulated results. DC link capacitor voltage

balancing is demonstrated using the methodology described in Figure 2-14. As expected from simulations, the DC link current I_{dc} has a high peak-to-average ratio as the outer rectifier diodes only conduct when active switches are open and inductor current is decaying to the DC bus. In this case the peak I_{dc} is approximately 8 A, while the average value is 2.78 A, which corresponds to an output power of approximately 700 W at the DC link voltage of 250 V_{dc}.
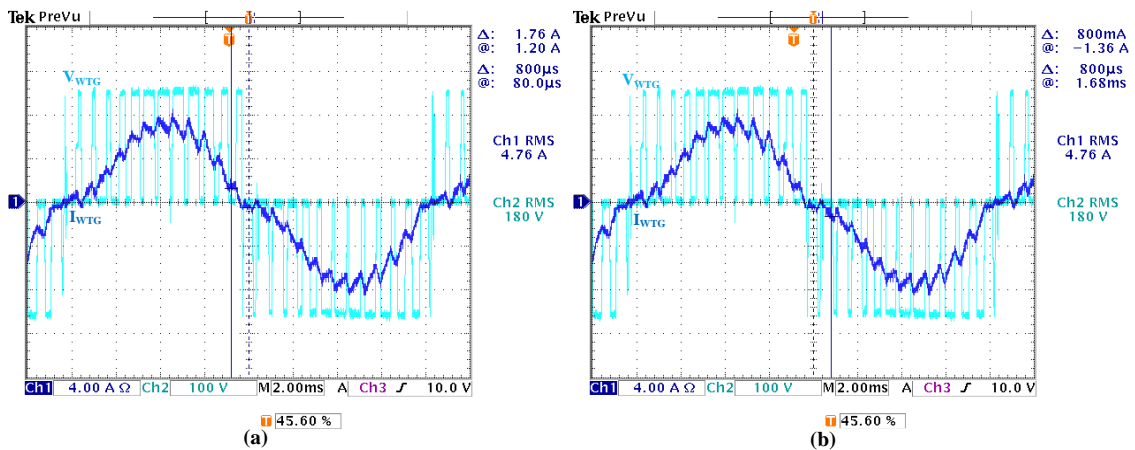
Figure 2-16. From the WTG voltage zero crossing at 0.88 ms, indicated by the blue dashed vertical cursor centered in (a) and (b), the current zero crossing is estimated to be within -0.8 ms, represented by the solid blue vertical cursor in (a), and +0.8 ms, represented by the solid blue vertical cursor in (b).

Note that in Figure 2-17 the DC link balancing current I_o has a small negative average value. This indicates that there is a natural imbalance between the top and bottom capacitors in the DC link. The average value of Io being negative further indicates that it is more often trying to increase the voltage of the top capacitor than the bottom capacitor by the method described in Figure 2-14. This would seem to indicate that the top capacitor has more capacitance than the bottom capacitor, and hence settles

at a lower voltage given the same charge according to Q = CV. Yet the top capacitor was measured to be 2.54 mF while the bottom capacitor was measured to be 2.68 mF, meaning the bottom capacitor would have a lower voltage in steady state and we would expect I_o to have a positive average value. However, when connected to a load other dynamics may effect the capacitor voltage balance, such as the smaller top capacitor experiencing a faster RC time constant and supplying its stored charge more rapidly to the load, requiring more frequent re-charging. Moreover, once the controller has instantaneously balanced capacitor voltages the smaller top capacitor must be holding
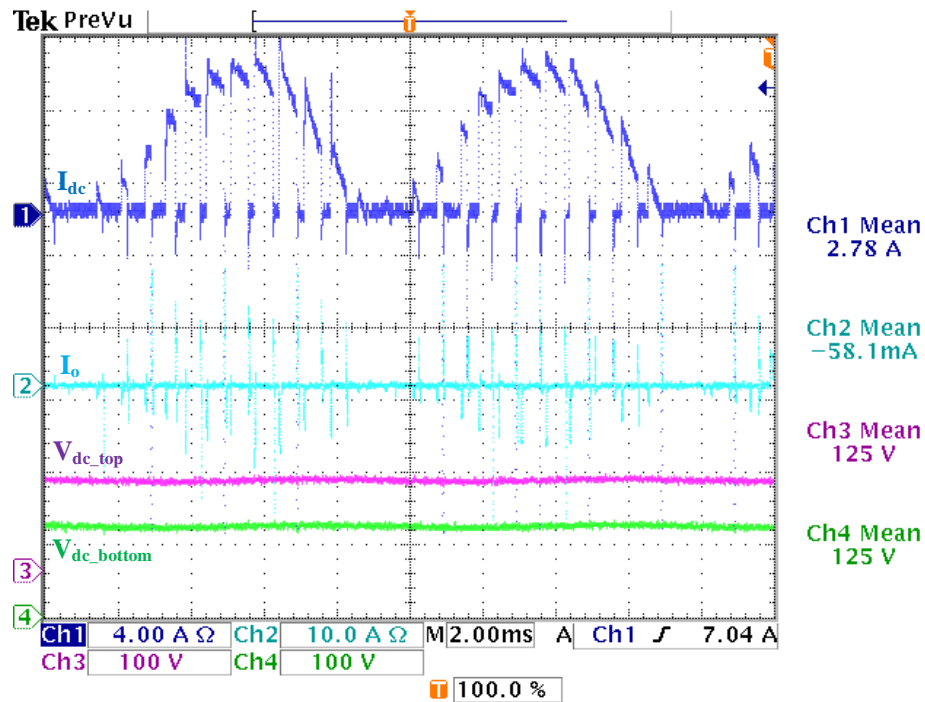
Figure 2-17: Active rectifier stage output DC waveforms. DC link top capacitor voltage (Ch.3, purple) and bottom capacitor voltage (Ch4, green) are balanced at 125 V_{dc} each, and balancing current I_o (Ch.2, light blue) shows only a small DC value and clamping to I_{dc} during capacitor balancing action as described in Figure 5-14. DC link current I_{dc} (Ch.1, dark blue) shows typical boost diode current characteristic as expected from Figure 2-8.

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less charge, and so it will be depleted more rapidly as it supplies the load.. These capacitor voltage balancing dynamics may be responsible for the negative average value of I_o, but further exploration of capacitor voltage balancing dynamics requires its own dedicated investigation beyond this paper.

2.5 Conclusions

A new power electronic interface for the integration of future offshore wind parks with MVDC collection grids has been introduced and analyzed. As wind parks are sited further out the sea, such next-generation interfaces are necessary for the continued development of offshore wind resources. A practical design case study provides guidance for future development of the proposed interface.

The results of detailed simulation of the proposed approach case study demonstrate operation from full rated power down to 25% rated power via a step change in WTG input power. Simulation results also demonstrate >0.95 displacement power factor magnitude, near sinusoidal WTG current, continuous output current, and stiff DC link voltage.

Experimental results from a lab-scale prototype are introduced, showing high fidelity to corresponding simulation results associated with the front-end active rectifier stage. The 250 V_{dc}, 700 W prototype achieves displacement power factor magnitude of >0.95 with balanced DC link capacitor voltages and an effective input switching frequency of 1.5 kHz.

3. AN IMPROVED OFFSHORE WIND TURBINE TO MVDC GRID INTERFACE USING HIGH FREQUENCY RESONANT ISOLATION AND INPUT POWER FACTOR CONTROL[*]

This work introduces a new approach using high frequency (HF) isolation transformers with a series resonant power transfer mechanism for interfacing next-generation offshore wind turbine generators (WTGs) to medium voltage DC (MVDC) collection grids, a necessity for the continued development of offshore wind resources as farms are sited further out to sea. Analysis of the proposed approach is provided, as well as a practical design example. Detailed simulation results demonstrate converter operation from full rated power down to 25% rated power. The WTG displacement power factor is found to be 0.96 lagging. The three-phase multilevel input rectifier allows 5 times reduction in DC link capacitance over the previous per-phase approach. Near-sinusoidal WTG and transformer currents, continuous output currents, stiff DC link voltages and zero current switching (ZCS) in the HF inverter are all observed in simulation. Experimental results from 50 W prototype single-phase multilevel input rectifier stage corroborate corresponding to simulation results, with measured DPF of 0.92 lagging.

3.1 Introduction

In this time of rapidly increasing standards of living, those in the developing world are gaining greater levels of economic power; as a result, new energy resources must be developed to maintain the accelerating demand for transportation, entertainment, communication, computing, and other such energy-centric industries[2]. Simultaneously, constraints owing to anticipated climate change and volatile petroleum markets have led many nations to develop their offshore wind resources due to this resource's attractiveness from both an environmental and economic perspective[3]-[5].

Wind energy resources are now being sited further out to sea than ever before[13], with Germany's Global Tech 1 farm, among the leaders in distance-to-shore, constructed nearly 100 km from land[57]. Additionally, state-of-the-art WTGs rated at 6 MW at 3.3 kV are available, necessitating nearly 1 km of inter-turbine spacing, as is the situation at Germany's Alpha Ventus farm[17]. In the near future it is likely that 8 and 10 MW WTGs will be entering service[15], and inter-turbine spacing beyond 1 km will likely be necessary for safe and effective operation.

These large distances to shore have made high voltage direct current (HVDC) necessary in transporting offshore wind energy to customers as it eliminates reactive power requirements and reduces cabling cost and complexity[16].

The growth of inter-turbine spacing, combined with the presence of HVDC links to shore makes the use of an MVDC collection grid more suited to aggregating WTG energy within the farm than the traditional MVAC architecture. Such an MVDC collection grid architecture is illustrated in Figure 3-1[61].
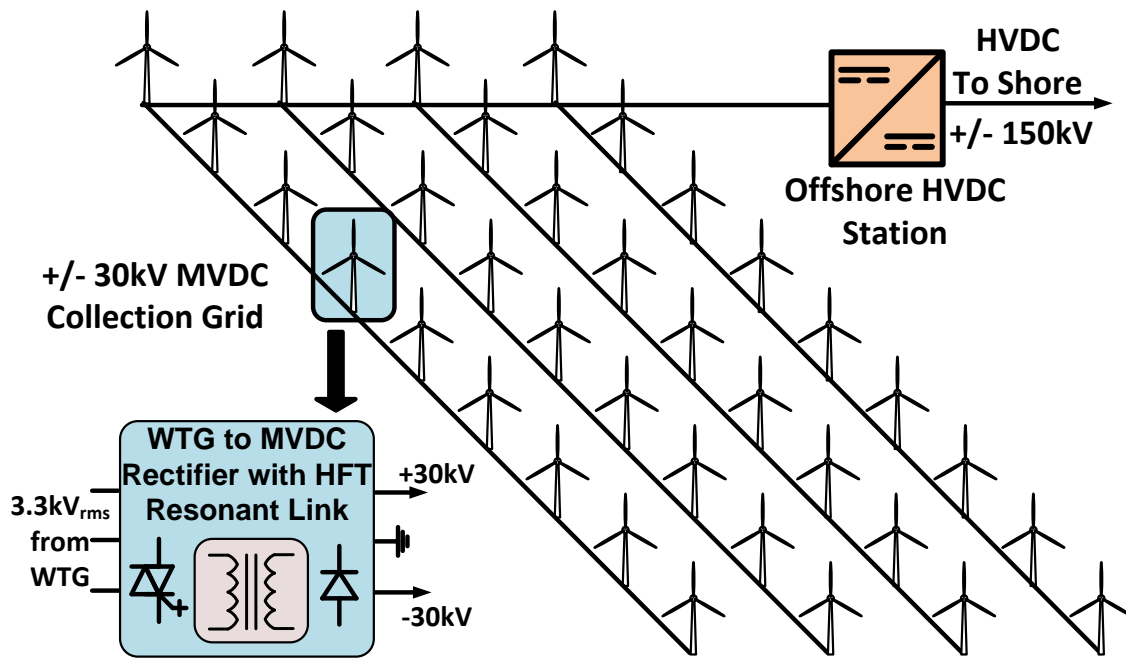
Figure 3-1: WTG interface to offshore wind farm with +/-30 kV MVDC collection grid architecture and HVDC link to shore, © IEEE 2014.

Evaluated against the traditional MVAC architecture [26], this MVDC option provides the following advantages:

- Elimination of line frequency transformers.

- Simplification of collection grid undersea cabling.

- Elimination of inter-turbine reactive power issues.

- Simplification of HVDC converter station interface.

This work focuses on an improved approach for interfacing individual WTGs to an MVDC collection grid. A number of previous proposed approaches for such an interface exist. Medium frequency generators have been proposed as the foundation of the interface to an MVDC grid via a simple diode rectifier in [25]; however, this non-

traditional generator may be too voluminous for a WTG due to requiring a large number of poles or gearbox to attain medium frequency operation. In [27] and [80] a series of converter stages are proposed between the WTG and the offshore HVDC station, potentially requiring additional platforms. A modular multilevel converter architecture is proposed in [28], requiring a four-armature machine to achieve substantial DC output voltage; galvanic isolation is not provided in this approach. A bridgeless PFC input approach is proposed in [29], along with a intricate transformer connection to provide isolation.

This work proposes a "per-pole" approach, in that each end-to-end converter module output interfaces to a single MVDC pole, hence there is one converter module per MVDC pole, as opposed to the "per-phase" approach in [10] where each end-to-end module input interfaces with a single WTG phase leading to one converter module per phase. This work utilizes high frequency resonant isolation while providing output current control to the MVDC bus and input power factor correction (PFC) at the WTG. Compared to [25],[27]-[29],[61],[80] the proposed approach has the following advantages:

- Uses conventional direct-drive synchronous generator.
- Compact high frequency transformer provides galvanic isolation.
- Resonant link allows ZCS in HF inverter.
- Input reactive power control capability for PFC.
- Large generator inductance becomes an advantage for multilevel rectifier boost PFC mode.

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- Decreased DC link capacitance due to 3-phase multilevel input rectifier.

- Single converter module per pole eliminates requirement to balance MVDC voltage between converters.

- Reduced common mode voltage stress and circulating currents compared to per-phase approach.

3.2 Proposed Approach and Analysis

A high-level illustration of the proposed approach is shown in Figure 3-2. A detailed view of a single pole module including the two control schemes is shown in Figure 3-3.

For the proposed approach a direct-drive permanent magnet synchronous generator (DD-PMSG) is assumed. Such a machine has a typical synchronous reactance of 0.6 per-unit, which is inversely proportional to machine volume [64], [65]. The MVDC voltage is considered fixed by the HVDC station, requiring current control at the converter output. The MVDC cable resistance is considered due to anticipated future inter-turbine spacing >1 km. The active switching device for the proposed approach is the integrated gate-commutated thyristor (IGCT) owing to the required voltage and power rating of the converter modules. State-of-the-art IGCTs are hard-switching capable up to several kHz, a limit that is due primarily to heat sinking capability. The resonant characteristic of the proposed approach allows for ZCS, which reduces heat dissipated in the IGCTs thereby allowing higher switching frequencies for the HF inverter.
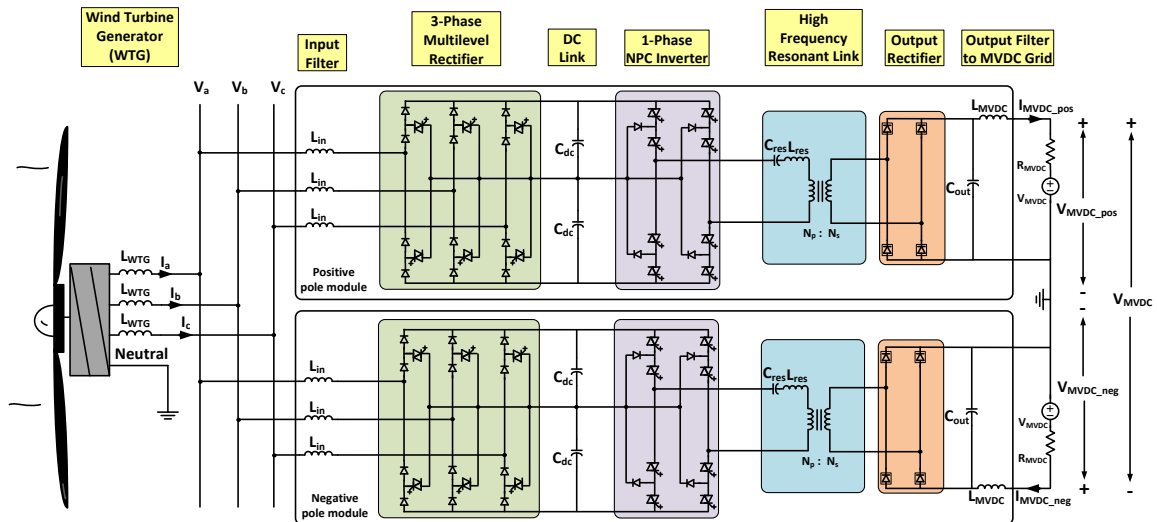
Figure 3-2. The proposed per-pole converter interface between WTG and MVDC collection grid using multilevel rectifier, NPC inverter and HF resonant AC link
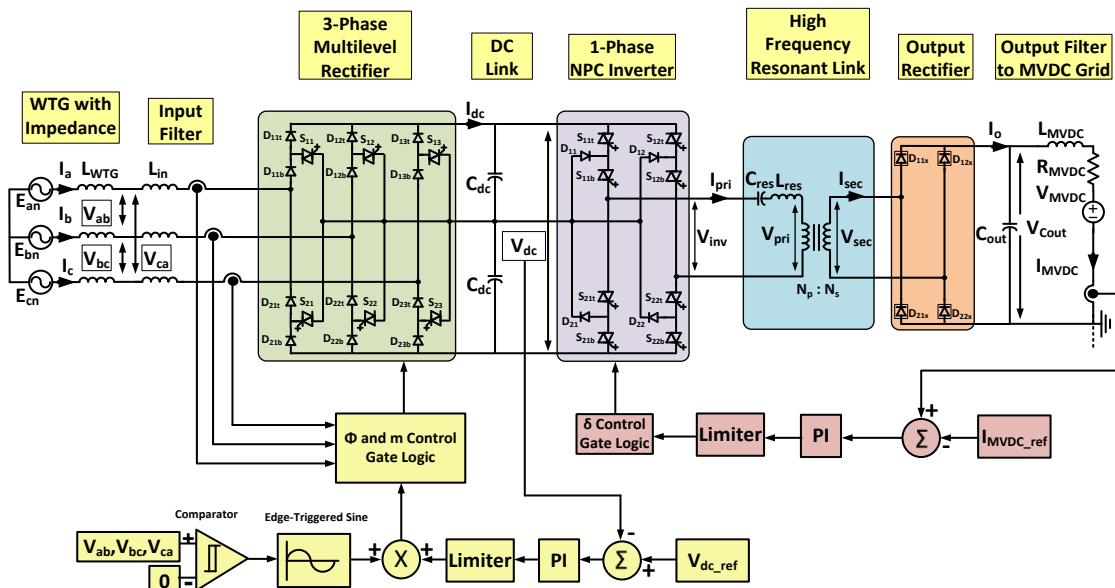
Figure 3-3. End-to-end detail of positive pole converter module showing output current control scheme and DC link voltage control scheme. The DC link control also implements boost PFC functionality through input reactive power control.

3.2.1 Multilevel Rectifier in Boost PFC Mode

The large generator impedance makes a boost-type input rectifier desirable. The input three-phase multilevel rectifier from [66] satisfies this requirement while also providing reactive power control capability and a DC bus neutral point which allows each semiconductor device to only block half the DC bus voltage. The DC bus voltage must be chosen to be greater than the peak of the internal WTG voltage for boost operation The DC link capacitor C_{dc} must be designed to suppress the sixth harmonic of the input current according to (3.1) to achieve a stiff DC bus voltage. An appropriate design margin must be applied to the results of (3.1), (3.6), and (3.7) to sufficiently suppress the desired frequencies.

$$C_{dc} = \frac{I_{dc}}{6\omega_{WTG}RF_{Vdc}V_{dc}} \tag{3.1}$$

The input inductance L_{in} is added to allow for a voltage sensing point separated from the switching at the multilevel rectifier inputs and is chosen to be small compared to L_{WTG}.

3.2.2 NPC Inverter

The NPC inverter, component-wise the dual of the multilevel rectifier, also allows the DC bus voltage to be shared between its component semiconductor devices. Quasi-square wave switching with free-wheeling zero states provided by closing either both positive or negative pole pairs of IGCTs is used in this approach. Owing to the resonant characteristic of the AC link, the IGCT switching instants occur near current zero crossings, reducing IGCT losses and heating, allowing for higher frequency operation.

3.2.3 Resonant AC Link

The resonant filter is designed via (3.2), (3.3), and (3.4) to control the distortion of the primary transformer current and voltage by designing for a maximum allowable third harmonic voltage at the transformer primary winding, a design approach described in [67]. A suitable turns ratio must be selected for the HF transformer to allow the output current controller to boost the DC link voltage to 1/2 the bipolar MVDC voltage with an acceptable duty cycle.

$$Q_{res} = \sqrt{\frac{\frac{V_{inv,3}^2}{V_{p,3}^2}-1}{2.67^2}} \qquad (3.2)$$

$$L_{res} = \left[\frac{Q_{res}}{\omega_{res}}\right]\left[\frac{N_p}{N_s}\right]^2\left[\frac{V_{MVDC}^2}{4P_{WTG}}\right] - L_{leak} \qquad (3.3)$$

$$C_{res} = \frac{1}{Q_{res}\omega_{res}\left[\frac{N_p}{N_s}\right]^2\left[\frac{V_{MVDC}^2}{4P_{WTG}}\right]} \qquad (3.4)$$

3.2.4 Output Rectifier and Filter

Each diode in the output rectifier must block 1/2 of the MVDC pole-to-pole voltage, which requires multiple series devices as indicated by the box drawn around each individual device in the output rectifiers of Figure 3-2 and Figure 3-3. The single phase nature of the output rectifier requires the output filter be designed according to (3.6) and (3.7) to suppress $2\omega_{res}$ voltage ripple from the output rectifier and maintain constant output current with acceptable ripple. To design C_{out}, the rms AC component of I_O must first be determined from (3.5). Unlike the per-phase approach of [61] a passive

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balancing network is not required to balance MVDC pole voltage between the outputs of multiple converter modules.

$$i_o = \sqrt{\left[\frac{\frac{P_{WTG}}{2}}{\frac{2\sqrt{2}V_{dc}}{\pi}}\right]^2 - I_{MVDC}^2} \qquad (3.5)$$

$$L_{MVDC} = \frac{RF_{V_{MVDC}}\frac{V_{MVDC}}{2}}{\omega_{res}RF_{I_{MVDC}}I_{MVDC}} \qquad (3.6)$$

$$C_{out} = \frac{\sqrt{2}i_o - RF_{I_{MVDC}}I_{MVDC}}{\omega_{res}RF_{V_{MVDC}}\frac{V_{MVDC}}{2}} \qquad (3.7)$$

3.2.5 Control Strategy

Figure 3-3 illustrates the two independent closed-loop controllers used in this approach. The output current controller is the slower of the two loops and dictates how much power is drawn through the converter by determining output current while the DC link controller maintains V_{dc} as output power varies while also controlling real and reactive power drawn from the WTG via the magnitude and phase on the input voltage fundamental, as described by (3.8) and (3.9).

$$P_{1\theta} = \frac{|E_{WTG,\theta N}||V_{rect,\theta N}|\sin(\varphi)}{X_{WTG}} \qquad (3.8)$$

$$Q_{1\theta} = \frac{|E_{WTG,\theta N}|^2 - |E_{WTG,\theta N}||V_{rect,\theta N}|\cos(\varphi)}{X_{WTG}} \qquad (3.9)$$

The current controller (red) applies PI control to I_{MVDC} error to generate a phase delay δ which is applied to the NPC inverter switches via gate logic. The two pairs of switches in each inverter leg have complementary switching functions and the gate logic applies δ phase delay to the S_{12}/S_{22} leg relative to the S_{11}/S_{21} leg. Larger δ decreases the

duty cycle of inverter quasi-square wave output with $\delta = \pi$ yielding $V_{inv} = 0V$ and $\delta = 0$ yielding full square wave output.

The DC link controller (yellow) applies PI control to V_{dc} error to generate a phase delay ϕ between the WTG voltage and the fundamental of the input rectifier voltage which modulates the real power drawn from the WTG according to (3.8). The input current phase with respect to the fundamental of the input rectifier voltage is also measured and error between this measurement and the reference power factor is applied to the input voltage modulation depth to adjust the magnitude of the input fundamental voltage and control input reactive power via (3.9).

3.3 Design Example

A practical design example of the proposed approach is based on a 6 MW, 3.3 $kV_{LL,rms}$ DD-PMSG WTG with the characteristics described in Table 3-1. The pole-to-pole MVDC voltage is assumed fixed by the HVDC station at 60 kV with each pole 30 kV to either side of ground. Voltage and current ripples riding on DC values are specified as ripple factors, where an RF of 0.1 would correspond to a ripple of +/-10% of the DC value.

Table 3-1: Design Input Parameters

Input Parameter	Value
P_{WTG}	6 MW
V_{WTG}	3.3 $kV_{LL,rms}$
X_{WTG}	0.6 p.u.
f_{WTG}	60 Hz
Displacement PF_{WTG}	> 0.9
V_{MVDC}	± 30 kV (60
L_{leak}	0.05 p.u.
RF_{VMVDC}	0.05
RF_{IMVDC}	0.1
RF_{VDC}	0.05

Table 3-2: Design Output Parameters

Output Parameter	Value
L_{WTG}	2.88 mH
L_{in}	10 µH
V_{dc}	6 kV
C_{dc}	10 mF
f_{res}	10 kHz
C_{res}	1.05 µF
L_{res}	233 µH
$N_p:N_s$	1:7
L_{leak}	7.7 µH
C_{out}	500 µF
L_{MVDC}	500 mH
R_{MVDC}	200 mΩ

After fixing the initial design parameters the DC link voltage must be selected to be greater than the peak line-to-line internal WTG voltage which is higher than the WTG terminal voltage under load and is a function of WTG power output. At rated load and terminal voltage this peak internal voltage was determined to be approximately 5400 V, hence the DC link voltage was selected to be 6 kV.

Applying the DC link voltage, WTG power, and sufficient design margin to (3.1) results in a C_{dc} value of 10 mF, which is 5 times smaller than C_{dc} in the per-phase approach [61] due to use of three-phase multilevel input rectifiers which allow the DC link to be designed to filter the sixth harmonic of input current instead of the second.

The operating frequency of the input rectifiers was chosen as 1.5 kHz to be sufficiently distant from the HF inverter frequency while maintaining sufficient control capability to achieve acceptable WTG displacement power factor and respond promptly to changes in WTG input power.

Based on the MVDC voltage, DC link voltage, inverter and rectifier switching frequencies, and converter current ratings, the ABB 5SHY 42L6500 IGCT [81] and Powerex RBK86525XXOO diode [82] were selected to provide conduction loss parameters for simulation.

The minimum ratio of $N_p:N_s$ is the ratio of $V_{dc}:(V_{MVDC}/2)$, which would produce required output voltage at V_{Cout} given full square wave switching at the inverter and no losses. The transformer turns ratio of $N_p:N_s = 1:7$ was selected to allow a reasonable inverter duty cycle while accounting for losses. The transformer leakage inductance was calculated by taking the fundamental of the inverter full square wave, $P_{WTG}/2$, and ω_{res} as

per-unit base values for the transformer. Note that the leakage inductance combines with L_{res} to achieve full resonance at ω_{res}.

The resonant filter was designed to limit the third harmonic of the transformer primary voltage V_p to 5% of the third harmonic of V_{inv}. This results in nearly all higher order harmonics of V_{inv} being rejected by the resonant filter. Applying this design criteria to (3.2) results in a Q_{res} of 2.47 which in turn yields $L_{res} = 233$ μH and $C_{res} = 1.05$ μF.

Applying (3.5) and the other design parameters to (3.6) and (3.7) with an appropriate design margin results in $L_{MVDC} = 500$ mH and $C_{out} = 500$ μF.

The MVDC cable resistance is determined by selecting a representative submarine cable rated for 80 kV pole-to-pole voltage such as those used in ABB HVDC Light applications [75]. The required cable has a conductor area of 95 mm2, or approximately 4/0 AWG, which has a DC resistance of 276 mΩ/mile [76]. Accounting for water depth, tower height, and turbine spacing, 200 mΩ per conductor to the nearest fixed MVDC source is assumed.

3.4 Simulation Results

For the purpose of evaluating the proposed approach, both steady-state and transient simulations were carried out. To enhance the validity of the simulation all inductors are considered to have an ωL:R ratio of 200:1; resulting inductor resistances are included in the simulation. Capacitor ESRs are also accounted for by introducing a series resistor across which 0.1% of each capacitor voltage is dropped. Diode and IGCT

on-state voltages of 1.5 V and 3 V, respectively, were included based on the devices selected in the previous design example.

Steady-state simulation results at rated WTG voltage, power, and frequency are shown in Figure 3-4 – Figure 3-8. The MVDC output current shown in Figure 3-4 and has a DC value of 100 A and is within the specified ripple of +/- 10%. Also note in Figure 3-4 the ripple on the MVDC bus due to cable resistance is negligible compared to the MVDC source voltage.

The WTG terminal waveforms are shown in Figure 3-5 where balanced WTG current can be observed, as well as the clamping of line-to-neutral WTG terminal voltages to half the DC link voltage since the WTG neutral is grounded. Beyond balanced operation, note that the WTG current is pulled in phase with the WTG fundamental terminal voltage by the multilevel rectifier control and is sinusoidal. Phase A terminal voltage and currents are shown in more detail in Figure 3-6 where the displacement power factor achieved by the multilevel rectifier achieves is 0.96 lagging. Note a voltage divider between L_{WTG} and L_{in} forms when rectifier switches are closed resulting in chopped WTG terminal voltage.

Figure 3-7 confirms stiff DC link voltage. The inverter outputs can also be seen to be interleaved in Figure 3-7; while not necessary, this arrangement reduces output current ripple.
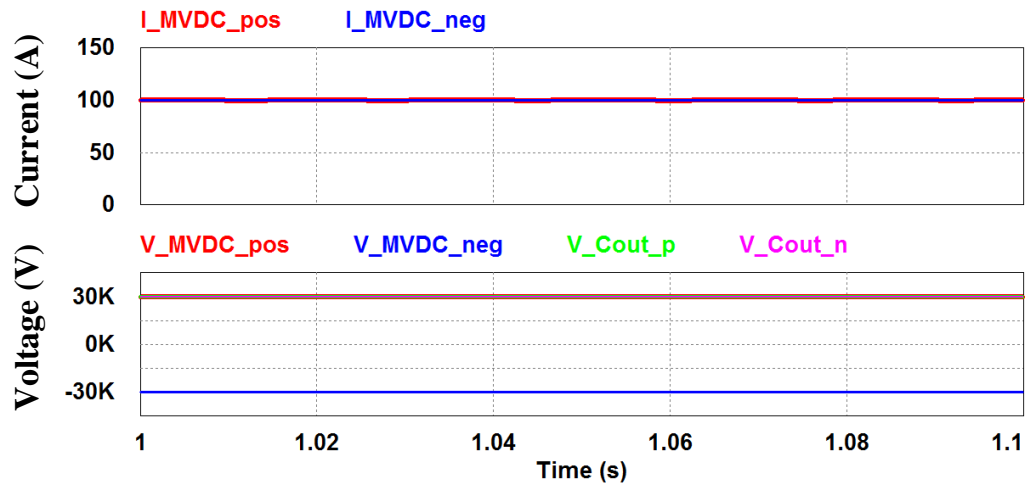
Figure 3-4: Simulated output current to MVDC grid and MVDC grid voltage in steady state.

Figure 3-8 confirms the transformer current is nearly sinusoidal and reveals the resonant frequency sinusoid riding on the inverter switching voltage, a common issue with resonant inverters. The transformer primary voltage of Figure 3-7 clamps to a voltage slightly less than that of the DC link due to the impedance of the resonant elements.
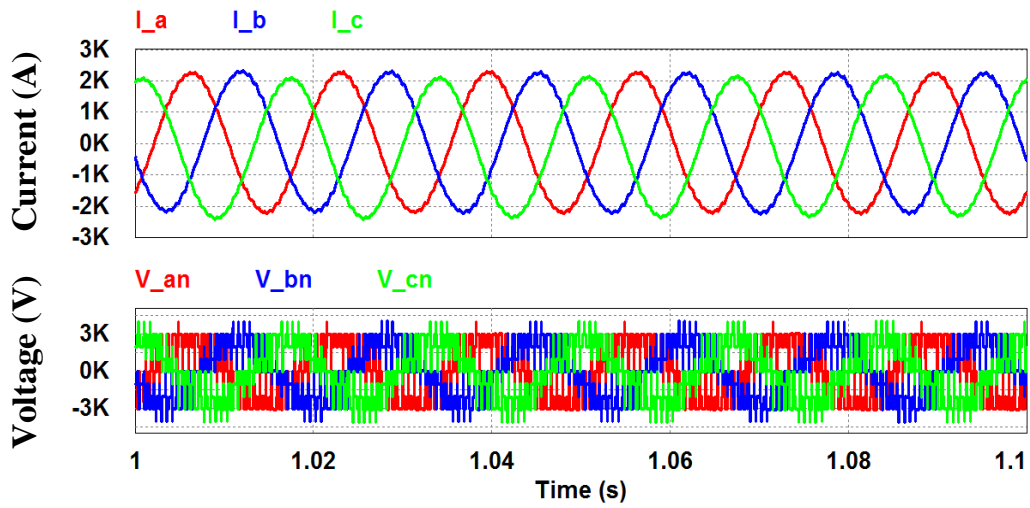
Figure 3-5: WTG terminal voltages and currents. Note that the DC link voltages must be equal since both input rectifiers may simultaneously connect their DC links to the same phase.
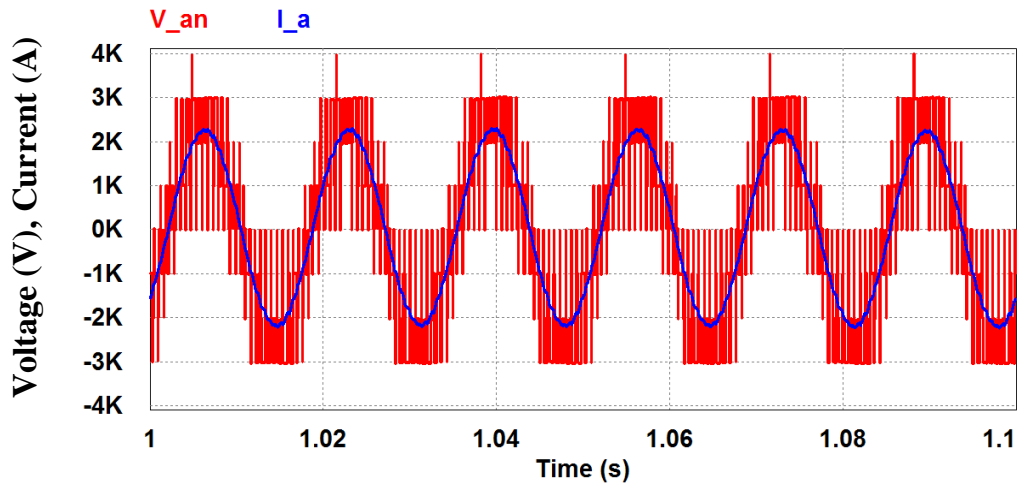
Figure 3-6: WTG terminal voltage and current for phase A of the positive pole module. Note terminal voltage with respect to ground is only ± half the DC link voltage.
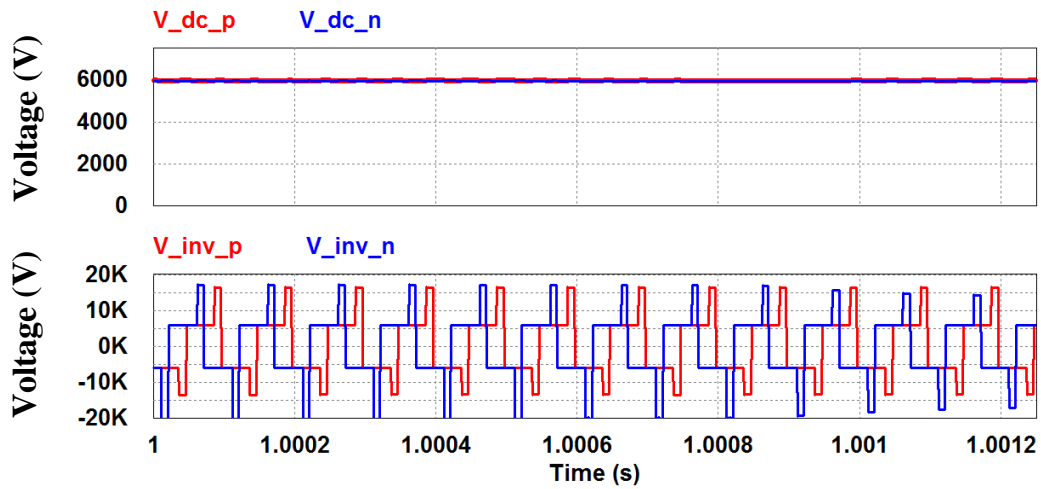
Figure 3-7: Positive and negative pole module DC link voltage as and inverter switching output voltages in steady state.
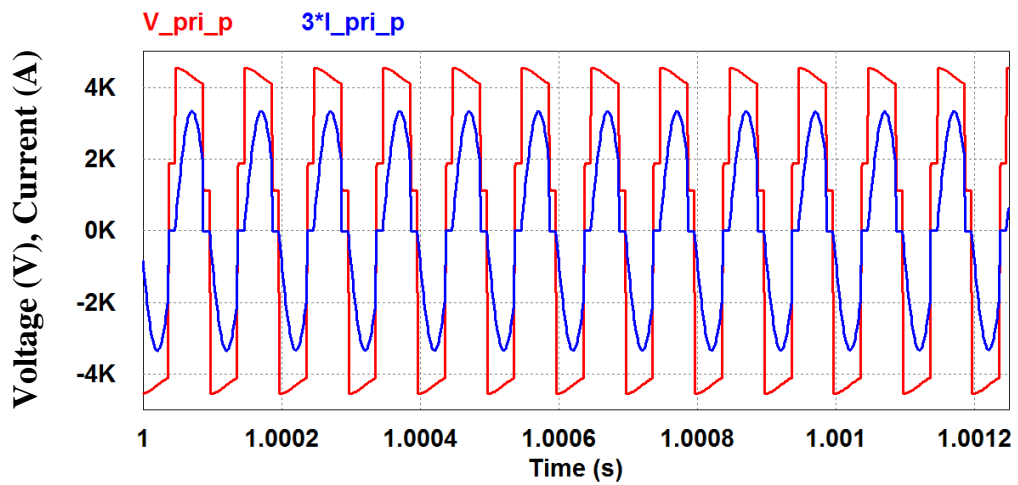
Figure 3-8: Steady state transformer voltage and current. Note ZCS and resonant frequency ripple riding on switching waveform.

A step change in wind velocity from 12 m/s to 6 m/s at t = 1.2s was used to carry out transient simulations, along with the WTG voltage, frequency, and power characteristics of [77], which demonstrate WTG voltage and frequency reducing to one

half and output power will reducing to one fourth of rated values post-transient given such a reduction in wind speed.

The output MVDC current is shown to settle to the new output level of 25 A after approximately 0.5 seconds in Figure 3-9. The low damping provided by the active MVDC source at the output results in some oscillation of the output current. This oscillation is not present and the output is significantly more damped when using an equivalent resistive load.

Figure 3-10 features the DC link voltage settling within 0.5 seconds post-transient, and the transformer primary currents reduce to half of their original peak values.

As expected, the WTG voltage and current are both shown to reduce in frequency following the transient in Figure 3-11. However, the WTG line-to-neutral voltage still clamps to half of the DC link voltage, resulting in no change of peak input voltage post-transient even though machine voltages within the WTG have dropped.
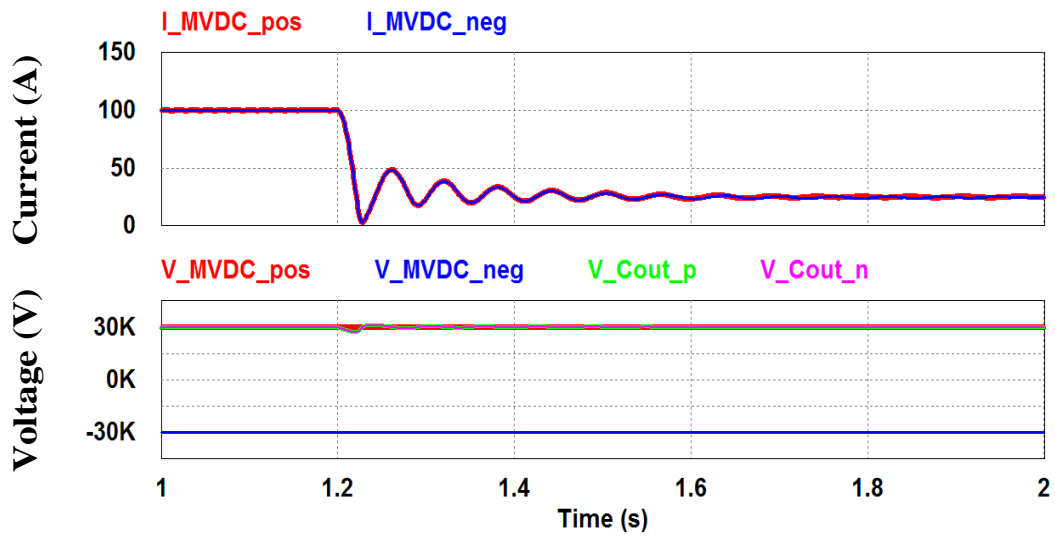
Figure 3-9: Output currents to MVDC grid and MVDC grid votlages during transient. While output current is drastically reduced, the output voltage remains fixed by the HVDC station and ripple is only a result of DC cable resistance.
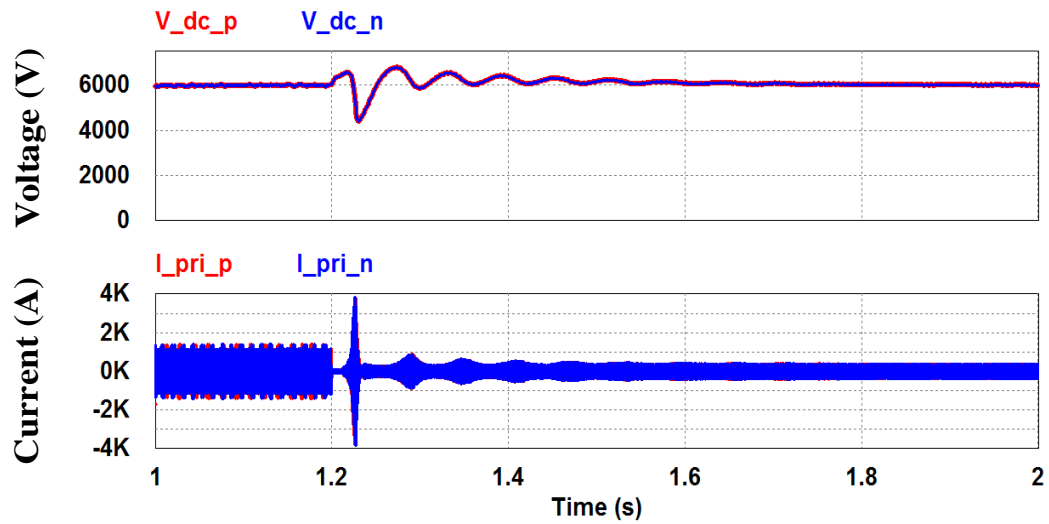
Figure 3-10: Simulated DC link voltages and transformer primary currents for both positive and negative pole modules during transient. DC link voltage initially sags during spike in transformer current, but both settle to new steady state values within 0.5 seconds.
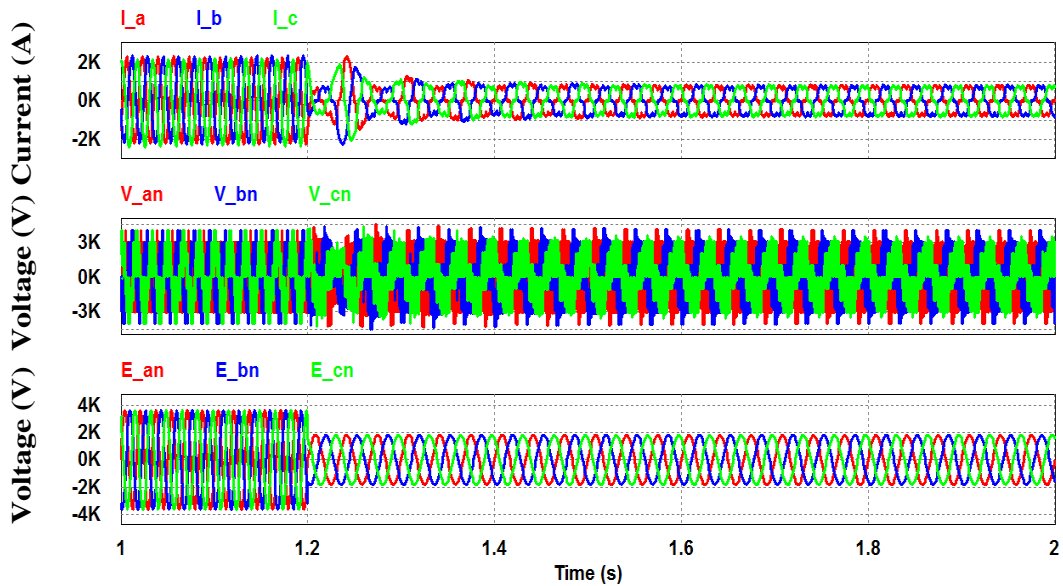
Figure 3-11: WTG terminal current and voltage, as well as internal machine voltage during transient.

3.5 Experimental Results

A lab-scale prototype of a single phase version of the input rectifier stage was constructed to validate the input power factor control and operating principle.

Figure 3-12 features waveforms from the AC input side of the prototype multilevel rectifier, as well as the full DC link voltage (Ch4, green). The input current (Ch1, yellow) exhibits mild 1.5 kHz switching ripple, but is nearly sinusoidal with fundamental current of 4.00 A_{rms} dominating approximately 0.8 A_{rms} third harmonic current as measured by the FFT trace (ChMath, red). The input current lags the converter terminal voltage (Ch2, blue) by 1 ms, which yields a power factor of approximately 0.92 lagging. The WTG internal voltage (Ch3, purple) is also captured. It can be observed that inductor current increases and converter terminal voltage collapses during active switch on time, while inductor current decays to the DC link and

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converter terminal voltage clamps to the DC link during switch on time, as expected from simulation.

Fig 13 features waveforms from the prototype rectifier DC link, including positive pole (Ch2, blue) and negative pole (Ch4, green) voltages showing balanced DC link operation. Balanced operation is achieved via addition of a small difference in average duty cycle between positive pole active switch pair S11/S12 and negative pole active switch pair S21/S22. Note that current into the DC link (Ch1, yellow) is only composed of decaying inductor current during switch off time, hence it has a high peak-to-average ratio.

Considering the input RMS fundamental current & voltage, and average DC link voltage & current the efficiency of this prototype is poor; however, this is due to the use of highly derated semiconductor devices such that prototype power and voltage may be scaled up rapidly when necessary.

Table 3-3: Lab-Scale Prototype Design Parameters

Input Parameter	Value
P_{out}	50 W
V_{WTG}	25 $V_{LN,rms}$
L_{WTG}	2.88 mH
f_{WTG}	60 Hz
f_{sw}	1.5 kHz
Displacement PF_{WTG}	>0.9
V_{DC}	50 V
C_{DC}	2.2 mF
IGBT	BSM 150GB 60
Diode	IRK D196-16
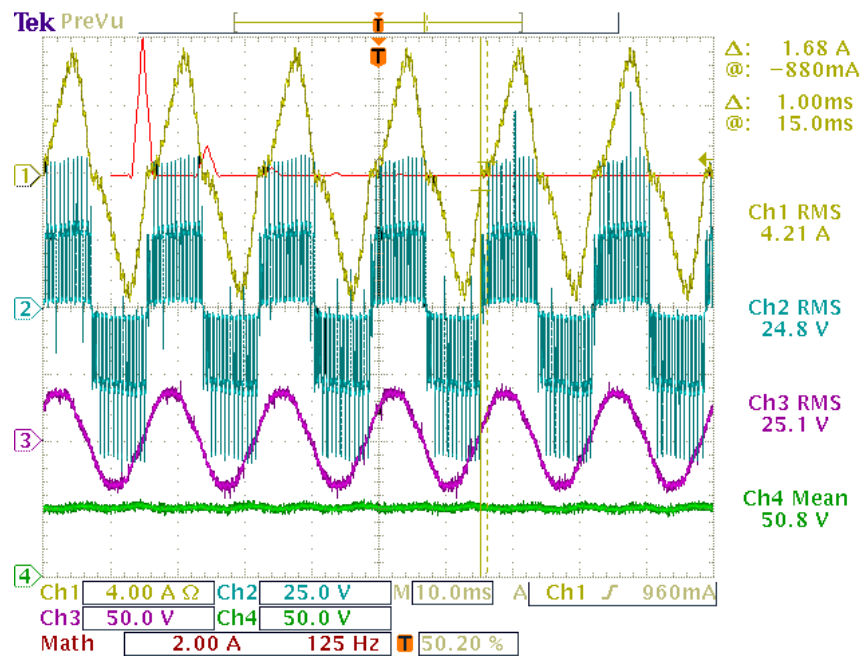
Figure 3-12: AC input waveforms of prototype single phase multilevel rectifier.
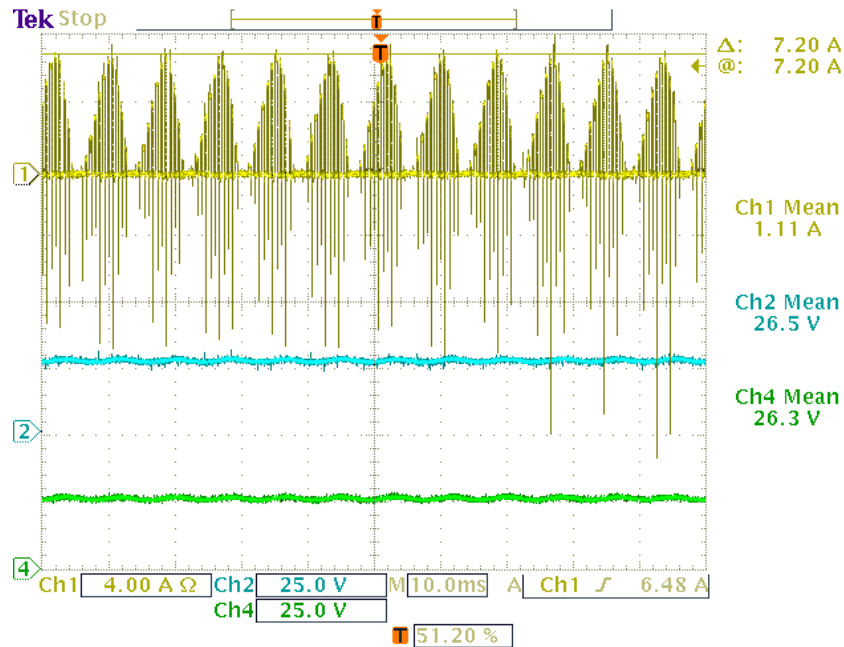
Figure 3-13: DC link waveforms of prototype single phase multilevel rectifier.

3.6 Conclusion

This work has proposed a new approach using high frequency (HF) isolation transformers with a series resonant power transfer mechanism for interfacing next-generation offshore wind turbine generators (WTGs) to medium voltage DC (MVDC) collection grids, a necessity for the continued development of offshore wind resources as farms are sited further out to sea.

Analysis and detailed simulation results demonstrate converter operation from full rated power down to 25% rated power. The WTG displacement power factor is found to be 0.96 lagging. The three-phase multilevel input rectifier allows 5 times reduction in DC link capacitance over the previous per-phase approach. Detailed simulation results confirm near-sinusoidal WTG and transformer currents, continuous

output currents, stiff DC link voltages and zero current switching (ZCS) in the HF inverter.

Experimental results from 50 W prototype single-phase multilevel input rectifier stage show high fidelity to simulation results, including measured displacement power factor of 0.92 lagging.

4. EXPLORING COMMON MODE VOLTAGE STRESS AND CIRCULATING CURRENTS IN OFFSHORE WIND TURBINE TO MVDC COLLECTION GRID INTERFACES[*]

This work investigates common mode (CM) voltage stress and circulating ground currents in two proposed power electronic interfaces for integrating next-generation offshore wind turbines (WTGs) to medium voltage DC (MVDC) collection grids. In addition to the DC CM voltage imposed by the MVDC grid, the use of switching power electronics results in high frequency (HF) CM voltage applied to the HF isolation transformers used in the proposed approaches. While DC CM voltages stress transformer insulation, HF CM voltages also cause current to flow through parasitic capacitances between transformer primary and secondary windings, as well as between transformer windings and the grounded chassis where it then circulates back to the WTG grounded neutral. Detailed simulation results indicate that use of a per-pole interface architecture leads to lower and more balanced CM voltage stress on isolation transformers, which would reduce cost and increase reliability of the interface. A CM filter and transformer shield are applied as mitigation strategies; corresponding simulation results show a reduction in the common mode current in the WTG neutral in both per-phase and per-pole interfaces.

4.1 Introduction

The world is entering an era of outstanding growth of energy demand as previously underdeveloped populations begin to adopt more energy-intensive lifestyles, requiring that new energy resources be developed to supply growing demand for transportation, communication, computing, and entertainment services, to name only a few[2]. At the same time humanity must consider the climatological consequences as new energy resources are exploited. These considerations have led many nations to develop offshore wind as an environmentally sound and economically viable energy resource[3].

The most distant offshore wind farms are now entering service[13], with Global Tech I, a 400 MW German installation undergoing commissioning in early 2015, sited approximately 100 km from shore[57]. The latest offshore WTGs have typical ratings of 5-6 MW at 3.3 kV and, in the case of Germany's Alpha Ventus wind farm, require almost a kilometer of inter-turbine spacing[17]. Proposed 8 and 10 MW WTGs may be available in the next few years[15], possibly requiring more than 1 km spacing between WTGs.

Due to the great distant that offshore wind energy must be transported before interfacing with the land-based AC grid in these cases, high voltage direct current (HVDC) transmission is typically used[16]. The presence of the HVDC link together with the growing inter-turbine spacing makes utilization of a medium voltage DC (MVDC) collection grid more suitable than the traditional MVAC architecture for aggregating WTG energy within the wind farm. Such an MVDC collection grid

architecture is illustrated in Figure 4-1. The MVDC architecture has the following advantages compared to the MVAC collection grid[26]:

- Elimination of line frequency transformers.

- Simplification of collection grid undersea cabling.

- Elimination of inter-turbine power flow issues.

- Simplification of HVDC converter station interface.
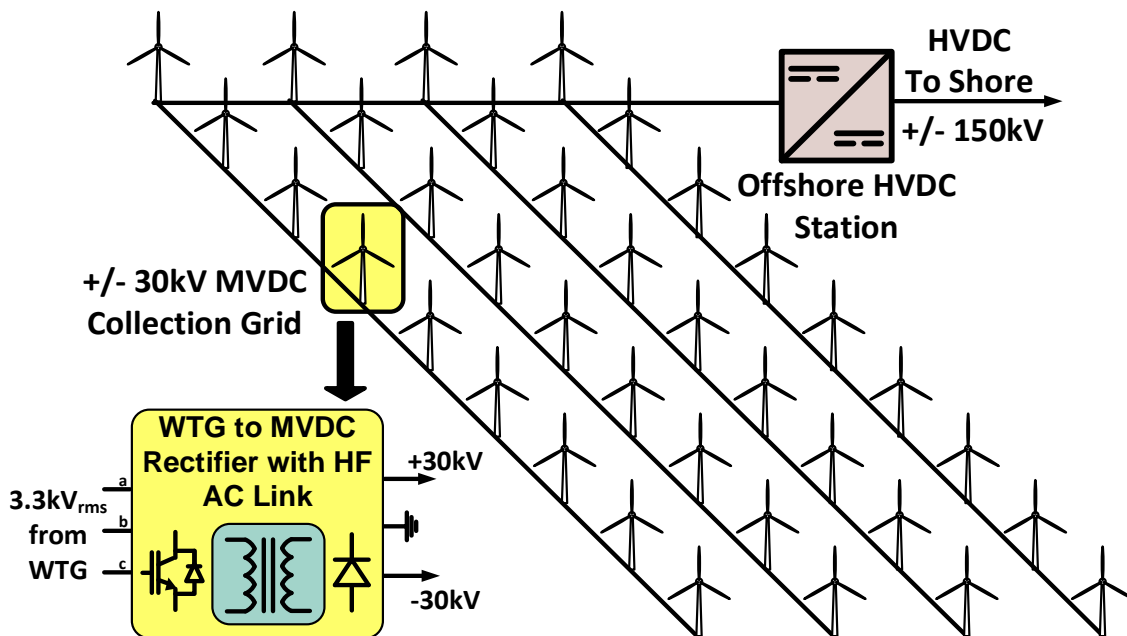
Figure 4-1: WTG interface to offshore wind farm with +/-30 kV MVDC collection grid architecture and HVDC link to shore.

This work is based on two recently proposed WTG-to-MVDC collection grid approaches as described in [61]-[62]. These approaches share the same overall conversion strategy and architecture; however they are fundamentally different in their interconnection to WTG and MVDC grid. The first approach, shown in Figure 4-2, is

considered the "per-phase" approach in that each end-to-end conversion module interfaces a single phase of the WTG to the MVDC grid; hence there are three end-to-end "phase" conversion modules. The second approach, shown in Figure 4-5, is considered the "per-pole" approach in that each end-to-end conversion module interfaces an entire MVDC pole to all three WTG phases; hence there are only two end-to-end "pole" conversion modules. Both approaches share similar design principles and control schemes as described in [61]-[62] and summarized in Table 4-1. The following advantages are realized by these interfaces when compared to other approaches for WTG-to-MVDC integration described in [22],[58],[60]:

- Provides "end-to-end" conversion interface from WTG to MVDC grid

- Provides galvanic isolation

- High output diode rectifier device rating utilization

- Fewer inverter input capacitor voltage levels to balance

- Conventional direct-drive synchronous generator.

- Compact high frequency transformer.

- Input current shaping capability for PFC.

- Large generator inductance is an advantage for multilevel rectifier boost PFC operation.

- Reduced DC link capacitance in per-pole interface

Table 4-1: WTG-to-MVDC Interface Design Parameters

Parameter	Per-Phase Value	Per-Pole Value
P_{WTG}	8 MW	6 MW
V_{WTG}	3.3 $kV_{LL,rms}$	3.3 $kV_{LL,rms}$
X_{WTG}	0.625 p.u.	0.6 p.u.
f_{WTG}	60 Hz	60 Hz
Displacement PF_{WTG}	> 0.9	> 0.9
V_{MVDC}	± 30 kV (60 kV)	± 30 kV (60 kV)
L_{leak}	0.05 p.u.	0.05 p.u.
RF_{VMVDC}	0.05	0.05
RF_{IMVDC}	0.1	0.1
RF_{VDC}	0.05	0.05
L_{WTG}	2.26 mH	2.88 mH
L_{in}	10 μH	10 μH
V_{dc}	4 kV	6 kV
C_{dc}	50 mF	10 mF
f_{inv}	10 kHz	10 kHz
$N_p{:}N_s$	1:8	1:7
L_{leak}	3.85 μH	7.7 μH
C_{out}	500 μF	500 μF
L_{MVDC}	500 mH	500 mH
R_{MVDC}	200 mΩ	200 mΩ
$R_{balance}$	1 MΩ	-

The differences in WTG power between the per-phase and per-pole approaches is due to the reduced number of HFTs in the per-pole approach available to process WTG power. This reduction in overall power, combined with the necessary higher DC link voltage due to the phase-to-phase input connection, yields not only a smaller DC link capacitance but also a larger generator synchronous reactance, lower transformer turns ratio, and higher transformer leakage reactance.

4.2 Per-Phase Interface

A common mode equivalent circuit must first be developed before analysis of common mode voltages and associated circulating currents can be carried out. Each power converter has both a differential and CM output voltage. The differential voltage is the desired output, but high frequency (HF) CM voltage appears due to the switching power electronics rapidly connecting and disconnecting converter output nodes to the DC bus [83]. Additionally, DC CM voltage appears due to the elevation of the MVDC grid. Both HF and DC CM voltage accumulate at the HF transformer, stressing transformer insulation above the nominal voltage ratings of the system. The HF CM voltage leads to current flow in transformer parasitic capacitances between windings, and between windings and the grounded chassis, where it then circulates back to the WTG grounded neutral[84]. The DC CM voltage does not contribute to circulating current as it has no time varying component to pass through the parasitic capacitors.

An equivalent circuit can be developed by considering the switching CM voltage produced between input and output nodes of each converter, as well as the DC potential between the output rectifier nodes and the MVDC grid. We are interested in CM

voltage, hence converter nodes that have primarily differential voltage, such as nodes "a" & "g" in the phase "a" module of Figure 4-2, are shorted. The WTG internal voltage is neglected as it is AC in nature and has no CM contribution. The result is the equivalent circuit shown in Figure 4-3. For simplicity only phase module "a" is illustrated. Applying (4.1)-(4.7) we can simplify Figure 4-3 to the equivalent circuit shown in Figure 4-4. Observing Figure 4-4 the circulating current can be described according to (4.8)-(4.12). A similar analysis can be carried out for the remaining two phase modules; while each would have a similar structure on the primary side of the transformer, V_{sg} and V_{ps} would be different due to different connection points to the MVDC grid.

Note that the parasitic capacitors of interest form a closed loop from ground to primary winding, to secondary winding, and back to the ground node. Therefore, as the secondary common mode voltage stress is dominated by the MVDC connection, so is the common mode voltage stress between the primary and secondary windings. This loop can be broken (short-circuited) via insertion of a grounded "shield" between primary and secondary windings such that the capacitance between the two windings is eliminated. This of course comes at the cost of increasing the capacitance between each winding and the ground node. While this does little to mitigate common mode voltage stress it can shorten circulating current paths and hence reduce the areas in which dangerous step and touch potentials may develop. This method of addressing circulating currents is investigated in a later section of this paper.
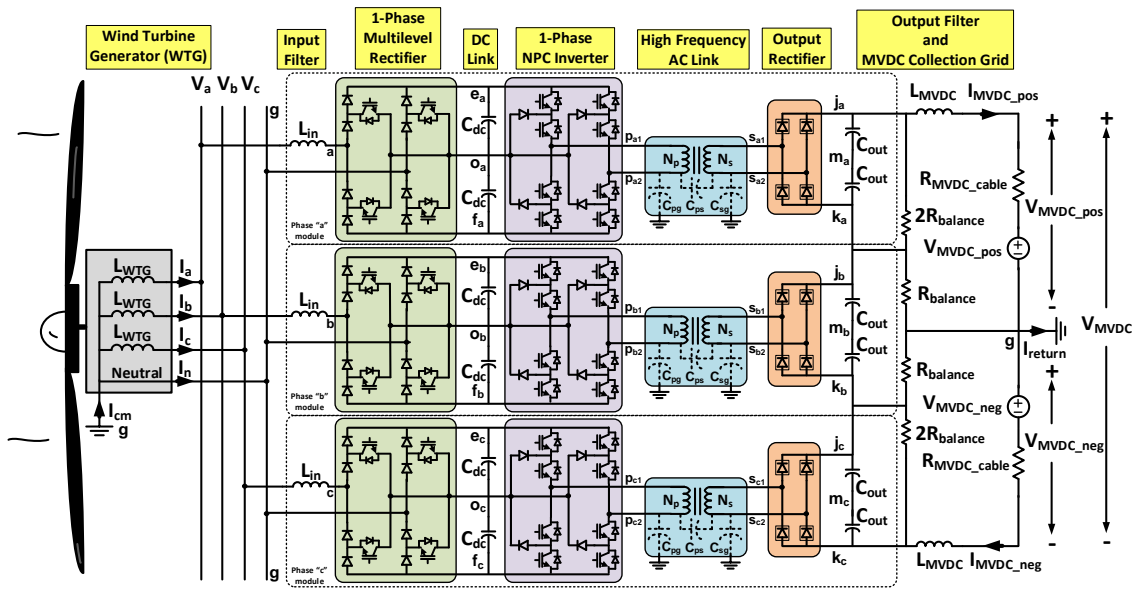
Figure 4-2: Per-phase interface using three end-to-end modules. Note the parasitic capacitances superimposed on each transformer. Outlined diodes indicate multiple devices in series.
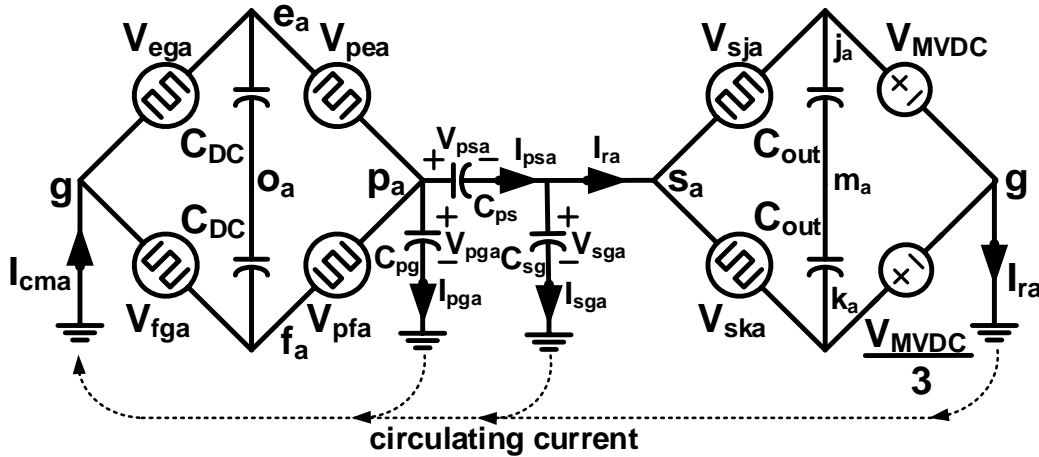
Figure 4-3: Detailed phase "a" CM equivalent circuit in per-phase approach.
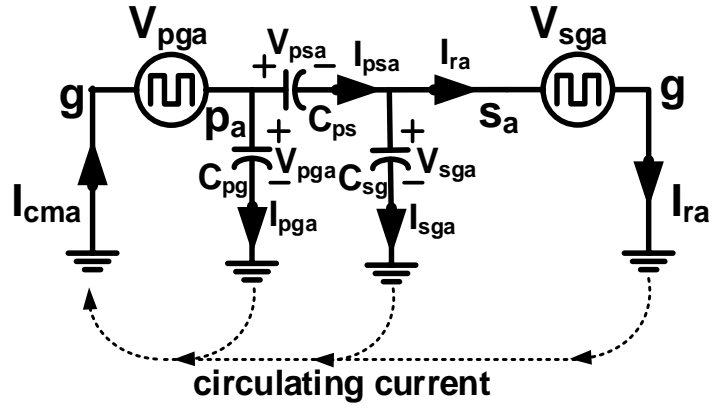
Figure 4-4: Simplified phase "a" CM equivalent circuit.

$$V_{og} = \frac{V_{eg} + V_{fg}}{2} \tag{4.1}$$

$$V_{po} = \frac{V_{eg} + V_{fg}}{2} \tag{4.2}$$

$$V_{sm} = \frac{V_{sj} + V_{sk}}{2} \tag{4.3}$$

$$V_{mg} = \frac{V_{MVDC} + \frac{V_{MVDC}}{3}}{2} \tag{4.4}$$

$$V_{pg} = V_{og} + V_{po} \tag{4.5}$$

$$V_{sg} = V_{mg} + V_{sm} \tag{4.6}$$

$$V_{ps} = V_{pg} - V_{sg} \tag{4.7}$$

$$I_{pg} = C_{pg} \frac{dV_{pg}}{dt} \tag{4.8}$$

$$I_{ps} = C_{ps} \frac{d(V_{pg} - V_{sg})}{dt} \tag{4.9}$$

$$I_{cma} = I_{pg} + I_{ps} \tag{4.10}$$

$$I_{cm} = I_{cma} + I_{cmb} + I_{cmc} \tag{4.11}$$

$$I_{return} = I_{ra} + I_{rb} + I_{rc} \tag{4.12}$$

4.3 Per-Pole Interface

Using the same modeling approach described in the previous section, the CM equivalent circuit for the per-pole approach can be developed as shown in Figure 4-6. In the per-phase case each phase leads to a separate input converter and can be considered shorted to the grounded neutral for common mode purposes. In the per-pole case all three phases connect to the same input converter, so the WTG impedance must be included in the model to prevent short circuit of CM voltages at the input.

Note that in Figure 4-6 node "d" is shorted to ground node "g"; similarly node "h" would be shorted to ground node "g" in the pole "n" module equivalent circuit. Figure 4-6 can be simplified via (4.13)-(4.19) to the equivalent circuit featured in Figure 4-7, and circulating currents can be described by (4.20)-(4.24).
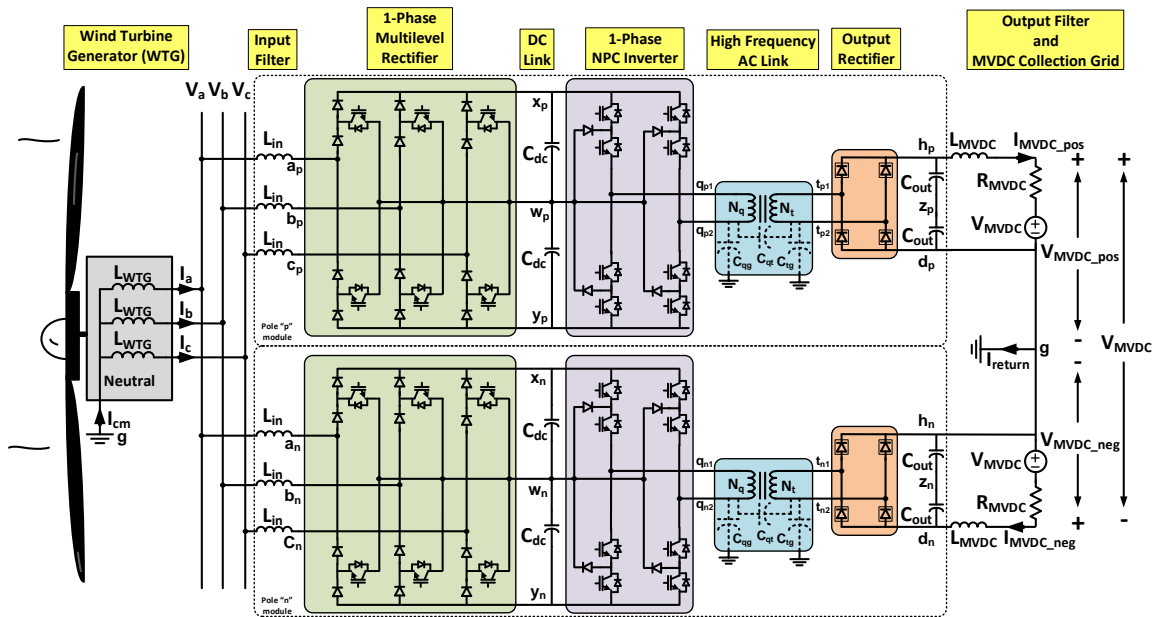
Figure 4-5: Per-pole interface using three end-to-end modules. Note the parasitic capacitances superimposed on each transformer.
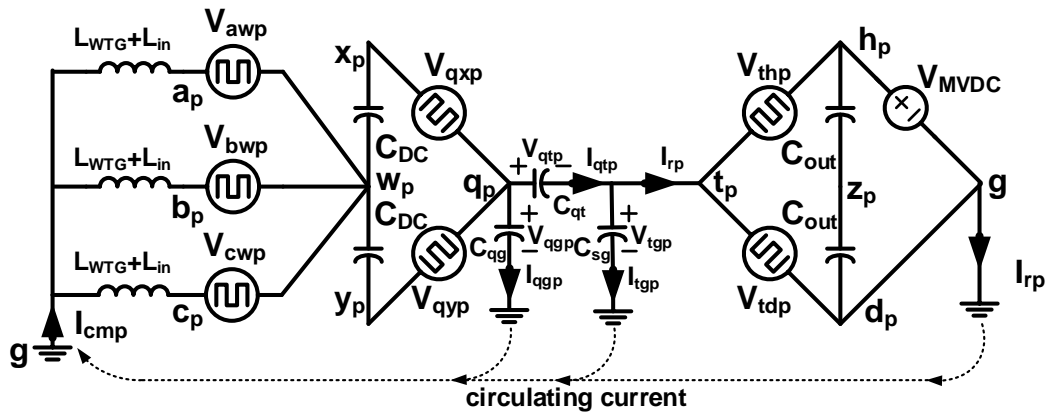
Figure 4-6: Detailed pole "p" CM equivalent circuit in per-pole approach.
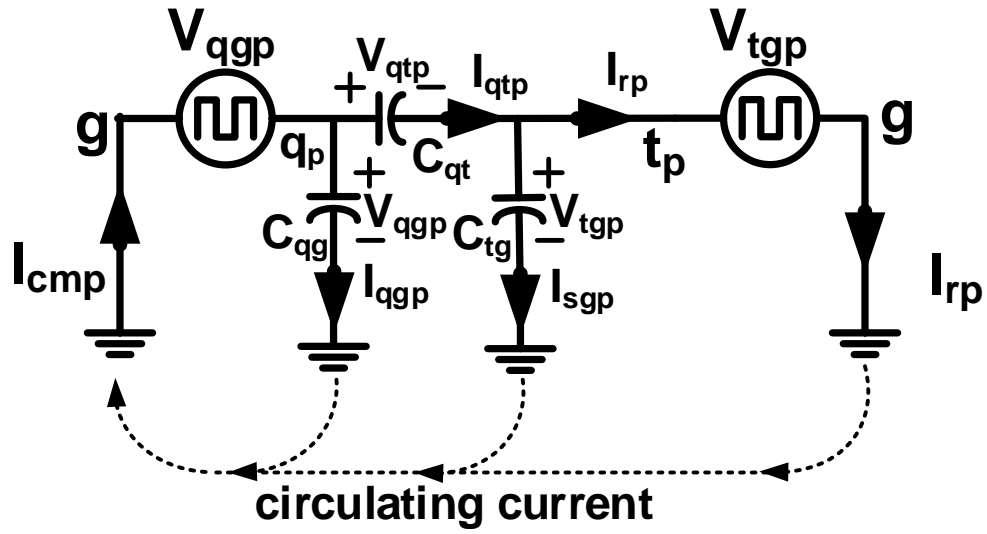
Figure 4-7: Simplified pole "p" CM equivalent circuit.

$$V_{wg} = \frac{V_{aw} + V_{bw} + V_{cw}}{3} \tag{4.13}$$

$$V_{qw} = \frac{V_{qx} + V_{qy}}{2} \tag{4.14}$$

$$V_{zg} = \frac{V_{MVDC}}{2} \tag{4.15}$$

$$V_{tz} = \frac{V_{td} + V_{th}}{2} = \frac{V_{tg} + V_{th}}{2} \tag{4.16}$$

$$V_{qg} = V_{qw} + V_{wg} \tag{4.17}$$

$$V_{tg} = V_{zg} + V_{tz} = V_{th} + V_{MVDC} \tag{4.18}$$

$$V_{qt} = V_{qg} - V_{tg} \tag{4.19}$$

$$I_{qg} = C_{qg} \frac{dV_{qg}}{dt} \tag{4.20}$$

$$I_{qt} = C_{qt} \frac{d(V_{qg} - V_{tg})}{dt} \tag{4.21}$$

$$I_{cmp} = I_{qg} + I_{qt} \tag{4.22}$$

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$$I_{cm} = I_{cmp} + I_{cmn} \qquad (4.23)$$

$$I_{return} = I_{rp} + I_{rn} \qquad (4.25)$$

4.4 Simulation Results

Simulations were carried out using $C_{pg} = C_{sg} = C_{qt} = C_{tg} = 500$ pF and $C_{ps} = C_{qt} =$ 1 nF [83],[84], assuming proportional geometry of windings and chassis relative to a line frequency transformer.

Per-phase results are shown in Figure 4-8 – Figure 4-14 while per-pole results are shown in Figure 4-15 – Figure 4-21. Both sets of results are summarized in Tables 4-2 and 4-3. The results show that the per-pole approach provides lower and more balanced DC common mode voltage stress on each transformer although HF circulating currents are generally higher. The greatest difference in circulating current magnitude occur in primary-to-ground, I_{cm}, and I_{return}, which are 1 to 2 orders of magnitude larger in the per-pole approach.

To enhance the simulation all inductors are considered to have an $\omega L{:}R$ ratio of 200:1; resulting inductor resistances are included in the simulation. Capacitor ESRs are also accounted for by introducing a series resistor across which 0.1% of each capacitor voltage is dropped. Diode and IGBT on-state voltages of 1.7 V and 3.1 V, respectively, were included based on datasheets for devices [69] and [68].
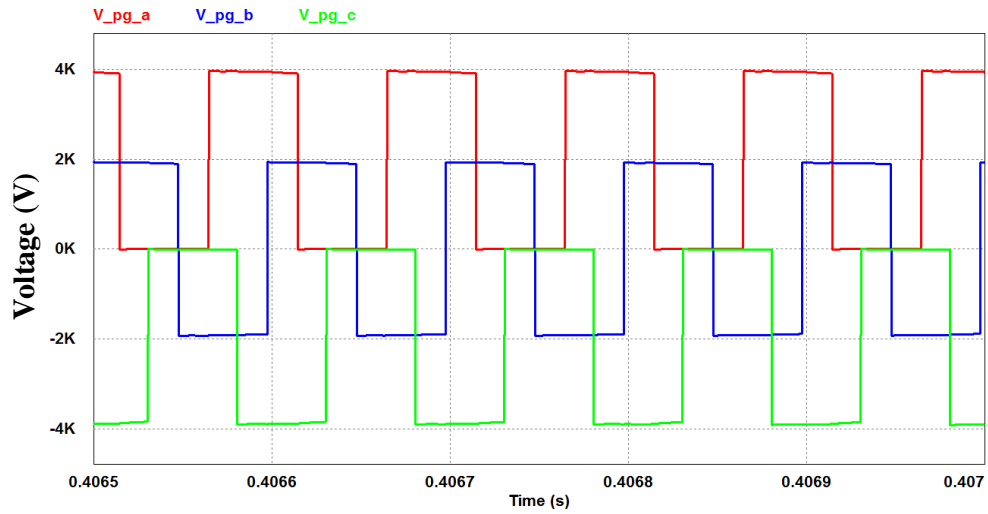
Figure 4-8: Voltage across C_{pg} in each phase of per-phase approach. Note that depending on WTG voltage phase, the DC value of each waveform in Figure 4-8 moves between -2 kV, 0 V, and +2 kV, hence each has approximately zero average as reflected in Table 4-2.
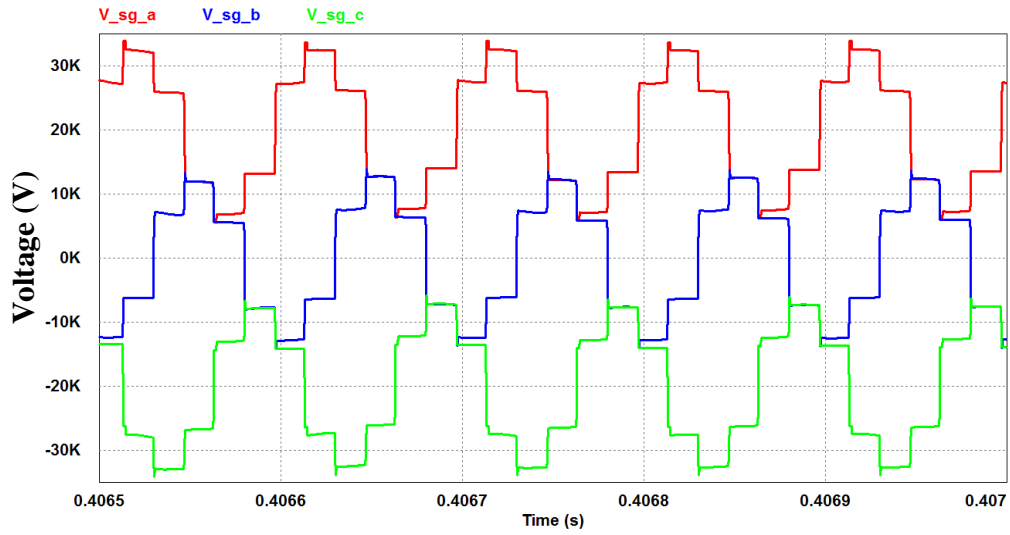
Figure 4-9: Voltage across C_{sg} in each phase of per-phase approach.
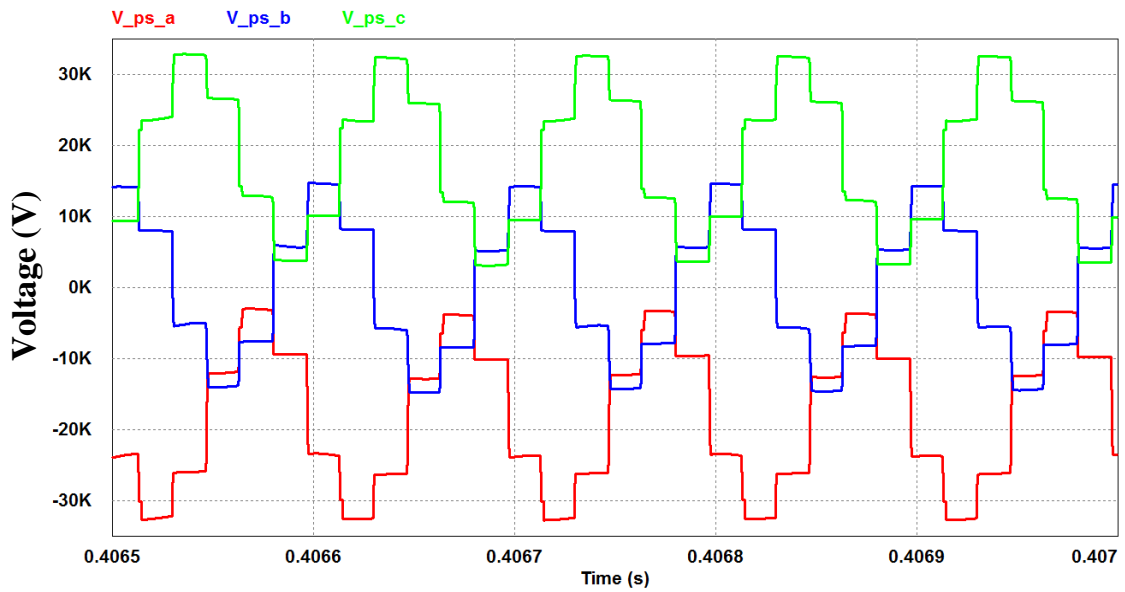
Figure 4-10: Voltage across C_{ps} in each phase of per-phase approach.
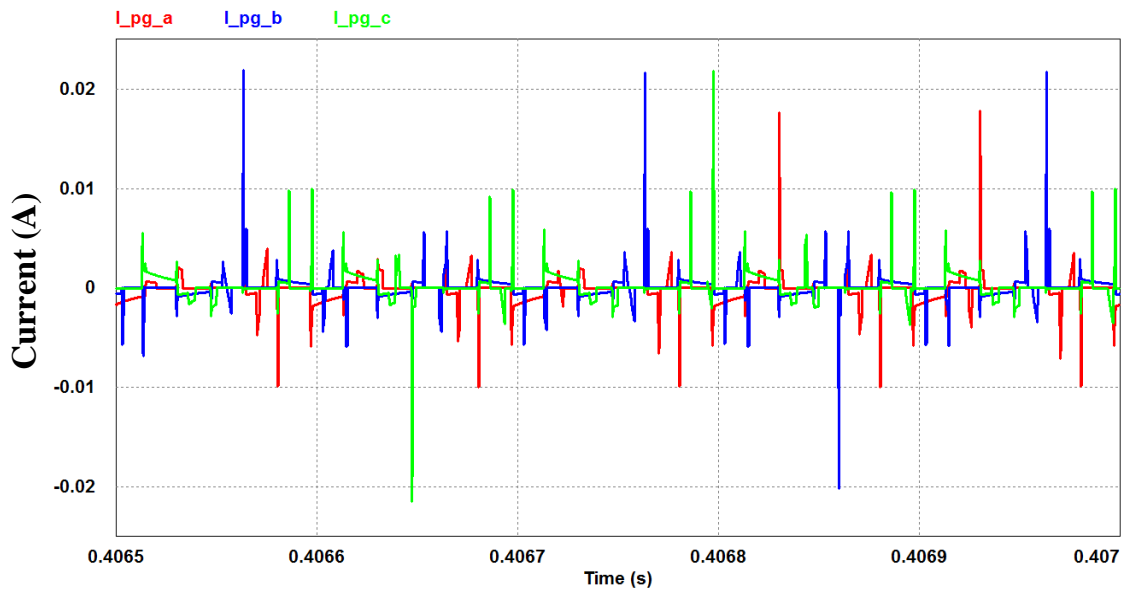
Figure 4-11: Current through C_{pg} in each phase of per-phase approach.

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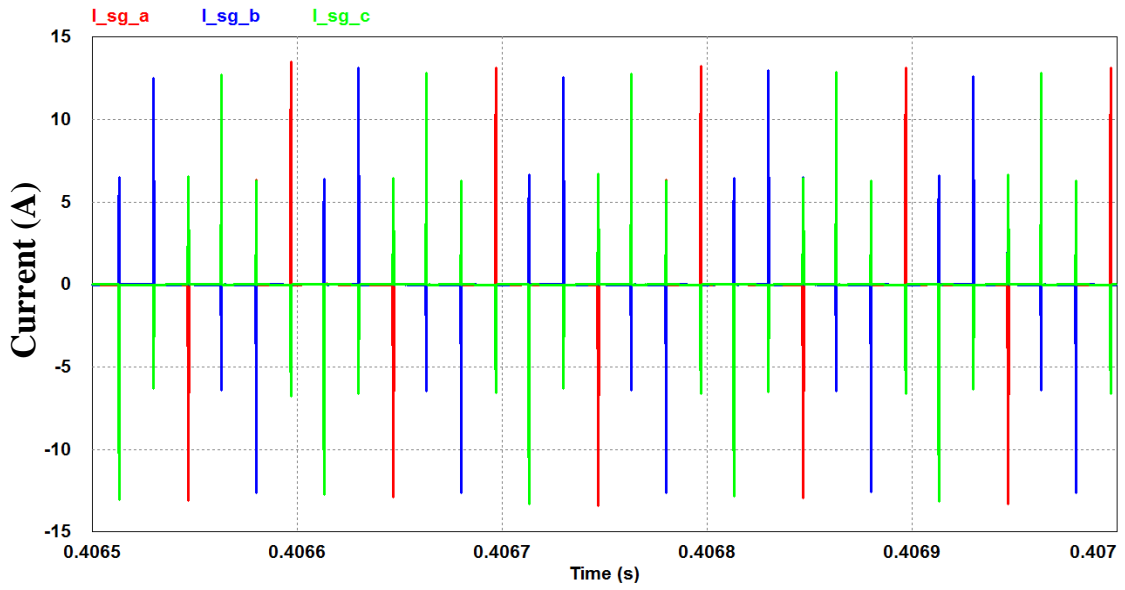
Figure 4-12: Current through C_{sg} in each phase of per-phase approach.
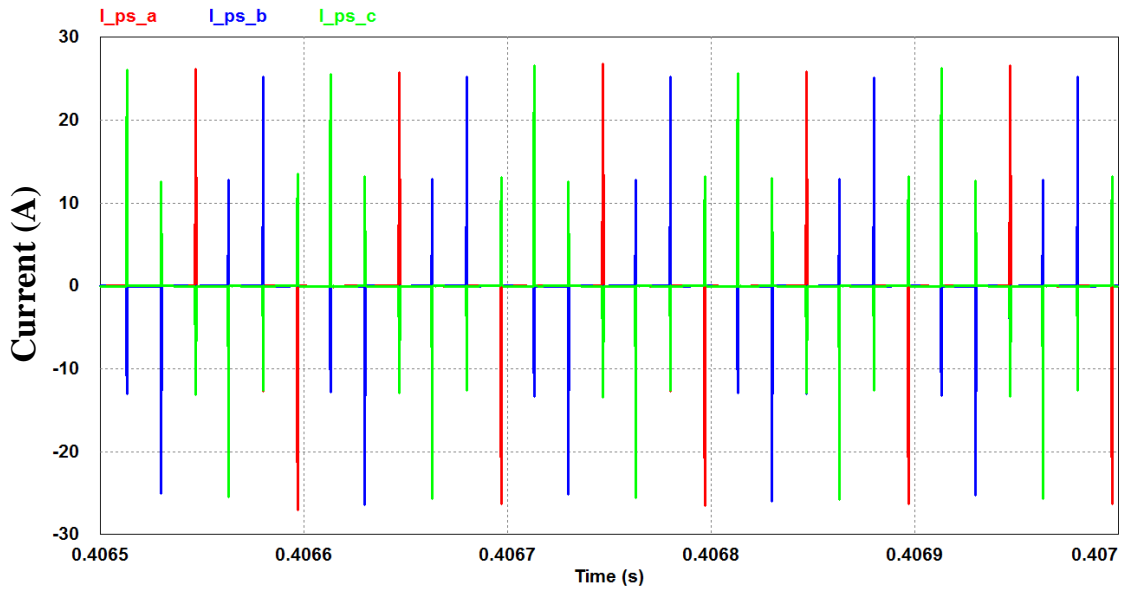
Figure 4-13: Current through C_{ps} in each phase of per-phase approach.
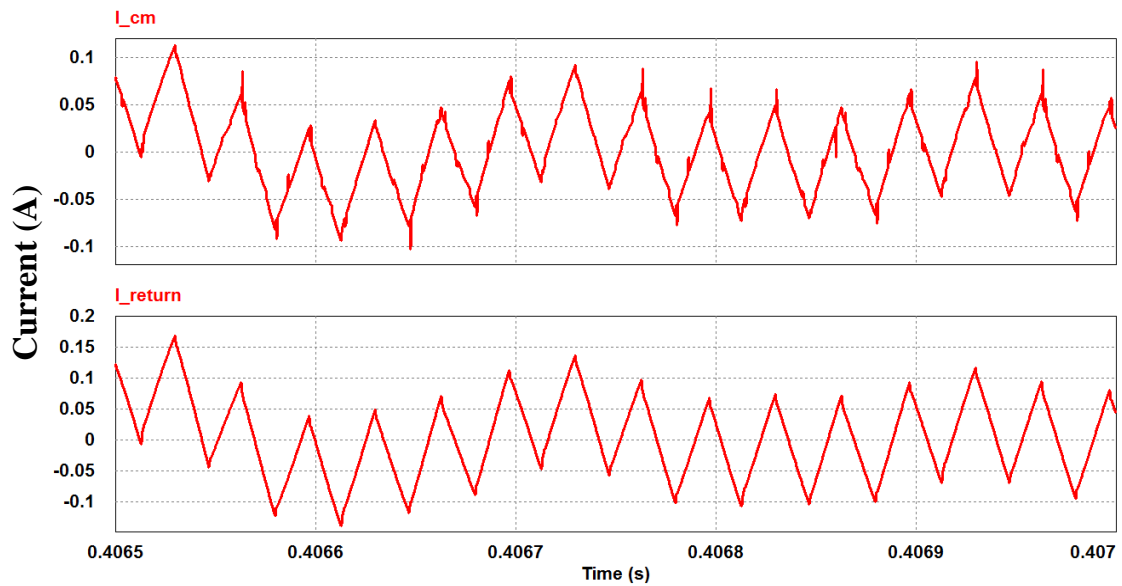
Figure 4-14: I_{cm} entering WTG neutral and I_{return} exiting MVDC ground.
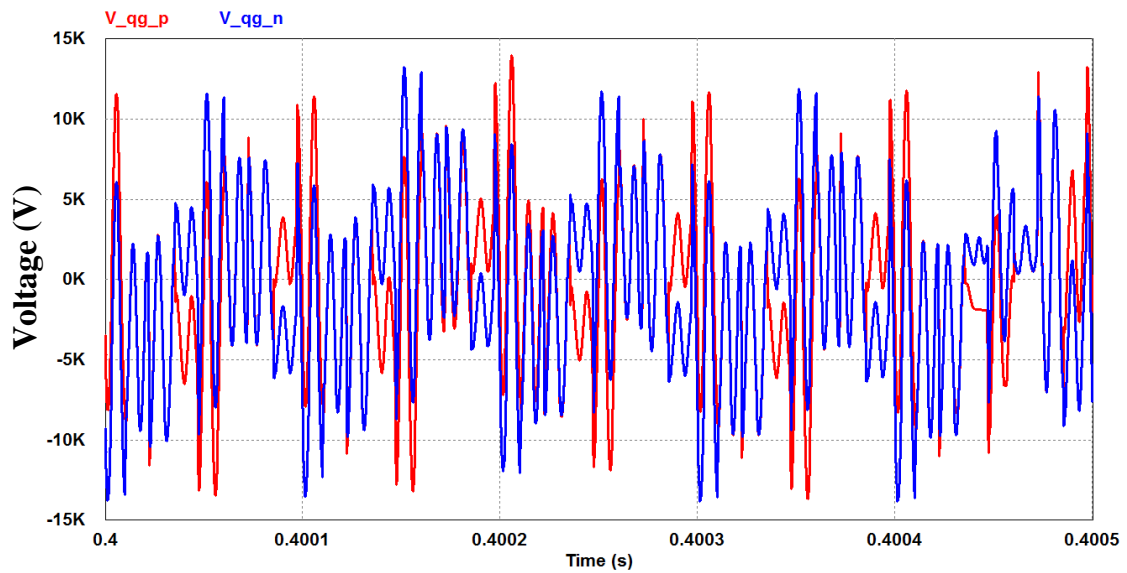
Figure 4-15: Voltage across C_{qg} in each pole of per-pole approach.

Note the high peak currents in every parasitic capacitor due to the large change in

voltage over a short time during each inverter switching instant. While this effect can be

mitigated via introduction of a larger IGBT gate resistance to reduce dv/dt at the HFT,

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this has the effect of increasing losses due to increased conduction during switching. Use of a soft-switching converter avoids these extra losses.
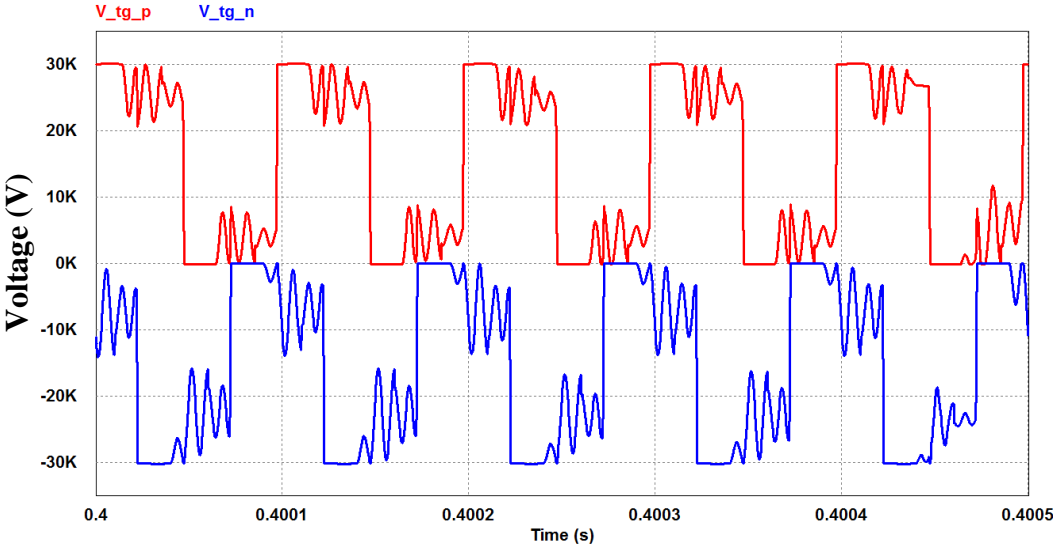
Figure 4-16: Voltage across C_{tg} in each pole of per-pole approach.
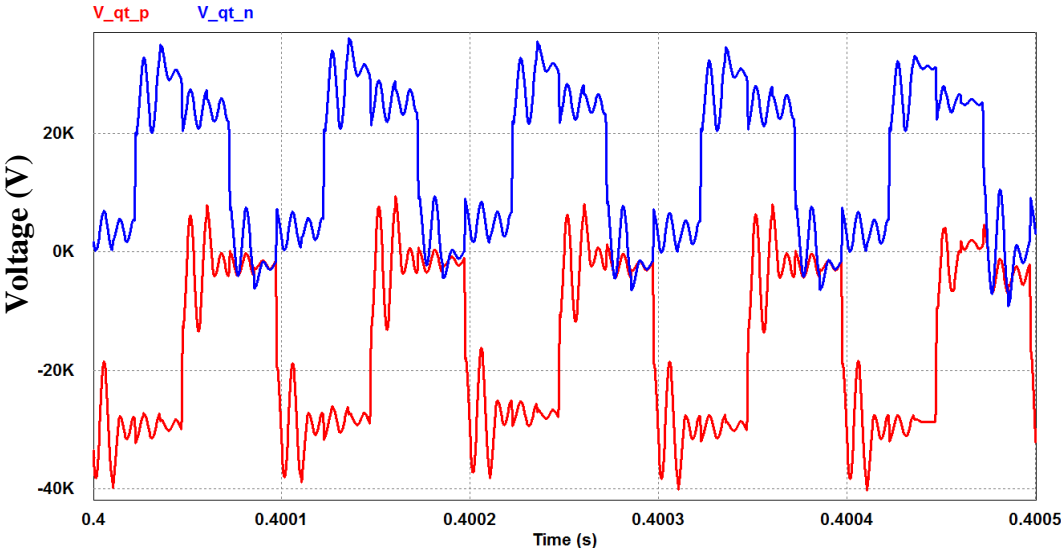
Figure 4-17: Voltage across C_{qt} in each pole of per-pole approach.
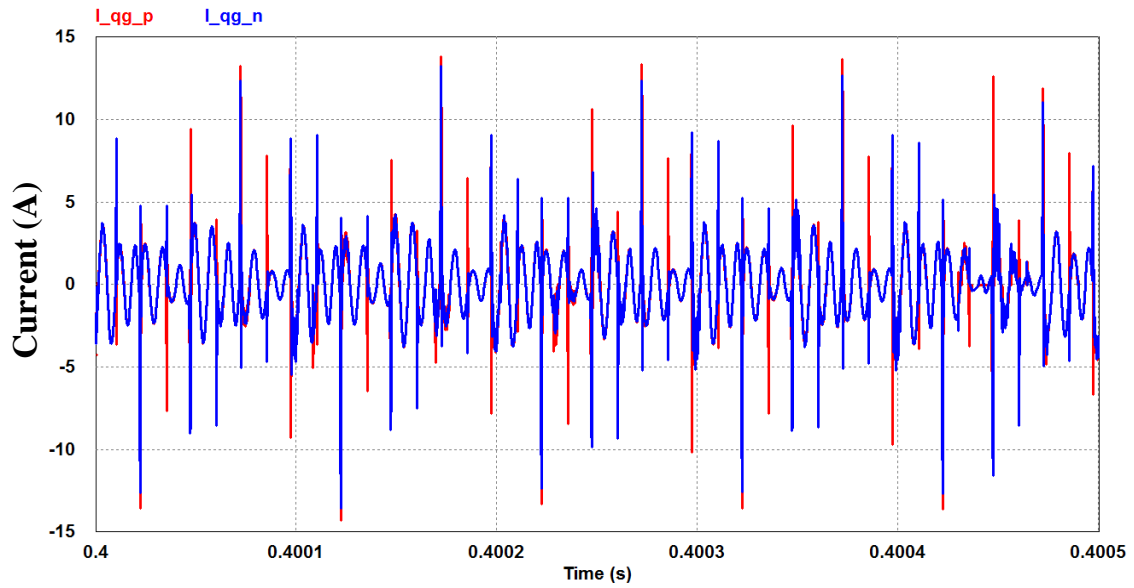
Figure 4-18: Current through C_{qg} in each pole of per-pole approach.
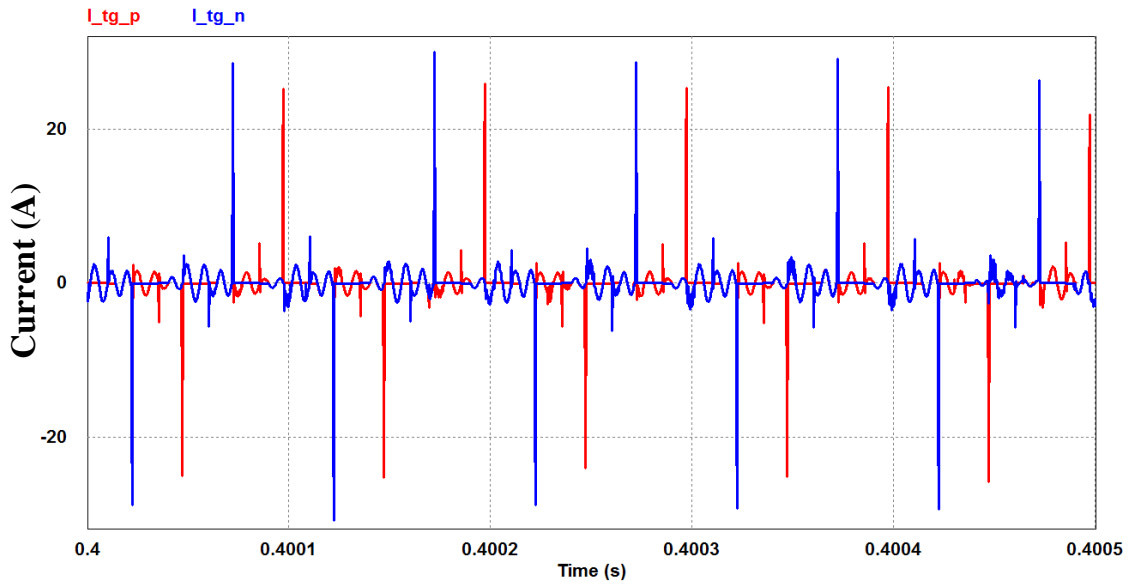
Figure 4-19: Current through C_{tg} in each pole of per-pole approach.

The HF ringing observed on the common mode voltages of the per-pole approach are reflected in the current through each capacitor, yielding RMS values generally larger

than those of the per-phase approach. This difference is most notable between C_{pg} and C_{qg}; the current through C_{qg} an RMS value greater by 2 orders of magnitude.
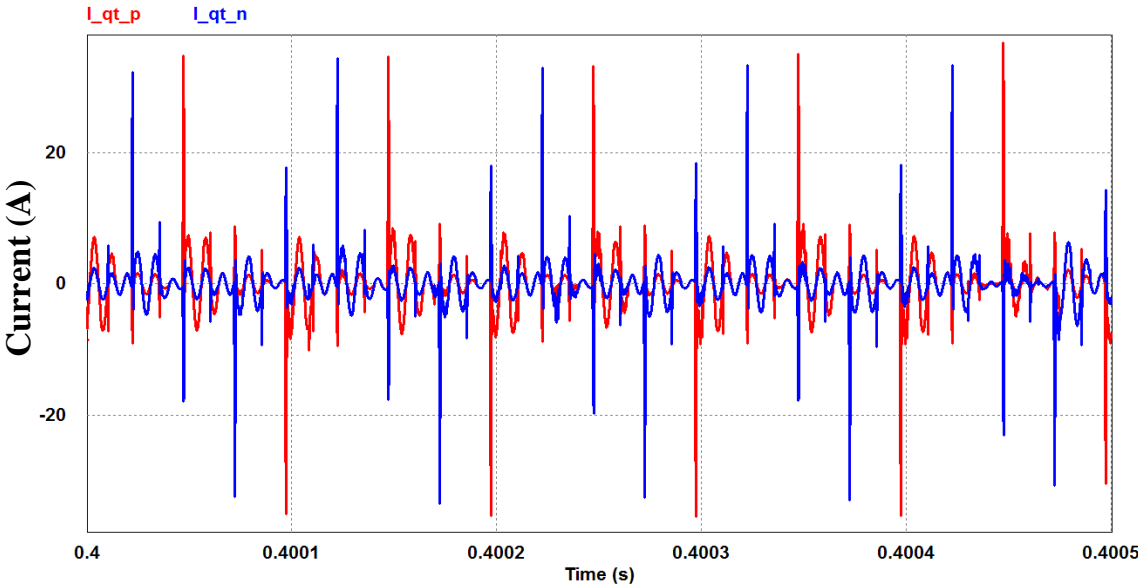
Figure 4-20: Current through C_{qt} in each pole of per-pole approach.
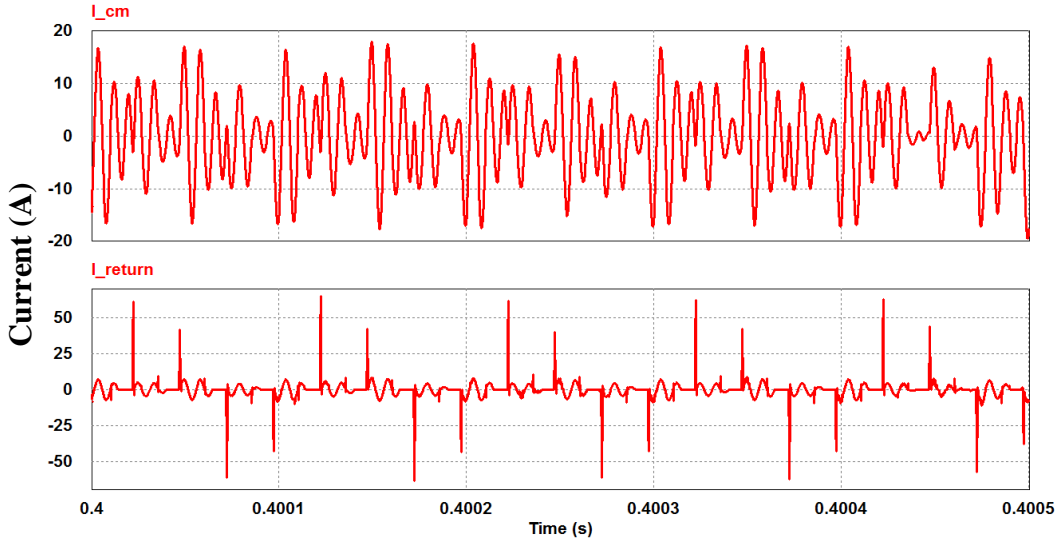
Figure 4-21: I_{cm} entering WTG neutral and I_{return} exiting MVDC ground.

Table 4-2: Per-phase CM voltages and currents

V_{pga}	-4.65 V_{dc}	I_{pga}	44.60 mA$_{rms}$	I_{cm}	185.05 mA$_{rms}$
V_{sga}	19.94 kV_{dc}	I_{sga}	1.21 A$_{rms}$	I_{return}	64.32 mA$_{rms}$
V_{psa}	-19.94 kV_{dc}	I_{psa}	2.43 A$_{rms}$		
V_{pgb}	6.39 V_{dc}	I_{pgb}	84.59 mA$_{rms}$		
V_{sgb}	-12.40 V_{dc}	I_{sgb}	1.19 A$_{rms}$		
V_{psb}	18.79 V_{dc}	I_{psb}	2.38 A$_{rms}$		
V_{pgc}	-3.09 V_{dc}	I_{pgc}	50.53 mA$_{rms}$		
V_{sgc}	-19.97 kV_{dc}	I_{sgc}	1.20 A$_{rms}$		
V_{psc}	19.97 kV_{dc}	I_{psc}	2.40$_{rms}$		

Table 4-3: Per-pole CM voltages and currents

V_{qgp}	-6.33 V_{dc}	I_{qgp}	2.38 A$_{rms}$	I_{cm}	7.85 A$_{rms}$
V_{tgp}	14.97 kV_{dc}	I_{tgp}	2.25 A$_{rms}$	I_{return}	6.77 A$_{rms}$
V_{qtp}	-14.98 kV_{dc}	I_{qtp}	4.18 A$_{rms}$		
V_{qgn}	-3.61 V_{dc}	I_{qgn}	2.29 A$_{rms}$		
V_{tgn}	-14.93 kV_{dc}	I_{tgn}	2.52 A$_{rms}$		
V_{qtn}	14.92 kV_{dc}	I_{qtn}	3.73 A$_{rms}$		

The improved balance and overall reduction in DC common mode voltage stress in the per-pole approach may help to provide easier manufacturability due to a single transformer design with respect to voltage stress and insulation coordination.

However, the total return current from the MVDC grid and HF common mode current into the generator neutral is significantly higher in the per-pole case, which could cause dangerous step- and touch-potentials to form between the earth and the WTG

neutral connection. For example, a bond impedance of 10 Ω between the per-pole WTG neutral and earth would yield nearly 80 V_{rms} of high-frequency voltage.

4.5 CM Filter and Shielded Transformer

To reduce the current I_{cm} returning to the WTG a common mode filter adapted from [85] can be added to the primary-side rectifier and inverter in both per-phase and per-pole interfaces as shown in Figs. 22 and 23, respectively. These CM filters are composed of C_{fWTG} & R_{fWTG}, and C_{finv} & R_{finv}, which are designed according to [85] such that they form L-C-R filters with L_{WTG} and L_{leak} which slow the dv/dt seen at the WTG and HFT primary terminals, thereby reducing circulating current. In effect, the CM filter provides a lower impedance path for circulating currents to return to the DC link neutral point instead of the WTG neutral. Both rectifier and inverter CM filters in the per-phase interface are designed for a rise time of 2.5 μs; CM filters in the per-pole approach are also designed for a rise time of 2.5 μs. Resulting filter values are given in Table 4-4.
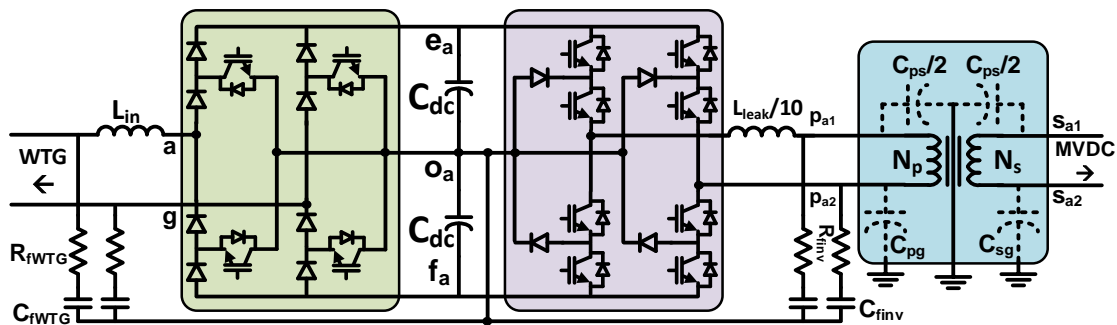
Figure 4-22: Phase "a" module with common mode filters and shielded transformer. Note additional discrete inductance equal to transformer leakage is added at inverter output to decouple C_{dc} and C_{finv} when inverter switches are closed and improve filter performance.
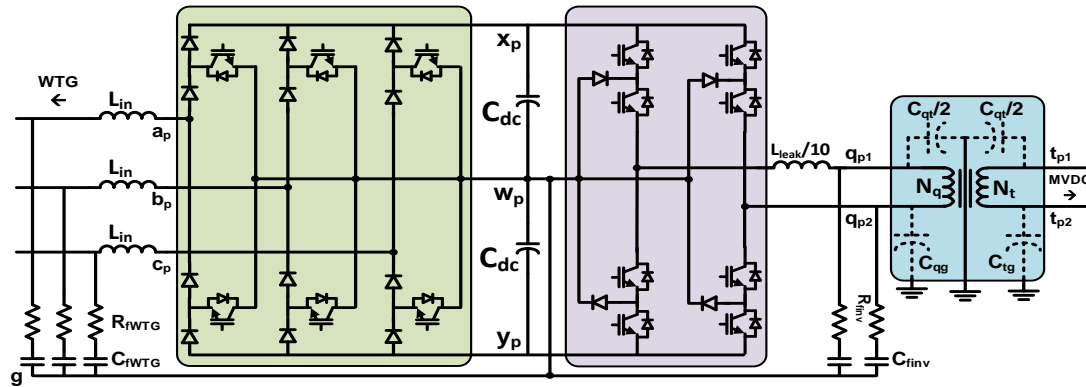
Figure 4-23: Pole "p" module with common mode filters and shielded transformer. Additional L_{leak} included as in per-phase case; see Figure4-22.

Table 4-4: CM filter component values

	Per-Phase	Per-Pole
C_{fWTG}	1.38 nF	2.16 nF
R_{fWTG}	1.82 kΩ	1.16 kΩ
C_{finv}	812 nF	406 nF
R_{finv}	3.08 Ω	6.16 Ω

To decouple the current returning from the MVDC grid and the common mode current entering the WTG neutral an earth-grounded shield can be introduced between the primary and secondary windings of the HFT. This shield effectively eliminates C_{ps} and C_{qt}, and splits those capacitances in parallel with C_{pg}, C_{sg}, C_{qg}, and C_{tg}, as shown in Figs. 24 and 25. As such, larger parasitic capacitor currents are traded for shorter paths over which that current flows. The resulting per-phase and per-pole common mode equivalent circuits using both a CM filter and shielded transformer are shown in Figure 4-24 and Figure 4-25, respectively.
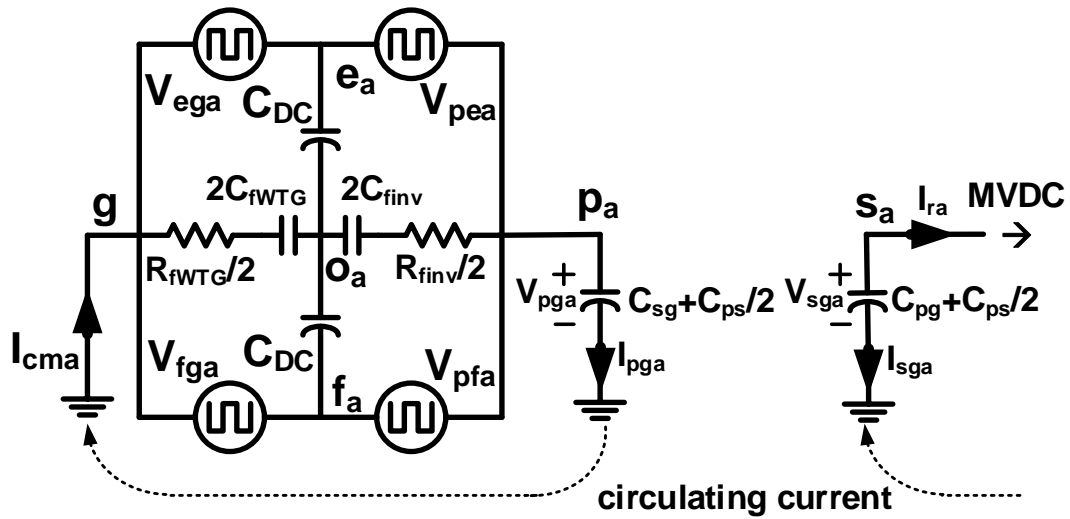
Figure 4-24: Phase "a" CM equivalent circuit with filter and shielding.
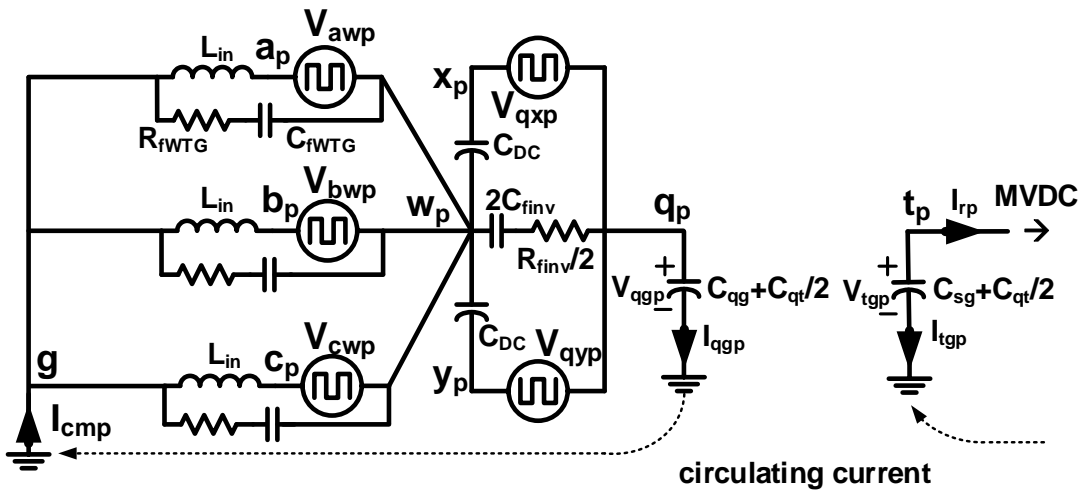
Figure 4-25: Pole "p" CM equivalent circuit with filter and shielding.

Both per-phase and per-pole simulations using a CM filter and shielded transformer yield the results summarized in Tables 4-5 and 4-6. Addition of a filter and transformer shield to the per-phase approach dramatically reduces the WTG neutral current I_{cm} by 15 times compared to the unfiltered and unshielded case, observed by

comparing Figs. 14 and 26. Addition of CM filter and shielding to the per-pole approach also yields reduced primary-to-ground currents, and I_{cm} is reduced by nearly 3 times, as observed by comparing Figs. 21 and 27. In both interfaces the MVDC grid return current I_{return} is mostly unchanged.
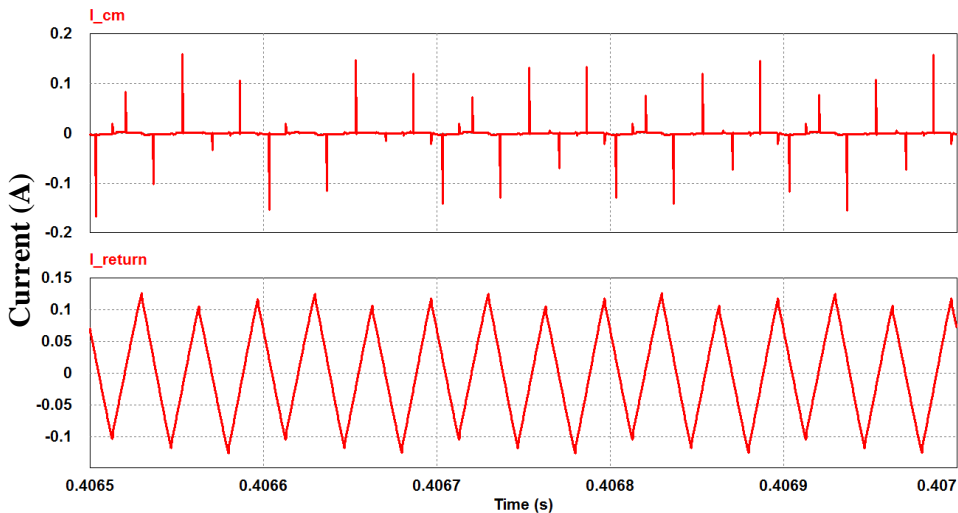
Figure 4-26: Per-phase I_{cm} and I_{return} with CM filter and HFT shield.
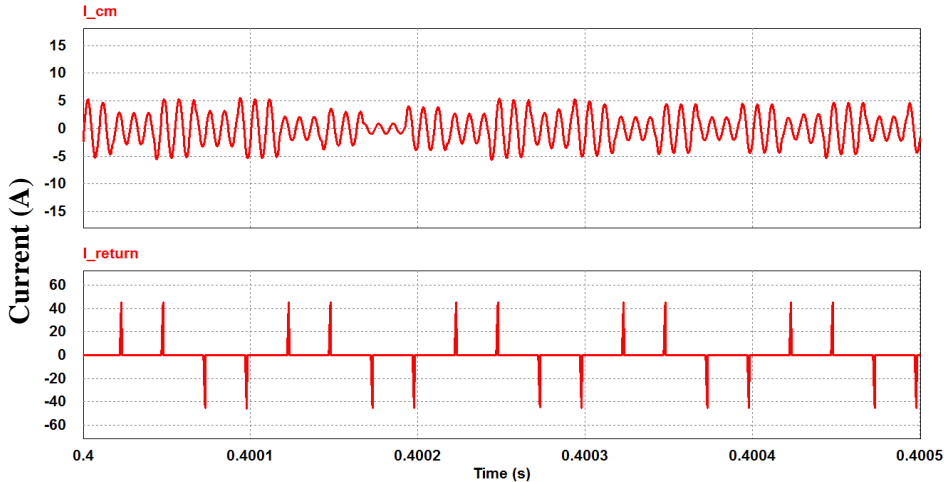
Figure 4-27: Per-pole I_{cm} and I_{return} with CM filter and HFT shield.

Table 4-5: Shielded & filtered per-phase voltages and currents

V_{pga}	4.98 V_{dc}	I_{pga}	6.26 mA$_{rms}$	I_{cm}	12.48 mA$_{rms}$
V_{sga}	19.95 kV$_{dc}$	I_{sga}	3.66 A$_{rms}$	I_{return}	67.26 mA$_{rms}$
V_{pgb}	-0.33 V_{dc}	I_{pgb}	7.51 mA$_{rms}$		
V_{sgb}	-69.06 V_{dc}	I_{sgb}	3.67 A$_{rms}$		
V_{pgc}	-8.26 V_{dc}	I_{pgc}	7.60 mA$_{rms}$		
V_{sgc}	-20.02 kV$_{dc}$	I_{sgc}	3.67$_{rms}$		

Table 4-6: Shielded & filtered per-pole voltages and currents

V_{qgp}	-5.07 V_{dc}	I_{qgp}	1.61 A$_{rms}$	I_{cm}	2.70 A$_{rms}$
V_{tgp}	14.99 kV$_{dc}$	I_{tgp}	4.79 A$_{rms}$	I_{return}	6.76 A$_{rms}$
V_{qgn}	-10.70 V_{dc}	I_{qgn}	1.61 A$_{rms}$		
V_{tgn}	-14.99 kV$_{dc}$	I_{tgn}	4.78 A$_{rms}$		

4.6 Conclusions

This work shows that use of a per-pole interface architecture for integrating WTGs to an MVDC collection grid leads to lower and more balanced CM voltage stress on isolation transformers. Significant WTG neutral current I_{cm} is observed in both interfaces. A common mode filter and transformer shield are applied as mitigation strategies, and corresponding simulation results show a significant reduction in I_{cm} in both per-phase and per-pole interfaces.

5. A POWER SHARING SCHEME FOR SERIES CONNECTED OFFSHORE WIND TURBINES IN A MEDIUM VOLTAGE DC COLLECTION GRID

This work introduces a new method for connecting offshore wind turbine generators (WTGs) in series when interfacing to a medium voltage DC (MVDC) collection grid. Limiting the series stacking to pairs of WTGs and introducing a power sharing converter (PSC) stage between them allows series connected WTGs to operate at independent power levels in a voltage sourced collection grid. This allows for reduced collection grid losses compared to previously proposed series connected current sourced approaches when operating below nominal power. Simulation results demonstrate system operation during a 1:2 power unbalance between series connected WTGs.

5.1 Introduction

Around the world people are continuing to attain higher standards of living, resulting in a continually growing global demand for energy[86]. To satisfy this demand within the contemporary context of global climate change, numerous countries are now aggressively developing their offshore wind energy resources[3]-[5].

Offshore wind resources are now being developed further out to sea than ever[13]. While Germany's Global Tech I farm, currently entering service approximately 100 km from shore[57], is one of the most distant, there are plans for wind farms to be constructed nearly twice that distance from shore[87]. Due to their large distance from shore, many of these modern wind farms rely on offshore HVDC stations to transmit their energy to shore[16].

Additionally, the ≥5 MW WTGs used in modern offshore farms require nearly 1 km of inter-turbine spacing[17], and 10 MW WTGs currently in development [15] may require >1 km of inter-turbine spacing.

Due to the large inter-turbine spacing and presence of an offshore HVDC converter, many researchers are now investigating MVDC collection grids for aggregating energy within the farm, including converter architectures for interfacing WTGs to such and MVDC grid[21]-[29],[58]-[61]. As part of this research thrust there has been significant work in the area of series connected WTGs[88]-[95]. However, these series-connected approaches require many WTGs to share the same DC current. This requires each WTG to modulate its DC output voltage to inject power into the current sourced DC line running through it, similar to a classic line-commutated HVDC converter. This is not desirable as collection grid conduction losses are constant, even when little power is being generated. A power sharing strategy similar to [74],[96]-[98] can be introduced to allow series connected WTGs to operate at independent power levels without modulating output voltage as required in a traditional series connected architecture.

5.2 Proposed Approach

This work proposes the WTG-to-MVDC grid connection shown in Figure 5-1c. Compared to the traditional connections of [21]-[29],[58]-[61],[88]-[95] illustrated by Figs. 1a and 1b, the proposed approach has the following advantages:

1) Reduced voltage stress at individual WTG converters.

2) Lower voltage step-up required from WTG to MVDC collection grid due to series connected WTGs.

3) PSC stage allows series connected WTGs to operate at independent power levels.

4) Isolated DC/DC for each series pair eliminates need to balance MVDC voltage among many WTGs.

5) Reduced collection grid losses when operating <100% power compared to traditional series connection.
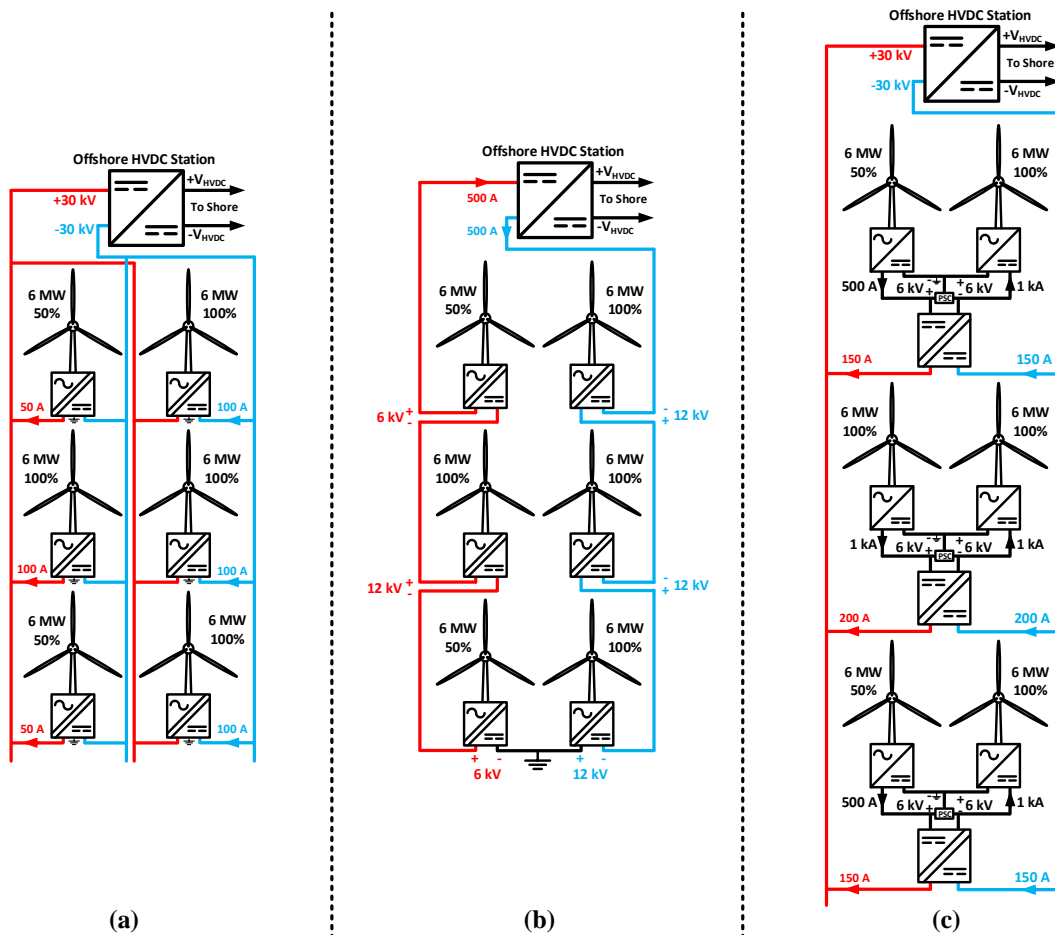
Figure 5-1: Farm with six 6 MW WTGs using (a) parallel connection (b) series connection (c) proposed connection; case (b) is current sourced.

Observing Figure 5-1c the proposed approach utilizes a PSC stage to allow two series connected WTGs to source different currents, and hence different amounts of power, while providing a higher pole-to-pole voltage to the input of the isolated DC/DC converter. PSC operation with the top two series connected WTGs from Figure 5-1c is shown in Figure 5-2.
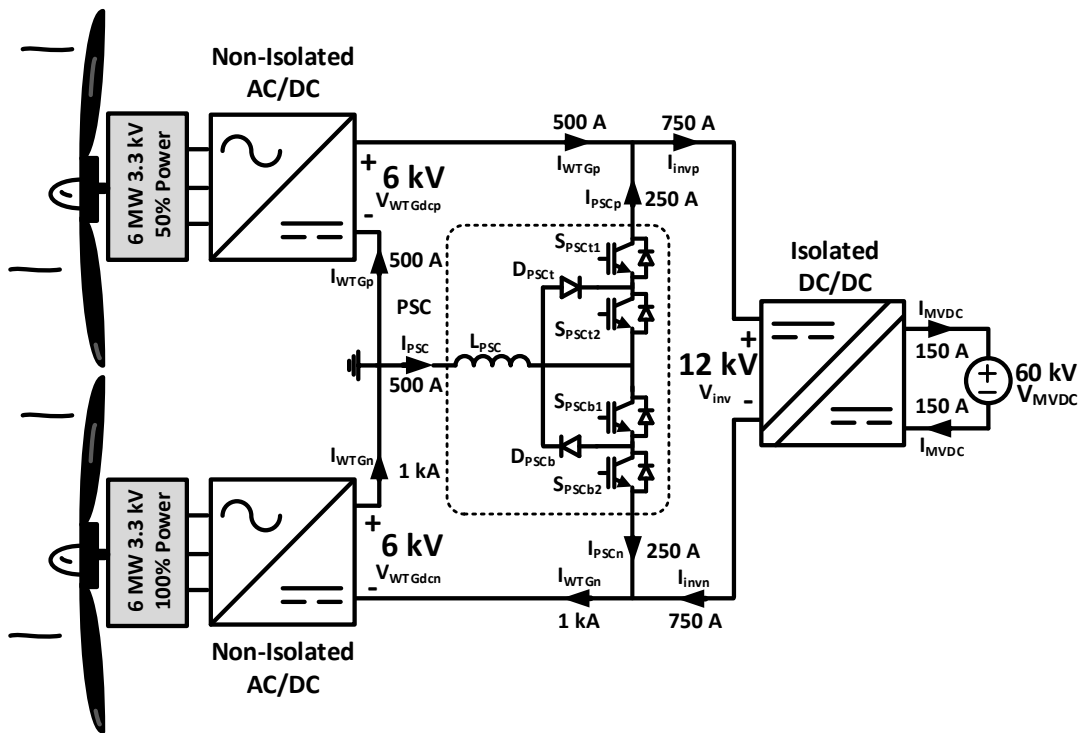
Figure 5-2: Details of power sharing converter.

In steady-state both switches maintain 50% duty cycle, regardless of the state of power unbalance between the WTGs, as zero average voltage must appear across L_{PSC} in steady state. When the state of unbalance changes, the switches temporarily increase or decrease their duty cycles to adjust the current in L_{PSC}. The PSC is important as

individual WTG output powers can vary greatly over a relatively small range of wind speed since WTG power scales with the cube of wind speed[77]. Each WTG of the series connected pair from Figure 5-2 is shown in detail in Figure 5-3. The AC/DC stage provides input current shaping capability for power factor correction, and the inverter stage of the isolated DC/DC features zero-current switching at the resonant frequency of L_{res} and C_{res}, which is 10 kHz. Note that the currents indicated in Figs 1, 2, and 3 are DC, and other components may exist, especially at the DC link due to sinusoidal current at the WTG terminals.
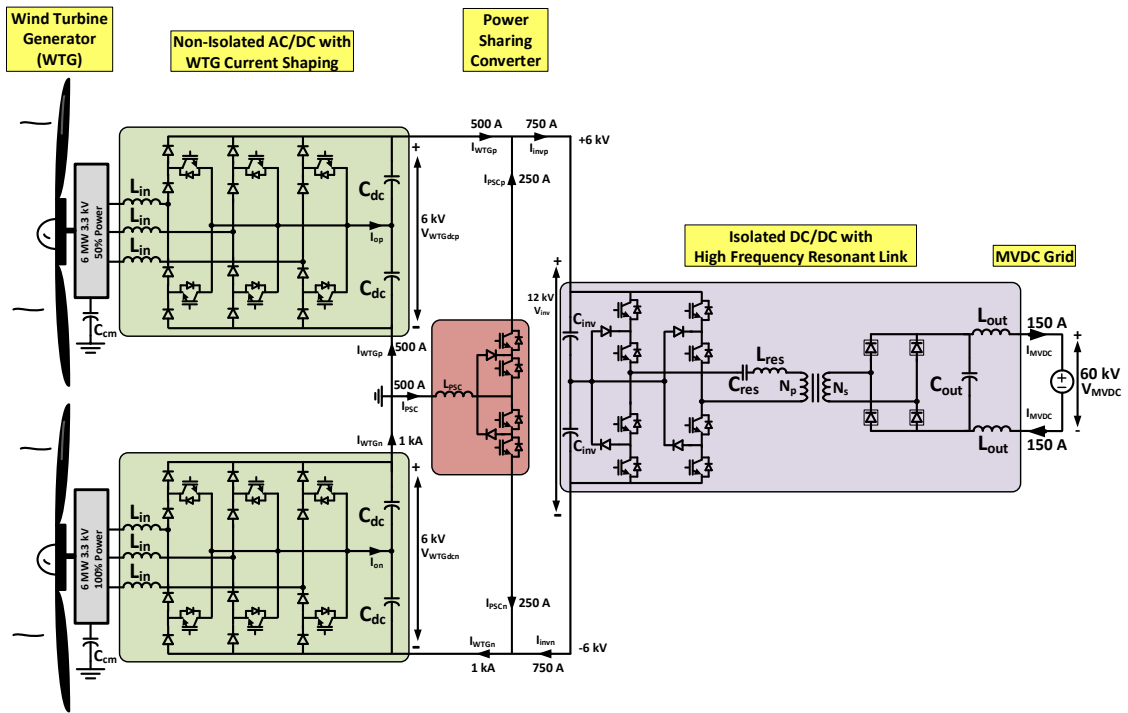
Figure 5-3: Detail of series connected WTG pair. WTG neutral is ungrounded, hence C_{cm} is included. Boxed devices are multiple series devices.

5.3 Simulations Results

For simulation purposes all inductors were considered to have an ωL:R ratio of 200:1. In addition, capacitor ESRs were accounted for by introducing a series resistor across which 0.1% of each capacitor voltage was dropped. IGBT and diode on-state voltages of 3.1 V [68] and 1.7 V [69], respectively, were included. Results of simulating the unbalanced WTG power case described by Figs. 1-3 are summarized in Figs. 4-7. C_{cm} was 100 nF[83],[84].

A 6 MW permanent magnet synchronous generator (PMSG) having a nominal terminal voltage of 3.3 kV$_{LL}$ and nominal frequency of 60 Hz is assumed. According to [77] the WTG generator voltage and frequency scale linearly with wind speed for the PMSG assumed in this approach, meaning WTG current must scale with the square of wind speed for power to scale with the cube of wind speed. As such, a wind speed of 79.4% of nominal is required for operation at only 50% power. The WTG voltage and frequency is also 79.4% of nominal at 50% power, while the current is 63% of nominal. The current of the 50% power turbine is shown in the top plot of Figure 5-4. Both DC link voltages are fixed at 6 kV, while DC link current is pulsating with average values of 500 A and 1 kA, as shown in Figure 5-5. The PSC is able to redirect the difference in WTG current through L$_{PSC}$ and on to the isolated DC/DC stage, shown in Figure 5-6. In Figure 5-7 the DC/DC stage converts pulsating input current to DC current for the MVDC grid
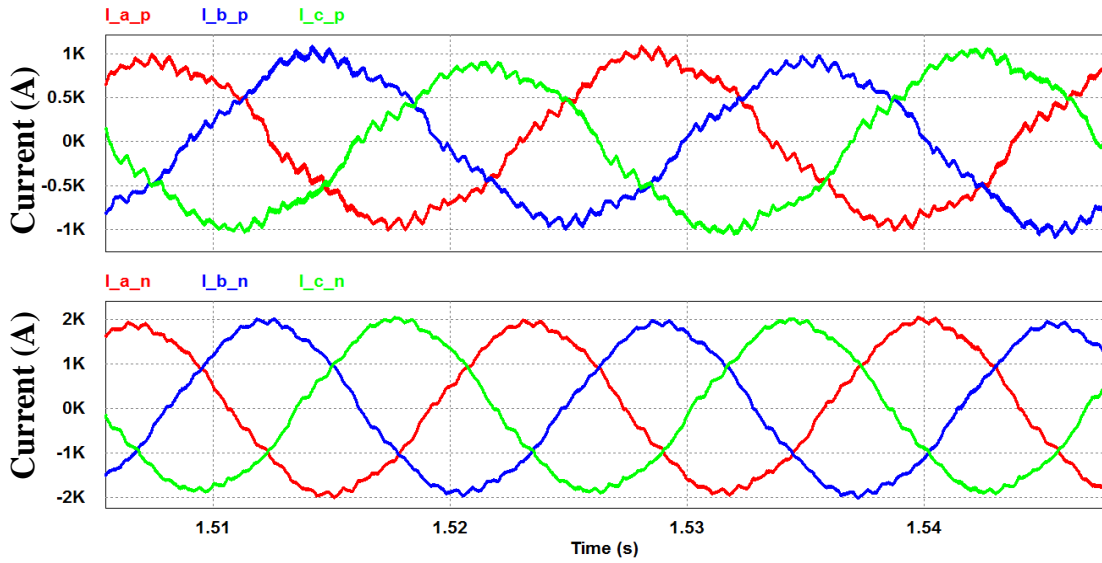
Figure 5-4: Generator currents; note pole "p" generator currents (top) are much less than pole "n" generator currents (bottom) since it is operating at 50% power. Also note pole "p" generator currents are approximately 48 Hz, or 79.4% of nominal frequency.
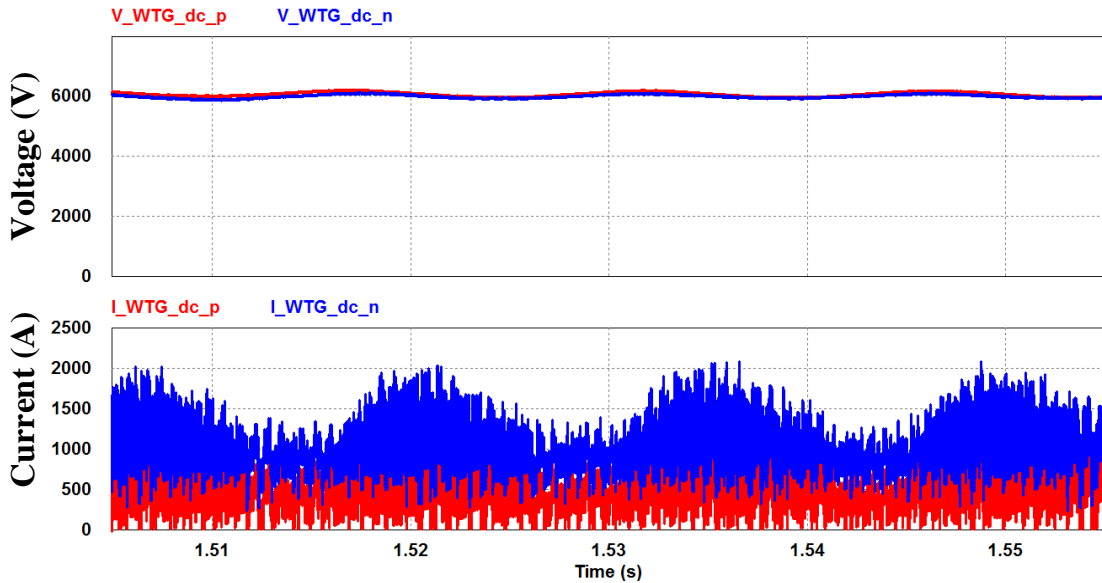
Figure 5-5: Rectifier output DC link voltages (top) and currents (bottom). Average value of pole "p" DC link current is approximately 500 A, while average of pole "n" current is approximately 1 kA. 3 MW are sourced by pole "p" WTG and 6 MW are source by pole "n" WTG.
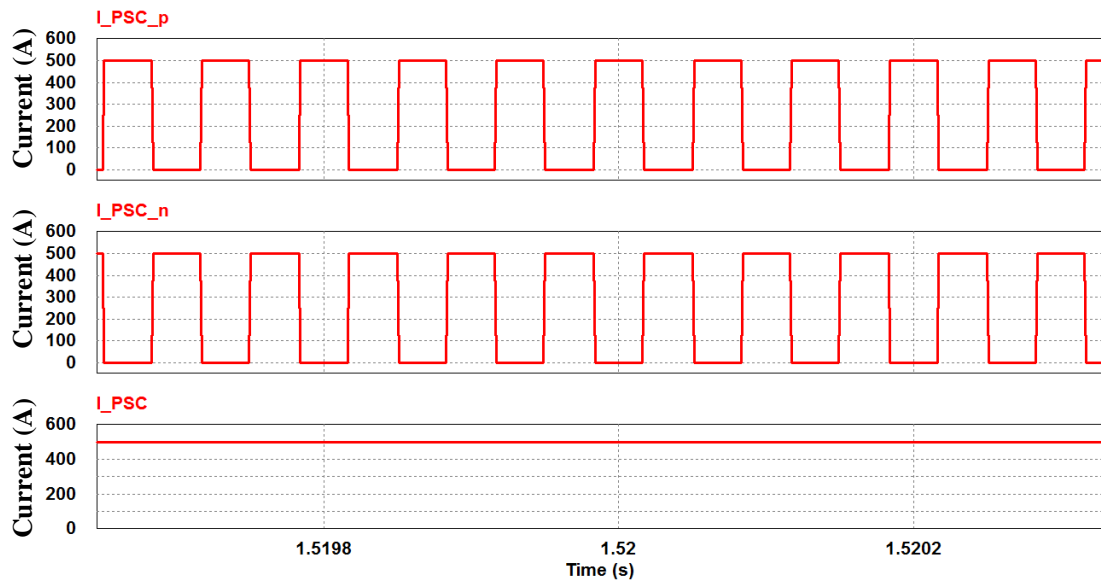
Figure 5-6: Current in pole "p" PSC switch (top), pole "n" PSC switch (middle), and PSC inductor (bottom). Steady state duty cycle is 50%, therefore average current is each switch is half I_{PSC}. I_{PSC} is difference between average of "p" and "n" DC link currents from Figure 5-5.
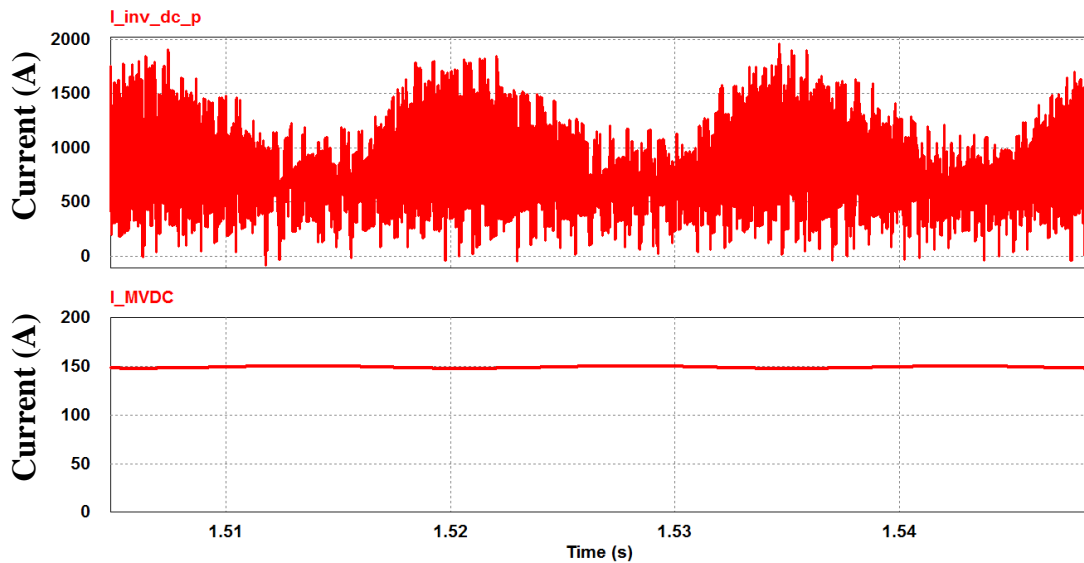
Figure 5-7: Current into isolated DC/DC (top) and current injected into MVDC grid (bottom). Average value of Iinv_dc_p is 750 A. MVDC grid voltage is fixed by HVDC converter station at 60 kV pole-to-pole. Therefore, 9 MW total are injected to MVDC grid.

5.4 Conclusion

This work introduces a new method for connecting offshore WTGs in series when interfacing to an MVDC collection grid. Limiting the series stacking to pairs of WTGs and introducing a PSC stage between them allows series connected WTGs to operate at independent power levels in a voltage sourced collection grid. Detailed simulation results demonstrate system operation in a 1:2 power unbalance between series connected WTGs, as well as near-sinusoidal WTG current shaped by the input AC/DC stage, stiff DC link voltages, and stiff output current to MVDC grid

6. SUMMARY

6.1 Conclusions

This work has presented two novel power electronic interfaces suitable for integrating state-of-the-art offshore wind turbine generators (WTGs) with medium voltage DC (MVDC) collection grids.

Simulation results demonstrate the desired high displacement power factor (DPF) magnitude of >0.95 and >0.96 at the input of the per-phase and per-pole interfaces, respectively, as well as <1 second output settling in response to a 75% reduction in available power and desired zero-current switching (ZCS) in the high frequency inverter stage.

Hardware results from a 250 V_{dc}, 700 W lab-scale prototype validate input rectifier voltage boost characteristic with >0.95 DPF magnitude. A practical capacitor-voltage-balance switching scheme is also implemented in the hardare control loop in addition to DC link voltage and input current shaping control.

Common mode voltage stress and circulating ground currents due to power electronic switching and HFT parasitic capacitances are also investigated through the reduction of each interface to a common mode equivalent circuit. The results of this investigation show that common mode voltage stress is far more balanced on the HFTs in the per-pole interface, and secondary winding common mode stress is dominated by the MVDC voltage. Circulating current reaches a maximum 105.3 A_{rms} and 20.2 A_{rms} at

the WTG neutral connection in the per-phase and per-pole interfaces, respectively, which provides guidance for practical design of ground current relay protection schemes.

The effect of unbalanced power injected from two series connected WTGs is also investigated via analysis and simulation. In the series case an additional power sharing converter (PSC) stage must be added between the series connected WTGs and the MVDC grid. This PSC must process any differential output current between the WTGs. WTG unbalance does not significantly affect the per-pole interface. The high frequency resonant AC link in this approach is shared between both series connected WTGs such that it can take advantage of the higher pole-to-pole DC link voltage to interface to a higher voltage MVDC grid..

This research suggests that both proposed power electronic interfaces are suitable for integrating state-of-the-art offshore WTGs with MVDC collection grids. The per-pole interface may be slightly more desirable for most offshore installations due to its improved common mode and WTG unbalance performance; however, the per-phase interface may be more attractive for installations with >6 MW WTGs due to its lower processed power per HFT.

With this technology countries that have already embraced offshore wind can move forward with development of their best wind resources, and countries like the US can begin to think about offshore wind as a viable energy resource with fewer political and environmental barriers. From the environmental perspective, a modern offshore wind turbine can power about 3,500 homes and eliminates about 7,200 tons of CO_2 emissions every year, which means that modest growth of 10% in offshore wind energy

due to the application of this technology could prevent the equivalent of 31,500 railroad cars worth of CO_2 from being released.

6.2 Future Work

There are three key areas that are suitable areas of future work with regard to this research. Investigation into these new areas may provide more insight into how to best operate entire wind farms using MVDC collection grids as proposed in this work.

The first area for future work is investigation of additional levels of series connection and power sharing among groups of WTGs. There are two approaches that could be used to stack two WTG series pairs (4 WTGs total) in series to achieve higher DC voltage yet allow each WTG to operate at an independent power level. This could be achieved by placing a second power sharing converter that across the entire DC link formed by 4 WTGs, or by placing the additional PSC between the two pairs of WTGs, reducing the DC voltage experienced by this second PSC. More work is needed to determine the best approach.

The second key area of future work is to carry out a more detailed trade study of overall converter mass and volume. This will require detailed models of devices and passive components, a deep understanding of converter manufacturing requirements, and communication with application engineers in many areas related to the offshore WTG power converter industry. However, building a more complete understanding of how converter losses, transformer frequency, power ratings, and voltage affect the converter mass and volume will allow the proposed power electronic interfaces to more readily be designed for manufacturing.

Finally, deployment of the proposed interface among all WTGs in large offshore wind farm will require an expanded control methodology to accommodate many turbines connected to the same MVDC collection grid over a wide area. This control scheme must account for the effect of voltage rise from the fixed MVDC voltage at converter station due to current in the MVDC collection grid. The effective MVDC voltage experience by each WTG will be a function of distance from offshore converter station (or nearest point of fixed MVDC voltage) as well as power inject by the WTG itself, and all other WTGs between it and the converter station. Perhaps a communication scheme will be required among all the WTG power converters to coordinate current injection from each WTG as MVDC voltage fluctuates at each WTG.

Should these areas of future work be investigated and provide the required results, it may allow the power electronic interfaces proposed in this work to be manufactured and deployed with the next generation of offshore wind turbines in farms with MVDC collection grids.

REFERENCES

[1]   Chefurka, P., "The Looming Energy Shortfall, Can Wind Fill the Gap?",
        December   2008.   [Online].   Available:
        http://www.paulchefurka.ca/EnergyGap.html

[2]   "International Energy Outlook 2013", EIA, US Department of Energy,
        September 2013 [Online]. Available: http://www.eia.gov/forecasts/ieo/world.cfm

[3]   Li Rennian; Wang Xin, "Status and challenges for offshore wind energy,"
        Materials for Renewable Energy & Environment (ICMREE), 2011 International
        Conference on, pp. 601-605, 20-22 May 2011

[4]   Higgins, P.; Foley, A.M., "Review of offshore wind power development in the
        United Kingdom," Environment and Electrical Engineering (EEEIC), 2013 12th
        International Conference on, pp. 589-593, 5-8 May 2013

[5]   Kling, W.L.; Gibescu, M.; Ummels, B.C.; Hendriks, R.L., "Implementation of
        wind power in the Dutch power system," Power and Energy Society General
        Meeting - Conversion and Delivery of Electrical Energy in the 21st Century,
        2008 IEEE, Proceedings of, pp. 1-6, 20-24 July 2008

[6]   "Project Details for Global Tech I", 4C Offshore, March 2015. [Online].
        Available: www.4coffshore.com/windfarms/global-tech-i-germany-de09.html

[7]   "EIA Projects U.S. Non-Hydro Renewable Power Generation Increases, Led by Wind and Biomass", US Energy Information Administration, December 2012. [Online]. Available: http://www.eia.gov/todayinenergy/detail.cfm?id=5170

[8]   "World-Wide Wind Energy Resource Distribution Estimates", US Department of Energy, December 1980. [Online]. Available: http://www.geni.org/globalenergy/library/renewable-energy-resources/wind.shtml

[9]   "Global Cumulative Offshore Wind Capacity in 2014", Global Wind Energy Council, March 2015. [Online]. Available: http://www.gwec.net/global-figures/global-offshore/

[10]   Apt, J.; Curtwright, A., "The Character of Power Output from Utility-Scale Photovoltaic Systems", Progress in Photovoltaics: Research and Applications, vol. 16, no. 3, pp. 241-247, 2008

[11]   "Real Time Wind & Weather Report Altamont 2015-04-18", Windfinder, April 2015. [Online]. Available: http://www.windfinder.com/report/altamont

[12]   "Real Time Wind & Weather Report Feuerschiff Dt. Bucht 2015-04-22", Windfinder, April 2015. [Online]. Available: http://www.windfinder.com/report/feuerschiff_dtbucht

[13]   "Upwind: design limits and solutions for very large wind turbines," European Wind Energy Association, March 2011 [Online]. Available:

http://www.ewea.org/fileadmin/files/library/publications/reports/UpWind_Report.pdf

[14] "Global Offshore Wind Farms Database – Global Map", 4C Offshore, March 2015. [Online]. Available: http://www.4coffshore.com/offshorewind/

[15] "Sea Titan 10 MW Wind Turbine: Maximum Power per Tower for Offshore Environment", Windtec Solutions, American Superconductor Corp., May 2012 [Online]. Available: http://www.amsc.com/documents/seatitan-10-mw-wind-turbine-data-sheet/

[16] Das, D.; Pan, J.; Bala, S., "HVDC Light for large offshore wind farm integration," Power Electronics and Machines in Wind Applications (PEMWA), 2012 IEEE, Proceedings of, pp. 1-7, 16-18 July 2012

[17] A. Westerhellweg, B. Cañadillas, F. Kinder, T. Neumann,"Detailed Analysis of Offshore Wakes Based on Two Years Data of alpha ventus and Comparison with CFD Simulations", DEWI Wilhelmshaven, DEWI Magazine, No. 42, pp. 65-70, Feb. 2013.

[18] "Worldwide offshore expert: offshore wind from Germany for the energy transition," Siemens AG, August 2013. [Online]. Available: http://www.siemens.com/press/photo/PN201311-09e

[19] "The final step: jacking up," Siemens AG, April 2014. [Online]. Available: http://www.siemens.com/press/photo/soew201402-10e

[20]   Daniel, M.T.; Krishnamoorthy, H.S.; Enjeti, P.N., "A New Wind Turbine Interface to MVdc Collection Grid With High-Frequency Isolation and Input Current Shaping," in Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 3, no. 4, pp. 967-976, Dec. 2015

[21]   Chen, W.; Huang, A. Q.; Li, C.; Wang, G.; Gu, W., "Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems," Power Electronics, IEEE Transactions on, vol. 28, no. 4, pp. 2014-2023, Apr. 2013

[22]   Parastar, A.; Jul-Ki Seok, "High power step-up modular resonant DC/DC converter for offshore wind energy systems," Energy Conversion Congress and Exposition (ECCE), 2014 IEEE, Proceedings of, pp. 3341-3348, 14-18 Sept. 2014

[23]   Jovcic, D., "Step-up DC-DC converter for megawatt size applications," Power Electronics, IET , vol. 2, no. 6, pp. 675-685, Nov. 2009

[24]   Lam, J.; Jain, P.K., "A high efficient medium voltage step-up DC/DC converter with zero voltage switching (ZVS) and low voltage stress for offshore wind energy systems," Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on, Proceedings of, pp.1-10, 26-28 Aug. 2014

[25]   Prasai, A.; Jung-Sik Yim; Divan, D.; Bendre, A.; Seung-Ki Sul, "A New Architecture for Offshore Wind Farms," Power Electronics, IEEE Transactions on , vol. 23, no. 3, pp. 1198-1204, May 2008

[26]   Steimer, P.K.; Apeldoorn, O., "Medium voltage power conversion technology for efficient windpark power collection grids," Power Electronics for Distributed Generation Systems (PEDG), 2010 2nd IEEE International Symposium on, Proceedings of, pp.12-18, 16-18 June 2010

[27]   Meyer, C.; Hoing, M.; Peterson, A.; De Doncker, R.W., "Control and Design of DC Grids for Offshore Wind Farms," Industry Applications, IEEE Transactions on, vol. 43, no. 6, pp. 1475-1482, Nov. 2007

[28]   Carmeli, M.S.; Castelli-Dezza, F.; Marchegiani, G.; Mauri, M.; Rosati, D., "Design and analysis of a Medium Voltage DC wind farm with a transformer-less wind turbine generator," Electrical Machines (ICEM), 2010 XIX International Conference on, Proceedings of, pp.1-6, 6-8 Sept. 2010

[29]   Ho-Sung Kim; Ju-Won Baek; Myung-Hyu Ryu; Jong-Hyun Kim; Jee-Hoon Jung, "The High-Efficiency Isolated AC–DC Converter Using the Three-Phase Interleaved LLC Resonant Converter Employing the Y-Connected Rectifier," Power Electronics, IEEE Transactions on, vol. 29, no. 8, pp. 4017-4028, Aug. 2014

[30] Kolar, J.W.; Friedli, T.; Krismer, F.; Looser, A.; Schweizer, M.; Friedemann, R.A.; Steimer, P.K.; Bevirt, J.B., "Conceptualization and Multiobjective Optimization of the Electric System of an Airborne Wind Turbine," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 2, pp. 73-103, June 2013

[31] Blaabjerg, F.; Ke Ma, "Future on Power Electronics for Wind Turbine Systems," Emerging and Selected Topics in Power Electronics, IEEE Journal of , vol. 1, no. 3, pp. 139-152, Sept. 2013

[32] Polinder, H.; Ferreira, J.A.; Jensen, B.B.; Abrahamsen, A.B.; Atallah, K.; McMahon, R.A., "Trends in Wind Turbine Generator Systems," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 3, pp. 174-185, Sept. 2013

[33] Yue Zhao; Chun Wei; Zhe Zhang; Wei Qiao, "A Review on Position/Speed Sensorless Control for Permanent-Magnet Synchronous Machine-Based Wind Energy Conversion Systems," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 4, pp. 203-216, Dec. 2013

[34] Lijun He; Yongdong Li; Harley, R.G., "Adaptive Multi-Mode Power Control of a Direct-Drive PM Wind Generation System in a Microgrid," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 4, pp. 217-225, Dec. 2013

[35]   Balogun, A.; Ojo, O.; Okafor, F., "Decoupled Direct Control of Natural and Power Variables of Doubly Fed Induction Generator for Extended Wind Speed Range Using Feedback Linearization," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 4, pp.226-237, Dec. 2013

[36]   Mesemanolis, A.; Mademlis, C.; Kioskeridis, I., "Optimal Efficiency Control Strategy in Wind Energy Conversion System With Induction Generator," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 4, pp. 238-246, Dec. 2013

[37]   Rodrigues, S.; Pinto, R.T.; Bauer, P.; Pierik, J., "Optimal Power Flow Control of VSC-Based Multiterminal DC Network for Offshore Wind Integration in the North Sea," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 4, pp. 260-268, Dec. 2013

[38]   Girsang, I.P.; Dhupia, J.S.; Muljadi, E.; Singh, M.; Jonkman, J., "Modeling and Control to Mitigate Resonant Load in Variable-Speed Wind Turbine Drivetrain," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 4, pp. 277-286, Dec. 2013

[39]   Mandic, G.; Nasiri, A.; Ghotbi, E.; Muljadi, E., "Lithium-Ion Capacitor Energy Storage Integrated With Variable Speed Wind Turbines for Power Smoothing," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 4, pp. 287-295, Dec. 2013

[40]   Junbiao Han; Solanki, S.K.; Solanki, J., "Coordinated Predictive Control of a Wind/Battery Microgrid System," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, no. 4, pp. 296-305, Dec. 2013

[41]   Yaramasu, V.; Bin Wu; Rivera, M.; Rodriguez, J., "A New Power Conversion System for Megawatt PMSG Wind Turbines Using Four-Level Converters and a Simple Control Scheme Based on Two-Step Model Predictive Strategy—Part I: Modeling and Theoretical Analysis," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 2, no. 1, pp. 3-13, March 2014

[42]   Yaramasu, V.; Bin Wu; Rivera, M.; Rodriguez, J., "A New Power Conversion System for Megawatt PMSG Wind Turbines Using Four-Level Converters and a Simple Control Scheme Based on Two-Step Model Predictive Strategy—Part II: Simulation and Experimental Analysis," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 2, no. 1, pp. 14-25, March 2014

[43]   Freire, N.M.A.; Cardoso, A.J.M., "Fault-Tolerant PMSG Drive With Reduced DC-Link Ratings for Wind Turbine Applications," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 2, no. 1, pp. 26-34, March 2014

[44]   Kuschke, M.; Strunz, K., "Energy-Efficient Dynamic Drive Control for Wind Power Conversion With PMSG: Modeling and Application of Transfer Function

Analysis," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 2, no. 1, pp. 35-46, March 2014

[45]   Fujin Deng; Zhe Chen, "Control of Improved Full-Bridge Three-Level DC/DC Converter for Wind Turbines in a DC Grid," Power Electronics, IEEE Transactions on, vol. 28, no. 1, pp. 314-324, Jan. 2013

[46]   Chen, W.; Huang, A. Q.; Li, C.; Wang, G.; Gu, W., "Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems," Power Electronics, IEEE Transactions on, vol. 28, no. 4, pp. 2014-2023, April 2013

[47]   Jun Yao; Hui Li; Zhe Chen; Xianfeng Xia; Xiyin Chen; Qing Li; Yong Liao, "Enhanced Control of a DFIG-Based Wind-Power Generation System With Series Grid-Side Converter Under Unbalanced Grid Voltage Conditions," Power Electronics, IEEE Transactions on, vol. 28, no. 7, pp. 3167-3181, July 2013

[48]   Yaramasu, V.; Bin Wu; Jin Chen, "Model-Predictive Control of Grid-Tied Four-Level Diode-Clamped Inverters for High-Power Wind Energy Conversion Systems," Power Electronics, IEEE Transactions on, vol. 29, no. 6, pp. 2861-2873, June 2014

[49]   Yongchang Zhang; Jiefeng Hu; Jianguo Zhu, "Three-Vectors-Based Predictive Direct Power Control of the Doubly Fed Induction Generator for Wind Energy

Applications," Power Electronics, IEEE Transactions on, vol. 29, no. 7, pp. 3485-3500, July 2014

[50] Krishnamoorthy, H.S.; Rana, D.; Garg, P.; Enjeti, P.N.; Pitel, I.J., "Wind Turbine Generator–Battery Energy Storage Utility Interface Converter Topology With Medium-Frequency Transformer Link," Power Electronics, IEEE Transactions on, vol. 29, no. 8, pp. 4146-4155, Aug. 2014

[51] Yaramasu, V.; Bin Wu, "Predictive Control of a Three-Level Boost Converter and an NPC Inverter for High-Power PMSG-Based Medium Voltage Wind Energy Conversion Systems," Power Electronics, IEEE Transactions on, vol. 29, no. 10, pp. 5308-5322, Oct. 2014

[52] Feifei Bu; Yuwen Hu; Wenxin Huang; Shenglun Zhuang; Kai Shi, "Wide-Speed-Range-Operation Dual Stator-Winding Induction Generator DC Generating System for Wind Power Applications," Power Electronics, IEEE Transactions on, vol. 30, no. 2, pp. 561-573, Feb. 2015

[53] Ke Ma; Liserre, M.; Blaabjerg, F.; Kerekes, T., "Thermal Loading and Lifetime Estimation for Power Device Considering Mission Profiles in Wind Power Converter," Power Electronics, IEEE Transactions on, vol. 30, no. 2, pp. 590-602, Feb. 2015

[54]   Parastar, A.; Jul-Ki Seok, "High-Gain Resonant Switched-Capacitor Cell-Based DC/DC Converter for Offshore Wind Energy Systems," Power Electronics, IEEE Transactions on, vol. 30, no. 2, pp. 644-656, Feb. 2015

[55]   Jelani, N.; Molinas, M., "Asymmetrical Fault Ride Through as Ancillary Service by Constant Power Loads in Grid-Connected Wind Farm," Power Electronics, IEEE Transactions on, vol. 30, no. 3, pp. 1704-1713, March 2015

[56]   Peng Li; Yong-Duan Song; Dan-Yong Li; Wen-Chuan Cai; Kai Zhang, "Control and Monitoring for Grid-Friendly Wind Turbines: Research Overview and Suggested Approach," Power Electronics, IEEE Transactions on, vol. 30, no. 4, pp. 1979-1986, April 2015

[57]   "Pioneering performance in the North Sea: The offshore wind farm Global Tech I", Global Tech I Offshore Wind GmbH, December 2012, [Online]. Available:http://www.globaltechone.de/en/about/

[58]   Jun Li; Bhattacharya, S.; Huang, A.Q., "A New Nine-Level Active NPC (ANPC) Converter for Grid Connection of Large Wind Turbines for Distributed Generation," Power Electronics, IEEE Transactions on, vol. 26, no. 3, pp. 961-972, March 2011

[59]   Lam, J.; Jain, P.K., "Single-stage three-phase AC/DC step-up medium voltage resonant converter for offshore wind power systems," Energy Conversion

Congress and Exposition (ECCE), 2014 IEEE, Proceedings of, pp. 4612-4619, 14-18 Sept. 2014

[60] Fujin Deng; Zhe Chen, "Control of Improved Full-Bridge Three-Level DC/DC Converter for Wind Turbines in a DC Grid," Power Electronics, IEEE Transactions on, vol. 28, no. 1, pp. 314-324, Jan. 2013

[61] Daniel, M.T.; Krishnamoorthy, H.S.; Enjeti, P.N., "A new wind turbine interface to MVDC grid with high frequency isolation and input current shaping,"Industrial Electronics Society, IECON 2014 - 40th Annual Conference of the IEEE, Proceedings of, pp. 1924-1930, Oct. 29 2014-Nov. 1 2014

[62] Daniel, Michael T.; Krishnamoorthy, Harish S.; Enjeti, Prasad N., "An improved offshore wind turbine to MVDC grid interface using high frequency resonant isolation and input power factor control,"Power and Energy Conference at Illinois (PECI), 2015 IEEE, Proceeedings of, pp. 1-8, 20-21 Feb. 2015

[63] Trivedi, M.; Shenai, K., "Internal dynamics of IGBT under zero-voltage and zero-current switching conditions," Electron Devices, IEEE Transactions on, vol. 46, no. 6, pp. 1274-1282, Jun 1999

[64] Reigstad, T., "Direct Driven Permanent Magnet Synchronous Generators with Diode Rectifiers for Use in Offshore Wind Turnbines", NTNU, June 2007 [Online]. Available: http://www.diva-portal.org/smash/get/diva2:347491/FULLTEXT01.pdf

[65] Rucker, J.E.; Kirtley, J.L.; McCoy, T.J., "Design and analysis of a permanent magnet generator for naval applications," Electric Ship Technologies Symposium, 2005 IEEE, Proceedings of, pp. 451-458, 25-27 July 2005

[66] Yifan Zhao; Yue Li; Lipo, T.A., "Force commutated three level boost type rectifier," Industry Applications, IEEE Transactions on, vol. 31, no. 1, pp.155-161, Jan./Feb. 1995

[67] Hart, D., "The Series Resonant Inverter", *Power Electronics*, McGraw-Hill, New York, 2011, pp. 404-405.

[68] "5SNA 1500E3303005 HiPak IGBT Module", ABB Switzerland Ltd., Feb 2014 [Online]. Available: http://www08.abb.com/global/scot/scot256.nsf/veritydisplay/d740233e818310bc 83257ca9002c95b1/$file/5SNA%201500E330305%205SYA%201407-07%2002-2014.pdf

[69] "5SDF 20L4521 Fast Recovery Diode", ABB Switzerland Ltd., September 2014 [Online]. Available: http://www08.abb.com/global/scot/scot256.nsf/veritydisplay/c085c2d712d4b4c2 83257d70002cd749/$file/5SDF%2020L4521_5SYA1186-01%20Sep%2014.pdf

[70] "Simplified Method of Estimating Heat Sink Thermal Resistance Θ_{SA} Forced Convection Applications", Wakefield Solutions Inc., February 2015. [Online]. Available:

https://www.digikey.com/Web%20Export/Supplier%20Content/Wakefield%20_

345/PDF/wakefield-pi-estimating-heatsink-resistance.pdf?redirected=1

[71]   Ruxi Wang; Wang, F.; Rixin Lai; Puqi Ning; Burgos, R.; Boroyevich, D., "Study of Energy Storage Capacitor Reduction for Single Phase PWM Rectifier,"Applied Power Electronics Conference and Exposition (APEC), Twenty-Fourth Annual IEEE, Proceedings of, pp. 1177-1183, 15-19 Feb. 2009

[72]   Kolar, J.W.; Ortiz, G., "Intelligent Solid State Transformers (SSTs) - A Key Building Block of Future Smart Grid Systems", Tutorial at the 19th China Power Supply Society Conference (CPSSC), Shanghai, China, November 18-21, 2011.

[73]   Raju, R., "Silicon Carbide: High Voltage, High Frequency Conversion", NIST High Megawatt Variable Speed Drive Technology Workshop, Apr. 2014.

[74]   Hawke, J.T.; Krishnamoorthy, H.S.; Enjeti, P.N., "A Family of New Multiport Power-Sharing Converter Topologies for Large Grid-Connected Fuel Cells,"Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 2, no. 4, pp. 962-971, Dec. 2014

[75]   "HVDC Light Cables: Submarine and Land Power Cables", ABB, May 2014. [Online].   Available: http://www05.abb.com/global/scot/scot245.nsf/veritydisplay/1591f139098f62e5c 1257154002f9801/$file/hvdc%20light%20power%20cables.pdf

[76] Glover, J.; Sarma, M.; Overbye, T., "Characteristics of Copper Conductors", *Power System Analysis and Design*, Cengage Learning, 2008, pp. 735.

[77] Polinder, H.; Bang, D.; Van Rooij, R. P J O M; McDonald, A.S.; Mueller, M.A., "10 MW Wind Turbine Direct-Drive Generator Design with Pitch or Active Speed Stall Control," Electric Machines & Drives Conference (IEMDC) IEEE International, Proceedings of, pp. 1390-1395, 3-5 May 2007

[78] "BSM 150 GB 60 DLC Techincal Information", Infineon Technologies, AG., October 2014 [Online]. Available: https://www.infineon.com/dgdl/Infineon-BSM150GB60DLC-DS-v01_00-en_de.pdf?fileId=db3a30431ff98815011ffb14c3 4f0010

[79] "IRK.166,.196,.236 Standard Recovery Diodes", International Rectifier, Inc., Mar 2002 [Online]. Available: http://www.irf.com/product-info/datasheets/data/irkd166.pdf

[80] Meyer, C., "Key Components for Future Offshore DC Grids", RWTH Aachen University, December 2007 [Online]. Available: http://www.isea.rwth-aachen.de/dissertations/request/159

[81] "Asymmetric Integrated Gate-Commutated Thyristor 5SH& 42L6500", ABB Switzerland Ltd., December 2012 [Online]. Available: http://www05.abb.com/global/scot/scot256.nsf/veritydisplay/a076cbdcb0d975d3 c12577590035538a/$file/5SHY%2042L6500_5SYA1245-03Dec%2012.pdf

[82]   "RBK8__25XX General Purpose Diode", Powerex Inc., June 2008 [Online].
        Available: http://www.pwrx.com/pwrx/docs/rbk8_25.pdf

[83]   Rendusara, D.A.; Cengelci, E.; Enjeti, P.N.; Stefanovic, Victor R.; Gray, J.W.,
        "Analysis of common mode voltage-"neutral shift" in medium voltage PWM
        adjustable speed drive systems," Power Electronics, IEEE Transactions on, vol.
        15, no. 6, pp. 1124-1133, Nov 2000

[84]   Palma, L.; Harfman Todorovic, M.; Enjeti, P.N., "Analysis of Common-Mode
        Voltage in Utility-Interactive Fuel Cell Power Conditioners,"Industrial
        Electronics, IEEE Transactions on, vol. 56, no. 1, pp. 20-27, Jan. 2009

[85]   Palma, L.; Enjeti, P., "An inverter output filter to mitigate dV/dt effects in PWM
        drive system,"Applied Power Electronics Conference and Exposition (APEC),
        Seventeenth Annual IEEE, Proceedings of, pp. 550-556, Mar. 2002

[86]   "Annual Energy Outlook 2015", EIA, US Department of Energy, September
        2015 [Online]. Available: http://www.eia.gov/forecasts/aeo/

[87]   "Nord-Ost Passat I", 4C Offshore, March 2015, [Online].   Available:
        http://www.4coffshore.com/windfarms/nord-ost-passat-i-germany-de1p.html

[88]   Gang Shi; Zhibing Wang; Miao Zhu; Xu Cai; Liangzhong Yao, "Variable speed
        control of series-connected DC wind turbines based on generalized dynamic
        model,"Renewable Power Generation Conference (RPG), 2nd IET,Proceedings
        of, pp. 1-6, 9-11 Sept. 2013

125

[89]   Takemura, A.; Tatsuta, F.; Yokoyama, H.; Nishikata, S., "Studies on field current control method for constant tip speed ratios of series connected wind turbine generators in a wind farm,"Electrical Machines and Systems (ICEMS), 2012 15th International Conference on, Proceedings of, pp. 1-5, 21-24 Oct. 2012

[90]   Holtsmark, N.; Bahirat, H.J.; Molinas, M.; Mork, B.A.; Hoidalen, H.K., "An All-DC Offshore Wind Farm With Series-Connected Turbines: An Alternative to the Classical Parallel AC Model?," Industrial Electronics, IEEE Transactions on, vol. 60, no. 6, pp. 2420-2428, June 2013

[91]   Nishikata, S.; Tatsuta, F., "Dynamic control of series connected wind turbine generating system," PowerTech, 2011 IEEE Trondheim, Proceedings of, pp.1-6, 19-23 June 2011

[92]   Garces, A.; Barrera-Cardenas, R.; Molinas, M., "Optimal control for an HVDC system with series connected offshore wind turbines,"Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, Proceedings of, pp. 3918-3925, 15-19 Sept. 2013

[93]   Gjerde, S.; Undeland, T.M., "Dynamic performance of the modular series connected converter in a 100 kVdc- transformerless offshore wind turbine,"OCEANS - Bergen, 2013 MTS/IEEE, Proceedings of, pp.1-9, 10-14 June 2013

[94]   Tatsuta, F.; Nishikata, S., "Basic investigations on a wind power plant consisting of series-connected wind turbine generators,"Electrical Machines and Systems (ICEMS), 2014 17th International Conference on, Proceedings of, pp. 1345-1349, 22-25 Oct. 2014

[95]   Veilleux, E.; Lehn, P.W., "Interconnection of Direct-Drive Wind Turbines Using a Series-Connected DC Grid,"Sustainable Energy, IEEE Transactions on, vol. 5, no. 1, pp. 139-147, Jan. 2014

[96]   Krishnamoorthy, H.S.; Essakiappan, S.; Enjeti, P.N.; Balog, R.S.; Ahmed, S., "A new multilevel converter for Megawatt scale solar photovoltaic utility integration,"Applied Power Electronics Conference and Exposition (APEC), Twenty-Seventh Annual IEEE, Proceedings of, pp. 1431-1438, 5-9 Feb. 2012

[97]   McClurg, J.; Pilawa-Podgurski, R.C.N.; Shenoy, P.S., "A series-stacked architecture for high-efficiency data center power delivery,"Energy Conversion Congress and Exposition (ECCE), 2014 IEEE, Proceedings of, pp. 170-177, 14-18 Sept. 2014

[98]   Shenoy, P. S.; Krein, P. T., "Differential Power Processing for DC Systems,"Power Electronics, IEEE Transactions on, vol. 28, no. 4, pp. 1795-1806, April 2013