COMPARATIVE STUDY ON PERFORMANCE AND VARIATION TOLERANCE OF LOW-POWER CIRCUIT

A Thesis

by

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ABSTRACT

The demand for low-power electronic devices is increasing rapidly in current VLSI technology. Instead of conventional CMOS circuit operating at nominal supply voltage, several kinds of circuits are brought about with the goal of reducing power consumption. This research is mainly focused on evaluating performance, power and variation tolerance of near/sub-threshold computing and adiabatic logic circuits. Arithmetic logic units (ALUs) are designed with 15nm FinFET process technologies for these circuit styles. The evaluation is carried out by simulations on these ALU designs. The variation model considers ambient temperature variations and power supply fluctuations that emulate wireless sensor node applications. The results shows that conventional static CMOS circuit operating in near-threshold region exhibits similar power efficiency with adiabatic logic circuit operating in the same region, while at the same time it bears better temperature and voltage variation tolerance in most of the cases. The study results provide helpful guidance to low-power electronic system designs.

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I. INTRODUCTION

Power consumption is playing a more and more important role in present days of VLSI technology. The demand for low-power circuit is growing as portable devices such as laptops, cellular phones, and wearable devices have become prevalent in people's lives. Wireless sensors, medical robot that can be injected into patient's body, and RF chips that process data remotely all need to operate under limited, and sometimes unstable, energy supply. The short battery life or large volume of the battery is one of the holdbacks for such devices. Therefore, lowering the power consumption while maintaining the performance of electronic system become necessary.

Different technologies has been brought about to reduce energy consumption. For example, at system level, designers can scale down power consumption by shutting down part of the system while it is not active in computing [1]. For gate level design, applying different unit designs such as approximate-adder can lower the power consumption as well, at the cost of inaccurate results [2].

To explore for more general methods to reduce power consumption, several methods are studied at transistor level. In part III, we introduce the concept of near-threshold (NTH) and sub-threshold (STH) computing, which are the most widely studied methods to reduce power consumption. By using supply voltages that is remarkably below nominal level, we can reduce power consumption significantly at the cost of performance degradation. It is known that CMOS circuits still functions at very low voltages even when supply voltage V_{DD} drops below threshold voltage. With the voltage

scaling potential, it is important to find the optimal V_{DD} which gives acceptable robustness of the system as well as low power dissipation.

Part III also introduces another transistor level design for low-power applications, which is adiabatic logic style circuit. Adiabatic circuit utilizes the parasitic capacitance to help reduce the charging and discharging speed and lowers the power consumption by storing charges in capacitance and giving it back to the supply. By using alternating current (AC) power source instead of direct current (DC) power, adiabatic circuit stores the charging energy in circuit and charges are moved back to the power source during the discharging process. This kind of charging and discharging process that happens in both pull-up and pull-down circuit can maintain energy in the power source and allow much little power dissipation. Adiabatic circuit is more of a concept than a specific circuit design style.

Several kinds of adiabatic circuit has been proposed and discussed in many previously published works [3]-[8]. They vary in 1) number of operation clocks; 2) single or dual-rail style;3) charging/discharging path; 4) reversible-/irreversible-logic style[9]. As the work of [9] concludes, the reversible energy recovery circuits cause large design overhead in large systems. The design of multiple and multi-clock operations also makes many power-clock-controlled adiabatic circuit unfavorable in complex design. Several other drawbacks of many adiabatic circuits include, 1) the difficulty to cascade logic gates; 2) high switching frequency that may hold back the overall performance; 3) use of trapezoid or triangular clocking scheme, which is hard to generate especially for remote wireless system.

This paper will mainly study complementary energy path adiabatic logic (CEPAL) as the sample adiabatic circuit. Even though it is not the kind of adiabatic circuit with the lowest power consumption, its simplicity in design and static-logic-resembled characteristics makes it easy to be applied in practical designs. Its robustness is also promising among different kinds of adiabatic circuits.

In part III, we show the design of two ALUs by the two different kinds of logic style, conventional static CMOS and adiabatic logic style. The ALU is implemented based on 15nm FinFET process. Part V to part VII describe experimental results from simulating the ALU designs. The experiments are focused on performance, power consumption and variation tolerance, which are the main concerns for designing a stable low-power-supply remote system. We also tried to combine adiabatic circuit with near-threshold circuit by using lower supply voltage on adiabatic circuit. From the results we can observe that, by lowering the supply voltage, near/sub-threshold circuit scales down the power consumption significantly when compared to nominal power supply. The trade-off is that performance is largely sacrificed as circuit delay increases about 100X-10000X from nominal supply power to sub-threshold region. Also because of the much smaller voltage swing of the adiabatic logic circuit under near-threshold region, noise tolerance is seriously weakened. .

II. BACKGROUND AND OBJECTIVE

II.A. Energy Harvesting

The demand for low-power design is extremely high in wireless, implantable devices where the energy often comes from energy harvesting. Energy harvesting is a technique that provides alternative sources of energy instead of energy that comes from large power grid. This harvesting technique is essential in future applications such as wireless devices, which are to operate in longer durations away from centered power sources. Existing energy harvesting techniques can operate on chip and the energy sources include radio frequency energy, thermal and solar energy, acoustic noise energy and many others. New technologies are emerging with better energy harvesting volume, higher efficiency and better power management such as in [16] and [18].

II.B. Low-power Design

To prolong the duration that wireless devices can operate and communicate with its host system, reducing power consumption of such devices is another important option. Technologies such as near/sub-threshold circuit, pass-transistor logic circuit, current mode MOS circuit, and adiabatic logic circuit have been investigated as solutions to reduce power consumption. All these technologies relies on changes in circuit structure at the gate or transistor level. By modifying below the system level, these kinds of techniques give more general alternatives in finding practical low-power designs.

II.C. Objective

The objective of this project is to explore and compare the characteristics of two candidate methods for low-power circuit design: near/sub-threshold computing and adiabatic logic style circuit. We evaluate their characteristics by designing arithmetic logic unit (ALU) using the two low-power techniques and performing simulations on the two designs.

The circuit power consumption, delay and variation tolerance were tested. In specific, for the variation tolerance, we mainly simulated the circuits under difference supply power noise and different temperature. By inserting different kinds of noise, we emulated situations where the supply power varies because of unstable energy harvesting. Studies on such cases could provide better understanding and more realistic expectation of how we design low-power circuit using these two methods and how they behave in real practice.

III. NEAR-THRESHOLD COMPUTING AND ADIABATIC LOGIC CIRCUIT

III.A. Near/sub-threshold Computing

The energy dissipation of CMOS can be attributed to two types, static and dynamic power dissipation. For conventional CMOS circuit, the static power dissipation mainly come from the leakage on the transistor channel. A main power dissipation arises from dynamic power consumption, since energy consumption largely results from the charging and discharging of internal node capacitances. According to a simple model of the transistors, the dynamic power dissipation is proportional to the square of supply voltage.

$$P \propto CV^2 f \tag{3.1}$$

Even though the current in the channel of transistors is not completely linear with the voltage across drain and source, the power dissipation rate is highly dependent on the supply voltage. Reducing the supply voltage has become one of the most widely used methods to reduce power dissipation. CMOS can still operate reasonably well in very low voltages even when V_{DD} goes below threshold voltage.

When V_{DD} goes down to near-threshold region, the power dissipation yields a reduction of about 10X-40X. The price is largely increased circuit delay. When the voltage goes even lower to sub-threshold region, the reduction rate of power dissipation become less. The energy consumption can still go down further but the delay increases exponentially with V_{DD}. As the delay increases, leakage energy become more dominant in sub-threshold region compared to energy dissipated during switching. The minimum

energy is reached when the decrease in dynamic energy dissipation cannot made up for the increase of leakage energy [9]. An approximate illustration of delay and energy consumption from super-threshold to sub-threshold region is given in Fig. 1 and Fig. 2

Because power consumption and delay are two important concerns of low-power circuit, the designer might need to find a balance between them based on whether the system favors low-power feature over performance or the other way around.

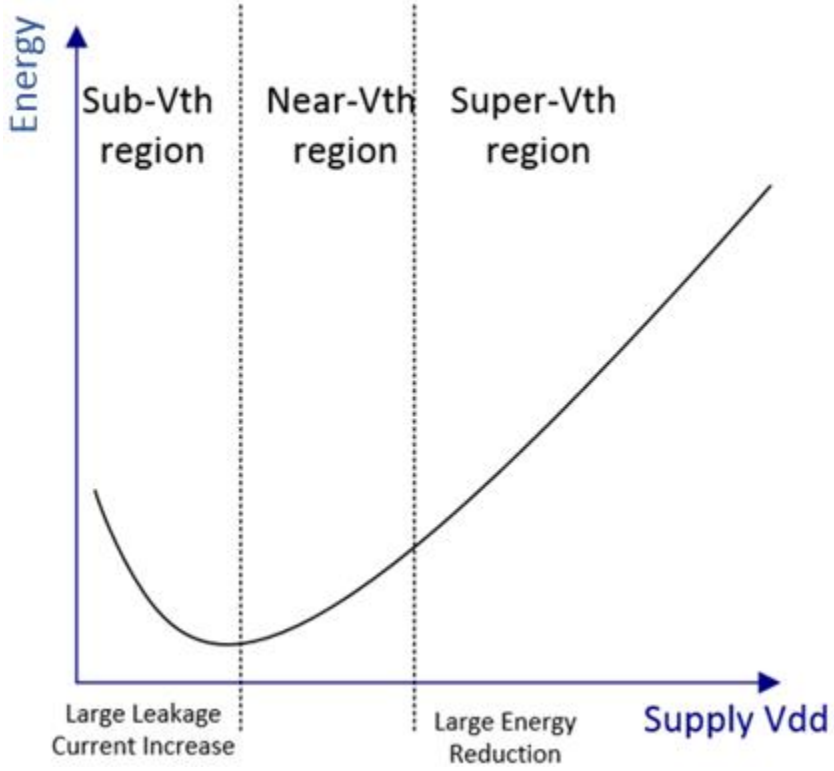

Fig. 1 Energy dissipation in different operating voltage regions[22]

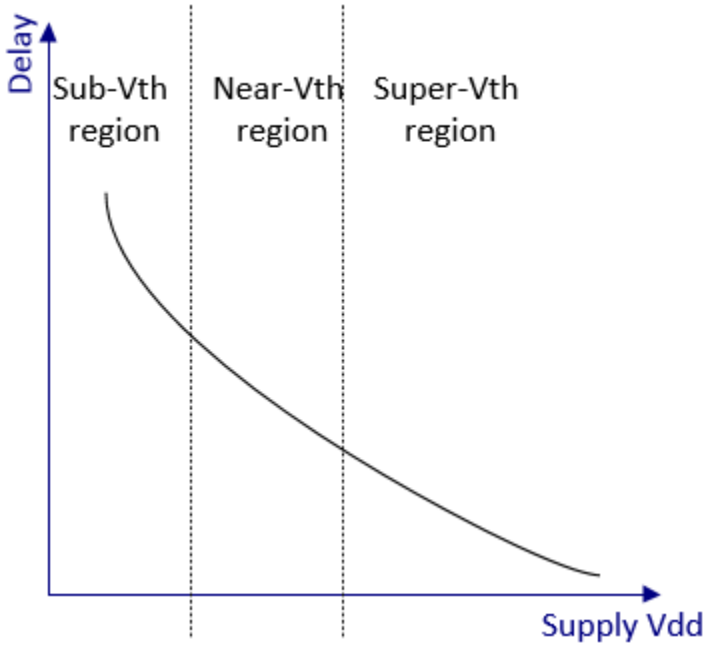

Fig. 2 Delay in different operating voltage regions[22]

III.B. Adiabatic Circuit Logic

Charging and discharging during the switching process is the main contribution to power dissipation. The fundamental principle of adiabatic circuit is to reduce the energy consumed during the charging and discharging process and reach an lower power consumption. Adiabatic logic is also known as “energy recovery” or “charge recovery” logic. As the name itself indicates, the circuit recycles the energy back into the power source and the overall power dissipation can thus be reduced. By using AC power, such kind of energy recycle can be achieved as the supply voltage is no longer constant, which gives a way for the output to recharge the supply source. Fig. 3 and Fig. 4 show the difference of conventional charging and discharging, and the adiabatic charging and discharging.

Consider the charging process, the voltage drop V_R across PMOS transistor can be expressed as

$$V_R = \left(\frac{V_{DD}}{T}\right) t - V_{out} = RC\left(\frac{dV_{out}}{d_t}\right) \tag{3.2}$$

where t is the rising time of the the AC power supply voltage, R is the resistance on the charging path, T is the total switching time of the output, V_{out} is the output voltage, and C is the parasitic capacitance along output path. By solving the above equation, we have

$$V_R = \begin{cases} \left(\frac{RC}{T}\right) V_{DD}\left(1 - e^{-\frac{t}{RC}}\right) & 0 \le t < T \\ \left(\frac{RC}{T}\right) V_{DD}\left(1 - e^{-\frac{t}{RC}}\right) e^{-(t-T)/RC} & t \ge T \end{cases} \tag{3.3}$$

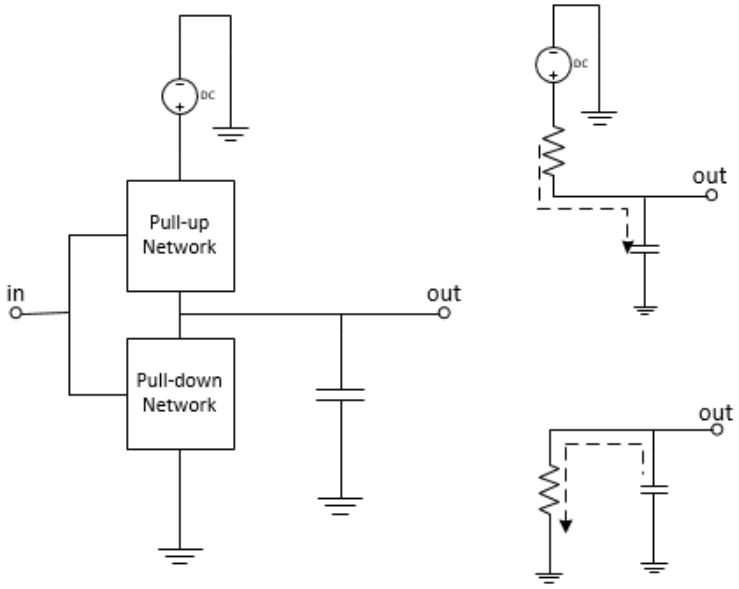

Fig. 3 Conventional CMOS Inverter (left) and its equivalent charging (upper right) and discharging (lower right) path

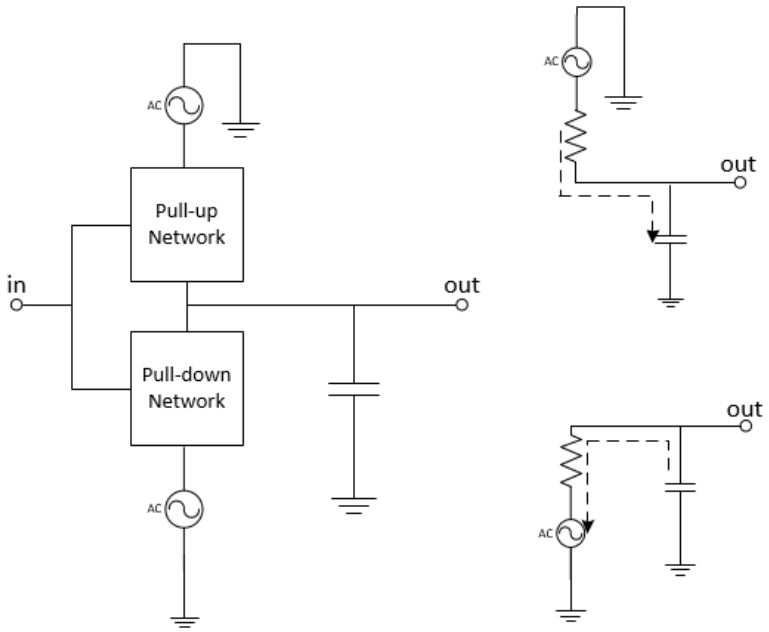

Fig. 4 Adiabatic Logic Inverter Structure (left) and its equivalent charging (upper right) and discharging (lower right) path

Since the power dissipation can be given by

$$P = \int_0^\infty iV_R dt \tag{3.4}$$

We can conclude by (3.3) and (3.4) that

$$P = \left(\frac{RC}{T}\right) CV_{DD}^2 \left(\frac{RC}{T} e^{-\frac{T}{RC}} - \frac{RC}{T} + 1\right) \tag{3.5}$$

The calculation implies that, when we allow longer charging time T, we can reduce power dissipation dramatically.

Allowing arbitrary charging and discharging process time is the main principle in designing adiabatic circuit. By maintaining low voltage drop across conducting devices, adiabatic logic minimizes the energy dissipation.

The energy stored in the output capacitance during the charging process can also be retained by reversing the current direction. Instead of simply discharging into ground in conventional CMOS, adiabatic logic can let the energy be stored in the output capacitance and charged back to the voltage source. The undissipated charges stored in the capacitance can be mostly conserved in the discharging process, or vice versa, instead of dissipating to the ground.

To achieve arbitrary slow charging and discharging process, adiabatic logic circuit requires non-conventional power supplies with time-varying voltage. The changing voltage can help slow down the charging and discharging process, but also cause hardware overhead. In practice, one can apply resonant inductor circuit to generate AC power clock.

Previously published work has covered many kinds of adiabatic logic circuits. These adiabatic logic circuits can be categorized into reversible and irreversible. Reversible energy recovery circuit has the control signal from the next stage, thus brings about large design overhead, which is quite considerable [3][4]. Some irreversible adiabatic logic circuit has the dynamic features that high switching activities may result in poor robustness and large design overhead. Also, many kinds of adiabatic circuit require trapezoid or triangular power clock as power supply, which creates additional difficulty for systems that do not allow too much design overhead. In wireless or remote systems, such design might incur energy waste and more noises. Some adiabatic circuits have poor signal integrity at their outputs. Cascading such circuits leads to progressive degradation of signal quality.

In order to build a robust system that can be easily designed, tested and verified, this paper uses complementary energy path adiabatic logic (CEPAL) as a representative adiabatic logic. Even though its energy consumption is not the minimum among all adiabatic logic styles, its simplicity in design, strong noise tolerance and simple sinusoidal power clock make it a good candidate for remote or wireless systems.

III.C. Complementary Energy Path Adiabatic Circuit

III.C.1. CEPAL Basics.

Complementary energy path adiabatic logic (CEPAL) is chosen for evaluating adiabatic design. CEPAL uses two sinusoidal power clocks, which is much easier to generate for wireless devices than other kinds of AC power clocks. Some adiabatic logic styles produce oscillating outputs that stands for "1" or "0", which is easy for human eyes to tell the result but hard to form combinational logic since the output is not constant. For CEPAL, the steady and constant output for '1' and '0' makes it easy to construct long chain combinational circuit. CEPAL also features similarity with conventional static CMOS and therefore is relatively easy to design.

A main drawback of CEPAL is that it does not provide full voltage swing. Instead, the output high voltage can only go to about 60~80% of V_{dd} and the output low voltage can only go to 20~40% of V_{dd} under nominal supply power.

III.C.2. Structure and Operation of CEPAL

The structure of CEPAL is given in Fig. 5. Besides the conventional CMOS design including the pull-up and pull-network, the CEPAL uses two sinusoidal power sources , PC and $\overline{PC}$ with the same amplitude, the same DC voltage offset, but opposite phases. Two diodes made up by PMOS guide the pull-up network to PC and $\overline{PC}$. Similarly, two diodes made up by NMOS are laid guiding the pull-down network to $\overline{PC}$ and PC. These diodes form two sets of discharging and charging paths for the gate.

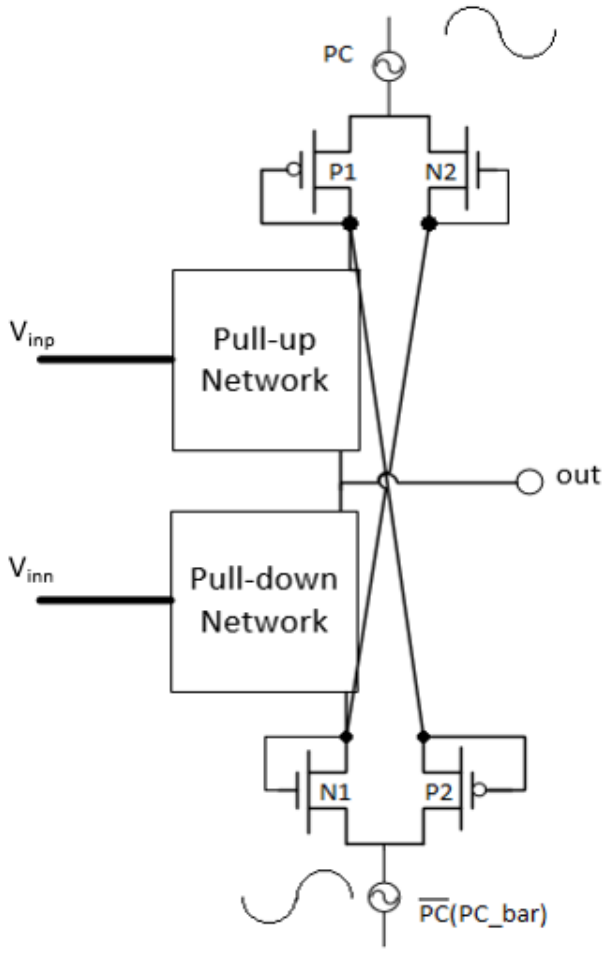

Fig. 5 CEPAL structure logic gate

The operating process of the gate is elaborated as follows. The PMOS pull-up charging paths only allow voltage from PC or $\overline{PC}$ charge the output, and prevent the output discharge through these paths. The NMOS pull-down discharging paths only allow output to discharge through them, and prevent the power source from charging the output through them. Because of the duality like in the conventional CMOS pull-up and pull-down network, either the charging paths or the discharging paths can be turned on at the same time.

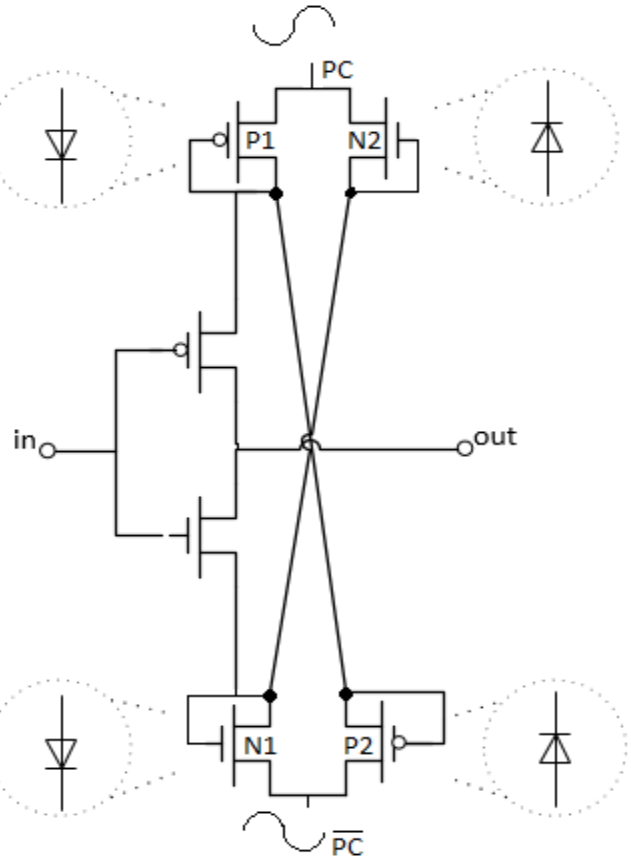

Fig. 6 CEPAL inverter

Take CEPAL NOT gate in Fig. 6 as an example and assume the output (V_{out}) is initially LOW. Now the input becomes LOW, which will turn on the PMOS in the pull-

up network and turn off the NMOS in the pull-down network (Fig. 7 left). Due to the diodes P1 and P2, the output will be charged by either PC or its complement ($\overline{PC}$) as it swings HIGH. When V_{out} reaches HIGH, the following power clock will swing down and leave the output floating. However, the floating situation will not last long since the complement power clock will swing HIGH after less than half power clock cycle, thereby eliminate the weak HIGH at the output(Fig. 7 right). Once the complement power clock swings to low, the output will become floating again, and the floating situation will then be eliminated once the power clock swings up. A loop between the charging and floating process will continue, thus maintains the output voltage level. Similar analysis can also be applied as the output is supposed to be LOW.

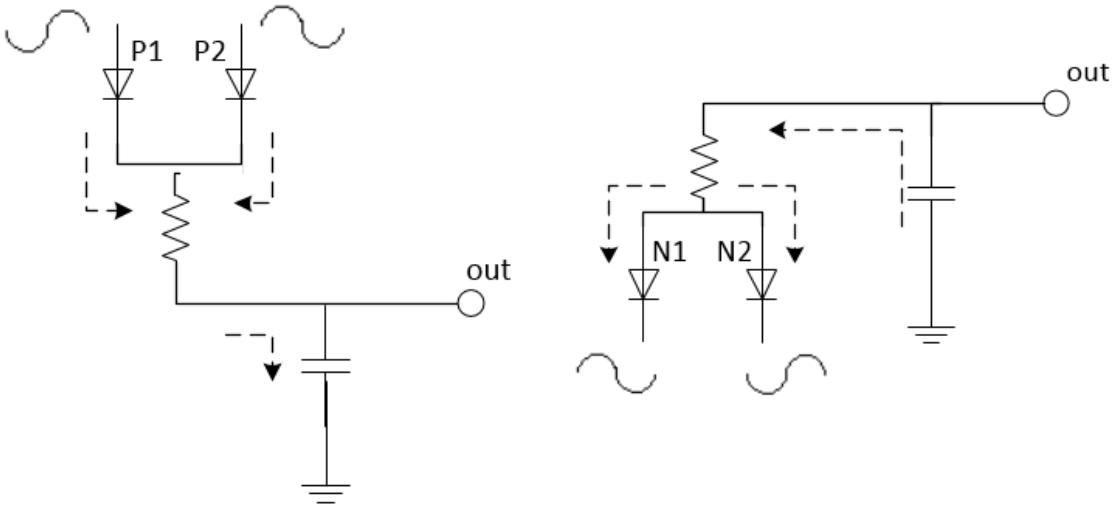

Fig. 7 Equivalent charging and discharging path for CEPAL inverter

III.C.3. Voltage Swing Range of CEPAL

Suppose that the peak value of power clock is V_{DD}, and the corresponding bottom value of power clock is V_{SS}, the power clock frequency is f, the output V_{out} can be charged only when the power clock has higher voltage than the output, the condition is:

$$V_{DD}\sin(2\pi ft) - \left[(V_{DD} - |V_{tp}|) - \left(\frac{I_{ds}\cdot t}{C_L}\right)\right] > V_{tp} \quad (3.6)$$

where V_{tp} is the threshold voltage of PMOS, C_L is the output load, I_{ds} is the leakage current and t is the accumulated time from the moment when the output node becomes floating.

Theoretically speaking, the output voltage can go as high as V_{DD}-$|V_{tp}| - \left(\frac{I_{ds}\cdot t}{C_L}\right)$, which enables the output voltage an almost full swing to the high voltage. Similar analysis can also help us understand the situation when the output is supposed to be discharged to LOW. However, the delay in the charging and discharging path makes the output unable to achieve full charging or discharging. For example, as Fig. 8 shows, when the output is supposed to be charged up to HIGH, the switching of the output is always slower than the switching of the power clock. Also, for charging up a fixed voltage value, the charging process takes long time. Once the power clock drops below output voltage V_{out}, the output node will become floating, and a decay process will happen to this output until the complementary power clock comes to charge the output again. Such repeated charging and floating process will eventually reach a relatively steady state and make the output fluctuate in a small range below V_{DD}. Similar analysis applies for the situation when the output is discharging to LOW. The above analysis

indicates that, for CEPAL circuit, the output cannot reach full swing because of the delay in the charging and discharging process, and the oscillating power clock. An example is the CEPAL Inverter output given in Fig. 9.

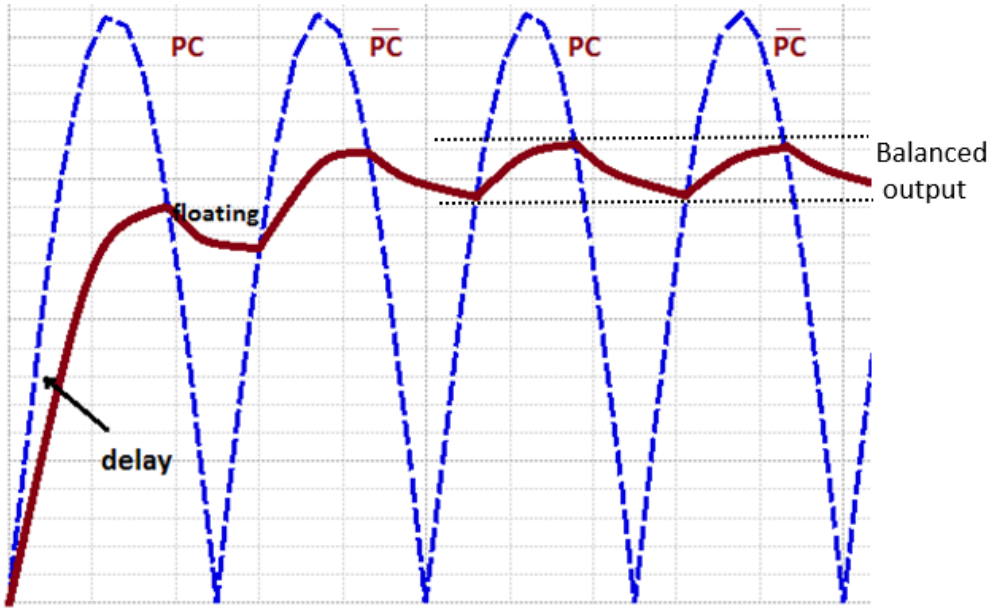

Fig. 8 Charging and floating process of the CEPAL output HIGH

For further analysis, the condition for maintaining the V_{out} can be derived from the analysis on the charging process and floating process when output is supposed to be HIGH, and the equations can be obtained as follows:

$$\begin{cases} t_{float} = \dfrac{C_L \cdot (V_{DD} - |V_{tp}| - \frac{V_{DD}+V_{SS}}{2})}{I_{ds}} \\ t_{charge} = \dfrac{1}{2\pi f} sin^{-1}(\dfrac{|V_{tp}| + \frac{V_{DD}+V_{SS}}{2}}{V_{DD}}) \end{cases} \tag{3.7}$$

where t_{float} is the time required that the output drops from V_{DD} to the switching point $\frac{V_{DD}}{2}$, and t_{charge} is the time required that the output charges from switching point to V_{DD}. The leakage current I_{ds} will be discussed in part 5 in this section.

The following equation always holds.

$$t_{float} + t_{charge} = T_{pc}/2 \tag{3.8}$$

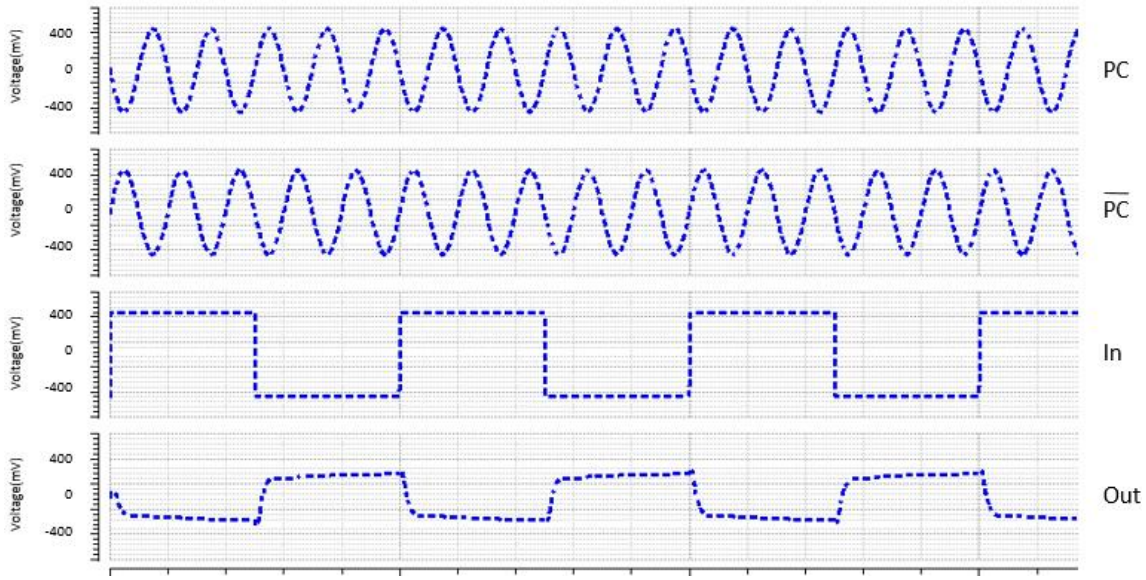

Fig. 9 Input and output of CEPAL Inverter

where T_{pc} is the power clock period. When the output stays at HIGH, it will be in either floating state or charging state. In reality, the time that the output stays floating is smaller than what (3.7) indicates, since the output cannot be charged to V_{DD}. In addition, because the power clock generally has much higher frequency than the circuit clock, the floating output will not reach the switching point $\frac{V_{DD}}{2}$ before the complementary power clock rises up and reaches switching point. Suppose the range where the output stays HIGH is V_{HL}~V_{HH}, (3.7) can be rewritten as:

$$\begin{cases} t_{float} = \frac{C_L \cdot (V_{HH} - V_{HL})}{I_{ds}} \\ t_{charge} = \frac{1}{2\pi f} sin^{-1}(\frac{|V_{tp}| + V_{HL}}{V_{HH}}) \end{cases} \tag{3.9}$$

where $\frac{V_{DD}}{2} < V_{HL} < V_{HH} < V_{DD}$. The actual value for V_{HL} and V_{HH} may need rigorous computation depending on the delay model.

III.C.4. CEPAL Power Clock Generation

This thesis work mainly focuses on the implementation of CEPAL and its combinational circuit. The power clock generation is assumed given and some previous work on this topic is briefly introduced in this section.

CEPAL circuit uses AC power source, which needs discussion on its generation. Most energy harvesting techniques are based on DC form, such as solar power. To achieve high power-conversion efficiency, oscillators based on LC resonant circuits can be used to provide the adiabatic system AC source.

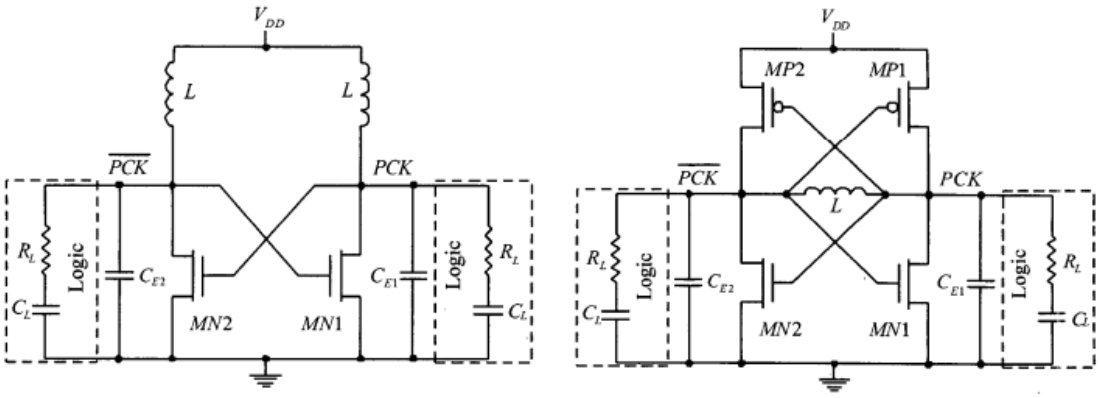

Fig. 10 An example of 2N and 2N2P power clock generator from[23]

Fig. 10 illustrates two commonly used power clock generators that can generate sinusoidal voltage based on self-oscillation without external timing signals: 2N and 2N2P power clock generators [23]. They are simple dual-rail LC oscillators based on the

coupled NMOS and PMOS transistor pairs. Even the self-oscillating power clock generators are quite sensitive to their capacitive load variations, thus the frequency of the power clock can be unstable. Simulation results show that the power and delay of adiabatic output has little dependence on the power clock frequency as long as it is much higher than the circuit frequency.

The work of [24] introduced a power clock generator design that has energy efficiency higher than 85%. The 1N1P self-oscillation in [24] is achieved through LC resonant circuit. The oscillation voltage swing can reach, or even be greater than the GND~Vdd range provided by the DC power supply. With the self-oscillation circuit, the AC power for CEPAL circuit can be well supported.

III.C.5. Power Dissipation and Leakage of CEPAL

III.C.5.a) Diode Dissipation

The main power dissipation in CEPAL occurs at the (MOS) diodes, which is a non-adiabatic loss. The main loss happens when a charge or a discharge happens in one of the four diodes. Actually when compared with QSERL [20], the power dissipation does not increase much since for both QSERL and CEPAL, only one of the diodes is conducting current during charging and discharging process. This kind of dissipation occurs all the time since one of the four diodes will be conducting current at any time when the transistor operates. However, as the later results show, the power dissipation on the diodes is quite significant, especially in near-threshold region.

III.C.5.b) Drain-Source Leakage

The leakage current is considered in (3.7). As in [18], the leakage current between drain and source can be written as:

$$I_{ds} = I_{ds0} \cdot e^{\left(\frac{V_{gs}-V_t}{nv_T}\right)} \cdot \left[1 - e^{\left(\frac{-V_{ds}}{V_T}\right)}\right] \tag{3.10}$$

where V_T is the thermal voltage, V_t is the threshold voltage and I_{ds0} is the process, dimension and thermal voltage-dependent coefficient. The greater V_{gs} is, or the greater V_{ds} is, the greater leakage there exists. However, the actual leakage is not as significant as what (3.10) indicates. In CEPAL, the output HIGH and LOW cannot reach V_{DD} or V_{SS}, hence the leakage is not as great as that in CMOS where the output can maintain a full swing.

On the other hand, leakage current may occur due to short circuit from pull-up network to pull-down network. In conventional static CMOS, weak input and output may lead to short circuit leakage from V_{DD} to GND. But in adiabatic logic style, since both of the power clocks are sinusoidal and either of them can be the charging source to HIGH or discharging drain to LOW, the leakage from one power clock to another can be viewed as two power clocks charging each other. Such leakage can be recycled between the two power sources, so it is not an actual power loss. Nevertheless, thermal dissipation still occurs on the pull-up and pull-down network as current flows through PMOS and NMOS.

III.C.6. Combination of CEPAL and Near-threshold Circuit

The mechanism of adiabatic circuit operations mainly relies on the special transistor-level circuit topology and the time-varying power supply. Near/sub-threshold circuit simply scales the supply voltage level for conventional static CMOS design. Therefore, adiabatic circuit and near/sub-threshold design are two orthogonal approaches that can be directly combined. By making the adiabatic circuit working in a near-threshold AC power source, or even sub-threshold region, we may achieve further power savings.

In the later sections, we will explore the power efficiency, delay and variation tolerance in CEPAL ALU, conventional ALU in near/sub-threshold region, and CEPAL ALU in near-threshold region (CEPAL/NTH combined).

IV. ALU DESIGN AND SIMULATION SETUP

IV.A. Process and Tools

The process we used is from NanGate FreePDK15, which includes 15nm process FinFET standard cells provided by NCSU. These standard cells cover models for both P-type FinFET and N-type FinFET, as well as a set of standard cell designs of basic static CMOS logics gates that can be used in logic synthesis. The static CMOS standard cells can be utilized to construct near/sub-threshold circuit.

To make fair comparison between conventional CMOS circuit, near/sub-threshold circuit and CEPAL circuit, we utilized the pFET and nFET to build the corresponding CEPAL standard cell. We mainly used Cadence Virtuoso as the tool in designing the CEPAL library cell we need to implement ALU and the test cases.

To complete the ALU design, we used Synopsys Design Vision to do the logic synthesis of the ALU netlist based on Verilog behavioral description. Once we obtain the netlist, we import the netlist to Cadence Virtuoso and assemble the conventional CMOS cell and CEPAL cell complete the design of the conventional, ALU circuit and the CEPAL ALU.

To test the power consumption, delay and noise tolerance of different designs, we used Cadence Virtuoso to set up the test bench. The simulations are conducted using Cadence Spectre.

IV.B. Arithmetic Logic Unit Design

The arithmetic logic unit (ALU) is a core component in typical microprocessor designs. It can perform basic arithmetic and bitwise logical operations. A wireless device with data processing capability often contains multiple ALUs.

The ALU we designed can perform 8 different arithmetic or logic operations on two active high unsigned 8-bit operation words A = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) and B = (B_7, B_6, B_5, B_4, B_3, B_2, B_1, B_0), and produce an 8-bit result R = (R_7, R_6, R_5, R_4, R_3, R_2, R_1, R_0). The operation mode is decided by three selection signal OP_2, OP_1, and OP_0 as summarized in Table 1. The implemented ALU structure is capable of operating in either conventional CMOS mode, near-sub-threshold mode or complementary energy path adiabatic logic mode.

Table 1. Functions of the ALU

Operation Select Signals			Operation
OP_2	OP_1	OP_0	
0	0	0	A+B
0	0	1	A-B
0	1	0	A and B
0	1	1	A or B
1	0	0	B shift right by A bits
1	0	1	A nor B
1	1	0	A xor B
1	1	1	A < B ?

Overall, the ALU has 19 input bits and 8 output bits. In our synthesis result, the ALU contains about 300 logic gates which are implemented by either conventional CMOS cells or CEPAL cells. The input and output pins are depicted in Fig. 11.

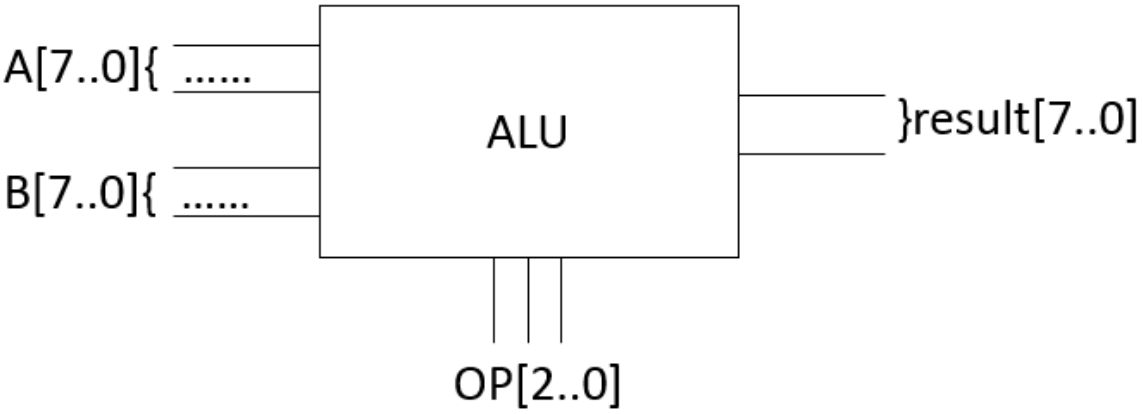

Fig. 11 Input and output pins of ALU

IV.C. Voltage and Frequency Setup

From the circuit topology point of view, the comparisons are mainly focused on power efficiency, performance and noise tolerance between static CMOS and CEPAL circuit. We start the comparison from where the supply voltage can give full swing of the input. For the 15nm technology, the nominal power supply range V_{DD}-V_{SS} is 0.8V.

For CEPAL circuit, which uses alternating current power, we set the one side amplitude of the sinusoidal supply voltage as 400mV. This will provide the input HIGH as 400mV and input low as -400mV. The output swing range will also be limited within -400mV to 400mV.

For near/sub-threshold circuit, we tested its performance under different voltages ranging from 800mV to several tens of millivolts. Reducing the supply voltage

amplitude is also a good way for adiabatic circuit in reducing its power dissipation. Thus, we further combine CEPAL circuit with near/sub-threshold computing, and tested its performance in near-threshold region.

Because of the poor performance for adiabatic circuit, the operating frequency for the ALU is set to be low. From simulation results, we see that the optimal frequency for adiabatic circuit is from several hundred kilo-hertz to several mega-hertz. Because we wish to ensure test the correctness of circuit operations, we set the operating frequency at 100kHz for adiabatic circuit working under near-threshold supply voltage region. Such low frequency is still practical in situations where high-performance computing is not very necessary. The corresponding power clock frequency is set to 5MHz, which is much higher than the circuit clock frequency.

V. POWER DISSIPATION AND DELAY COMPARISON

V.A. Power Dissipation Estimation

V.A.1. Power Dissipation Estimation in CMOS

Energy consumption in CMOS mainly comes from the charging and discharging process, which is also known as dynamic power dissipation. The instantaneous power dissipation rate of a voltage source can be written as:

$$\mathrm{P(t)} = \mathrm{i}_{DD}(\mathrm{t})\mathrm{V}_{DD}(\mathrm{t}) \tag{5.1}$$

where the current flowing through the source and the voltage source instant voltage value are dependent on time. The majority part of dissipation, which is dynamic power, can be written as:

$$\mathrm{P(t)} = \frac{1}{T}\int_0^T \mathrm{i}_{DD}(\mathrm{t})\mathrm{V}_{DD}(\mathrm{t}) \tag{5.2}$$

For static CMOS, supply voltage $\mathrm{V}_{DD}(\mathrm{t})$ remains constant V_{DD}. Meanwhile, the integral of charge from time 0 to clock period T is proportional to the parasitic capacitance and the supply voltage,

$$\int_0^T \mathrm{i}_{DD}(\mathrm{t}) = T\mathrm{f}_{sw}C\mathrm{V}_{DD} \tag{5.3}$$

where f_{sw} is the frequency at which the output swings. By combining (5.2) and (5.3), we obtain

$$\mathrm{P(t)} = CV_{DD}^2 f_{sw} \tag{5.4}$$

From (5.4) we can see that for conventional static CMOS, the power dissipation is proportional to V_{DD}^2. However, this is merely an approximation with simple model, especially in super-threshold region. In the super-threshold region, the voltage scaling

down to near-threshold yields an energy reduction more than quadratic changes. However, the leakage effect becomes dominant in the near-threshold region and the power savings from voltage scaling would be different.

V.A.2. Power Dissipation Estimation in CEPAL

For CEPAL circuit, where V_{DD} is dependent on time:

$$V_{DD}(t) = A \cdot \sin(2\pi f_{pc} t + \beta) \tag{5.5}$$

where A is the amplitude of the sinusoidal voltage, f_{pc} is the frequency of the power clock, and β is the initial phase of the clock. Combining (5.5) and (5.2) will result in a complex expression, which will not be further elaborated here. Also, the voltage scaling on the diodes on the 4 charging and discharging paths will affect the power dissipation on these diodes. While the analysis of static CMOS still applies to a certain extent, accurate measurement from simulation could better demonstrate the voltage scaling effect on CEPAL circuit.

V.B. Delay Estimation

An effective way of estimating the delay is by using RC model where

$$\text{delay} \propto RC \tag{5.6}$$

MOSFET, including FinFET, is not linear device, as the effective resistance depends on V_{gs} and V_{ds}. From Shockley 1st order transistor models

$$I_{ds} = \begin{cases} \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}, & V_{ds} < V_{dsat} \\ \frac{\beta}{2} (V_{gs} - V_t)^2, & V_{ds} > V_{dsat} \end{cases} \tag{5.7}$$

which defines the Drain-Source current for linear and saturation region. From both equations in (5.7), we can see that the drain-source current is strongly dependent on the square of the drain-source voltage, which is approximately $V_{DD} - V_{SS}$ when voltage drop is applied on the transistor. From Ohm's law we can derive that the effective resistance is inversely proportional to the supply voltage.

The dependency of delay on V_{dd} becomes more complex as voltage scales to near or sub-threshold region. In such situation, the delay increases exponentially [22] with V_{dd}. A reduction of 50% on supply voltage might bring only 50% reduction in power dissipation in sub-threshold region, but may cause about 50X-100X delay increase.

V.C. Condition Set-ups and Results Display Methods

Unless otherwise explained, all the simulations are conducted with temperature being set to 27℃. For the result, the power dissipation is the average power dissipated from the voltage source in the entire simulated period.

Measuring delays of all input switching patterns is not practical. We selected 8 switching patterns of the input, tested the output delay caused by the corresponding switching activity, and calculated the average of the 8 delays.

The waveforms provided in this thesis are restricted to several representative cases, as it is neither practical nor necessary to cover all cases.

V.D. Power Dissipation and Delay Simulation

To compare the power dissipation and delay difference between static CMOS and CEPAL circuit, we simulated cases where the supply voltage ranges from 800mV to 200mV. From the sets of simulation we have done, even though CEPAL ALU with supply collage of 800mV can be operating at the input frequency of 1MHz, its output yields much higher delay when the supply voltage drops to 200mV. Hence, we set the input frequency to 100kHz for all simulations we conducted. Accordingly, the power clock frequency of CEPAL circuit is set to 5MHz. Table 2 shows the power and delay dependency on the supply voltage swing.

Table 2. Power dissipation and delay of conventional CMOS and CEPAL ALU under different supply voltages

Supply Voltage Range (mV)	Static CMOS		CEPAL	
	Power Dissipation(nW)	Average Delay(ns)	Power Dissipation(nW)	Average Delay(ns)
800	3255	0.7	2278	31.6
600	1360	1.2	1182.2	39.0
400	540.9	2.1	521	138.4
300	320.9	3.8	318.6	362.7
200	167.4	19.7	174.6	940.8
100	64.24	258.7	-	-

It can be observed that, when operating under nominal voltage, CEPAL circuit yields 30% better power efficiency compared to static CMOS. However, the delay is

about 16 times greater than that of static CMOS. As the supply voltage level scales down, power consumption for both circuit decreases, with the increase in delay.

Table 3. Power and delay comparison between static CMOS and CEPAL ALU under different supply voltages

Supply Voltage Range(mV)	Power Dissipation Ratio (Static CMOS/CEPAL)	Delay Ratio (Static CMOS/CEPAL)	Power×Delay Ratio
800	1.4289	0.0206	0.0294
600	1.1504	0.0301	0.0346
400	1.0382	0.0149	0.0155
300	1.0072	0.0105	0.0106
200	0.9588	0.0210	0.0201

For CEPAL ALU, its power dissipation decreases more slowly than that of static CMOS, and reaches almost same level when the supply voltage is at 200mV. When the supply voltage is below 200mV, CEPAL ALU fails to function correctly, so no delay and power dissipation results are provided for CEPAL at 100mV. Such fact makes CEPAL circuit unfavorable in term of performance when the supply voltage is very low, since its delay is still over 10 times greater than static CMOS. Moreover, CEPAL circuit costs more area as it needs more transistors in each gate design.

A ratio between the power × delay product of static CMOS and CEPAL is given in table 3. For designs that value performance and power dissipation both, the data shows that static CMOS is still more favorable under most of the situations. CEPAL

circuit might be a good choice when the delay constraint is not strict and supply voltage is relatively high.

V.E. CEPAL Voltage Swing

Besides the delay increase, for CEPAL ALU, its input/output voltage swing ratio reduces as the supply voltage scales down, as is shown in Fig. 12 and Fig. 13, which provide the waveforms of three output pins for the two simulations. For CEPAL ALU working under -400mV~400mV supply voltage, the voltage swing of the output can reach to about 71% of the input swing. However, when the supply voltage scales down to -100mV~10mV, the output swing only reaches 25% of the input. The main reason for the loss in output voltage swing is that the voltage drop on the diodes become dominant as the supply voltage scales down. Even when fully charged through the charging paths with the diodes, the output voltage cannot reach very high as the diodes account for a large portion of the overall voltage drop. Additionally, as the charging and discharging process become slower when the voltage scales down, the output capacitance gains less charging or discharging from the voltage source.

Such loss in voltage swing is harmful as it reduces noise margin and jeopardizes functional correctness. As such, a minor fluctuation in the supply voltage can easily lead to incorrect output. Such influence can be illustrated in the following analysis in noise tolerance especially when working under situations where the supply voltage is low and unstable.

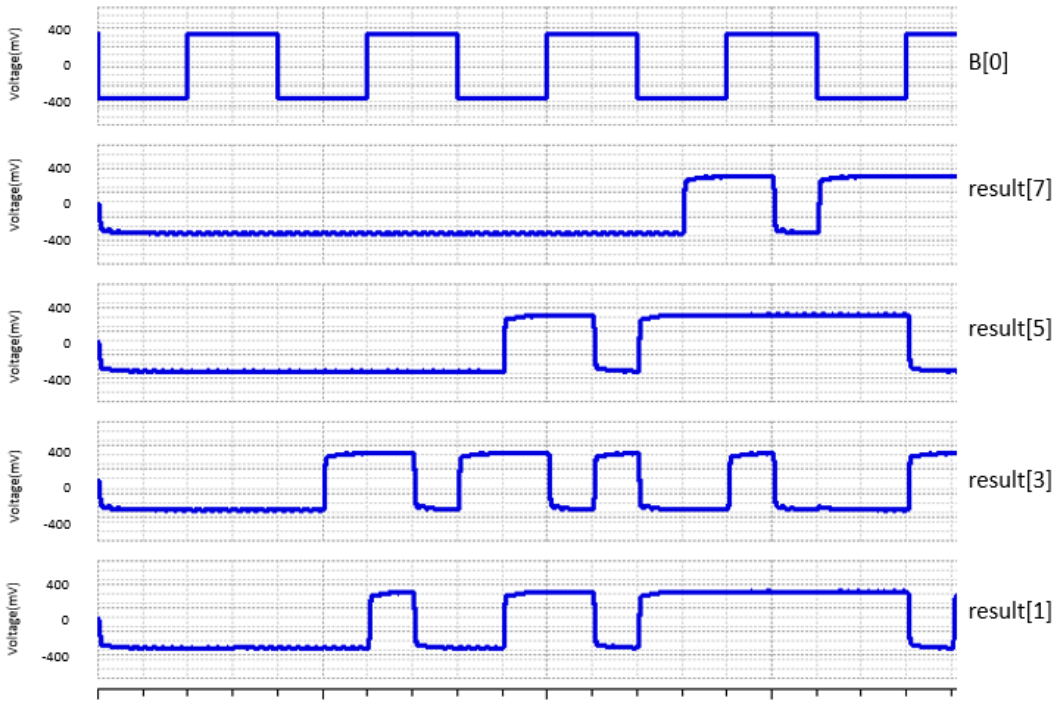

Fig. 12 CEPAL output when working under -400mV~400mV

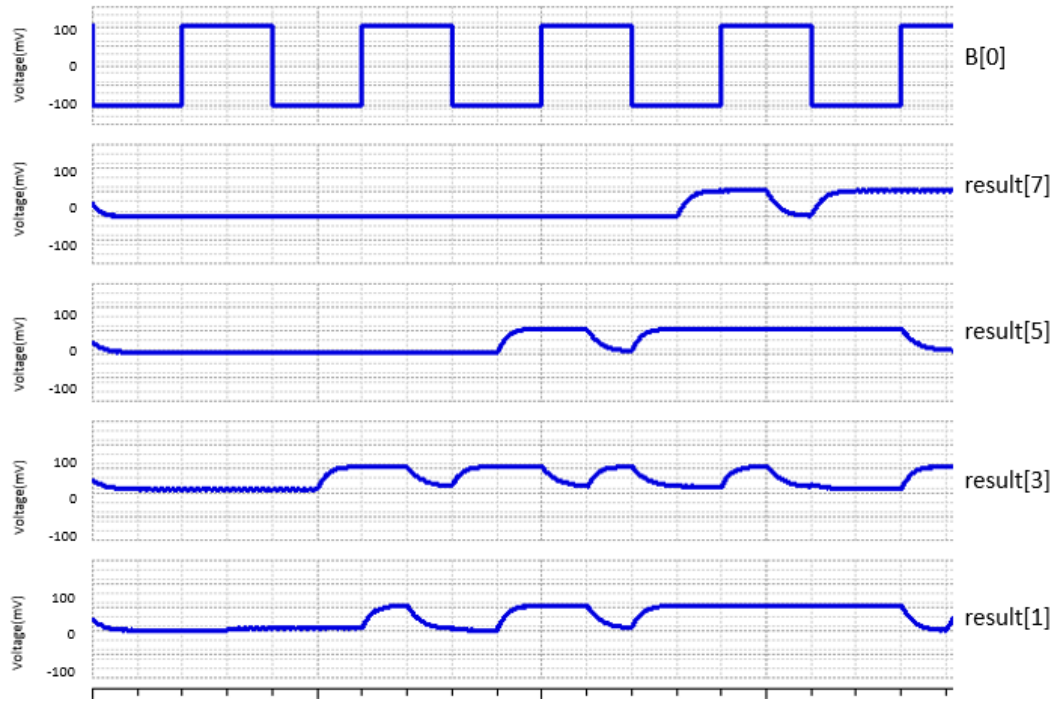

Fig. 13 CEPAL output when working under -200mV~200mV

VI. TEMPERATURE VARIATION TOLERANCE

VI.A. Simulation Set-ups

From previous simulation results, we found that static CMOS in near/sub-threshold computing and CEPAL in near-threshold computing yield similar power consumption. Next, we compare their tolerance to temperature variations and noise interference.

For the temperature variation tests, we simulated static CMOS ALU in near-threshold region under supply voltage 200mV, and CEPAL ALU under alternating supply voltage -100mV~100mV. The temperature range is set to from 0℃ to 125℃.

VI.B. Simulation Result for Static CMOS and CEPAL at NTH

As shown in Table 4, for both static CMOS and CEPAL circuit, the power consumption and delay are greatly influenced by temperature changes. An approximately 80X increase in power occurs when temperature rises from 0℃ to 100℃ for both type of circuits, while the power increase for static CMOS is slightly less (81X) than CEPAL (83X). At 125℃, CEPAL circuit consumes significantly more power than static CMOS, and it also fails to function correctly. When the temperature rises to 125, the CEPAL ALU output is so unstable output that the delay is hard to determine.

Table 4. Power dissipation and delay of conventional CMOS and CEPAL ALU under different temperatures

Temperature (℃)	Static CMOS		CEPAL	
	Power Dissipation(nW)	Average Delay(ns)	Power Dissipation(nW)	Average Delay(ns)
0	43.5	44.98	42.7	3369.5
27	167.4	19.72	174.6	940.8
50	487.4	11.45	493.8	135.8
75	1388	6.98	1374	70.0
100	3527	3.93	3550	50.8
125	8137	2.13	15885	-

As the temperature rises to 75℃ or higher, which is actually a common situation, the output voltage swing scales down and the expected LOW output rises to only several millivolts below 0. This is dangerous since such high LOW output could be easily evaluated as HIGH by flip-flops. Even though we can adjust flip-flops to change the threshold between HIGH and LOW, such small output swing could easily lead to incorrect operation of the ALU (see Fig. 14).

CEPAL circuit has another drawback. That is, as the temperature goes up, its output becomes more and more unstable such that it fluctuates in a small range in the HIGH margin. Fig. 14 for CEPAL ALU operating at 100℃ shows that its output HIGH fluctuates in range 135~142mV, and its output LOW fluctuates in range 89~93mV. When operating at 125℃, CEPAL circuit is so unstable so that its output HIGH fluctuate

in range 99~155mV and LOW in range 94~106mV. The overlap in the HIGH and LOW output range makes it almost impossible to function correctly.

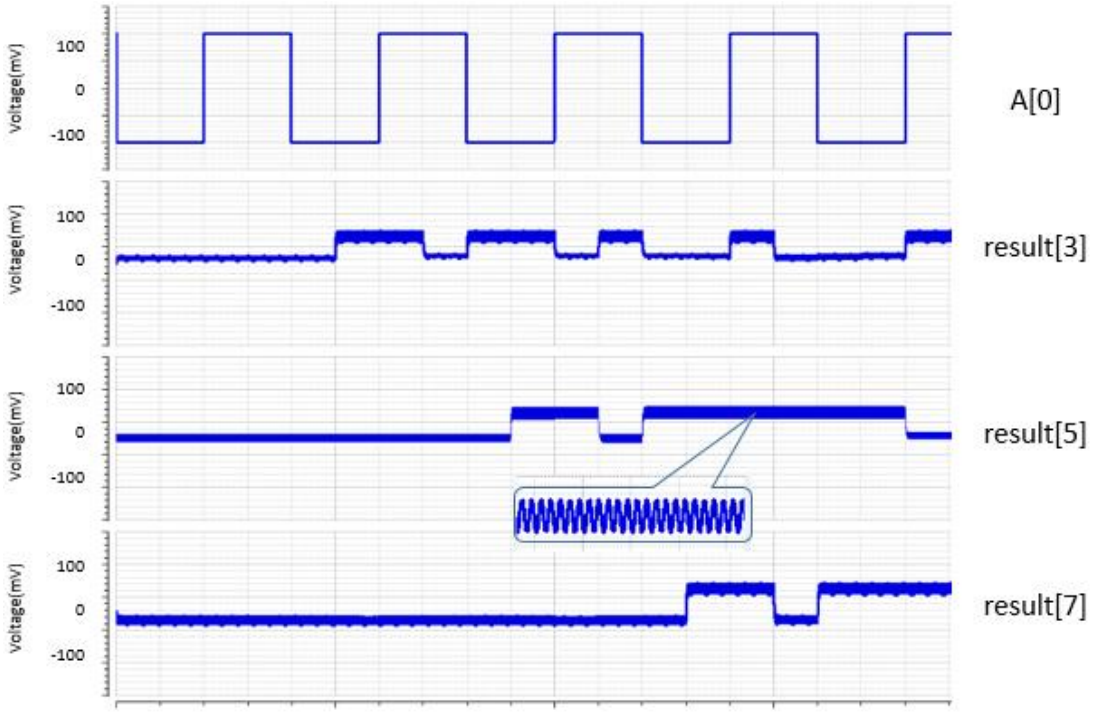

Fig. 14 CEPAL ALU waveform when working under 100℃

On the contrary, static CMOS shows better stability at high temperature. Its output LOW only rises to about 4mV at 125℃. Its output HIGH is stabilized around 200mV (Fig. 15).

In terms of delay, CEPAL circuit experiences relatively large changes when temperature rises. An interesting fact for the FinFET ALU is that, as the temperature goes higher, circuit delay becomes smaller. A 66X delay reduction is observed for CEPAL when temperature rises from 0℃ to 100℃. The delay change for the static

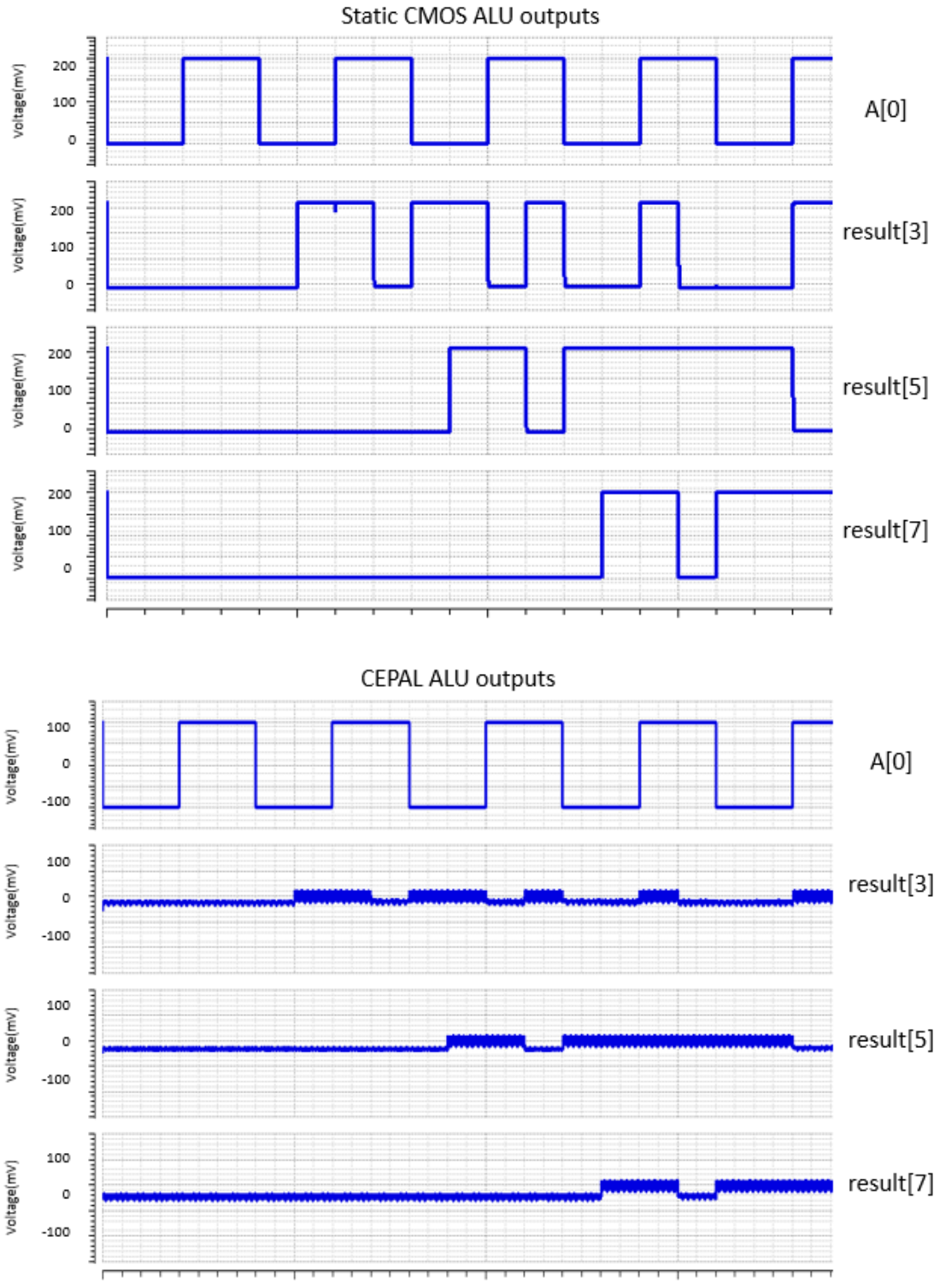

Fig. 15 Static CMOS and CEPAL ALU outputs at 125℃

CMOS counterpart is 11X. However, the absolute delay for CEPAL is still 10X to 100X greater than static CMOS.

VI.C. Static CMOS at Near and Sub-threshold Region

Previous results have shown that at different temperatures, static CMOS is still superior on power dissipation, delay and stability. Furthermore, we lower the supply voltage and see its characteristics in sub-threshold region. Table 5 gives the comparison between sub-threshold static CMOS operating at 100mV supply voltage and near-threshold static CMOS from the previous section.

Table 5. Power dissipation and delay of conventional CMOS working at near-threshold region(200mV) and sub-threshold regions(100mV)

Temperature (℃)	NTH(200mV)		STH(100mV)	
	Power Dissipation(nW)	Average Delay(ns)	Power Dissipation(nW)	Average Delay(ns)
0	43.5	44.98	14.3	859.0
27	167.4	19.73	64.2	258.7
50	487.8	11.45	195.9	107.8
75	1388	6.98	572	36.9
100	3527	3.93	1481	24.3
125	8137	2.13	3480	4.6

From the comparison between near-threshold computing at 200mV and sub-threshold computing at 100mV, we can see that sub-threshold ALU power consumption is about 1/3 of near-threshold ALU, with much greater delay. The power consumption

ratio of near-threshold/sub-threshold decreases as temperature increases (Table 6), which indicates that sub-threshold is a little more sensitive in terms of power as the temperature increases. The delay ratio, on the other hand, shows that sub-threshold computing still achieves good performance in high temperature since it is only several times higher than that of near-threshold computing. However, its delay is relatively large at low temperature.

Table 6. Power and delay and their product comparison between near-threshold CMOS and sub-threshold CMOS

Temperature (℃)	Power Dissipation Ratio (NTH/STH)	Delay Ratio (NTH/STH)	Power×Delay Ratio
0	3.04	0.0524	0.1592
27	2.61	0.0762	0.1987
50	2.49	0.1062	0.2645
75	2.43	0.1890	0.4587
100	2.38	0.1619	0.3855
125	2.34	0.4670	1.0920

Like the case of CEPAL ALU in near-threshold region, the waveform of sub-threshold computing result shows that the output signal becomes unstable at high temperature (Fig. 16). For example, at 125℃, the output LOW for the sub-threshold ALU rises up to nearly 59mV and at 100℃ the output LOW can rise up to 29mV. Such abnormal output LOW could degrade the ALU accuracy since it might go beyond the LOW noise margin and be recognized as HIGH by flip-flops. Near-threshold circuit, as shown before, maintains stable output with LOW at 4mV, which means about 196mV

output swing compared to about 41mV for sub-threshold computing at 125℃. High output swing promises strong noise tolerance and stability.

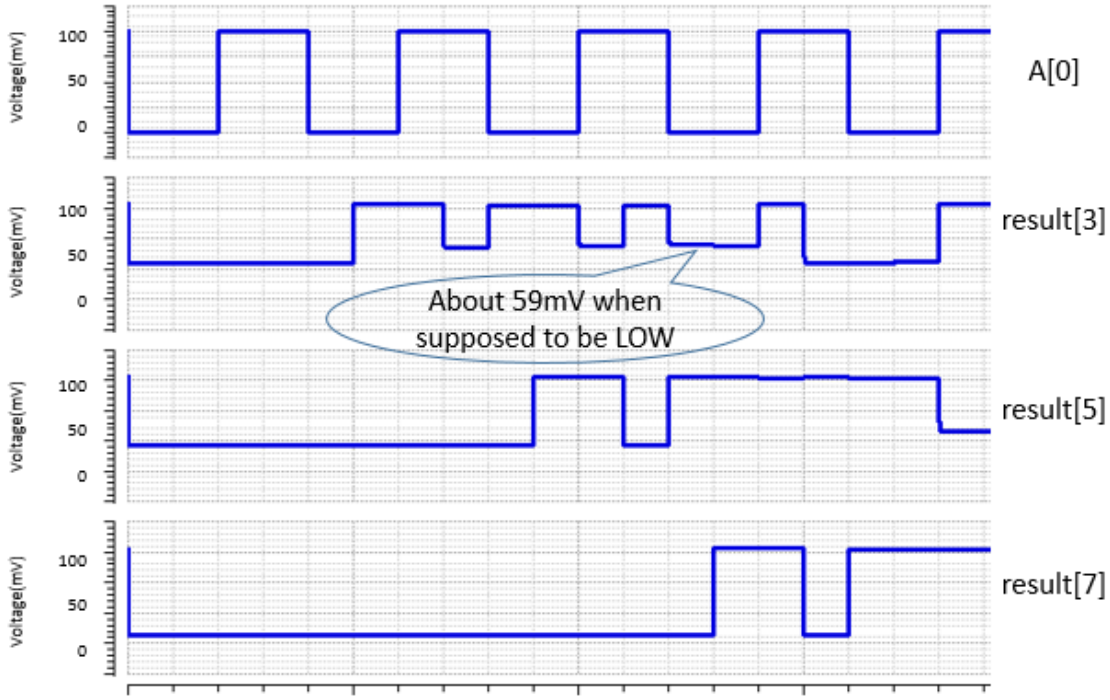

Fig. 16 Abnormal outputs given by sub-threshold computing ALU

VII. VOLTAGE NOISE TOLERANCE COMPARISON

In this section, we will mainly compare the noise effect between static CMOS on near-threshold computing and CEPAL ALU on near-threshold computing We will mainly compare the characteristics of static CMOS and the CEPAL circuit operating at 200mV voltage (swing) since they exhibit similar power dissipation level at this voltage level.

VII.A. High Frequency Noise Effect

VII.A.1. Simulation Results

High frequency noise, in this simulation setup, refers to noise with frequency higher than the circuit frequency. In our simulation, we used "Gaussian Noise" with frequency range 10kHz~20MHz, the PSD (power spectrum density) of the noise is set to $10^{-9}V^2/Hz$. We assume such noise is additive and superposed on the supply voltage source.

The output waveforms of the two kinds of ALUs are shown in Fig. 17. The waveforms indicate that while the output of static CMOS is strongly distorted in presence of the noise, the CEPAL circuit does not show much distortion in the output. Unlike static CMOS, the output of CEPAL can always stay within the HIGH or LOW noise margin. This observation might not be sufficiently convincible that CEPAL circuit is more high-frequency-noise-tolerant than static CMOS. Therefore, we run simulation to verify the correctness of both of the ALU outputs.

Because the noise we injected is time-dependent, to verify the outputs, we can sample the output for the same input several times in one simulation to test the output correctness. For example, for a certain pattern of input vector, we can make the input signals A[7..0], B[7..0]and OP[2..0] unchanged during one verification process, and sample its output at time 1us, 2us, …10us. Also, at the end of the output, we put a flip-flop to translate the low HIGH and high LOW output to strong output voltage. To verify the intermediate output voltage that is neither close to V_{DD} or V_{SS}, we used flip-flops to evaluate the output and examine its logic result.

Because the verification process for ALU on Cadence Spectre is slow, we only tested 78 sets of input vectors. For every input vectors we tested 10 times, so the total number of outputs sampled is 780. Only 2 out of 780 outputs from static CMOS ALU produce inaccurate outputs, and each wrong output has only one bit error. The two incorrect outputs happen on result[0] and result[5].

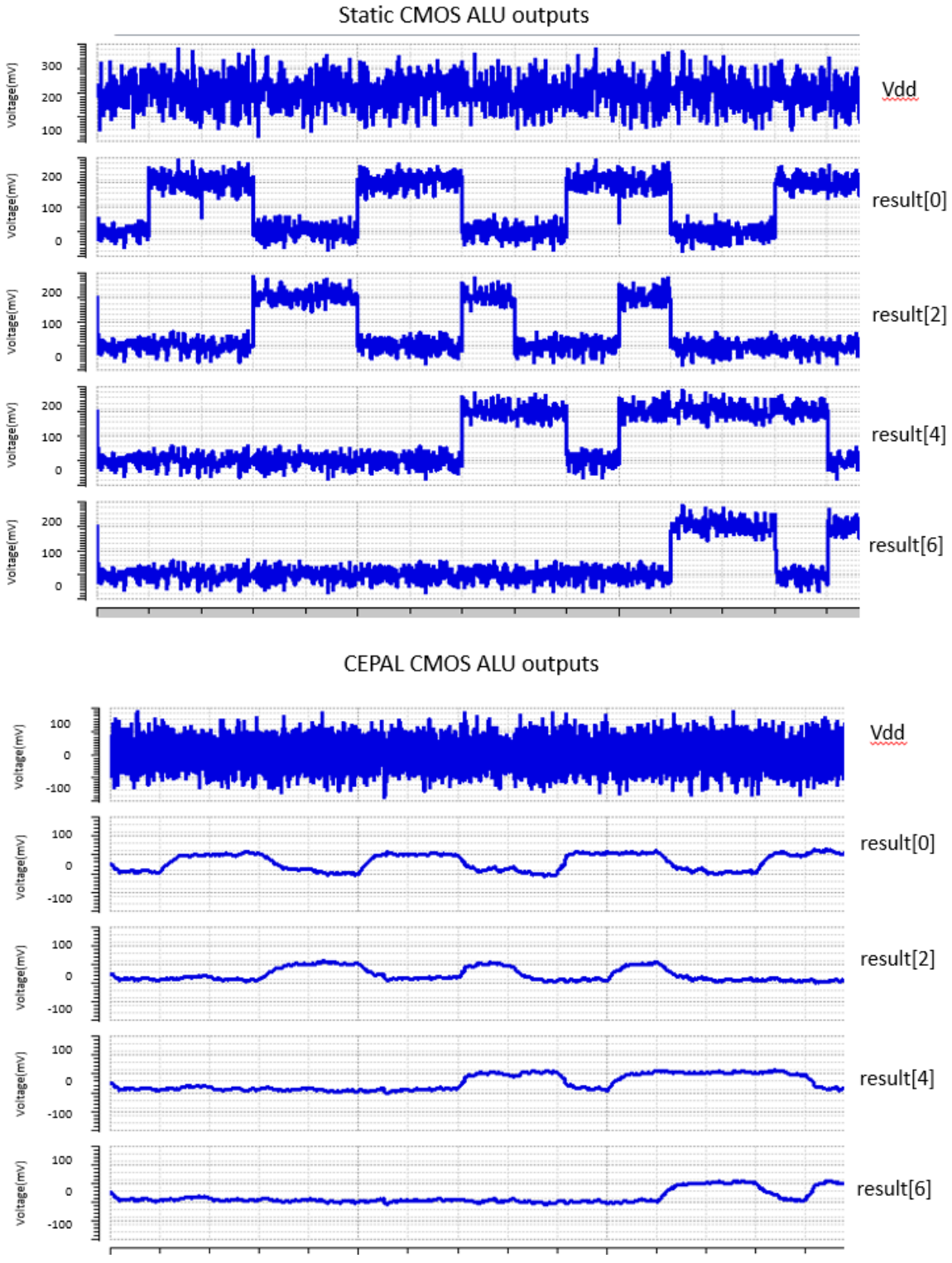

Fig. 17 ALU outputs when supply voltage is injected with additive noise

Table 7. Verification results for static CMOS and CEPAL ALU

	Static CMOS ALU	CEPAL ALU
Number of input vectors tested	78	78
Number of output sampled	780	780
Number of Outputs that is totally accurate	778	780
Number of input vectors that produces all 10 accurate outputs	76	78

Even though the sample case set is not large enough to fully verify the ALU outputs, we can still conclude that CEPAL exhibits better tolerance to high frequency noise than static CMOS. Although static CMOS still has high accuracy, CEPAL circuit yields 100% accuracy, at least in our test cases. Since CEPAL circuit uses two 5MHz power clocks as its supply power sources, the addition of noise of similar frequency does not change the power clock waveform significantly. Also, since CEPAL circuit has large delay at the output, the output might not be able to quickly follow the fast changing noise.

VII.A.2. Voltage Regulation Methods on High Frequency Noise

A simple way to reduce noise of a different frequency is to use filters. Filters can regulate the voltage and filter out noise with quite different frequency. Common filters include passive filter and active power filter. Active power filters exhibits better performance, better quality and sharp passband edge. However, in our case, where

power source is limited and we cannot find another stable power source to stabilize the devices, such as amplifiers, a passive filter might be a better choice.

For static CMOS, a low pass RC filter is good choice to regulate the voltage (Fig 18). By setting resistance R=1kOhm and capacitance C=50nF, the high frequency noise at power supply can be largely filtered out. In later simulation, we can see that by using the RC filter, we can approximately treat the system as it works without the power supply noise.

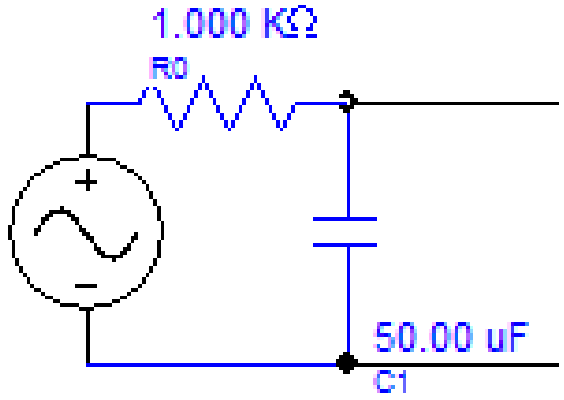

Fig. 18 Low Pass Filter that is used for the static CMOS

For CEPAL circuit, an ideal solution is to use a band-pass-filter to eliminate noise with frequency other than 5MHz. However, the band-pass-filter will bring in decay in the pass band and waste too much energy. Also, the decay will result in voltage decrease that makes the CEPAL ALU unable to function well. Thus, in this thesis work, we did not make a filter for the CEPAL circuit because of the difficulty to design one with little decay and small power loss.

VII.B. Pulse Noise Effect

VII.B.1. Pulse Noise Characteristic

Pulse noise is common in natural environment. A pulse noise could affect the supply power source of a chip by causing sudden disconnection between the source and the circuit, or just simply inject energy or induce energy loss to the circuit. In this part, we mainly studied the pulse noise effect on static CMOS and CEPAL ALU operation, and we mainly focused on pulse noise that produce sudden disconnection between the circuit and power supply.

To simulate such kind of noise, we used a voltage multiplier to produce supply power that goes through instant disconnection during the simulation period. The principle of the multiplier is given in Fig. 19. The first input of the voltage multiplier is the ideal supply voltage source with steady 200mV DC voltage for static CMOS, or 100mV AC voltage for CEPAL. The second input of the multiplier is a pulse voltage source that produce 1V DC voltage and occasional 0V pulse, which can act as a pulse coefficient for the ideal input voltage source. By multiplying the two inputs together, we can simulate a sudden disconnection during the simulation period. In addition, we used different pulse width to simulate short disconnection and longer disconnection for both of the circuits.

VII.B.2. Pulse Noise Simulation

Since the filters we used in the previous section shows better output result, we continue to use such designs when dealing with pulse noise.

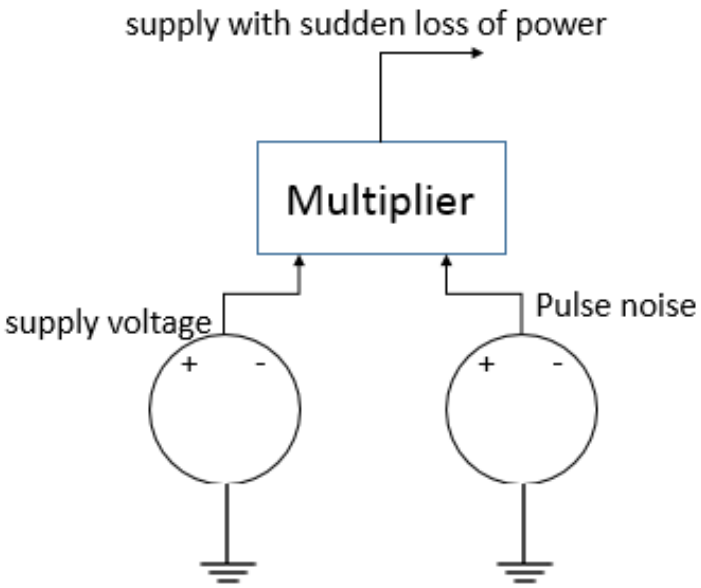

Fig. 19 Formation of the supply voltage with pulse noise

Results show that such pulse noise in the supply voltage has less impact on static CMOS circuit than CEPAL circuit when the low pass filter is utilized in static CMOS ALU. In the simulation, we tested pulse noise with pulse width 1 μs and 4 μs. From the results shown in Fig.20 and Fig. 21, we can conclude that with the low pass filter, the supply voltage for static CMOS can maintain stability, even though the maintained voltage level is lower than ideal V_{DD}, which stays at approximately 185~195mV instead of Vdd 200mV.

For CEPAL circuit, the output waveforms suffers obvious distortion. The situation for CEPAL gets worse when we enlarge the pulse width. If such pulse noise happens at evaluation phase of the circuit, the CEPAL ALU will produce neutral output that stays at around 0mV. Even though once the pulse disappears, the CEPAL ALU can recover to normal output in a short time, such neutral output will leave the output in

ambiguous state.

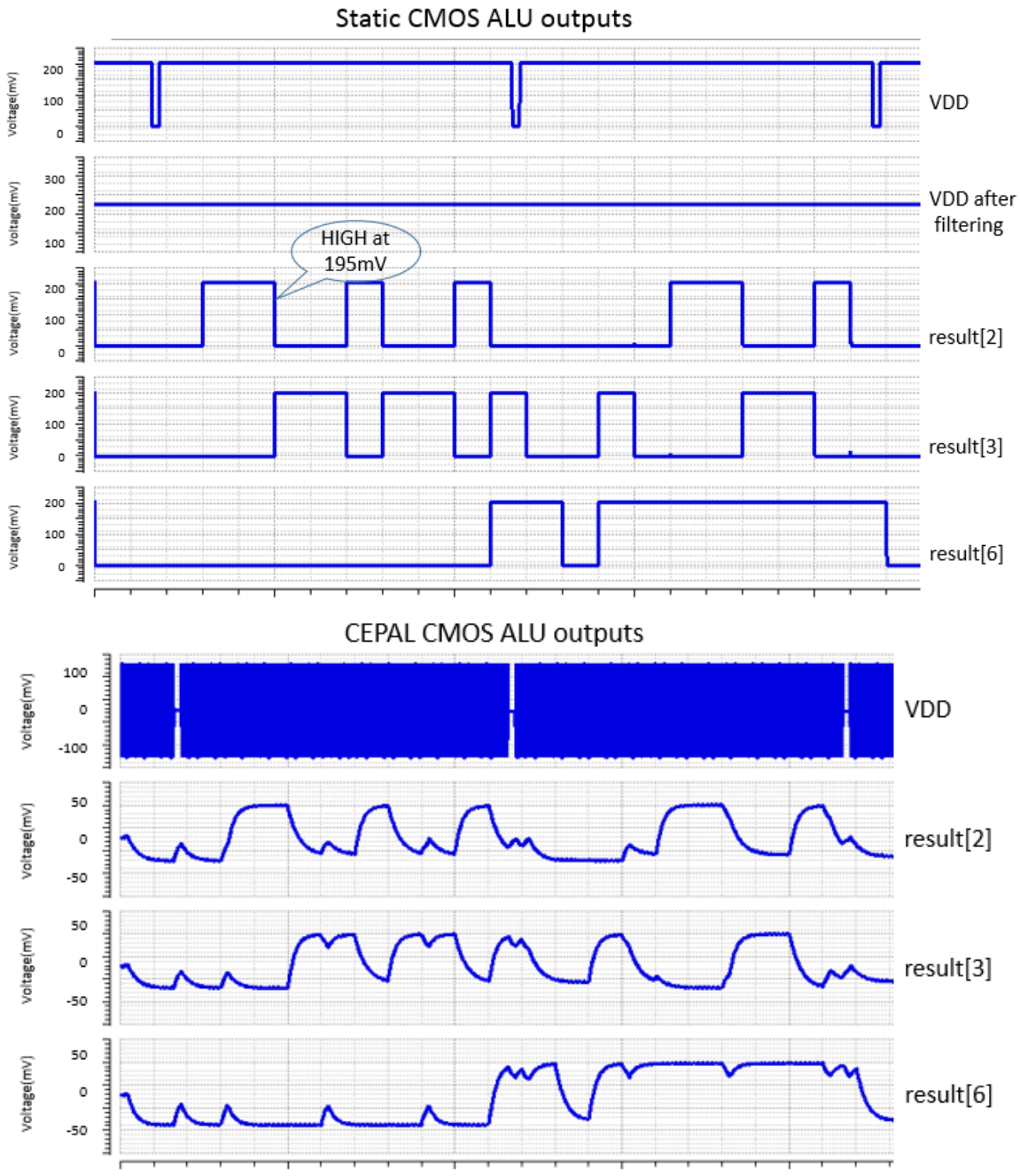

Fig. 20 ALU outputs with 1us power loss in pulse noise

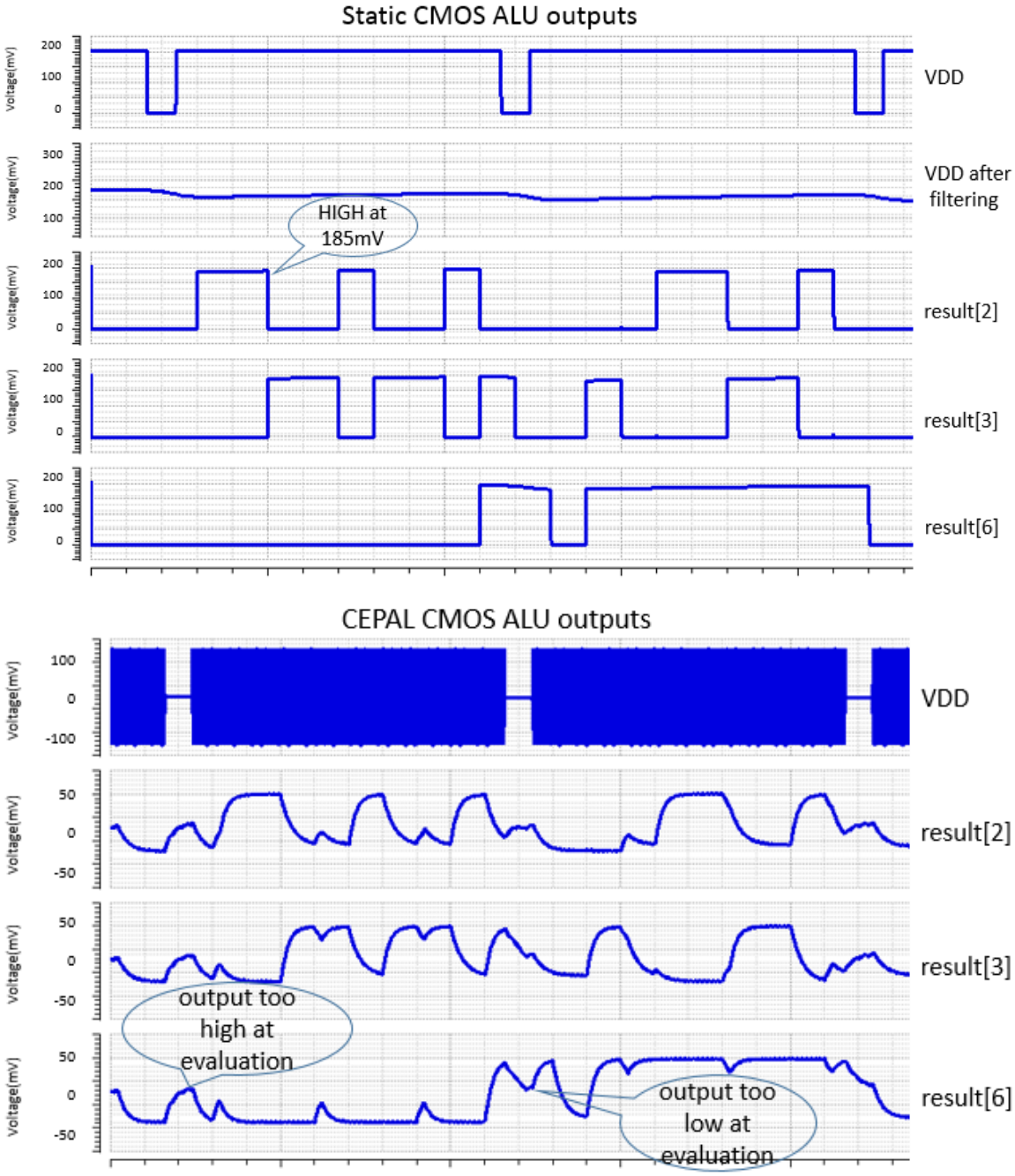

Fig. 21 ALU outputs with 4us power loss in pulse noise

VII.C. Low Frequency Noise Effect

For energy harvesting system, it is common that the energy source is unstable and the energy it can harvest varies from time to time. Minor environmental changes that take place at a low frequency could result in fluctuation in the supply voltage. To bear such fluctuation and maintain good output is essential for wireless system working under energy harvesting. We also simulated situations where low frequency noise affects the energy harvesting system.

Unlike the high frequency noise which comes from additive noise and produces offset to the supply voltage, we suppose the environmental changes in low frequency acts as coefficient to the supply voltage, like what we do in pulse noise simulation. We used voltage multiplier again and set the coefficient fluctuates between 0 and 2 and made its average at 1. We considered noises of frequency from 30Hz to 400Hz and enlarged the simulation length for both types of circuit to 30ms.

The simulation results of static CMOS is given in Fig. 22 and Fig. 23, and the results for CEPAL are given in Fig. 24 and Fig. 25.

From the simulation, we can see that, by using a 50uF large capacitor in the RC filter, the supply voltage of static CMOS can again maintain at a stable level. The volume of the 50uF capacitor might be as large as a piece of finger nail. Even when the supply voltage drops to a critically low level that is around 0mV, the output can still maintain at desired level (Fig. 22). This is because the capacitor has filtered out the noise. The large capacitor can store the excessive charge and give it out when the voltage is too low. This will help balance the voltage level and keep it stable.

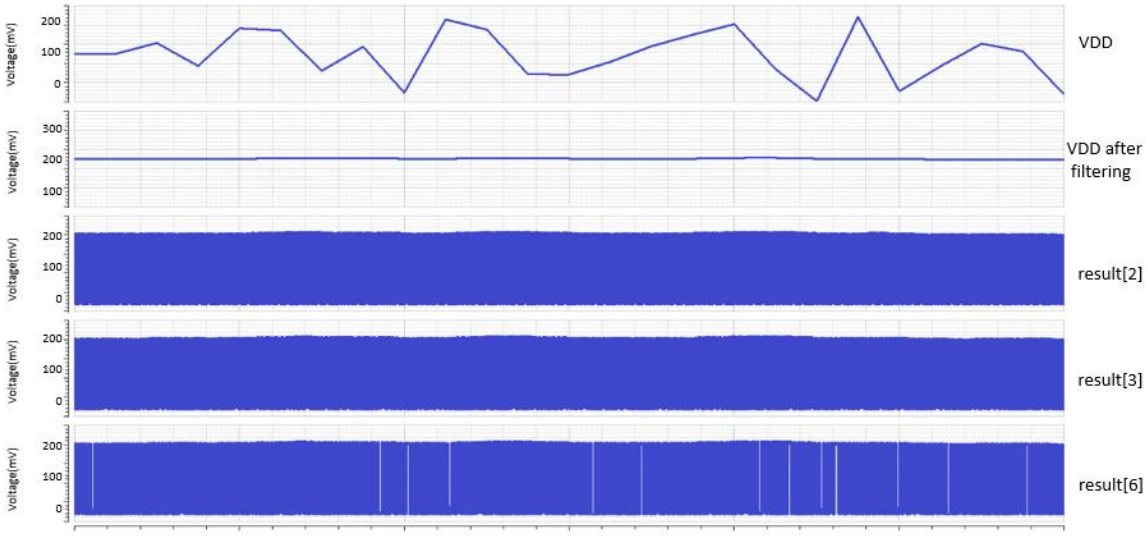

Fig. 22 Overall view of static CMOS simulation in low frequency noise

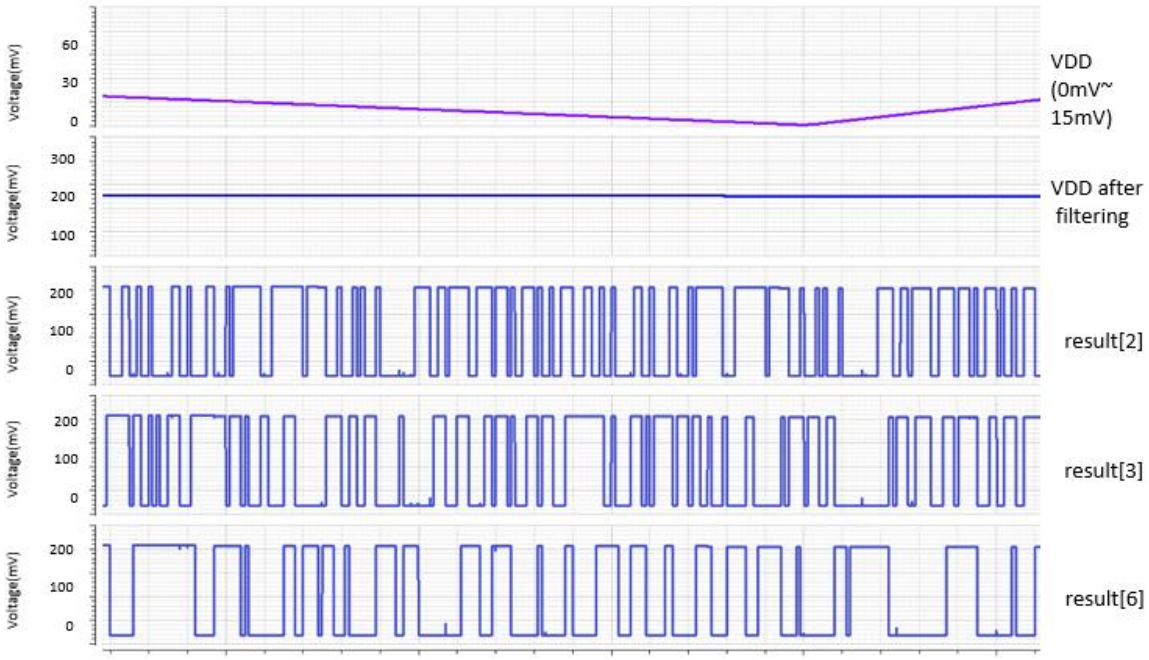

Fig. 23 Static CMOS got good outputs when V_{DD} reaches 0~15mV

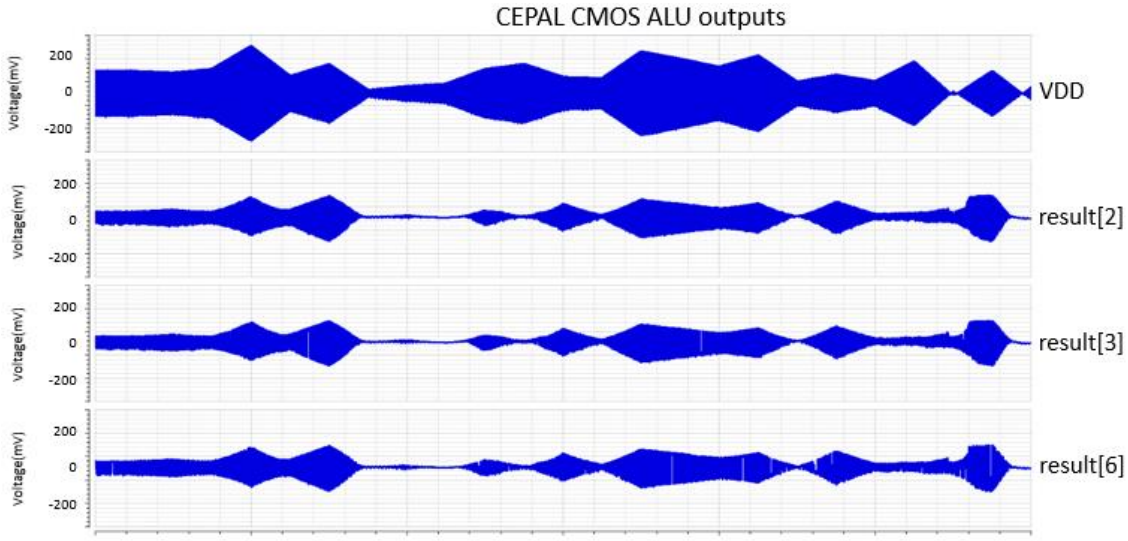

Fig. 24 Overall view of CEPAL simulation in low frequency noise

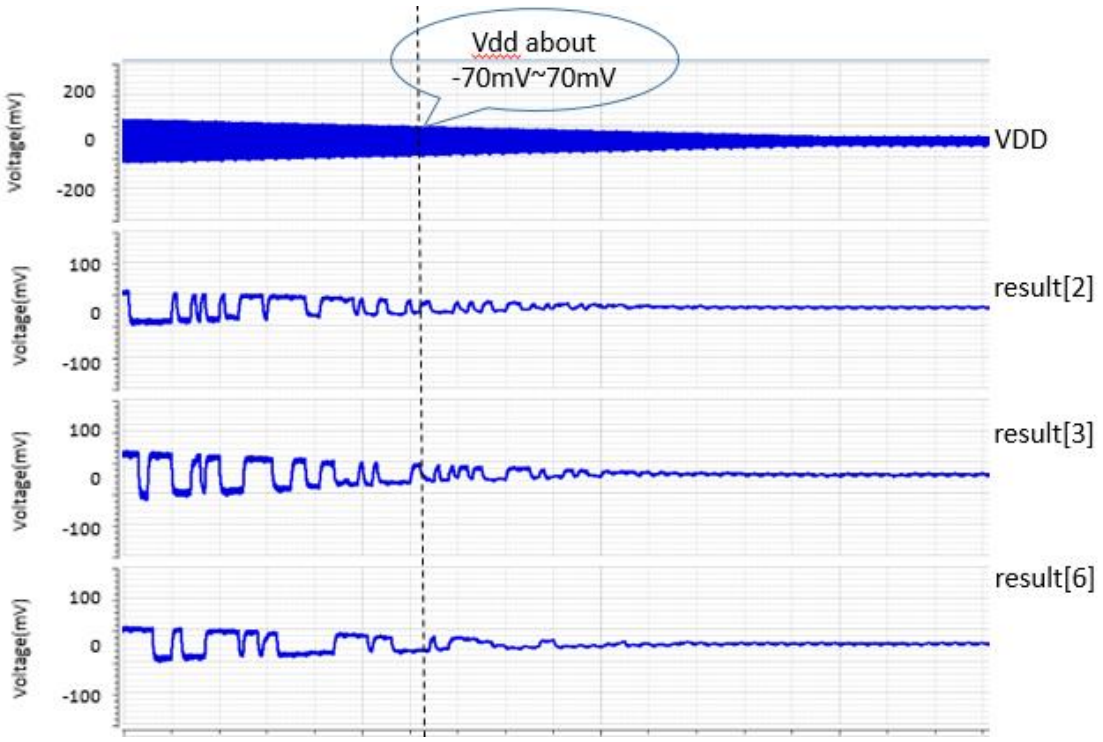

Fig. 25 Bad outputs given y CEPAL ALU as the voltage level scales down
But for CEPAL, we are unable to utilize capacitor to store energy and consume it

while it is needed, since it uses AC power. Thus, the output for the CEPAL circuit is highly dependent on the instantaneous voltage level. From Fig. 24 we can see that, since the voltage fluctuation is so large that CEPAL cannot maintain good output, especially when the supply voltage goes down to near 0mV.

At the time when the original voltage source fluctuates to a low level, the output of the static CMOS ALU maintains at around V_{DD} level for HIGH or 0mV level for LOW, which makes good waveform shape. But for the CEPAL ALU, the output gains much less voltage swing when supply voltage amplitude scales down. When the amplitude scales down to around 70mV (the original input voltage amplitude is 100mV),

CEPAL ALU produces poor outputs such that the output HIGH and LOW are too close. Such kind of output often leads to incorrect computing results.

VII.D. Long Time Energy Loss Effect

When the energy harvesting system cannot produce enough power due to long time harsh environment, the ALU might need to work with even lower supply voltage. This part will generally simulate situations where the supply power is even lower than what we previously simulated. Through this process we can find the minimum voltage under which the ALUs can function properly. Instead of running single simulations with power sources influenced by noise, we simulated with constant power source but with lower voltage amplitude. The related simulation results is given in Fig. 26 and 27.

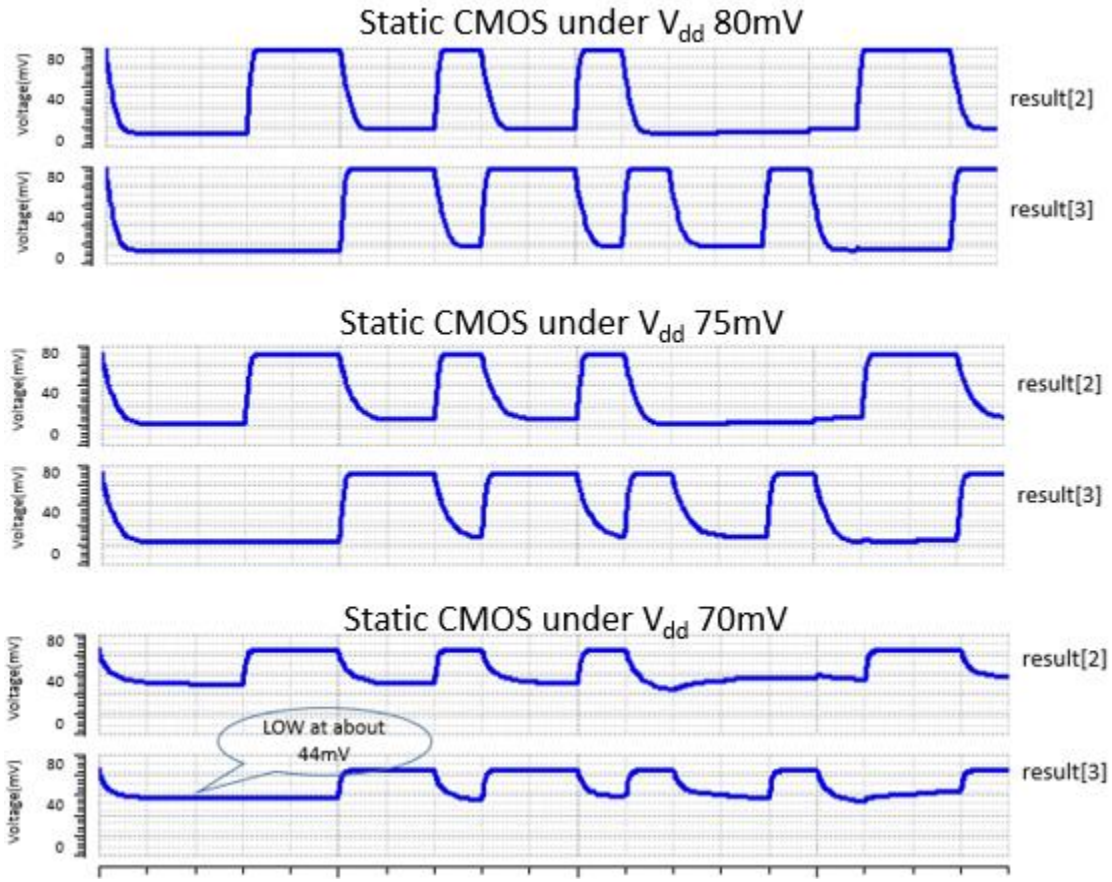

Fig. 26 Outputs given by static CMOS ALU working under different low voltages

For static CMOS circuit, when the supply voltage is as low as 70mV, the output LOW will become abnormally high, which resembles the previous high LOW output phenomenon in the 125 ℃ sub-threshold simulation. While operating above 75mV, the output maintains good quality. For CEPAL circuit, the supply voltage amplitude cannot go far below 100mV. When reaching -90mV~90mV, the output LOW rises to above 0mV, which lays in the HIGH voltage margin. The output HIGH also drops down to several millivolts, which will make a small output swing. Such unstable output will not guarantee an accurate output.

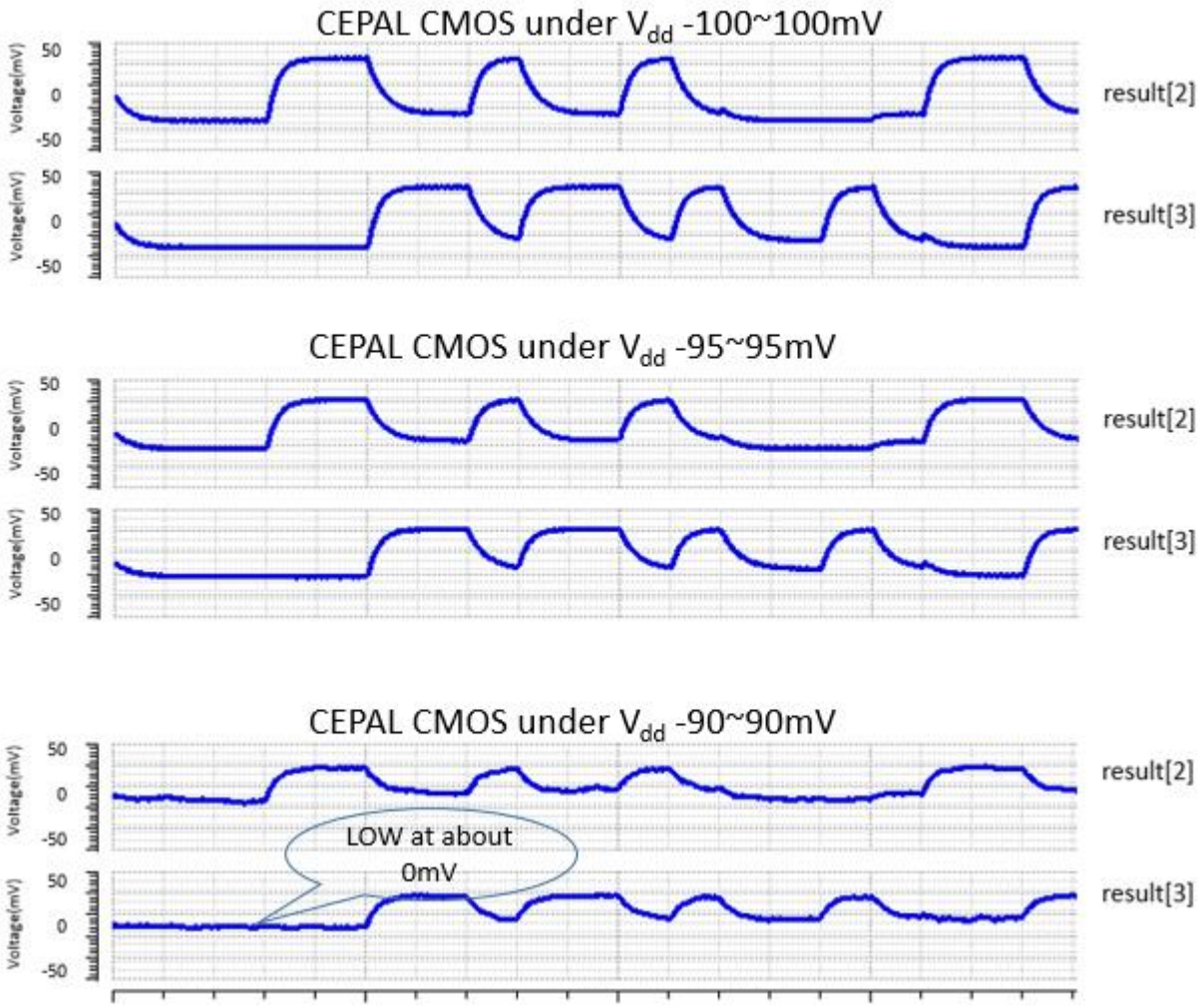

Fig. 27 CEPAL ALU working under different low voltages

In conclusion, the static CMOS ALU can function with 125mV (200-75) reduction in the supply voltage, while the CEPAL ALU can only endure less than 20mV (200-180) reduction in the supply voltage fluctuation.

VIII. CONCLUSIONS AND FUTURE WORK

This thesis mainly studied two kinds of low-power design methods, near/sub-threshold computing and adiabatic logic style design. The objective of the research is to compare these two kinds of circuits' characteristics in wireless remote system where the supply energy is limited and the environment is harsh. The application of energy harvesting technique allows wireless system to operate without electric power source, and makes low-power design necessary in such kind of system.

Near/sub-threshold region computing circuit is first introduced. By lowering the supply voltage to near-threshold or sub-threshold level, we can still obtain accurate logic output with very small power consumption. Along with the scaling of the supply voltage, the circuit delay becomes higher.

Adiabatic logic style is a kind of circuit that can reduce power dissipation. By giving the stored energy back to the supply, adiabatic circuit can save portion of the dissipated power back to the voltage source. Complementary energy path adiabatic logic (CEPAL) circuit is mainly studied in this thesis as the representative of adiabatic logic circuit. We compared CEPAL with static CMOS circuit in the aspects of power consumption, delay, temperature variation tolerance and power noise variation tolerance.

We designed a static CMOS ALU and a CEPAL ALU with the same netlist. The result shows that, at near-threshold region (200mV), these two ALUs show similar power dissipation, while CEPAL ALU suffers much larger circuit delay.

In the aspect of temperature variation, CEPAL circuit is more sensitive in high temperature. Also, output swing become significantly smaller as temperature rises high. Static CMOS shows much more stability in this comparison, which makes it a favorable approach. Further study on static CMOS in sub-threshold region shows that even when operating in sub-threshold region, the delay, output accuracy and power consumption of static CMOS is better than CEPAL circuit in near-threshold region. Regarding power noise tolerance, different kinds of noise impact were tested on the two ALUs. CEPAL ALU shows better accuracy when dealing with high frequency noise. But it is much easier to design a filter for the static CMOS ALU to eliminate noise. As for pulse noise and low frequency noise, static CMOS ALU with the low pass filter shows much better robustness while CEPAL ALU tends to have abnormal output. For low supply voltage comparison, CEPAL ALU can only work 20mV away from the specification of 200mV voltage while static CMOS can go as low as 75mV. Static CMOS also shows much better noise tolerance than CEPAL.

Overall, although at 200mV of supply voltage (swing), static CMOS and CEPAL consumes similar power, the delay, variation tolerance for static CMOS circuit is much better than CEPAL circuit. The result indicates that static CMOS is still more favorable in low-power design and adiabatic technique might only be practical in super-threshold computing.

Future work could be focused on finding ways to optimize CEPAL circuit or other adiabatic logic circuit in reducing its delay, power dissipation and improving robustness. Other circuit styles such as RAMs, pipelining and clock generating circuit

also needs to be studies as they are also important part of a system design. In the transistor level, modification in the design parameters, could also be a chance to gain better performance in near/sub-threshold region.

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