

THE NEW ACTIVE OUTPUT FILTER FOR VARIABLE SPEED CONSTANT
FREQUENCY AEROSPACE APPLICATIONS

A Thesis

by

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ABSTRACT

A concept called “Active Output Filter” (AOF) for performing output filtering in switching converter is proposed. The methodology is based on voltage harmonic injection via a combination of H Bridge and minimized LC filter to cancel out the odd harmonics from a 400Hz square wave 3 phase inverter to achieve a pure sinusoidal output with modulation index of 1.27. Investigation reveals that AOF allows a substantial size reduction and gives competitive efficiency, as compared to passive inductor capacitor filter. Moreover, the main square wave inverter has a capability to regulate the output voltage depending on the Load requirements providing a wide range of modulation index. The operation principle of the concept is demonstrated for Variable Speed Constant Frequency (VSCF) high power aircraft application. The exploration lays a foundation for further investigation into the use of AOF concept for other power electronic converter systems.

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1. INTRODUCTION AND LITERATURE REVIEW

1.1 Introduction

The design of a conventional civil aircraft consists of a combination of systems: mechanical, pneumatic, hydraulic, and electrical systems. These systems have several drawbacks, such as low efficiency and difficulty in detecting leaks in a pneumatic system; the use of gearboxes in a mechanical system; heavy, inflexible piping; and the potential leakage of dangerous and corrosive fluids for the hydraulic system. The concept of the More Electric Aircraft (MEA) has been introduced to overcome some of the drawbacks found in conventional architectures and bring more attractive advantages, such as more electrical capacity, better efficiency improved fuel consumption, and lower maintenance and operation costs and improved safety as well as reliability [1-2].

The MEA revolutionary idea is expected to drive modern aircraft power system industries towards a more efficient, reliable and compact electrical system. MEA based airplanes deploy several voltage levels composed of a combination AC and DC Sub-systems. Those MEA subsystems are mainly in the form multi-converter power systems utilizing power electronics and transformers conversion stages. Modern aircrafts consists of four major AC and DC voltage levels: 405VAC (variable frequency), 200VAC, 28VDC and 270VDC. The main electrical generation source in airplanes is supplied from two or more engine-driven-generators to feed the AC. All aircraft systems needs a mixed AC and DC power altogether. The DC power comes from rectification of the AC power using transformer rectifier units (TRUs) based on 12-pulse configuration [3-5].

The traditional constant speed drive (CSD) generating system used in several aerospace applications since 1945 [16]. It is composed of a regulated synchronous generator, the output frequency of which is maintained constant by means of a hydro-mechanical drive CSD system connecting it to the engine via a gearbox mechanical interface [1].

One possible approach to decrease the weight and volume of the system is introduced by an integration of the drive and the generator integrated into a single unit, thereby providing the integrated drive generator (IDG) [2]. However, Towards MEA topology as well as continuing developments in power electronics the DC-link variable-speed constant-frequency (VSCF) generating system, becoming a feasible replacement to the CSD and IDG systems. Unlike CSD/IDG, The VSCF electrical system is more flexible since its components can be distributed throughout the aircraft while CSD/IDG mechanical system must unavoidably be located close to the engine [5].

1.1.1 Need of compact and light weight system

Power density of energy conversion systems is one of the most crucial factors in aerospace applications; this is the motive behind using 400Hz power systems on planes rather than conventional 50, 60Hz. important equipment occupying less space in an aircraft or space shuttle will result in increased functionality within a limited space as long as maximizing the performance. Moreover the development of the aircrafts in the past few decades results a larger electrical capacity as shown in Figure 1

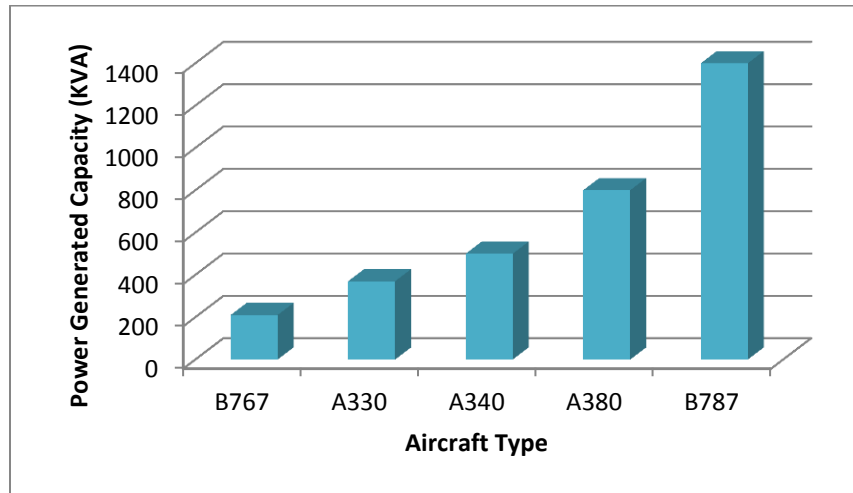


Figure 1 Commercial aviation electrical power systems and infrastructure market: aircraft electrical power generating capacity by aircraft type [5]

Higher Power Capacity within a space constrains require higher voltage levels. Thereby, the aircrafts Electrical System Designers Tends to increase the voltage levels to allow more electrical loads to be added to the system as illustrated Figure 2 and that add a significant need to optimize the size and weight of all aircrafts equipment's.

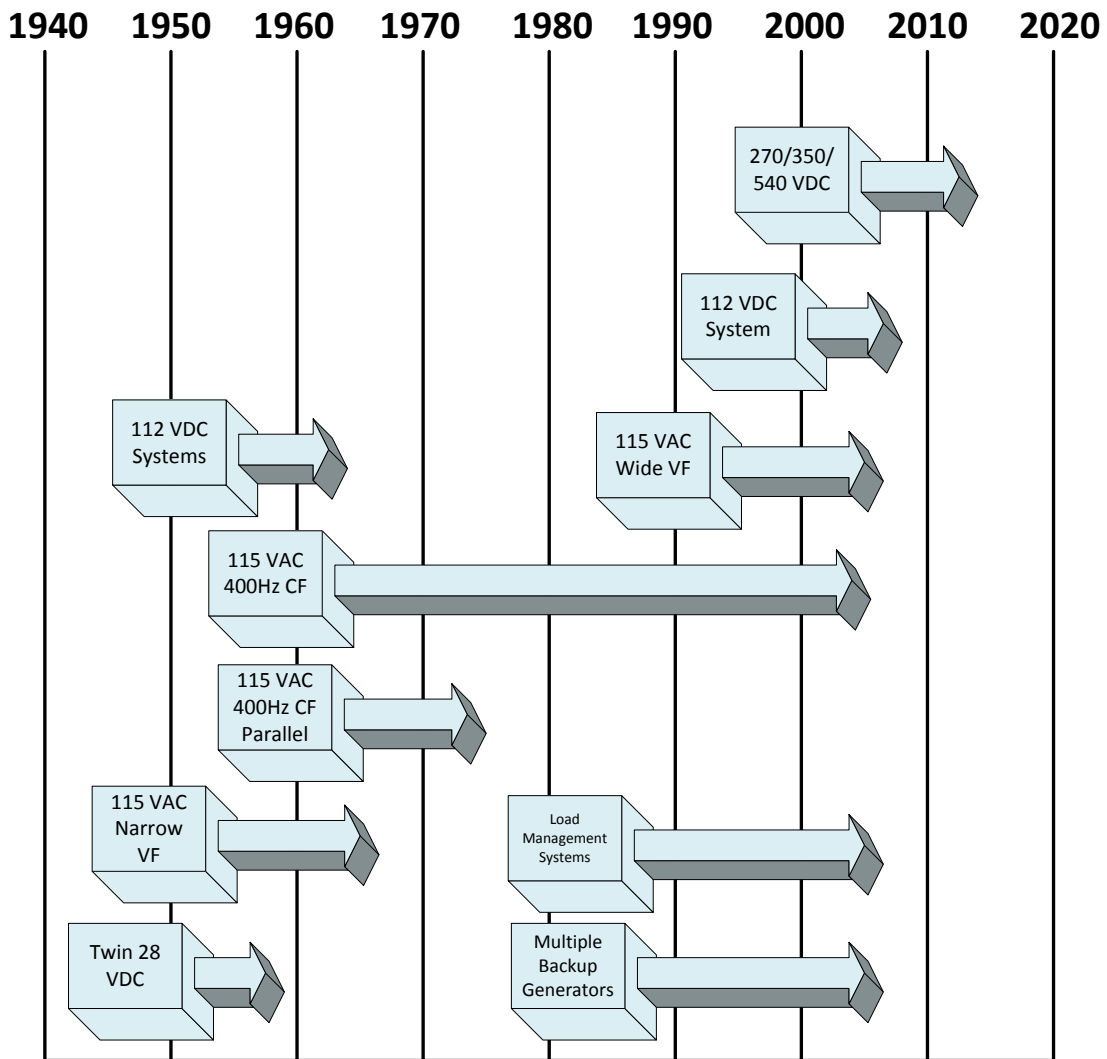


Figure 2 Aircrafts electrical system development [6]

Similarly, offshore drilling rigs are now built in deeper waters with depths of up to 7000ft and have to operate in severe conditions [7-8]. Thus, support structures are needed for these rigs to ensure equipment's safe and reliable operation. Consequently, the equipment needs to be lightweight, for the subsea structure to provide stability. In

order to improve the petroleum production, it is desired to have more functionality within a narrow space.

Likewise, it is desired to have shipboard systems such as battle cruiser, aircraft carriers and naval vessels to become as compact as possible and reduce the amount of energy spent in navigating with other heavy equipment. Especially, that the cost of generating electricity at sea is higher than the cost of electricity produced by land power plant's [7-8]. Therefore, any reduction in size or weight is saving on cost of electricity. At the same time, such shipboard systems would like to have compact systems to house other major equipment. Thus, a lot of efforts are being put to develop strong composites which will replace heavy materials as steel in aerospace applications, on offshore platforms for drilling and shipboard systems [8-9].

1.1.2 Need for compacts VSCF

After the MEA Revolution the aircrafts electrical system has an increased value contribution up to 14 % of the total commercial aviation market as illustrated in Figure 3 [4]. Therefore the importance of electrical systems forces the development of power generation and power distribution systems. In case of power generation system, VSCF's systems are vital stage systems due their ability to manage the full generated power delivered by each jet engine respectively. Thus, its design criteria's must be selected strictly. Moreover, any improvement in power density, efficiency or power quality is also considered to be vital in Aerospace applications.

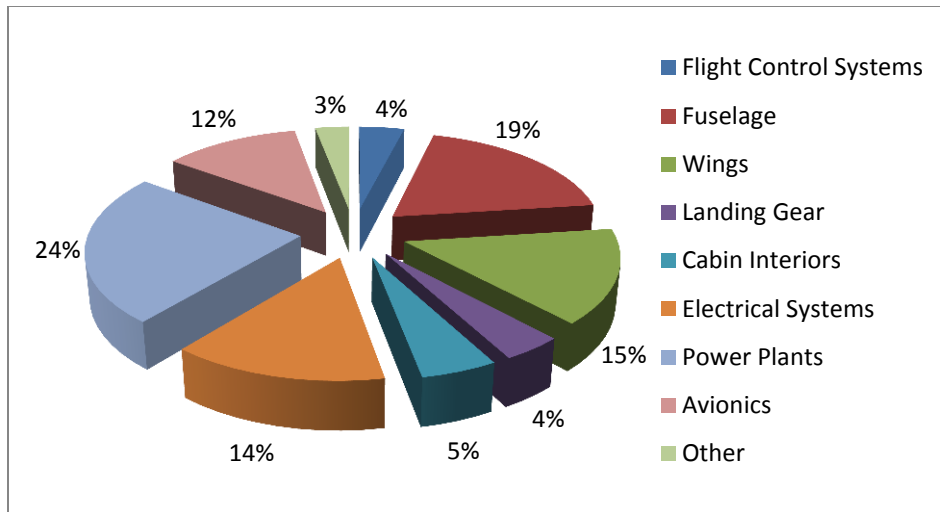


Figure 3 Commercial aviation electrical power systems and infrastructure market: aircrafts systems value contribution, 2007 [4]

1.1.3 Research objective

The goal of this study is to propose and analyze an Active Output Filter (AOF) which will replace the bulky passive output L-C filter suitable for high power applications such as Variable Speed Constant Frequency units in Aerospace applications having weight and size constraints. A 3 phase diode rectifier stage followed by The Direct Current (DC) link capacitor converts the generated power from AC to DC. Then the DC voltage in turns converted to 400Hz constant frequency AC Voltage via inverter stage to supply the aircraft loads.

To improve output Total harmonic Distortion a passive output LC filter stage is deployed to remove switching frequency harmonics generated by the inverter offering a low Total Harmonic Distortion (THD) output voltage. The Size of this Passive LC-Filter is forced to be bulky due to inverter switching frequency constrains incorporated

by high power generation output that can reach up to 250KVA in case B787[2]. Thus, lowering the L-C filter size will result in degrading the output voltage quality and incorporated undesired harmonics in the system.

The proposed topology involves adding 3 Active output filter (AOF) blocks to the inverter in which each AOF blocks contains of H Bridge, minimized LC filter and DC link. As a result, the main inverter switching frequency is lowered down to the fundamental 400Hz frequency which incorporates a boost in efficiency.

Moreover, the processed power is divided into the 3 AOF blocks since that their rating is $1/3$ p.u and that enables very high switching frequency capabilities incorporated by AOF's H bridge. With very high switching frequency i.e. 200 KHz the AOF's L-C filter will significantly minimized and the overall passive components power density will be reduced compared to the conventional 3 phase inverter topology.

Unlike to 3 phase inverter each AOF block is a single phase unit capable of unipolar scheme in which the harmonics start to appear at twice switching frequency instead of the switching frequency and that features a better quality filtration advantage. Moreover, more efficient switches i.e. GaN, SiC and MOSFET can be employed instead of IGBT's due to lower applied voltage and power rating as wells as lower power density switches up to 80% smaller than silicon based devices[10]. In addition, the voltage stress of the filter inductor will be reduced to $1/3$ which will reduced the inductance and the core size even more.

Furthermore, the nature of AOF blocks involves a voltage injection stage after a 3-phase six step inverter stage enabling a modulation index up to 1.27 that also allow a

lower main DC-Link Applied Voltage. The Proposed topology have been tested under balanced, unbalanced and nonlinear load condition and it's proves it's feasibility under different loading conditions.

Also, Voltage control have been applied to the main inverter offering a regulated load voltage using two different PWM methods: Selective harmonic Elimination Pulse Width Modulation (SHEPWM) and Space Vector Pulse Width Modulation (SVPWM).

1.2 Literature review

1.2.1 Electrical power system (EPS) architecture

Traditional airplane electric power system (EPS) often composed of two or more jet engine-driven generators to supply aircraft electrical loads needs. Since that engine driven-generators are solely connected to the distribution buses in some modern aircraft almost all American and European air forces use the parallel connection structure due it's high reliability and efficiency. In parallel connection structure, the main generators bus bars are connected together through Bus-Tie Breaker [6]. In the event that one generator should fail it is automatically isolated from its respective bus bar and all bus bar loads are then taken over by the operative generator to ensure optimum possible performance. If both generators fail, the batteries will automatically supply power to only the essential loads and keep them operating for a pre-specified period depending on load requirements and battery condition. In conventional aircraft system, the synchronous generator supplies AC voltage at fixed frequency to feed the AC loads [6]. AC/DC conversion stages based rectifiers are used to convert the AC voltage with

constant frequency at the main AC bus to several DC voltage levels at the secondary buses which supply electrical power to DC loads as shown in Figures 4.

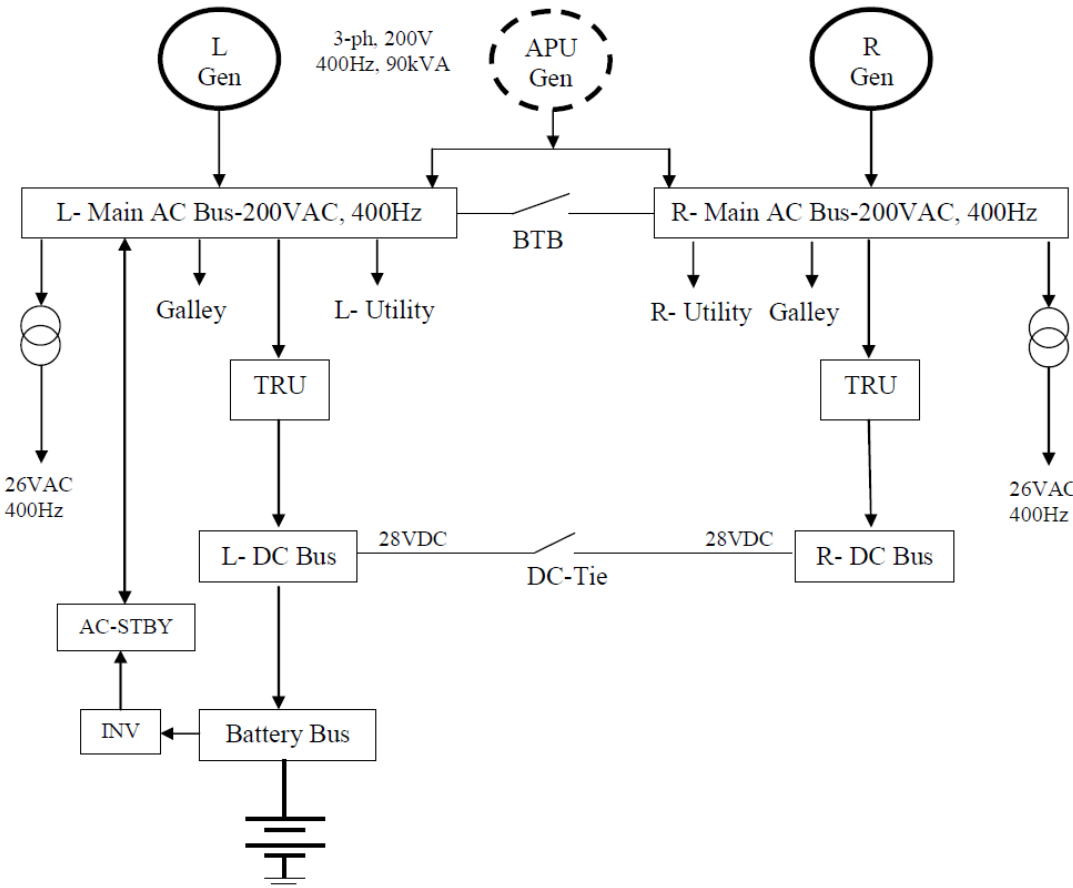


Figure 4 Conventional B767/A320 aircraft power distribution system. (© 2008 IEEE [1]- Adapted with permission)

The main parameters of the Electrical Power System (EPS) are as follows:

- a) Main engine generator: IDG, 3 Phases, 115/200V, 400Hz, 90KVA
- b) APU: 3 Phases, 115/200V 400Hz, 90KVA
- c) EXT Power: 3 Phases, 115/200V 400Hz
- d) RAM Air Turbine (RAT): Single Phase, 115/200V 400Hz, 5kVA
- e) Static Inverter: Single Phase, 115V 400Hz, 1kVA
- f) Transformer Rectifier Units (TRU): 28V 200A
- g) Battery: 28V, 23Ah

1.2.1.1 Main generators and (apu) generator

The two aircrafts' jet-engines drive the two 3-phase AC main generators (GEN1, GEN2) on A320 through an integrated drive method. Each generator can provide up to 90kVA electrical power at 115/200V and 400Hz. The Auxiliary Power Unit Generator (APU GEN) is driven directly by the APU and can provide the same electrical power as the main generators, and can act as the substitution of either or both main generators at any time for safe landing. A Generator Control Unit (GCU) can respectively control the output of each generator. The primary functions of GCU are as follows [6]:

- a) Control and regulate the frequency and voltage of the GEN output
- b) Protect the power network by controlling the associated Generator Line Contactor (GLC)

1.2.1.2 External power (ground power)

For long periods of aircraft operation on the ground, a supply of power is needed for maintenance and testing. Ground power can be generated by means of a motor-generator set. The usual standard for ground power is three-phase 200VAC 400 Hz, which is the same as the aircraft AC generators. The Ground Power is provided for specially appointed aircraft systems, while other systems will not be powered. A Ground Power Control Unit (GPCU) can provide protection for the network by controlling the external power contactor [5-6].

1.2.1.3 Emergency generator

In case both main generators and APU generator fail, the blue hydraulic circuit drives an emergency generator which can automatically provide emergency AC power for the aircraft electrical system. This generator can produce 5kVA of 3-phase 115/200V 400Hz electrical power. There is a corresponding GCU to perform the following functions [6]:

- A) Regulates the emergency generator at a constant speed
- B) Regulates the output voltage of the generator
- C) Controls the emergency generator line contactor to protect the network
- D) Control the start-up of the emergency generator

1.2.1.4 Static inverter

The static inverter transforms 28V DC power from Battery1 into 1kVA of single-phase 115V 400Hz electrical power, which is then transferred to the AC essential bus. If

only the batteries are providing electrical power to the aircraft, disregarding the pushbutton positions of the BAT1 and BAT2, when the speed of the aircraft is above 50 knots, the inverter will be automatically activated. When the speed of the aircraft is below 50 knots, if only the batteries are providing electrical power to the aircraft, and the BAT1 and BAT2 pushbuttons are both on at auto position, the inverter will also be activated [6].

1.2.1.5 Transformer rectifier units

There are two transformer rectifiers, TR1 and TR2, to provide up to 200A of 28V DC power for the electrical system on board. When the main engine generators and the APU generator all fail, or if either TR1 or TR2 fails, the ESS TR can supply the essential DC network from the emergency generator. Every TR can control its own contactor by internal logic [6].

1.2.1.6 Batteries

There are two main batteries, each one with a normal capacity of 23Ah. Both of them are permanently connected to the two corresponding buses. Each battery has an associated Battery Charge Limiter (BCL) to detect the charging status and to control the battery contactor.

1.2.2 More electric aircrafts

Development in power electronics, control systems, motor drives, and electric machines helped in discovering new technologies of the VSCF system. The main advantage of MOE system is that it offers better starter /generator systems, higher reliability, lower maintenance costs. In addition higher efficiency can also be achieved especially that 400Hz aircraft systems involves more passive elements losses than 60Hz systems. VSCF systems employ an AC three-phase synchronous generator and solid state converters. Each solid state converter consists of:

- (a) Rectifier Unit: which converts a variable frequency AC voltage into DC
- (b) Intermediate circuit: Including DC-Link Unit
- (c) Inverter: Converts the DC into three-phase AC constant frequency voltage.

The configuration of a typical variable-speed constant-frequency starter/generator system [11-12] is operating in generation motoring modes. In the motoring mode, the constant frequency AC system, via the bi-directional power converter, provides input electric power to the electric machine which acts as a starter to the aircraft engine. On the other hand, during generating mode of VSCF system, the aircraft engine rotating in a variable speed, provides mechanical input power to the electric generator. The electric generator then supplies variable frequency AC power to a (bi-directional) power converter which provides AC fixed frequency voltage to the main bus[5].

1.2.3 Aircrafts power generation sources

The electrical power systems of aircrafts have been significantly improved in latest years towards increased dependency of electricity as was illustrated in Figure 2 . The voltage 28 VDC was the conventional EPS from the starting of forties to the starting of the fifties [13]. There were either one or two DC batteries to support the critical loads during an emergency.

The 200VAC at 400Hz constant frequency (CF) aircraft system started on the beginning of the sixties to supply the AC Loads. The variable-frequency (VF) generators appeared since nineties and the load management systems and backup generators. Finally, Variable-speed constant-frequency (VSCF) aircraft appeared on 2000 and continues until today.

This VSCF aircrafts contains a constant DC bus of 270VDC and for feeding AC loads; three-phase inverters are used.. The generation power rating of Boeing and Airbus increased continuously over the years until it reaches 0.8MVA for Airbus A380 while it reaches 1.4MVA for Boeing B787 as shown in Figure 1. Different aircraft power ratings with their used technologies [5] are listed in Table 1. These aircraft systems are highlighted as follows. More detailed explanation of CSD, IDG, VF and VSCF need to be realized to obtain the reason behind proposing the VSCF topology to the aircraft industry.

Table 1: Civil/military aircraft and electrical power generation techniques [5]

Generation Type	Civil Application		Military Application	
IDG/CF [115VAC/400Hz]	B777	2×120kVA		
	A340	4×90kVA		
	B737NG	2×90kVA		
	MD-12	4×120kVA		
	B747-X	4×120kVA		
	B717	2×40kVA		
	B767-400	2×120kVA		
	Do728	2×40kVA		
VSCF (Cycloconverter) [115VAC/400Hz]			F-18E/F	2×60/65kVA A
VSCF (DC Link) [115VAC/400Hz]	B777(Backup)	2×20kVA		
	MD-90	2×75kVA		
VF [115VAC/380-760Hz Typical]	Global Ex	4×50kVA	Boeing JSF[X- 32A/B/C]	2×50kVA
	Horizon	2×20/25kVA		
	A3XX	4×150kVA		
270VDC			F-22 Raptor	2×70kW
			JSF[X- 35A/B/C]	2×50kW

1.2.3.1 Constant speed drive

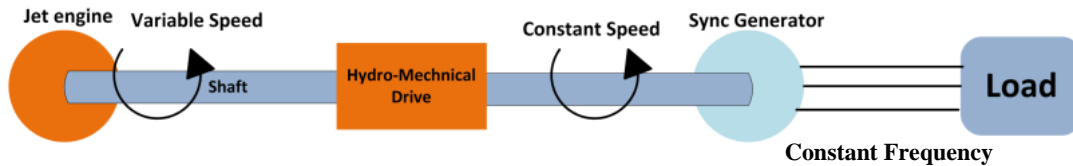


Figure 5 Constant speed drive

Constant Speed Drives (CSD) shown in Figure 5 has been implanted to provide a mechanical interface block between the variable speed input jet engine and a 400Hz synchronous generator that directly supply the 400Hz Sinusoidal Load as expressed in [14]. The mechanical interface is basically a hydro-mechanical variable-ratio drive that couple the jet-engine shaft to the synchronous generator via stages of gears and hydraulic cylinder block common to both pump and a motor. And these stages help to regulate the jet-engine speed to the required generator constant speed.

Though CSD delivers a constant 400Hz frequency output it suffers from several disadvantages such as:

- Low efficiency range from 74%-79% [16].
- The size and weight of the CSD system is high.
- The hydro-mechanical coupling and the synchronous generator has to be placed next to each other's.
- Frequent Maintenance Required.

Towards the improvement of CSD, an Integrated Drive Generator (IDG) have been introduced

1.2.3.2 Integrated drive generator

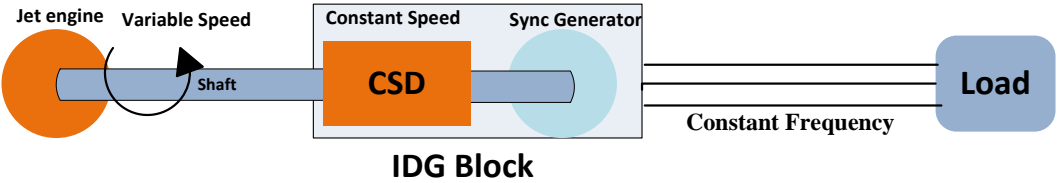


Figure 6 Integrated drive generator block diagram representation

Integrated Drive Generator (IDG) expressed in Figure 6 is a combination of the CSD and the oil cooled generator into a single compact unit sharing the same case. This configuration requires less space, and reduces weight and vibration when compared with the CSD configuration [1].

Continuing developments in both power electronics and microprocessor technology have led to the dc-link Variable-Speed Constant-Frequency (VSCF) generating system and Variable Frequency system (VF) which becomes a viable alternative to the CSD and IDG systems.

1.2.3.3 Variable frequency

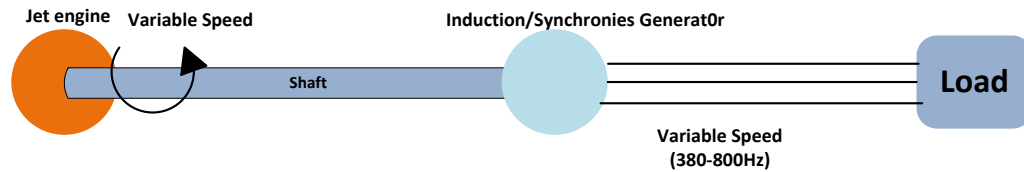


Figure 7 Variable frequency configuration

The Variable Frequency (VF) generator can be driven by the engine directly via Synchronous, induction, and switched reluctance machines and can supply the variable frequency (generally 380~760Hz) power to airframe systems without the aid of complex mechanical conversion equipment's [17] as shown in the above Figure 7.

The main advantages of the VF technology are: cost saving and reliability improving. However the disadvantages of the VF generator are also obvious. Much AC equipment cannot work normally and steadily under VF power generation because of the frequency mismatch. Therefore some regulation methods need to be adopted hence that it also affects the fuel system involving ac-motor driven pumps design.

Conventional induction motors must be designed to accommodate the frequency variation resulting in a significant speed variation between minimum and maximum frequency. Thus both transfer and boost pumps must be sized to meet minimum flow and pressure at the lowest available ac frequency (and hence the lowest rotational speed), four significant issue result from this situation [17]:

1. Boost pumps are typically oversized for the cruise flight condition where engine speed are high and hence pump rotational speeds are high
2. Power factors are much lower than for constant frequency power systems.
3. Heavier pumps to accommodate the specified performance at low frequency
4. More Current is required to deliver the required power

1.2.3.4 Variable speed constant frequency block diagram

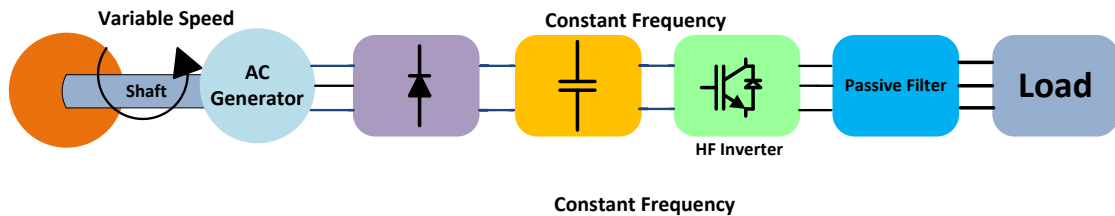


Figure 8 Variable speed constant frequency block diagram

Mechanical Interface of CSD/IDG have been replaced by an AC Generator rotating at variable speed followed by a Rectifier then a DC Link that supply a high switching frequency Inverter with output passive filter (Figure 8). This inverter produces the required sinusoidal voltage with constant frequency providing the following advantages

- High Efficiency (more than 85% according to [16])
- Smaller Size and Weight
- Less fuel consumption,

- Lower maintenance and operation costs
- Electrical power does not require a heavy infrastructure
- Very flexible

The first VSCF has been successfully used on the military aircraft F-18E/F, while the second one has been widely used on the commercial aircraft, such as B737 and B777 [5]. The new variable speed constant frequency system (VSCF) contains a lot of harmonics due to the existing of power converters. To meet the standards of harmonic contents based on Total Harmonic Distribution measure either passive filters [1] or active power filters [18-19] are used. Unfortunately these filter have and a negative impact in power density as well the efficiency of the system. This study is only focused in improving the high switching frequency inverter block and output passive filter block therefore, detailed analysis and design will be obtained for these two blocks next chapters.

2. AOF FOR SINGLE PHASE VSCF APPLICATION

(PROOF OF CONCEPT)

2.1 Introduction

The power quality of the electrical system is an important matter especially in modern applications. Thus, if a high quality sinusoidal voltage waveform must be available at a certain point in the electrical system to supply standard or critical loads, a voltage filtering system is required comply with IEEE standards and technical recommendations.

Passive filtering is a possible solution, but presents several drawbacks e.g. larger Weight and volume. Another option could be an ac/dc/ac system, which produces high quality sinusoidal voltages. However, it needs more than one stage of conversion and implies higher costs as well as complex configuration. Another possibility is the utilization of active filters, theoretically introduced in the 1970 [20]. A series active filter is the appropriate choice to improve voltage waveforms [21] but it requires DC-Link or a power source supplied by an auxiliary source.

Another proposed approach is utilizing active filters in harmonic current reduction or compensation [22-23]. While another proposed topology that combined active filter filters with a passive element causing in a hybrid voltage filter [24-25]. Unlike hybrid voltage filters used in [24-25], proposed Active Output Filter (AOF) has the following advantages:

- ❖ Lower DC input voltage
- ❖ High modulation index up to $m_a = 1.27$
- ❖ AOF is dynamic and can be used for retro-fit applications
- ❖ AOF DC Link Storage elements has a self-balancing advantage without a need close-loop control
- ❖ High power quality output in compliance with IEEE THD Standards
- ❖ Can be utilized for different loading condition e.g. unbalanced and nonlinear-load with maintaining good quality sinusoidal output

2.2 Analysis

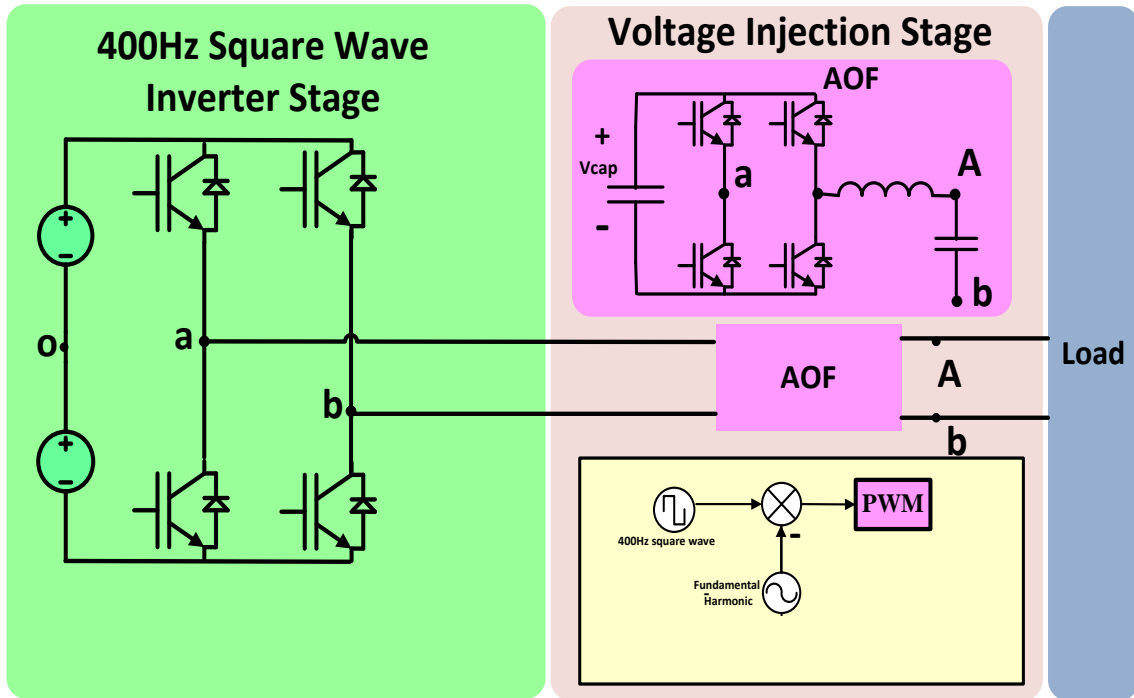


Figure 9 The proposed topology containing square wave inverter and the high switching frequency AOF

Since that the inverter in the proposed AOF topology show in Figure 9 switches the input DC link voltage in square wave pattern thus the resulted input voltage will be as follows:

$$v_{inv}(t) = \frac{4}{\pi} V_{DC} \cdot \sum_{n=1,3,5..}^{\infty} \frac{\sin(n\omega t)}{n} \quad (1)$$

$$v_{inv}(t) = \frac{4}{\pi} V_{DC} (\sin(\omega t) + \frac{\sin(3\omega t)}{3} + \frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} + \frac{\sin(9\omega t)}{9} \dots) \quad (2)$$

The voltage across AOF has been modulated to generated harmonics 3rd, 5th, 7th...nth

which has a magnitude of $-\frac{4}{n\pi}$ as expressed in the following equation

$$v_{AOF}(t) = -\frac{4}{\pi}V_{DC}\left(\frac{\sin(3\omega t)}{3} + \frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} + \frac{\sin(9\omega t)}{9} \dots\right) \quad (3)$$

To obtain the resulted output voltage waveform we Take KVL shown in Figure 10

$$v_o(t) = v_{inv}(t) + v_{AOF}(t) \quad (4)$$

$$v_o(t) = \frac{4}{\pi}V_{DC} \sin(\omega t) \quad (5)$$

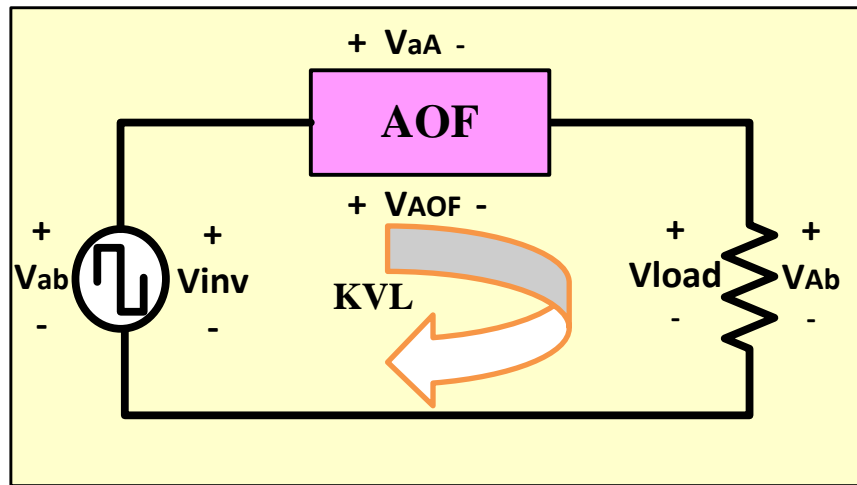


Figure 10 Single phase AOF voltage representation

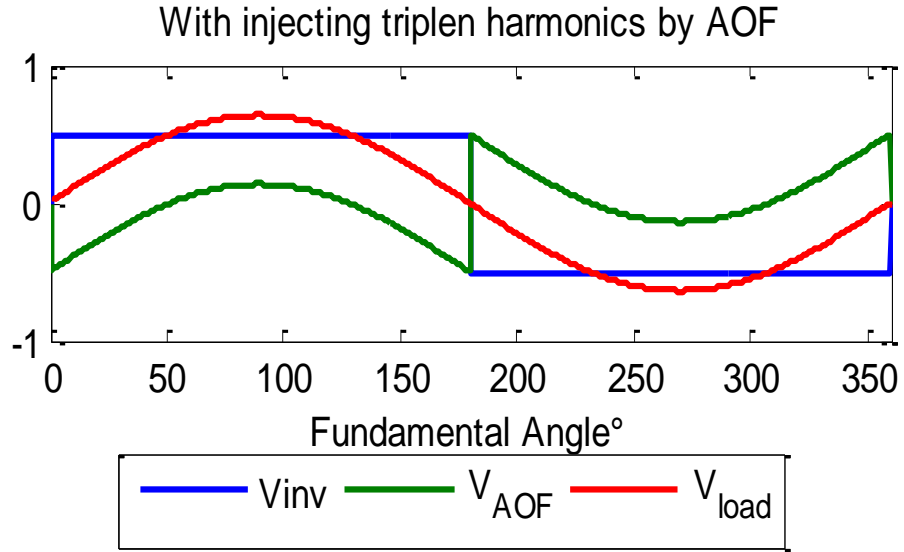


Figure 11 Voltage wave form of the main inverter voltage(V_{inv}), AOF injected voltage(V_{AOF}) and load voltage (V_{load})

As a result, a pure sinusoidal output has been achieved featuring a modulation index m_a of $\frac{4}{\pi}$ or 1.27 exceeding the common maximum modulation value of 1 obtained from conventional single phase pulse width modulated inverter as demonstrated in Figure 11. And that offers an opportunity to reduce the DC link capacitor size as shown in below. Hence that v_{ab} is the peak load voltage such that $v_{ab} = V_{Load}$

$$v_{ab} = m_a V_{DC} \longrightarrow V_{DC} = \frac{v_{ab}}{m_a} \quad (6)$$

Table 2: Modulation index comparison between conventional inverter and the proposed AOF topology

m_a	V_{DC}
1	100% of v_{ab}
1.27	78.7% of v_{ab}

Table 2 summarizes the main dc-link voltage reduction to achieve the same output voltage compared to traditional passive filter topology.

However, injecting voltage harmonics (3rd, 5th, 7th...) into the System will also generate even harmonics in the AOF DC link capacitor reflected from the dc-link current $i_{DC AOF}$. To find the DC link Current the switching function $S_{AOF}(t)$ that governs AOF is assumed to equal the AOF injected voltage $v_{AOF}(t)$ obtained from Equation 3 when assuming ripple free AOF DC Link.

$$S_{AOF}(t) = \frac{v_{AOF}(t)}{V_{DC AOF}} \quad (7)$$

$$\frac{-4}{\pi} V_{DC} \sum_{n=3,5,7,9,\dots}^{\infty} \frac{\sin(n\omega t)}{n} = \frac{-4}{\pi} \sum_{n=3,5,7,9,\dots}^{\infty} \frac{\sin(n\omega t)}{n} \quad (8)$$

Then $i_{DC AOF}$ can be attained when assuming a pure sinusoidal output of I_o magnitude

$$i_{DC AOF} = i_o(t) S_{AOF}(t) = I_o \sin(\omega t) S_{AOF}(t) \quad (9)$$

$$i_{DC AOF} = I_o \frac{4}{\pi} \left(\frac{\cos(2\omega t)}{6} - \frac{\cos(4\omega t)}{6} + \frac{\cos(4\omega t)}{10} - \frac{\cos(6\omega t)}{10} + \frac{\cos(6\omega t)}{14} \dots \right) \quad (10)$$

Thus, by injecting harmonics voltage (3^{rd} , 5^{th} , 7^{th} , ..) current harmonics (2^{nd} , 4^{th} ...) are reflected on the DC link capacitor and we can find those harmonics components as demonstrated above. This will cause low order (2^{nd}) voltage harmonic ripples to appear on the DC link voltage of the AOF and hence the size of the capacitor is selected accordingly.

2.3 Passive filter sizing

Since that the AOF emulates all the odd harmonics (3^{rd} , 5^{th} , 7^{th} ) generated from equation (3) an undesired switching frequency harmonics will also appear on the output due to pulse width modulation switching as shown in Figure 12. A minimized second order LC filter has been added to attenuate those harmonics to ensure power high quality sinusoidal output.

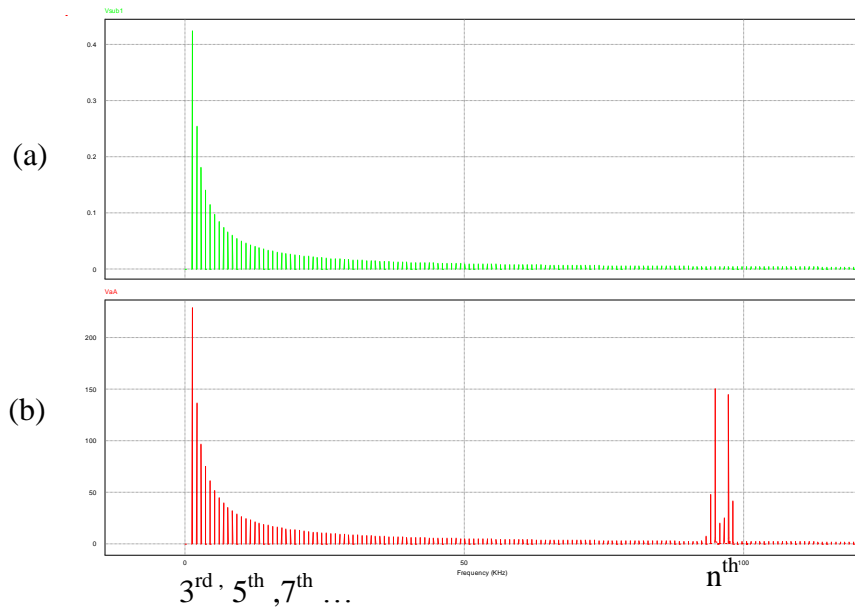


Figure 12 Harmonic distribution for a) AOF modulating signal b) AOF voltage VaA

To illustrate the AOF advantage the following design example shown in Table 3 has been taken into consideration:

Table 3: Design example for single phase AOF

Fsw	Input DC	Load	Load RMS Voltage
50KHz	533v	3KW	480v

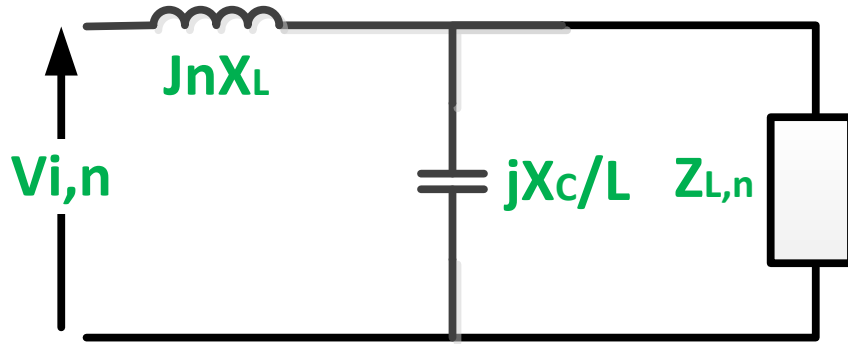


Figure 13 Second order passive filter

The transfer function of a second order LC filter shown in Figure 13 can be illustrated in the following transfer function such that X_L is the inductive reactance at 400Hz while X_C is the capacitive reactance at 400Hz

$$H = \frac{V_o}{V_{in}} = \frac{-jX_c \cdot Z_{LN}}{nX_L X_c + jZ_{LN}(n^2 X_L - X_c)} \quad (11)$$

Assuming $X_L \ll X_C$ to obtain a close to unity filter gain at full load condition such that

$$: H \approx 1$$

At no load condition Z_{LN} is very large such that:

$$H = -\frac{X_c}{n^2 X_L - X_c} = \frac{1}{n^2 \cdot \frac{X_L}{X_c} - 1} \quad (12)$$

Assuming Total Harmonic Distortion (THD) is less than 5% and hence that H is

$$\text{equivalent to } H \text{ such that } H = \frac{1}{n^2 \cdot \frac{X_L}{X_c} - 1} < 0.045.$$

Then:

$$\frac{X_L}{X_C} \geq \frac{23.333}{n^2} \quad (13)$$

$$X_L = 2\pi L f_1, \quad X_C = \frac{1}{2\pi f_1 C}, \quad n = \frac{f_{sw}}{f_1} \quad (14)$$

And for unipolar switching schemes the harmonic start to appear at twice the switching frequency thus the effective switching frequency is twice the switching frequency. The LC filter is designed assuming that the harmonics is appeared at the switching frequency which is the worst case scenario at $n = \frac{f_{sw}}{f_1} = 120$. And since the resonance frequency of the LC filter can be found using the following equation:

$$\frac{f_r}{f_1} = \sqrt{\frac{X_L}{X_C}} \leq \sqrt{\frac{n^2}{23.333}} \leq 25 \quad (15)$$

Than $f_{res} = 10Khz$

Since that non-linear diode rectifier load is mostly the case for single phase inverter application thus the LC filter will be designed in compliance with it as expressed in Figure 14.

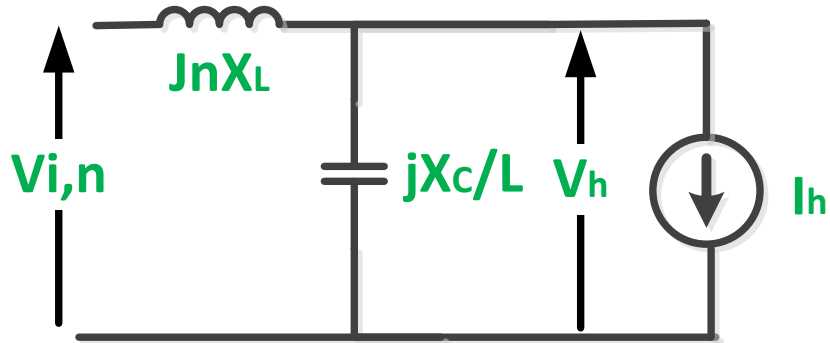


Figure 14 Passive filter equivalent circuit for non-linear load condition

Such that:

$V_h = \text{equivalent voltage}$

$h = \text{harmonic}$

$I_h = \text{Current at "h" harmonic}$

$$|V_h| = \frac{h}{1 - h^2 \frac{X_L}{X_C}} \cdot I_h \quad (16)$$

For the previous assumption such that $X_L \ll X_C$ which also implies that $\frac{X_L}{X_C}$ is very small

and that will lead us to the following equation:

$$|V_h| \cong hX_L \cdot I_h \quad (17)$$

Assuming that the 3rd harmonic is 80% of all the harmonics components and since that

THD is assumed to be 5% then THD for only the 3rd harmonic is $0.05 \cdot 0.8 = 0.03$ such

that:

$$\frac{|V_3|}{V_1} = \frac{3 \cdot X_L \cdot I_3}{V_1} = 0.03 \quad (18)$$

For our designed example of 3KW resistive load $I_1 = \frac{P}{V_o} = 6.25$

From Equation 14 $I_3 = 0.8 \cdot I_1 = 5A$

Substituting all the calculated parameters in equation 18 then

$$X_L = 0.96\Omega$$

From Equation 14

$$L = \frac{X_L}{2\pi f_1} = 380\mu H$$

Given equation 13 X_C can be computed to be 600Ω

$$c = \frac{1}{2\pi f_1 X_c} = 0.663 \mu F$$

The inductor current ripple has to pass through the following check point to insure a viable design:

$$\Delta i_{Lmax} = \frac{1}{8} \frac{V_{Dc}}{L \cdot f_{sw}} \leq 20\% i_{peak} \quad (19)$$

And that check point is met as shown in below Figure 15 obtained from PSIM simulation since that the ripple on L is proved to be less than 20%.

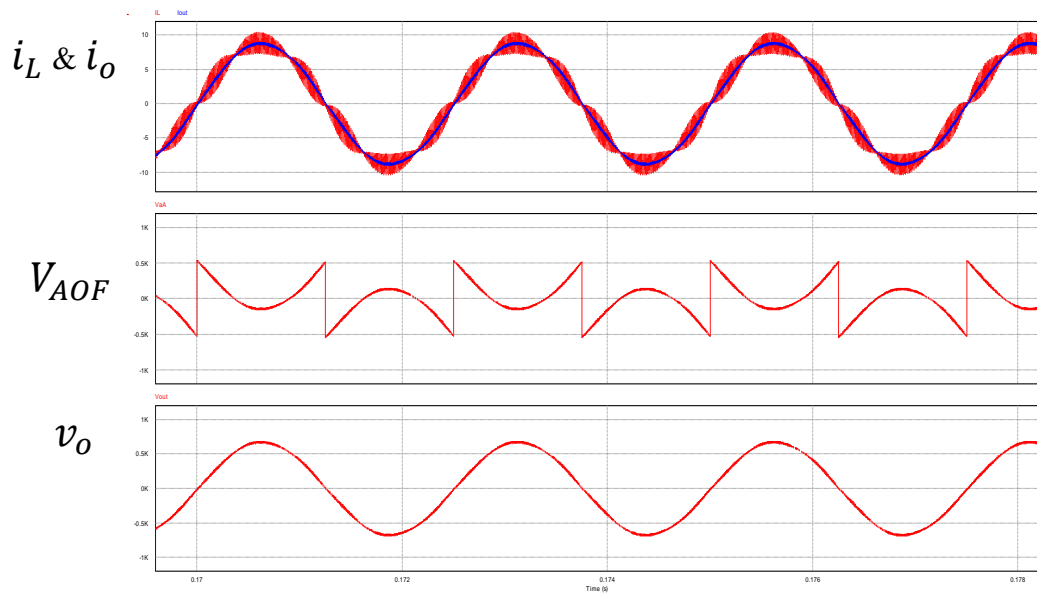


Figure 15 The filter current waveform in comparison with output current wave

2.4 AOF dc-link design

The AOF Direct Current (DC) Link is basically a capacitor that stores the energy coming from the main DC voltage source after the main square wave stage as shown in Figure 9. Ideally, DC Link Capacitor is a voltage source. However, in practical application it needs to be closed loop controlled to maintain the designed voltage charged value while in this study the DC Link is self-balanced in which it get charges until it reached Vdc and maintain its value there with only associating ripples generated from harmonics starting from 2nd harmonic as was explained in analysis section and that can be illustrated in below equation in which K equals Vdc in steady state and the other terms associate the ripple to that Vdc value

$$v_{DC\ AOF}(t) = \frac{1}{c} \int i_{DC\ AOF}(t) + K \quad (20)$$

$i_{DC\ AOF}(t)$ Have been demonstrated before in equation (10)

Given that

$$\Delta Q = C\Delta V \quad (21)$$

And ΔQ can be obtained by plotting equation 10 and integrate the area when the capacitor is charging as shown in the following Figure 16:

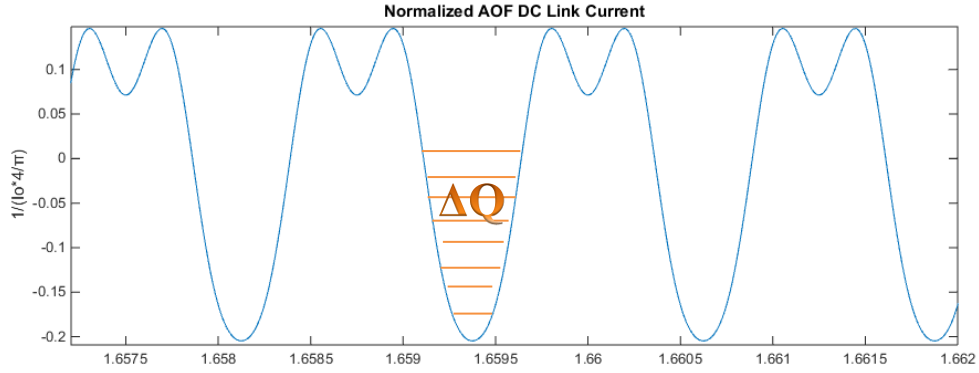


Figure 16 Active output filter normalized dc-link current

The shaded area can be calculated to obtain normalized ΔQ value for 400Hz fundamental frequency. Using MATLAB, the normalized $\Delta Q_{normalized} = 65.258 \cdot 10^{-6}$. Note that this number is linearly proportional to fundamental frequency. Then substituting that number in Equation 21

$$\Delta Q_{normalized} \cdot I_o \cdot \frac{4}{\pi} = C \Delta V_{AOF_DC} \quad (22)$$

And when dividing by the output voltage V_o the following equation will be resulted

$$\Delta Q_{normalized} \cdot \frac{I_o}{V_o} \cdot \frac{4}{\pi} = \frac{C \Delta V_{AOF_DC}}{V_o} \quad (23)$$

Hence that from Equation 6, then $V_o = m_a V_{DC}$ and that will lead to below equation

$$\Delta Q_{normalized} \cdot \frac{I_o}{V_o} \cdot \frac{4}{\pi} = \frac{C}{m_a} \frac{\Delta V_{AOF_DC}}{V_{AOF_DC}} \quad (24)$$

For resistive load the capacitance can be computed using this equation:

$$C = \frac{4}{\pi} \cdot \frac{m_a \cdot \Delta Q_{normalized}}{R \cdot \frac{\Delta V_{AOF_DC}}{V_{AOF_DC}}} \quad (25)$$

For the given design example in analysis section the DC Link can be found to be $C = 7\mu\text{F}$ (for 20% ripple and $ma=1.274$) and as a safety Factor the DC Link value have been increased to $15\mu\text{F}$.

2.5 Self-balancing strategy

In previous analysis the DC-Link Capacitor was assumed to reach the V_{DC} voltage value after the certain transient time and then maintains that DC voltage which also associate ripple. The DC link current equation has been illustrated in Analysis Section in Equation 10.

$$v_{inv}(t) = \frac{4}{\pi} V_{DC\ inv} \cdot \sum_{n=1}^{\infty} \frac{\sin(n\omega t)}{n} \quad (26)$$

$$S_{AOF}(t) = -k \frac{4}{\pi} \left(\frac{\sin(3\omega t)}{3} + \frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} + \frac{\sin(9\omega t)}{9} \dots \right) = -k \frac{4}{\pi} \sum_{n=3,5,\dots}^{\infty} \frac{\sin(n\omega t)}{n} \quad (27)$$

To investigate DC Link capacitor response we need to formulate $v_{AOF\ DC\ link}$ with respect to $i_{AOF\ DC\ link}$ and that can be done by substituting equations 26 and 27 in 28

$$i_O(t) = \frac{v_{inv}(t) + v_{AOF}(t)}{R} \quad (28)$$

$$i_O(t) = \frac{\left[\frac{4}{\pi} V_{DC\ inv} \sum_{n=1}^{\infty} \frac{\sin(n\omega t)}{n} \right] + [S_{AOF}(t) v_{DC\ AOF}(t)]}{R} \quad (29)$$

$$i_O(t) = \frac{\left[\frac{4}{\pi} V_{DC\ inv} \sum_{n=1}^{\infty} \frac{\sin(n\omega t)}{n} \right] + \left[\frac{4}{\pi} \sum_{n=3,5,\dots}^{\infty} \frac{\sin(n\omega t)}{n} v_{DC\ AOF}(t) \right]}{R} \quad (30)$$

$$i_{DC\ AOF}(t) = \left[\frac{4}{\pi} \sum_{n=3,5,\dots}^{\infty} \frac{\sin(n\omega t)}{n} \right] \frac{\left[\frac{4}{\pi} V_{DC\ inv} \sum_{n=1}^{\infty} \frac{\sin(n\omega t)}{n} \right] + \left[\frac{4}{\pi} \sum_{n=3,5,\dots}^{\infty} \frac{\sin(n\omega t)}{n} v_{DC\ AOF}(t) \right]}{R} \quad (31)$$

Then substituting equation 31 in equation 32 note that $K=0$ since that the DC Link is initially uncharged.

$$v_{DC\ AOF}(t) = \frac{1}{C} \int i_{DC\ AOF}(t) dt + K \quad (32)$$

To simplify the analysis only the DC components of the previous equation have been taking into consideration the results equation will be as follows:

$$I_{DCAOF} = \frac{(a_0)V_{dcinv} + (a_1)V_{dcaof}}{R} \quad (33)$$

Table 4: The coefficients of V_{dcinv} and V_{dcaof} with respect to the presented injected harmonics

Harmonics Taken Into consideration	a_0	a_1
1 st , 3 rd	0.09	-0.09
1 st , 3 rd , 5 th	0.1224	-0.1224
1 st , 3 rd , 5 th , 7 th	0.1389	-0.1389
1 st , 3 rd , 5 th , 7 th , 11 th	0.1556	-0.1556
All odd Harmonics	0.1892	-0.1892

It can be noticed from the previous Table 4 that $a_0 = -a_1$ in all cases. Moreover, almost half of the DC components generated from fundamental and 3rd only. On the other hand, 82% of the total DC Components when taking up to 11th harmonic component from the square wave injected voltage. Therefore lower order harmonics are mainly responsible for charging the AOF DC Link capacitor and since that

$$I_{DCAOF} = S \cdot V_{DC\ AOF}(s) \quad (34)$$

Then

$$V_{DCAOF}(s) = \frac{a_0}{SRC - a_1} V_{dcinv}(s) \quad (35)$$

From the Final Value Theorem, the DC gain is the value of the transfer function when $s=0$ for stable transfer function. Thus, DC gain is equal $= \frac{a_0}{-a_1} = 1$ as been expressed in Table 4. And the response time constant $\tau = R*C$ which determines the settling time and the rising time as well. V_{DCAOF} response for step input of $V_{inv} = 100v$ assuming $R=1$ and $c=5mF$ is illustrated in below Figure 17.

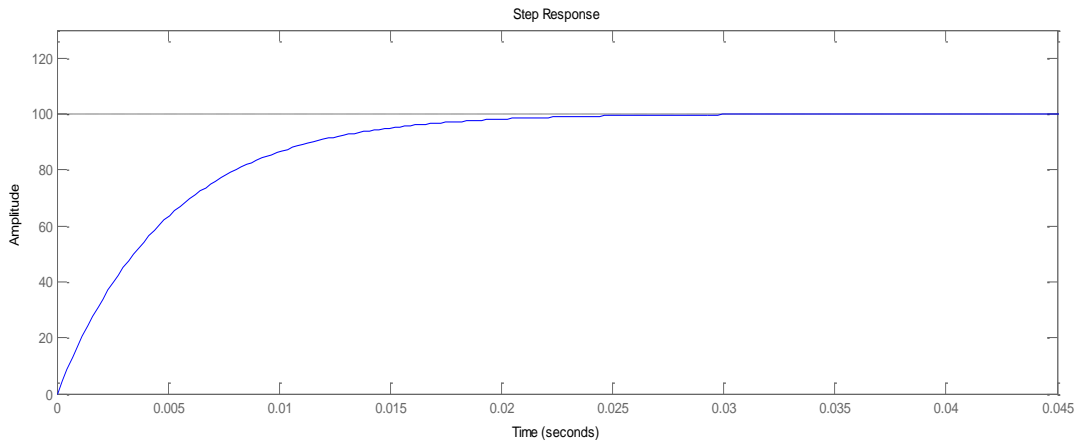


Figure 17 V_{dcaof} response to step input of $V_{dcinv} = 100v$. And that demonstrate that the system is stable.

Hence that the previous response (Figure 17) excludes the ripple effect caused by the even harmonics 2^{nd} , 4^{th} , 6^{th} ...etc., Thus, by simply adding those ripple resulted from equation 10 to Figure 17 we can find dc-link normalized ripple waveform.

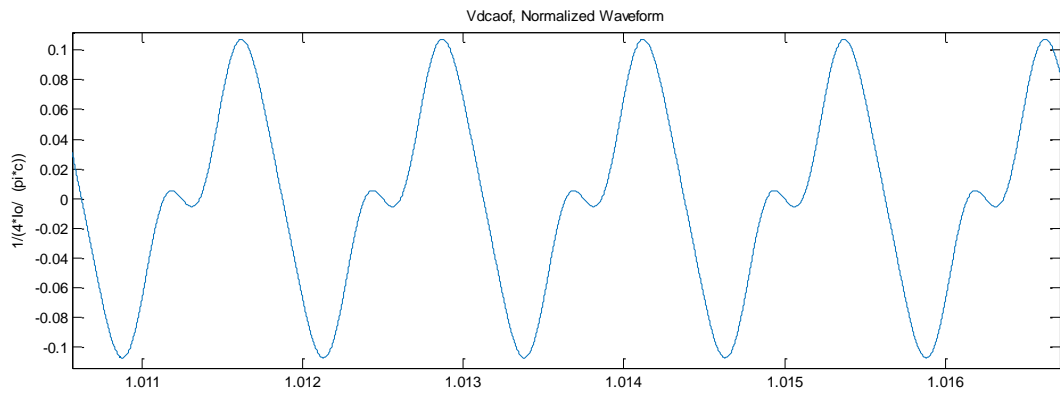


Figure 18 AOF dc ripple waveform

And the resulted wave for is expressed in Figure 19:

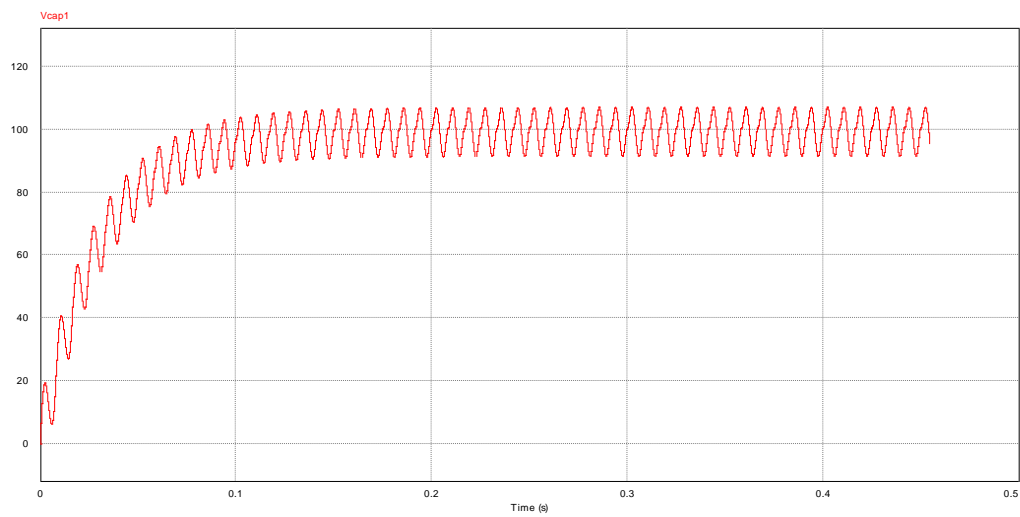


Figure 19 AOF final dc-link wave form after adding the ripples obtained from PSIM simulation

2.6 Comparison between AOF and passive filter in terms of size

Assuming that the switching frequency capability of the conventional IGBT-based inverter is 10 KHz then for design example taken from Table 3 can be summarized into in the following Table 5:

Table 5: Comparison between conventional single phase inverter and single phase AOF configuration

Criteria	Traditional Inverter	AOF topology
Switching Frequency	10Khz	48Khz/400Hz
Required DC Link Voltage	679v	533v
L-Filter	380 μ H	380 μ H
C-Filter	4 μ F	0.66 μ F

It can be observed from the Table 5 that single phase AOF reduce the DC Link voltage requirement by 21.5% offering a lower voltage stress switching devices. Moreover, the capacitor size has been reduced 6 times due to higher switching frequency operation.

2.7 Software simulation

2.7.1 Active output filter for resistive load

The Summarized inverter and AOF specification obtained from the previous sections have been tabulated in Table 6 and Simulated in PSIM. Figure 20 and 21 show the output current i_o with respect to inductor current i_L , AOF voltage V_{AOF} , output voltage across 3 phase resistive load v_o and AOF DC link voltage. It can be confirmed that Figure 9 complies with the analysis section incorporating a stable first order response dc-link voltage. Figure 22 expressed the main inverter dc-link current with respect to AOF dc-link current. When performing FFT to Figure 21 it can be noticed from Figure 23 that 6th harmonic is dominant in the main dc-link current while 4th harmonic is dominant in AOF dc-link current.

Table 6: Design parameters after computing passive filter and dc-link values

f_{sw}	Input DC	AOF DC Link	AOF Filter	Load	Load RMS Voltage
50KHz	533v	15μF	380μH, 0.663μF	3KW	480v

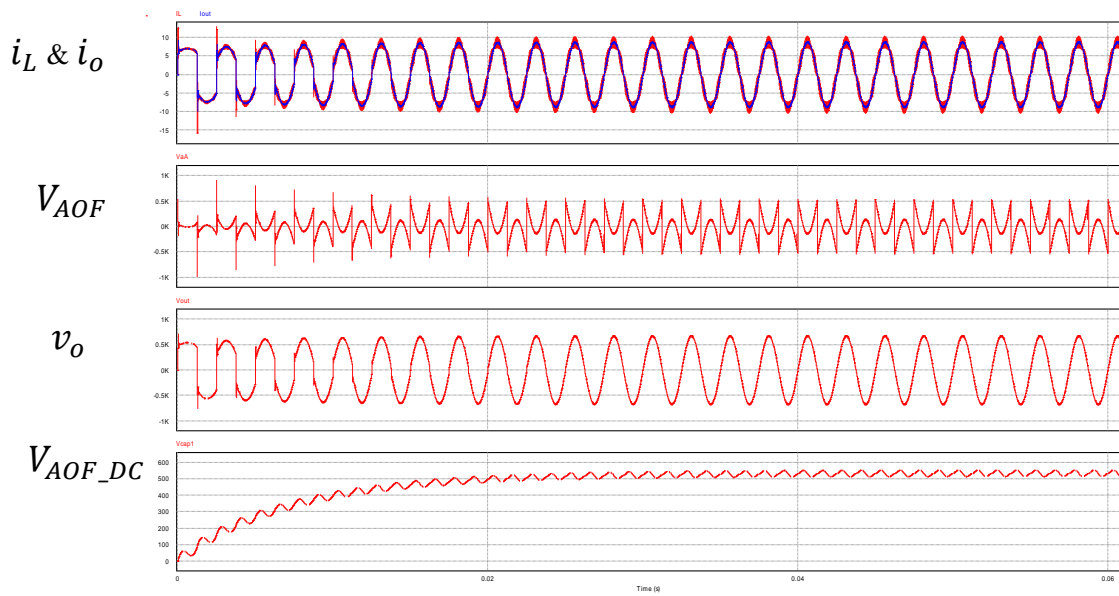


Figure 20 This figure shows that the capacitor is self-balanced with 5 % ripple with a sinusoidal output

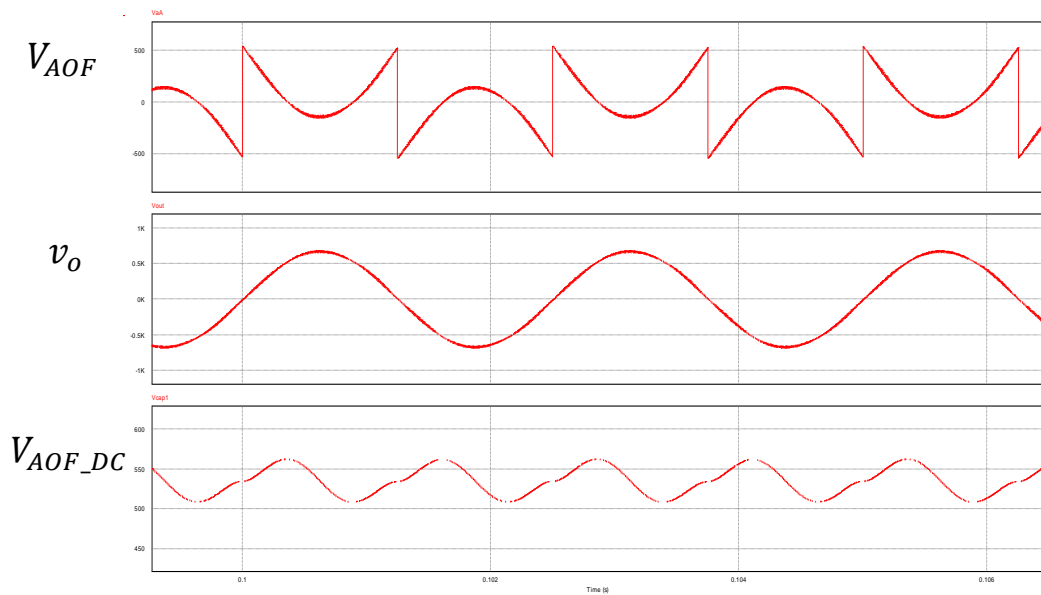


Figure 21 This figure shows the sinusoidal output for 480v RMS 3 kw resistive with capacitor ripple of 10.7 %

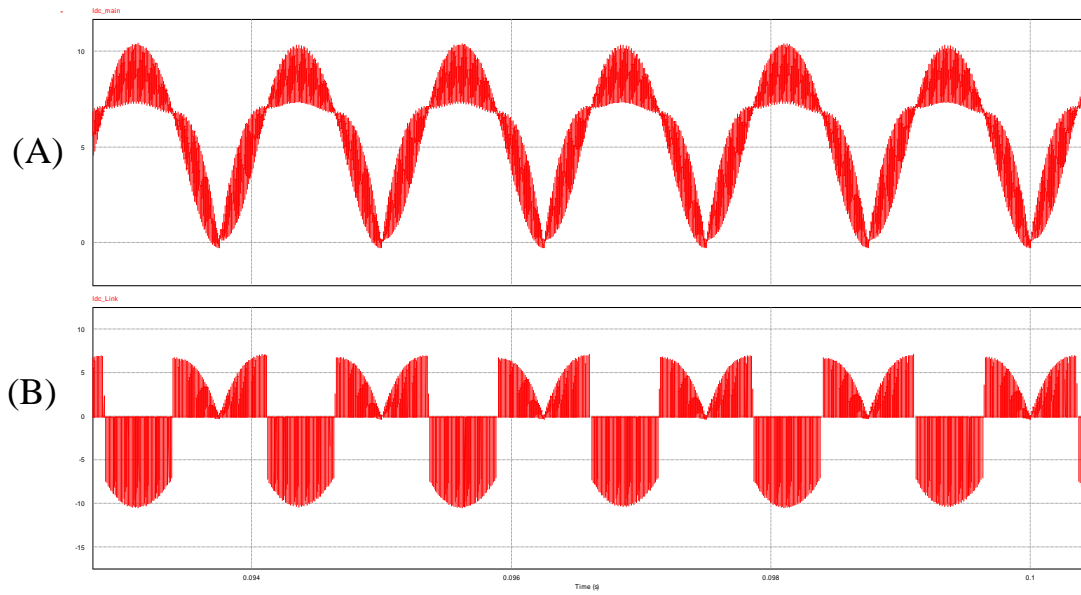


Figure 22 (A) DC current waveform input from the main dc voltage source. (B) dc current waveform of AOF

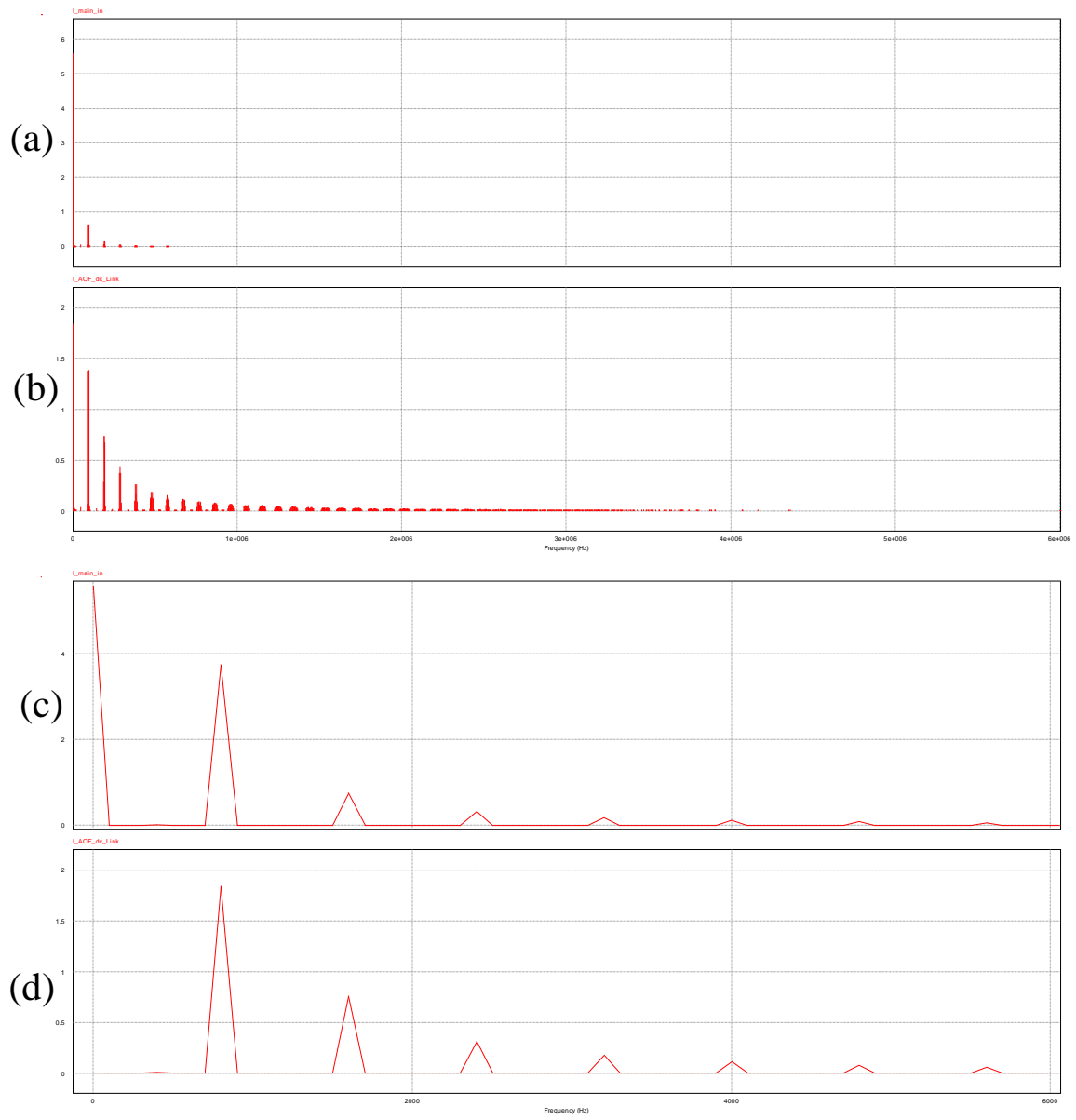


Figure 23 Total harmonic distortion spectrum of: (a) the main dc input current (b) active output filter dc current (c) zoomed in of a (d) zoomed in of b

2.7.2 AOF for non-linear load application

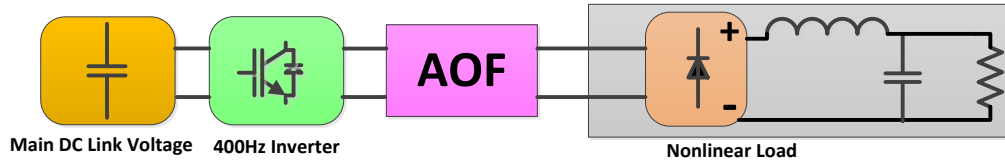


Figure 24 Active output filter block diagram for nonlinear diode rectifier load

Nonlinear load i.e. diode rectifier involves variance of impedance though sinusoidal input is presented. Thus, when the input voltage to the rectifier is sinusoidal the input current will be non-sinusoidal and that present harmonics that might disturb the system. Therefore VSCF with AOF block have been tested under diode rectifier non-linear load to analyze its performance as shown in Figure 24. For Ideal sinusoidal voltage input to a rectifier the current waveform will involve lower odd harmonics and the 3rd is typically the largest one therefore the LC filter need to be designed accordingly. Table 7 summarizes the components parameters selected for testing sinusoidal output resulted from AOF to feed a non-linear diode rectifier load. Since that AOF is self-balanced and the close loop control has not been used in this analysis, a small passive impedance in series with Filter inductor to assist in neutralizing the added nonlinear load harmonic effects [3].

Table 7: Design parameters for 1-phase nonlinear load

f_{sw}	Input DC	AOF DC Link	AOF Filter	load	Load RMS Voltage	Rectifier Ld,Cd
50KHz	533v	15 μ F	300 μ H, 5 μ F	3KW	480v	4mH 133 μ F

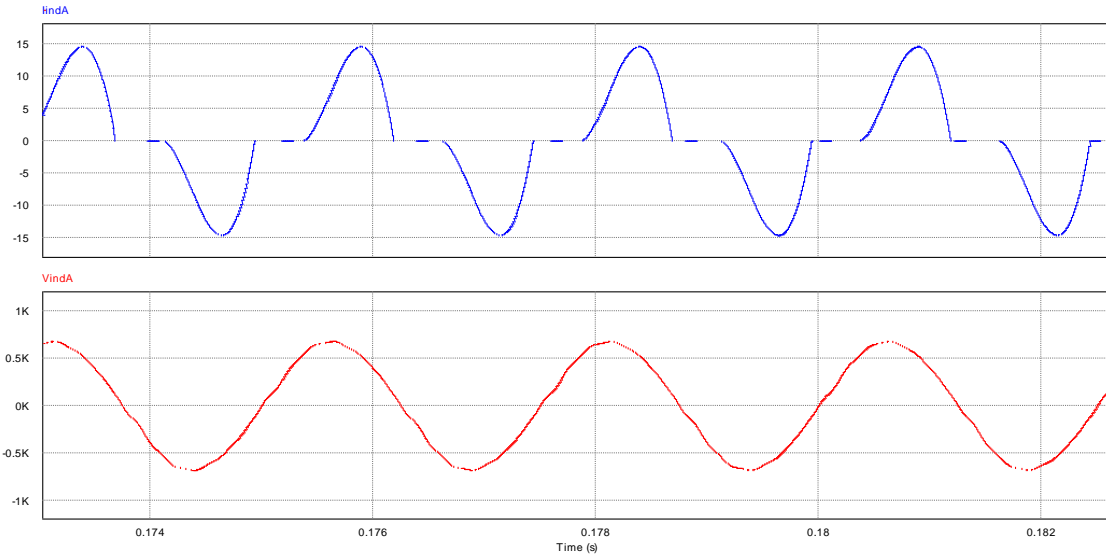


Figure 25 The upper figure describes the diode rectifier input current while the lower figure describes the diode rectifier input voltage that maintains a very good quality at total harmonic distortion of 3%

Given the above Figure 25, AOF supply the nonlinear load with a high quality input voltage though the non-linear case is presented. Given Figure 26 the DC voltage output of the rectifier is maintained with ripple of 10% and the AOF DC Link is self with a ripple of 14%.

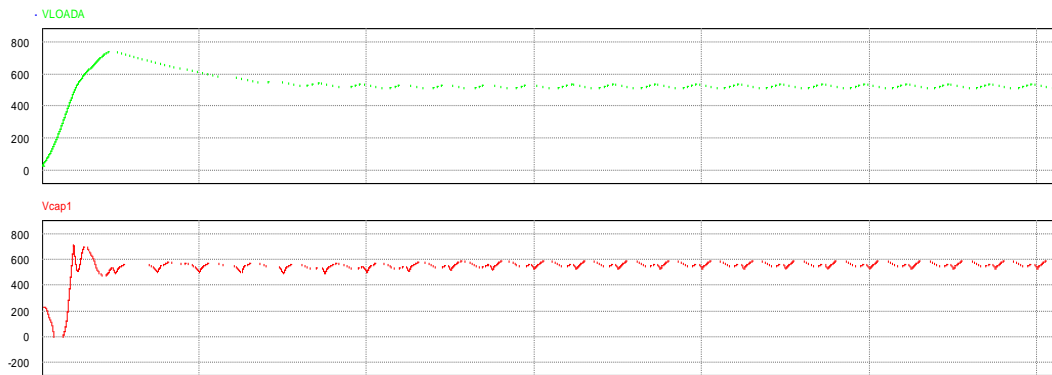


Figure 26 The upper figure shows the dc output voltage of the rectifier in "green" while the second figure shows that the dc-link capacitor is self-balanced to 533v+14% ripple

When Considering AOF DC Link Current and Main inverter DC Link Current the resulted waveform is described below Figure 27:

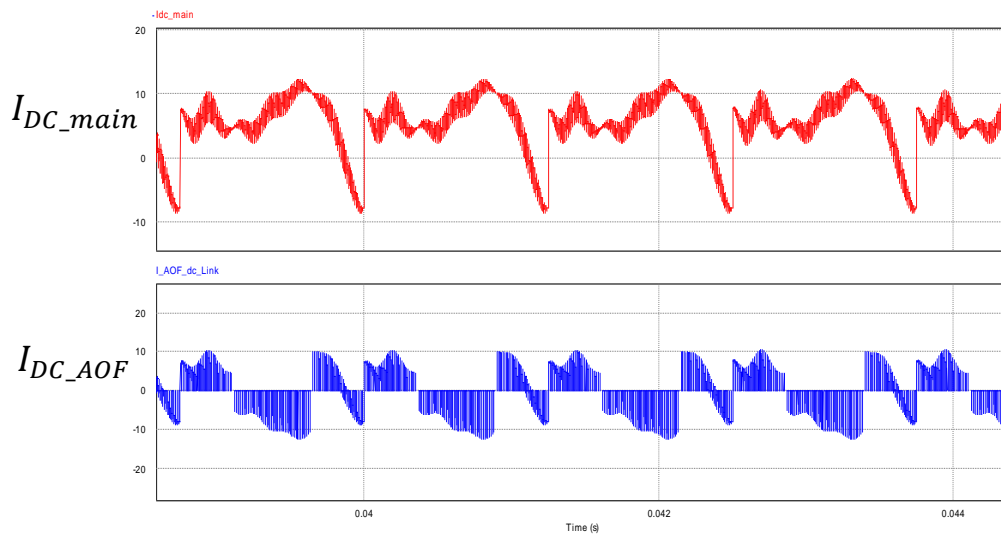


Figure 27 DC Current waveform input from the main DC voltage source to the square Inverter and it's not affected with diode rectifier addition

To investigate the harmonics distribution for the above currents, Fast Fourier Transform have been analyzed using PSIM and the results is expressed Figure 28. As expected, the main inverter has a DC components and harmonics starting at the 2nd while AOF involve even harmonics components and it's slightly effected by non-linear load condition.

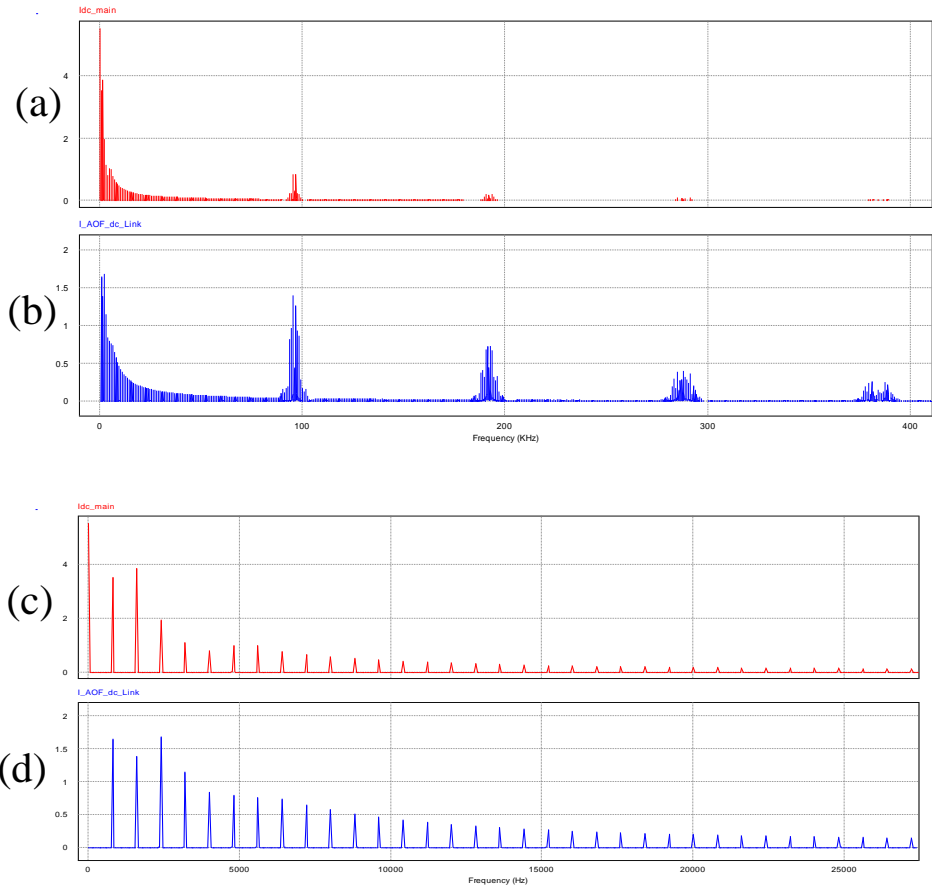


Figure 28 Total harmonic distortion spectrum of: (a) he main dc input current (b) AOF dc current in bottom (c) zoomed in of a (d) zoomed in of b

3. THREE PHASE AOF FOR VSCF APPLICATION

3.1 Introduction

Similar to single phase AOF approach, The 3 phase Active Output Filter topology also cancels out the voltage harmonics from the main inverter using the switching strategy. The design of the Active Output Filter topology is shown in Figure 29. The structure can be broadly divided into two main sub-systems, main inverter and 3 AOF block. Moreover, each AOF block contains H Bridge, DC Link and LC filter.

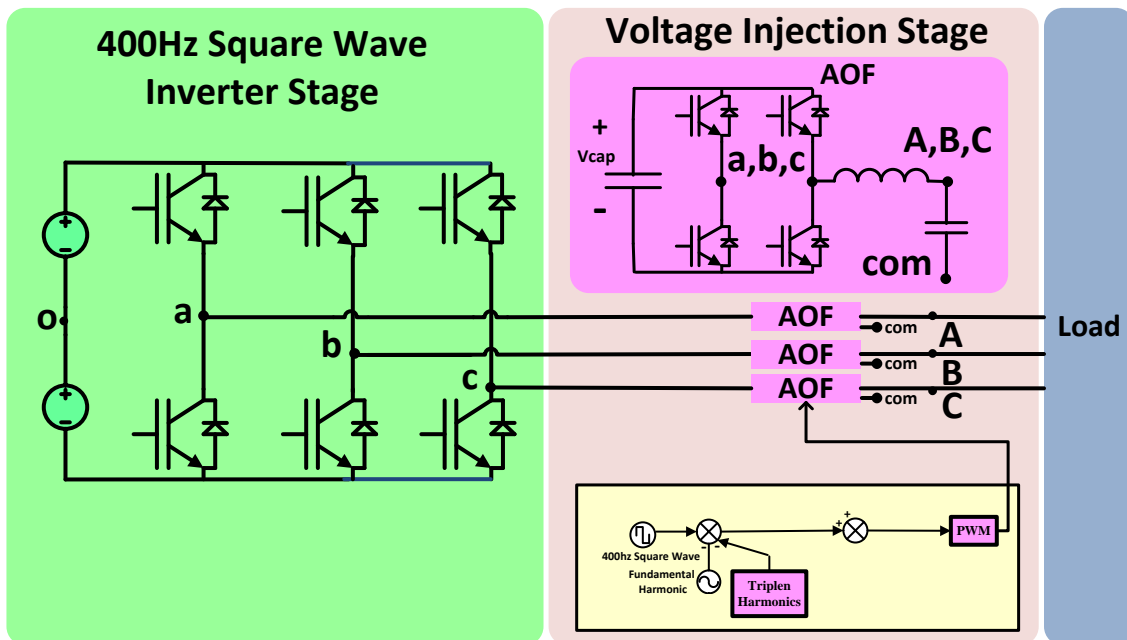


Figure 29 The proposed system architecture using 400Hz inverter and 3 AOF blocks

The proposed topology has the following advantages:

- ❖ AOF Reduce The Passive elements down to 70% smaller in size depending on the switching frequency
- ❖ AOF is capable to switch at very high switching frequency i.e. 200Khz due to lower VA rating of 1/3 PU
- ❖ Main inverter low switching frequency at 400 Hz results in a boost in efficiency
- ❖ Lower DC input voltage
- ❖ High modulation index up to $m_a = 1.27$
- ❖ AOF is dynamic and can be used for retro-fit applications
- ❖ AOF DC Link Storage elements has a self-balancing advantage without a close-loop control
- ❖ High power quality output in compliance with IEEE THD Standards
- ❖ Can be utilized for different loading condition e.g. unbalanced and nonlinear-load with maintaining good quality sinusoidal output

3.2 Conventional 3 phase inverter with passive output filter approach

In this study only the main inverter and the passive output filter blocks have been considered from VSCF power generation system which has been presented in Figure 8 in Chapter 1. Moreover, the Direct Current Link (DC Link) is assumed to be very large and ripple free to act as an ideal DC voltage source as illustrated in Figure 30 below.

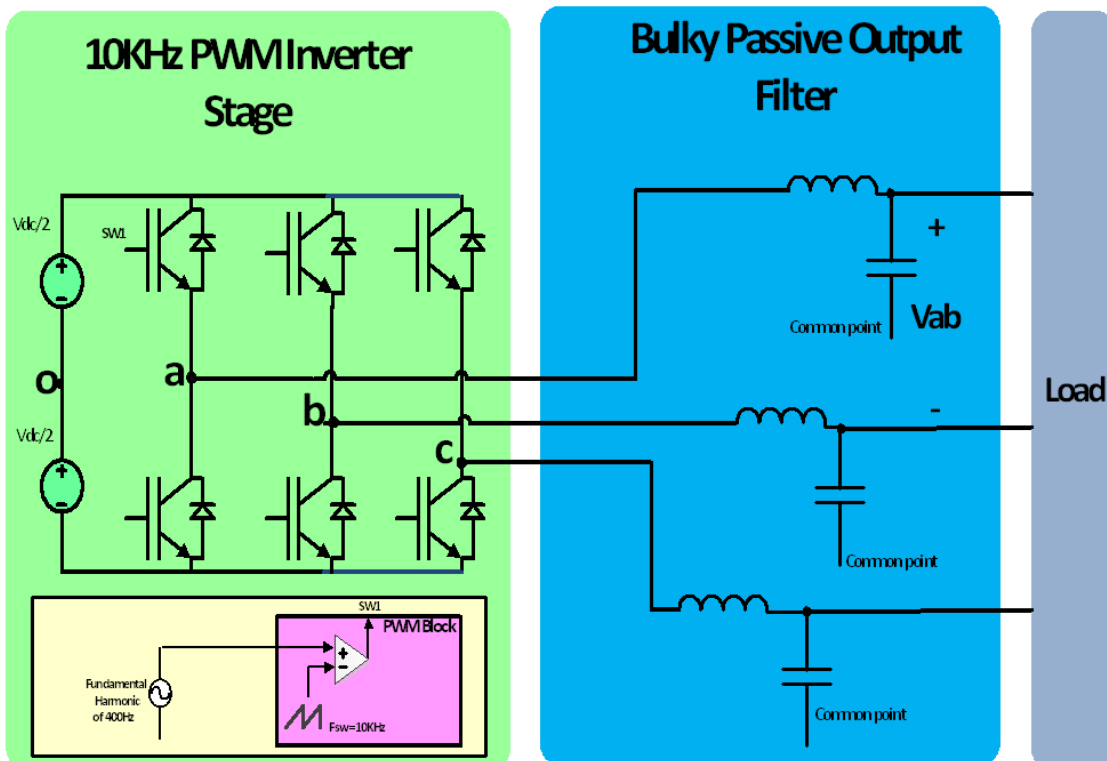


Figure 30 Circuit waveform of conventional 3 phase inverter

3.2.1 Main inverter block

The main inverter contains six full VA rated power switches to convert the DC voltage input voltage to a Pulse Width Modulated voltage waveform that contains the desired fundamental and the unwanted harmonics starting at the switching frequency as tabulated in Table 8.

Table 8: Normalized amplitudes V_{n3}/V_{dc} for line-to-line three-phase pwm voltages [26]

$m_a \backslash h$	0.2	0.4	0.6	0.8	1.0
m_f	1.242	1.15	1.006	0.818	0.601
$m_f \pm 2$	0.016	0.061	0.131	0.220	0.318
$m_f \pm 4$					0.018
$2m_f \pm 1$	0.190	0.326	0.370	0.314	0.181
$2m_f \pm 3$		0.024	0.071	0.139	0.212
$2m_f \pm 5$				0.013	0.033
$3m_f$	0.335	0.123	0.083	0.171	0.113
$m_f \pm 2$	0.044	0.139	0.203	0.176	0.162
$m_f \pm 4$		0.012	0.047	0.104	0.157
$m_f \pm 6$				0.016	0.044

Given Table 8 above, m_a which stands for the modulation index is defined as follows:

$$m_a = \frac{2v_{ab}}{V_{dc}\sqrt{3}} \quad (36)$$

$$m_f = \frac{f_{sw}}{f_o} \quad (37)$$

Hence that

m_a : Modulation Index

m_f : The ratio between modulating signal and reference signal

v_{ab} : Line to Line voltage RMS

f_{sw} : Switching Frequency

f_o : Fundamental Frequency

V_{dc} : Input DC voltage to the inverter

The largest harmonics start to appear at the switching frequency in which the LC filter will be sized accordingly. Moreover, the maximum m_a in this case is 1. However, when using Space Vector Pules Width Modulation switching scheme higher modulation index can be achieved at $m_a = 1.1547$. However, since that VSCF module handles high complex power that can reach to 250VA per module in large aircrafts. Thus, the switching frequency is constrained due to higher switching losses as well as lower reliability of those switches at high power which force the design of the output L-C filter to be bulky. The following design example shown in Table 9 will be considered in order to obtain a reasonable LC size comparison between the traditional inverter topology and the proposed AOF topology.

Table 9: Design example for passive elements size comparison

f_{sw}	V_{dc}	Load	$V_{Load}(RMS)$
50Khz	681v	52.5KW per/phase	311v

3.2.2 Output passive filter design

Similar to dc-dc buck converter [87], the relation the L-Filter value can be obtained when related to the current ripple Δi_L by analyzing the following equation 38

$$\Delta i_L = \frac{V_{dc} D(1-D)}{f_{sw} \cdot L} \quad (38)$$

It can be noticed that the current ripple is maximum at duty ration (D) of 50%. And that will lead to the following

$$\Delta i_{Lmax} = \frac{V_{dc}}{4 \cdot f_{sw} \cdot L} \quad (39)$$

For 3 phase system the DC input voltage is divided equally between two inductors since that there are two inductor current path for each switching state and that results in equation below:

$$\Delta i_{Lmax} = \frac{V_{dc}}{8 \cdot f_{sw} \cdot L} \quad (40)$$

A reasonable Δi_{Lmax} is assumed to be less that 20% of the peak load current

i_{peak} and that will results the following equation

$$L \geq \frac{V_{dc}}{8 \cdot f_{sw} \cdot 0.2 \cdot i_{peak}} \quad (41)$$

Given Table 9, the L Filter need to be $L \geq 177 \mu H$

To find the filter capacitor value a proper resonance frequency can be selected given the following inequality:

$$5f_o \leq f_{res} \leq \frac{1}{5} f_{sw} \quad (42)$$

Assuming that the hardware switching frequency capability is $f_{sw} = 10Khz$ then, $f_{res} = 2KHz$, and the capacitance can be found using the following equation note the resulted c is $36\mu F$.

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{1}{LC}} \quad (43)$$

$$c = \frac{1}{L(2\pi f_{res})^2} \quad (44)$$

Total Harmonic Distortion (THD) is a term used to quantify the non-sinusoidal property of a waveform. THD is the ratio of the rms value of all the non-fundamental frequency terms to the rms value of the fundamental frequency term as expressed in the following equation [87]:

$$THD = \sqrt{\frac{\sum_{n \neq 1} V_{n,rms}^2}{V_{1,rms}^2}} \quad (45)$$

Total harmonic distortion is often applied in situations where the dc term is zero, in which case THD may be expressed as

$$THD = \sqrt{\frac{\sum_{n=2} V_{n,rms}^2}{V_{1,rms}^2}} \quad (46)$$

However THD is assumed to be equivalent to the gain of the 2nd order LC filter at the switching frequency since that all harmonics components between the fundamental and the switching frequency equals to zero due Pulse Width Modulation operation

$$H = \frac{X_c}{n^2 X_L - X_c} \quad (47)$$

$$X_L = 2\pi L f_o = 11.05 \quad , \quad X_C = \frac{1}{2\pi f_o c} \quad , \quad n = \frac{f_s}{f_1} \quad (49)$$

$$X_L = 0.445\Omega, \quad X_C = 11.05\Omega, \quad n = 25,$$

The resulted gain (H) is 4.1% then THD is less than 5% which is complies with industrial IEEE standards. A reasonable assumption for the main inverter switching frequency has been chosen to 10 KHz in order to achieve high power quality which minimum possible switching frequency. The results have simulated in MATLAB for an ideal resistive balanced load condition as shown in Figure 31 and Figure 32 below:

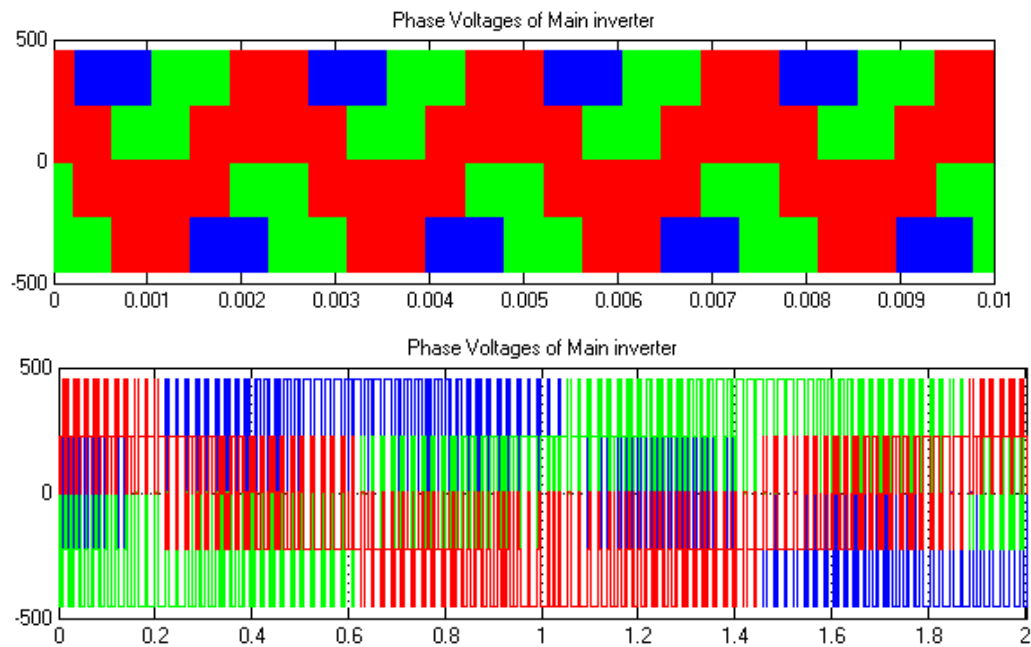


Figure 31 Phase voltage for the 10 khz switching frequency inverter without AOF presence

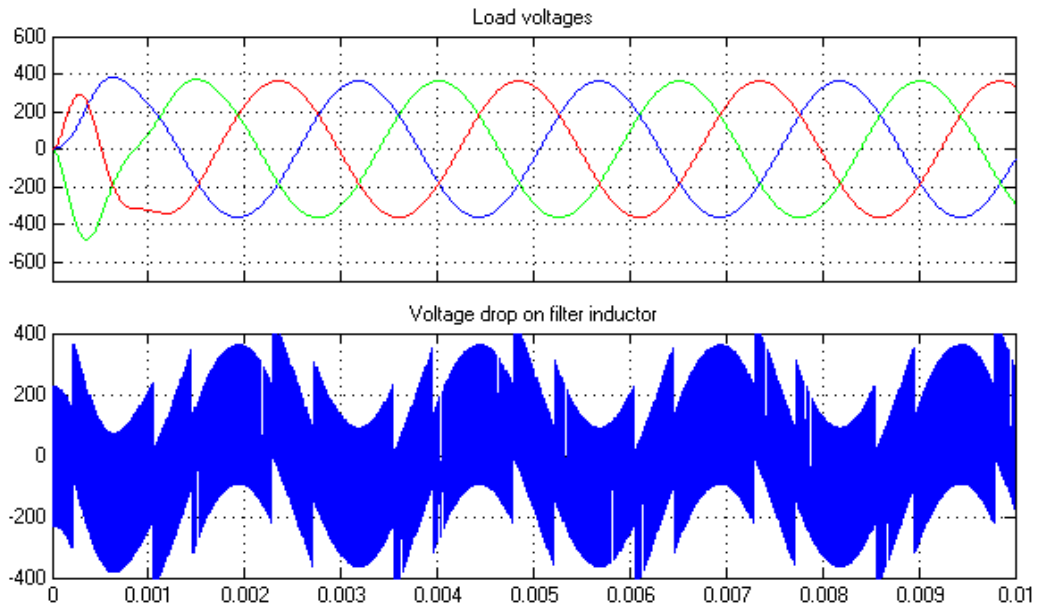


Figure 32 The achieved sinusoidal output voltage at very low THD along with the voltage drop of the AOF inductor filter

3.3 Analysis of the two proposed AOF topologies

Given Figure 29, the three phase AOF contains mainly the main inverter switching at the fundamental frequency (400Hz in this case) since that each leg is connected in series with AOF block. Unlike Single phase, triplen harmonics got cancelled automatically in the Line to Line voltage. And that give an opportunity to produce another voltage injection waveform that include the triplen harmonics in the modulating signals. In Order to obtain a valid comparison between the conventional inverter case and the proposed AOF with triplen harmonic cancellation and without the triplen harmonic cancelation a simulation in MATLAB program have been conducted to present a comparison between the three cases that will be shown in later sections

3.3.1 Three phase AOF with triplen harmonic cancelation

When considering the output phase voltage of the main inverter referred to the DC link midpoint (square wave voltage shown on Fig. 3a. In which that the Triplen Harmonics (3rd , 9th, 27th ...) are canceled by AOF blocks.

The first case, the square wave voltage (1) contains all the odd harmonics (including all the triplen harmonics), hence the required injected voltage by the AOF is (1). The maximum voltage to be injected by the AOF is equal to half the DC link voltage of the main inverter.

$$v_{inv}(t) = \frac{2}{\pi} V_{DC} \sum_{n=1,3,5,7,9,\dots}^{\infty} \frac{\sin(n\omega t)}{n} \quad (50)$$

$$v_{AOF}(t) = \frac{-2}{\pi} V_{DC} \sum_{n=3,5,7,9,\dots}^{\infty} \frac{\sin(n\omega t)}{n} \quad (51)$$

$$v_{inv}(t) = \frac{2}{\pi} V_{DC} \left(\sin(\omega t) + \frac{\sin(3\omega t)}{3} + \frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} + \dots \right) \quad (52)$$

$$v_{AOF}(t) = -\frac{2}{\pi} V_{DC} \left(\frac{\sin(3\omega t)}{3} + \frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} + \dots \right) \quad (53)$$

In this case the resulting output voltage waveform will be a pure sinusoidal with a modulation index m_a of $\frac{4}{\pi}$ or 1.27 (as expressed in Figure 33) which is higher than the maximum modulation index achievable by Sinusoidal PWM '1' and Space Vector Modulation '1.1547', giving the chance to reduce the DC link working voltage, reducing the voltage rating of the DC link capacitor and switching devices.

$$v_O(t) = v_{inv}(t) + v_{AOF}(t) = \frac{4}{\pi} \frac{V_{DC}}{2} \sin(\omega t) \quad (54)$$

The switching function $S_{AOF}(t)$ that governs the AOF voltage is

$$S_{AOF}(t) = \frac{v_{AOF}(t)}{V_{DC AOF}} \quad (55)$$

$$S_{AOF}(t) = \frac{-\frac{2}{\pi} V_{DC} \sum_{n=3,5,7,9,\dots}^{\infty} \frac{\sin(n\omega t)}{n}}{\frac{V_{DC}}{2}} = \frac{-4}{\pi} \sum_{n=3,5,7,9,\dots}^{\infty} \frac{\sin(n\omega t)}{n}$$

$$i_{DC AOF} = i_o(t) S_{AOF}(t) = I_o \sin(\omega t) S_{AOF}(t) \quad (56)$$

Assuming sinusoidal load current

$$i_{DC AOF} = I_o \frac{4}{\pi} \left(\frac{\cos(2\omega t)}{6} - \frac{\cos(4\omega t)}{6} + \frac{\cos(4\omega t)}{10} - \frac{\cos(6\omega t)}{10} \dots \right) \quad (57)$$

By injecting harmonics voltage (3rd, 5th, 7th, etc.) current harmonics (2nd, 4th ...) are reflected on the DC link capacitor and we can find those harmonics components as demonstrated above. This will cause low order (2nd) harmonic ripples to appear on the DC link voltage of the AOF and hence the size of the capacitor is selected accordingly.

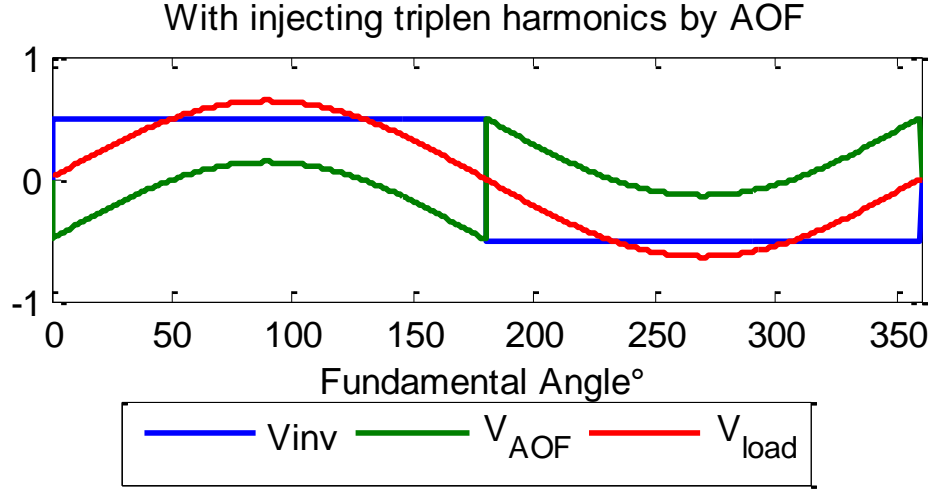


Figure 33 Voltage wave form of the main inverter voltage(V_{inv}), AOF injected voltage(V_{AOF}) and load voltage (V_{load})

3.3.1.1 Self-balancing strategy

The dc-link current equation has been illustrated in analysis section in

Equation 10. note that:

$$v_{inv}(t) = \frac{2}{\pi} V_{DC\ inv} \cdot \sum_{n=1}^{\infty} \frac{\sin(n\omega t)}{n} \quad (58)$$

$$S_{AOF}(t) = -\frac{2}{\pi} \left(\frac{\sin(3\omega t)}{3} + \frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} + \frac{\sin(9\omega t)}{9} + \dots \right) = -\frac{2}{\pi} \sum_{n=3,5,\dots}^{\infty} \frac{\sin(n\omega t)}{n} \quad (59)$$

To investigate DC Link capacitor response we need to formulate $v_{AOF\ DC\ link}$ with respect to $i_{AOF\ DC\ link}$ and that can be done by substituting equations 58 and 59 in 69:

$$i_o(t) = \frac{v_{inv}(t) + v_{AOF}(t)}{R}$$

$$i_o(t) = \frac{\left[\frac{2}{\pi} V_{DC\ inv} \sum_{n=1}^{\infty} \frac{\sin(n\omega t)}{n} \right] + [S_{AOF}(t) v_{DC\ AOF}(t)]}{R} \quad (60)$$

$$i_o(t) = \frac{\left[\frac{2}{\pi} V_{DC\ inv} \sum_{n=1}^{\infty} \frac{\sin(n\omega t)}{n} \right] + \left[\frac{2}{\pi} \sum_{n=3,5,\dots}^{\infty} \frac{\sin(n\omega t)}{n} v_{DC\ AOF}(t) \right]}{R} \quad (61)$$

$$i_{DC\ AOF}(t) = \frac{\left[\frac{2}{\pi} \sum_{n=3,5,\dots}^{\infty} \frac{\sin(n\omega t)}{n} \right] \left[\frac{2}{\pi} V_{DC\ inv} \sum_{n=1}^{\infty} \frac{\sin(n\omega t)}{n} \right] + \left[\frac{2}{\pi} \sum_{n=3,5,\dots}^{\infty} \frac{\sin(n\omega t)}{n} v_{DC\ AOF}(t) \right]}{R} \quad (62)$$

Then substituting equation 62 in equation 63 note that $K=0$ since that the DC Link is initially uncharged.

$$v_{DC AOF}(t) = \frac{1}{c} \int i_{DC AOF}(t) dt + K \quad (63)$$

To simplify the analysis only the DC components of the previous equation have been taken in consideration. Thus, when finding the mean of the previous equation the resulted equations is the same as equation 33 and 34 in single phase AOF case.

Table 10: The coefficients of V_{dcinv} and V_{dcaof} with respect to the presented injected harmonics for case 1

Harmonics Taken Into consideration	a_1	a_0
1 st , 3 rd	0.09	-0.045
1 st , 3 rd , 5 th	0.1224	-0.0612
1 st , 3 rd , 5 th , 7 th	0.1389	-0.0694
1 st , 3 rd , 5 th , 7 th , 9 th	0.1489	-0.0744
1 st , 3 rd , 5 th , 7 th , 11 th	0.1556	-0.0778
All odd Harmonics	0.1892	-0.0946

Similar to single phase AOF, it can be noticed from Table 10 that $a_0 = -\frac{1}{2}a_1$ in all cases. Moreover, almost half of the DC components generated from fundamental and 3rd only. On the other hand, when taking up to 11th harmonic into consideration we can reach 82% of the total DC Components. Therefore lower order harmonics are mainly responsible for charging the AOF DC Link Capacitors. And since that I_{DCAOF} equals $S.V_{DC AOF}(s)$ thus, we carry on the analysis in S domain

From the Final Value Theorem, the DC gain is the value of the transfer function when $s=0$ for stable transfer function. Thus, DC gain is equal $= \frac{a_0}{-a_1} = 1/2$ as been expressed in the previous table. And the response time constant $\tau = R*C$ which determines the settling time and the rising time as well. V_{DCAOF} Response for $V_{inv}=681$ step input of the design example in Table 9 ($R = 1.84\Omega$, $C = 286\mu F$) will results $V_{DCAOF} = 340.5v$ when excluding the lower harmonics and the ripple effects. The step response is expressed in MATLAB simulation as verified in the Next Figure 34.

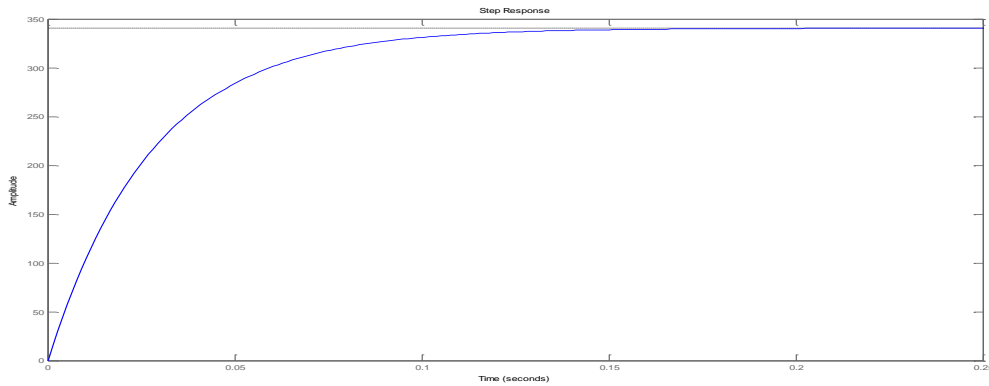


Figure 34 V_{dcaof} response to a step input of $V_{dcinv} = 681v$

Hence that the previous response (Figure 34) excludes the ripple effect caused by the even harmonics 2nd, 4th, 6th ...etc., Thus, by simply adding those ripple resulted from equation 64 to Figure 34 we can find DC Link normalized ripple waveform which is equal to the single phase AOF case.

$$v_{DC AOF}(t) = I_o \frac{4}{\pi c} \left(\frac{\sin(2\omega t)}{12} - \frac{\sin(4\omega t)}{12} + \frac{\sin(4\omega t)}{20} - \frac{\sin(6\omega t)}{20} + \frac{\sin(6\omega t)}{28} \dots \right) \quad (64)$$

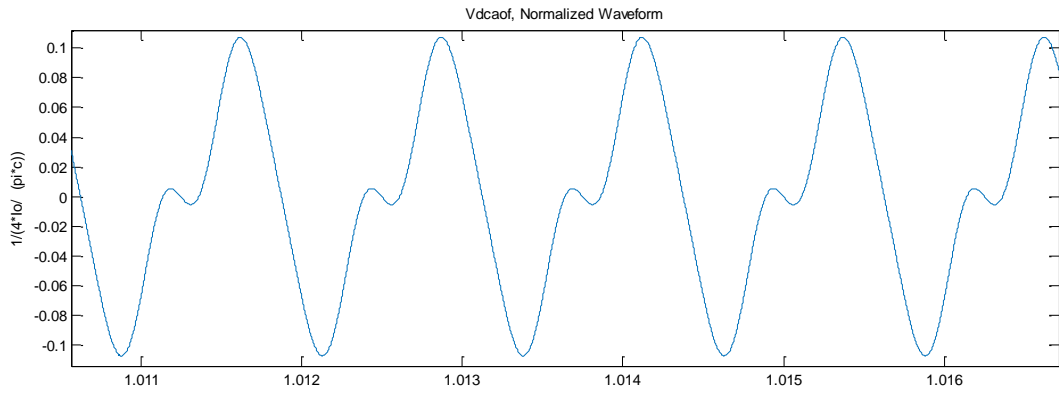


Figure 35 Three phase AOF dc-link ripple waveform

And the resulted addition of the AOF DC gain obtained from Figure 34 and ripple obtained from Figure 35 has been simulated in PSIM (Figure 36).

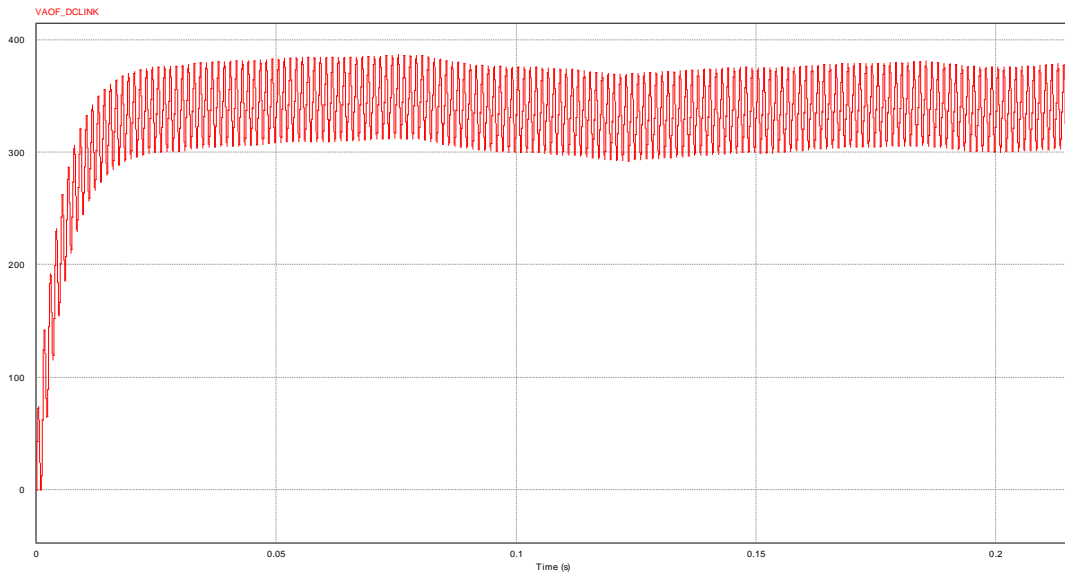


Figure 36 AOF final dc-link wave form after adding the ripples obtained using PSIM simulation

3.3.1.2 AOF dc-link design

In this study the DC Link is self-balanced in which it get charges until it reaches $V_{dc}/2$ and maintain its value there with only associating ripples generated from harmonics starting from 2nd harmonic similar to what was explained in in chapter 2. And that can be illustrated using equation 20 from single phase AOF case in which K equals $V_{dc}/2$ in steady state and the other terms associate the ripple to the $V_{dc}/2$ value.

Note $i_{DC_AOF}(t)$ Have been demonstrated in equation (57).

While ΔQ can be obtained by plotting equation (57) and integrate the area when the capacitor is charging note that the normalized ΔQ value for 400Hz fundamental frequency exactly equals to single phase AOF case obtained from chapter 2. The normalized $\Delta Q_{normalized} = 65.258 \cdot 10^{-6}$ Note that this number is linearly proportional to fundamental frequency.

$$\Delta Q_{normalized} \cdot I_o \cdot \frac{4}{\pi} = C\Delta V_{AOF_DC} \quad (65)$$

And when dividing by the output phase voltage (Peak) V_o the following equation will be resulted

$$\Delta Q_{normalized} \cdot \frac{I_o}{V_o} \cdot \frac{4}{\pi} = \frac{C\Delta V_{AOF_DC}}{V_o} \quad (66)$$

Hence that:

$$V_{dc} = \frac{2\sqrt{2} \cdot V_{ab_rms}}{m_a \sqrt{3}} \quad (67)$$

$$\text{Then } V_{dc} = \frac{2 \cdot V_{a0}}{m_a} \quad (68)$$

And $V_{DC_AOF} = \frac{V_{DC}}{2}$ as attained from pervious section. Moreover, $V_o = V_{a0}$

Then

$$V_o = V_{DC_AOF} \cdot m_a \quad (69)$$

Substituting equation 69 in 66 will lead to below equation

$$\Delta Q_{normalized} \cdot \frac{I_o}{V_o} \cdot \frac{4}{\pi} = \frac{C \cdot \Delta V_{AOF_DC}}{V_{DC_AOF} \cdot m_a} \quad (70)$$

For resistive load the capacitance can be computed using this equation:

$$C = \frac{4}{\pi} \cdot \frac{m_a \cdot \Delta Q_{normalized}}{R \cdot \frac{\Delta V_{AOF_DC}}{V_{AOF_DC}}} \quad (71)$$

For the given design example from Table 9 the DC Link can be found to be

$$C = 286 \mu\text{F (for 20\% ripple and } m_a=1.274)$$

3.3.1.3 Passive filter design

Considering the design parameters in Table 9 the inductance value can be obtained in the same manner as conventional inverter by using equation 41. However, the voltage of the AOF is one half the main DC-link giving a inductor reduction advantage by a factor of 2. Moreover, the switching frequency is 5 times more due to high performance switching used in AOF as a result the inductance value will be further reduced by a factor of 5. Therefore the inductance is 10 times smaller than conventional 3 phase inverter note that $L = 18\mu\text{H}$.

$$L \geq \frac{\frac{V_{dc}}{2}}{8 \cdot f_{sw} \cdot 0.2 \cdot i_{peak}} \quad (72)$$

To find the filter capacitor value a proper resonance frequency can be selected given equation 42.

Assuming that the hardware switching frequency capability is $f_{sw} = 50\text{Khz}$ then, $f_{res} = 10\text{KHz}$, and the capacitance can be found using the equation 43 and 44 hence that the resulted c is $15\mu\text{F}$.

Similar to 3 phase inverter, THD is assumed to be equivalent to the gain of the 2nd order LC filter at the switching frequency since that all harmonics components between the fundamental and the switching frequency equals to zero according to Pulse Width Modulation operation. Then the filter gain H can be found using equation 47

$H = 3.9\%$ then THD is $< 5\%$ which is complies with industrial IEEE standards.

Finally 3 phase AOF topology have been simulated in MATLAB considering Table 9 specification and the designed LC-Filter and DC Link Values as demonstrated in Figures 37, 38 and 39.

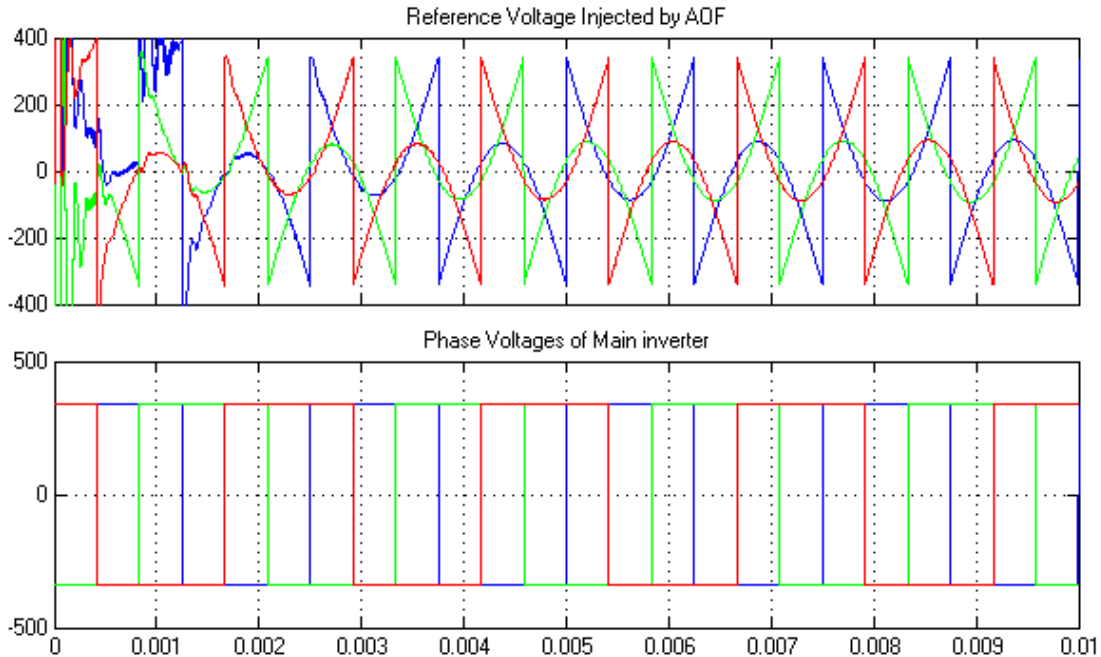


Figure 37 Reference voltage injected by AOF on top, phase voltage of main inverter in bottom

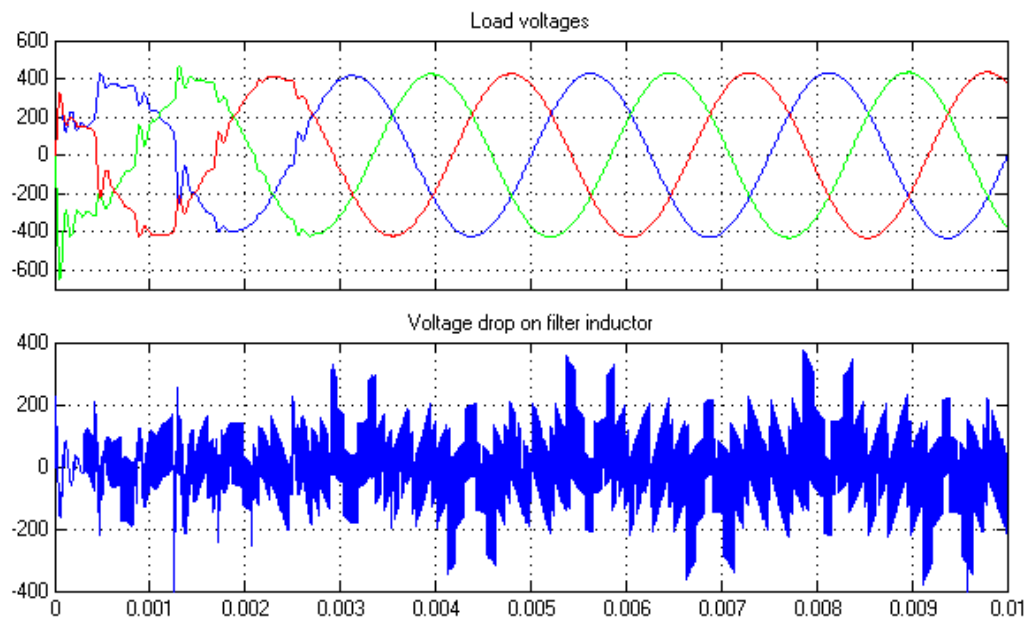


Figure 38 Load voltage for the 3 phases on top, voltage drop on the filter inductor for one of the phases

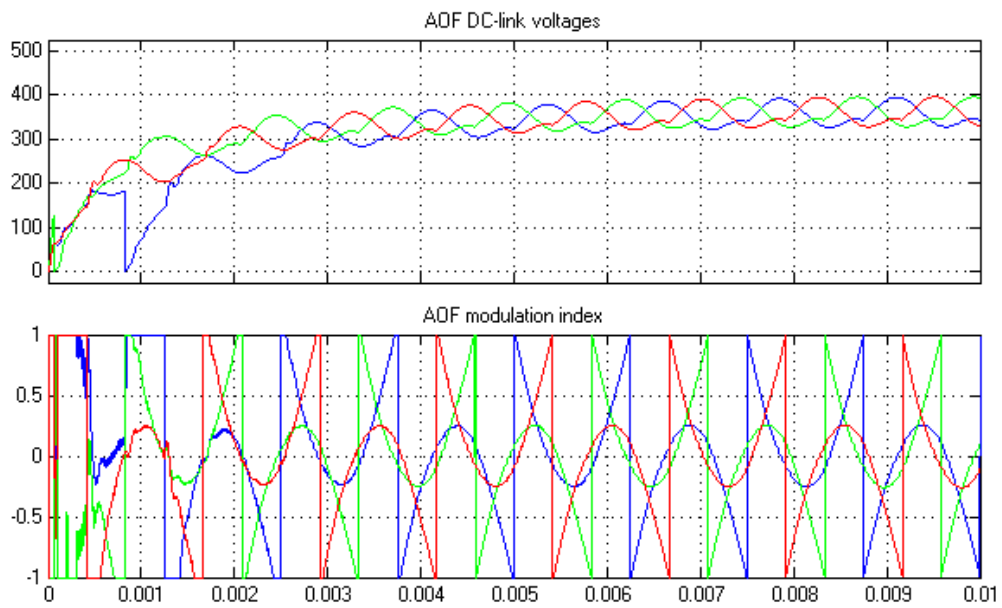


Figure 39 AOF dc-link voltages on top, and AOF modulation index in bottom

3.3.2 Three phase AOF without triplen harmonic cancelation

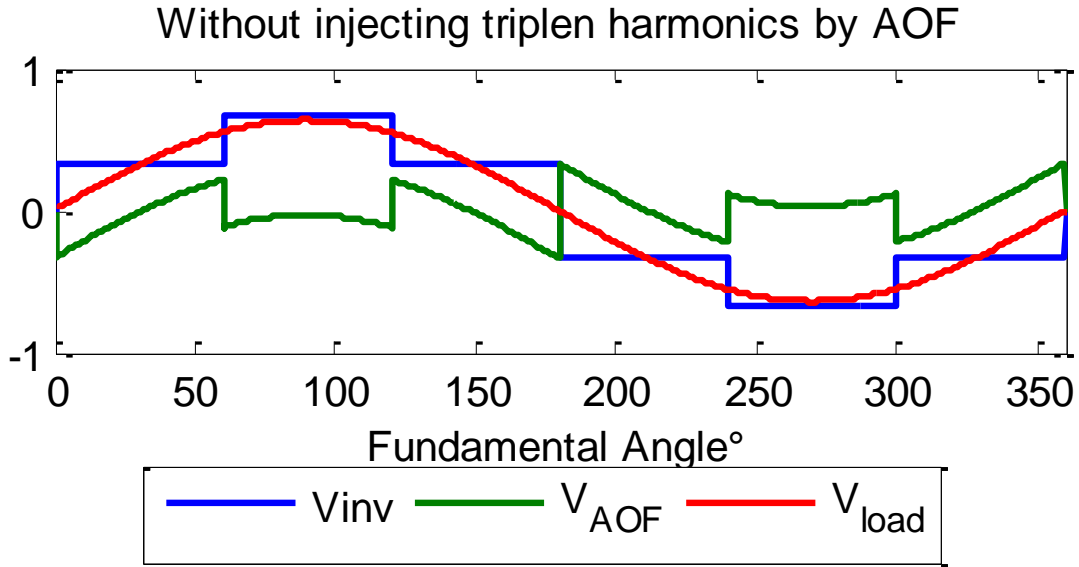


Figure 40 Three phase AOF voltage waveforms without injecting triplen harmonics

The difference between this cases and the previous proposed case is the presence of the triplen harmonics [27] and requiring the AOF to cancel these harmonic components or not. When considering the output phase voltage of the main inverter as referred with respect to the neutral point of a 3phase load (six-step voltage shown on Figure 40, since that the triplen harmonic is not canceled by AOF, the six-step voltage (equation 75) contains all the odd harmonics (except the triplen harmonics), hence the required injected voltage by the AOF is (2). The maximum voltage to be injected by the AOF is equal to 1/3 the DC link voltage of the main inverter.

$$v_{inv}(t) = \frac{2}{\pi} V_{DC} \sum_{n=1,5,7,11\dots}^{\infty} \frac{\sin(n\omega t)}{n} \quad (73)$$

$$v_{AOF}(t) = \frac{-2}{\pi} V_{DC} \sum_{n=5,7,11\dots}^{\infty} \frac{\sin(n\omega t)}{n} \quad (74)$$

$$v_{inv}(t) = \frac{2}{\pi} V_{DC} \left(\sin(\omega t) + \frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} + \frac{\sin(11\omega t)}{11} \dots \right) \quad (75)$$

$$v_{AOF}(t) = -\frac{2}{\pi} V_{DC} \left(\frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} \dots \right) \quad (76)$$

The resulting output voltage waveform will be a pure sinusoidal with a modulation index m_a of $\frac{4}{\pi}$ or 1.27 which is higher than the maximum modulation index achievable by Sinusoidal PWM ‘1’ and Space Vector Modulation ‘1.1547’, giving the chance to reduce the DC link working voltage, reducing the voltage rating of the DC link capacitor and switching devices.

$$v_o(t) = v_{inv}(t) + v_{AOF}(t) = \frac{4}{\pi} \frac{V_{DC}}{2} \sin(\omega t) \quad (77)$$

The switching function $S_{AOF}(t)$ that governs the AOF voltage can be denoted as:

$$S_{AOF}(t) = \frac{v_{AOF}(t)}{V_{DC AOF}} \quad (78)$$

$$S_{AOF}(t) = \frac{\frac{-2}{\pi} V_{DC} \sum_{n=5,7,11\dots}^{\infty} \frac{\sin(n\omega t)}{n}}{\frac{V_{DC}}{3}} = \frac{-6}{\pi} \sum_{n=5,7,11\dots}^{\infty} \frac{\sin(n\omega t)}{n} \quad (79)$$

Due to power invariance (neglecting the converter losses), the DC link current of the AOF is:

$$i_{DC AOF} = i_o(t) S_{AOF}(t) = I_o \sin(\omega t) S_{AOF}(t) = \frac{v_{AOF}(t)}{V_{DC AOF}} \quad (80)$$

$$i_{DC AOF} = I_o \frac{6}{\pi} \left(\frac{\cos(4\omega t)}{10} - \frac{\cos(6\omega t)}{10} + \frac{\cos(6\omega t)}{14} - \frac{\cos(8\omega t)}{14} \dots \right)$$

By injecting harmonics voltage (5th, 7th, 11th ...) current harmonics (4th, 6th ...) are reflected on the DC link capacitor and we can find those harmonics components as

demonstrated above. This will cause low order (4nd) harmonic ripples to appear on the DC link voltage of the AOF and hence the size of the capacitor is selected accordingly.

3.3.2.1 Self-balancing strategy

For previous analysis, the DC-Link Capacitor was assumed to reach the $V_{DC}/3$ voltage value and after the transient time and then sustain that DC voltage which also associate ripple. The DC link current equation has been illustrated in Analysis Section in Equation 10.

$$v_{inv}(t) = \frac{2}{\pi} V_{DC\ inv} \cdot \sum_{n=1,5,7..}^{\infty} \frac{\sin(n\omega t)}{n} \quad (81)$$

$$S_{AOF}(t) = -\frac{6}{\pi} \left(\frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} + \frac{\sin(11\omega t)}{11} \dots \right) = -\frac{6}{\pi} \sum_{n=5,7,11...}^{\infty} \frac{\sin(n\omega t)}{n} \quad (82)$$

To investigate DC Link capacitor response we need to formulate $v_{AOF\ DC\ link}$ with respect to $i_{AOF\ DC\ link}$ and that can be done by substituting equations 81 and 82 in 83:

$$i_o(t) = \frac{v_{inv}(t) + v_{AOF}(t)}{R} \quad (83)$$

$$i_o(t) = \frac{\left[\frac{2}{\pi} V_{DC\ inv} \sum_{n=1,5,7...}^{\infty} \frac{\sin(n\omega t)}{n} \right] + [S_{AOF}(t) v_{DC\ AOF}(t)]}{R} \quad (84)$$

$$i_o(t) = \frac{\left[\frac{2}{\pi} V_{DC\ inv} \sum_{n=1,5,7...}^{\infty} \frac{\sin(n\omega t)}{n} \right] + \left[\frac{6}{\pi} \sum_{n=5,7,11...}^{\infty} \frac{\sin(n\omega t)}{n} v_{DC\ AOF}(t) \right]}{R} \quad (85)$$

$$i_{DC\ AOF}(t) = \frac{\left[\frac{6}{\pi} \sum_{n=3,5,..}^{\infty} \frac{\sin(n\omega t)}{n} \right] \left[\frac{2}{\pi} V_{DC\ inv} \sum_{n=1,5,7...}^{\infty} \frac{\sin(n\omega t)}{n} \right] + \left[\frac{6}{\pi} \sum_{n=3,5,..}^{\infty} \frac{\sin(n\omega t)}{n} v_{DC\ AOF}(t) \right]}{R} \quad (86)$$

Then substituting equation 86 in equation 87 note that $K=0$ since that the DC Link is initially uncharged

$$v_{DC\ AOF}(t) = \frac{1}{c} \int i_{DC\ AOF}(t) + K \quad (87)$$

To simplify the analysis only the DC components of the previous equation have been taking in consideration. Thus, when the mean value of the previous equation 87 is obtained the resulted equation is the same as equation 33 attained from single phase AOF :

Table 11: The values of V_{dcinv} and V_{dcaof} average values with respect to the presented injected harmonics for case 2

Harmonics Taken Into consideration	a_1	a_0
1 st , 5 th	0.0729	-0.0243
1 st ,5 th ,7 th	0.11	-0.0367
1 st , 5 th , 7 th ,11 th	0.1251	-0.0417
All odd Harmonics	0.1782	-0.059

It can be noticed from the Table 11 that $a_0 = -\frac{1}{3}a_1$ in all cases. Moreover, 41% of the DC components generated from fundamental and 3rd only. On the other hand, when taking up to 11th harmonic into consideration we can reach 70% of the total DC Components. Therefore lower order harmonics are mainly responsible for charging the AOF DC Link Capacitors which was also the case for the previous sections. Not that

The DC gain $\frac{a_0}{-a_1}$ equal $\frac{1}{3}$ in this case.

V_{DCAOF} Response for step input of $V_{inv} = 681v$ assuming $R=1.832$ and $c=220\mu F$ driven from design example in Table 9 will results $V_{DCAOF} = 227v$ when excluding the lower harmonics and the ripple effects. The step response is expressed in MATLAB simulation as illustrated in Figure 41.

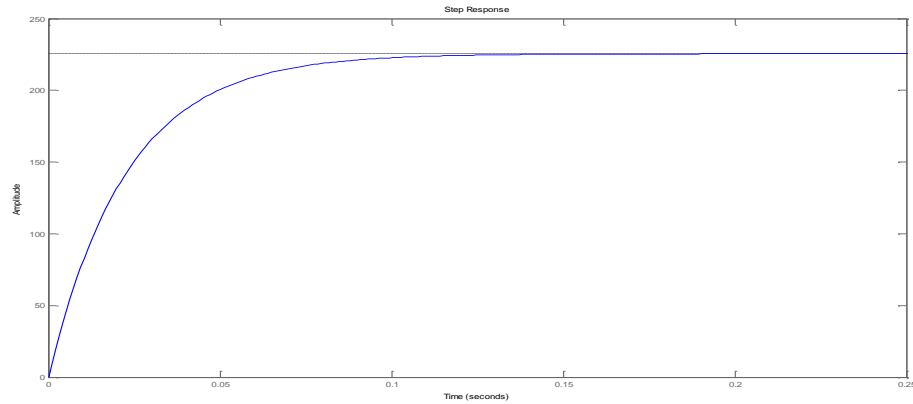


Figure 41 Vdcaof response to step input of Vdcinv =681v

Note that the previous response (Figure 41) excludes the ripple effect caused by the even harmonics 2nd, 4th, 6th...etc. Thus, by simply adding those ripple resulted from equation 88 to Figure 41 the DC Link normalized ripple waveform can be found as follows:

$$v_{DC\ AOF}(t) = I_o \frac{6}{\pi c} \left(\frac{\sin(4\omega t)}{20} - \frac{\sin(6\omega t)}{20} + \frac{\sin(6\omega t)}{28} - \frac{\sin(8\omega t)}{28} \dots \right) \quad (88)$$

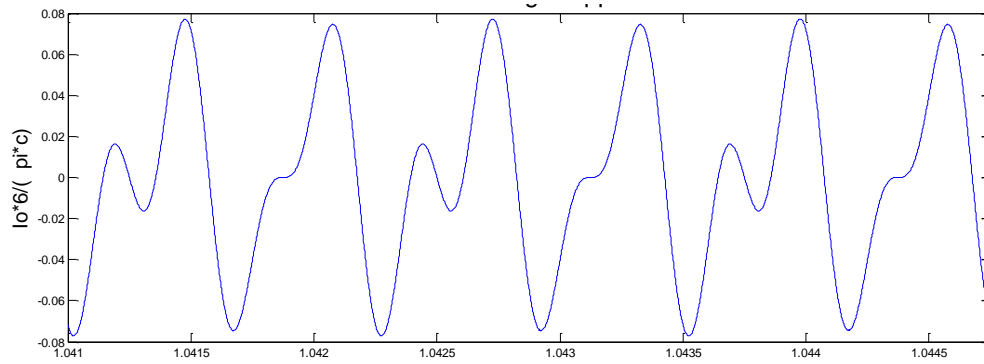


Figure 42 AOF dc-link ripple waveform in case of voltage injection excluding triplen harmonics

And the resulted addition of the AOF DC gain obtained from Figure 41 and ripple obtained from Figure 42 has been simulated in PSIM (Figure 43).

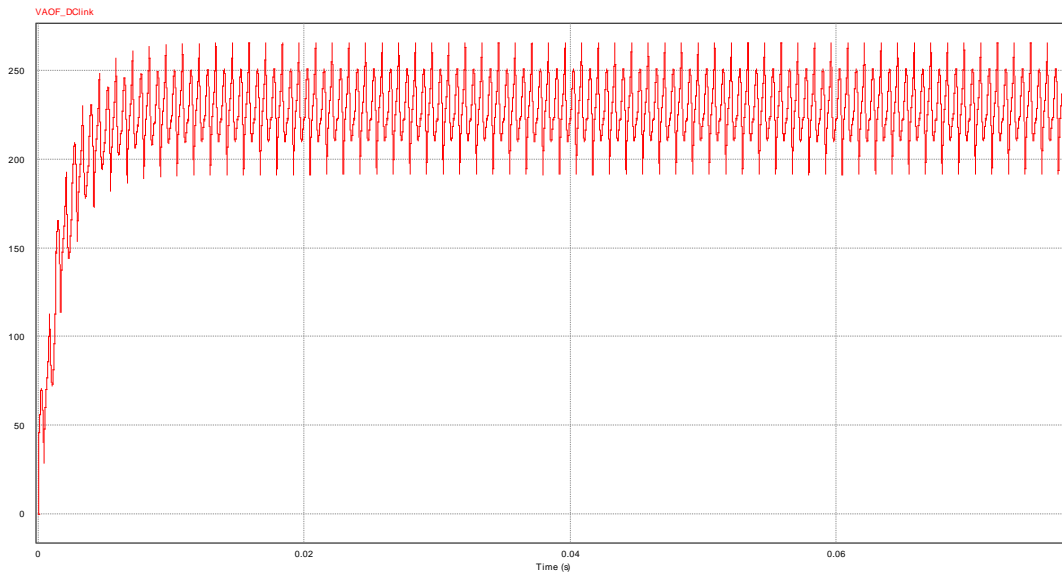


Figure 43 AOF final dc-link wave form after adding the ripples obtained from PSIM simulation

3.3.2.2 AOF dc-link design

In this study the DC Link is self-balanced in which it get charges until it reached V_{dc} and maintain its value there with only associating ripples generated from harmonics starting from 4th harmonic similar to what was explained in in chapter 2. And that can be illustrated in equation 20 in which K equals $V_{dc}/3$ in steady state and the other terms associate the ripple to the $V_{dc}/3$ value.

$i_{DC\ AOF}(t)$ have been demonstrated before in equation (80) and can be related ΔQ . ΔQ can be obtained by plotting equation (80) and integrate the area when the capacitor is charging as shown in the following Figure 44:

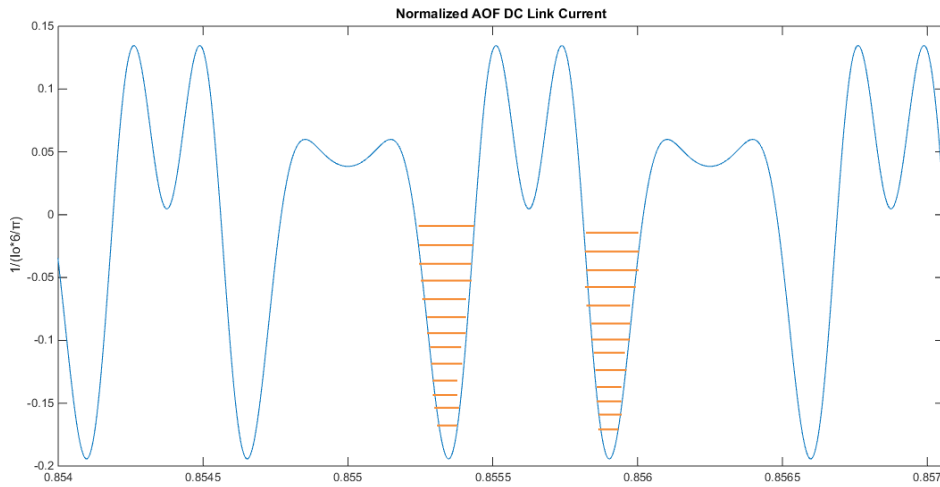


Figure 44 AOF normalized dc-link current

The shaded area can be calculated to obtain normalized ΔQ value for 400Hz fundamental frequency. Using MATLAB, the normalized $\Delta Q_{normalized} = 22.342 \cdot$

10^{-6} Note that this number is linearly proportional to fundamental frequency. Then substituting that number in equation 18

$$\Delta Q_{normalized} \cdot I_o \cdot \frac{6}{\pi} = C \Delta V_{AOF_DC} \quad (89)$$

And when dividing by the output phase voltage (Peak) V_o the following equation will be resulted

$$\Delta Q_{normalized} \cdot \frac{I_o}{V_o} \cdot \frac{6}{\pi} = \frac{C \Delta V_{AOF_DC}}{V_o} \quad (90)$$

And $V_{DC_AOF} = \frac{V_{DC}}{3}$ which is the minimum possible ratio between that main inverter DC Link and the three AOF DC Links. Moreover the following equations are carried out:

$$3 \cdot V_{DC_AOF} = \frac{2 \cdot V_o}{m_a} \quad (91)$$

$$V_o = \frac{3}{2} \cdot V_{DC_AOF} \cdot m_a \quad (92)$$

Substituting equation 92 in 90 will lead to below equation

$$\Delta Q_{normalized} \cdot \frac{I_o}{V_o} \cdot \frac{6}{\pi} = \frac{C \cdot \Delta V_{AOF_DC}}{\frac{3}{2} \cdot V_{DC_AOF} \cdot m_a} \quad (93)$$

For resistive load the capacitance can be computed using this equation:

$$C = \frac{9}{\pi} \cdot \frac{m_a \cdot \Delta Q_{normalized}}{R \cdot \frac{\Delta V_{AOF_DC}}{V_{AOF_DC}}} \quad (94)$$

For the given design example in analysis section the DC Link can be found to be

$$C = 220 \mu F \text{ (for 20\% ripple and } m_a=1.274)$$

3.3.2.3 Passive filter design

Considering the design parameters in Table 9 the inductance value can be obtained in the same manner as conventional inverter by using equation 41. However, the voltage of the AOF is one third the main DC link giving an inductor reduction advantage by a factor of 3. Moreover, the switching frequency is 5 times more due to high performance switching used in AOF as a result the inductance value will be further reduced by a factor of 5. Therefore the inductance is 15 times smaller than conventional 3 phase inverter. Hence that the filter inductor value can be obtained from equation (95):

$$L \geq \frac{\frac{V_{dc}}{3}}{8 \cdot f_{sw} \cdot 0.2 \cdot i_{peak}} \quad (95)$$

$L = 12\mu H$ for this case.

To find the filter capacitor value a proper resonance frequency can be selected given Equation 42.

Assuming that the hardware switching frequency capability is $f_{sw} = 50Khz$ then, $f_{res} = 10KHz$, and the capacitance can be found using 43 and 44. The resulted filter capacitance c is $21\mu F$.

Total Harmonic Distortion (THD) can be assumed to be equivalent to the gain H (equation 47) of the 2nd order filter at the switching frequency since that all harmonics components between the fundamental and the switching frequency equals to zero due Pulse Width Modulation scheme. The resulted gain (H) is 4.2% then THD is less than 5% which is complies for most industrial applications.

Finally 3 phase AOF topology have been simulated in MATLAB considering Table 9 specification and the designed LC-Filter and DC Link Values as demonstrated in Figures 45 and 46.

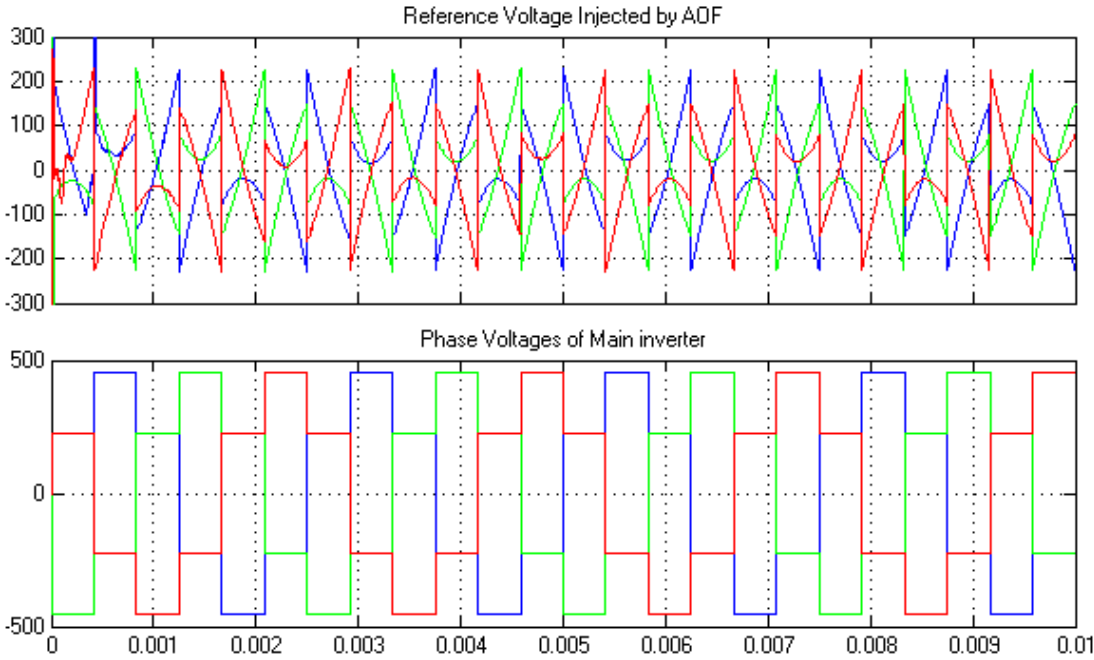


Figure 45 Simulation of reference voltages injected by AOF and phase voltages of the main in MATLAB

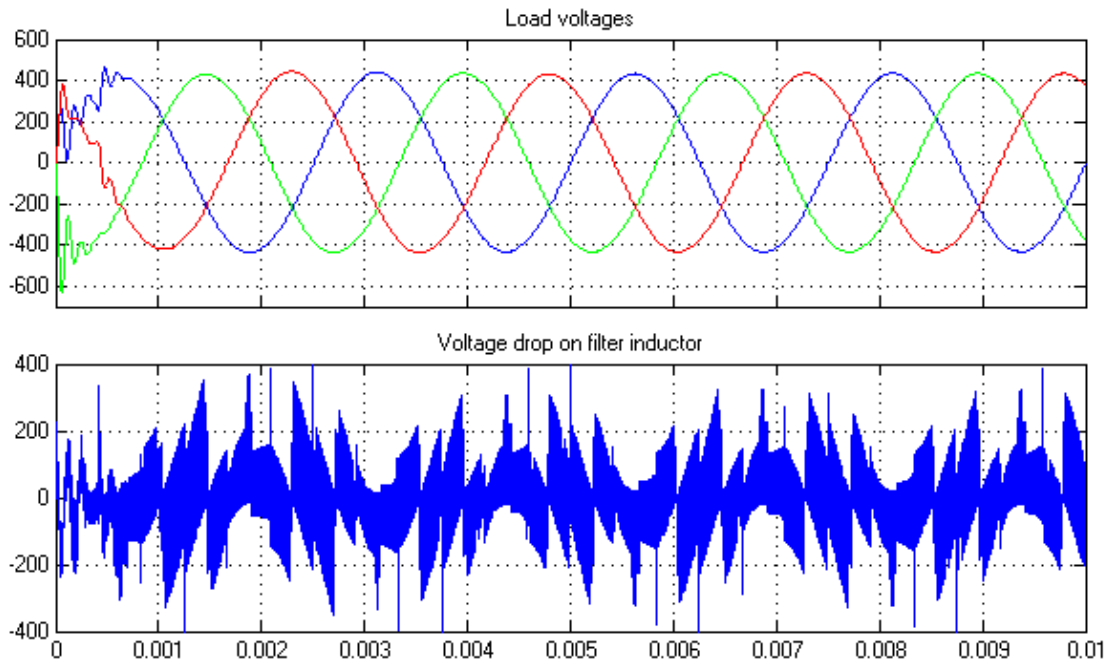


Figure 46 Simulation of load voltages and voltage from of the filter inductor in MATLAB

4. COMPARISON BETWEEN THE THREE METHODS

Since that the passive elements (L-C filters/DC links) have been analyzed for the conventional inverter (case 1), proposed AOF with triplen harmonic injection (case 2) and proposed AOF without triplen harmonic injection (case 3), a fair comparison can be made in terms of size. The inductor size in terms of volume and weight is proportional to the energy density and that concept can also be applied to the capacitors as shown in [28].

It is well know that energy stored in the inductor is:

$$E_L = \frac{1}{2} L i_{peak}^2 \quad (96)$$

Note that i_{peak} is the maximum peak current that can pass through the inductor when including current ripple. On the other hand energy stored in the capacitor can be denoted as:

$$E_c = \frac{1}{2} C v_{peak}^2 \quad (97)$$

Hence that v_{peak} is the maximum peak voltage across the capacitor when including voltage ripple. Generally, the inductor energy density ρ_L is less than the capacitor ρ_c although the same amount of energy is presented in both of them. Thereby, it's advised to use capacitive instead of inductive as energy storage when possible to offer more space. However, in this study the inductor is assumed to be 5 times bigger than the capacitors such that

$$\rho_c = 5 \cdot \rho_L \quad (98)$$

Table 12 summarizes the outcomes of size comparison for the aforementioned 3 topologies when excluding switches and heat sinks sizes.

Table 12: Comparison between the two proposed AOF topologies and the conventional high frequency three phase inverter

	Case1	Case2	Case 3
	Without AOF	Injected Voltage from square Waveform (3th,5th,7th..etc..)	Injected Voltage from 6 step Waveform (5th,7th..etc..)
Modulation Index (M)	1.1547	1.278	1.278
Harmonic In AOF DC Link	NA	2 nd	4 th
Harmonic In Main Inverter DC Link	25 th	4 th	6 th
Main Inverter SW Stress	Vdc	Vdc	Vdc
LC Filter	177 μ H-36 μ F	18 μ H-15 μ F	12 μ H-21 μ F
DC Capacitor Size	NA	286 μ F	220 μ F
DC Capacitor Voltage(Peak)	NA	400v	267v
Switching Frequency	10kHz	400Hz/ 50kHz	400Hz/ 50kHz
THD	<5%	<5%	<5%
Number of Switches	6	6+12	6+12
Energy Inductive (Filter) 240Amp_peak load in J	5.1 x 3	0.518 x 3	0.346 x 3
Energy Capacitive (DC Link) in Joule	NA	22.88 x 3	7.84 x 3
Energy Capacitive AC 440 Vpeak Load in Joule	3.5 x 3	1.452 x 3	2.03 x 3
LC Filter Size Assuming ($\rho_c = 5 \times \rho_L$)	(3.5 +5.1/ ρ) = 29	(1.452+22.88 +0.518/ ρ) =27	(2.03+7.84 +0.346/ ρ) = 11.6
Size index (Dividing by 29)	1	0.93	0.4

Given Table 12, the proposed 3 phase AOF without injected triplen harmonics proves to be 60% smaller than conventional 3 phase inverter. While the 3 phase AOF with injected triplen harmonics is 7% smaller due to the large added AOF DC Link. As a further step, the proposed topologies have been also tested under different switching frequency f_{sw} conditions as tabulated in Table 13:

Table 13: L-C filter size reduction with respect to f_{sw} increase

$f_{sw} = 50KHz$		$f_{sw} = 100KHz$		$f_{sw} = 200KHz$		$f_{sw} = 400KHz$	
Case 2	Case 3	Case 2	Case 3	Case 2	Case 3	Case 2	Case 3
L-C	L-C	L-C	L-C	L-C	L-C	L-C	L-C
18 μ H/15 μ F	12 μ H/21 μ F	11 μ H/6 μ F	7 μ H/9 μ F	6 μ H/3 μ F	4 μ H/4 μ F	3 μ H/2 μ F	2 μ H/2 μ F

The L-C filter size reduce significantly with switching frequency and that filter side reduction with further decrease the overall passive elements size index. A relationship between the size index and switching frequency have been obtained after combining data from Tables 12 and 13 as shown below Figure 47:

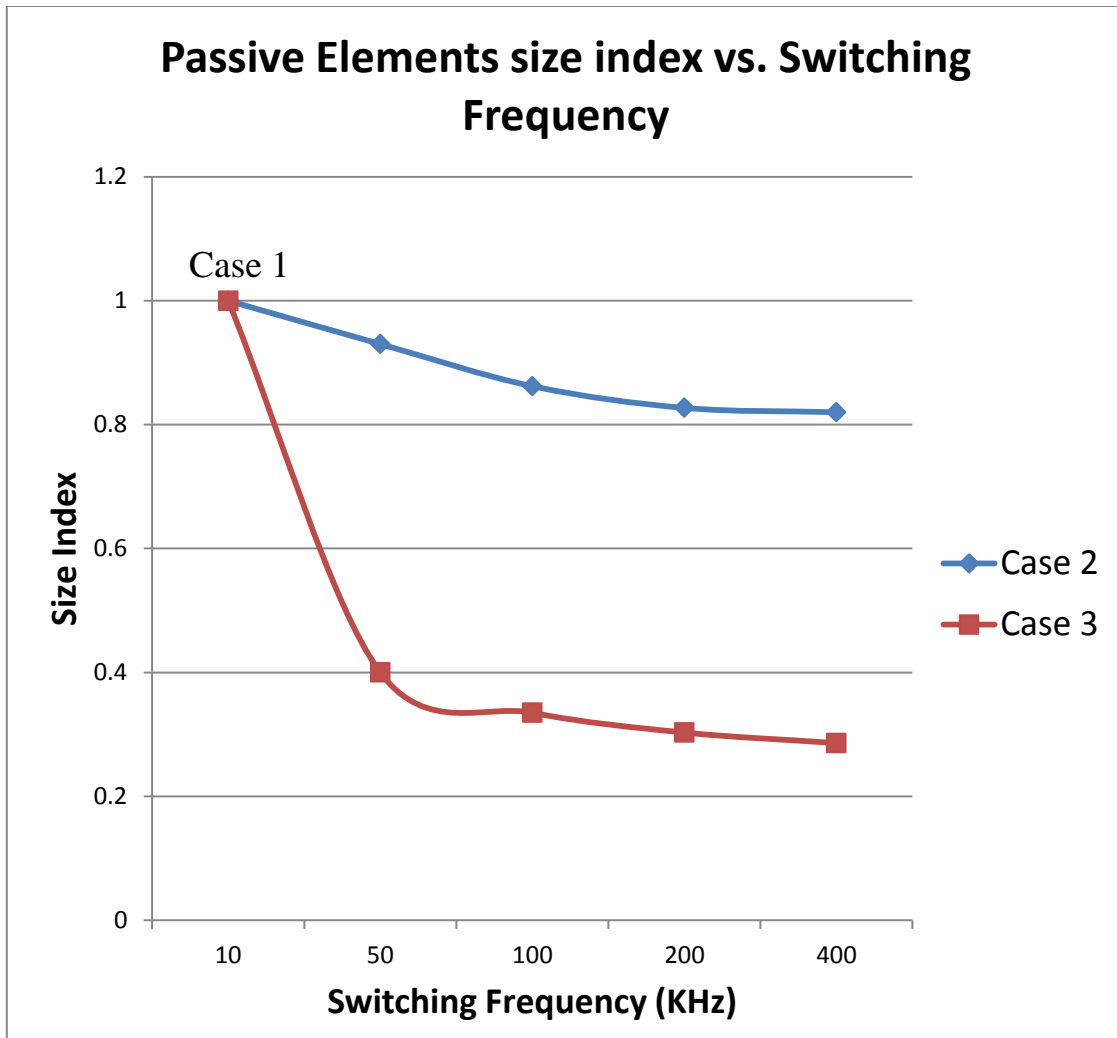


Figure 47 Passive elements size index vs. switching frequency

The overall passive elements of case 3 decrease the size of passive elements by up 71% in case of $f_{sw} = 400KHz$ while case 2 reduce the passive elements size by 20%.

5. SOFTWARE SIMULATION

5.1 Three phase AOF for resistive load

Three phases AOF have been simulated in PSIM under resistive load condition giving the following parameters as tabulated in Table 14 below:

Table 14: Design example

f_{sw}	Input DC to AOF	AOF DC Link	AOF Filter	Line to Line RMS Voltage	AC 3phase load
50Khz	681v	100μf	200μH, 1μF	530v	20kW

The performance of the 3 phase AOF without the triplen harmonics cancelation is illustrated in Figures 48 and 49 below since that the AOF DC Link capacitors are self-balanced of a value of $V_{dc}/3$.

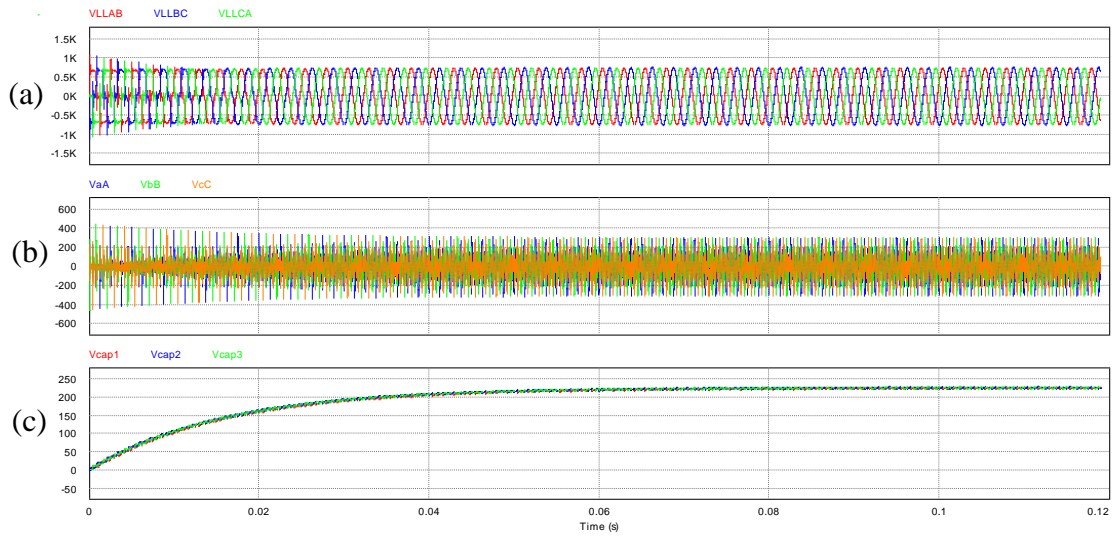


Figure 48 The performance of the 3 phase AOF with 3 phase resistive load THD (below 3%)

When zooming in Figure 48 we can observe high quality voltage output waveform (THD < 3) shown in Figure 49 (a) and the voltage subtraction stage waveform presented in Figure 49 (b). Also the ripple of the AOF DC Link is less than 5% Figure 49 (c).

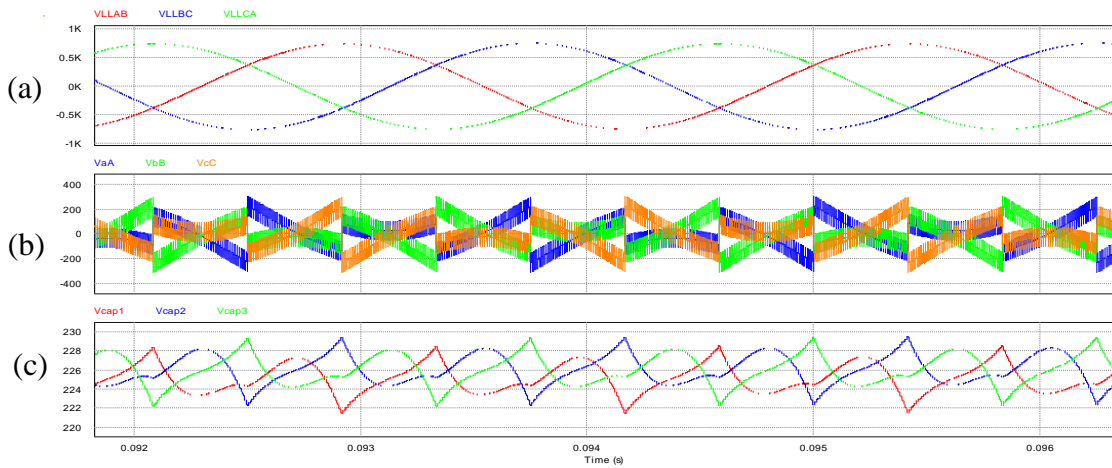


Figure 49 More insight figure of the previous Figure 48

Considering Main inverter DC Link current and AOF DC Link Current illustrated in Figure 50 (a) and Figure 50 (b) respectively, the harmonic distribution of those currents can be obtained by applying FFT which lead to Figure 51.

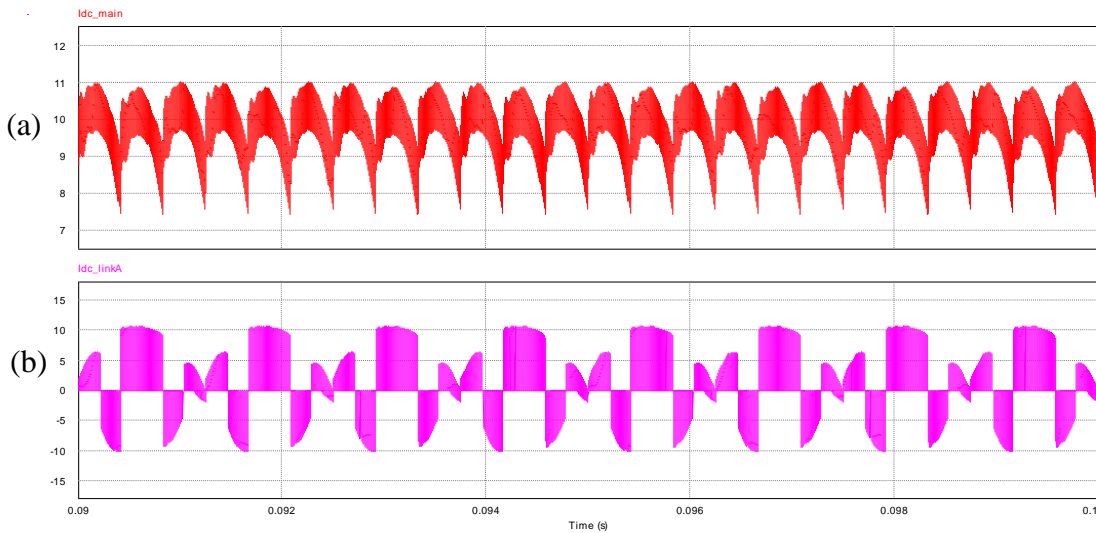


Figure 50 Main dc-link current on top and AOF dc-link current in bottom

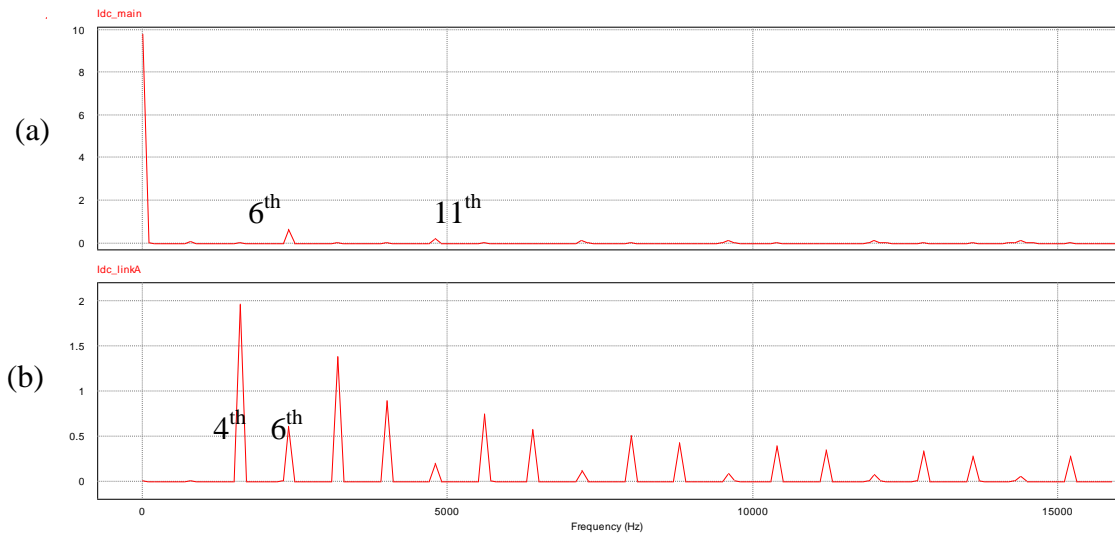


Figure 51 This figure shows the THD of the main dc current and AOF dc-link current since that the low harmonics are presented starting from 6th for main dc- link current while it starts from 4th for AOF dc-link current

Figure 51 shows the THD of the main DC current and AOF DC Link Current since that low order harmonics are presented starting from 6th for main DC LINK Current while it starts from 4th for AOF DC Link Current.

5.2 Three phase AOF for non-linear load condition

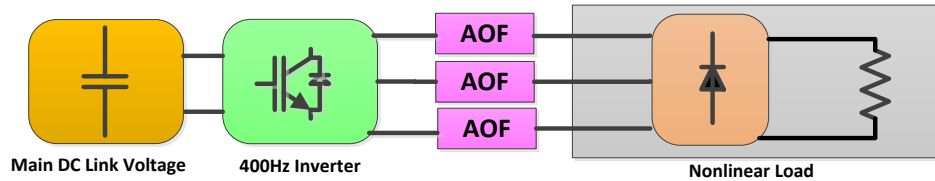


Figure 52 Three phase AOF block diagram for non-linear load condition

Non Linear load i.e. diode rectifier shown in Figure 52 involves variance of impedance though sinusoidal input is presented. Thus, when the input voltage to the 3 phase diode rectifier is sinusoidal the input current will be non-sinusoidal and that present harmonics that might disturb the system. Therefore VSCF with 3 AOF blocks have been tested under 3 phase diode rectifier non-linear load to analyze its performance. For Ideal 3 phase sinusoidal voltage input to a 3 Phase rectifier the current waveform will involve lower odd harmonics occur on: $2k \pm 3, k = 1, 2, 3 \dots$. Thus the lowest current harmonic presented is 6th and it's approximated magnitude is assumed to be 50% of the fundamental. Table 15 summarizes the components parameters selected for testing 3 phase sinusoidal output resulted from the 3 AOF blocks which feeds a 3 phase non-linear diode rectifier load. Note that that AOF is self-balanced at one third of the main DC input voltage value thus that the close loop control has not been used in this analysis. Small passive damping impedance in series with Filter inductors is needed to assist in neutralizing the added 3 phase nonlinear load harmonic effects [3]. The

schematic of PSIM circuit is shown in Figure 53 and the results are demonstrated in Figures 54,55 and 56.

Table 15: 3 phase AOF design parameters under 3 phase diode rectifier load

Fsw	Input DC to AOF	AOF DC Link	AOF Filter	Line to Line RMS Voltage	DC load	DC Output
50KHz	681v	100μF	200μH, 50μF	530v	20KW	718v

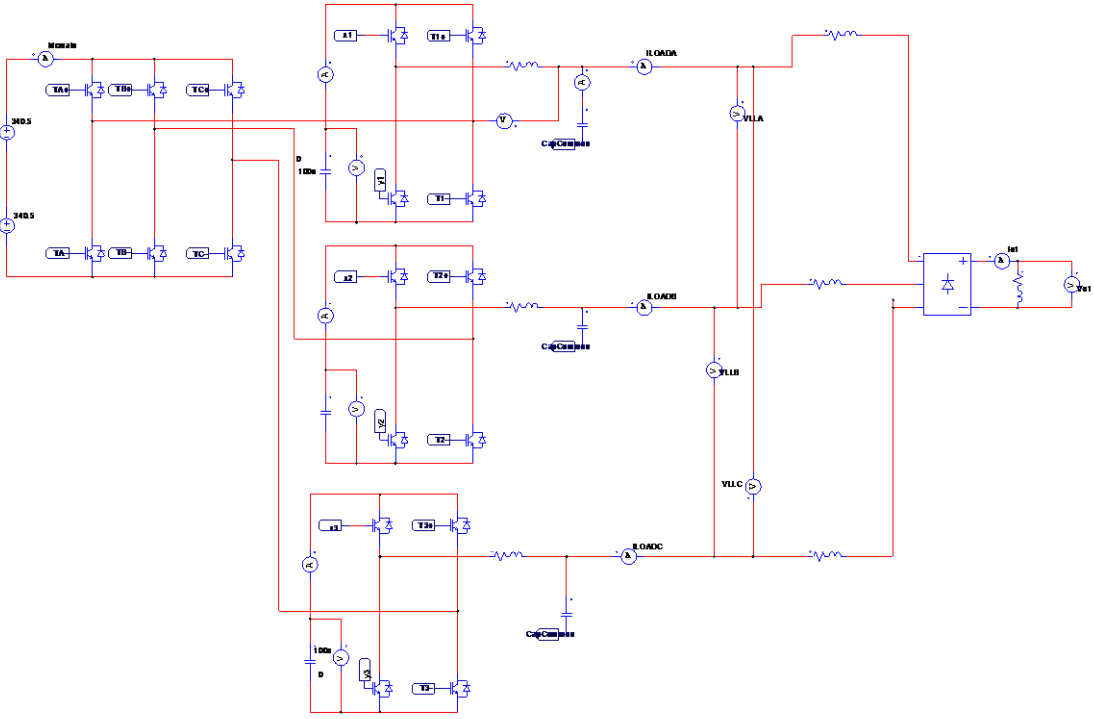


Figure 53 PSIM circuit schematic for 3 phase AOF with 3 phase diode rectifier that supply resistive load

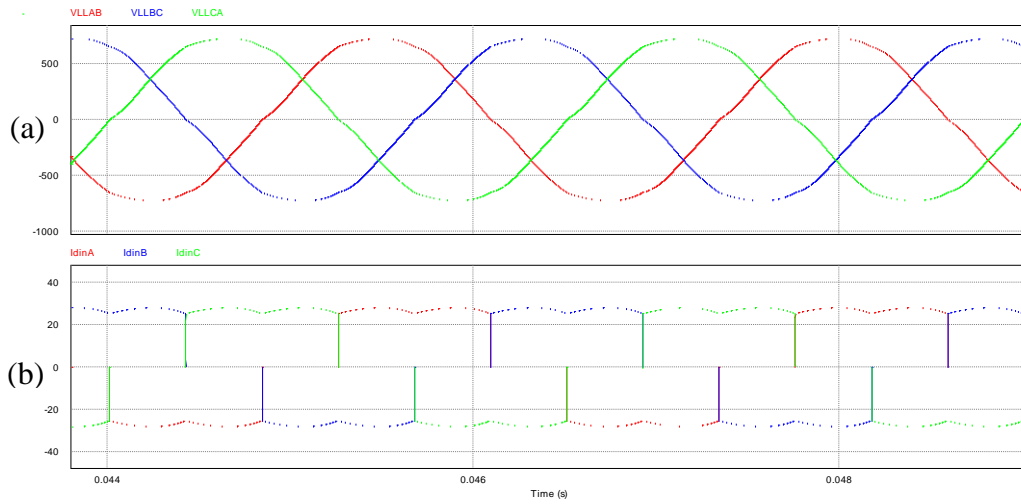


Figure 54 (a) Line to line output voltage from AOF (b) line current to the 3 phase diode rectifier. Although the 3 phase nonlinear load is presented still input voltage maintains a good quality voltage at THD less than 5%.

Next Figure 55 shows V_{LLAB} (a) with Respect to Line current I_{LA} (b) and the voltage injection stage waveform V_{aA} (c)

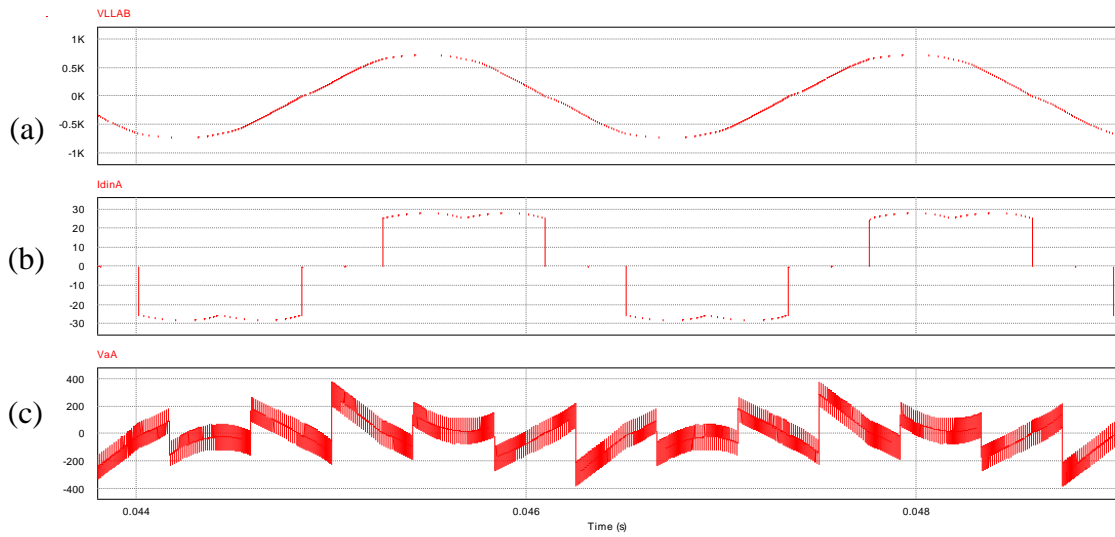


Figure 55 (a) The line to line voltage waveform (VLLAB). (b) line current ILA wave form (c) the voltage injection stage waveform V_{aA}

When observing the transient response of the three AOF DC link block voltages it can be noticed that the system is naturally stable at DC-Link voltage value of one third of the main input voltage as proved in Figure 56.

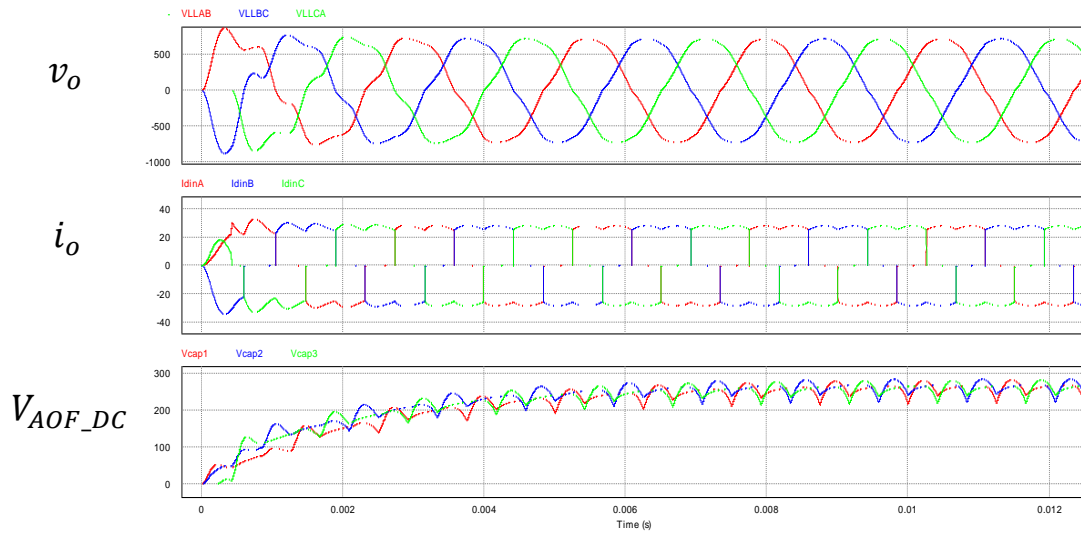


Figure 56 The transient response of the three AOF DC link block voltages

5.3 Three phase AOF under unbalanced load condition

Considering the design specification shown in Table 16 for an ideal balanced resistive load, the resulted simulated voltage waveforms are shown in Figure 57.

Table 16: Design example for unbalanced load condition

f_{sw}	Input DC to AOF	AOF DC Link	AOF Filter	Load RMS Voltage	AC load
50KHz	681v	40uF	5μH, 10μF	480v	20kW

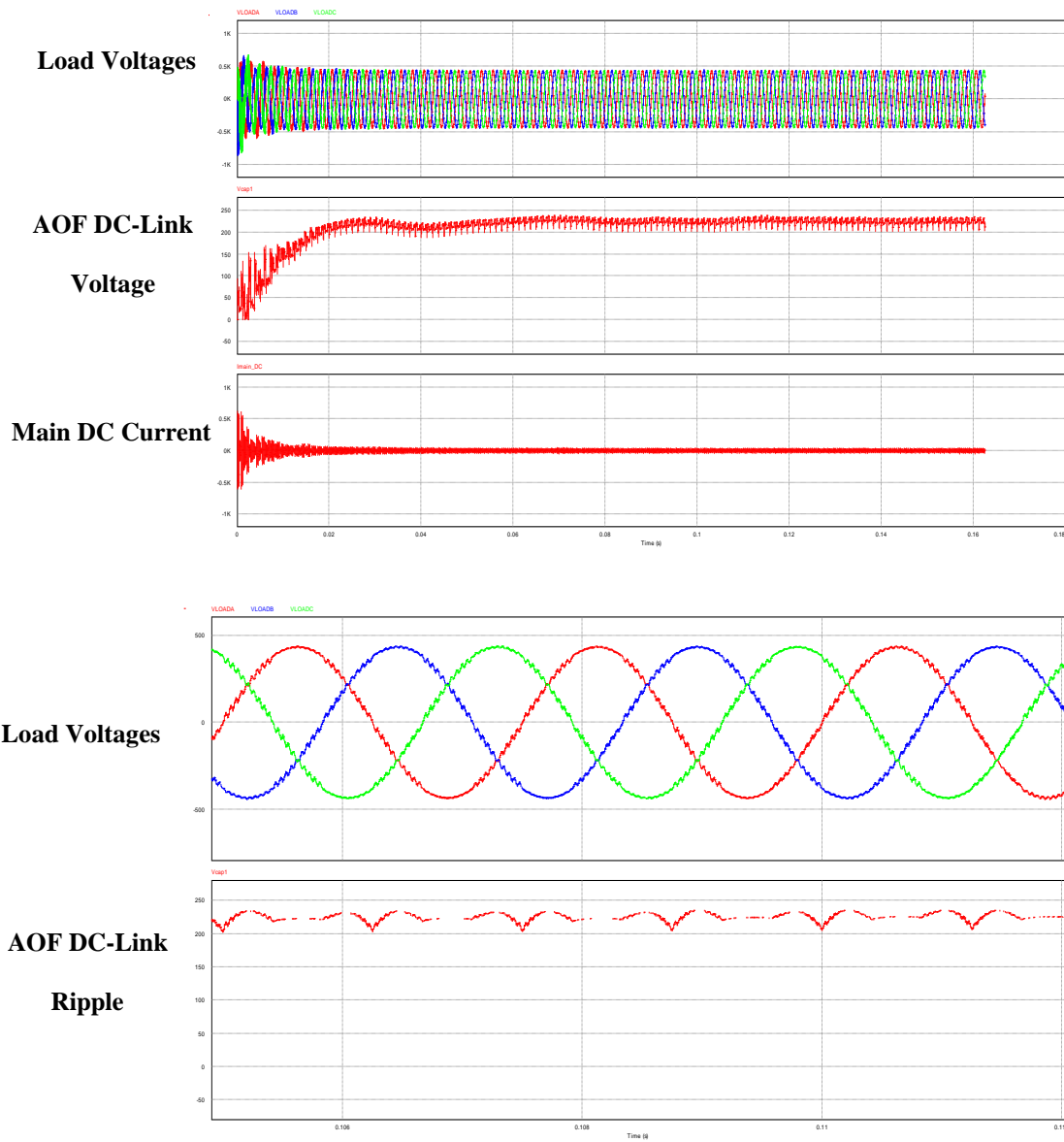


Figure 57 The design example waveforms before the unbalanced load

Since that the balance load condition implies that:

1. All 3 loads consumes the same amount of power
2. All 3 load have the same frequency
3. All 3 loads are 120° phase from each other's

In this study, only the first condition have been analyzed.

5.3.1 When one of the phases of Y connected resistive load draw more power than the others (case 1)

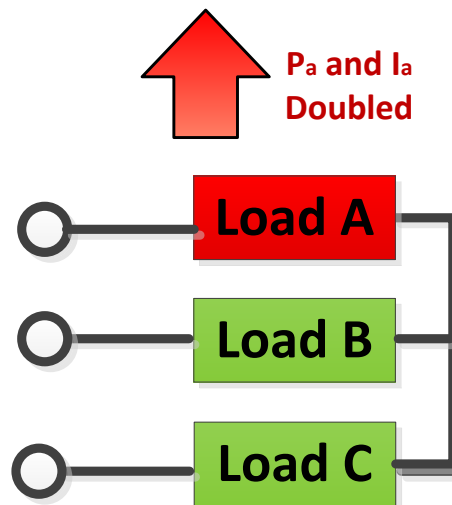


Figure 58 Case 1 load representation

When simulating condition shown in Figure 58 in PSIM (Figure 59) the resulted line to line voltage is not affected though the phase current and phase voltage is disturbed as shown in Figure 60.

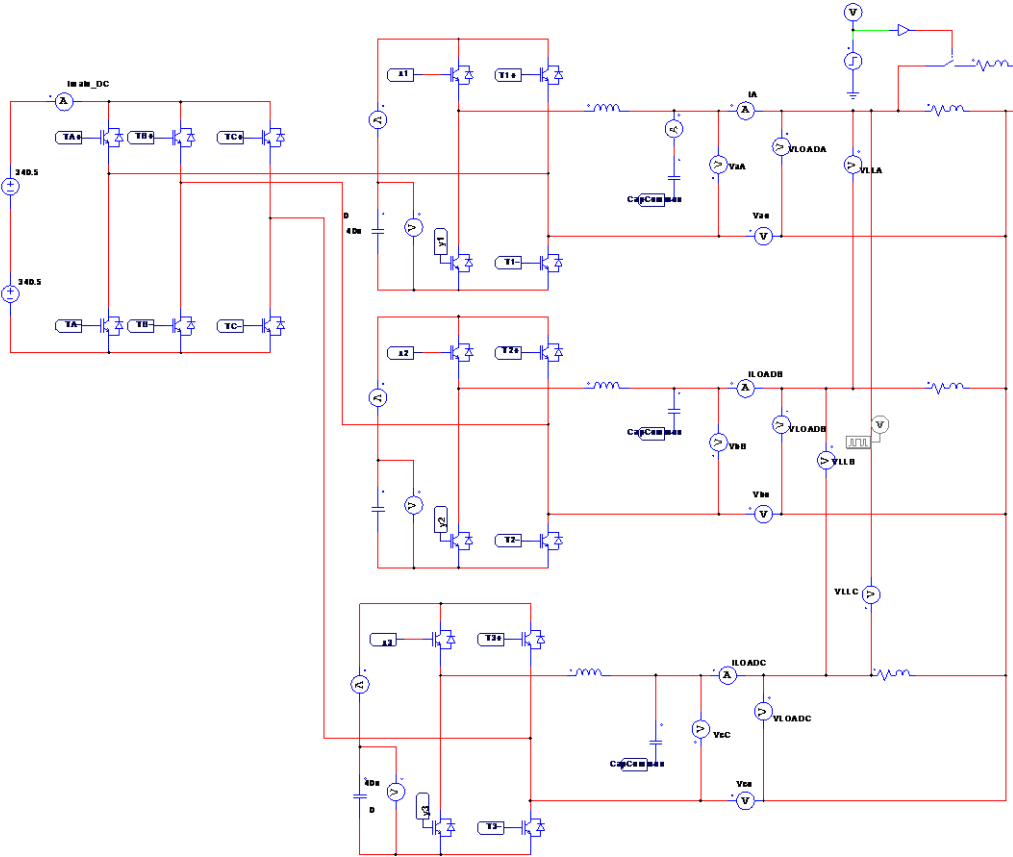


Figure 59 Case 1 representation in PSIM

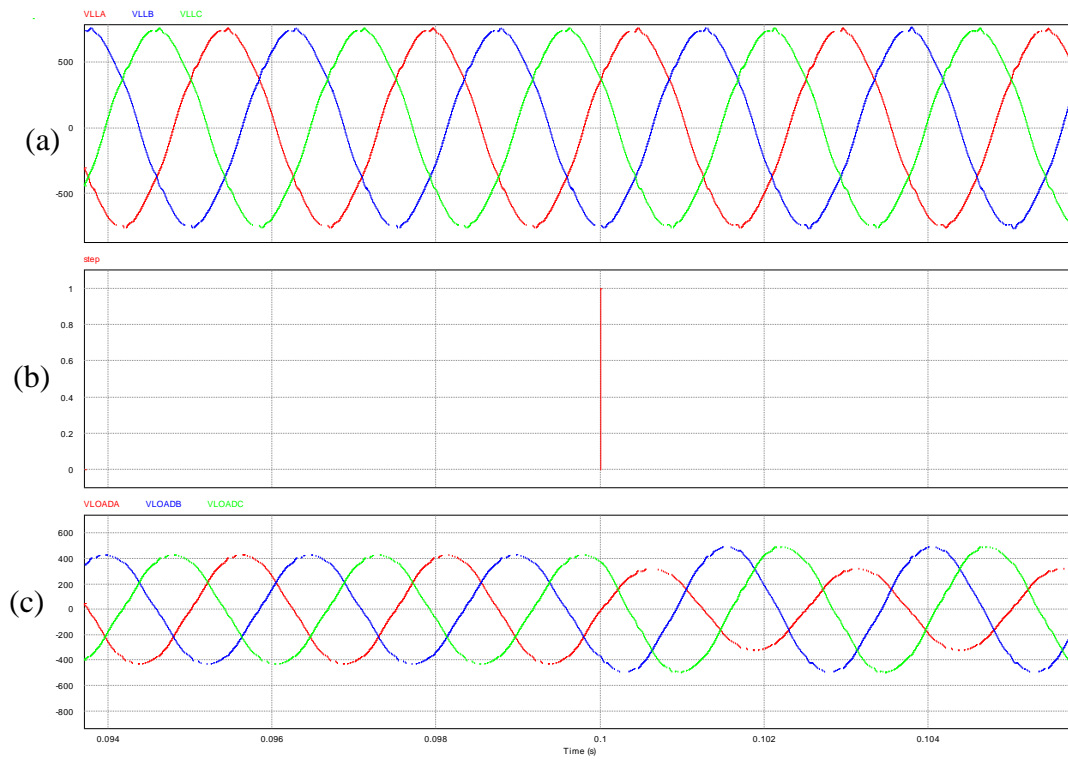


Figure 60 (a) Shows the line to line voltages of the load (b) the time in which over loading in phase A occur (c) the phase voltage which is affected by the unbalanced condition

5.3.2 When one of the three phase is disconnected for delta connected resistive load
(case 2)

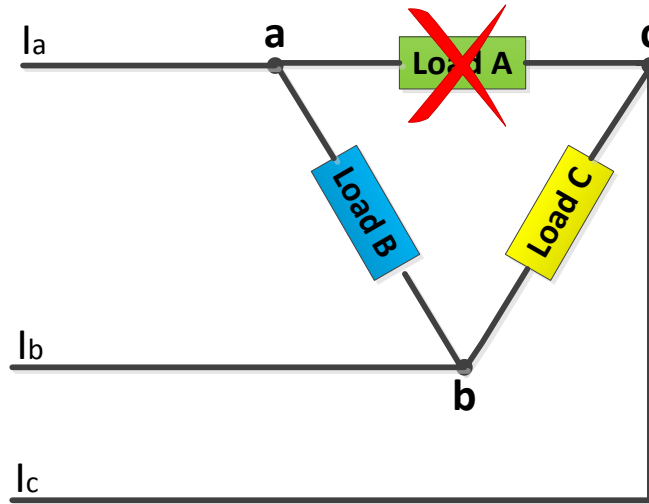


Figure 61 Case 2 load representation

If a fault occur in delta connected ac load in which one of the phases load draw zero current (Figure 61) as simulated in PSIM (Figure 62) the resulted output line to line voltage is maintained within 3.5% of the pre-fault value and 5 % THD. On the other hand the phase current is severely effected as expected. This performance is shown in Figure 63.

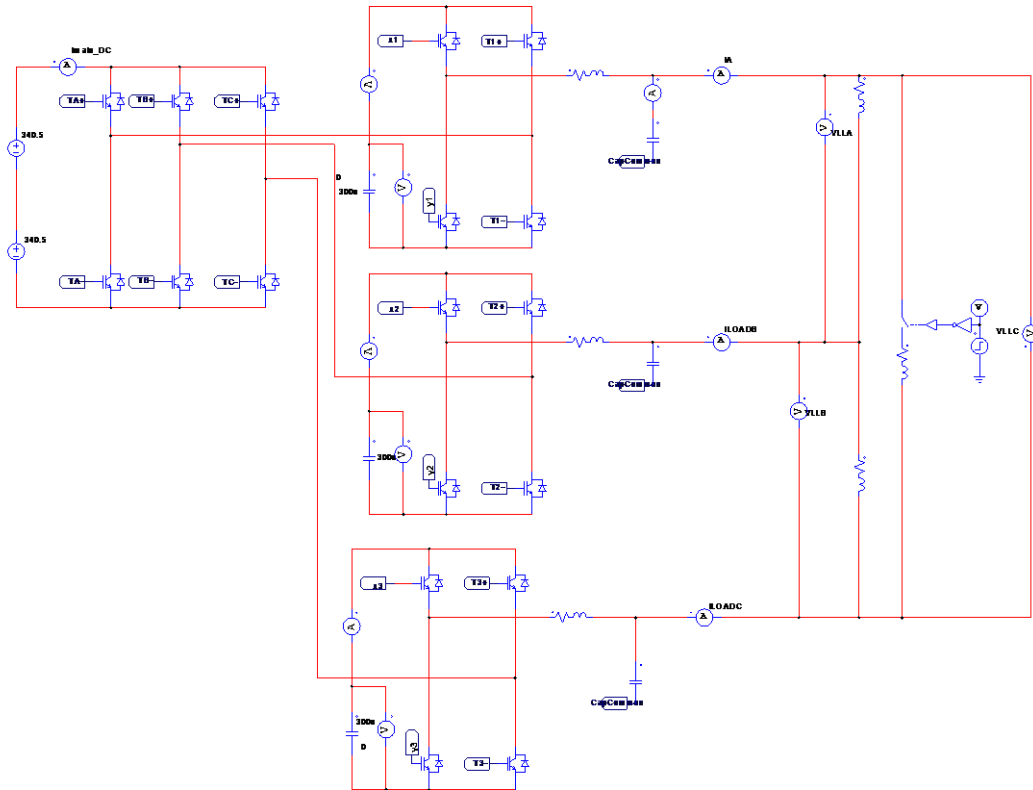


Figure 62 PSIM schematic for case 2

It can be notice from Figure 63 that VLLA and VLLB slightly increased by (20v about 3.2%) while the VLLC in which the faults occurs has been increased by 80v about 12.9%. While the line Currents A and C decreases by 41.5% though the line B currents remain the same.

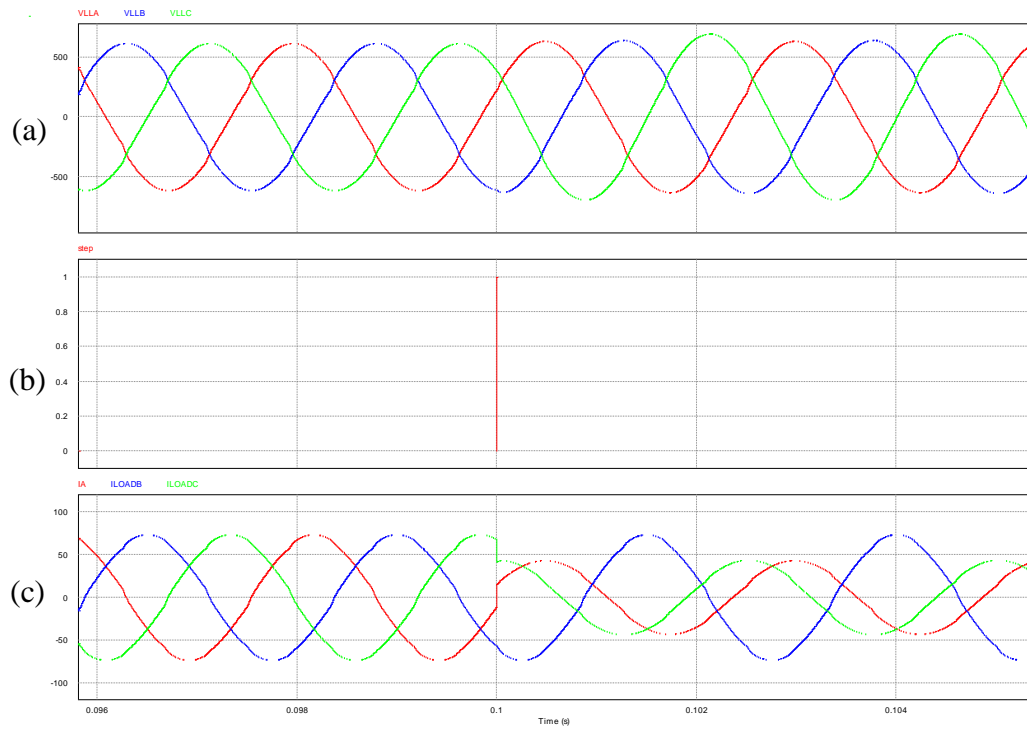


Figure 63 Unbalanced load case 2 results (a) VLLA,VLLB and VLLC (b) fault response (c) the line currents

6. MAIN INVERTER VOLTAGE CONTROL METHODOLOGY

Since that Pulse with modulation techniques can be classified into 4 main types:

- Sinusoidal PWM (SPWM)
- Selective Harmonic Elimination PWM (SHEPWM)
- Space Vector PWM (SVPWM)
- Delta Modulation PWM

In this study only SPWM have been used for the conventional inverter case in chapter 2, while SHEPWM and SVPWM modulation will be considered in this chapter for their competitive advantages compared to other topologies.

6.1 Adding one firing angle to the main inverter using SHPWM

Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) is a programmed pulse width modulated technique in which the magnitude of the fundamental components is controlled as well selected harmonics to be eliminated. And the analysis can be obtained graphically in which the angles α_0 , α_1 , α_2 , α_3 ,..... α_n are assumed to be variable as shown in Figure 64[29-31]:

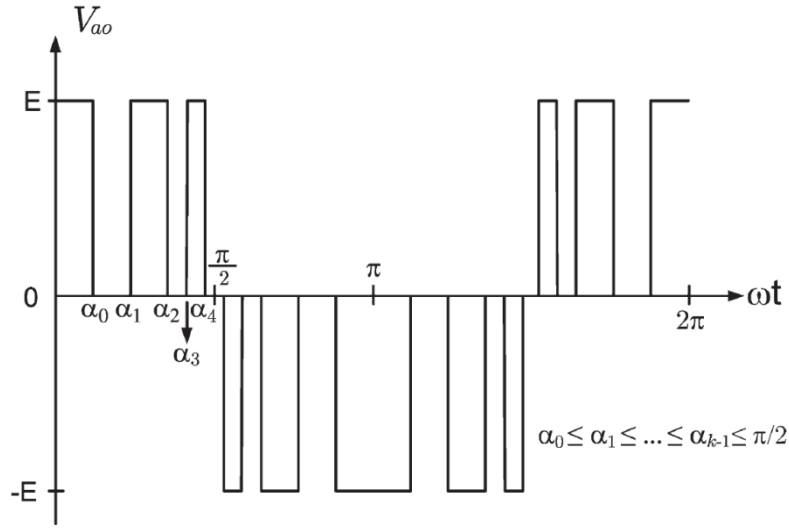


Figure 64 Three-level preprogrammed PWM switching pattern with five switching angles (α_0 , α_1 , α_2 , α_3 , and α_4). (© IEEE 2010 [29]- Adapted with permission)

Then when applying FFT for the waveform shown on Figure 64 the following

Fourier coefficient will be resulted

$$a_n = \frac{4}{n\pi} [1 + 2 \sum_{k=1}^N (-1)^{-k} \cos(n\alpha_{k-1})] \quad (99)$$

$$b_n = 0 \quad (100)$$

Equation (99) has N variables (α_0 to α_{k-1}) thus to obtain a set of solution by N-1 equations to zero the harmonics and assign a specific value of the magnitude of the fundamental such that [89-91]:

$$\alpha_0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_{k-1} < \frac{\pi}{2} \quad (101)$$

Then a set of nonlinear equation will be resulted to obtain the values of those angles as shown below

$$\begin{aligned}
2 \cos(\alpha_0) - 2\cos(\alpha_1) \dots + 2(-1)^{N+1} \cos \alpha_N &= \frac{\pi a_1}{2} + 1 \\
2 \cos(5\alpha_0) - 2\cos(5\alpha_1) \dots + 2(-1)^{N+1} \cos 5\alpha_N &= 1 \\
\cdot & \\
\cdot & \\
\cdot & \\
2 \cos(x_1 \alpha_0) - 2\cos(x_1 \alpha_1) \dots + 2(-1)^{N+1} \cos x_1 \alpha_N &= 1
\end{aligned} \tag{101}$$

When finding the solution of the following set of equation hence that only one angle is needed to control the fundamental frequency while any additional angle can eliminate one harmonics i.e. to eliminate 5th and 7th and obtain a fundamental amplitude of 80% of the normal value 3 angles α_0 , α_1 and α_2 are required.

The Programmed PWM Technique Advantages are [31]:

- 1- High Quality Output Voltage
- 2- About 50% reduction in switching frequency compared to SPWM
- 3- Suitable for Higher voltage and higher power inverter systems, where switching frequency is a limitation.
- 4- Higher voltage gain to over modulation
- 5- Reduced size of dc-link components
- 6- Selective elimination of lower order harmonics guarantee avoidance of resonances with external line filtering networks

Thus, Deploying Programmed PWM concept on the main inverter shown in Figure 64 will allow an output voltage control feature. To demonstrate the Programmed

PWM affectivity in the proposed topology angles 0, 6, 12, 30 and 45 have been simulated in PSIM expressed in Figures 65 and 66 using parameters selected from Table 17.

Table 17: Proposed topology designed parameters for programmed PWM technique

Main Inv. f_{sw}	AOF f_{sw}	Input DC to AOF	AOF DC Link	AOF Filter	L-L RMS Voltage	AC load
400Hz	50KHz	100v	100uF	15μH, 50μF	100v	167W

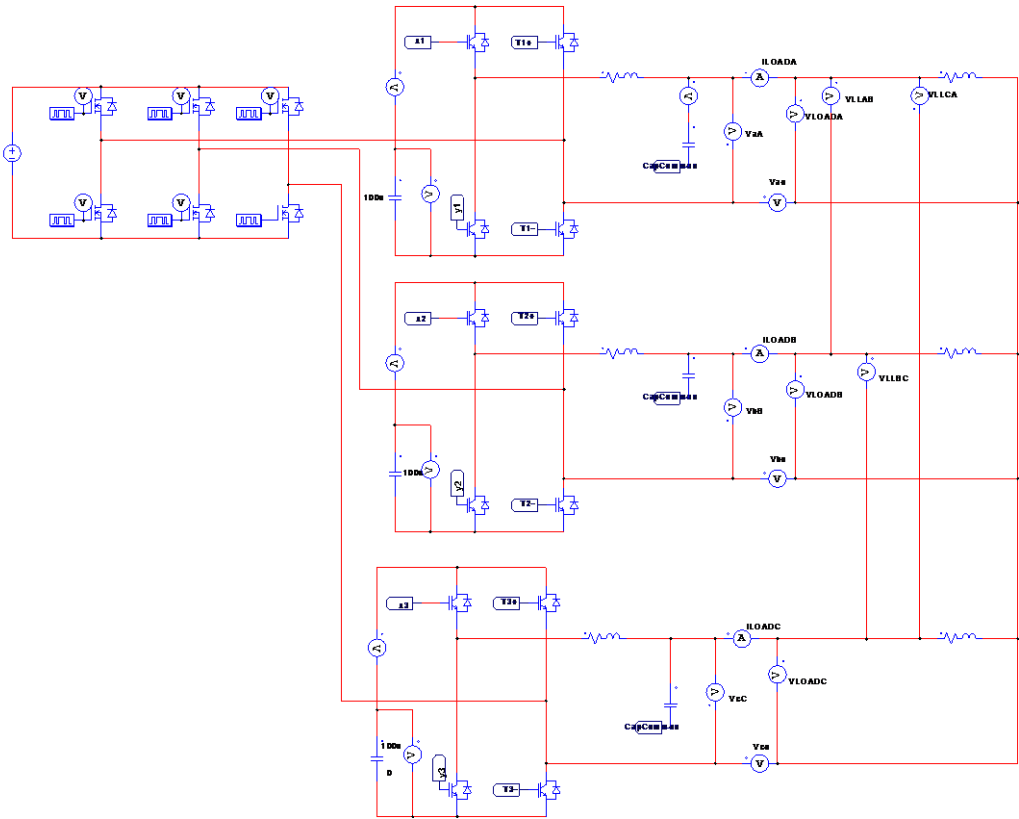


Figure 65 PSIM schematic for the proposed topology power circuit when the main inverter is controlled using programmed PWM

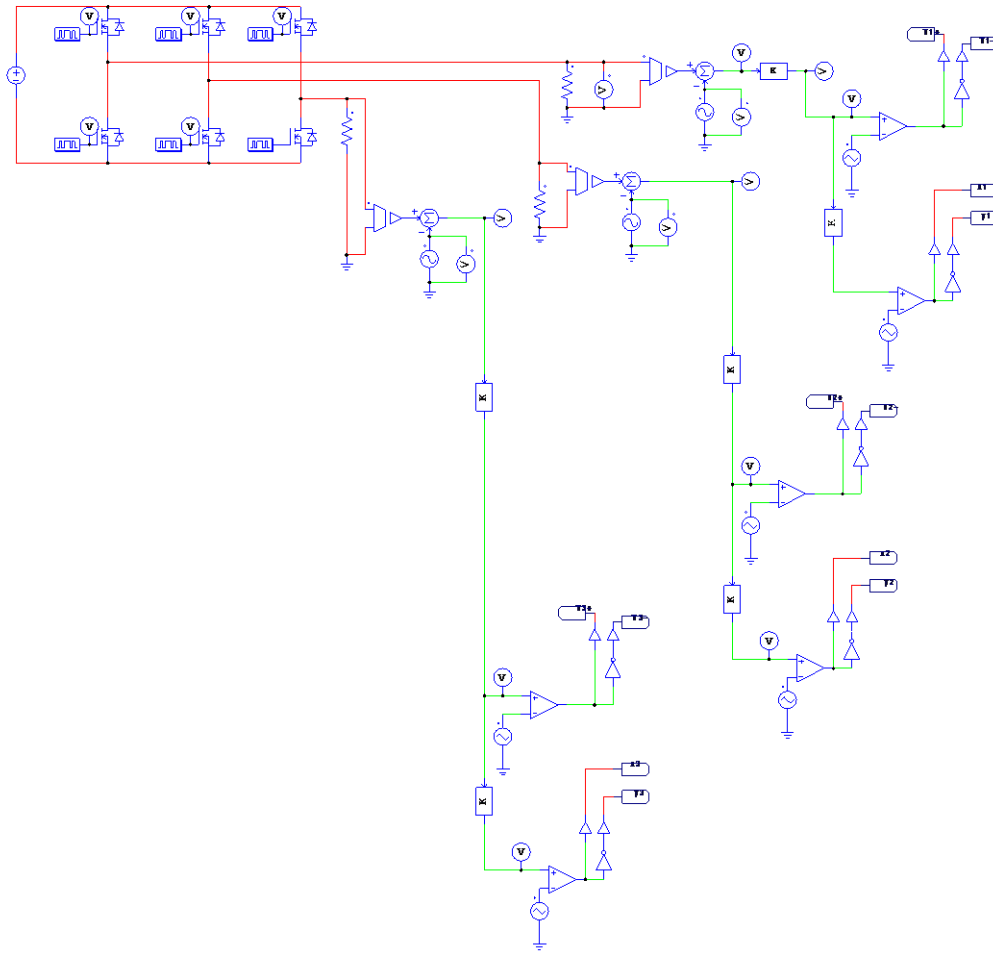


Figure 66 PSIM schematic for the proposed topology control circuit when the main inverter is controlled using programmed PWM

The simulation has been demonstrated Figure 67 hence that the output line to line voltage is successfully regulated according to m_a value:

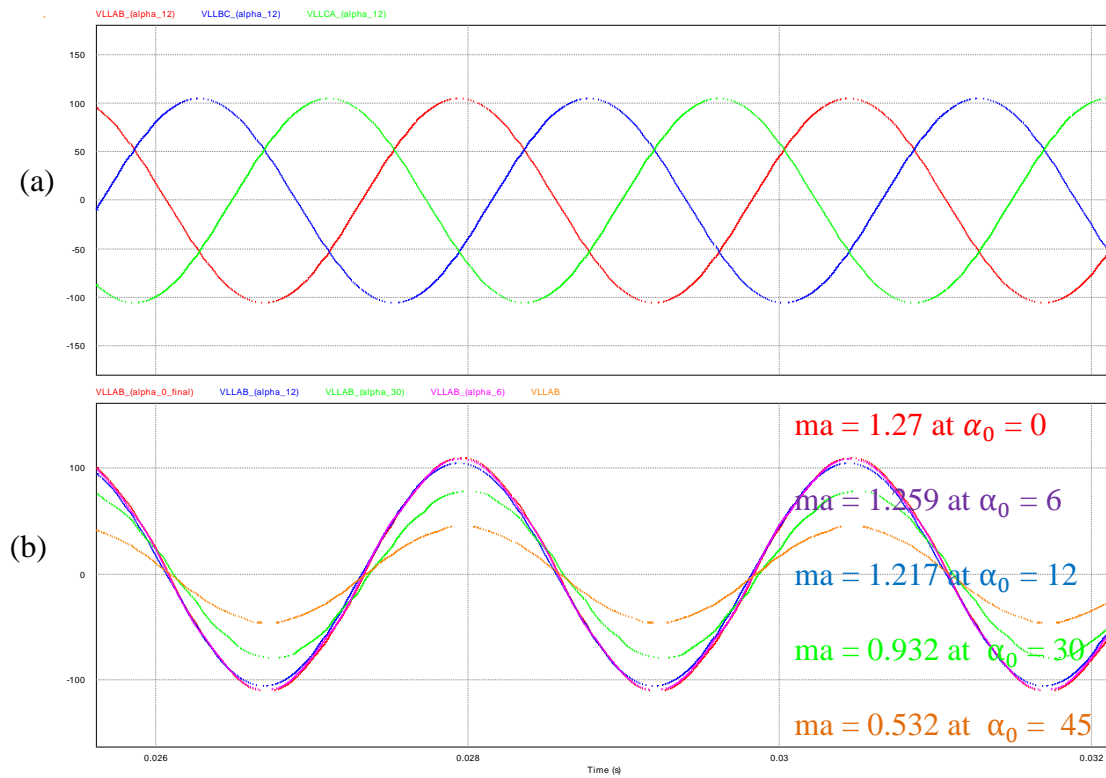


Figure 67 Voltage control method using Programmed PWM showing: (a) line to line voltages for $m_a=1.217$. (b) line to line output voltages for several m_a 's.

The voltage injection stage waveform will be changed depending on the m_a as shown in Figure 68 hence that when $\alpha_0=0$ the modulating signal will be equivalent to the proposed topology from Chapter 3.

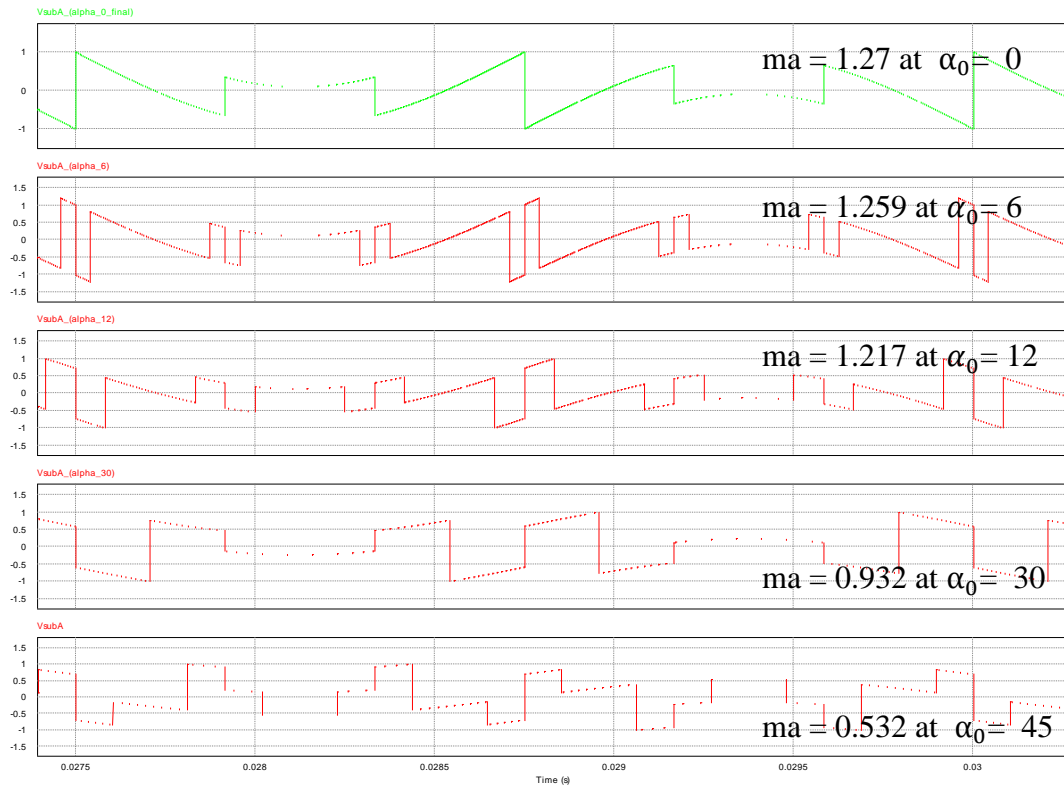


Figure 68 Modulating signal waveform for angles 0, 6, 12, 30 and 45

Consequently, the AOF DC link waveform will be varied with respect to m_a variation as illustrated in Figure 69.

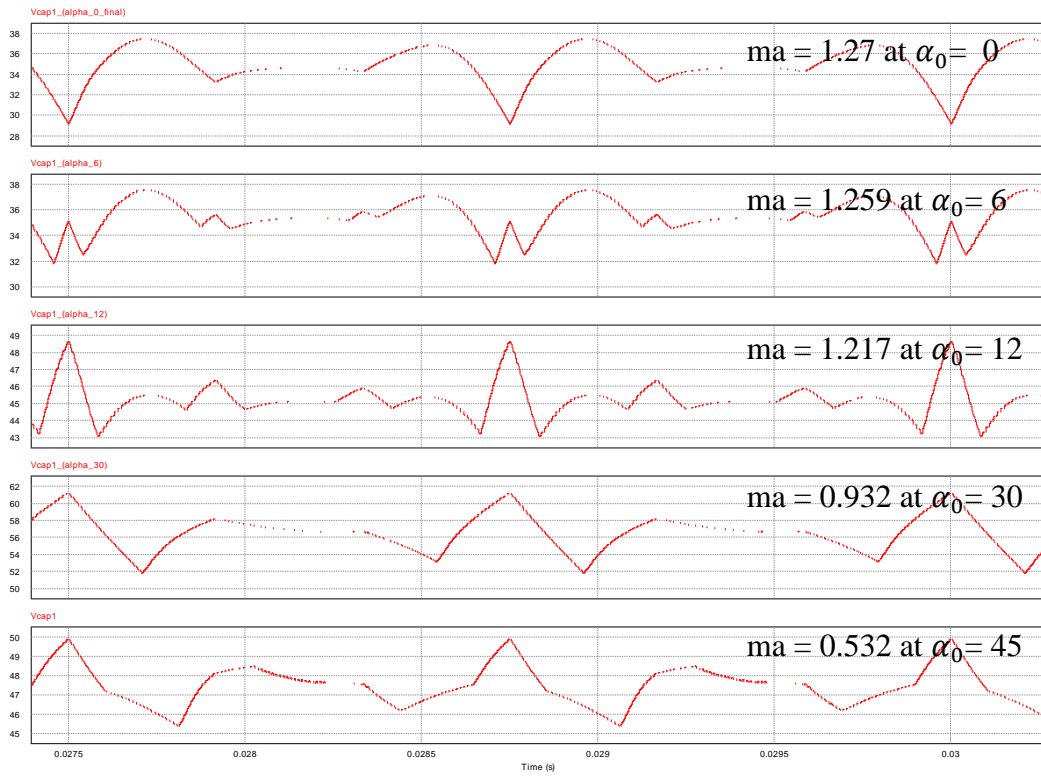


Figure 69 AOF dc-link waveform under different ma values

Moreover, at $ma = 1.217$ at $\alpha_0 = 12$ the magnitude of fifth harmonic is equal to 0 as shown in Figure 70 as a result, the harmonic of the AOF DC Link will start at 7th and that can be utilized in reducing the DC Link size.

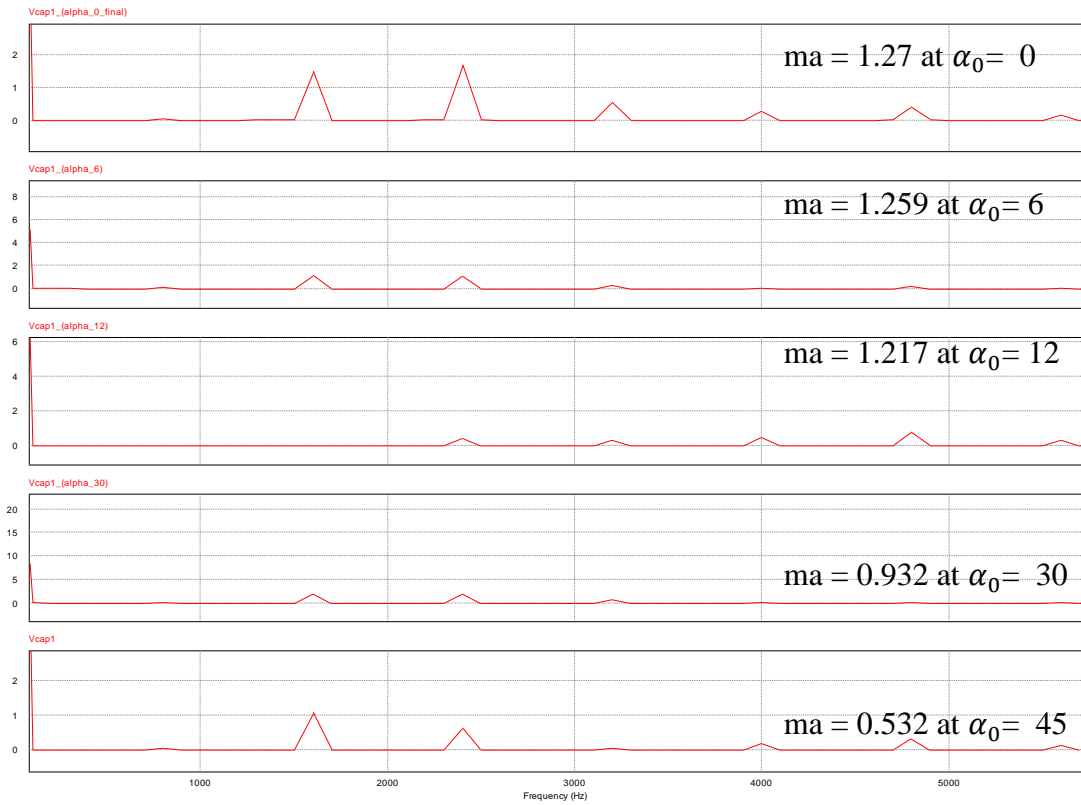


Figure 70 Harmonics distribution for AOF dc-Link voltage for different ma values

6.2 Low switching frequency of the main inverter using SVPWM

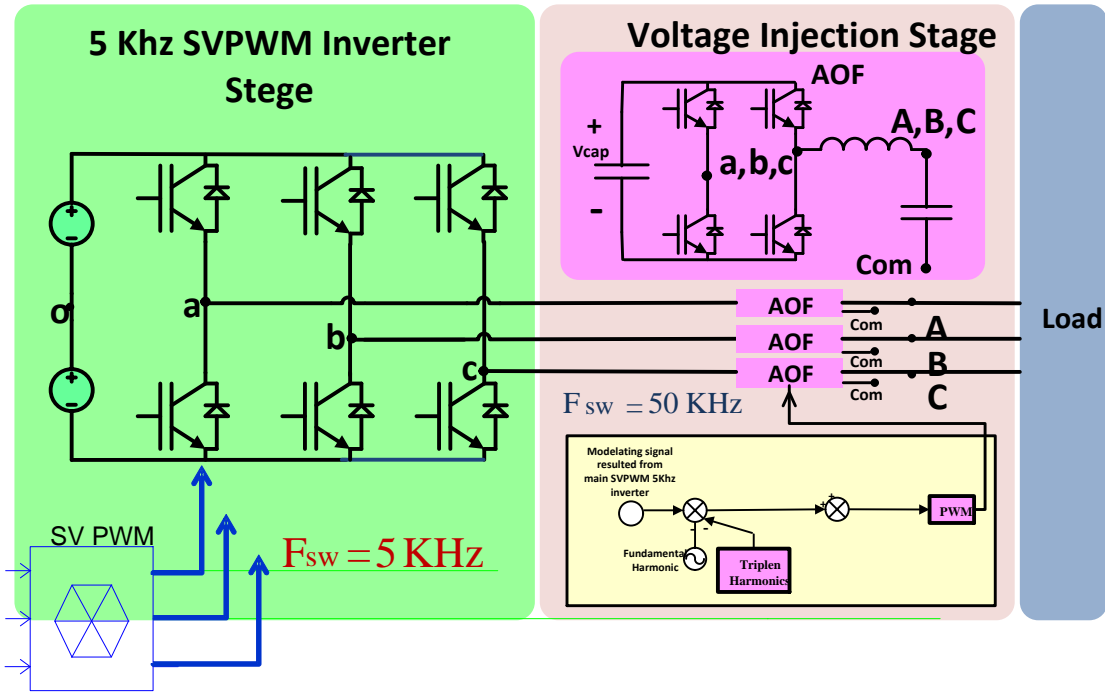


Figure 71 Proposed topology with SVWPWM main inverter voltage control

There are several ways to drive the Space Vector Pulse Width Modulation (SVPWM) technique for the proposed AOF topology shown in Figure 71. And the most simplified one is Carrier Based PWM CBPWM. The analysis can be started by first obtaining the zero sequence voltage $V_{Nn}(t)$ (shown in Figure 72 (b)) using the following equation [32-34]:

$$V_{Nn}(t) = \frac{1}{2} [\max(V_a(t), V_b(t), V_c(t)) + \min(V_a(t), V_b(t), V_c(t))] \quad (102)$$

Since that $V_a(t)$, $V_b(t)$ and $V_c(t)$ Are sinusoidal voltages with unity magnitude, thus, when subtracting $V_{Nn}(t)$ from $V_a(t)$, $V_b(t)$ and $V_c(t)$ as shown in Figure 72 it will cause the modulating signal expressed in Figure 73 (a). This wave from is under modulated with a maximum amplitude of ± 0.866 and to make this waveform fully modulated at ± 1 value $V_{svpwm*}(t)$ have to be multiplied with a 1.154 factor to results the final 3 phases modulating signal illustrated in Figure 73(c). Moreover, 1.154 gain factor is equal to the maximum modulation index hence that the major SVPWM advantage is it's over modulation capability up to $ma = 1.154$. Unlike SPWM, SVPWM involve lower order harmonics but very small in magnitude.

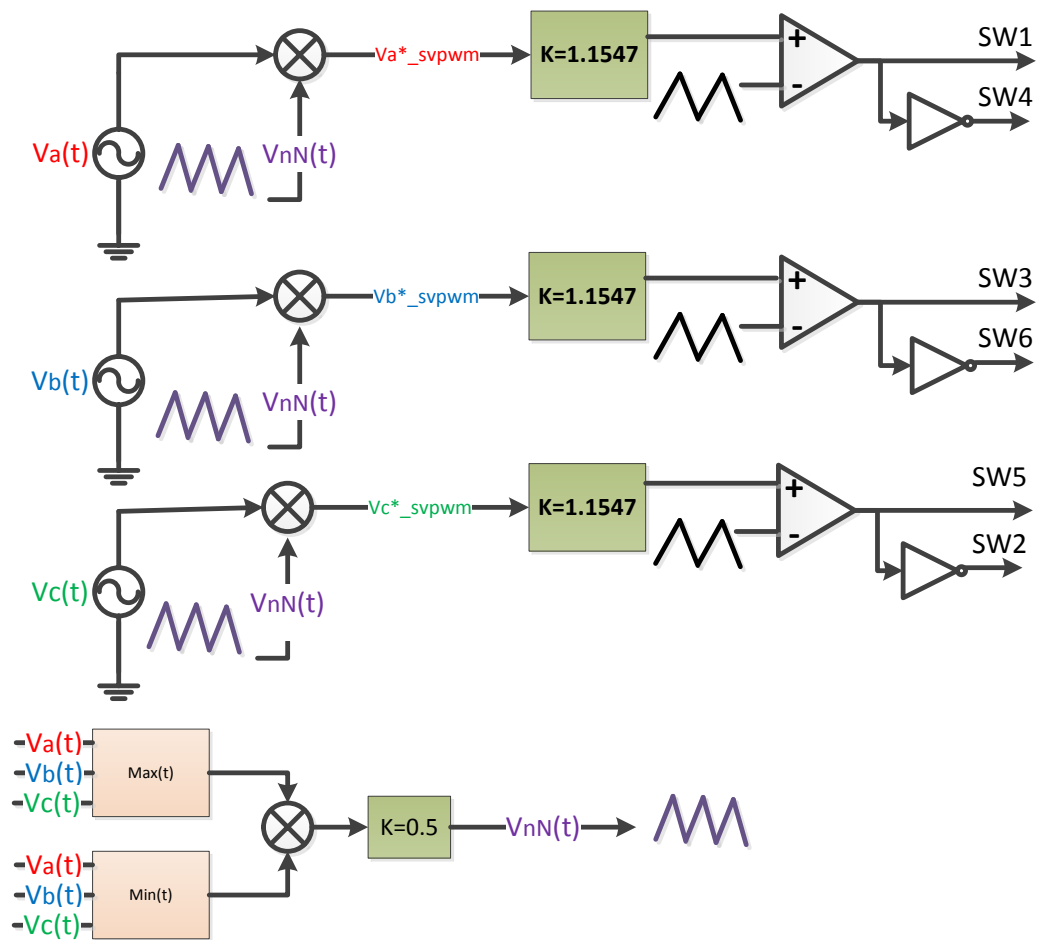


Figure 72 SVPWM generation

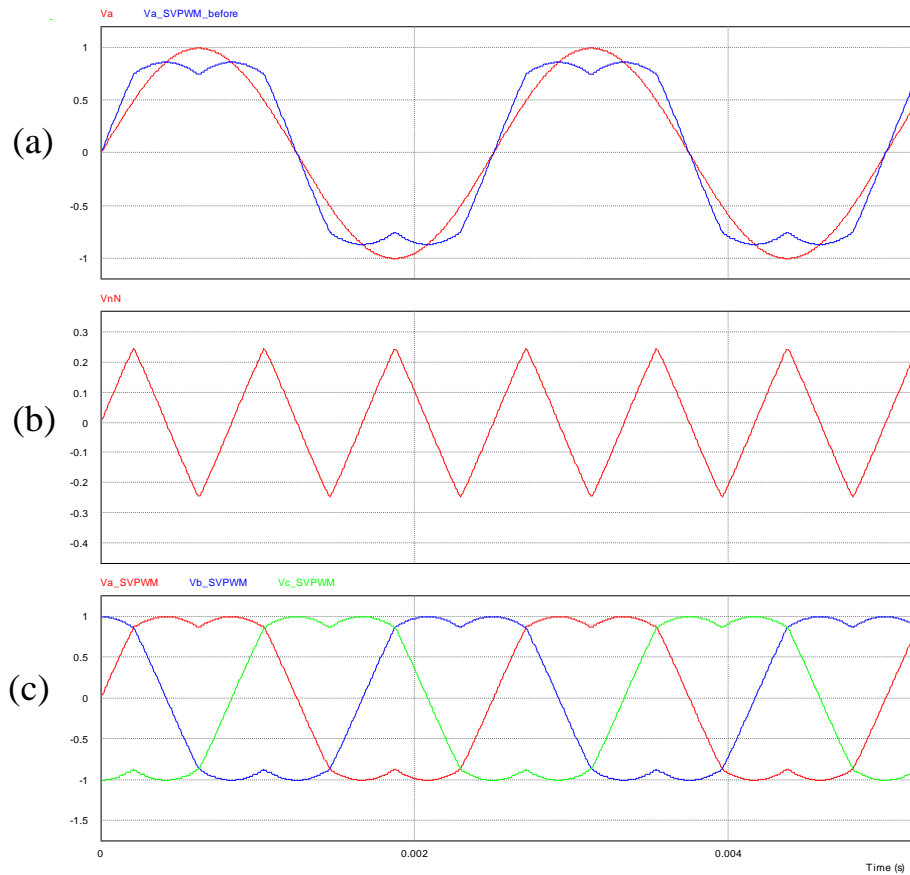


Figure 73 This figure shows the control voltage waveforms driven from the previous Figure 72

Similar to SHPWM, SVPWM have been employed in the main inverter to regulate the output voltage depending on the modulation index when using design specification obtained from Table 18.

Table 18: Proposed topology designed parameters for SVPWM technique

Main Inv.	AOF	Input DC	AOF DC	AOF Filter	L-L RMS	AC
f_{sw}	f_{sw}	to AOF	Link		Voltage	load
5KHz	50KHz/effective 100KHz	100v	100 μ F	15 μ H, 50 μ F	100v	16.67 W

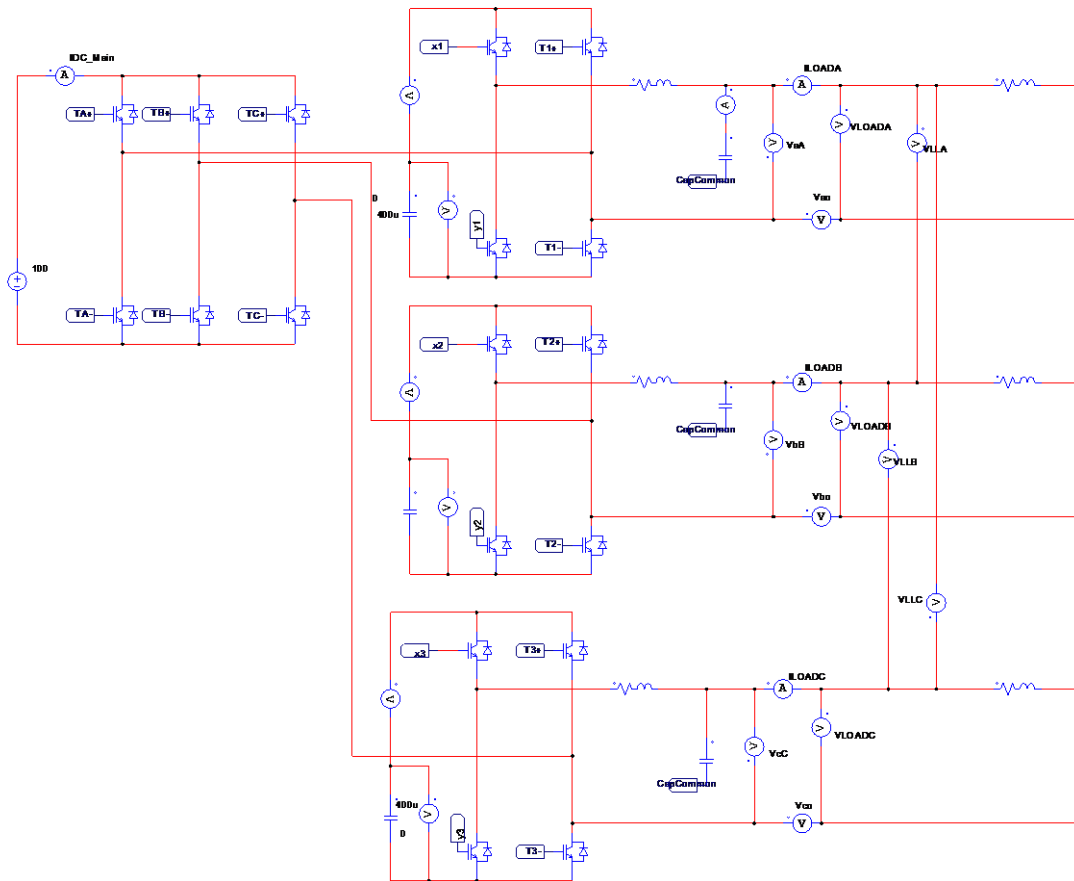


Figure 74 PSIM schematic for the proposed topology power circuit when the main inverter is controlled using SVPWM

When using PSIM, the SVPWM block diagram illustrated in Figure 72 is integrated in one block (Figure 75) in which it directly generates the full modulated signal that in turns compared to saw tooth carrier signal to drive the switches in AOF blocks as expressed in Figure 76.

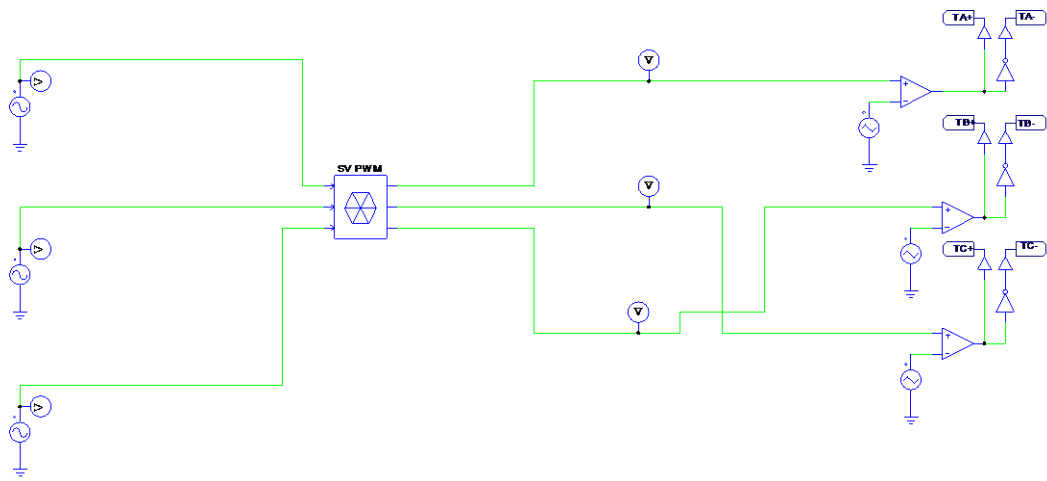


Figure 75 SVPWM implementation in PSIM to control the main 3 phase inverter as low switching frequency

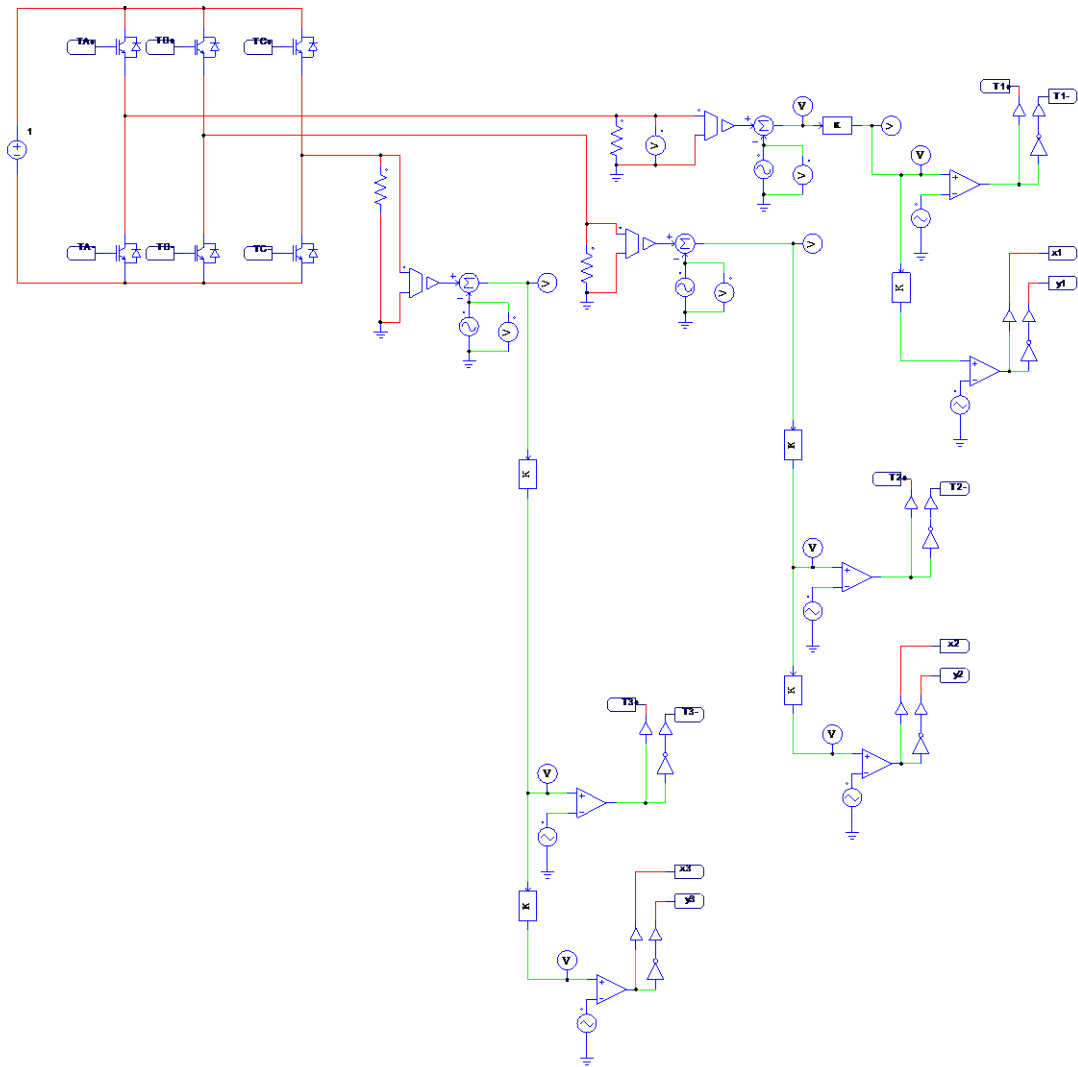


Figure 76 PSIM schematic for the proposed topology control circuit when the main inverter is controlled using SVPWM

The results have been demonstrated in below Figure 77 hence that the output line to line voltage is successfully regulated according to m_a value:

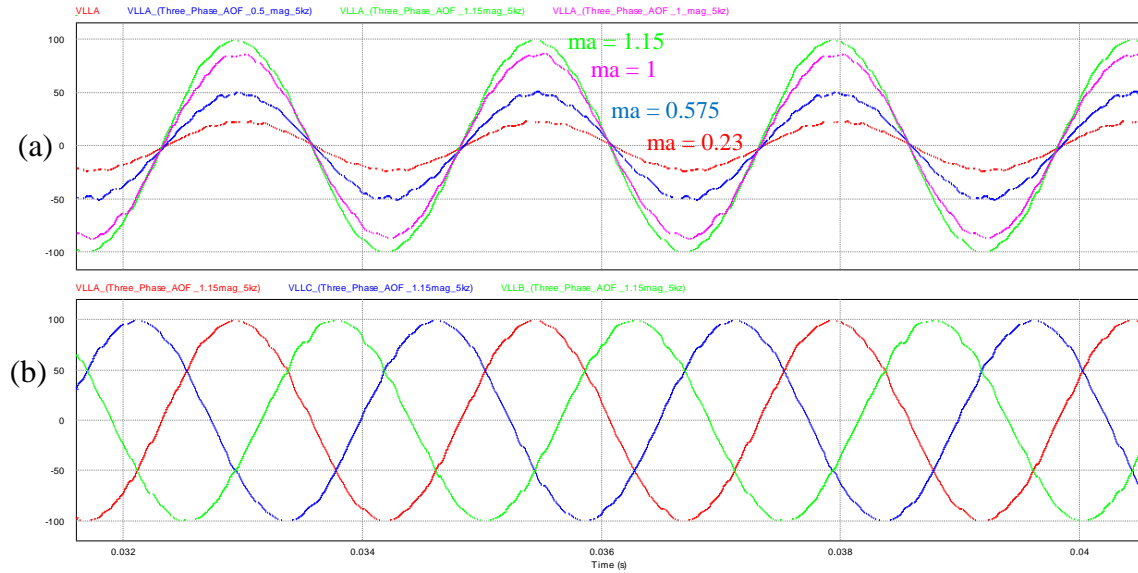


Figure 77 Voltage control method using SVPWM in the main inverter showing:
 (a) line to line output voltages for several m_a 's.(b) line to line voltages for $m_a=1.15$

The voltage injection stage waveform will be changed depending on the m_a as expressed in the following Figure 78. Consequently, AOF DC Link will involve ripples with different harmonic distribution as expressed in Figures 79 & 80.

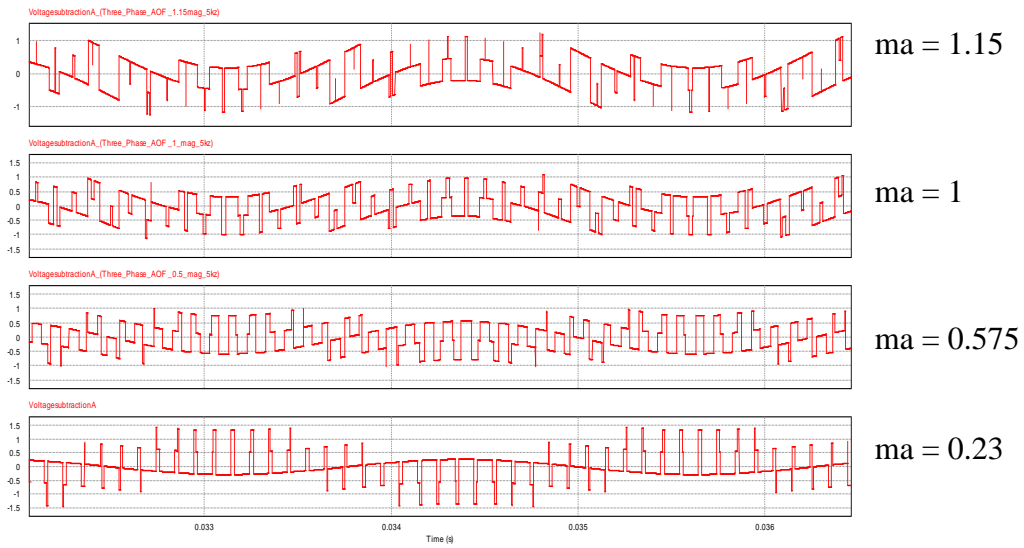


Figure 78 Modulating signal waveform for $ma=1.15, 1, 0.575$ and 0.23

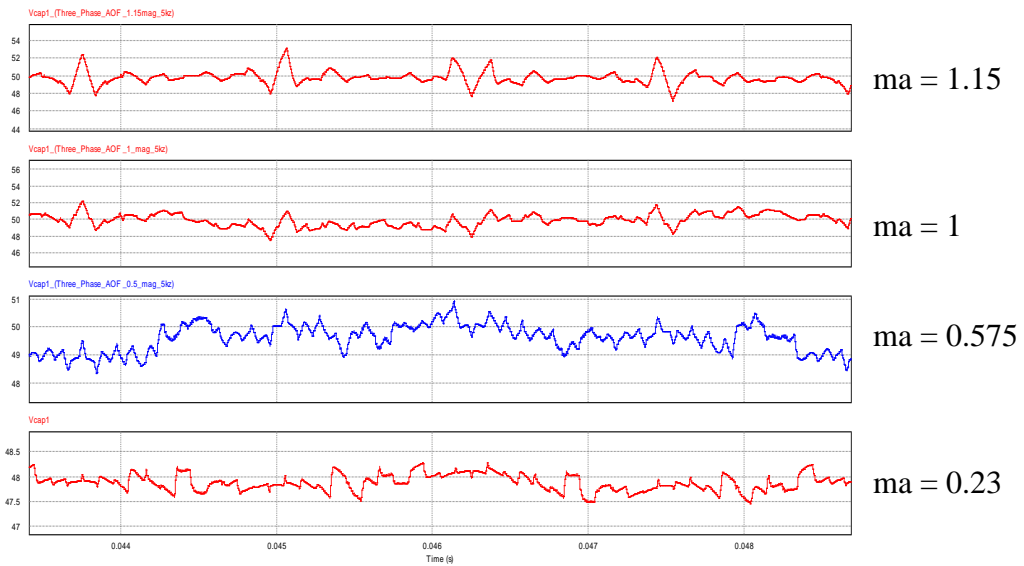


Figure 79 AOF dc-link waveform for different ma values

Therefore when FFT has been implemented for the waveform given in Figure 79, it can be observed that the harmonics in DC link start to occur close to the main inverter switching frequency which is in this case $5\text{kHz} \pm 800\text{Hz}$ according to the 3 phase SVPWM $m_f \pm 2$. However, when varying the modulation the harmonics distribution varies accordingly.

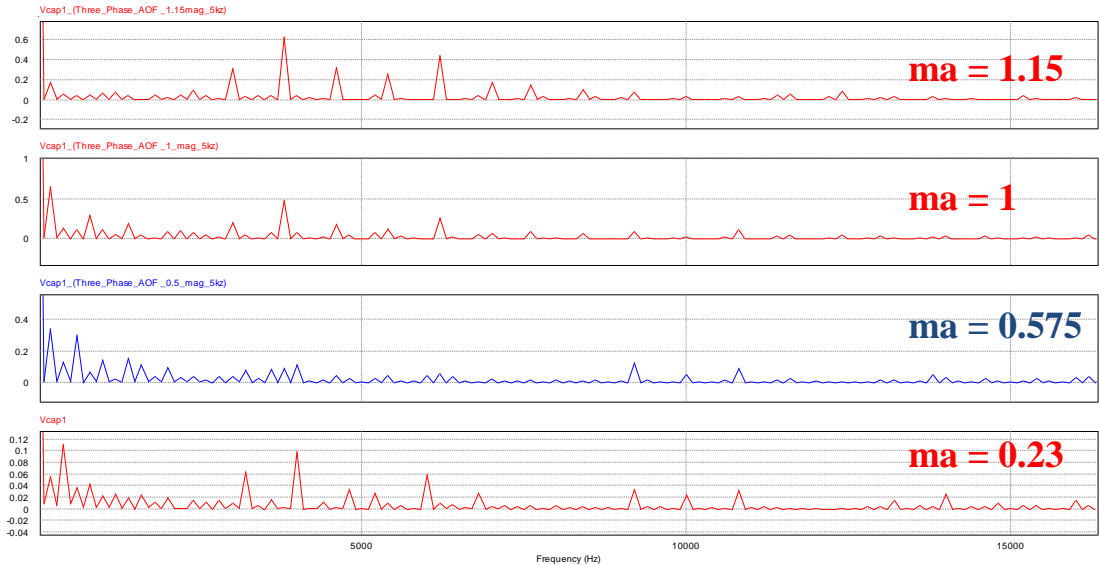


Figure 80 Harmonic distribution for AOF dc-link voltage for different ma values

7. HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

7.1 Digital signal processor (DSP) implementation

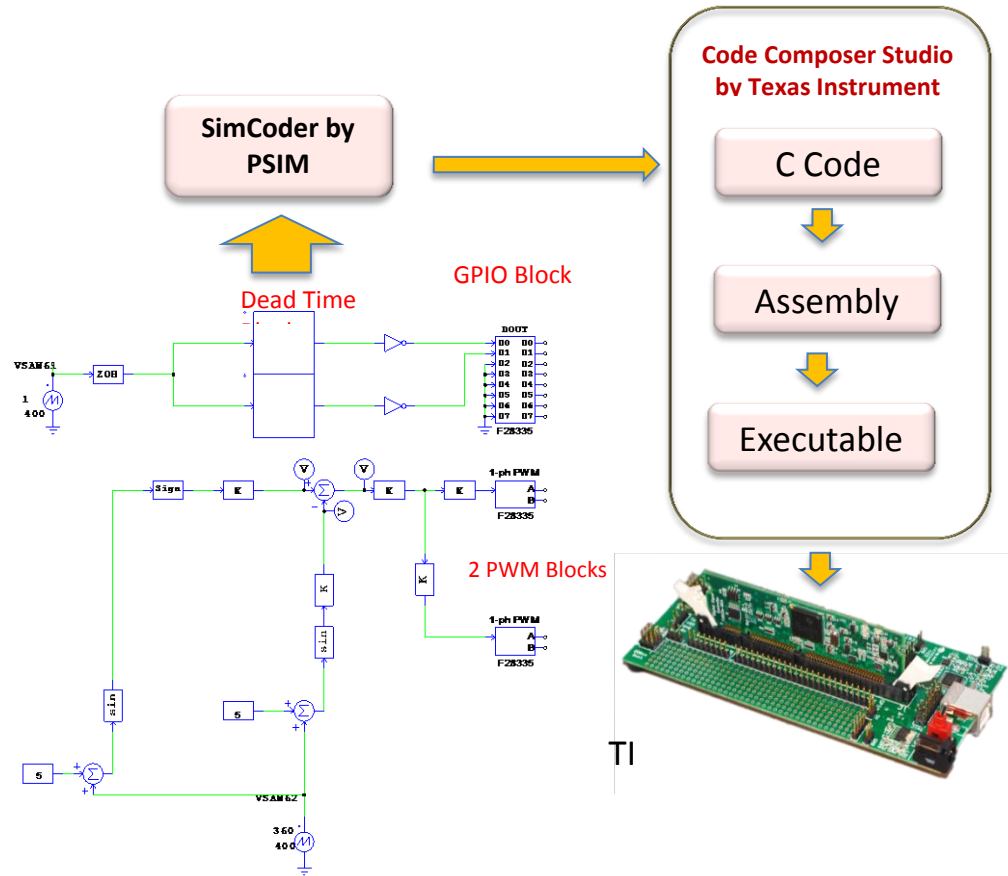


Figure 81 DSP implementation for single phase AOF

The Digital Signal Processor (DSP) implementation have accomplished by utilizing SIMCPDER graphical feature in PSIM shown in Figure 81. Thus, 2 GPIO registers has been used to drive the 4 switches on the main 400Hz square wave inverter. On the other hand, two PWM signals have been used to drive the 4 AOF switches in a

unipolar scheme. After drawing the Schematic in PSIM SIMODER convert the PSIM graphical interface into C code. Then by compiling the generated code in Code Composer Studio (CCS) the code will be converted eventually to executable file to be uploaded in the TIF28335 DSP which designed by Texas Instrument.

7.2 Hardware implementation

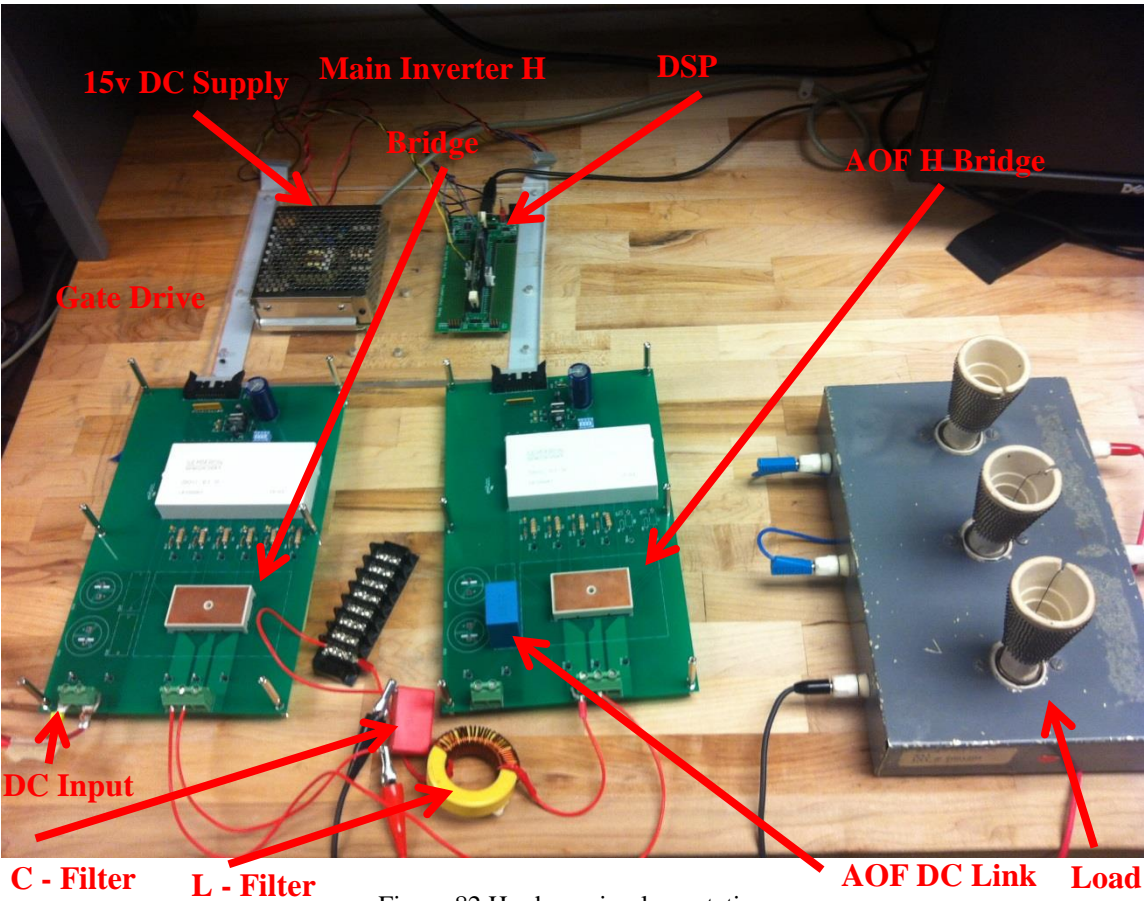


Figure 82 Hardware implementation

The main inverter and AOF inverter have been implemented using two SEMEKRON GATE Drives “**SKHI- 61R**” in which they were powered by the 15v DC supply as presented in Figure 82. While two “**SKHI- 61R SEMEKRON 10KW**” inverter module have been selected to drive 400HZ Square wave Inverter and AOF Inverter. Hence that over all VA rating of the PCB board in 1.2KVA. The main DC Power supply for the power circuit is “**B&K Precision XLN10014**” which capable to supply 100Vdc-14A Load as displayed in Figure 83.



Figure 83 DC supply to the power circuit

Moreover, L-C and DC Link Values have been designed according to Chapter 2 equations and tabulated in Table 19 and the results are demonstrated in the following figures taken from oscilloscope (oscilloscope is manufactured by **Tektronix** with Model TDS3034C). Using a bipolar switching scheme illustrated in Figures 84 & 85 verified the Chapter 2 waveforms shape and THD less compliance than 5%.

Table 19: Design parameters for hardware implementation in case of resistive load (AOF switching at bipolar scheme)

AOF f_{sw}	Input DC to AOF	AOF DC Link	AOF Filter	RMS Voltage	AC load
24KHz	100v	1.1mF	10 μ H, 130 μ F	90v	100W

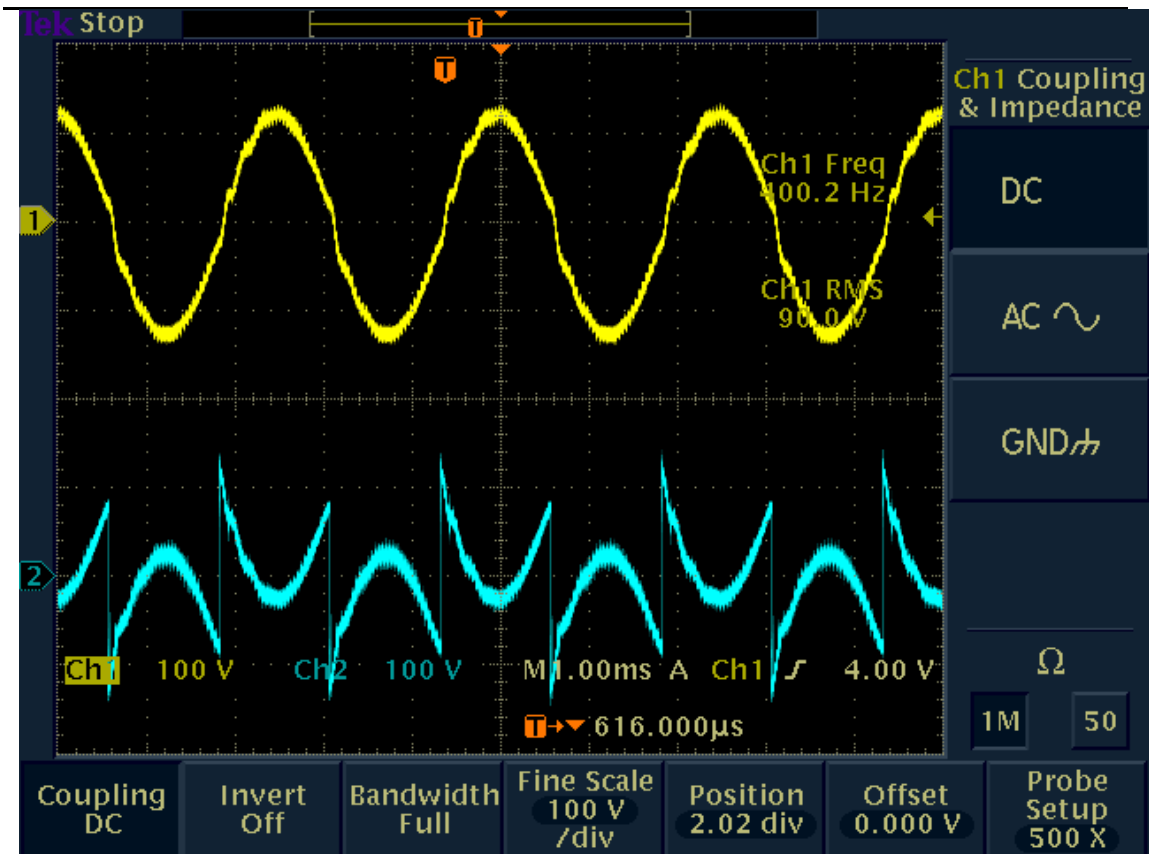


Figure 84 The upper waveform represents the load voltage while the lower waveform represents the voltage injection stage

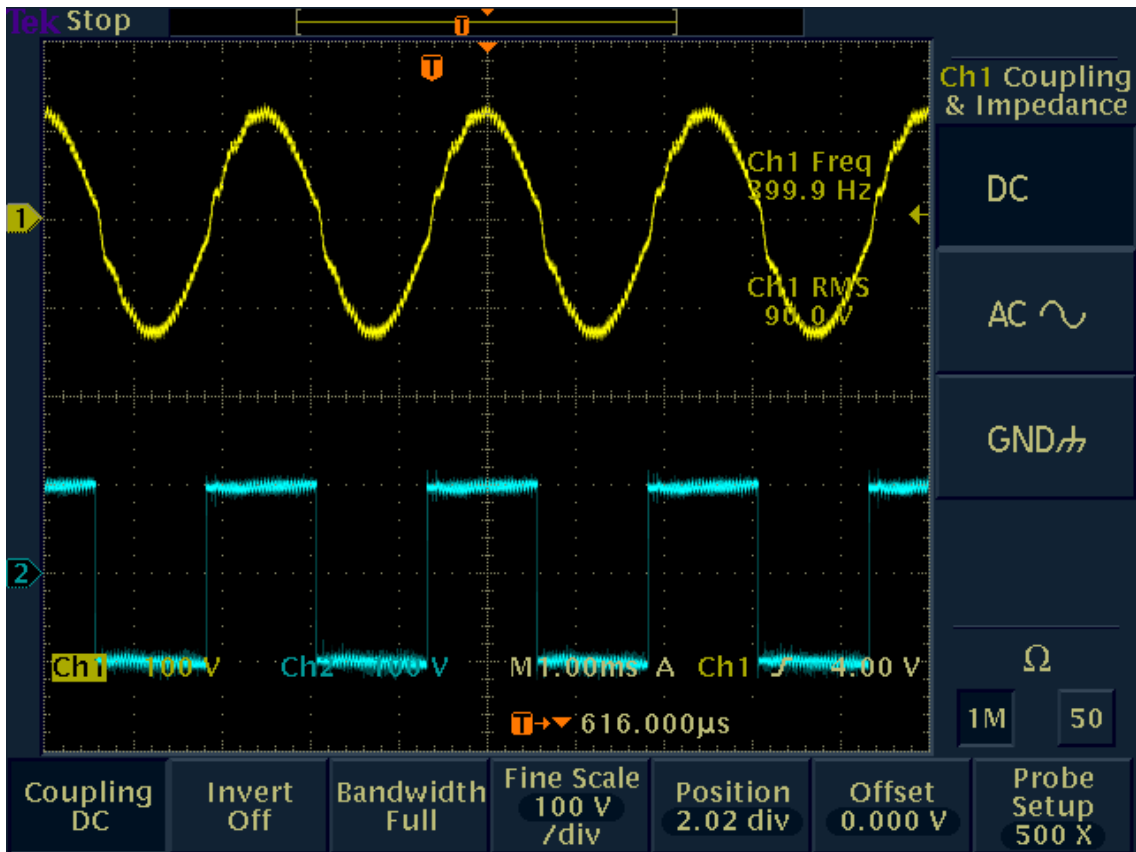


Figure 85 The upper waveform represents the load voltage while the lower waveform represents the main inverter square wave voltage stage

Hence a unipolar Switching scheme cause a better quality output due to the unwanted harmonics start to appear at twice the switching frequency [26]. Thus, Unipolar Switching Scheme has been also considered in thus experimental results. Table 20 express reduced power design example and the obtained voltages waveforms are Figures 86 & 87. As expected, load voltage THD is improved compared to bipolar case.

Table 20: Design parameters for hardware implementation in case of resistive load (AOF switching at unipolar scheme)

AOF Fsw	Input DC to AOF	AOF DC Link	AOF Filter	RMS Voltage	AC load
24Khz /Unipolar	100v	50 μ F	1.1mH, 0.22uF	81.6v	51.6W

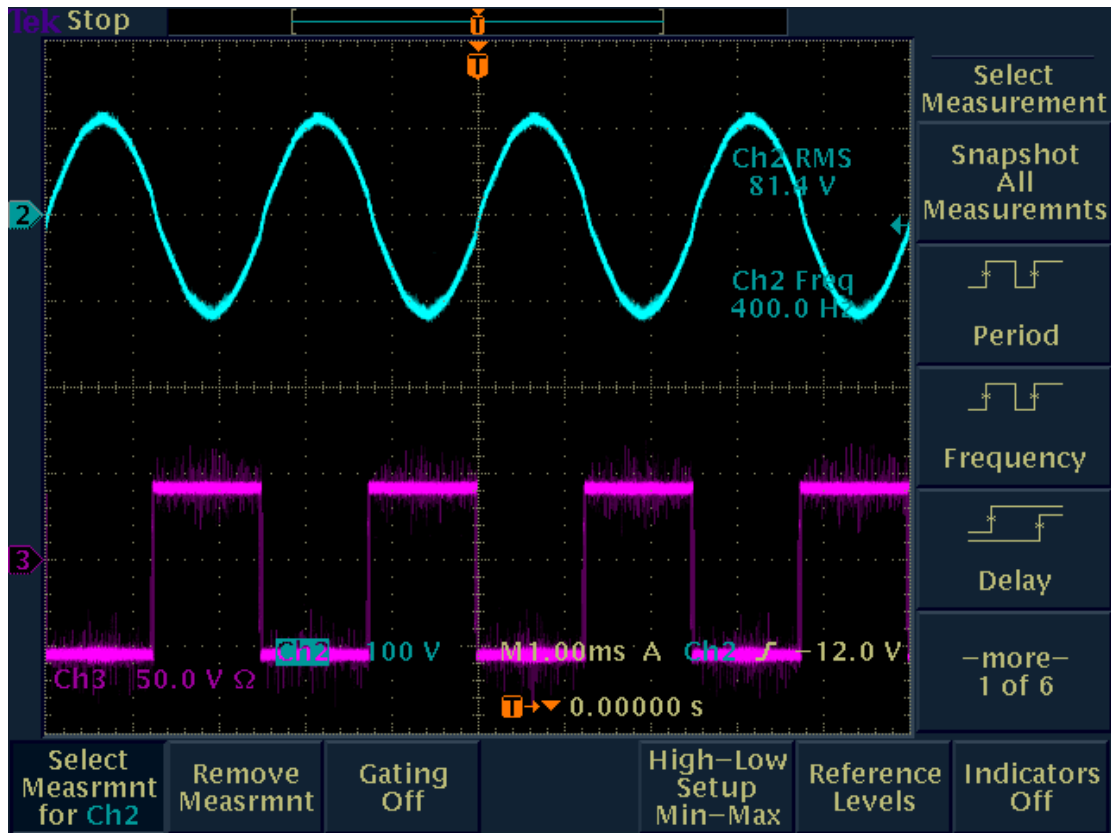


Figure 86 The upper waveform represents the load voltage while the lower waveform represents the main inverter voltage Vab

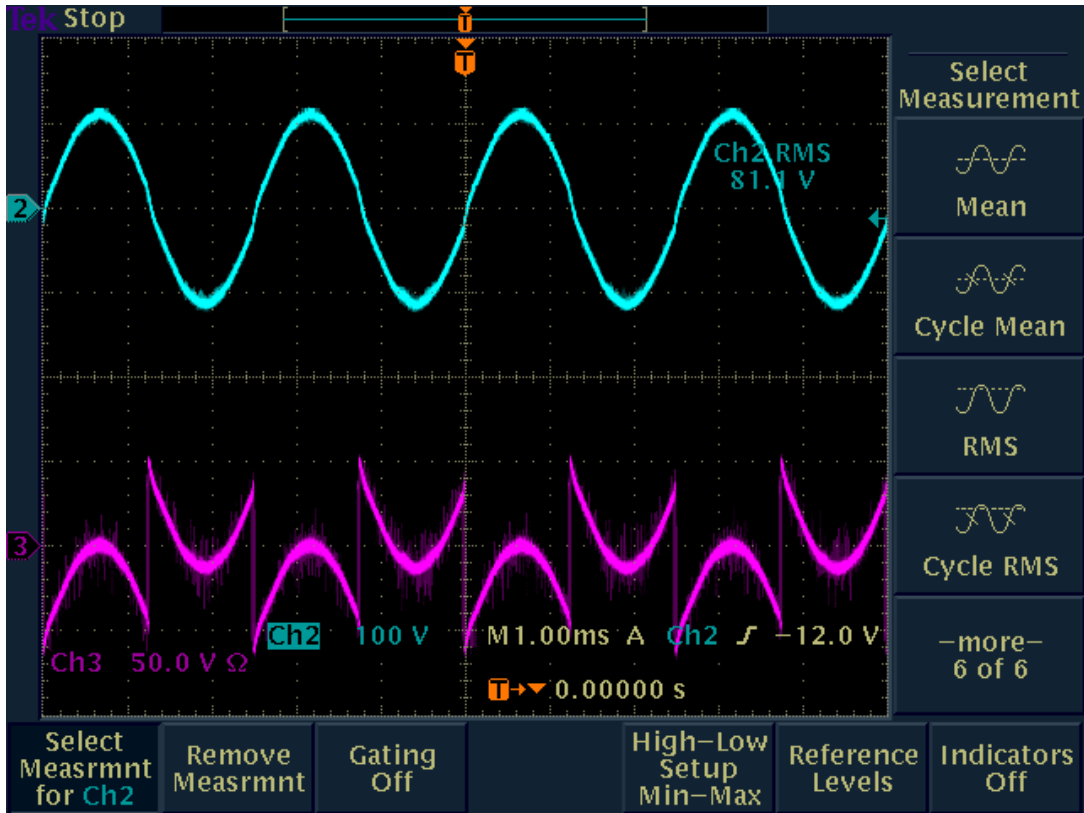


Figure 87 Sinusoidal output waveform (on top) with respect to AOF voltage waveform (on bottom)

Finally, the proposed Single phase AOF topology has been tested under a non-linear load diode rectifier having the specifications expressed in Table 21. AOF voltage output maintain a good quality voltage waveform hence that it is slightly degraded due to low order harmonics generated by the diode rectifier load as verified in Figure 88.

Table 21: Design parameters for hardware implementation in case of a diode rectifier load

AOF Fsw	Input VDC to AOF	AOF DC Link	AOF Filter	RMS Voltage to the rectifier	AC load	Ld, Cd for rectifier
24KHz /Unipolar	65v	20 μ F	110 μ H, 5 μ F	58.5	32.75W	6.6mH, 1.1mF

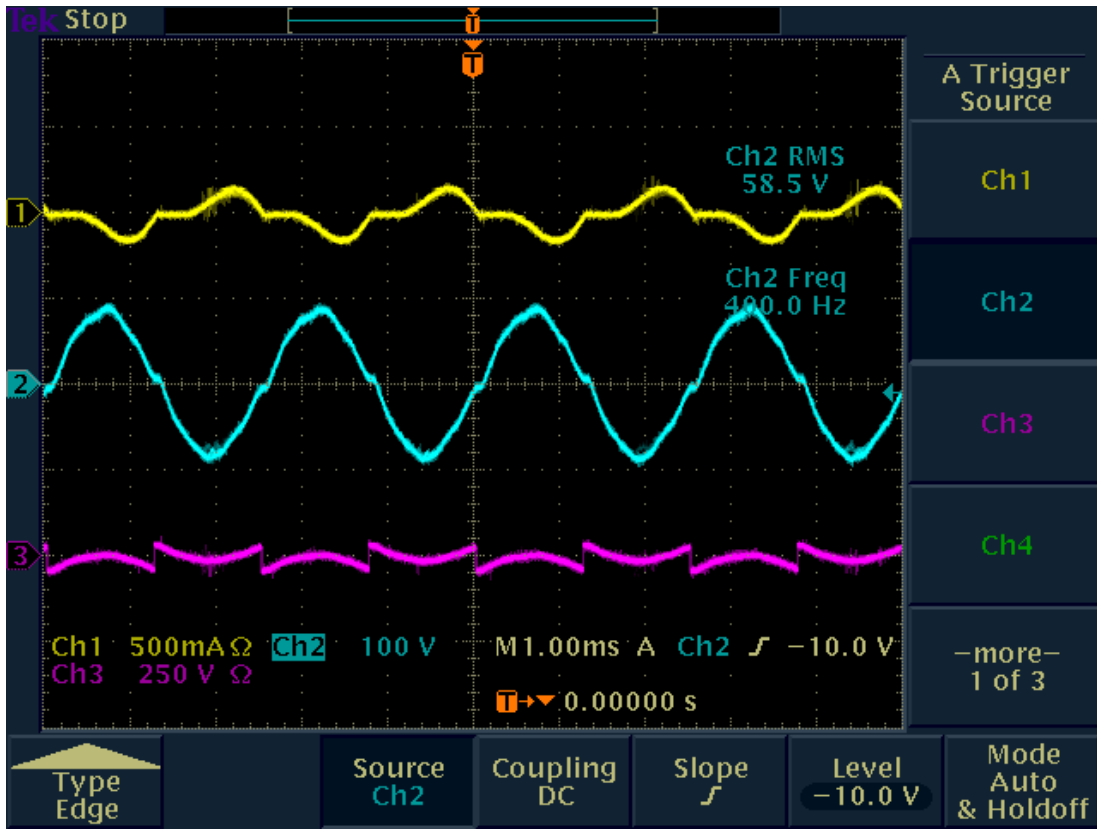


Figure 88 The results with nonlinear diode rectifier load showing: Ch1 as output current from AOF into diode rectifier and Ch2 as output voltage from AOF into diode rectifier and Ch3 as voltage injected waveform across AOF

8. CONCLUSION AND FUTURE WORK

8.1 Conclusion

A concept called “Active Output Filter” (AOF) has been proposed. It aims to enable the replacement of bulky passive output filter with semiconductor-based devices in series with a minimized LC that perform two cases of voltage harmonic injection with an advantage of 1.27 modulation index. The first case in which the triplen harmonic is presented have reduced the size of the LC filter by 7% while the second case in which the triplen harmonic is canceled in the injected voltage have reduced the size of the LC filter by more than 60%. Moreover, 2nd harmonic is existed in AOF dC-link in the first case while the second case has even harmonics starting from the 4th. Thereby the second case is preferable and selected for software and experimental implementations. Moreover, the size of the LC filter is switching frequency dependent in which it can be further reduced up to 71% times when the f_{sw} is 400Khz. Finally, SHEPWM and SVPWM have been implemented for the main inverter to offer an output voltage control feature.

8.2 Future work

Future work would be done to explore the following:

- Perform a detailed inductor sizing and performance utilizing MAXWELL Program
- Exploring Efficiency analysis utilizing efficient switches i.e. GaN, SiC
- Utilize AOF for 60 Hz Adjustable Speed Drive Application
- Exploring Heat Sink Design and optimization
- Investigating LCL filter configuration effect

REFERENCES

- [1] Eid, A.; El-Kishky, H.; Abdel-Salam, M.; El-Mohandes, T., "Constant frequency aircraft electric power systems with harmonic reduction," *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE* , vol., no., pp.623,628, 10-13 Nov. 2008.

- [2] Aero Maintenance Group, "IDG," 2015 Available:
<http://www.aeromaintenancegroup.com/en/products/products\>.

- [3] De, D.; Ramanarayanan, V., "Decentralized parallel operation of inverters sharing unbalanced and nonlinear loads," *Power Electronics, IEEE Transactions on* , vol.25, no.12, pp.3015,3025, Dec. 2010.

- [4] Srimoolanathan, Balaji "Aircraft electrical power systems – charged with opportunities" *Frost & Sullivan Market Insight* , Date Published: 24 Nov 2008.

- [5] Abdel-Fadil, Reyad, Ahmad Eid, and Mazen Abdel-Salam. "Electrical Distribution Power Systems of Modern Civil Aircrafts." *International Conference on Energy Systems and Technologies*, 2nd (ICEST'13), Cairo, Egypt. 2013.

- [6] Xia, Xiuxian(2011). Dynamic power distribution management for all electric aircraft. Master's thesis, Cranfield University. Available:
<http://core.ac.uk/download/pdf/140642.pdf>

- [7] M. Salama, "Lightweight materials for deepwater offshore structures," *Offshore Technology Conference*, 1986.

- [8] Rana, Dibyendu (2014). Analysis & Design of Active Inductor. Master's thesis, Texas A & M University. Available:
<http://hdl.handle.net/1969.1/152536>.

- [9] ABB Ltd., "Special Report – Motors & Drives," 2004. Available: [http://www05.abb.com/global/scot/scot271.nsf/veritydisplay/97051077deb4950fc1256ea6004ffac5/\\$file/motors%20and%20drives.pdf](http://www05.abb.com/global/scot/scot271.nsf/veritydisplay/97051077deb4950fc1256ea6004ffac5/$file/motors%20and%20drives.pdf).
- [10] GaN Systems Inc., "Little Box Challenge," 2015 Available: http://www.gansystems.com/little_box_challenge.php.
- [11] Moir, Ian, and Allan Seabridge. *Aircraft systems: mechanical, electrical and avionics subsystems integration*. vol. 52. John Wiley & Sons, Virginia, 2011.
- [12] Maldonado, M.A.; Shah, N.M.; Cleek, K.J.; Walia, P.S.; Korba, G., "Power management and distribution system for a more-electric aircraft (MADMEL)-program status," *Energy Conversion Engineering Conference, 1996. IECEC 96., Proceedings of the 31st Intersociety*, vol.1, no., pp.148,153 vol.1, 11-16 Aug 1996.
- [13] J. I. Corcau and L. Dinca, " Generation on more electric aircraft on using PEMFC for electrical power " ,*International Journal of Electronics and Electrical Engineering*, no.62, pp. 246-249, Feb. 2012.
- [14] Pallett, Edwin Henry John. *Aircraft electrical systems*. Halsted Press, 1987.
- [15] Wikipedia, "Constant Speed Drive," Nov, 2014. Available: http://en.wikipedia.org/wiki/Constant_speed_drive.
- [16] Ying Shing Shiao; Lin, C.E., "A prototype induction generator VSCF system for aircraft," *Industrial Automation and Control: Emerging Technologies, 1995., International IEEE/IAS Conference on*, vol., no., pp.148,155, 22-27 May 1995.
- [17] Langton, Roy, et al. *Aircraft fuel systems*. John Wiley & Sons, Ltd, 2009.
- [18] A. Eid, M. Abdel-Salam, H. El-Kishky and T. El-Mohandes, " Active power filters for harmonics cancellation in conventional and advanced aircraft electric power systems", *Electric Power Systems Research*, vol. 79, Issue 1, pp. 80-88, January 2009.

- [19] A. Eid, H. El-Kishky, M. Abdel-Salam, and T. El-Mohandes "On power quality of variable speed constant frequency aircraft electric power systems", *IEEE Trans. Power Delivery*, vol. 1, No. 25, pp. 55-65, January 2010.
- [20] Byung-Moon Han; Byong-Yeul Bae; Ovaska, S.J., "Reference signal generator for active power filters using improved adaptive predictive filter," *Industrial Electronics, IEEE Transactions on* , vol.52, no.2, pp.576,584, April 2005.
- [21] Campos, A.; Joos, G.; Ziogas, P.D.; Lindsay, J.F., "Analysis and design of a series voltage unbalance compensator based on a three-phase VSI operating with unbalanced switching functions," *Power Electronics, IEEE Transactions on* , vol.9, no.3, pp.269,274, May 1994.
- [22] Nastran, J.; Cajhen, R.; Seliger, M.; Jereb, P., "Active power filter for nonlinear AC loads," *Power Electronics, IEEE Transactions on* , vol.9, no.1, pp.92,96, Jan 1994.
- [23] Peng, F.Z., "Harmonic sources and filtering approaches," *Industry Applications Magazine, IEEE* , vol.7, no.4, pp.18,25, Jul/Aug 2001.
- [24] Koczara, W.; Dakyo, B., "AC voltage hybrid filter," *Telecommunication Energy Conference, 1999. INTELEC '99. The 21st International* , vol., no., pp.8 pp., Jun 1999.
- [25] Ribeiro, E.R.; Barbi, I., "Harmonic voltage reduction using a series active filter under different load conditions," *Power Electronics, IEEE Transactions on* , vol.21, no.5, pp.1394,1402, Sept. 2006.
- [26] Hart, Daniel W. *Power electronics*. Tata McGraw-Hill Education, 2011.
- [27] Garcia, C.A.; Llorens, F.; Garcia, P.; Fernandez, L.M.; Jurado, F., "Voltage harmonic compensation control for a stand-alone single phase inverter-based fuel cell," *Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2012 International Symposium on* , vol., no., pp.379,383, 20-22 June 2012

- [28] Precision Incorporated, "Large inductors/reactors," 2015. Available: http://www.precision-inc.com/power-large-inductors-reactors-c-1_7_328-1-en.html.
- [29] Napoles, J.; Leon, J.I.; Portillo, R.; Franquelo, L.G.; Aguirre, M.A., "Selective harmonic mitigation technique for high-power converters," *Industrial Electronics, IEEE Transactions on* , vol.57, no.7, pp.2315,2323, July 2010.
- [30] Enjeti, P.; Lindsay, J.F., "Solving nonlinear equations of harmonic elimination PWM in power control," *Electronics Letters* , vol.23, no.12, pp.656,657, June 4 1987.
- [31] Enjeti, P.N.; Ziogas, P.D.; Lindsay, J.F., "Programmed PWM techniques to eliminate harmonics: a critical evaluation," *Industry Applications, IEEE Transactions on* , vol.26, no.2, pp.302,316, Mar/Apr 1990.
- [32] Iqbal, A.; Moinuddin, S., "Comprehensive relationship between carrier-based PWM and space vector PWM in a five-phase VSI," *Power Electronics, IEEE Transactions on* , vol.24, no.10, pp.2379,2390, Oct. 2009.
- [33] Hongyang Wu; Xiangning He, "Inherent correlation between multilevel carrier-based PWM and space vector PWM: principle and application," *Power Electronics and Drive Systems, 2001. Proceedings., 2001 4th IEEE International Conference on* , vol.1, no., pp.276,281 vol.1, 22-25 Oct. 2001.
- [34] Choudhury, A.; Pillay, P.; Williamson, S.S., "A performance comparison study of space-vector and carrier-based PWM techniques for a 3-level neutral point clamped (NPC) traction inverter drive," *Power Electronics, Drives and Energy Systems (PEDES), 2014 IEEE International Conference on* , vol., no., pp.1,6, 16-19 Dec. 2014.
- [35] Wing-to Fan; Kuen-faat Yuen; Chung, H.S.-H., "Power semiconductor filter: Use of series-pass device in switching converters for input filtering," *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE* , vol., no., pp.948,955, 14-18 Sept. 2014.

- [36] Rana, D.; Hafez, B.; Garg, P.; Essakiappan, S.; Enjeti, P., "Analysis and design of active inductor as DC-link reactor for lightweight adjustable speed drive systems," *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE* , vol., no., pp.3243,3250, 14-18 Sept. 2014.
- [37] Elbuluk, M.E.; Kankam, M.D., "Potential starter/generator technologies for future aerospace applications," *Aerospace and Electronic Systems Magazine, IEEE* , vol.12, no.5, pp.24,31, May 1997.
- [38] U.S. Energy Information Administration(EIA),"Annual Energy Outlook," March 2009. Available: [http://www.eia.gov/oiaf/aeo/pdf/0383\(2009\).pdf](http://www.eia.gov/oiaf/aeo/pdf/0383(2009).pdf).
- [39] R. Campos, IMS Research(IHS), "The World Market for Low Voltage AC & DC Motor Drives," November 2012. Available: http://www.imsresearch.com/products-services/pr-detail.php?pr_id=3244.
- [40] A. Fakhrol-Razi, A. Pendashteh, L. C. Abdullah, D. R. A. Biak, S. S. Madaeni, and Z. Z. Abidin, "Review of technologies for oil and gas produced water treatment," *Journal of Hazardous Materials*, vol. 170, pp. 530-551, 10/30/ 2009.
- [41] TE Connectivity Ltd.,"Solutions for Offshore and Commercial Marine," 2012. Available: <http://www.te.com/content/dam/te/global/english/tradeshaw/Topsides2012/solutions-brochure-commercial-offshore-marine.pdf>.
- [42] K. H. Milo Hyde, "Energy Savings from Application of Variable Speed Drive (VSD) Motor Controllers in U.S. Navy Ships " in *ASNE Conference Proceedings.*, 2010.
- [43] J. T. Raimund Rolfes, Richard Degenhardt, Hubert Temmen, Philipp Bürmann, Janos Juhasz, "New design tools for lightweight aerospace structures.," *Proceedings of the Seventh International Conference on Computational Structures Technology, Lisbon, Portugal, 2004*.
- [44] V. R. Stefanovic, "Trends in AC drive applications," *ELEKTRONIKA ELECTRONICS*, p. 10, 2000.

- [45] T. Ericson, "Engineering "Total electric ship"," presented at the Petroleum and Chemical Industry Technical Conference, 2007. PCIC '07. IEEE, 2007.
- [46] H. S. Krishnamoorthy, P. N. Enjeti, I. J. Pitel, and J. T. Hawke, "New medium-voltage Adjustable Speed Drive (ASD) topologies with medium-frequency transformer isolation," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, 2012, pp. 814-819.
- [47] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *Industrial Electronics, IEEE Transactions on*, vol. 51, pp. 641-660, 2004.
- [48] ABB Ltd., "Offshore Drilling Vessels:Total electrical systems for safe, efficient and environmental drilling operations," 2012. Available:
[http://www05.abb.com/global/scot/scot293.nsf/veritydisplay/ccf4f40a1062f74bc12577290036aaca/\\$file/abb%20drilling%20vessel%20brochure_lowres.pdf](http://www05.abb.com/global/scot/scot293.nsf/veritydisplay/ccf4f40a1062f74bc12577290036aaca/$file/abb%20drilling%20vessel%20brochure_lowres.pdf).
- [49] European Wind Energy Association(EWEA), "The European offshore wind industry - key trends and statistics," 2012. Available:
http://www.ewea.org/fileadmin/files/library/publications/statistics/European_offshore_statistics_2012.pdf.
- [50] X. Sun, D. Huang, and G. Wu, "The current state of offshore wind energy technology development," *Energy*, vol. 41, pp. 298-312, 2012.
- [51] Ng, C.H.; Parker, M.A.; Ran, L.; Tavner, P.J.; Bumby, J.R.; Spooner, E., "A multilevel modular converter for a large, light weight wind turbine generator," *Power Electronics, IEEE Transactions on* , vol.23, no.3, pp.1062,1074, May 2008.
- [52] Gjerde, S.S.; Olsen, P.K.; Ljokelsoy, K.; Undeland, T.M., "Control and fault handling in a modular series-connected converter for a transformerless 100 kV low-weight offshore wind turbine," *Industry Applications, IEEE Transactions on* , vol.50, no.2, pp.1094,1105, March-April 2014.

- [53] Solar Energy Industries Association(SEIA), "U.S. solar market insight: 2010 year in review," 2010. Available: <http://www.seia.org/sites/default/files/us-solar-market-insight-report-q1-2011-120627093305-phpapp01.pdf>.
- [54] Essakiappan, S.; Krishnamoorthy, H.S.; Enjeti, P.; Balog, R.S.; Ahmed, S., "A new control strategy for megawatt scale multilevel photovoltaic inverters under partial shading," *Power Electronics for Distributed Generation Systems (PEDG), 2012 3rd IEEE International Symposium on* , vol., no., pp.336,343, 25-28 June 2012.
- [55] Fang Zheng Peng; Akagi, H.; Nabae, A., "A new approach to harmonic compensation in power systems-a combined system of shunt passive and series active filters," *Industry Applications, IEEE Transactions on* , vol.26, no.6, pp.983,990, Nov/Dec 1990.
- [56] E. Koutroulis and F. Blaabjerg, "Methodology for the optimal design of transformerless grid-connected PV inverters," *Power Electronics, IET*, vol. 5, pp. 1491-1499, 2012.
- [57] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems," in *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*, 2010, pp. 1-20.
- [58] J. W. Kolar, J. Biela, and U. Badstuebner, "Impact of power density maximization on efficiency of dc-dc converter systems," in *Power Electronics, 2007. ICPE '07. 7th International Conference on*, 2007, pp. 23-32.
- [59] H. Mirzaee, S. Bhattacharya, R. Sei-Hyung, and A. Agarwal, "Design comparison of 6.5 kV Si-IGBT, 6.5kV SiC JBS diode, and 10 kV SiC MOSFETs in megawatt converters for shipboard power system," in *Electric Ship Technologies Symposium (ESTS), 2011 IEEE*, 2011, pp. 248-253.
- [60] Grady, W.M.; Samotyj, M.J.; Noyola, A.H., "Survey of active power line conditioning methodologies," *Power Delivery, IEEE Transactions on* , vol.5, no.3, pp.1536,1542, Jul 1990.

- [61] Enjeti, P.N.; Shireen, W.; Packebush, P.; Pitel, I.J., "Analysis and design of a new active power filter to cancel neutral current harmonics in three-phase four-wire electric distribution systems," *Industry Applications, IEEE Transactions on* , vol.30, no.6, pp.1565,, Nov/Dec 1994.
- [62] Asiminoaei, L.; Aeloiza, E.; Enjeti, P.N.; Blaabjerg, F., "Shunt active-power-filter topology based on parallel interleaved inverters," *Industrial Electronics, IEEE Transactions on* , vol.55, no.3, pp.1175,1189, March 2008.
- [63] Cuzner, R.; Drews, D.; Kranz, W.; Bendre, A.; Venkataramanan, G., "Power-dense shipboard-compatible low-horsepower variable-frequency drives," *Industry Applications, IEEE Transactions on* , vol.48, no.6, pp.2121,2128, Nov.-Dec. 2012.
- [64] Kerekes, T.; Teodorescu, R.; Rodriguez, P.; Vazquez, G.; Aldabas, E., "A New High-Efficiency Single-Phase Transformerless PV Inverter Topology," *Industrial Electronics, IEEE Transactions on* , vol.58, no.1, pp.184,191, Jan. 2011.
- [65] Harb, Souhib; Balog, Robert S., "Single-phase PWM rectifier with power decoupling ripple-port for double-line-frequency ripple cancellation," *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE* , vol., no., pp.1025,1029, 17-21 March 2013.
- [66] Harb, S.; Mirjafari, M.; Balog, R.S., "Ripple-port module-integrated inverter for grid-connected PV applications," *Industry Applications, IEEE Transactions on* , vol.49, no.6, pp.2692,2698, Nov.-Dec. 2013.
- [67] Elasser, A.; Chow, T.P., "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE* , vol.90, no.6, pp.969,986, Jun 2002.
- [68] Smith, M.C., "Synthesis of mechanical networks: the inerter," *Automatic Control, IEEE Transactions on* , vol.47, no.10, pp.1648,1662, Oct 2002.
- [69] Qing-Chang Zhong, "Active capacitors: Concept and implementation," *Industrial Electronics (ISIE), 2012 IEEE International Symposium on* , vol., no., pp.149,153, 28-31 May 2012.

- [70] M. Pierzchala, M. Fakhfakh, and B. Rodanski, "A novel design of active inductors based on current controlled voltage sources," in *Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD), 2010 XIth International Workshop on*, 2010, pp. 1-4.
- [71] Gyugyi, Laszlo, "Power electronics in electric utilities: static VAR compensators," *Proceedings of the IEEE* , vol.76, no.4, pp.483,494, Apr 1988.
- [72] H. Fnato, Y. Chiku, and K. Harakawa, "Wireless power distribution with capacitive coupling excited by switched mode active negative capacitor," in *Electrical Machines and Systems (ICEMS), 2010 International Conference on*, 2010, pp. 117-122.
- [73] Pierquet, B.J.; Perreault, D.J., "A single-phase photovoltaic inverter topology with a series-connected energy buffer," *Power Electronics, IEEE Transactions on* , vol.28, no.10, pp.4603,4611, Oct. 2013.
- [74] Prasai, A.; Divan, D., "Scaling the Dynamic Capacitor (D-CAP) to medium voltages," *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE* , vol., no., pp.158,165, 12-16 Sept. 2010.
- [75] Funato, H.; Kawamura, A.; Kamiyama, K., "Realization of negative inductance using variable active-passive reactance (VAPAR)," *Power Electronics, IEEE Transactions on* , vol.12, no.4, pp.589,596, Jul 1997.
- [76] Ishikawa, T.; Funato, H.; Ohtaki, T.; Kamiyama, K., "Transmission power control using variable inductance with feedforward- and feedback-based power controllers," *Power Electronics and Drive Systems, 1999. PEDS '99. Proceedings of the IEEE 1999 International Conference on* , vol.1, no., pp.46,51 vol.1, 1999.
- [77] Funato, H.; Kawamura, A., "Control of variable active-passive reactance (VAPAR) and negative inductance," *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE* , vol., no., pp.189,196 vol.1, 20-25 Jun 1994.

- [78] Sabate, J.A.; Vlatkovic, V.; Ridley, R.B.; Lee, F.; Cho, B.H., "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," *Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990., Fifth Annual* , vol., no., pp.275,284, 11-16 March 1990.
- [79] Wood, R.A.; Salem, T.E., "Evaluation of a 1200-V, 800-A All-SiC dual module," *Power Electronics, IEEE Transactions on* , vol.26, no.9, pp.2504,2511, Sept. 2011.
- [80] AVX Corporation, "High power capacitors for power electronics," 2014, Available: <http://www.avx.com/docs/masterpubs/hipwrflm.pdf>.
- [81] J. Long, M. McHenry, D. P. Urciuoli, V. Keylin, J. Huth, and T. E. Salem, "Nanocrystalline material development for high-power inductors," *Journal of Applied Physics*, vol. 103, pp. 07E705-07E705-3, 2008.
- [82] B. Horvath, TMGE Automation Systems, "TM-GE MV Drives," November 2004. Available: <http://www.wmea.net/Technical%20Papers/GE%20Medium%20Voltage%20Drives.pdf>.
- [83] Mohan, Ned, and Tore M. Undeland. *Power electronics: converters, applications, and design*. John Wiley & Sons, 2007.
- [84] Duran-Gomez, J.L.; Enjeti, P.N., "A new approach to mitigate nuisance tripping of PWM ASDs due to utility capacitor switching transients (CSTs)," *Power Electronics, IEEE Transactions on* , vol.17, no.5, pp.799,806, Sep 2002.
- [85] Yang, Yongheng; Blaabjerg, F., "Synchronization in single-phase grid-connected photovoltaic systems under grid faults," *Power Electronics for Distributed Generation Systems (PEDG), 2012 3rd IEEE International Symposium on* , vol., no., pp.476,482, 25-28 June 2012.
- [86] Erickson, Robert W., and Dragan Maksimovic. *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

- [87] Richmond, J.; Leslie, S.; Hull, B.; Das, M.; Agarwal, A.; Palmour, J., "Roadmap for megawatt class power switch modules utilizing large area silicon carbide MOSFETs and JBS diodes," *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE* , vol., no., pp.106,111, 20-24 Sept. 2009.
- [88] Rylko, M.S.; Lyons, B.J.; Hayes, J.G.; Egan, M.G., "Revised magnetics performance factors and experimental comparison of high-flux materials for high-current DC-DC inductors," *Power Electronics, IEEE Transactions on* , vol.26, no.8, pp.2112,2126, Aug. 2011.
- [89] Wima Capacitors, "DC-Link Capacitors," 2011, Available: http://www.mouser.com/pdfDocs/WIMA_DC_Link_Capacitors.pdf.
- [90] JFE Steel Corporation, "JFE Super Cores - Magnetic Property Curves," 2014, Available: <http://www.jfe-steel.co.jp/en/products/electrical/catalog/f2e-001.pdf>.
- [91] Vacuumschmelze GmbH & Co. KG, "Tape-wound cores for magnetic amplifier chokes - Nanocrystalline VITOPERM 500 Z," 2014, Available: http://www.vacuumschmelze.com/fileadmin/documents/broschueren/kbbrosch/PK_VP500Z_10.pdf
- [92] Wakefield-Vette, "Heat sinks," 2014, Available: <http://www.wakefield-vette.com/Portals/0/resources/datasheets/392.pdf>.
- [93] Laird Technologies, "Tgrease 980," 2014, Available: <http://www.abcpol.pl/download/materialy-termoprzewodzace/tgrease->