

PHASE TRANSFORMATION FOR THE LARGE-SCALE SYNTHESIS AND
ASSEMBLY VIA WELDING OF METAL SILICIDE NANOWIRES FOR
THERMOELECTRIC APPLICATIONS

A Dissertation

by

YONGMIN KANG

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Chair of Committee,	Sreeram Vadiraju
Committee Members,	Ibrahim Karaman
	Mustafa Akbulut
	Tahir Cagin
Head of Department,	Ibrahim Karaman

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ABSTRACT

Solid-state thermoelectrics that convert thermal energy into electricity have the potential to increase the efficiencies of existing process and systems (e.g., automobiles). The large-scale deployment of thermoelectrics for terrestrial use requires the following: a) enhancing their efficiencies beyond that are currently possible, and b) their fabrication from non-toxic, inexpensive, earth-abundant elements. Recent studies have determined that nanostructuring of earth-abundant materials, such as magnesium silicide (Mg_2Si), is a possible pathway for accomplishing this task.

Contextually, the overall aim of this dissertation is to engineer highly efficient Mg_2Si nanowire-based thermoelectrics. This was achieved through the design of strategies for (1) the large-scale synthesis of a form of nanostructured Mg_2Si , nanowires of Mg_2Si , and (2) the interface-engineered assembly of the synthesized nanowires into welded nanowire networks that do not have any insulating MgO at the nanowire interfaces. Together, these strategies are intended to offer the ability to control thermal and electrical transport through Mg_2Si .

For the large-scale synthesis of Mg_2Si nanowires, a phase transformation strategy that converts pre-synthesized silicon nanowires into Mg_2Si nanowires was engineered. Experimentation performed indicated that 20 to 300 nm-thick, 5 to 20 μm -long silicon nanowires obtained by electroless etching can be phase transformed into polycrystalline Mg_2Si nanowires by reacting them with magnesium supplied via the vapor phase. To prevent the formation of multiple nuclei within each silicon nanowire during the phase

transformation process and the formation of polycrystalline Mg₂Si nanowires, a solid-state phase transformation process was engineered. Here, the solid-state reaction of sharp-tipped silicon nanowires with magnesium foils was employed for obtaining single-crystalline Mg₂Si nanowires.

To assemble the nanowires, the solid-state phase transformation strategy was extended and the phase transformation of silica nanoparticle coated silicon nanowires was employed. This procedure led to the formation of welded Mg₂Si nanowire networks, where both the nanowires and the bridges connecting the nanowires were composed of Mg₂Si. Thermoelectric performance evaluation of these networks and microcrystalline Mg₂Si devices proved our hypothesis and indicated a 2-fold increase in the power factors. The high power factor of $0.972 \times 10^{-3} \text{ Wm}^{-1}\text{K}^{-2}$ achieved at 875 K is twice that reported in the literature for undoped Mg₂Si.

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CHAPTER I

INTRODUCTION

The growing demand for fossil fuel and increasing global warming have become critical issues in daily lives, and alternative cleaner energy source is required.¹ Most of the waste energy generated (about 57%) in the big industrial plants and automobile engines is just lost out into the environment.¹⁻⁵ Thermoelectric devices can convert this waste heat directly into electricity and they have the potential to reduce greenhouse gas emissions and provide a cleaner mode of generating electricity.⁶⁻⁸ They can not only enhance the efficiencies of existing processes by converting some of the waste heat generated into electricity, but also generate electricity from renewable sources such as solar energy.^{9, 10} Thermoelectric device have been used in the automobile to control the temperature on the seat and generate electricity from surplus heat on exhaust system.^{1, 11} NASA developed radioisotope thermoelectric generator (RTG) to convert heat from radioactive fission into powering up satellites such as Viking, Apollo 12-17, and Voyager.¹² They are also used to generate electricity for outdoor activities by using cooking fire as the heat source (600°C) and boiling water in a cooking pot as the heat sink (100°C).¹¹ Also, thermoelectric devices can be manufactured and designed in various sizes range, shapes, operating voltage and current.

In this chapter, background information on thermoelectricity and high performance thermoelectric materials are described. Especially, enhancement of the

thermoelectric efficiency through nanostructuring of earth abundant materials, such as Mg_2Si , is provided.

1.1 Background on Thermoelectricity

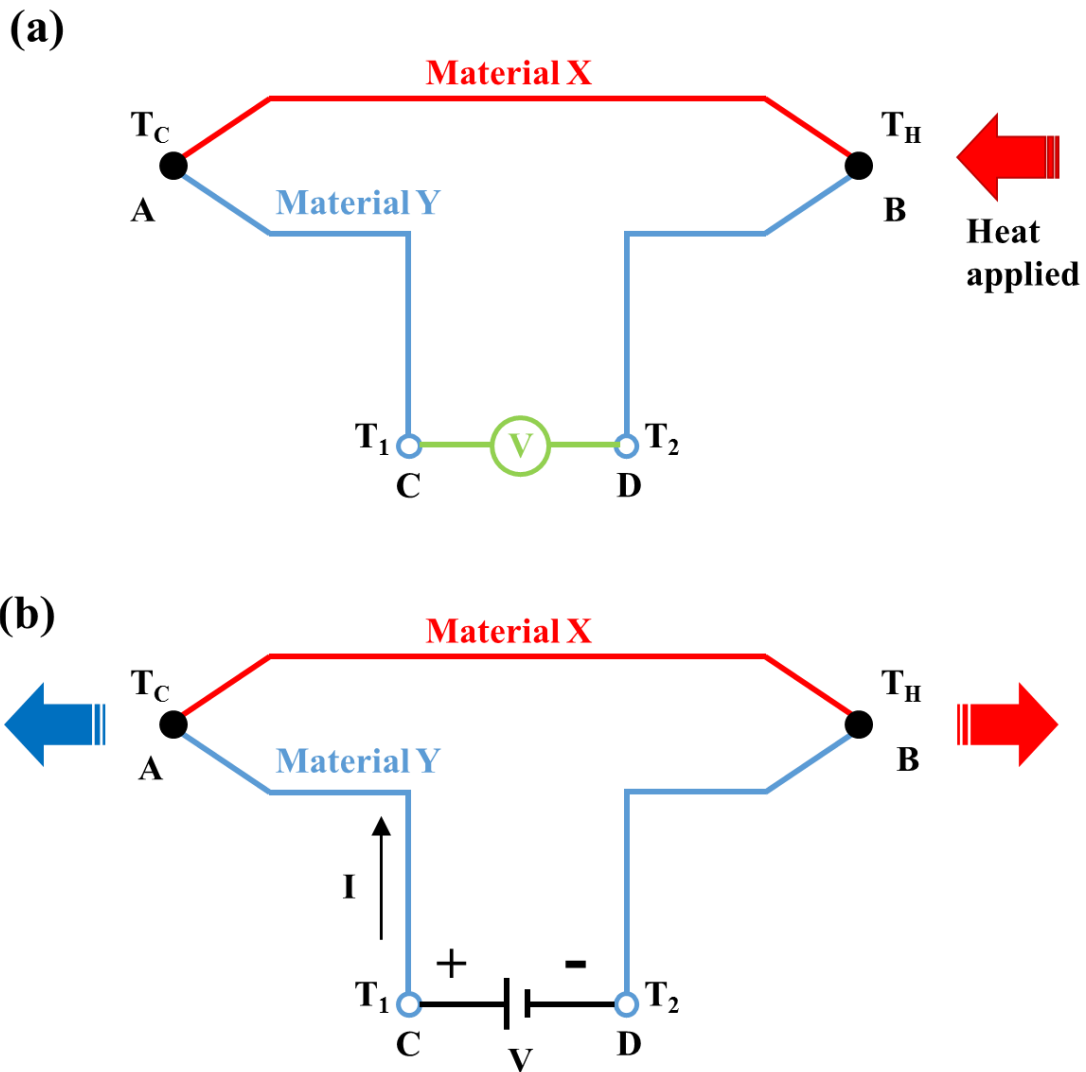


Figure 1.1. Schematics of a thermocouple circuit formed from two dissimilar materials X and Y. (a) Illustration of Seebeck effect for electricity generation and (b) Illustration of Peltier cooling.¹³⁻¹⁶

The generation of electricity in a thermoelectric materials is based on Seebeck effects. Figure 1.1 show a thermocouple circuit formed from two dissimilar materials X and Y. If there is temperature difference between junction A and B, electric potential, V , is produced between C and D, and the V is given by $V = S(T_H - T_C)$ where S is Seebeck coefficient (V/K). This is called the Seebeck effect. In the reverse process, if external voltage is applied between C and D, electric current will flow through the circuit. Because of the electric current, cooling ($-Q$) of junction A and heating of junction B ($+Q$) occur. This complementary effect is called Peltier effect, and the rate of electric current (I) to q defines the Peltier coefficient as $\pi = I/Q$.

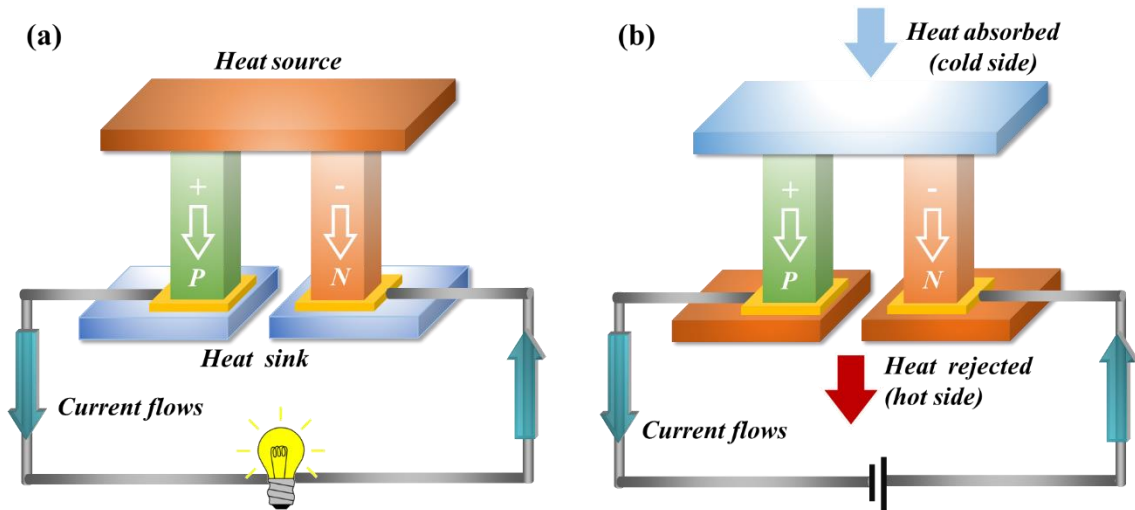


Figure 1.2. Schematics of (a) power generation and (b) refrigeration thermoelectric devices. A thermoelectric device consists of p-n junctions which are connected electrically in series and thermally in parallel, respectively.¹⁷⁻¹⁹

A thermoelectric device consists of p-n junctions which are connected electrically in series and thermally in parallel, respectively. Figure 1.2 shows the combination of series-connected p- and n-type semiconductor materials between hot and cold sides. When temperature gradient is applied to the devices, charge carriers in hot side (n-type: electrons, p-type: holes diffuse to the cold end, whereas, cold charge carriers diffuse to the hot end less than hot charge carriers. Because of the electrons and holes diffusion from the hot side to the cold side, it results current flow through the module in Figure 1.2.

The maximum efficiency of thermoelectric power generation is given by

$$\eta = \frac{\text{energy supplied to the load}}{\text{heat energy abosorbed at hot junction}}$$

$$= \frac{\Delta T}{T_h} \cdot \frac{\sqrt{1 + zT} - 1}{\sqrt{1 + zT} + \frac{T_c}{T_h}}$$

where T_c is hot side temperature and T_h is cold side temperature. To maximize the efficiency, both high zT and a large average of zT in the specific temperature range are required to make a large temperature drop. The maximum performance of refrigeration can be measured by the coefficient of performance (COP) given by

$$\text{COP} = \frac{\text{heat abosrbed}}{\text{electrical power input}}$$

$$= \frac{T_c}{T_h - T_c} \cdot \frac{\sqrt{1 + zT} - \frac{T_h}{T_c}}{\sqrt{1 + zT} + 1}$$

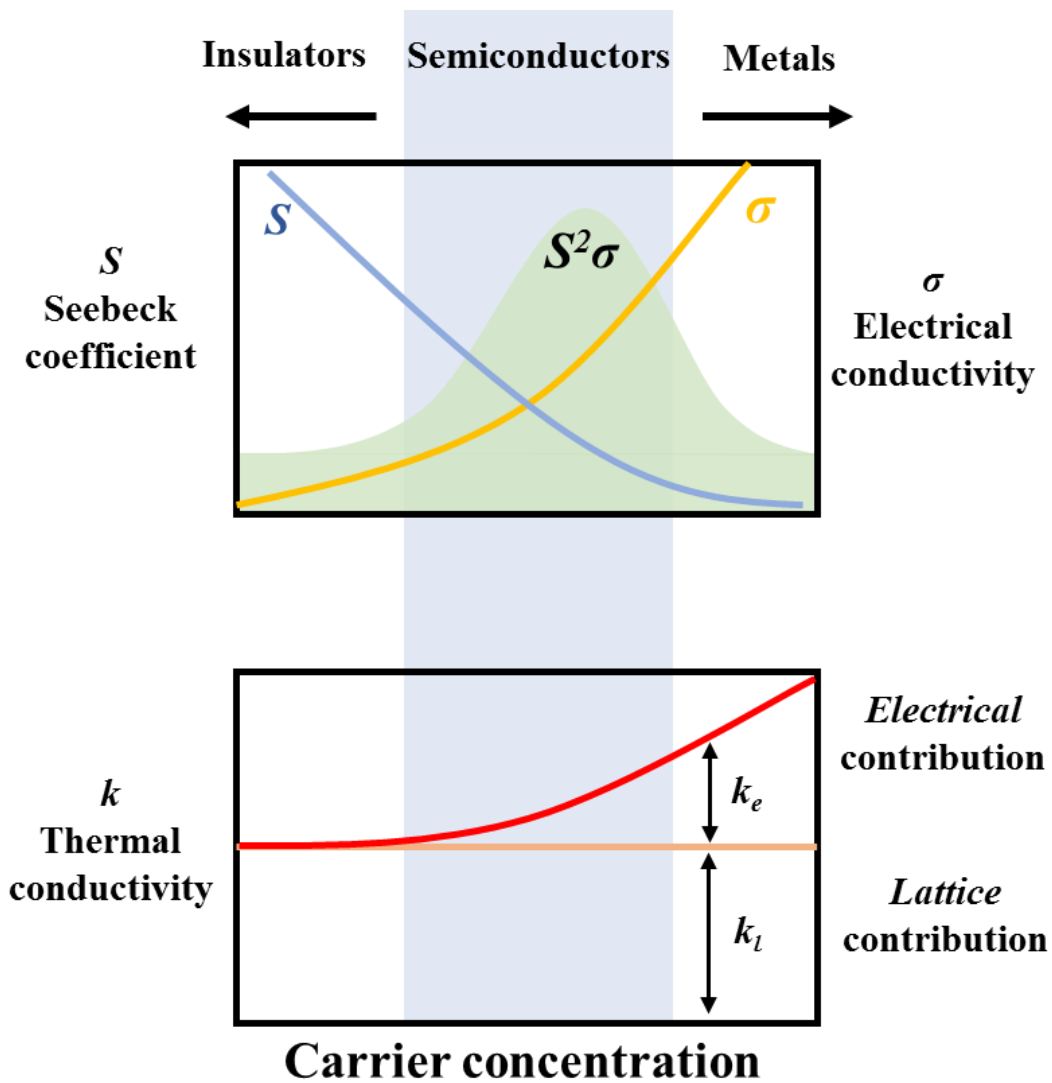


Figure 1.3. Schematic diagram of the dependence of electrical conductivity (σ), Seebeck coefficient (S), and thermal conductivity (k) of insulators, semiconductors and metals.^{6, 20}

To increase the value of COP for thermoelectric refrigeration, high zT is required to maximize the temperature difference. The performance of thermoelectric materials that serve as building blocks in the fabrication of thermoelectric modules can be gauged by examining their figure of merit, zT , which is given by

$$zT = \frac{S^2 \sigma T}{(k_e + k_l)}$$

where S is the Seebeck coefficient of the material, σ is the electrical conductivity of the material, and κ_e and κ_l are the thermal conductivities of the material from electronic and lattice contributions, respectively. The zT values of current, commercially available thermoelectric materials are approximately one.^{6, 21}

Figure 1.3 shows dependence of electrical conductivity (σ), Seebeck coefficient (S), and thermal conductivity (k) of insulators, semiconductors and metals. Metals have high electrical conductivity but they have relatively low Seebeck coefficient and high thermal conductivity. Insulators have high Seebeck coefficient, however, they exhibit low electrical conductivities. Enhancing the performance of thermoelectrics beyond that is currently achievable requires materials with lower thermal conductivities and higher electrical conductivities. According to the Wiedemann-Franz law, κ_e cannot be reduced without reducing σ .^{6, 8} This constraint leaves room for enhancing zT of materials through a reduction in only their κ_l .⁶⁻⁸ The lattice thermal conductivity of an isotropic material is given by

$$k_l = \frac{1}{3} \int c_\lambda(\lambda, T) v(\lambda) L(\lambda, T) d\lambda$$

where λ is the wavelength, c_λ is the spectral specific heat per unit wavelength, v is the group velocity, and L is the spectral mean-free path. The lattice thermal conductivity (κ_l) of materials could be reduced using two different strategies, either reducing $c_\lambda(\lambda, T)v(\lambda)$ through phonon confinement in nanowires and superlattices with extremely small dimensions, or reducing $L(\lambda, T)$ through enhanced phonon scattering in boundaries and

interfaces in nanowires and composites.^{7, 8} Also, materials in single-crystalline one-dimensional nanostructured format also exhibit higher electrical conductivities compared to their nanoparticle counterparts. Therefore nanowires as a material format could be employed to decrease the thermal conductivity by selectively enhancing phonon scattering, and enhance thermoelectric performance compared to bulk counterparts.²²⁻²⁶

1.2 High Performance Thermoelectric Materials

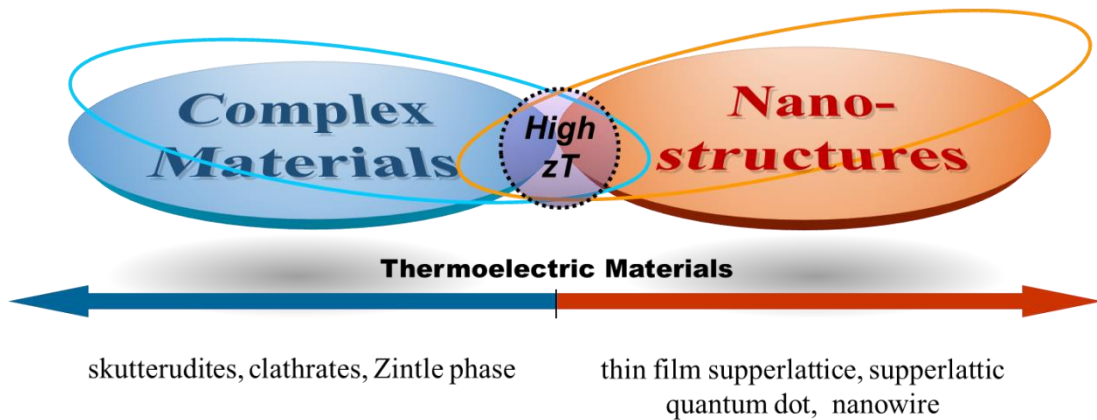


Figure 1.4. Enhancement of thermoelectric efficiency by two different approaches: one by complex crystalline bulk materials, and the other by low dimensional nanostructured materials.

In the 1960s, high performance thermoelectric materials based on Bi_2Te_3 and its alloys were developed. The maximum figure of merit achieved with these materials is 1. But these materials were not cost effective for their use in terrestrial applications owing to their high cost per efficiency metric. After 1990s, theoretical predictions indicated that the thermoelectric efficiency could be enhanced by two different approaches (Figure 1.4):

through the use of complex crystalline bulk materials, or through the use of low dimensional nanostructured materials.^{6, 21, 27-33} In fact, high figure of merit, $ZT > 1$, was obtained using complex thermoelectric materials such as skutterudites,^{34, 35} clathrates,³⁶ and Zintl phase.³⁷ In the case of low dimensional nanostructured materials, power factor ($S^2\sigma$) can be enhanced by the quantum confinement effect when the size decrease to a nanometer scale,^{30, 38} and thermal conductivity expected to be decreased by scattering phonons propagation at the interfaces when the dimension of materials is less the mean free path of phonons.^{30, 32} In fact, Venkatasubramanian et al. have reported that a zT of 2.4 (at 300K) can be achieved in p-type superlattice layers of Bi_2Te_3 and Sb_2Te_3 through the strong scattering at the interfaces that led to a decrease in lattice thermal conductivity.³¹ Kanatzidi et al. have reported Ag-Sb nanostructure embedded in a PbTe matrix ($\text{AgPb}_m\text{SbTeTe}_{2+m}$) showing zT of 2.2 (at 800K). Also, Harman et al. have reported that PdTe and PbTeSe superlattice quantum dot structure showing zT of 1.6 (at room temperature) and 3.0 (at 600K).³³ Specifically, materials in nanowire morphology can enhance zT through the quantum confinement effect or phonon scattering at their boundaries. Both theoretical and experimental study of the nanowire based thermoelectrics confirmed that zT increases with decreasing the diameter of nanowires.^{32, 39-42} For example, Ju et al. reported that the effective mean free path of dominant phonon of silicon is near to 300 nm. They showed that silicon nanowires less than diameter of 300 nm, and it could reduce their effective mean free path.⁴³ Also, Boukai et al reported that zT of 1 (at 200 K) is available for silicon nanowires by the reduction in thermal conductivities and it is about 100-fold improvement over the bulk silicon value.⁴²

Hochbaum et al. showed that thermal conductivity of rough silicon nanowire surface with diameters of about 50 nm were two orders of magnitude lower than the bulk silicon due to enhanced phonon boundary scattering at the rough surface and zT was 0.6 at room temperature.²²

1.3 Metal Silicide Thermoelectrics

Table 1.1. Figure of merit of Mg_2Si based thermoelectric materials

Material	Type	zT
Mg_2Si	N	0.04 (823 K) ^{44, 45}
$Mg_2Si_{0.85}Bi_{0.15}$	N	0.7 (775 K) ⁴⁶
$Mg_2Si_{0.4}Sn_{0.6}$	N	1.1 (800 K) ⁴⁷
$Mg_2(Si_{0.4}Sn_{0.6})Bi_{0.03}$	N	1.2 (573 K) ⁴⁸
$Mg_2Si_{0.55}Sn_{0.4}Ge_{0.05}Bi_{0.02}$	N	1.4 (800K) ⁴⁹
Pb doped- Mg_2Si	N	0.5 (873K) ⁴⁵
Sb doped Mg_2Si	N	0.62 (823K) ⁵⁰
$Mg_2Si_{0.6}Sn_{0.4}$	N	1.1 (830 K) ⁵¹
$Mg_2Si_{0.6}Ge_{0.4}$	P	1.68 (629 K) ⁵²
Li and Ag doped $Mg_2Si_{0.25}Sn_{0.75}$	P	0.32 (610 K) ⁵³

Thermoelectric materials have been studied for their applications in various fields. Some of the highly researched thermoelectric materials with good performance are

Bi₂Te₃-based alloys, CoSb₃-based skutterudites, Ag-Pb-Sb-Te, Half-Heusler compounds,^{6, 21, 54} Also, metal silicides are excellent compounds for potential thermoelectric applications as they are inexpensive, environmentally friendly, mechanically and chemically strong properties. Especially, higher silicides of transition metals (such as Ru, Mn, Fe, Ru and Cr), and magnesium silicide (Mg₂Si) attract special attention because of high figure of merit. Table 1.1 shows figure of merit of Mg₂Si based thermoelectric materials. Figure of merit of higher manganese silicide (Mn₄Si₇) values up to 0.8-0.9 due to their low thermal conductivity of 2-4W/mK at the temperature range of 300 – 700K.⁵⁵⁻⁵⁷ Ru₂Si₃ (melting point 1970 K) can be a candidate for higher temperature application than conventional SiGe (melting point 1550K).⁵⁶ However, an essential aspect that needs to be considered in the design of these materials for the fabrication of thermoelectrics is their cost. Lowering the cost of thermoelectrics modules requires their fabrication from component elements that are abundantly available in the earth's crust.⁵⁸ One of the materials that fit into all the above criteria is magnesium silicide (Mg₂Si). It is non-toxic, comprised of only abundantly available elements, and inexpensive. Mg₂Si is a low bandgap semiconductor and has a bandgap of 0.78 eV.⁵⁹ However, Intrinsic Mg₂Si has low zT value less than 0.2, because of the low carrier concentration.⁴⁶ The zT values of bulk Mg₂Si alloyed with Ge, Sn, Sb or Bi have been reported in the 0.5-1.4 range as shown in Table 1.1. Also, the preparation and thermoelectric property characterization of bulk ingots, thin films, and nanocrystals of Mg₂Si have been reported numerous times in the literature.⁶⁰⁻⁶⁶ It was also predicted through theoretical modeling by Satyala and Vashaee that reduction of grain sizes lead to an increase in the zT values of Mg₂Si.⁶⁷

Therefore, it is possible to achieve zT values of ~ 1.2 by making Mg_2Si in nanowire form with diameters on the order of 5-20 nm even without impurity doping in Mg_2Si .⁶⁷

1.4 Dissertation Outline

The main objective of this dissertation is large scale synthesis and assembly of Mg_2Si nanowires for fabrication of highly efficient thermoelectric modules. The three major drawbacks involved in the synthesis and assembly Mg_2Si nanowires for fabricating thermoelectrics (Figure 1.5) are solved and presented.

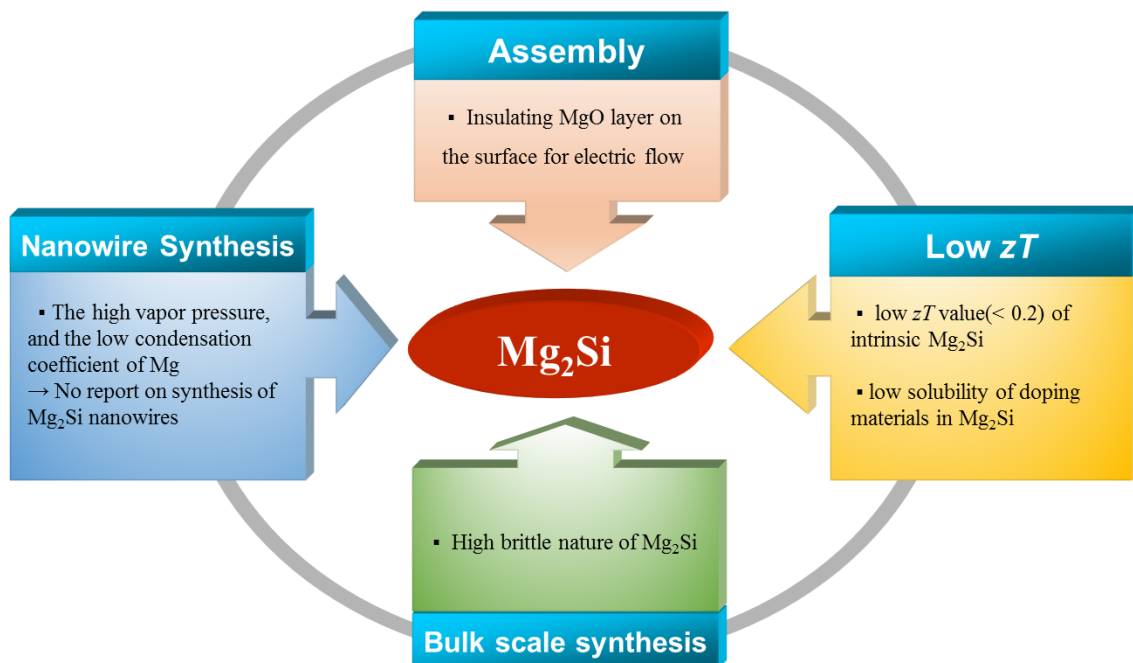


Figure 1.5. Problems with Mg_2Si for use as a thermoelectric material.

Firstly, the high vapor pressure, and consequently the low condensation coefficient of magnesium coupled with its high propensity to oxidation prevent the use of chemical

vapor deposition (CVD) for the synthesis of Mg_2Si nanowires.^{63, 68} Because of these problems, synthesis of Mg_2Si nanowires and their thermoelectric properties are not reported yet. Therefore, development of alternative technique, which is simple and inexpensive, is required for synthesizing Mg_2Si nanowires. In this dissertation, solid-state phase transformation of pre-synthesized silicon nanowires into Mg_2Si nanowires was employed as a strategy for the synthesis of Mg_2Si nanowires. Chapter II of this dissertation describes fabrication of silicon nanowires and arrays by using electroless etching of silicon wafers for the solid-state phase of silicon nanowires into Mg_2Si nanowires. The phase transformation of silicon nanowires into polycrystalline Mg_2Si nanowires is discussed in Chapter III. Mg vapor was supplied onto silicon nanowire surface, and the diffusion and reaction of Mg with silicon nanowire led to the formation of polycrystalline Mg_2Si nanowires. Chapter IV describes single-crystalline phase transformation of Si nanowires into Mg_2Si nanowires. Solid-state reaction of silicon nanowire tips with magnesium foils was employed to make formation of only one Mg_2Si nucleus per nanowire, and it led to phase transformation into single-crystalline Mg_2Si nanowire.

Secondly, the MgO layer on Mg_2Si nanowire surface insulates the electric flow,⁶⁹ and the formation of the oxide is enhanced during the thermoelectric heating and cooling cycles. In Chapter V, the Mg_2Si nanowires were welded with same Mg_2Si which lead to oxide-free interfaces and provide an uninterrupted electrical path without change in a nanowire morphology.

Finally, because of high brittle nature of Mg_2Si ,⁷⁰ the Mg_2Si nanowires cannot be easily removed from the substrates without braking, and this makes it hard handle and

assemble it into bulk scale devices like nanowire a pellet. The large-scale synthesis of Mg_2Si nanowire and assembly into bulk scale Mg_2Si device and its thermoelectric properties will be discussed in Chapter VII.

CHAPTER II

FABRICATION OF SILICON NANOWIRES AND ARRAYS

2.1 Introduction

In recent years, silicon nanowires have attracted interest because of their chemical stability, mechanical strength, ease of fabrication. The transport properties of nano-scale devices made from silicon are well studied which makes the design and fabrication of these devices simple and inexpensive. Silicon nanowires have potential application in thermoelectrics,^{22, 42} microelectronics,^{71, 72} lithium ion batteries,^{73, 74} light emitting diodes,⁷⁵ solar cells,⁷⁶ and bio/chemical sensors.⁷⁷

There are various ways to synthesis of silicon nanowires. The most commonly used silicon nanowires synthesis method is the vapor-liquid solid (VLS).^{78, 79} Figure 2.1 shows the schematics of VLS growth mechanism of silicon nanowire. In this reaction, gold nanoparticle is generally used as a catalyst and SiCl_4 is used as the silicon source gas, and the gold nanoparticle catalyzes the growth of silicon nanowire from the SiH_4 or SiCl_4 vapor source by forming liquid Au-Si droplet. The catalyst defines the diameter of nanowire, and the growth time and rate kinetics defines the length of nanowire. Typically, the diameter of nanowire is in range of five - several hundred nm, and the length can be controlled from several nm to tens of microns.

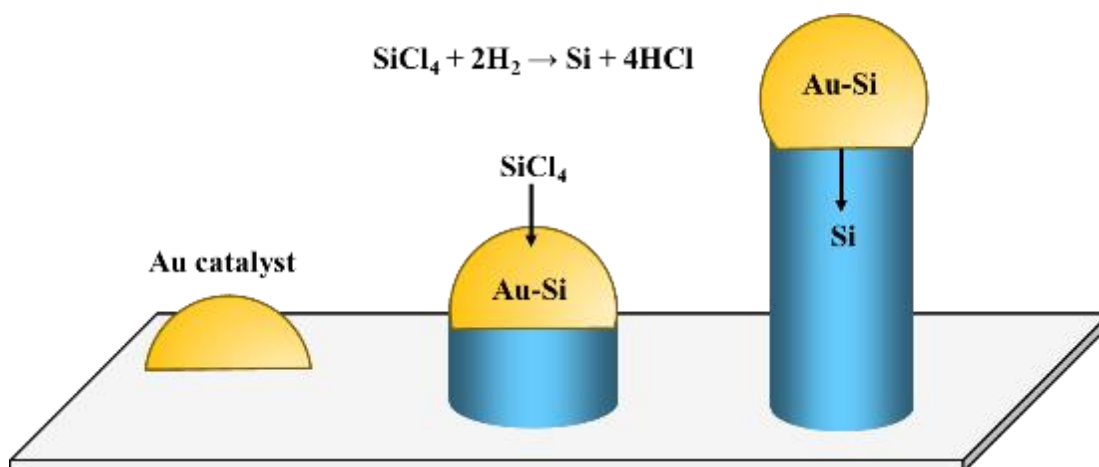


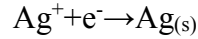
Figure 2.1. Schematics of vapor-liquid-solid (VLS) growth mechanism of silicon nanowire synthesis.

There are other techniques available to synthesize silicon nanowires such as anodic alumina oxide (AAO) template assisted growth,⁸⁰ thermal evaporation,⁸¹ molecular beam epitaxy,⁸² and electroless etching of silicon wafers.^{22, 83, 84} However, the electroless etching method is not required gold catalyst and the mild etching conditions do not lead to unintentional contamination of the nanowires, unlike the traditional vapor-liquid-solid approaches.⁸⁵ Also, large scale production of vertical silicon nanowires over large area can be accomplished at low temperatures (25 – 50 °C) in a cost effective manner. Silicon nanowires fabricated by this method, have same crystal structure and dopants as the wafer from which these nanowires are fabricated.

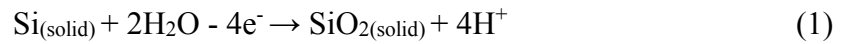
2.2 Fabrication of Silicon Nanowires by Electroless Etching Method

Silicon nanowires necessary for the phase transformation were obtained using electroless etching of silicon wafers. The electroless etching of silicon was accomplished

by using mixture of AgNO₃ and HF solution. In this process, galvanic reaction of silicon by



take place and forms Ag nanoparticles on silicon wafer surface. The silicon underneath the Ag nanoparticle oxidizes (equation 1) and etched by HF after which the Ag nanoparticles fall in to pit (equation 2).



After Si wafer etching, excess Ag was removed by dipping the wafer in HNO₃ solution at 100 °C for 1hour. The selective etching of silicon wafer leaves vertical holes on the surface, and remaining structure results in the formation of well-oriented silicon nanowire arrays (Figure 2.2). The silicon nanowires were fabricated using various concentration of AgNO₃ in HF solution in range of 0.2 - 0.8 M, various etching time in the range of 5 minute to 2 hours and different temperatures in the range of 25 - 50°C. Electroless etching of both p-type (boron doped) and n-type (phosphorus or antimony doped) wafers was performed multiple.

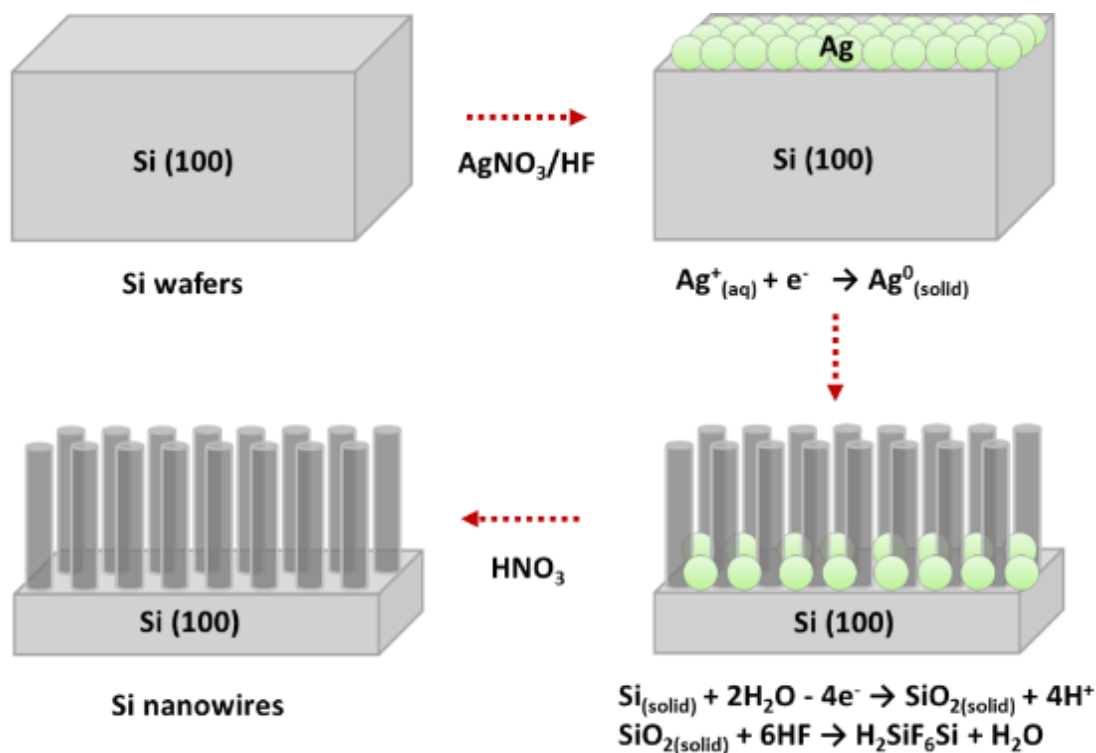


Figure 2.2. Schematic illustration of electroless etching of silicon wafer using AgNO_3/HF solution.⁸⁶⁻⁸⁹

2.3 Results and Discussion

2.3.1 Diameter and Length Control of the Silicon Nanowires

Scanning electron microscope (SEM) images of silicon nanowires fabricated by using 0.2M, 0.4M and 0.8M AgNO_3 solution in 5M HF solution are shown in Figure 2.3. The electroless etching of boron doped p-type silicon wafer result in formation of vertically arrayed silicon nanowires. By increasing the concentration of AgNO_3 solution from 0.2M to 0.8M, the number of Ag nanoparticles on silicon wafer surface increases which increases the area of silicon wafer etched, thereby increasing the number of

nanowires formed. Also, the effect of HF concentration was investigated but it did not made difference in density and diameter of the nanowires.

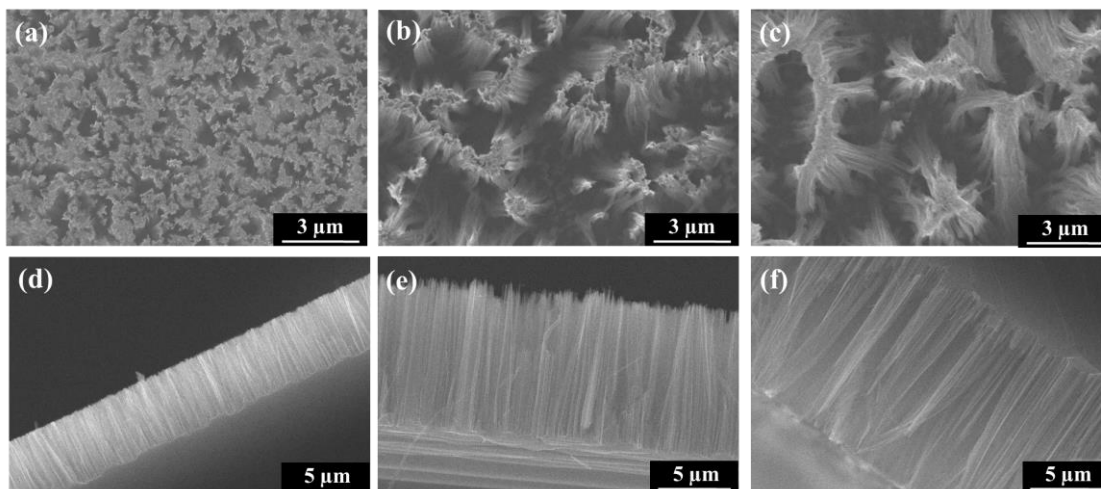


Figure 2.3. Scanning electron micrographs of silicon nanowires fabricated by using (a), (d) 0.2M, (b), (e) 0.4M and (c), (f) 0.8M AgNO_3 solution in 5M HF.

Figure 2.4 and Figure 2.5 show SEM images of top view (a)-(b) and cross-sectional view (c)-(d) of the silicon nanowire synthesized at 0.4M AgNO_3 /5M HF solution at room temperature and 50°C, respectively. At room temperature, the diameter of the nanowire was 100 – 300 nm, and the diameter was 20 – 100 nm of the nanowire was decreased by increasing temperature of the solution up to 50°C because the applied thermal energy enhanced the number of silver nanoparticles generation and leave behind columns of one-dimensional silicon nanostructures.⁹⁰ Also, the length of the nanowire was increased at the same time from 5μm to 10μm because of enhanced rate of etching.⁹¹

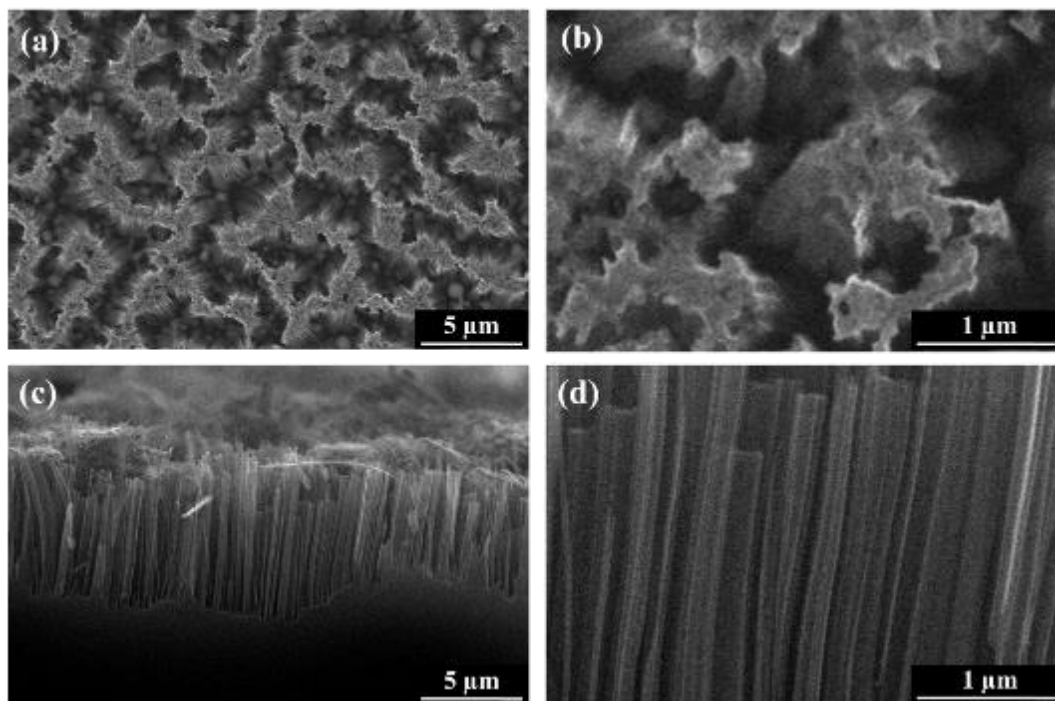


Figure. 2.4. SEM images of top view (a)-(b) and cross-sectional view (c)-(d) of the silicon nanowire synthesized at room temperature.

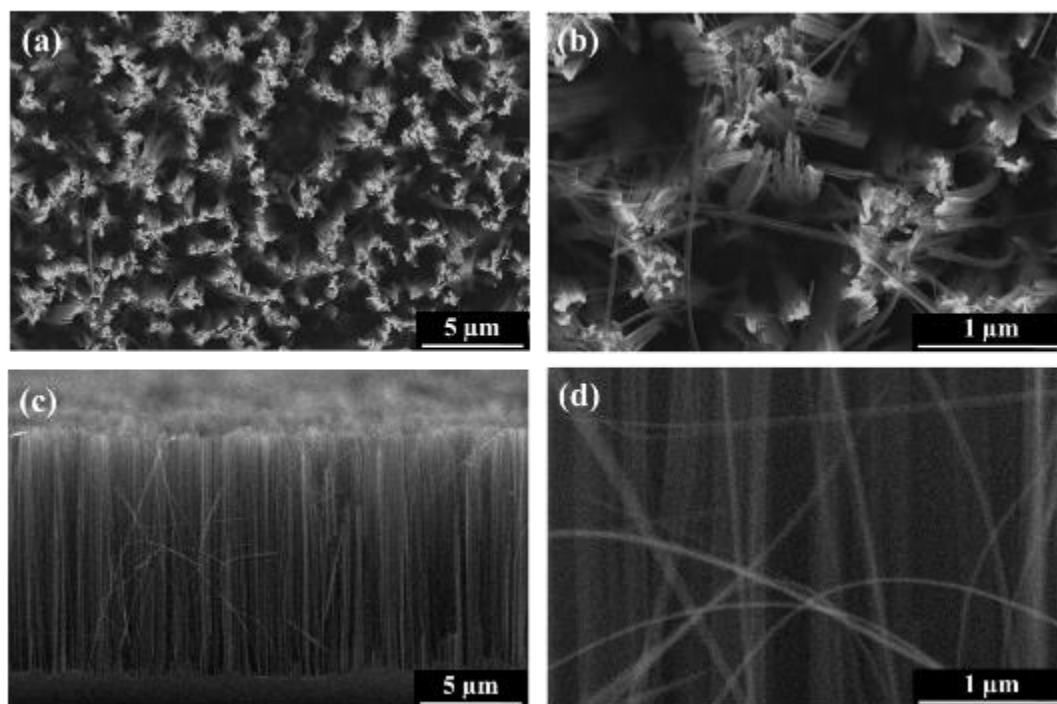


Figure. 2.5. SEM images of top view (a)-(b) and cross-sectional view (c)-(d) of the silicon nanowire synthesized at 50°C.

Figure 2.6 shows SEM images of the silicon nanowires fabricated in 0.4M AgNO_3 /5M HF at 50°C for 5min and 2h, respectively. The length of silicon nanowire was increased from 5μm to 20μm. Further increase in etching time led to increase in the length of the nanowire but the nanowires branched up because of van der Waals forces.⁹²

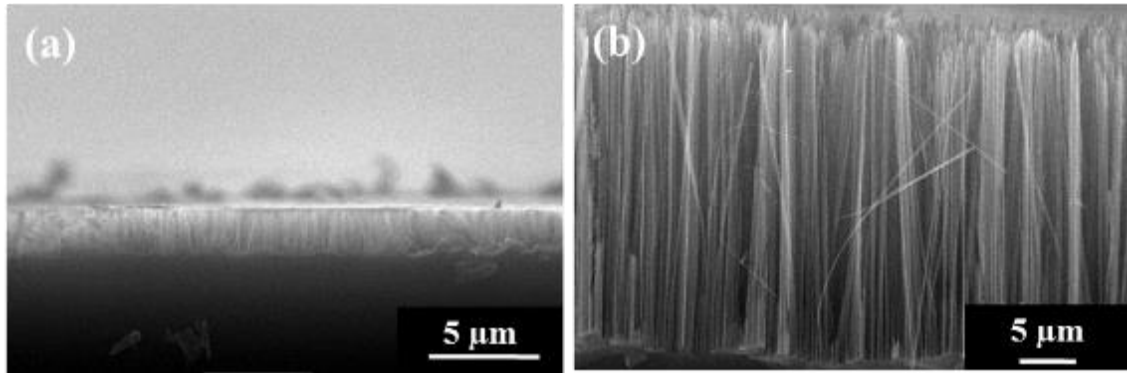


Figure 2.6. SEM images of the silicon nanowires fabricated in 0.4M AgNO₃/5M HF at 50°C for (a) 5minutes and (b) 2hours.

2.3.2 Crystal Structure of the Silicon Nanowires

Transmission electron microscopy (TEM) of nanowires obtained by etching of p-type single-crystalline (100) wafers indicated that they were single-crystalline in nature, and that their growth direction was either along the [110] (Figure 2.7(a)) or the [100] (Figure 2.7(b)) crystal orientation. (100) Oriented silicon wafers are etched perpendicular to the wafer surface along [100] direction, and it leads to the formation of vertically arrayed silicon nanowires which have [100] crystal orientation. However, the [110] oriented silicon nanowires were also observed. Etching of planes other than (100) planes on the rough unpolished back side of the wafer is believed to be responsible for the formation of these nanowires. And it was confirmed by studying the nanowire in a TEM shown in Figure 2.8. Also the nanowire showed rough surface (Figure 2.8(c)) compared with other silicon nanowire fabrication techniques. The rough surface is caused by the slow HF etching and corrosive condition of the solution, or randomly oxidation after etching.²² This rough surface can their thermal conductivity by phonon scattering at the surface without significant change of the power factor ($S^2\sigma$).²²

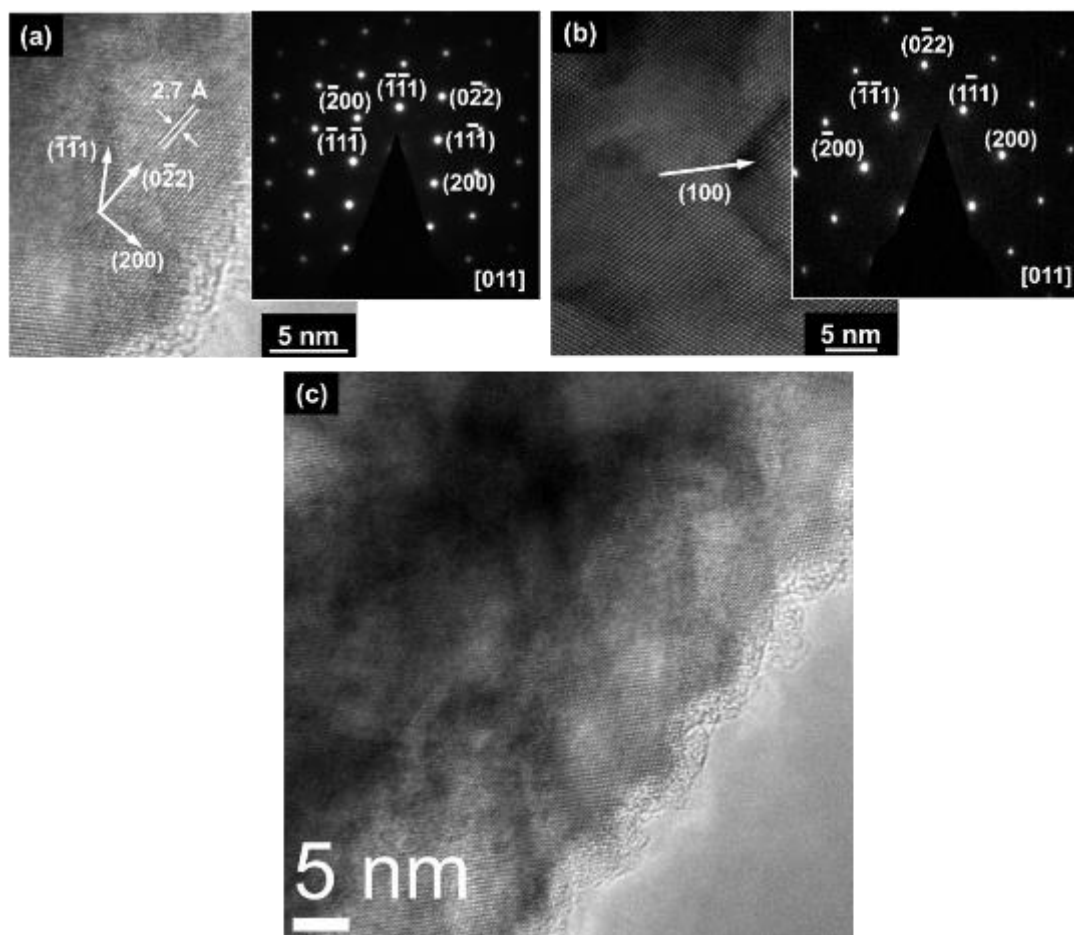


Figure 2.7. High resolution TEM micrograph of a silicon nanowires indicating that they are single-crystalline in nature and exhibit either (a) [110] or (b) [100] growth direction,* and (c) rough silicon nanowire surface image.

* Parts (a) and (b) are reprinted from *Materials Letters* **2013**, *100*, Yongmin Kang, Lance Brockway, Sreeram Vaddiraju, “A simple phase transformation strategy for converting silicon nanowires into metal silicide nanowires: Magnesium silicide”, 106-110, Copyright 2013, with permission from Elsevier

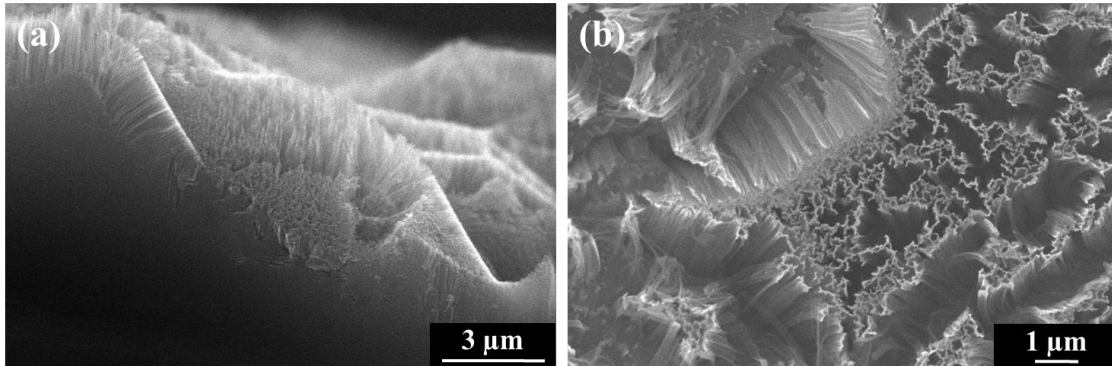


Figure 2.8. (a) Cross sectional, and (b) top view SEM images of silicon nanowires etched perpendicular to the rough wafer surface.

2.3.3 Impurity Doping in the Silicon Nanowires

Not only boron (B) doped p-type silicon wafer, but also phosphorus (P) or antimony (Sb) doped silicon wafers were applied in the etching to fabricate n-type silicon nanowires (Figure 2.9). Although p-type and n-type have different charge carrier characteristics, both n-type silicon wafers shows that similar etching behavior was observed in the same etching conditions.

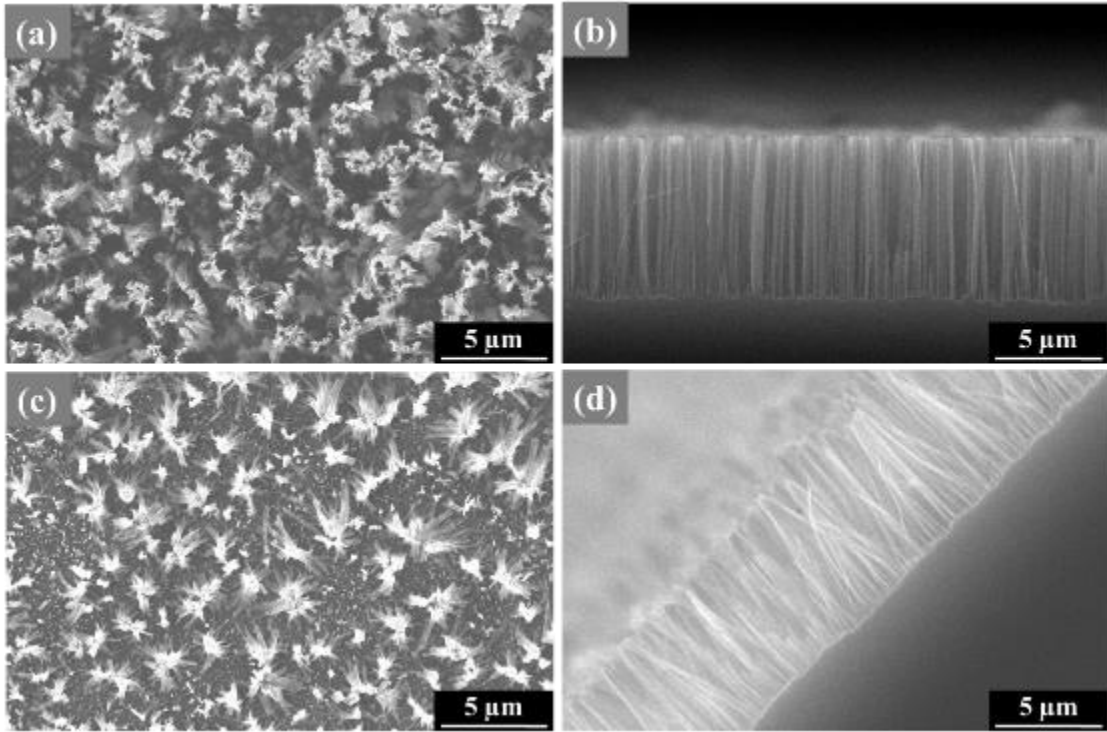


Figure 2.9. SEM images of n-type silicon nanowire array from (a), (b) phosphorus and (c), (d) antimony (Sb) doped silicon wafers.

2.3.4 Mass Production of the Silicon Nanowires

For the large scale synthesis of silicon nanowires, multiple p-type (100) oriented silicon wafers were etched with 0.04M AgNO_3 /5M HF solution at 50°C for 2h. After etching, the acid cleaned silicon nanowire wafers were sonicated in isopropyl alcohol for 20 second to remove the nanowires from the wafer. The isopropanol was the removed by evaporation to obtained silicon nanowire powders. For example, 15 pieces of 4 inch wafers gave 300mg of silicon nanowire powder, and the powder still had nanowire morphology (Figure 2.10).

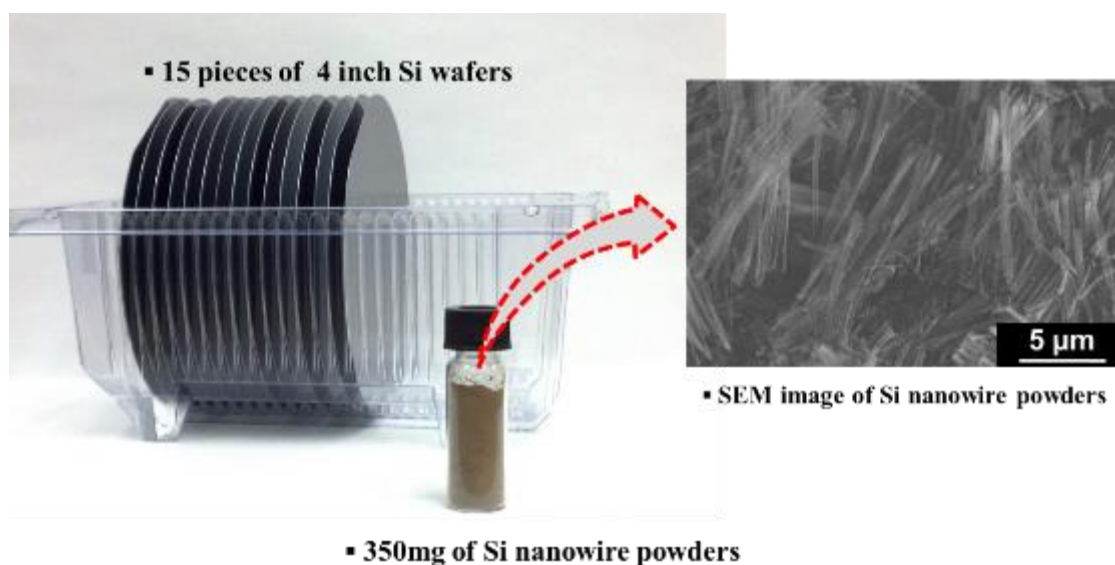


Figure 2.10. Mass production of silicon nanowire by electroless etching of silicon wafers. 350 mg of silicon nanowire powder was obtained from the 15 pieces of 4 inch wafers etching.

2.4 Conclusions

Silicon nanowires necessary for the phase transformation were obtained using electroless etching of silicon wafers. Various etching conditions such as concentration of AgNO_3/HF solution, etching temperature and time was applied to the p-type (B doped) and n-type (P or Sb doped) wafers. The selective etching of silicon wafer left vertical holes on the wafer surface, and resulted in the formation of well-oriented silicon nanowire arrays. The diameter of nanowires was controlled from 20 nm to 300 nm, and the length of nanowire was controlled in range of 3 – 20 μm . The nanowire was single-crystalline in nature, and that growth direction was either along the [110] or the [100] crystal orientation. The zT of silicon nanowires can be increased by optimizing dopant concentration, diameter and roughness of the nanowires. These attributes can also increase the zT of other

silicide nanowire systems, which can be made by phase transformation of silicon nanowires.

CHAPTER III

POLYCRYSTALLINE PHASE TRANSFORMATION OF Si NANOWIRES INTO

Mg₂Si NANOWIRES*

3.1 Introduction

In this chapter, the aim of the study is to explore the possibility of completely phase transforming silicon nanowires into metal silicide nanowires. Specifically, the reaction of silicon nanowires with magnesium supplied via the vapor phase for their phase-transformation into Mg₂Si nanowires is studied. The intent is to preserve the nanowire morphology after the phase transformation of silicon into Mg₂Si, without introducing any additional contaminants in them through the use of external templates or catalysts.

3.2 Experimental Methods

The silicon nanowires necessary for the phase transformation studies were obtained using electroless etching, previously described in a number of publications.^{84, 93, 94} This procedure typically results in the formation of well-oriented silicon nanowire arrays. This process was specifically chosen for silicon nanowire synthesis for the following reasons: **i)** the mild etching conditions do not lead to unintentional contamination of the nanowires, unlike the traditional vapor-liquid-solid approaches,⁹⁴⁻⁹⁶

* Parts of this chapter are reprinted from *Materials Letters* **2013**, *100*, Yongmin Kang, Lance Brockway, Sreeram Vaddiraju, “A simple phase transformation strategy for converting silicon nanowires into metal silicide nanowires: Magnesium silicide”, 106-110, Copyright 2013, with permission from Elsevier

ii) uniform supply of magnesium onto the nanowire surfaces is possible when they are in array format as magnesium diffuses not only from the top, but also the sides of the nanowires (Figure 3.1).

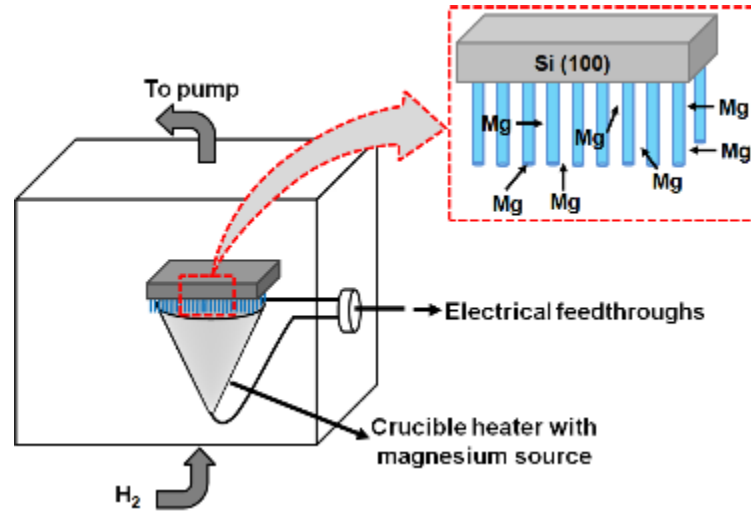


Figure 3.1. A schematic representation of the experimental setup employed for studying the phase transformation of silicon nanowires into Mg₂Si nanowires.

For the synthesis of silicon nanowire arrays, (100)-oriented Si wafers were rinsed with acetone and cleaned using piranha solution (a mixture of 3 parts H₂SO₄ solution (98% w/w) and 1 part H₂O₂ solution (35% w/w) by volume) for 15 minutes. The wafers were then etched with a 1:1 mixture of 0.04M AgNO₃ solution and 5M HF solution by volume at room temperature for 30 minutes. Following the etching, excess silver was removed from the wafers by cleaning them with a 1:1 mixture of HCl solution (33% w/w) and HNO₃ solution (70% w/w) by volume at 100°C for 1 hour. The phase transformation of silicon nanowire arrays was accomplished by reacting them with magnesium supplied via

the vapor phase. Freshly polished magnesium foils served as the source of magnesium in these experiments. These foils were loaded into an alumina coated tungsten crucible heater for the phase transformation experiments. The silicon nanowire array was physically held on the top of this crucible heater, facing the magnesium source, at an approximate distance of 1 cm from the magnesium source (Figure 3.1). In this configuration, the silicon nanowire array was mainly heated by conduction from the crucible heater. The magnesium source was always maintained at a temperature of 400-700 °C. Under the conditions, the temperature the substrate was measured to vary between 350 °C and 400 °C (Figure S2 of supplementary information). All the experiments were performed in the presence of hydrogen at a pressure of 400 mTorr and typically lasted for duration of 4-20 minutes.

3.3 Results and Discussion

3.3.1 Reaction of Silicon Nanowire Arrays with Magnesium

The electroless etching of silicon wafers resulted in the formation of silicon nanowire arrays, as expected (Figures 3.2 (a) and 1(b)). Electron microscopy indicated that the silicon nanowires obtained had diameters in the 20-300 nm range, with an average diameter of 100 nm. Transmission electron microscopy (TEM) of the obtained nanowires indicated that they were single-crystalline in nature, and that their growth direction was either along the [110] (Figure 3.2 (c)) or the [100] (Figure 3.2 (d)) crystal orientation.

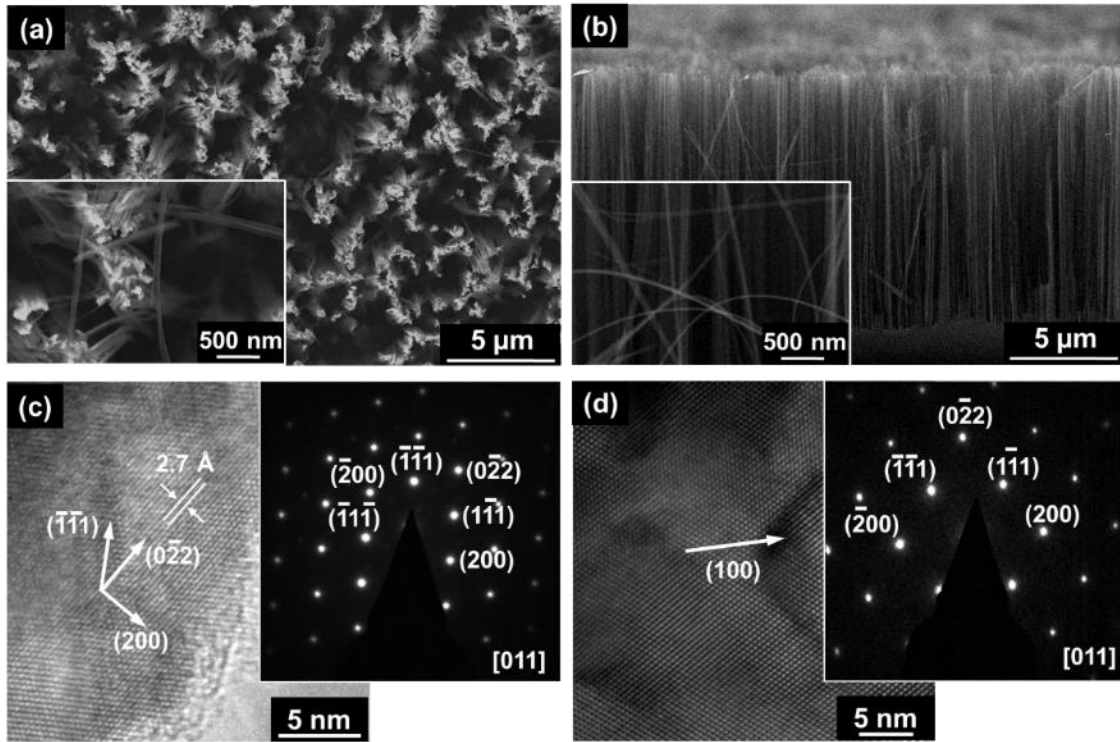


Figure 3.2. Representative scanning electron micrographs showing the top view (a) and cross-sectional view (b) of the silicon nanowire, and high resolution TEM micrograph of a silicon nanowires indicating that they are single-crystalline in nature and exhibit either (c) [110] or (d) [100] growth direction.

The reaction of silicon nanowire arrays with magnesium was performed in a cyclical manner. In a typical reaction cycle lasting for a period of 4 minutes, magnesium was evaporated onto the silicon nanowire array substrates using a source temperature of 700°C and a substrate temperature of 400 °C for the first 1 minute. This step was followed by a 3-minute annealing step where the magnesium source temperature was lowered to 400 °C. This lowered the temperature of the substrate to 350°C (Figure 3.3). This temperature decrease allowed the magnesium to diffuse into the silicon nanowires and react without any significant evaporation from the nanowire surfaces. Phase

transformation experiments lasting for longer duration involved repeating these cycles two, three or five times.

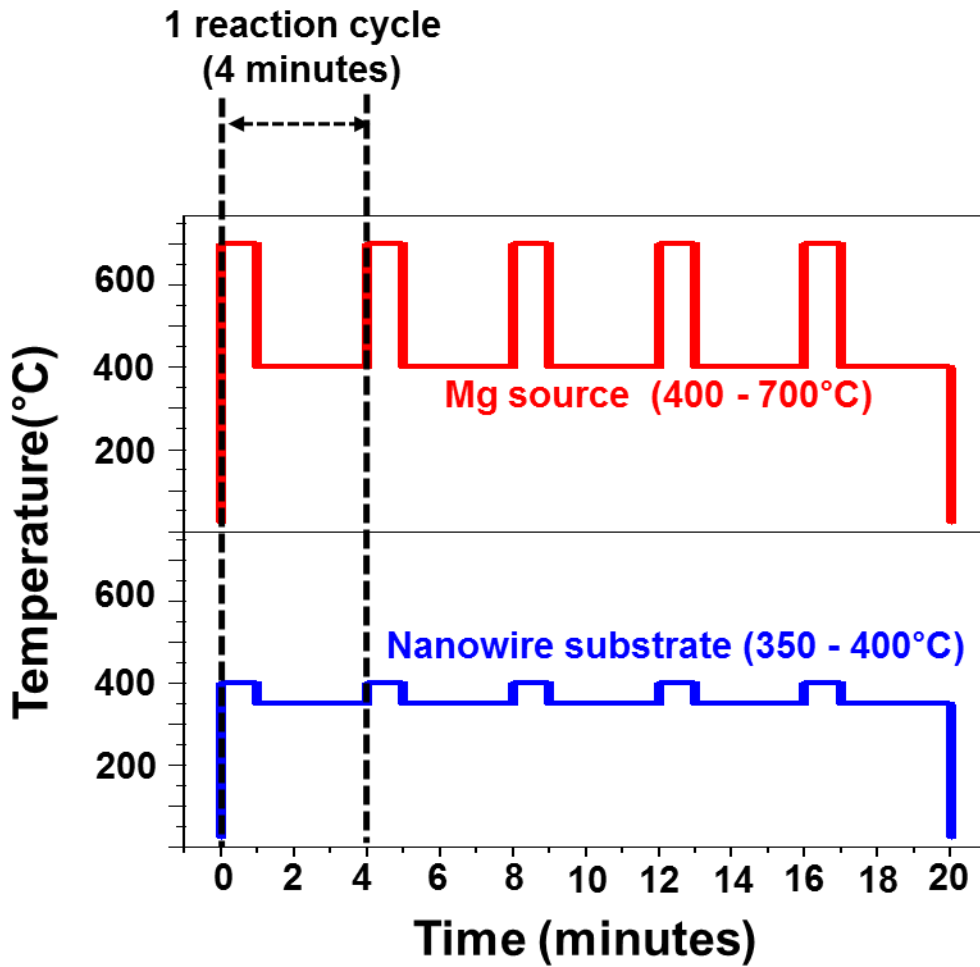


Figure 3.3. Temperature profile of the magnesium source and the substrates employed for the phase transformation of silicon nanowires into Mg_2Si nanowires. The definition of one reaction cycle is also pictorially represented in the figure. One reaction cycle involved heating the magnesium source for one minute at 700 °C, followed by reducing its temperature to 400 °C and holding it there for 3 minutes. The corresponding temperatures of the nanowires substrates were measured to be respectively 400 °C and 350 °C.

3.3.2 Nanowire Characterization

Scanning electron micrographs of the nanowires after reaction with magnesium for one, three and five reaction cycles are presented in Figures 3.4(a) through 3.4(f). As observed in the Figures, no morphology changes were observed in the nanowires after their reaction with magnesium. To confirm that the reaction went to completion, the change in the diameter of the wire before and after phase transformation was monitored. The volume of the nanowire should theoretically increase by 3.4 and the diameter by 1.8 upon a complete transformation assuming no silicon is lost through evaporation and that axial nanowire growth is negligible. A survey of the wires before and after transformation confirmed that this is true.

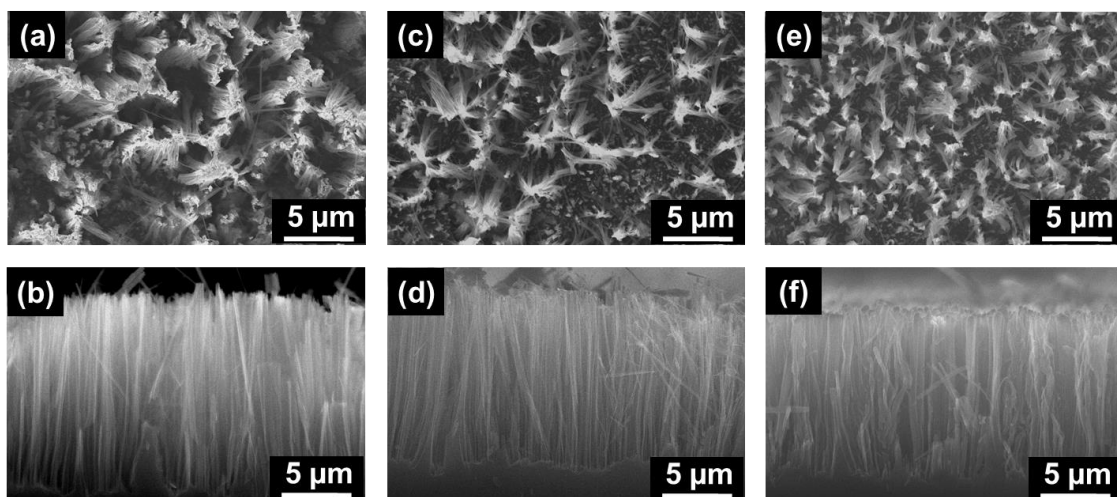


Figure 3.4. (a) and (b) Top view and cross-section view of the silicon nanowires after reaction with magnesium for two reaction cycles. (c) and (d) Top view and cross-section view of the silicon nanowires after reaction with magnesium for three reaction cycles. (e) and (f) Top view and cross-section view of the silicon nanowires after reaction with magnesium for five reaction cycles. No change in the morphology of the nanowires was observed after their reaction with magnesium.

Raman spectroscopy of the samples indicated the formation of Mg₂Si nanowires. Raman spectra of the nanowires (Figure 3.5) indicated the presence of a triply degenerate F_{2g} mode corresponding to Mg₂Si at 258 cm⁻¹.⁹⁷ Another broad peak at 345 cm⁻¹ corresponding to the Fröhlich-interaction-induced Raman-inactive longitudinal optical (LO) mode of Mg₂Si was also observed in the spectra.⁹⁸ The peak at 432 cm⁻¹ is expected to be the result of the interfacial stress arising from the boundaries between Mg₂Si nanowires and the bulk silicon wafer.⁹⁹ Finally, Raman modes at 290 and 519 cm⁻¹ corresponding to the second-order transverse acoustic phonon mode 2TA and F_{2g} of silicon¹⁰⁰ were also observed in Figure 3.5. The intensity of the Mg₂Si peaks relative to the intensity of the silicon peaks increased as the number of reaction cycles increased from one to five due to the reaction going to completion.

X-ray diffraction analysis of the samples (Figure 3.6) confirmed the results observed in the Raman spectroscopy studies and indicated that the relative ratio of Mg₂Si to silicon increased as the number of reaction cycles increased from one to five. The silicon signal still observed in the Raman and XRD analysis of the nanowires after five reaction cycles is believed to be from the unreacted silicon substrate underlying the Mg₂Si nanowires.

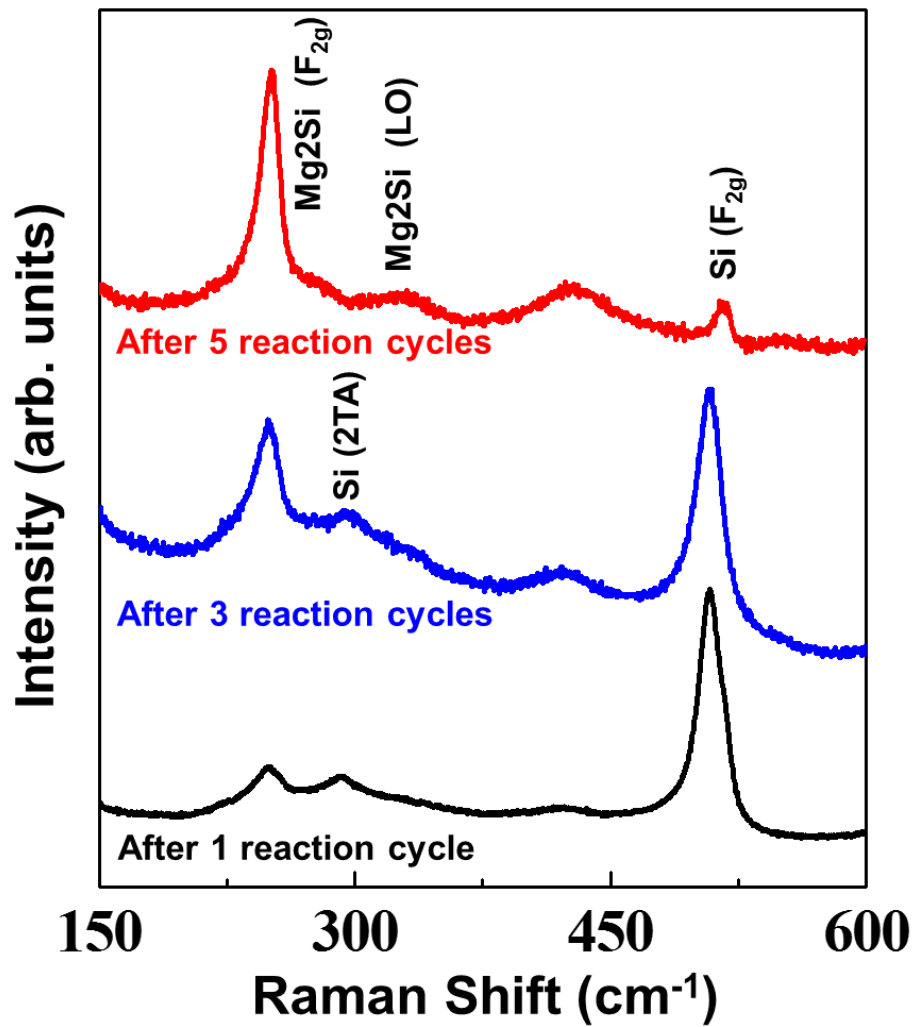


Figure 3.5. Raman spectra of the nanowires after their reaction with magnesium for two, three and five reaction cycles. The amount of Mg₂Si formed was observed to increase with the increase in the number of reaction cycles.

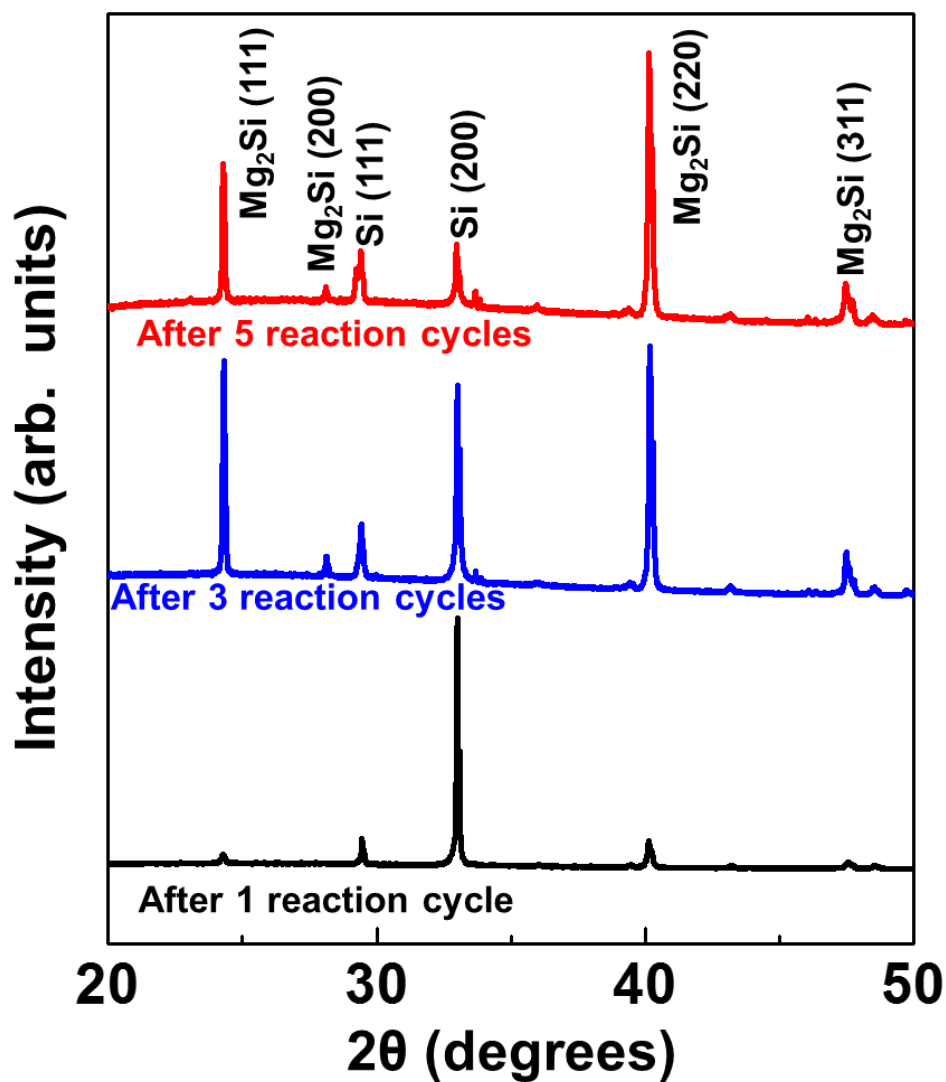


Figure 3.6. XRD spectra of the nanowires after their reaction with magnesium for two, three and five reaction cycles, confirming the enhancement in the amount of Mg₂Si formed as the number of reaction cycles was increased.

TEM analysis of a 200 nm-thick nanowire indicated that the reaction went to completion resulting in the formation of Mg₂Si after five reaction cycles (Figure 3.7). A thin sheath of MgO observed on the nanowire surface is believed to be the result of the reaction of native SiO₂ present on the silicon nanowire surface with magnesium

$(\text{SiO}_2+4\text{Mg}\rightarrow 2\text{MgO}+\text{Mg}_2\text{Si})$.¹⁰¹ The TEM analysis also indicated that the nanowires were polycrystalline in nature (Figure 3.7).

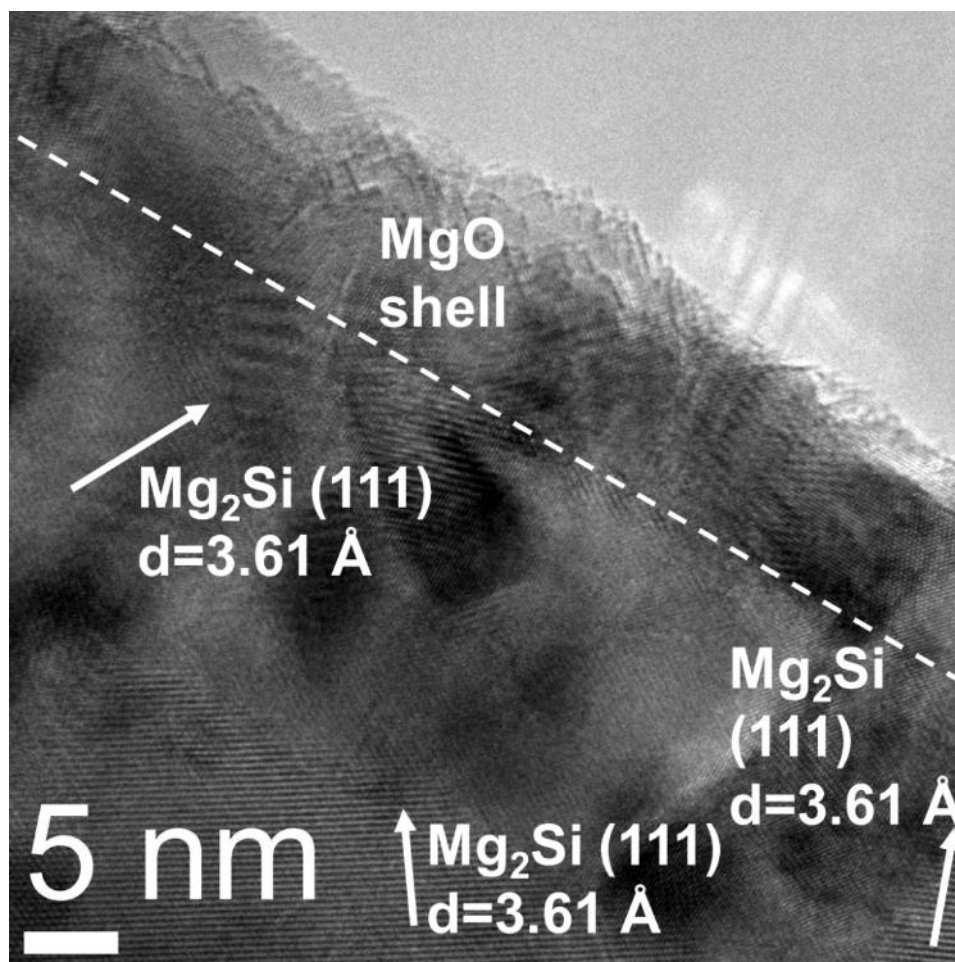


Figure 3.7. High resolution TEM micrograph of the Mg_2Si nanowire formed after the reaction of silicon nanowire with magnesium for five reaction cycles. The data indicated the complete transformation of silicon nanowires into polycrystalline Mg_2Si nanowires.

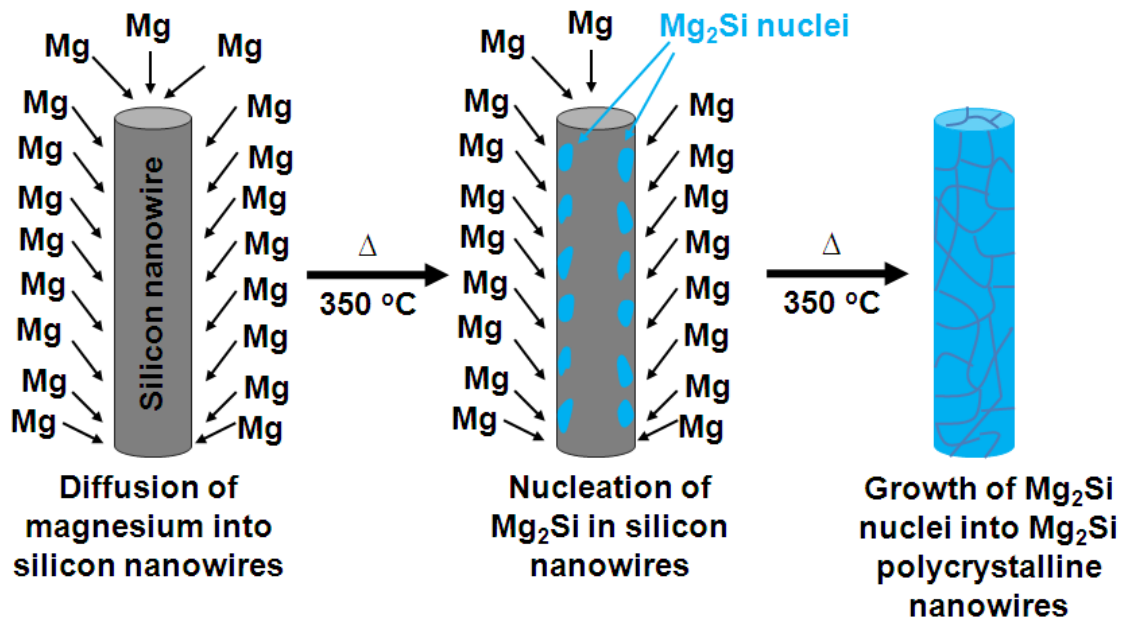


Figure 3.8. A pictorial representation of the nucleation and growth steps proposed to be involved in the phase transformation of silicon nanowires into polycrystalline Mg_2Si nanowires. The diffusion and reaction of magnesium with silicon is expected to first lead to the formation of Mg_2Si nuclei inside the silicon nanowires. The growth of these nuclei as the reaction proceeds leads to the formation of polycrystalline Mg_2Si nanowires.

3.3.3 Phase Transformation Mechanism

From the results discussed above, it can be concluded that the following mechanism is responsible for Mg_2Si nanowire formation. First and foremost, the use of silicon nanowire arrays allowed for the uniform supply of magnesium all along the length of the arrays. The diffusion of magnesium into silicon, its subsequent dissolution in silicon and finally the supersaturation of silicon with magnesium will ultimately lead to the solid-state nucleation of Mg_2Si nuclei inside the surfaces of the nanowires (Figure 3.8). Any additional magnesium supplied via the vapor phase will also eventually diffuse into the nanowire and react with silicon near the surfaces of nuclei, leading to their growth. The

growth of nuclei proceeds until all the silicon converts into Mg_2Si leading to the formation of polycrystalline nanowires (Figure 3.8). Even though both magnesium and silicon can diffuse inside the nanowire during the growth phase, it is well known that the dominant diffusing species is dependent on the final composition of the silicide.^{102, 103} If the final silicide phase is stoichiometrically metal-rich, then the metal is the dominating diffusing species.^{102, 103} Alternately, if the silicide is stoichiometrically silicon-rich, then the dominating diffusion species is silicon.^{102, 103} This implies that magnesium is the dominant diffusing species and diffuses around the nuclei during the growth phase. The rate of supply of magnesium also dictates whether the nanowire morphology is preserved during such transformation. If the rate of supply of magnesium is approximately equal to the total rate at which it is desorbed and consumed for the formation of Mg_2Si , then ultra-thin conformal layers of magnesium can be deposited on nanowire surfaces and their morphologies can be preserved. Pulsing the magnesium for 1 minute followed by reacting/annealing the metal coated nanowires for 3 minutes was utilized to obtain a thin conformal layer of magnesium on the nanowire surfaces.

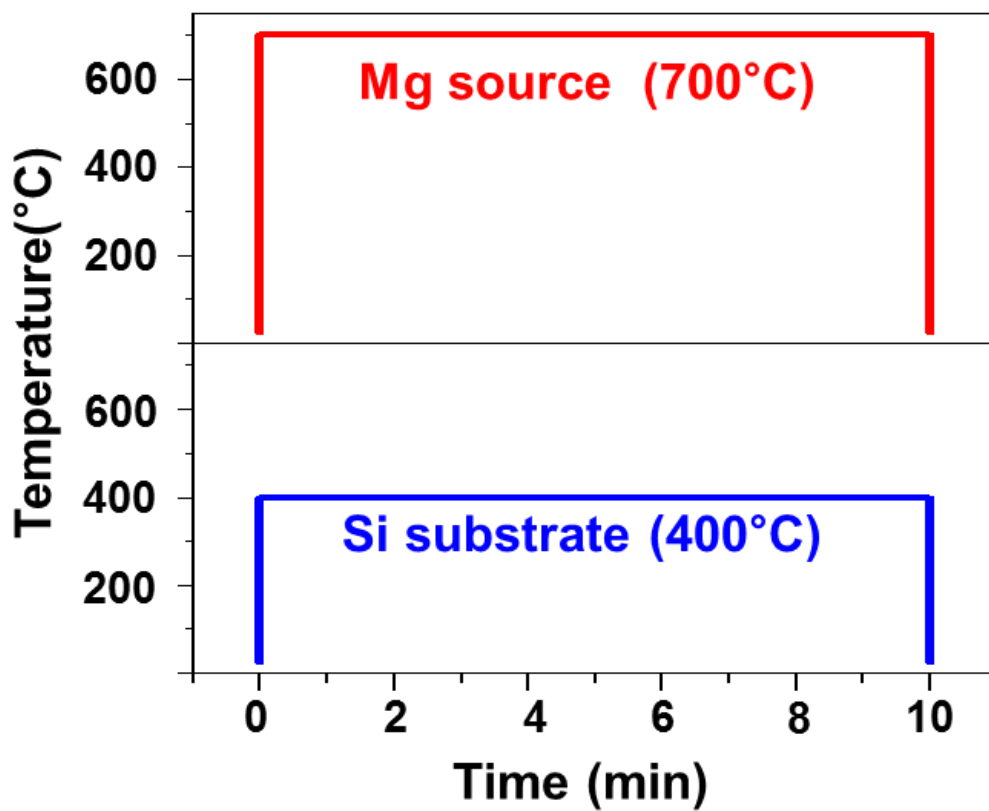


Figure 3.9. Temperature profile of the magnesium source and the substrates employed for the studying the phase transformation of silicon nanowires under prolonged magnesium supply conditions

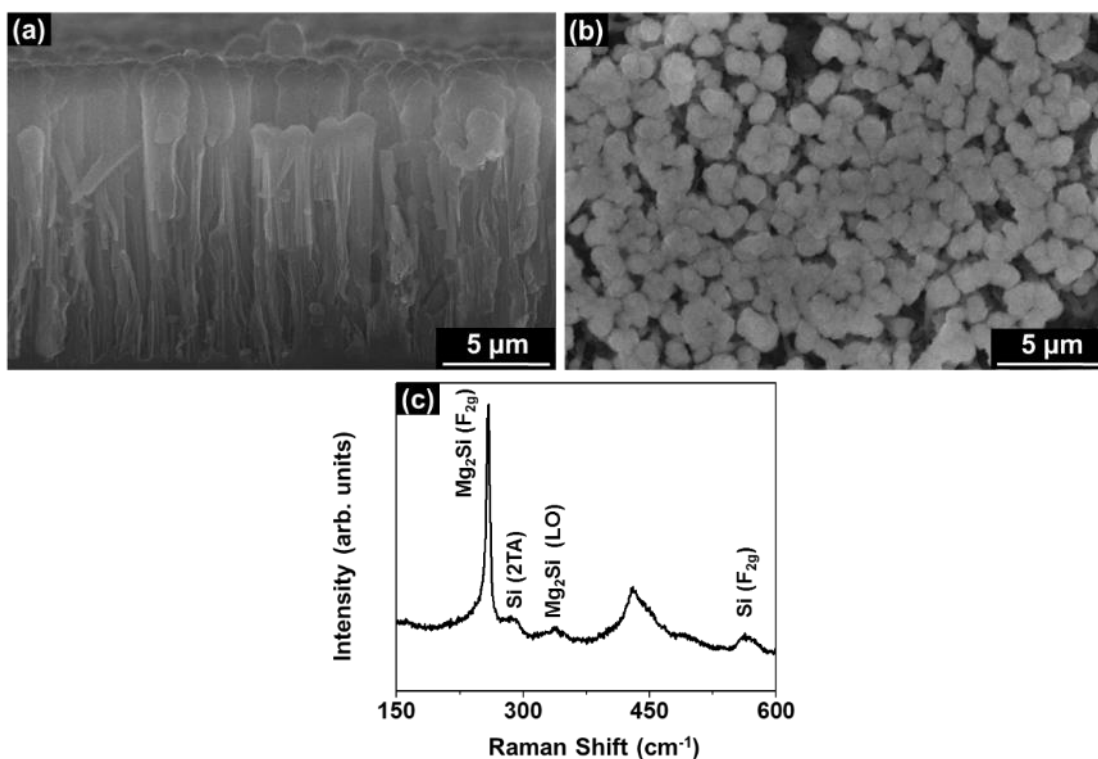


Figure 3.10. (a) and (b) Under prolonged magnesium supply conditions, loss of nanowire morphology was observed. (c) Raman spectroscopy indicated the formation of Mg_2Si phase, although the morphology was lost during the phase transformation.

However, if the rate of supply of magnesium is far higher than the total rate at which it is reacted and desorbed from the surface (Figure 3.9), then a non-conformal layer of magnesium will be formed on top of the nanowires. This non-conformal layer fills the pitch between adjacent nanowires leading to a loss of the nanowire morphology (Figure 3.10), while the thin conformal coating prevents nanowire agglomeration and consequently morphology is conserved.

3.4 Conclusions

In summary, a simple phase transformation strategy for changing the chemical compositions of nanowires without varying their morphologies was presented. The strategy was demonstrated with the phase transformation of silicon nanowires into Mg_2Si nanowires. A pulsed supply of magnesium onto the silicon nanowire arrays followed by an annealing step that allowed the magnesium to diffuse through the nanowires led to the complete phase transformation of the single crystalline silicon nanowires into polycrystalline magnesium silicide nanowires. The use of silicon nanowires in array format for the phase transformation process ensured the conformal coating of magnesium all along the lengths of the nanowires, and hence in their complete phase transformation into Mg_2Si . The ability to phase transform silicon nanowires uniformly allows for the future implementation of this strategy not only in the bulk production of many other metal silicide nanowire powders, but also in the production of efficient and inexpensive thermoelectric modules.

CHAPTER IV

SINGLE-CRYSTALLINE PHASE TRANSFORMATION OF Si NANOWIRES INTO

Mg₂Si NANOWIRES*

4.1 Introduction

In the previous chapter, we have demonstrated that phase transformation of single-crystalline silicon nanowires by reacting them with magnesium supplied via the vapor phase led to the formation polycrystalline Mg₂Si nanowires in that case.¹⁰⁴ Single-crystalline nature of the nanowires offers the possibility of realizing enhanced electrical conductivity.¹⁰⁵ However, No reports on the synthesis of single-crystalline Mg₂Si nanowires exist in the literature. Synthesis of other metal silicide nanowires has been accomplished in the past and reported. These reports include the phase transformation of silicon nanowires into MnSi_{1.75},^{55, 106, 107} CoSi,^{108, 109} GdSi_{1.75},¹¹⁰ NiSi,¹¹¹ NiSi₂¹¹² and PtSi¹¹³ nanowires. In addition, synthesis to the synthesis of PtSi nanowires, PtSi/Si heterojunctions have also been synthesized and reported.¹¹³ Most of these reports relied on the supply of either metal or metal halides through the vapor phase onto pre-synthesized silicon nanowires for their conversion into metal silicide nanowires. A few others relied on the solid-state diffusion of metal into silicon nanowires for the synthesis of metal silicide nanowires.^{111, 113} In this chapter, the aim of this study is that tune the nucleation

* Parts of this chapter are reprinted from *Chemistry of Materials* **2014**, 26, Yongmin Kang, Sreeram Vaddiraju, "Solid-state phase transformation as a route for the simultaneous synthesis and welding of single-crystalline Mg₂Si nanowires", 2814-2819, Copyright 2014, with permission from American Chemical Society

and growth steps involved in the solid-state phase transformation of silicon nanowires and realize single-crystalline Mg_2Si nanowires

4.2 Experimental Methods

Silicon nanowires necessary for the synthesis and welding of Mg_2Si nanowires were obtained using electroless etching (Figure 4.1(a)). This procedure was described in detail previously.^{22, 83, 104} Boron doped $\langle 100 \rangle$ -oriented silicon wafers (obtained from University Wafer) were employed as the raw materials for the synthesis of silicon nanowires. Following the electroless etching, the obtained silicon nanowires were additionally etched using a 3 wt. % KOH aqueous solution for 2 minutes to ensure that they had sharp tips (Figure 4.1 (b)).⁹² The anisotropic etching behavior of (100) Si wafer in KOH solution makes higher etching rate of (100) and (110) planes than (111) plane (Figure 4.2), and it leads to sharp end (3-5 nm) of Si nanowires (Figure 4.1 (b)). The diameters of the nanowires obtained using the electroless etching typically ranged from 50 to 100 nm range, while the lengths ranged from 4.9 to 5.3 μm .

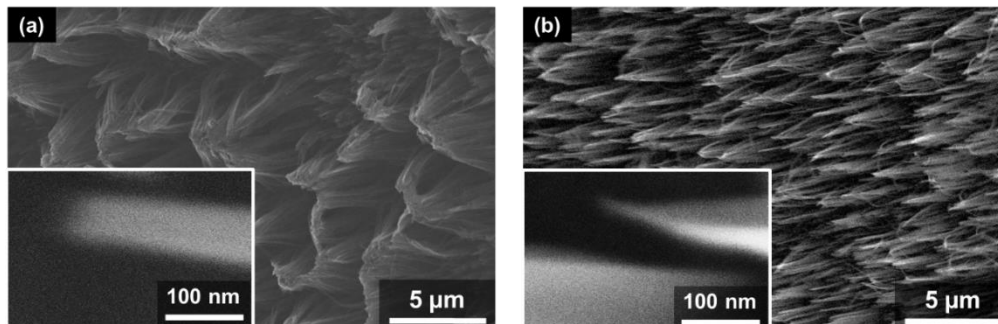


Figure 4.1. Representative SEM images showing (a) Si nanowires synthesized using electroless etching, and (b) additional KOH etched Si nanowires which have sharp end.



Figure 4.2. Schematic illustration of electroless etching of Si wafers using AgNO_3/HF , and KOH solution.

All the phase transformation experiments were performed using a solid-state reaction. Typically, these experiments involved bringing the as-obtained silicon nanowire arrays in contact with a polished magnesium foil, followed by heating them to 350-400 °C in a vacuum chamber (Figure 4.3). Mild manual pressure was employed to ensure a good contact between the nanowires and the foil before the start of the phase transformation experiments. The flexible nature of the polished magnesium foil allowed for the formation of a good contact. A boron nitride ceramic plate weighing 45 grams was placed on top of the silicon nanowires + magnesium foil experimental setup aided in ensuring that this contact remained in place all throughout the phase transformation process (Figure 4.3). These experiments were performed in the presence of hydrogen, and at a pressure of 100 mTorr. The typical duration of these experiments was 20-60 minutes. The lower reaction temperature ensured that the supply of magnesium into silicon nanowires for the formation of Mg_2Si occurred only through solid-state diffusion. No appreciable evaporation of magnesium is expected to occur at these temperatures. Therefore, the supply of magnesium vapor via the vapor phase onto silicon nanowires for the formation of Mg_2Si nanowires is not expected at these low reaction temperatures. For the synthesis of Mg_2Si nanowires, as-obtained silicon nanowires were phase transformed using this solid-state

reaction. The obtained Mg_2Si nanowires were characterized using an array of techniques, including scanning electron microscopy (SEM), transmission electron microscopy (TEM), and X-ray diffractometry (XRD).

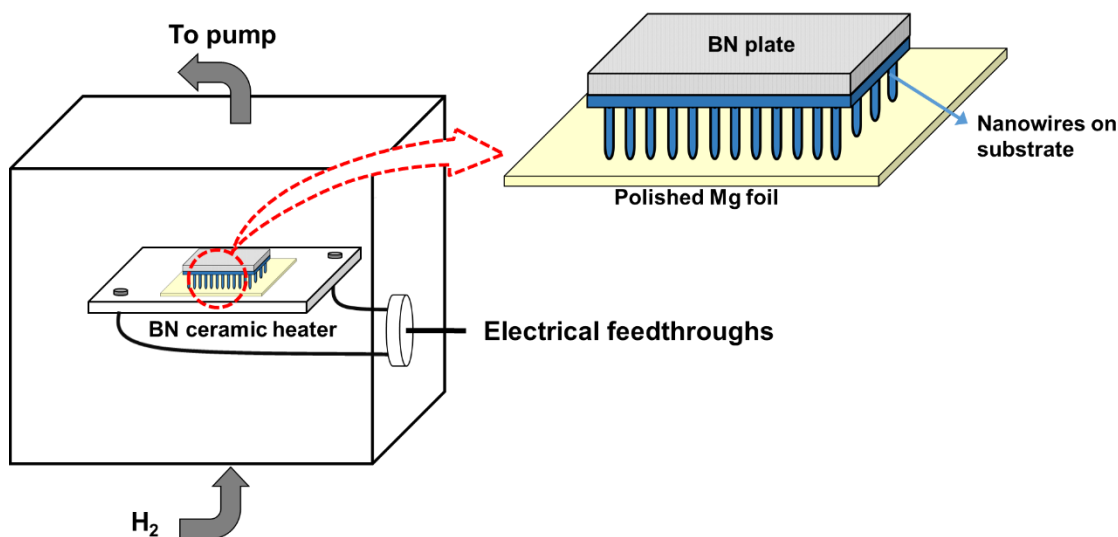


Figure 4.3. A pictorial representation of the reactor used for the simultaneous synthesis and welding of Mg_2Si nanowires. The placement of the magnesium foil relative to the substrate containing the nanowires is also indicated.

4.3. Results and Discussion

4.3.1 Nanowire Characterization

A scanning electron micrograph of an array of as-obtained silicon nanowires is depicted in Figure 4.1. These silicon nanowires had diameters in the range of 50-100 nm. As observed in the figure, the nanowires also had sharp tips (Figure 4.1(b)). A micrograph of these nanowires after solid-state phase transformation into Mg_2Si nanowires is presented in Figure 4.4. As is clearly evident in the figure, the phase transformation allowed for the retention of the nanowire morphology.

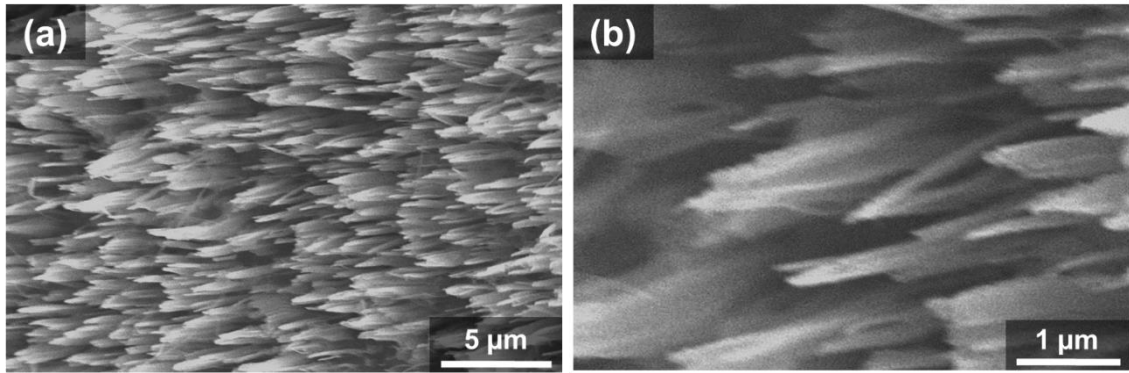


Figure 4.4. Scanning electron microscope images of phase transformed Mg₂Si nanowires

XRD pattern of the silicon nanowires after phase transformation is presented in Figure 4.5. It is clearly evident from the data that the nanowires are composed of only Mg₂Si after phase transformation (cubic crystal structure with a lattice parameter of 0.639 nm).¹¹⁴

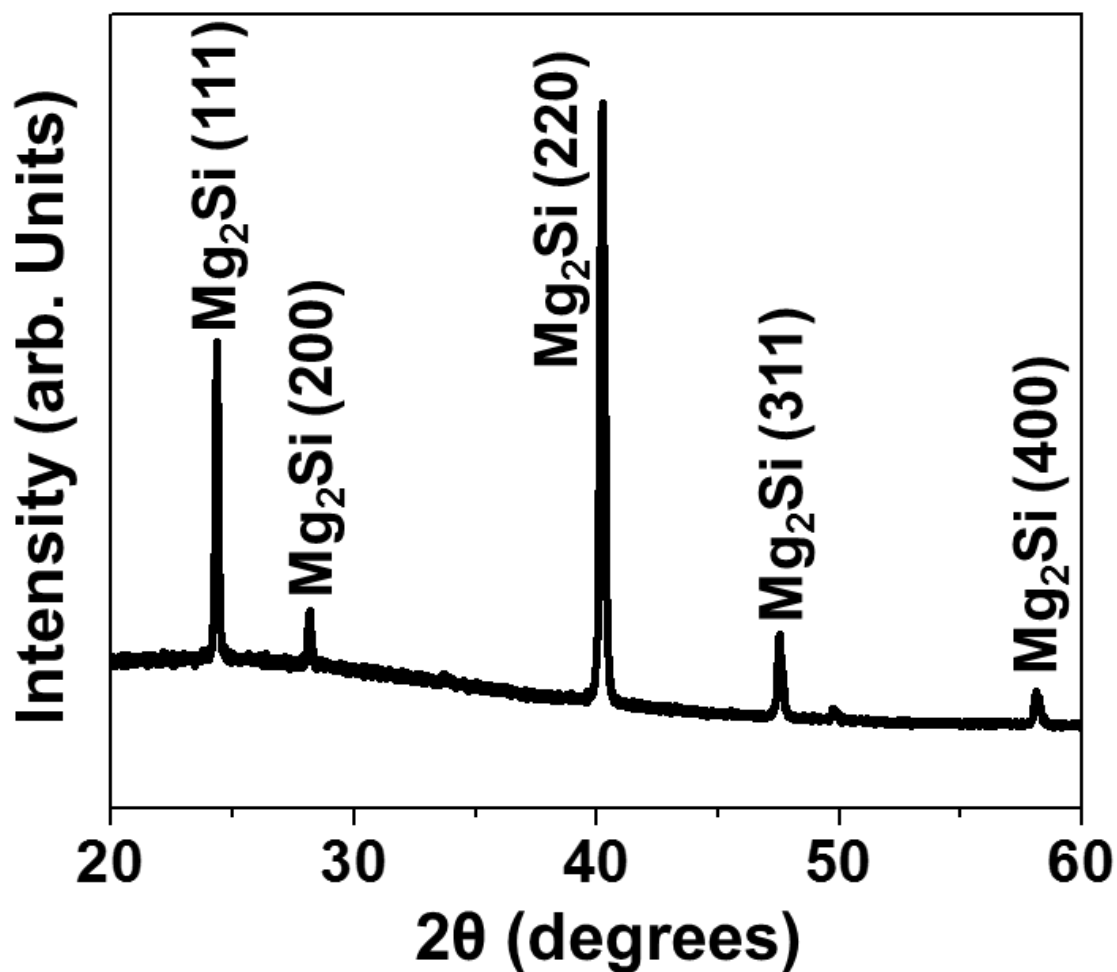


Figure 4.5. XRD pattern of Mg_2Si nanowires obtained by solid-state phase transformation of silicon nanowires

TEM analysis of the phase transformed nanowires was performed to determine whether the Mg_2Si nanowires formed by the phase transformation process are single-crystalline or polycrystalline. The results indicated that the phase transformation of the as-obtained silicon nanowires resulted in the formation of single-crystalline Mg_2Si nanowires (Figure 4.6). The analysis indicated the presence of an MgO sheathe around the Mg_2Si nanowires. Analysis of the diffraction pattern from the Mg_2Si nanowire shown in Figure

4.6 (a) indicated that their growth direction was $[202]$ (inset to Figure 4.6(a)). Also, energy dispersive x-ray spectrometry (EDS) analysis confirmed that the elemental composition consisted of stoichiometry Mg_2Si nanowires (Figure 4.6 (d)).

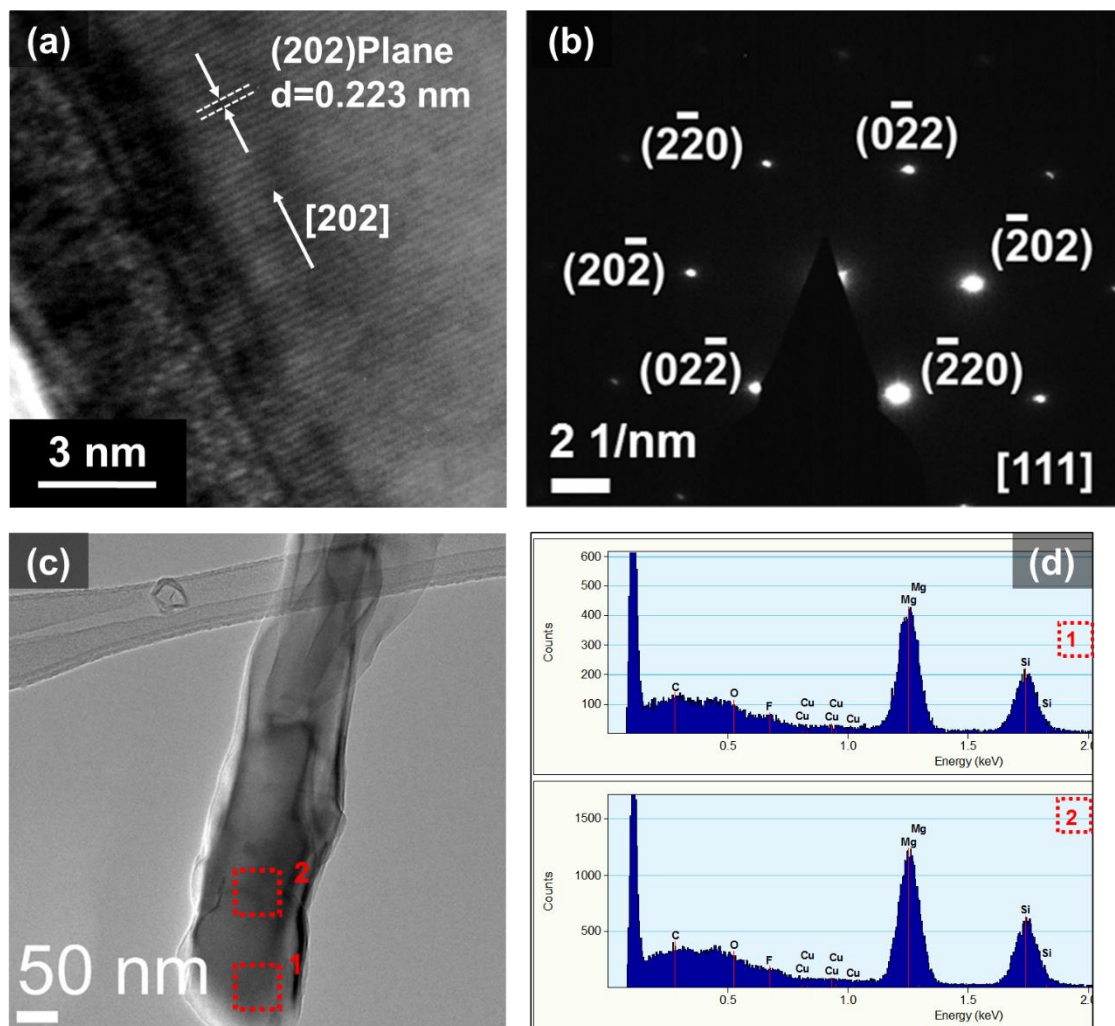


Figure 4.6. (a) High resolution of TEM micrograph of Mg_2Si nanowire indicating $[110]$ growth direction, (c) the image of the nanowire, (b) corresponding selected area electron diffraction (SAED) indicating single-crystalline nanowire and (d) EDS analysis of the Mg_2Si nanowires.

4.3.2 Single-crystalline Phase Transformation Mechanism

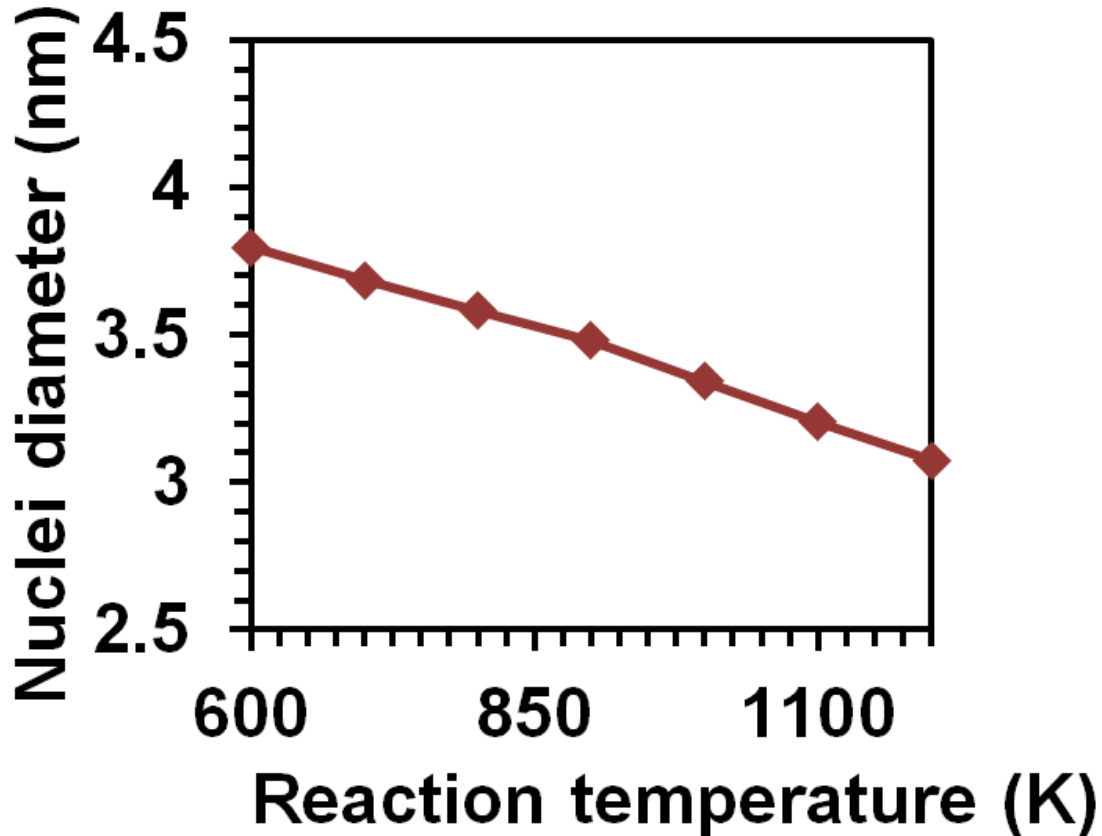


Figure 4.7. An estimate of the variation of the size of the Mg_2Si nuclei formed inside silicon nanowires at various temperatures when they (silicon nanowires) are reacted with magnesium at elevated temperatures.

The formation of single-crystalline Mg_2Si nanowires using phase transformation can be explained using the following mechanisms. Typically, the supply of magnesium through the vapor phase onto silicon nanowires, and the subsequent supersaturation of the nanowires with magnesium leads to the formation of multiple Mg_2Si nuclei inside each nanowire. Further reaction of silicon with additional magnesium diffusing into the nanowires leads to the growth of these nuclei and the formation of polycrystalline Mg_2Si

nanowires.¹⁰⁴ However, tuning the experimental conditions to allow for the formation of only one Mg₂Si nucleus per nanowire should lead to the growth of this nucleus into a single-crystalline Mg₂Si nanowire. The experimental procedure employed in this study allows for this possibility as illustrated in Figure 4(a). Heating the silicon nanowire arrays with sharp tips placed in contact with a magnesium foil leads to the formation of a single nucleus at the tip of each nanowire. The formation of a single Mg₂Si nucleus inside each nanowire can be concurred from the fact that at substrate temperatures in the range of 350-900 °C, Mg₂Si nuclei of sizes in the range of 3-4 nm will be formed. This nuclei size was estimated using nucleation theory as explained below. The critical nuclei size of the second phase (R^*) formed inside a parent phase during phase transformation would be $R^* = 2\gamma/(\Delta G_v + \Delta G_s)$.¹¹⁵⁻¹¹⁷ Here, ΔG_v and ΔG_s are the total volume free energy and the free energy change resulting from strain, respectively, and γ is the surface energy.¹¹⁸ The free energy change resulting from strain (ΔG_s) can be expressed as, $\Delta G_s = 2Y(1 + \nu)\varepsilon^2/(1 - \nu)$.¹¹⁵⁻¹¹⁷ Here, Y is the Young's modulus of the second phase, ν is the Poisson ratio of second phase, and ε is the lattice mismatch between the two phases.¹¹⁵ Estimation of the variation in the size of the Mg₂Si nuclei formed inside Si nanowires with phase transformation temperature indicated that the nuclei size decreases with increase in the phase transformation temperature (Figure 4.7). The following data aided in this estimation: the crystal structures of both Mg₂Si and Si are cubic (lattice parameters are $a=0.639$ nm¹¹⁴ and $a=0.543$ nm),¹¹⁴ $Y_{Mg_2Si}=7.6 \times 10^{10}$ Pa,¹¹⁹ and $\nu_{Mg_2Si}= 0.161$.¹²⁰ Therefore, at substrate temperatures in the range of 350-900 °C, Mg₂Si nuclei of sizes in the range of 3-4 nm will be formed (Figure 4.7). As the nanowire diameters are in the range of 50-100 nm, the

possibility of forming multiple Mg_2Si nuclei inside each nanowire exists in silicon nanowires with uniform diameter all along their lengths. But, in tapered nanowires, the size of the nanowires at the tip is reduced to sizes on the order of the Mg_2Si nuclei size (Figure 4.1 (b) for micrographs of the tips of silicon nanowires before and after KOH etching). This essentially leads to the formation of only one Mg_2Si nucleus per nanowire. The growth of this nucleus into a single-crystalline Mg_2Si nanowire proceeds via the reaction of silicon of the nanowire with additional magnesium diffusing through it.

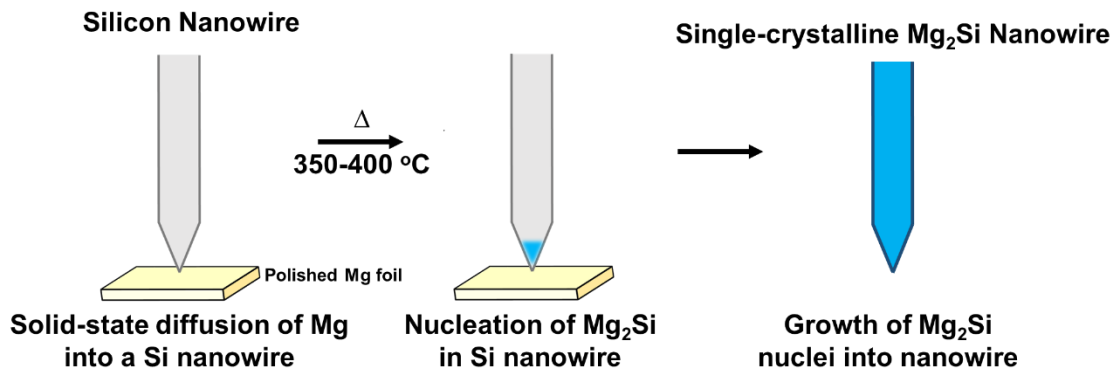


Figure 4.8. A schematic representing the steps involved in the solid-state phase transformation of single-crystalline silicon nanowires into single-crystalline Mg_2Si nanowires. The sharp tips of the silicon nanowires allow for the formation of a single nucleus within each nanowire when they are brought in contact with a magnesium foil and heated. The growth of this lone nucleus within each nanowire leads to the formation of single-crystalline Mg_2Si nanowires

4.4 Conclusions

In summary, a simple solid-state phase transformation strategy for the synthesis of Mg_2Si nanowires was presented. In this strategy, pre-synthesized silicon nanowires, obtained by electroless etching, were phase transformed into single-crystalline Mg_2Si

nanowires. To circumvent the formation of multiple Mg_2Si nuclei within each nanowire and the formation of polycrystalline Mg_2Si nanowires, solid state reaction of sharp silicon nanowires with magnesium foils was employed. The supersaturation of the sharp tips of the silicon nanowires with the diffusing magnesium led to the formation of a single nucleus within each nanowire. The growth of this single nucleus within each nanowire led to the formation of single-crystalline Mg_2Si nanowires.

CHAPTER V

Mg₂Si NANOWIRE ASSEMBLY AND WELDING VIA SOLID-STATE DIFFUSION*

5.1 Introduction

In the field of thermoelectric engineering, nanowire structured morphology is the one of the most promising component because of their geometrical efficiency in electronic and thermal transport.^{7, 8} However, there are still several obstacles against fully use of the unique properties of nanowires, for example, assembled nanowires are loosely connected to each other without stable electrical path between nanowires, and the morphology of nanowires are changed during the assembly. Various nanowire joining methods such as welding, soldering and mechanical bonding (table 5.1) are being reported for the nanowires assembly in optoelectronics,^{121, 122} photonics,^{123, 124} and nanoelectromechanical systems.^{125, 126}

For example, fusion welding of nanowires is a process that including formation of liquid phase at the nanowire interface by Joule heating, electron induced local heating, or direct heating, then solidification of the interface. Unlike the fusing welding, soldering of nanowire includes foreign solder materials which have good electrical conductivity and low melting point to join nanowires. However, these kinds of conventional joining techniques are not adequate for nanowire-based thermoelectric device applications.

* Parts of this chapter are reprinted from *Chemistry of Materials* **2014**, 26, Yongmin Kang, Sreeram Vaddiraju, "Solid-state phase transformation as a route for the simultaneous synthesis and welding of single-crystalline Mg₂Si nanowires", 2814-2819, Copyright 2014, with permission from American Chemical Society

Table 5.1. Nanowire joining methods

Joining Methods		Advantages	Limitation
Welding	Fusion Welding	No contamination or impurity	Rely on advanced equipment Low efficiency Material deformation
	Solid state welding	Single-crystalline welding	
Soldering	Nanowire solder	Robust interconnect Good thermal and electrical conductivity	Surface oxidation High temperature process
	Pre-coated solder layer		
Mechanical bonding	Hot pressing	Large-area fabrication	May damage the sample

The fusion welding of nanowires is required high temperature heating process to melt joining part, and it can lead to formation of oxide on nanowire surface and only limited to gold, silver, and platinum nanowires. Because of MgO layer on Mg₂Si nanowire surface, the nanowires surface have to be heat more than 1000°C to form liquid phase on the interface, and it will lead to not only oxidation of surface, but also decomposition of Mg₂Si nanowires during the fusion welding. And MgO interface welding of Mg₂Si nanowires will insulates electric flow. For the soldering, the soldering materials composed of metals such as indium, tin, gold, and silver, and they are easy to diffuse into semiconducting nanowire materials on heating. During the thermoelectric heating and cooling cycles, the materials can act as unintentional dopants on the nanowires and lead to change in thermoelectric performance. Also these techniques can be employed only local area of nanowire, and they rely on advanced equipment. If the welding materials has

same composition of the nanowire materials with stable electrical conduction path, it will be an ideal way for nanowire welding.

In this chapter, the aim of this study is extension the solid-state phase transformation strategy for the simultaneous synthesis and welding of Mg_2Si nanowires. By the end of this chapter, it was demonstrated that solid-state phase transformation (i.e., reaction of magnesium with silicon or SiO_2) can be employed for the simultaneous formation and welding of single-crystalline Mg_2Si nanowires. More specifically, the welding of Mg_2Si nanowires through the formation of Mg_2Si bridges between them will be demonstrated. Finally, the effect of this welding process on the electrical properties of Mg_2Si nanowire assemblies will be discussed.

5.2 Experimental Methods

Silicon nanowires necessary for the synthesis and welding of Mg_2Si nanowires were obtained using electroless etching. This procedure was described in detail in the Chapter II and IV. Boron doped $\langle 100 \rangle$ -oriented silicon wafers (obtained from University Wafer) were employed as the raw materials for the synthesis of silicon nanowires. Following the electroless etching, the obtained silicon nanowires were additionally etched using a 3 wt. % KOH aqueous solution for 2 minutes to ensure that they had sharp tips.⁹² The diameters of the nanowires obtained using the electroless etching typically ranged from 50 to 100 nm range, while the lengths ranged from 4.9 to 5.3 μm . All the phase transformation experiments were performed using a solid-state reaction. Typically, these experiments involved bringing the as-obtained silicon nanowire arrays/silica nanoparticle

decorated silicon nanowire arrays in contact with a polished magnesium foil, followed by heating them to 350-400 °C in a vacuum chamber. Mild manual pressure was employed to ensure a good contact between the nanowires and the foil before the start of the phase transformation experiments. The flexible nature of the polished magnesium foil allowed for the formation of a good contact. A boron nitride ceramic plate weighing 45 grams was placed on top of the silicon nanowires + magnesium foil experimental setup aided in ensuring that this contact remained in place all throughout the phase transformation process (Figure 4.3 in Chapter IV). These experiments were performed in the presence of hydrogen, and at a pressure of 100 mTorr. The typical duration of these experiments was 20-60 minutes. The lower reaction temperature ensured that the supply of magnesium into silicon nanowires for the formation of Mg₂Si occurred only through solid-state diffusion. No appreciable evaporation of magnesium is expected to occur at these temperatures. Therefore, the supply of magnesium vapor via the vapor phase onto silicon nanowires for the formation of Mg₂Si nanowires is not expected at these low reaction temperatures. For the synthesis of Mg₂Si nanowires, as-obtained silicon nanowires were phase transformed using this solid-state reaction.

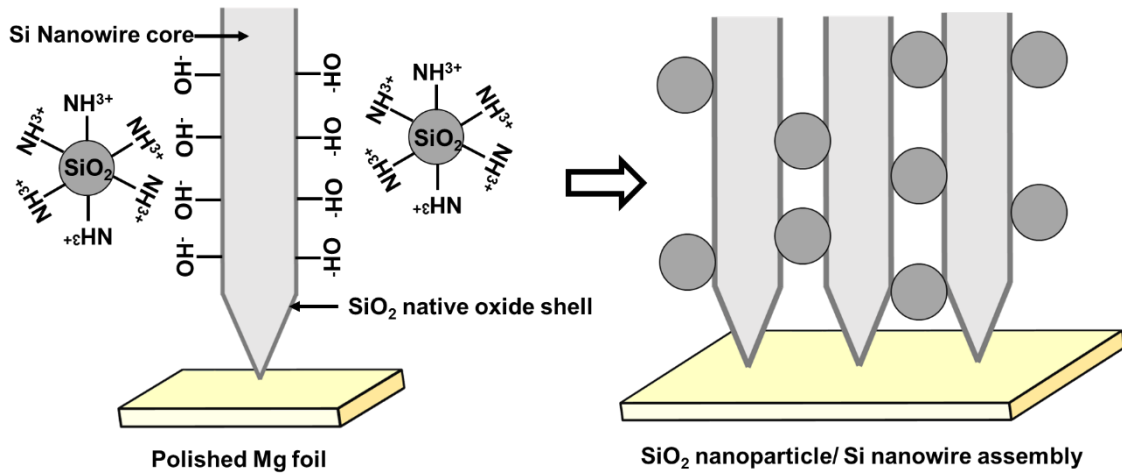


Figure 5.1. A pictorial representation of silica nanoparticle decoration on silicon nanowire surface. Electrostatic attraction between the NH_3^+ end groups on top of the silica nanoparticles and OH^- groups on top of the silicon nanowires leads to the formation of silica nanoparticle decorated silicon nanowires

For welding the obtained nanowires and realizing Mg_2Si nanowires welded together with Mg_2Si bridges between them, phase transformation of silica nanoparticle decorated silicon nanowires was employed. Silica nanoparticle decorated silicon nanowires necessary for this purpose were obtained using the following procedure. Silicon nanowires were first exposed to oxygen plasma for 5 minutes for the formation of $-\text{OH}$ groups on their surfaces. The silicon nanowire arrays were then dipped in a dilute solution of (3-aminopropyl)trimethoxysilane functionalized silica nanoparticle dispersion in water for a duration of 10 minutes. Electrostatic attraction between the NH_3^+ end groups on top of the silica nanoparticles and OH^- groups on top of the silicon nanowires leads to the formation of silica nanoparticle decorated silicon nanowires (Figure 5.1).¹²⁷ The nanowires were then cleaned with excess deionized (DI) water to remove excess silica nanoparticles. The silica nanoparticles used in these experiments had an average diameter

of 200 nm, sufficient enough to bridge the gap (or pitch) between two adjacent silicon nanowires in the array. These silica nanoparticle coated silicon nanowires were also phase transformed using the same procedure described above. The obtained Mg_2Si nanowires were characterized using an array of techniques, including scanning electron microscopy (SEM), transmission electron microscopy (TEM), and X-ray diffractometry (XRD).

For the measurement of the electrical conductivities of the nanowires, they were scraped off the wafers onto pyrolytic BN substrates in the form of mats. Silver paste was employed to make 4 contacts to each nanowire mat. The electrical conductivities of these mats were then measured using 4-point probe method. These measurements were performed in vacuum at temperatures in the range of 325-625 K. Thickness of the nanowire mats necessary for the determination of the electrical conductivities were measured using profilometry, and confirmed using electron microscopy measurements.

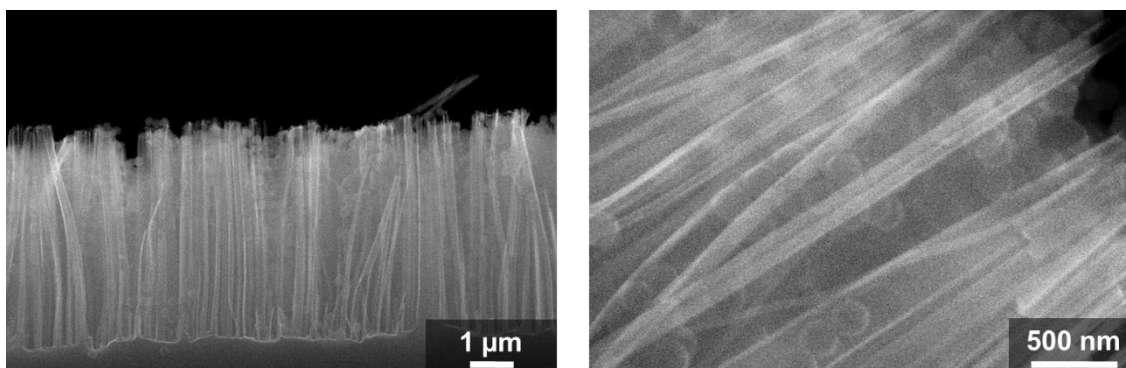


Figure 5.2. Scanning electron micrographs of an array of as-obtained silica nanoparticle decorated silicon nanowires

5.3. Results and Discussion

5.3.1 Nanowire Welding Characterization

SEM images of an array of as-obtained silica nanoparticle decorated silicon nanowires is depicted in Figure 5.2. These silicon nanowires had diameters in the range of 50-100 nm. The silicon nanowires also had sharp tips and the phase transformation of silicon nanowire into single-crystalline Mg_2Si nanowire allowed for the retention of the nanowire morphology (Chapter IV). Scanning electron micrographs of these nanowires after phase transformation is presented in Figure 5.3. Similar to the case of silicon nanowires, the nanowire morphology was still retained after phase transformation. The spherical bridges between the nanowires are also clearly observed after phase transformation.

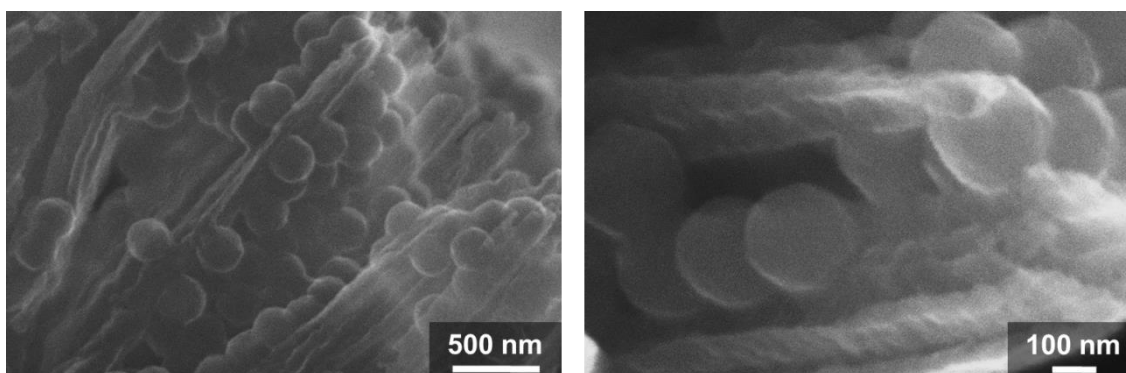


Figure 5.3. Scanning electron micrographs of welded nanowires after phase transformation

XRD pattern of the silica nanoparticle decorated silicon nanowires after phase transformation is presented in Figure 5.4. This result clearly indicated the complete transformation of silica nanoparticle decorated silicon nanowires into Mg_2Si nanowires.

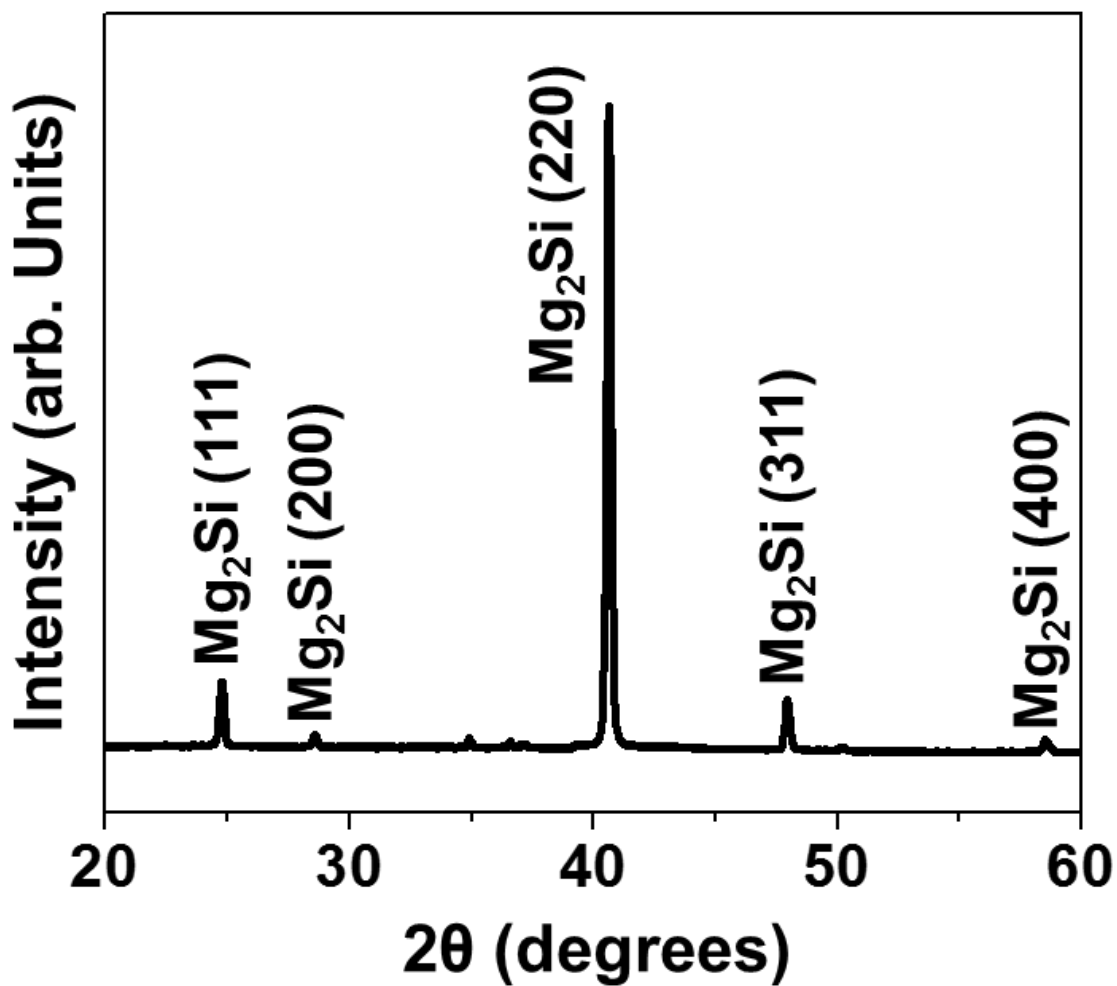


Figure 5.4. XRD pattern of the silica nanoparticle decorated silicon nanowires after phase transformation

TEM analysis of the phase transformed nanowires was performed to determine not only whether the Mg_2Si nanowires formed by the phase transformation process are single-crystalline or polycrystalline, but also whether the Mg_2Si bridges formed between the nanowires ensure the formation of an oxide-free path (i.e., devoid of MgO) for electrical conduction between them. The results indicated that the phase transformation of the as-obtained silicon nanowires resulted in the formation of single-crystalline Mg_2Si

nanowires (Figure 5.5(a)). The analysis indicated the presence of an MgO sheathe around the Mg₂Si nanowires. Analysis of the diffraction pattern from the Mg₂Si nanowire shown in Figure 3(a) indicated that their growth direction was [202] (inset to Figure 3(a)). TEM analysis of welded nanowires indicated that post phase transformation they are composed of Mg₂Si nanowires welded together via Mg₂Si bridges (Figures 5.5 (b) to (d)). The phase transformation led to the formation of a single-crystalline Mg₂Si bridge between adjacent single-crystalline Mg₂Si nanowires, and that the bridge is devoid of the presence of any electrically-insulating MgO. This result (Figures 5.5 (b) to (d)), in conjunction with the fact that the phase transformation of only silicon nanowires led to the formation of Mg₂Si nanowires (Figure 5.5(a)), clearly indicated that the presence of silica nanoparticle between the silicon nanowires is essential for the formation of Mg₂Si bridges between the nanowires.

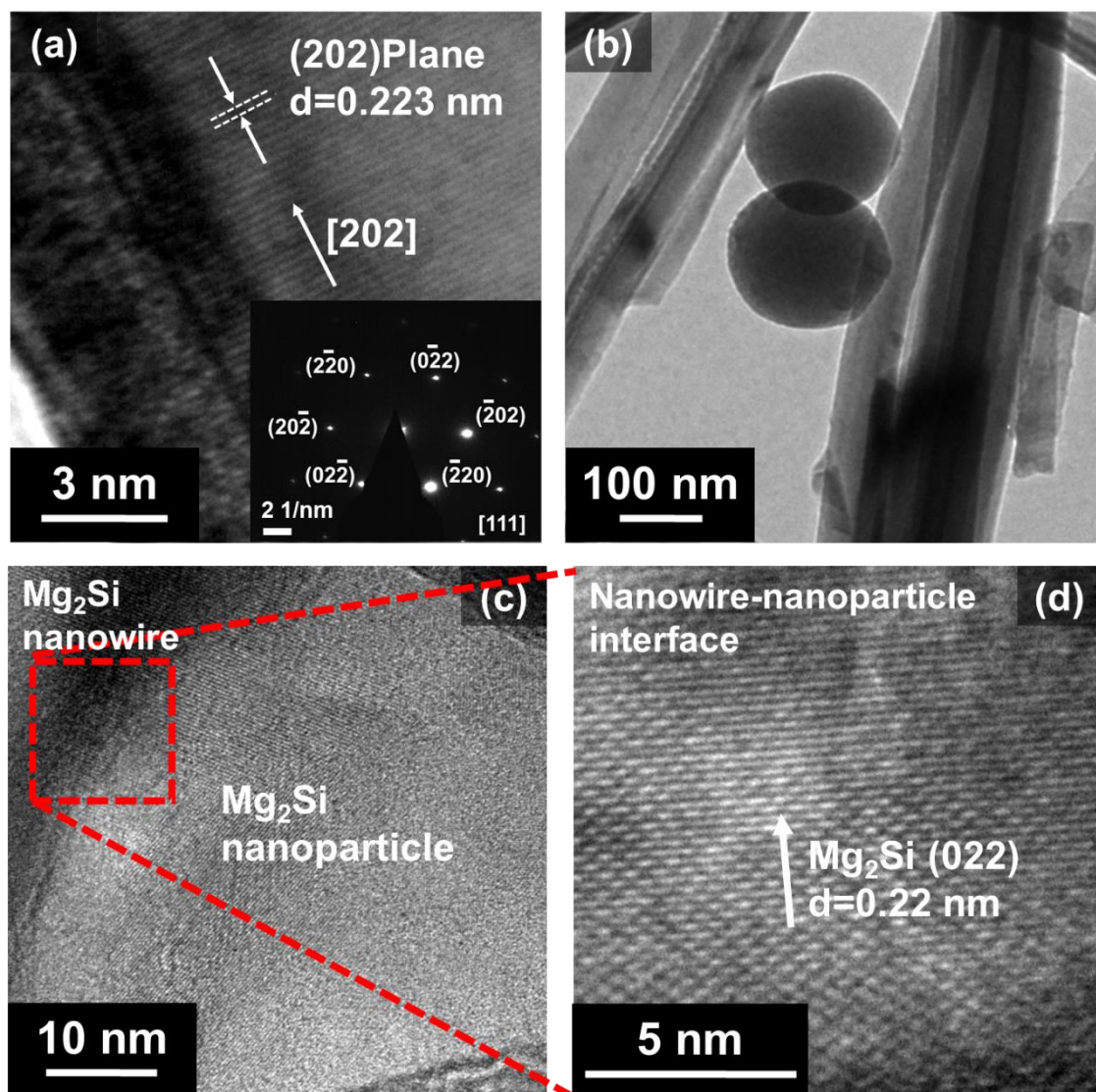


Figure 5.5. (a) A HRTEM image and the corresponding SAED pattern of a single-crystalline Mg₂Si nanowires obtained by solid-state phase transformation of silicon nanowires with sharp tips. (b) to (d) Representative TEM micrographs of welded Mg₂Si nanowires obtained by solid-state phase transformation of silica nanoparticle coated silicon nanowires. As is observed in the images, this procedure led to the seamless welding of Mg₂Si nanowires. The formation of Mg₂Si bridges between the nanowires after welding was clearly observed in the high-resolution TEM image provided in (d). No MgO phase was observed at the interface between the welded nanowires.

5.3.2 Nanowire Welding Mechanism

Formation of single-crystalline Mg_2Si nanowires using solid-state phase transformation was discussed detail in the Chapter IV. The growth step involved in the growth of Mg_2Si nuclei into single-crystalline Mg_2Si nanowires also explains the phenomenon of nanowire welding.

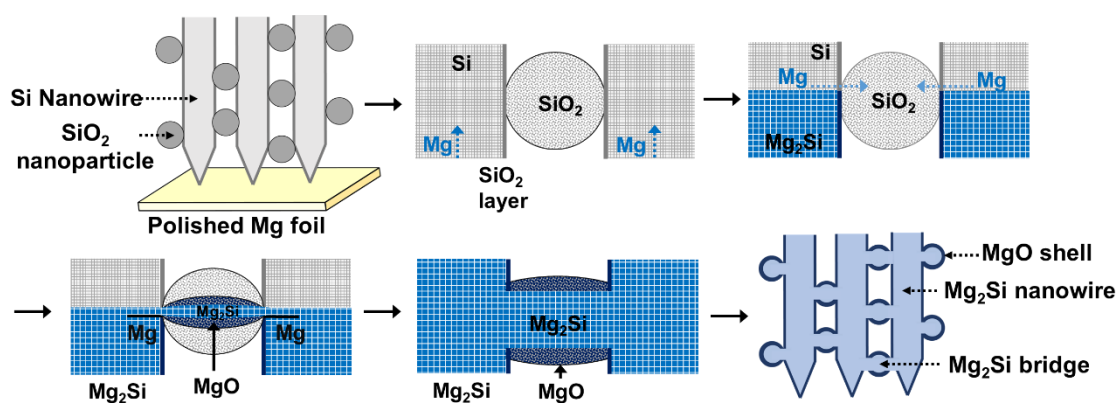


Figure 5.6. Schematic representation of the steps involved in the solid-state phase transformation process for obtaining Mg_2Si nanowires welded via the formation of Mg_2Si bridges. The path for the diffusion of Mg is through the Mg_2Si first and then through the silica nanoparticles bridging them. As magnesium diffuses through the silica nanoparticle, it reacts with it and forms an Mg_2Si bridge between two adjacent Mg_2Si nanowires.

As depicted above in Figure 5.5, on addition of silica nanoparticles to the silicon nanowires, the phase transformation leads to the formation of Mg_2Si nanowires with Mg_2Si bridges between them. The mechanism underlying this phenomenon is pictorially depicted in Figure 5.6. It is well-known that reaction of Mg with silica leads to the formation of Mg_2Si and MgO, according to the following reaction: $4\text{Mg} + \text{SiO}_2 \rightarrow \text{Mg}_2\text{Si} + 2\text{MgO}$.^{101, 128, 129} Although previous studies have indicated that at the micro-scale this reaction leads to the formation of alternating layers of Mg_2Si and MgO,^{101, 128} TEM

analyses of the structures reveal randomly distribution of MgO and Mg₂Si within a region at nanoscale.¹²⁹ The diffusion of magnesium and its reaction with SiO₂ is responsible for the formation of Mg₂Si and MgO. Previous studies have indicated that the diffusion of magnesium occurs preferentially through the Mg₂Si phase, and not the MgO phase.¹⁰¹ Therefore, if silicon nanowires bridged together with silica nanoparticles are brought in contact with a magnesium foil and heated (Figure 5.5), the formation of a lone Mg₂Si nucleus inside and its growth leads to the formation of Mg₂Si nanowires (Figure 4.8 in Chapter IV). Any additional magnesium diffusing through the Mg₂Si nanowires diffuses through the silica nanoparticles bridging them and leads to the formation of an Mg₂Si bridge between the nanowires. Had the reaction of magnesium with silica nanoparticles led to the formation of Mg₂Si/MgO core/shell nanoparticle, no further diffusion of magnesium occurs and the reaction would not reach completion.

5.3.3 Electrical Property of Welded Nanowires

Further confirmation of the formation of Mg₂Si nanowires bridged together with Mg₂Si bridges comes from electrical conductivity measurements. The electrical conductivities of both mats of Mg₂Si nanowires and mats of Mg₂Si nanowires welded together via Mg₂Si bridges were measured and presented in Figure 5.7. As expected, both the Mg₂Si nanowire mats and welded Mg₂Si nanowire mats exhibited semiconducting behavior. Their conductivities increased exponentially with temperature. However, the electrical conductivities of the welded Mg₂Si nanowire mats were observed to be two orders of magnitude higher than the bare Mg₂Si nanowire mats that are not welded.

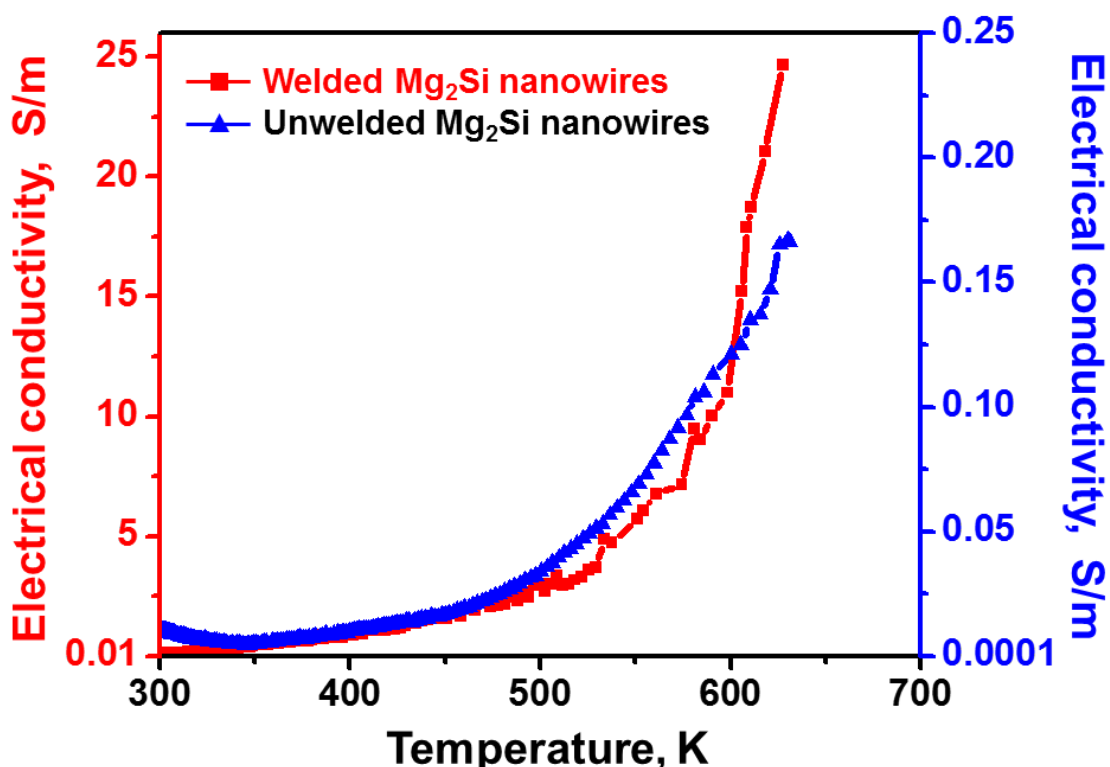


Figure 5.7. A plot comparing the variation of the electrical conductivities with temperature of both non-welded Mg₂Si nanowires and welded Mg₂Si nanowires. The process of welding enhanced the electrical conductivity of Mg₂Si nanowires by approximately two orders of magnitude.

The enhanced electrical conductivity in the welded nanowire mats cannot be attributed to density changes owed to the addition of silica nanoparticles. This is because only a mere 1 wt. % silica nanoparticles were added to the silicon nanowires to weld them using phase transformation. The higher conductivities of the welded Mg₂Si nanowire mat, compared to the bare Mg₂Si nanowire mats, is therefore believed to be the result of the absence of insulating MgO layers at the interfaces between welded Mg₂Si nanowires. Still, the electrical conductivities of welded Mg₂Si nanowire mats (25 S/m at 625 K) were observed to be lower than those reported for bulk Mg₂Si (850 S/m at 623 K).^{44, 45} This is

believed to be the result of the higher porous nature of the welded nanowire mats employed in this study. It is well known that the porosity of nanomaterial assemblies impacts their electrical conductivities.¹³⁰

5.4 Conclusions

In this chapter, solid-state phase transformation strategy for the synthesis and assembly via welding of Mg_2Si nanowires was presented. The phase transformation strategy was extended for phase transforming silica nanoparticle bridged silicon nanowires into Mg_2Si nanowires welded together with Mg_2Si bridges. It is believed that the magnesium diffusing through the silicon nanowires first and then the silica nanoparticle bridging the nanowires reacts with them and leaves an Mg_2Si path between the nanowires, thereby welding them together. In the absence of silica nanoparticles, no welding of the nanowires was observed. The formation of Mg_2Si bridges between Mg_2Si nanowires was further confirmed by the electrical conductivity measurements. Welded nanowires assemblies exhibited conductivities two orders of magnitude higher than those exhibited by non-welded nanowires. This strategy is simple and extendable for obtaining welded nanowires assemblies of many other metal silicides, in addition to Mg_2Si .

CHAPTER VI
FABRICATION OF BULK THERMOELECTRIC DEVICES FROM WELDED Mg₂Si
NANOWIRE ASSEMBLIES

6.1 Introduction

Recent theoretical and experimental studies indicated that nanostructuring of materials is a possible pathway for enhancing their thermoelectric performances, which are determined using figure of merit, zT ($zT = S^2 \sigma T / (\kappa_e + \kappa_l)$). These groundbreaking studies showed that tailor-synthesized materials in nanostructured form are useful for selectively reducing their κ_l and enhancing their thermoelectric efficiencies. For instance, it was demonstrated that individual silicon,^{94, 131} and InSb^{132, 133} nanowires exhibit enhanced thermoelectric performance relative to their bulk counterparts. While these studies provide a pathway for enhancing the thermoelectric performance of small quantities of materials (e.g., an individual nanowire), they do not describe pathways for extending this enhanced performance to bulk devices composed of large quantities of the desired materials (e.g., nanowire pellets). Therefore, the need of the hour is strategies for the mass production and assembly of nanowires that aid in extending the enhanced thermoelectric performance observed in individual nanowires to bulk devices composed of multiple nanowires. Particularly important in the development of strategies for assembling nanowires is ensuring that the thermal and electrical properties of the interfaces between the nanowires, after assembly, are in the least the same as those of the nanowires themselves. In an ideal scenario, this could be accomplished by welding individual nanowire during assembly and

ensuring that the chemical composition of the welds at the nanowire interfaces is the same as that of the nanowires.¹³⁴ Strategies for obtaining such welded compound semiconductor nanowire network assemblies do not currently exist. The current assembly strategies for consolidating nanocrystalline semiconductors lead to the formation of electrically-insulating oxide interfaces between them after consolidation (e.g., interfaces composed of electrically-insulating MgO are formed when nanocrystalline Mg₂Si is assembled). Furthermore, these differences in the chemical compositions of the cores and the surfaces of the nanocrystals composing a thermoelectric device make them expand unevenly on heating, introduce mechanical cracks in the devices, and degrade their thermoelectric performance.¹³⁵

In Chapters III and IV, I demonstrate a phase transformation technique that can be employed not only for converting silicon nanowires into polycrystalline¹⁰⁴ or single-crystalline nanowires,¹³⁴ but also for assembling the nanowires via welding. Also in Chapter VI demonstrate that the welding strategy allows for the formation of single-crystalline oxide-free Mg₂Si bridges between single-crystalline Mg₂Si nanowires.¹³⁴ It is believed that such oxide-free welding strategy is highly beneficial for extending enhanced thermoelectric performance expected of individual nanowires to bulk devices composed of multiple nanowires. In this chapter, the aim of the current manuscript is to assess and describe the thermoelectric performance of these large-scale Mg₂Si welded nanowire assemblies obtained using the solid-state phase transformation strategy, and compare it to that obtained from microcrystalline Mg₂Si assemblies (assemblies composed of multiple micron-scale Mg₂Si crystals will henceforth be referred to as microcrystalline Mg₂Si

assemblies in this chapter). In addition, the challenges involved in retaining enhanced thermoelectric performance expected of individual nanowires even in bottom-up assembled devices composed of large quantities of nanowires, and opportunities available to overcome these challenges will be discussed in detail in this chapter.

6.2 Experimental Methods

Four different types of pellets were prepared for this study: (a) non-welded microcrystalline Mg_2Si pellets, (b) welded microcrystalline Mg_2Si pellets, (c) non-welded Mg_2Si nanowire pellets and (d) welded Mg_2Si nanowire network pellets (Table 6.1). The primary raw material employed for the fabrication of these pellets is (100)-oriented silicon wafers. Wafers of the same type were employed for the fabrication of all the samples. One of the primary processes employed for obtaining microcrystals and nanowires of Mg_2Si is solid-state phase transformation. More specifically, the following procedure was employed for the fabrication of non-welded microcrystalline Mg_2Si nanowire pellets. (100)-oriented silicon wafers were crushed in a mortar and pestle for 15 minutes to obtain 5-20 micron sized silicon crystals. The silicon microcrystals were then cold pressed at a pressure of 500 MPa and 25 °C to obtain 'green' pellets that are 7 mm in diameter and 60 μm in thickness each. Following the pelletization, polished magnesium foils were added to both the flat ends of the green pellets and pressed again at the same temperature and pressure. This composite composed of microcrystalline silicon pellets covered at the ends with polished magnesium foil was then heated to 400 °C for 2 hours in a vacuum chamber operating at a pressure of 50 mTorr. This heating allowed for phase transforming silicon

microcrystals into Mg_2Si microcrystals. These phase transformation experimentation was performed in the presence of hydrogen to minimize the formation of MgO . The Mg_2Si microcrystalline powder was then hot pressed at 500 MPa and 400 °C for 2 hours to obtain highly dense microcrystalline Mg_2Si pellets that are 7 mm in diameter and 1 mm in thickness each. The highly dense pellets were then annealed inside the vacuum chamber at 650 °C for 1 hour. Welded microcrystalline Mg_2Si pellets were also made using the same procedure, with one exception. Here silica nanoparticle-decorated silicon microcrystals were employed as the starting material. The average diameter of the silica nanoparticles in these powders was 200 nm. The procedure useful for preparing these silica-nanoparticle decorated silicon microcrystals was described previously.¹³⁴

On a similar note, non-welded Mg_2Si nanowires pellets and welded Mg_2Si nanowire network pellets were also fabricated using the same procedure described above, with the exception being that silicon nanowires were employed as the starting material. The silicon nanowires employed for this purpose were obtained by electroless etching, a procedure that was described in chapter II. The silicon nanowires obtained by electroless etching had diameters in the range of 20-50 nm and a length of approximately 20 microns. While silicon nanowires and magnesium foils served as the raw materials for the fabrication of Mg_2Si nanowire pellets, silica nanoparticle-decorated silicon nanowires and magnesium foils served as raw materials for the fabrication of Mg_2Si welded nanowire pellets. For clarity, the nomenclatures that will be employed to describe the samples employed in this chapter, along with their densities, are presented in Table 6.1.

Table 6.1. The nomenclature employed to describe various samples employed in this study, along with the densities of their respective pellets.

Sample name	Description	Density of the pellet
Non-welded microcrystalline Mg ₂ Si pellet	Pellet composed of microcrystals of Mg ₂ Si	84.48
Welded microcrystalline Mg ₂ Si pellet	Pellet composed of welded Mg ₂ Si microcrystalline networks that have Mg ₂ Si microcrystals connected together via Mg ₂ Si bridges	83.7
Non-welded Mg ₂ Si nanowire pellet	Pellet composed of nanowires of Mg ₂ Si	83.64
Welded Mg ₂ Si nanowire network pellet	Pellet composed of welded Mg ₂ Si nanowire networks that have Mg ₂ Si nanowires connected together via Mg ₂ Si bridges	83.38

For determining thermoelectric characterization of the samples, the Seebeck coefficient was obtained by using analog subtraction method.^{136, 137} Here, a platinum resistive heater was used to supply a time dependent temperature difference on the sample by the pulsed heat. The temperature difference (ΔT) between two electrical contacts and the voltage at each location (ΔV_1 and ΔV_2 ,) on the sample was measured by using two same thermocouples (chromel or alumel) in Figure 6.1. From these temperature and voltage difference, Seebeck coefficient (S) of the sample was calculated using the formulae below. ($\Delta V_1 = (S - S_C)\Delta T$ and $\Delta V_2 = (S - S_A)\Delta T$)

$$\frac{\Delta V_1}{\Delta V_2 - \Delta V_1} = \frac{S - S_C}{S_C - S_A}$$

$$\frac{\Delta V_2}{\Delta V_2 - \Delta V_1} = \frac{S - S_A}{S_C - S_A}$$

Here S is seebeck coefficient of the material being tested, S_C and S_A are the seebeck coefficients of chromel and alumel wires respectively. Simultaneously, electrical conductivity of the sample was measured by four probe method.

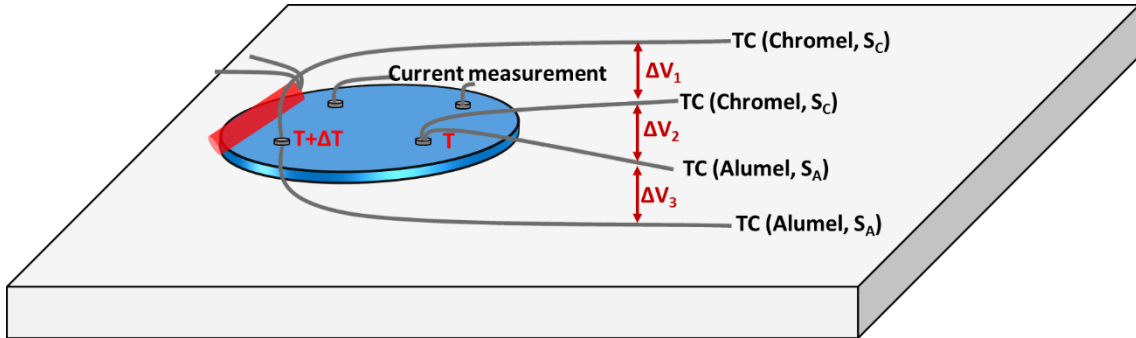


Figure 6.1. A schematic for thermoelectric measurement of Mg_2Si pellet on a BN substrate via analog subtraction method. The same setup is also used for measuring electrical conductivity via 4-probe van-der-paw technique.

6.3. Results and Discussions

6.3.1. Synthesis of Mg_2Si Microcrystals and Nanowire Pellets

Micrographs of silicon microcrystals and nanowires obtained respectively by crushing and electroless etching are presented in Figure 6.2(a) and 6.2(b). Mg_2Si microcrystals and nanowires obtained by reacting silicon microcrystals and nanowires with magnesium foils and phase transforming them are respectively presented in Figures 6.2(c) and 6.2(d). For obtaining welded Mg_2Si networks in both microcrystalline and nanowire forms, phase transformation of silica nanoparticle-decorated silicon microcrystals and nanowires was performed.

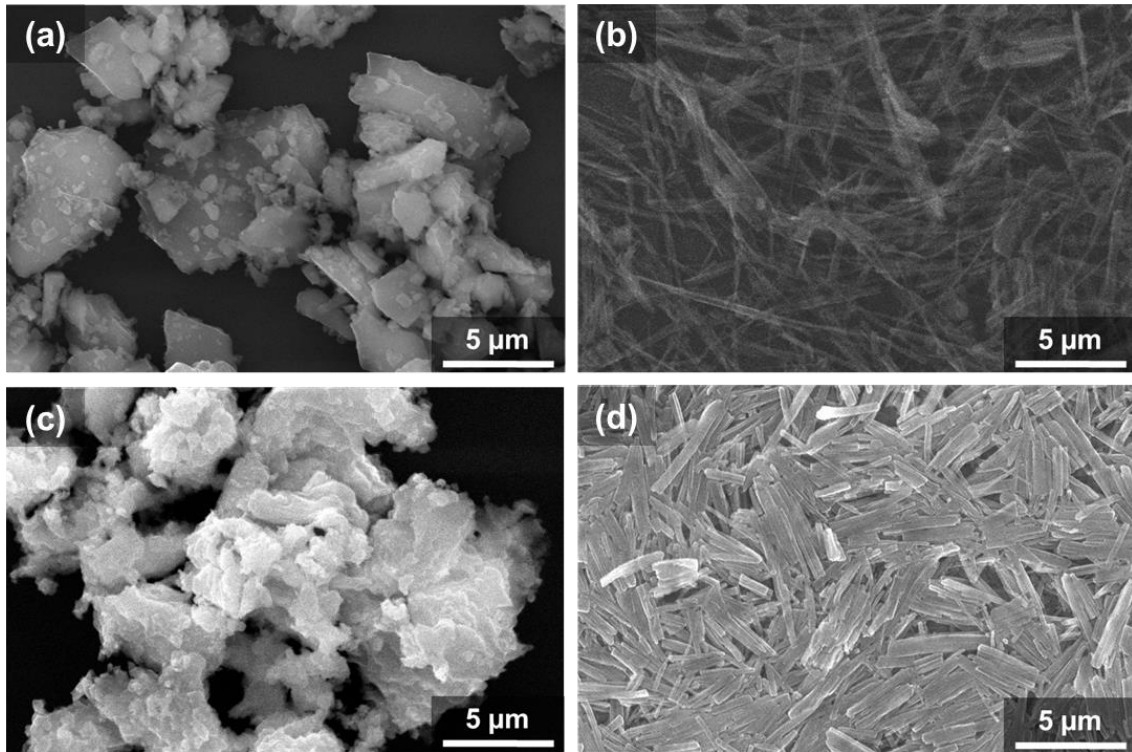


Figure 6.2. Scanning electron micrograph of (a) silicon microcrystals and (b) silicon nanowire. The silicon microcrystals and nanowires were phase transformed into (c) Mg₂Si microcrystals and (d) Mg₂Si nanowires by solid-state of magnesium into silicon microcrystals and nanowire, respectively.

Micrographs of silica nanoparticle-decorated silicon microcrystals and nanowires are shown in Figure 6.3(a) and 6.3(b). Welded Mg₂Si microcrystalline networks and Mg₂Si welded nanowire networks obtained by phase transforming silica nanoparticle-decorated silicon microcrystals and nanowires are presented in Figures 6.3(c) and 6.3(d). From a comparison of nanowires in Figures 6.2(b) and 6.3(b), and Figures 6.2(d) and 6.3(d), it could be clearly seen that welding of nanowires led to the formation of bridges between the nanowires (Figure 6.3(d)) and thereby the formation of networks.

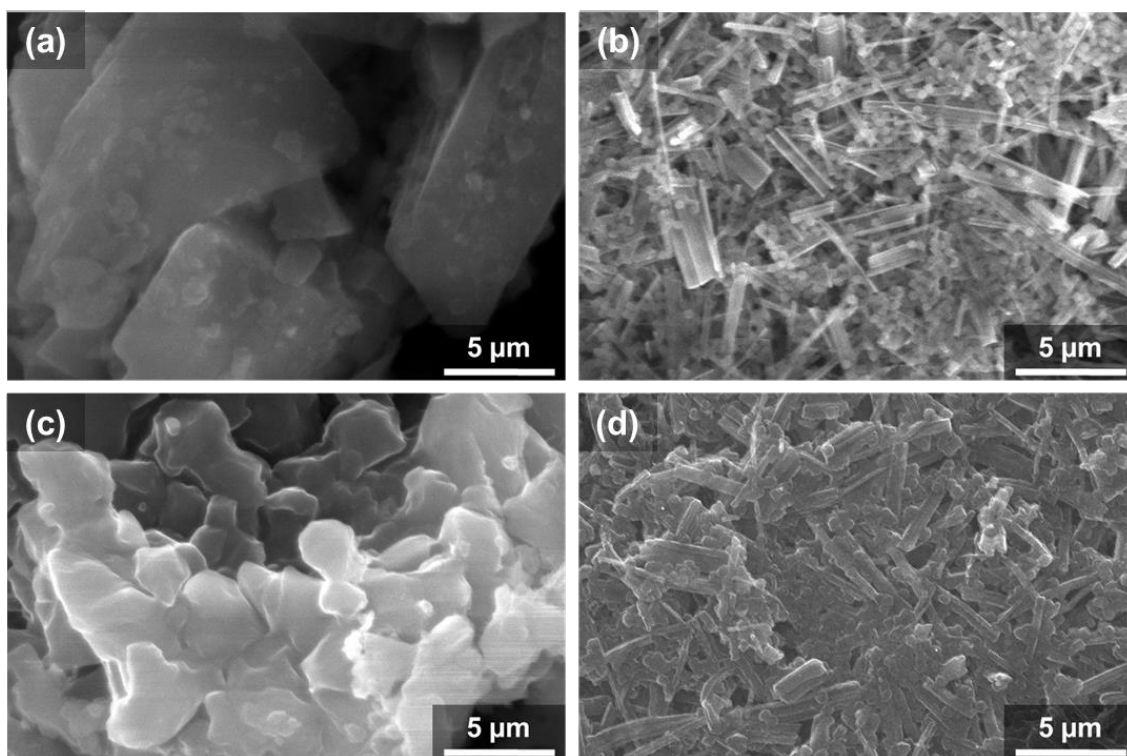


Figure 6.3. Scanning electron micrograph of silica nanoparticle decorated (a) silicon microcrystals and (b) silicon nanowire. SEM images of (c) welded Mg_2Si microcrystalline networks and (d) Mg_2Si welded nanowire networks.

Density measurements of the nanowire pellets indicated that they are highly dense in all the cases, and that they exhibited densities in the range of 83-85% of the theoretical density of Mg_2Si .

Post phase transformation, XRD analyses of all the samples were performed. The analysis indicated that in all the cases, the phase transformation led to the complete conversion of silicon into Mg_2Si (Figure 6.4). No presence of any residual silicon was observed in these samples. Although it is believed that the surfaces of the Mg_2Si nanowires and bridges are covered with MgO layers, these minute amounts of MgO on their surfaces was not detected in the XRD analyses (Figure 6.4).

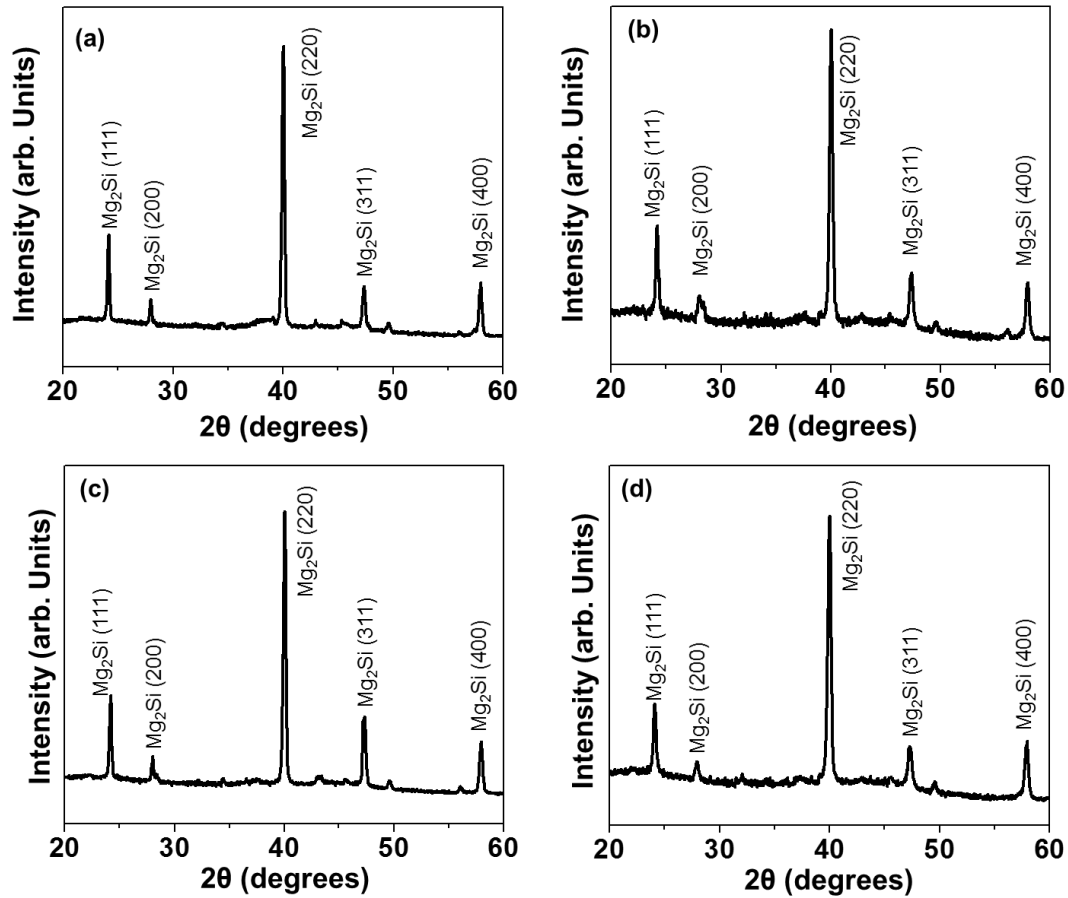


Figure 6.4. XRD pattern of (a) Mg_2Si microcrystals, (b) Mg_2Si nanowires, (c) welded Mg_2Si microcrystalline networks and (d) Mg_2Si welded nanowire networks.

6.3.2. Thermoelectric Performance of Mg_2Si Device

Figure 6.5 shows temperature dependence of the electrical conductivities of both (a) non-welded and welded microcrystalline Mg_2Si pellets, and (b) non-welded and welded Mg_2Si nanowire network pellets, respectively. The electrical conductivity of all samples increased with increase in temperature due to increase in the number of charge carriers, which is typical behavior of non-degenerate semiconductor. A maximum difference was observed in the electrical conductivities of the sample at 875 K. At this

temperature, electrical conductivity of welded microcrystalline Mg_2Si pellet was observed to be 2.2 times that of the non-welded microcrystalline Mg_2Si pellet. Also, as compared to non-welded nanowire network pellet, welded Mg_2Si nanowire network pellet was has 5-fold higher electrical conductivity. However, in the case of Mg_2Si nanowire network pellets, it was observed that the electrical conductivity was lower than microcrystalline Mg_2Si pellets. Although Mg_2Si nanowire welding can enhance their electrical conductivity, the increased presence of MgO layer on Mg_2Si nanowire surface decreases their electrical conductivity.

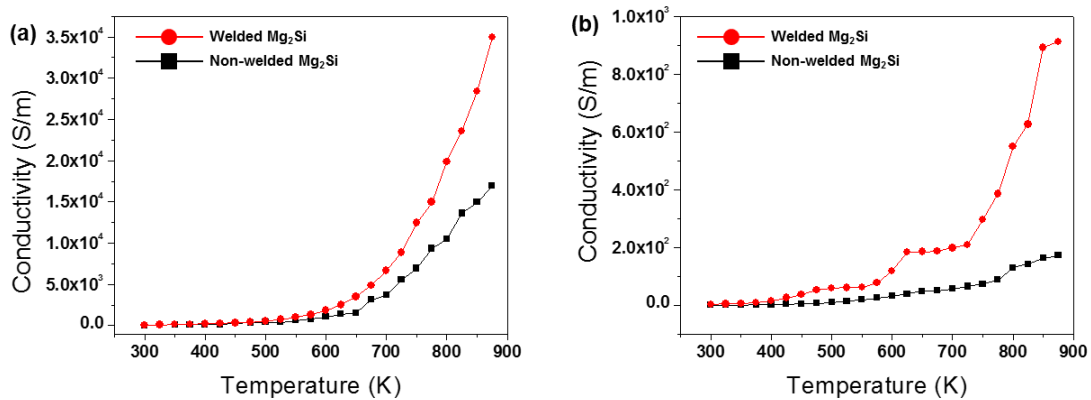


Figure 6.5. Temperature dependence of the electrical conductivity of (a) non-welded and welded microcrystalline Mg_2Si pellets, and (b) non-welded and welded Mg_2Si nanowire network pellets, respectively.

Figure 6.6 shows temperature dependence of Seebeck coefficients of (a) non-welded and welded microcrystalline Mg_2Si pellets, and (b) non-welded and welded Mg_2Si nanowire network pellets, respectively. The Seebeck coefficient of all samples showed negative values throughout the entire temperature range indicating n-type behavior. The Seebeck coefficient of the both non-welded and welded microcrystalline Mg_2Si pellets

were observed to be similar. The absolute value of Seebeck coefficient increased up to 425K and later decreased as increasing temperature because of increase in the carrier concentration by intrinsic conduction. Similar behavior was reported in number of experimental and theoretical studies.¹³⁸⁻¹⁴¹ However, the Seebeck coefficient of non-welded and welded Mg₂Si nanowire network pellets showed lower values than microcrystalline Mg₂Si pellets. It is possible that the sample might be doped with Ag, which is known as p-type dopant in Mg₂Si, that might remain after the electroless etching of Si wafers even after HNO₃ etching.

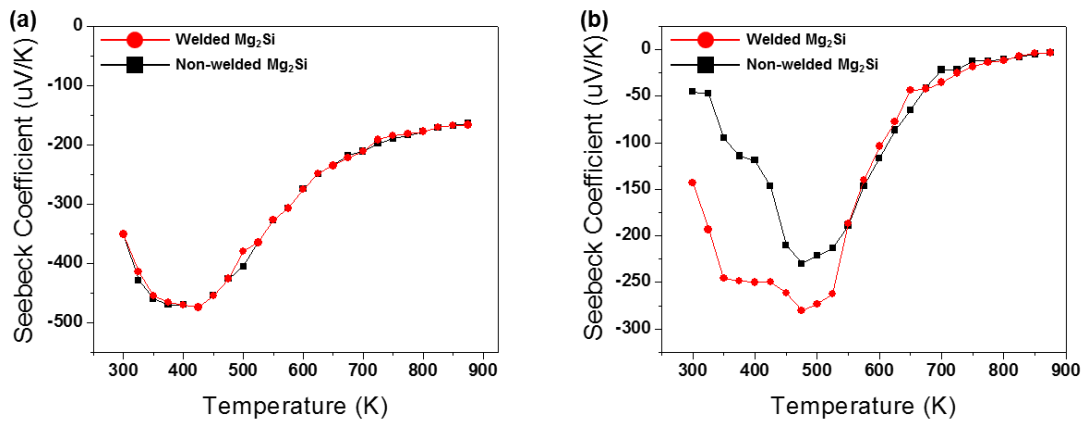


Figure 6.6. Temperature dependence of the Seebeck coefficient of (a) non-welded and welded microcrystalline Mg₂Si pellets, and (b) non-welded and welded Mg₂Si nanowire network pellets.

Figure 6.7 shows the temperature dependence of power factor of (a) non-welded and welded microcrystalline Mg₂Si pellets, and (b) non-welded and welded Mg₂Si nanowire network pellets. The power factor of non-welded and welded microcrystalline Mg₂Si pellets samples was increase as increasing temperature due to increase in electrical

conductivity. The highest power factor of welded and non-welded microcrystalline sample were $0.972 \times 10^{-3} \text{ Wm}^{-1}\text{K}^{-2}$ and $0.455 \times 10^{-3} \text{ Wm}^{-1}\text{K}^{-2}$ at 875 K, respectively, and the performance of thermoelectric power factor welded Mg_2Si pellet was shown to be 2-fold higher than the non-welded pellet. For the Seebeck coefficient of non-degenerate semiconductor is given by

$$S = \frac{8\pi^2 k_B^2}{3eh^2} m^* T \left(\frac{\pi}{3n}\right)^{\frac{2}{3}}$$

where n is carrier concentration, m^* is the effective mass of carrier, k_B is the Boltzmann constant, e is the electronic charge, and h is the Planck constant. This equation shows that interrelationship between Seebeck coefficient and carrier concentration. Higher carrier concentration of non-degenerated Mg_2Si results in higher electrical conductivity but it leads to the lower Seebeck coefficient. In this experiment, the Seebeck coefficient of welded and non-welded microcrystalline Mg_2Si is almost the same, but the electrical conductivity ($\sigma = ne\mu$, μ is carrier mobility) of welded microcrystalline Mg_2Si pellet shows higher than non-welded microcrystalline pellet. This is believed to be the result of increase in carrier mobility through Mg_2Si bridges. The performance of thermoelectric power factor of the welded microcrystalline Mg_2Si pellet was shown to be 2-fold higher than the non-welded microcrystalline pellet. This value is twice that reported in the literature for undoped Mg_2Si . By assuming literature value for thermal conductivity of Mg_2Si ^{139, 141, 142} ($k=3 \text{ W/m-K}$), zT was estimated to be about 0.3 at 850K (Figure 6.8). However, the power factor of non-welded and welded Mg_2Si nanowire network pellets increases up to 525-550K and then decrease upon further temperature rise. The lower electrical conductivity of Mg_2Si nanowire network sample compared to that of the

microcrystalline sample is believed to be caused by MgO layer on nanowire surface. This result led to a decrease in the zT of nanowire network samples compared to microcrystalline samples.

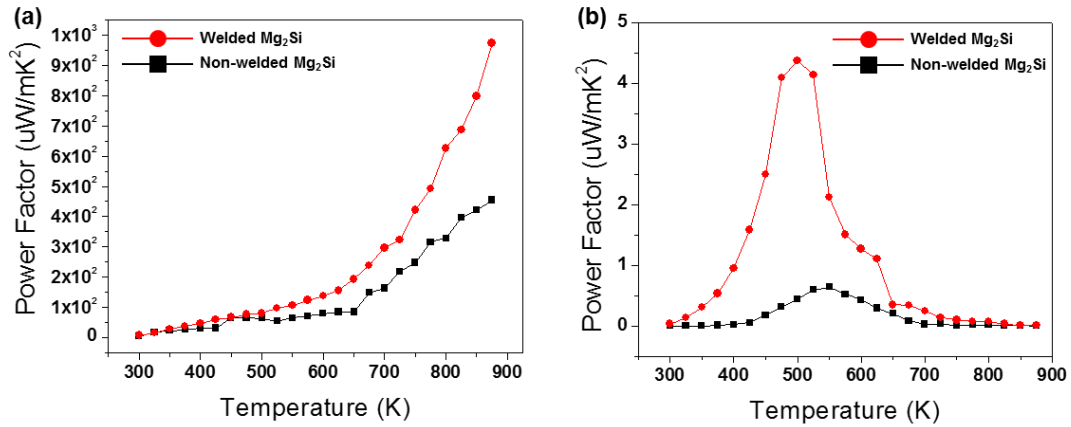


Figure 6.7. Temperature dependence of the powder factor ($S^2\sigma$) of (a) non-welded and welded microcrystalline Mg_2Si pellets, and (b) non-welded and welded Mg_2Si nanowire network pellets.

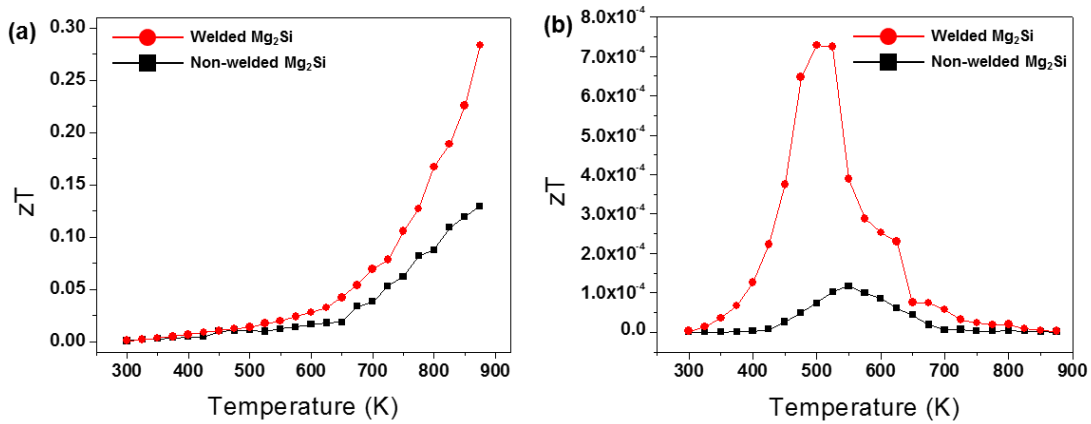


Figure 6.8. Dimensionless figure of merit (zT) of (a) non-welded and welded microcrystalline Mg_2Si pellets, and (b) non-welded and welded Mg_2Si nanowire network pellets.

6.4 Conclusions

Thermoelectric performance of Mg_2Si fabricated by solid-state phase transformation for the synthesis and assembly via welding of Mg_2Si microcrystalline and nanowire network devices was investigated. The solid state diffusion of magnesium through silicon microcrystals/nanowires and then the silica nanoparticles present between them resulted in phase transformation of silicon into Mg_2Si microcrystalline/nanowire network and formation of Mg_2Si path between the microcrystals/nanowires. As compared to non-welded microcrystalline Mg_2Si device, welded microcrystalline Mg_2Si device was shown to have 2-fold higher electrical conductivity, while maintaining the same Seebeck coefficient. The performance of thermoelectric power factor of the welded Mg_2Si pellet was shown to be 2-fold higher than the non-welded pellet because of increased carrier mobility through the Mg_2Si bridges. The high power factor of $0.972 \times 10^{-3} \text{ Wm}^{-1}\text{K}^{-2}$ achieved at 875 K is twice that reported in the literature for undoped Mg_2Si . It is expected that, the increased surface area MgO layer on Mg_2Si nanowire of the network samples led to decrease in electrical conductivity, and unintentional impurity doping led to decrease in Seebeck coefficient of both nanowire network samples. Nevertheless, these results suggest that oxide-free interface formation through the nanowire welding is essential for the large scale nanowire thermoelectric applications.

CHAPTER VII

SUMMARY AND FUTURE WORK

7.1. Dissertation Summary

The main objective of this dissertation is large scale synthesis and assembly of Mg₂Si nanowires. Mg₂Si is a promising thermoelectric material in the temperature range from 500 to 800 K because it is non-toxic, abundant, and inexpensive material. It was predicted through theoretical modeling by Satyala and Vashaee that reduction of grain sizes lead to an increase in the zT values of Mg₂Si.⁶⁷ Therefore, it is possible to achieve zT values of ~ 1.2 by making Mg₂Si in nanowire form with diameters on the order of 5-20 nm.⁶⁷ However, high vapor pressure and consequently low condensation coefficient of magnesium coupled with its oxidizing nature prevent the synthesis of Mg₂Si nanowires by chemical vapor deposition (CVD). In this dissertation, the phase transformation of pre-synthesized Si nanowires into Mg₂Si nanowires was performed as a strategy for the synthesis and assembly of Mg₂Si nanowires, and their thermoelectric performance was characterized by mass producing them.

Fabrication of silicon nanowire array was obtained by using electroless etching of silicon wafers. P-type (B doped) and n-type (P or Sb doped) wafers are applied for the synthesis of silicon nanowires, the diameter of nanowires was controlled from 20 nm to 300 nm, and the length of nanowire was controlled in range of 3 – 20 μm . The nanowire was single-crystalline in nature, and that growth direction was either along the [110] or the [100] crystal orientation.

The reaction of silicon nanowires with magnesium supplied via the pulsing through the vapor phase led to complete phase transformation of the single crystalline silicon nanowires into polycrystalline Mg_2Si nanowires. The use of silicon nanowires in array format for the phase transformation process ensured the conformal coating of magnesium all along the lengths of the nanowires, and hence in their complete phase transformation into Mg_2Si . The supersaturation of the sharp tips of the silicon nanowires with the diffusing magnesium led to the formation of a single nucleus within each nanowire. The growth of this single nucleus within each nanowire led to the formation of single-crystalline Mg_2Si nanowires.

The phase transformation strategy was extended for phase transforming silica nanoparticle bridged silicon nanowires into Mg_2Si nanowires welded together with Mg_2Si bridges. Magnesium diffused through the silicon nanowires first and then the silica nanoparticle bridging the nanowires reacted with them and left an Mg_2Si path between the nanowires. The welding of Mg_2Si nanowires with Mg_2Si bridges was further confirmed by the electrical conductivity measurements. Welded nanowires assemblies exhibited conductivities two orders of magnitude higher than those exhibited by non-welded nanowires. Thermoelectric performance evaluation of these nano-scale welded and assembled pellets proved our hypothesis that solid-state phase transformation can be used for both the synthesis and assembly of highly efficient bulk Mg_2Si nanowire pellets. The performance of thermoelectric power factor of the welded microcrystalline Mg_2Si device was shown to be 2-fold higher than the non-welded pellet because of increased carrier

mobility through the Mg₂Si bridges. The high power factor of $0.972 \times 10^{-3} \text{ Wm}^{-1}\text{K}^{-2}$ achieved at 875 K is twice that reported in the literature for undoped Mg₂Si.

7.2 Future Research Directions

From this research, the phase transformation strategy of pre-synthesized silicon nanowires into Mg₂Si nanowires led to both polycrystalline and single-crystalline crystal structure. Through mass production of Mg₂Si microcrystals/nanowire powder and welded Mg₂Si assemblies, thermoelectric performance was enhanced. However, it is expected that the increased surface area MgO layer on Mg₂Si nanowire of the network samples led to decrease in electrical conductivity, and unintentional impurity doping led to decrease in Seebeck coefficient of both nanowire network samples. Also, intrinsic Mg₂Si still has low zT value less than 0.3, because of the low carrier concentration.⁴⁶ Impurity doping such as Sb, Al, Ag in Mg₂Si can lead to increase in thermoelectric properties by increasing carrier concentration, but these dopant materials have very low solubility in Mg₂Si.^{46, 141-146} To enhance thermoelectric performance of intrinsic Mg₂Si nanowires, impurity doping in Si nanowires should be performed using two different strategies: 1) Sn diffusion into Si nanowires by solid state diffusion, and 2) Si nanowires fabrication from Sb doped Si wafer. The impurity doped Si nanowires can be phase transformed into single-crystalline Mg₂Si nanowires by solid state diffusion and the nanowires can be welded together with Mg₂Si bridges. Then, it is possible to fabricate high thermoelectric performance Mg₂Si devices.

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