CLOCK GENERATION DESIGN FOR CONTINUOUS-TIME SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER IN COMMUNICATION SYSTEMS

A Dissertation

by

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ABSTRACT

Software defined radio, a highly digitized wireless receiver, has drawn huge attention in modern communication system because it can not only benefit from the advanced technologies but also exploit large digital calibration of digital signal processing (DSP) to optimize the performance of receivers. Continuous-time (CT) bandpass sigma-delta (ΣΔ) modulator, used as an RF-to-digital converter, has been regarded as a potential solution for software defined ratio. The demand to support multiple standards motivates the development of a broadband CT bandpass ΣΔ which can cover the most commercial spectrum of 1GHz to 4GHz in a modern communication system.

Clock generation, a major building block in radio frequency (RF) integrated circuits (ICs), usually uses a phase-locked loop (PLL) to provide the required clock frequency to modulate/demodulate the informative signals. This work explores the design of clock generation in RF ICs. First, a 2-16 GHz frequency synthesizer is proposed to provide the sampling clocks for a programmable continuous-time bandpass sigma-delta (ΣΔ) modulator in a software radio receiver system. In the frequency synthesizer, a single-sideband mixer combines feed-forward and regenerative mixing techniques to achieve the wide frequency range. Furthermore, to optimize the excess loop delay in the wideband system, a phase-tunable clock distribution network and a clock-controlled quantizer are proposed. Also, the false locking of regenerative mixing is solved by controlling the self-oscillation frequency of the CML divider. The proposed frequency synthesizer performs excellent jitter performance and efficient power consumption.

Phase noise and quadrature phase accuracy are the common tradeoff in a quadrature voltage-controlled oscillator. A larger coupling ratio is preferred to obtain good phase accuracy but suffer phase noise performance. To address these fundamental trade-offs, a phasor-based analysis is used to explain bi-modal oscillation and compute the quadrature phase errors given by inevitable mismatches of components. Also, the ISF is used to estimate the noise contribution of each major noise source. A CSD QVCO is first proposed to eliminate the undesired bi-modal oscillation and enhance the quadrature phase accuracy. The second work presents a DCC QVCO. The sophisticated dynamic current-clipping coupling network reduces injecting noise into *LC* tank at most vulnerable timings (zero crossing points). Hence, it allows the use of strong coupling ratio to minimize the quadrature phase sensitivity to mismatches without degrading the phase noise performance. The proposed DCC QVCO is implemented in a 130-nm CMOS technology. The measured phase noise is -121 dBc/Hz at 1MHz offset from a 5GHz carrier. The QVCO consumes 4.2mW with a 1-V power supply, resulting in an outstanding Figure of Merit (FoM) of 189 dBc/Hz.

Frequency divider is one of the most power hungry building blocks in a PLL-based frequency synthesizer. The complementary injection-locked frequency divider is proposed to be a low-power solution. With the complimentary injection schemes, the dividers can realize both even and odd division modulus, performing a more than 100% locking range to overcome the PVT variation. The proposed dividers feature excellent phase noise. They can be used for multiple-phase generation, programmable phase-switching frequency dividers, and phase-skewing circuits.

DEDICATION

To my Parents, Wife, and Sister

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CHAPTER I

INTRODUCTION

1.1 Motivation

Over the past several decades, the rapid development and growth of wireless communication engineering have significantly changed and influenced our daily lives. With the advances of the los-cost CMOS technology and the progress in the fields of radio frequency (RF) integrated circuit (IC) design, wireless communication engineering has tremendously been applied in the area of wireless networks, mobile phones, television, data transferring and identification, positioning, and sensors. A lot of studies and developments keep focusing on improving the communication quality, reducing the cost, and enhancing the power efficiency [1, 2]. Although most RF IC design stressed on narrow-band systems in the past, nowadays the design techniques for broadband wireless systems are drawing a huge attention. For example, the high-level integration of multiple wireless standards which requires broadband spectrums becomes one of major trends of the modern wireless communication engineering. These changes and demands lead to the abrupt desire to developing the advanced wireless transceiver architectures.

Digital-IF receivers [3] and software radio receivers [4] are known as a potential architecture for highly-integrated wireless broadband systems. The extensive use of digitals and signal processing makes these software-oriented receivers capable to comply with the requirements of cost-efficient, multi-standards, broadband, and reconfigurability. High-resolution wide-bandwidth analog-to-digital converters (ADCs) and broadband

frequency synthesizer are one of the most critical building blocks in the development of the software-oriented receivers. Continuous-time (CT) sigma-delta (ΣΔ) ADCs have been found to be a promising architecture for these applications [5, 6, 7, 8]. However, the fact that the purity of clock crucially influences the performance of continuous-time ΣΔ ADCs makes it more challenging to design a broadband frequency synthesizer for the receivers employing a continuous-time ΣΔ ADC.

A frequency synthesizer, the core of clock generation, usually uses a phase-locked loop (PLL) to provide the required clock frequency to modulate/demodulate the informative signals. Ideally, the clock signal is expected to be a clean and sharp impulse tone in an output frequency spectrum. However, in practical the intrinsic device/component noise unpredictably and instantaneously changes the clock period and appears to be a skirt in the output spectrums. For most wireless applications, the phase noise requirement is defined according to the system signal-to-noise ratio (SNR) that heavily depends on the purity of the clock. Furthermore, the power consumption, spur tones, silicon area and circuit complexity are also the emphasis of developing a frequency synthesizer. These issues inspire a lot of studies and innovation on designing the building blocks and architectures of frequency synthesizers.

This dissertation explores the design of clock generation in RF ICs. A wideband frequency synthesizer architecture is proposed for the use in a broadband software radio receiver based on a programmable continuous-time band-pass ΣΔ modulator. Also, innovative techniques in critical building blocks such as quadrature voltage-controlled

oscillator (QVCO) and injection-locked frequency divider (ILFD) are also presented to achieve better noise performance and lower power consumption.

1.2 Research Contribution

This research investigates the design of high-performance broadband clock generation. A 2–16 GHz frequency synthesizer is proposed to generate the sampling clock for a programmable broadband continuous-time band-pass ΣΔ modulator, which is utilized in a software radio receiver to digitize the RF signals. The wide frequency range is achieved by a single-sideband (SSB) mixer that combines feed-forward and regenerative mixing techniques. A phase-tunable clock distribution network and a novel two-bit quantizer design are presented to manage the excess loop delay of the CT ΣΔ modulator over the wide operating frequencies. With the proposed dynamic current-clipped (DCC) QVCO, the broadband frequency synthesizer exhibits excellent jitter performance, less than 0.6ps when phase noise integrated in 10KHz – 20MHz. The spur tones are under -42dBc across the 1 – 8GHz range. Fabricated in a 0.13-μm CMOS technology, the core active area of the frequency synthesizer occupies 1.08mm^2 and the power consumption of the frequency synthesizer operated at maximum frequency is 64mW with 1.2/1.8V power supplies. The proposed architecture is a very cost-efficient approach for emerging broadband RF transceivers.

Quadrature voltage-controlled oscillators are recognized to be a low-power solution to generate the quadrature signals, usually a must in transceivers. However, QVCOs exhibit inferior phase noise performance and their inherent quadrature phase error

due to device mismatch leads to the problem of sideband image during mixing operation. Two QVCO topologies are proposed in this work. The first QVCO employs the capacitive source degeneration (CSD) techniques to achieve excellent quadrature phase accuracy. The second QVCO uses the dynamic current-clipped (DCC) technique to reduce the current/noise injection at the most vulnerable zero-crossing timings in order to minimize the phase noise contribution from the coupling network. The DCC QVCO allows a large coupling ratio to improve the quadrature phase accuracy and also reduce the sideband images of SSB mixer. Fabricated in TSMC 130-nm technology, the current-clipped 5GHz QVCO perform a phase noise of -121dBc/Hz at 1MHz offset while consuming 4.2mW with a 1V power supply. Monte-Carlo simulations show that quadrature phase error standard deviation is around 0.15 degree. The QVCO shows excellent performance while compared with previously reported works.

High-speed frequency dividers are the most power-hungry building block in the frequency synthesizers. Injection-locked frequency dividers are found to be one low-power solution but the narrow frequency locking range usually limits their extensive use. A complementary injection technique is proposed to enlarge the locking range to overcome the PVT variations. The complementary injection-locked frequency dividers (CILFDs) can be implemented to have even and odd division ratios. CILFDs can not only used for the frequency conversion and multi-phase clock generation but also for the phase-skewing or phase alignment as well. Fabricated in TSMC 180-nm technology, the 5GHz CILFDs have a more than 100% locking range while consuming less than 1mW power. Because of their low noise and small phase mismatch properties, CILFDs are very

potential for time-to-digital conversion. One example shows the CILFD is implemented in a 3-bit time-domain quatizer of a continuous-time lowpass ΣΔ modulator. The other example shows the excellent power consumption performance while constructing a multi-modulus phase-switching divider based on the CILFD.

1.3 Organization

A brief introduction and review of wireless communication systems are presented in Chapter II. The wireless communication standards, the major trends of wireless communication, RF receiver architectures and frequency synthesizers are discussed. Chapter III introduces the 0.5 – 4 GHz software radio receiver based on a core continuous-time bandpass ΣΔ modulator. The design issues and requirements of frequency synthesizer for the specific wireless system are emphasized and demonstrated by examples. A low-power 2 – 16 GHz frequency synthesizer is proposed to satisfy the requirements of jitter and spurious tones. A phase-tunable clock distribution network is presented for providing the clocks to the 2-bit quantizer where a timing-control technique is implemented to meet the requirement of excess loop delay.

The design of quadrature voltage-controlled oscillators is discussed in Chapter IV. The models of bimodal oscillation and phase accuracy based on the effective current phasor diagram are presented. The phase noise is modeled by a simplified time-variant analysis. Two QVCOs are presented where the first one employs the capacitive source degeneration technique to improve the quadrature phase accuracy and the second one use an innovative coupling elements to improve phase noise and phase accuracy.

Chapter V discusses the proposed complementary injection-locked frequency dividers. Two circuit implementation examples are given to demonstrate the excellent performance of the CILFDs. The final chapter draws the conclusion and summary of this research work, together with the possible future implementation and design related to this work.

CHAPTER II

CLOCK GENERATION IN WIRELESS COMMUNICATION RECEIVERS

2.1 Wireless Communication Standards and Applications

The most often used wireless standards with their occupied spectrum are shown in Fig. 2.1. It illustrates that the rapid growth of wireless communication crowds the limited spectrums. Thus, efficiently using the limited resource of spectrums has become an urgent issue. Also, preventing a good communication quality from the interference of other standards is extremely critical. Usually, each standard has its own specific requirements of data rate, coverage range and mobility as shown in Fig. 2.2. Several most important wireless standards and their applications will be introduced in the following sections.

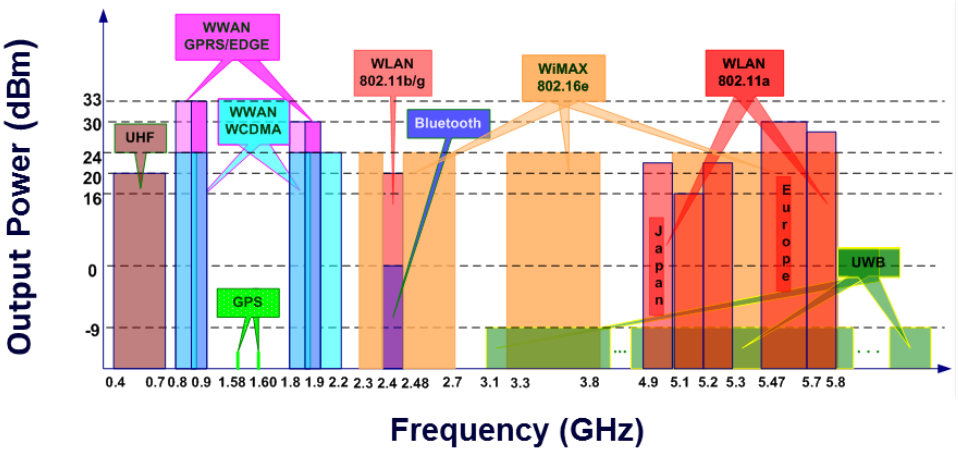


Fig. 2.1 The spectrum used in popular wireless standards.

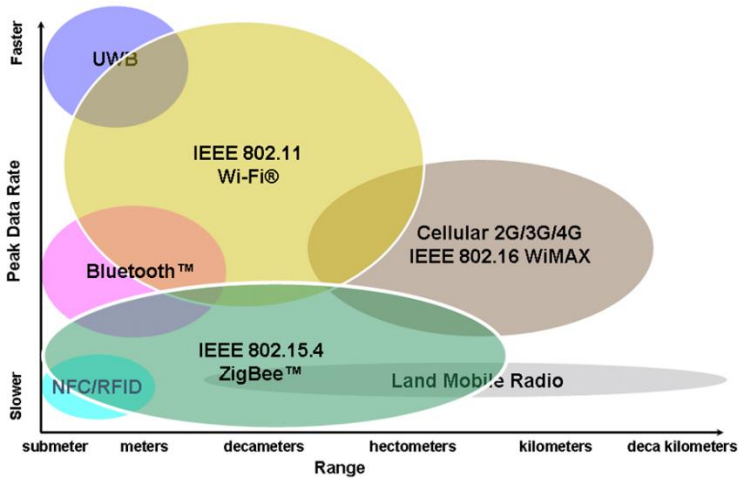


Fig. 2.2 Data-rate and coverage range of major wireless standards.

2.1.1 Mobile Phones

Mobile phones use the term "generation" to describe the status and evolution of wireless network standards. The standards of mobile phones can be categorized into 1G (first generation), 2G, 2.5G, 3G, 3.5G, 3.75 and 4G. The rise and success of mobile phones start from the 2G standards, dominated by GSM (Global System for Mobile Communication) in the early nineties. The 2G standards provide limited data rates, up to 14.4 kbps. The 2.5 G standards, such as GPRS (General Packet Radio Service) and EDGE (Enhanced Data Rates for Global Evolution), provide higher data rates than 2G standards. The fact that the 2.5G standards have good compatibility with the existing GSM networks reduces the cost of implementing 2.5G standards. This low-cost advantage of 2.5G standards deferred the growth and success of 3G standards. The 3G standards, such as CDMA2000 (Code Division Multiple Access 2000) and UMTS (Universal Mobile Telecommunications System), were launched between 2001 and 2003. The 3G standards

require expensive infrastructure costs of base station, mobile phones and new design to access modes based on CDMA.

In 2009, the 4G standards, such as mobile WiMAX and LTE (Long Term Evolution), are expected to provide the peak downstream over 100 Mbps. However, based on the IMT-Advanced (International Mobile Telecommunications Advanced) the future goal of the 4G standards requires a peak speed up to 100 Mbps for high mobility communication and 1 Gbps for low mobility communication. The 4G candidate systems able to satisfy this requirement are LTE advanced and IEEE 802.16m, both still being under development. The 4G standards also feature providing high-level reconfigurability, a flexible interoperability of various wireless networks, such as satellite, cellular, wireless local area network (WLAN) and wireless personal area network (WPAN). The reconfigurability which communicates with different standards and operates at different spectrums increases the difficulty of designing the 4G systems.

2.1.2 Wireless Local Area Network

A wireless local area network (WLAN) is a network which links two or more devices without wires/cables within a local coverage range. The WLAN devices can communicate not only via base stations but also through the peer-to-peer operation. Most WLANs are based on IEEE 802.11 standards. For avoiding the long name, 802.11 standards are also labeled as Wi-Fi (Wireless Fidelity). The currently used 802.11 a/b/g/n can cover a distance up to 100m. The wireless access method of 802.11n standard uses

MIMO (Multiple In Multiple Out) so the date rate can be enhanced up to 100 Mbps. The most frequently used WLANs are listed and compared in Table 2.1.

Table 2.1 Comparison of major WLAN standards.

Wireless Local Area Network (WLAN)				
Standard	802.11a	802.11b	802.11g	802.11n
Release Year	1999	1999	2003	2009
Frequency Band	5 GHz	2.4 GHz	2.4 GHz	2.4/5 GHz
Max. Range	50 - 100 m	~ 100 m	~ 100 m	~ 160m
Max. Data Rate	54 Mbps	11 Mbps	54 Mbps	248 Mbps
Modulation	OFDM	DSSS	OFDM	OFDM
MIMO Streams	1	1	1	4

2.1.3 Wireless Personal Area Network

Similar to WLANs, a wireless personal area networks (WPANs) is a wireless network to communicate between devices with a shorter coverage range of less than 10 meters. Bluetooth, a low-cost and low-power WPAN technology, provides a secure way to communicate information between devices such as computers, phones, electronic accessories, GPS receivers, and video game consoles with a date rate of 3 Mbps. The Ultra-Wideband (UWB) standard utilizes a high bandwidth (> 500MHz) to increase the data rate while the transmit power has to be low because the spectrum used in UWB has

to be shared with other wireless standards. Based on the rules regulated by Federal Communication Commission (FCC), the bandwidth of UWB spans from 3.1 to 10.6 GHz and the maximum emitted power spectral density has to be lower than -41.3 dBm/MHz. Recently, millimeter wave (mmWave) band is proposed for the use of WPAN in order to further increase the date rate in the short-distance wireless applications. The 802.15.3c standard, an mmWave WPAN, operates at 57 – 64 GHz and aims to allow the data rate over 1 Gbps for the applications of file transferring, HDTVs and video downloading. In contrast, ZigBee standard features a low data rate of 250 Kbps with lower power, cost and complexity than the other WPANs. A comparison table for most WPAN standards is summarized in Table 2.2.

Table 2.2 Comparison of major WPAN standards.

Wireless Personal Area Network (WPAN)				
Standard	Bluetooth	UWB	802.15.3c	ZigBee
Release Year	2002	2003	NA	2003
Frequency Band	2.4 GHz	3.1 - 10.6 GHz	60 GHz	868, 915 MHz 2.4 GHz
Max. Range	~ 10 m	~ 10 m	~ 10 m	~ 100m
Max. Data Rate	3 Mbps	1 Gbps	2 Gbps	250 Kbps
Modulation	FHSS	DS-UWB/ OFDM	SC/OFDM	DSSS

2.1.4 Worldwide Interoperability for Microwave Access

WiMAX (Worldwide Interoperability for Microwave Access), a wireless digital communications system, refers to interoperable implementations of the IEEE 802.16 family. WiMAX can provide broadband wireless access up to 30 miles for fixed stations and 3 - 10 miles for mobile stations. Based on 802.16m, WiMAX is expected to provide a peak data rate of at least 1 Gbps for fixed stations and 100Mbps to mobile users.

2.1.5 Global Positioning System

GPS (Global Positioning System) is a spaced-based global navigation satellite system which provides users the information of location, velocity and time in all weather conditions, anywhere in the world. The satellites broadcast two frequencies, 1.5754 GHz (L1 signal) and 1.2276 GHz (L2 signal) with a CDMA spread-spectrum technique.

2.2 Major Trends of Wireless Communication

Although wireless communication has been developed for more than 30 years, the desire and demand for more advanced high-performance wireless communication systems have never been stopped. The development of wireless communication closely depends on the applications of commercial products and marketing. In this section, the major trends on the path of current wireless communication technology development will be discussed.

2.2.1 High-Level Integration of Multiple Communication Standards

Recently some personal electronics, for example smart phones, have included several wireless standards in one device for approaching various applications. Moreover, integrating multiple wireless standards in a single device can fully exploit the advantageous properties of each standard. For example, Wi-Fi would be chosen for the condition of low coverage range and low mobility, and LTE would be selected for the desire of high data rate and high mobility. Currently smart phones aim to at least integrate some of GSM, LTE, WiMAX, Wi-Fi, Bluetooth, and GPS but the future goal would be integrating all standards in one electronic device. High-level integration of multiple wireless standards dramatically increases the design difficulty and complexity. The major concerns include fast switching and settling between standards, cross-talk and mutual interference between standards, and extensive reusing and sharing the circuitry for different standards.

2.2.2 Broadband

Two reasons bring the broadband wireless communication into a great demand. First, a wider bandwidth has a better capability to support a higher data rate. Second, a broadband system has better potential to accommodate multiple wireless standards.

2.2.3 High Data Rate

Twenty years ago, a data rate of tens Kbps was enough for transmitting a voice by cellular phones. With the advances of technologies, the demand for a higher data rate has

never been stopped. Several wireless applications, such as mobile TV and cloud computing, have required a data rate more than 100 Mbps and 1 Gbps data rate is seeable in applications such as HDTVs, home entertainment/theater, and mass data transferring in the very near future.

2.2.4 Low Power

Most portable wireless electronic devices are powered by batteries. The up-time and standby-time of these portable devices mainly relies on the length of batter lives and the power consumption of these portable devices. Hence, low power consumption is always desired for extending the on-time of portable devices. Also, low power consumption favors generating less heat, hence improving the reliability of these electronic devices.

2.2.5 Highly Digitalized

The CMOS technology scaling brings the advantages of low cost, fast speed and less power consumption. However, since the power supply voltage decreases with the technology scaling severely challenges the performance and design complexity of analog circuits. Therefore, a trend that digital circuits replace analog parts as more as possible is developing. In addition, digital circuits occupy smaller area and perform more robust functionality. The calibration and mass computing is easier to be realized by digital circuitry as well. As an example, the all-digital phase-locked loop has been successfully

implemented in various products. It would not be far to see the day that the digital circuits prevails in RF front-ends.

2.2.6 Low Cost

Cost is a dominating factor to influence the development of a wireless technology. Cost is the expense spent from planning a product to delivering the product to markets. A lower cost is always favorable. From the perspective of integrated circuits, low cost means less chip area, less design complexity, less power consumption and cheaper technology. Current wireless communication systems intend to minimize the number of ICs. To save cost, there have been a lot of researches working on reuse or sharing circuits between multiple wireless standards.

2.2.7 Cognitive

Cognitive radio [9] is an intelligent radio transceiver which can use the RF spectrum dynamically based on the communication quality and environment. If multiple wireless standards are achievable or multiple frequency bands are allowed to use, the cognitive radio will judiciously select the wireless standard or frequency band which can provide best communication quality.

2.3 RF Receiver Architecture

The function of wireless receivers is to demodulate RF signals down to baseband in the presence of undesired interferences and noise. Since the wanted RF signals are weak

to process in the digital domain after the attenuation of wireless transmission, the wireless receivers must provide strong signal amplification to strengthen the signal. Noise, linearity, gain, signal bandwidth, and power consumption are the critical specifications in wireless receiver design. In this section, several most important and popular receiver architectures will be introduced and compared.

2.3.1 Super-Heterodyne Receivers with Single-IF and Dual-IF

The super-heterodyne receiver, which was proposed in 1917, is still used in a lot of wireless communication systems. Fig. 2.3 shows the simplified architecture of super-heterodyne receiver with single IF (intermediate frequency) conversion. The RF signal ω_{RF} is received by an antenna and then an off-chip band-pass filter (can be a SAW filter with a high quality factor more than 1000) preserves the RF signal and attenuate the unwanted signals to avoid that strong interferences saturate the receiver. The following low-noise amplifier (LNA), which compromises the gain, noise figure and linearity, amplifies the RF signal. Then, a mixer down converts the RF signal ω_{RF} into the IF signal ω_{IF} with a LO signal ω_{LO} generated by a local oscillator (LO). The frequency of LO signal is tuned for RF frequencies to have a fixed IF frequency. An image-rejection filter and channel-selection filter are placed before and after the mixer, respectively. In most cases, the image-rejection filter is an off-chip filter due to the requirements of excellent filtering. The IF signal is then resolved into the digital domain by an analog-to-digital converter. Finally, the information is reconstructed by the digital signal processing. There is a compromise to determine the frequency of IF signal in the super-heterodyne architecture.

For example, a higher IF frequency simplifies the design complexity of the image-rejection filter because the image frequency is farer away from the frequency of the RF signal. However, a higher IF frequency complicates the design of channel-selection filter because the channel-selection filter needs a better selectivity [10, 11].

In order to mitigate this tradeoff, the super-heterodyne with dual-IF conversions is proposed in Fig. 2.4. The first mixer converts the RF signal to a high IF signal to ease the design complexity of image-rejection filter. The second mixer subsequently converts the high IF signal to a low IF signal so the requirements of channel-selection filter are relaxed. This approach relaxes the requirements of both image-rejection filter

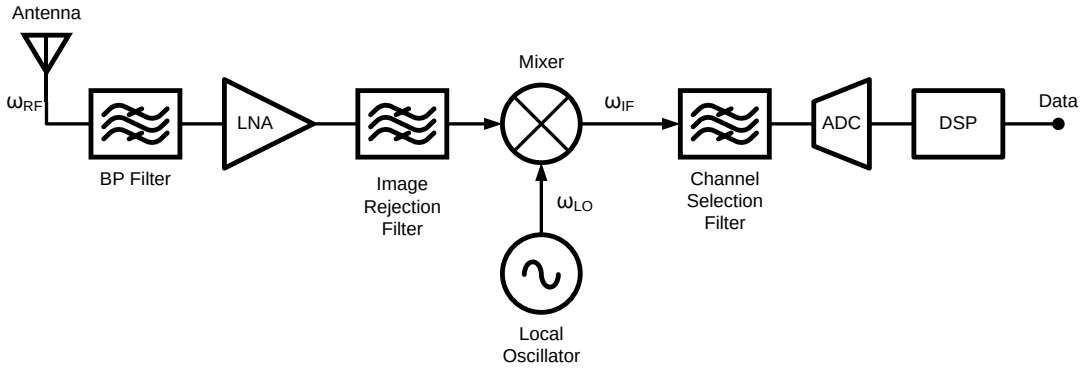


Fig. 2.3 Simplified architecture of super-heterodyne receiver with single IF conversion.

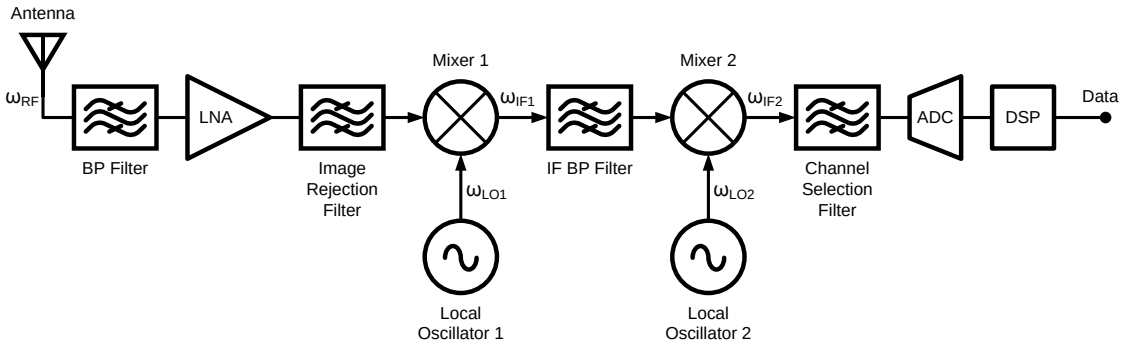


Fig. 2.4 Simplified architecture of super-heterodyne receiver with dual-IF conversion.

and channel-selection filter but one additional IF BP filter, which is mostly high-Q and off-chip, and double mixers and local oscillators required increase the cost, design complexity and power consumption.

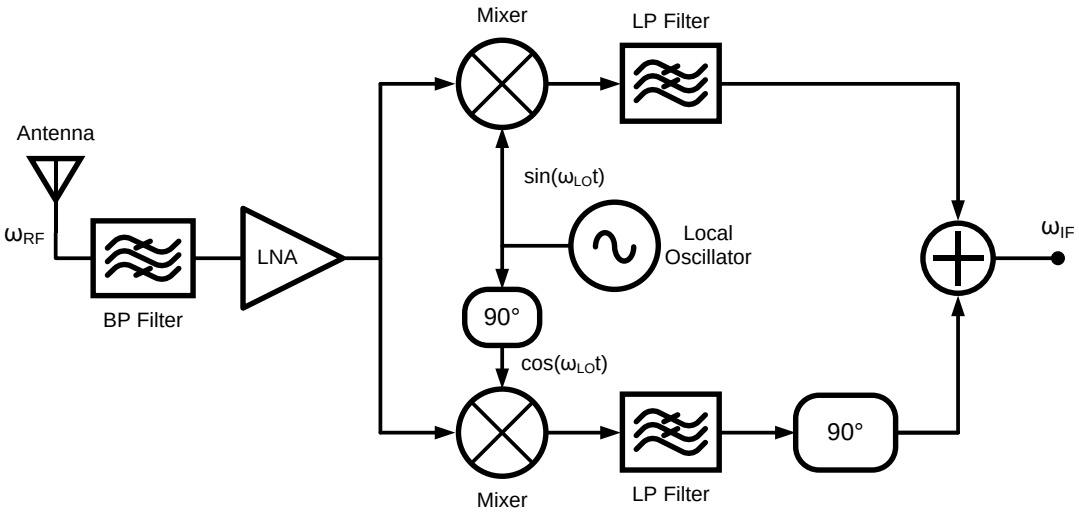
The super-heterodyne receivers mostly designed for one single wireless standard are generally used in the narrow band systems. Therefore, paralleling several super-heterodyne receivers in needed for using the super-heterodyne architectures in broadband or multi-standard wireless communications.

2.3.2 Image-Reject Receivers

The image-rejection receivers were developed to eliminate the problem of image rejection to avoid using expensive and complex band-pass filters. Image rejection receivers also relax the design requirements of band-pass filter [10, 11, 12]. The image-rejection receivers use two signal paths to sum the RF signals at the IF frequencies but cancel the image tone by manipulating quadrature phases. Fig. 2.5(a) shows the Hartley architecture uses the quadrature phase shifter to cancel the image tones. The 90 degree

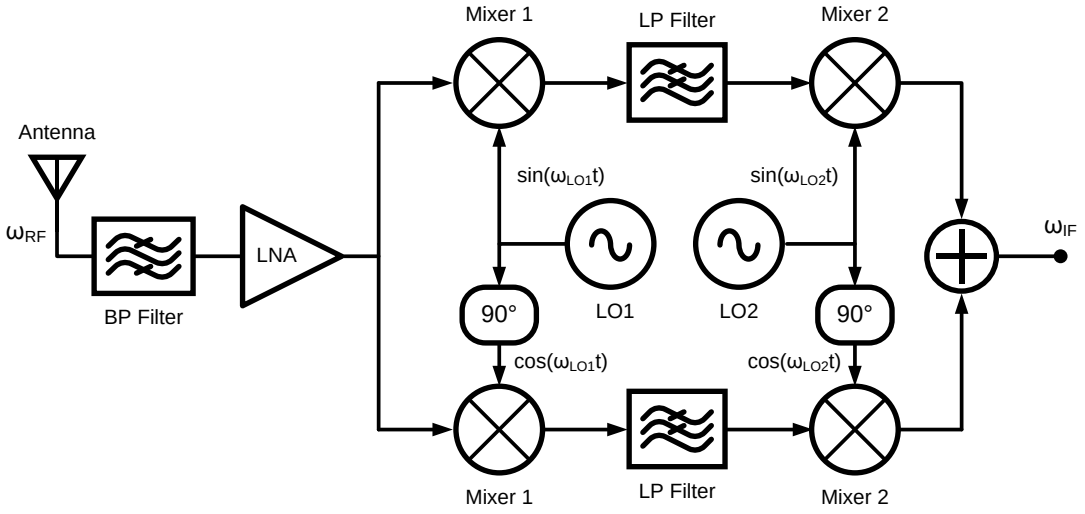
phase shifter can be replaced by the approach using a 45 degree phase shift in one signal path and -45 degree in the other signal path. These phase shifters can be realized by RC or LC filters. On the other hand, the Weaver architecture uses one additional mixer pair and quadrature LO clocks to replace the phase shifter for reconstructing the signal and canceling the image signal as shown in Fig. 2.5(b). The Weaver architecture provides better capability to drive a larger bandwidth and achieve better image rejection.

The performance of image-rejection significantly depends on the phase and amplitude mismatches between the two signal paths in the image-rejection receivers which rely on using quadrature phases to remove the image tone. These mismatches due to process variations are inevitable in current modern technologies. Therefore, the image-rejection receivers usually provide more than 40 dB image rejection.



(a)

Fig. 2.5 Image-rejection receivers: (a) Hartley architecture; (b) Weaver architecture.



(b)

Fig. 2.5 Continued.

2.3.3 Direct Conversion Receiver

The demands for image rejection and high-level chip integration motivate the development of the direct conversion receivers, which is also referred to homodyne or zero-IF receiver [13]. Fig. 2.6 shows the simplified architecture of direct conversion receiver. The frequency of LO signal ω_{LO} is tuned by an LO to match the frequency of RF signal ω_{RF} so no image frequency occurs and the frequency of IF signal ω_{IF} locates at DC. Direct conversion receivers remove the need of external expensive image-rejection filter. Moreover, the implementation of the low-pass channel-selection filter is less expensive than that of a band-pass filter. Consequently, the direct conversion receiver performs high-level on-chip integration.

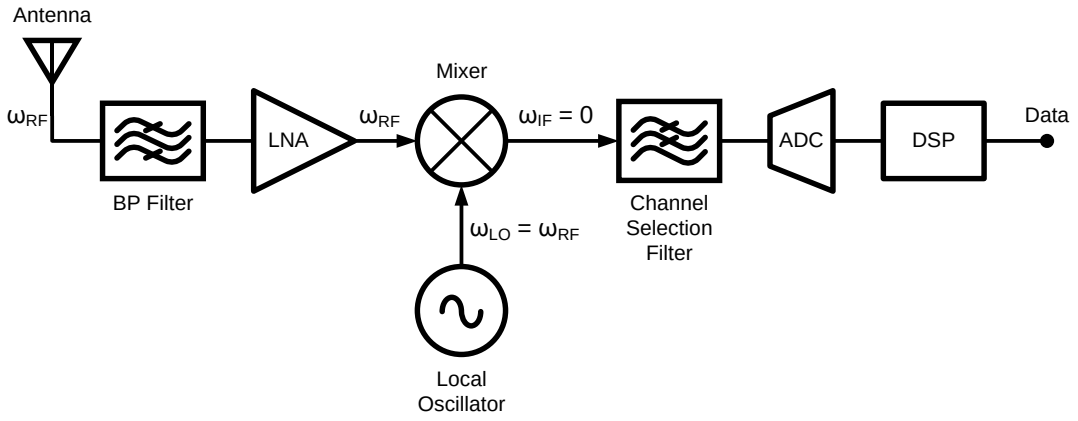


Fig. 2.6 Simplified architecture of direct conversion receiver.

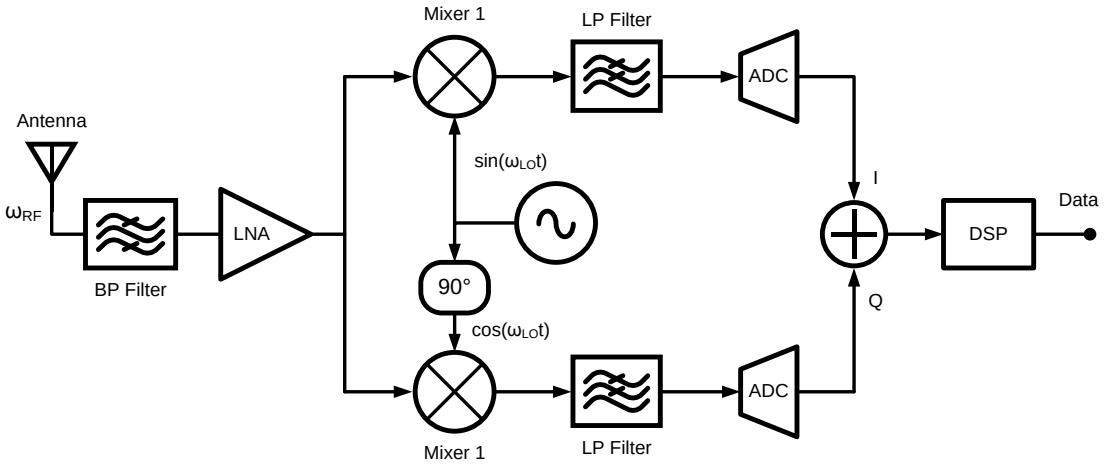


Fig. 2.7 Simplified architecture of direct conversion receiver with I/Q mixing.

In order to acquire the information of both sidebands allocated around the carrier frequency, the quadrature mixing with in-phase (I) and quadrature (Q) signals are used in direct conversion receivers as shown in Fig. 2.7. The quadrature mixing can preserve the information in both sidebands and separate the information into two paths to avoid losing

information. Therefore, the quadrature mixing provides more efficient modulation schemes.

Though the direct conversion performs excellent image rejection and high-level integration, several practical problems limit the widespread use of direct conversion receivers. The LO leakage, a leakage from local oscillator to the RF signal input of mixer, and the interferer leakage, a type of leakage from the interferers at the output of LNA to the path of local oscillator, generate the DC offsets at output of mixer. The DC offsets occurred after mixing operation would corrupt the signal quality and saturate the baseband circuitries so the bit error rate of the system would be degraded. Furthermore, because the power spectral density of flicker noise of MOS transistors, which is inversely proportional to frequency, is significant at low frequencies, the performance of direct-conversion receivers are vulnerable to the flicker noise of MOS transistors. The intermodulation from harmonics would directly locate at DC, where the signal locates, so these intermodulation tones can hardly be reduced by the filtering techniques.

2.3.4 Low-IF Receiver

As for mitigating the DC offset and flicker noise of direct conversion and keeping all its advantages, low-IF receiver was proposed [14]. Low-IF architecture compromises between direct conversion and super-heterodyne architectures. As shown in Fig. 2.8, a quadrature mixer directly converts the RF signal down to IF frequencies which can be as low as one or two channel bandwidths away from DC. The use of IF frequency not only makes the low-IF receiver not so sensitive to the DC offsets and

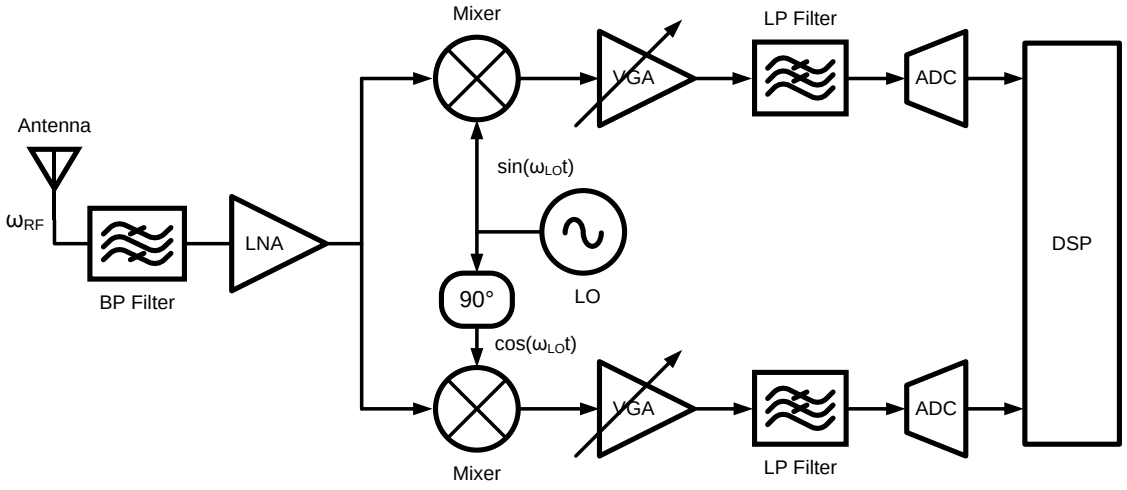


Fig. 2.8 Simplified architecture of low-IF receiver.

fliker noise but also allow the IF signals to be easily sampled by ADC. The image rejection can be implemented in the digital domain. Since all the filtering can be realized on-chip, low-IF receivers perform high-level on-chip integration.

2.3.5 Digital-IF Receiver

Digital-IF receivers are also referred to as software defined radio. The aim of digital-IF receivers is to use robust and low-cost CMOS digital circuitries and digital signal processing as more as possible. The extensive use of digital circuitries and signal processing makes the digital-IF receiver reconfigurable for various systems, wireless standards, and modulation schemes. The communication signal quality can be tuned and calibrated through the DSP.

Fig. 2.9 shows a simplified architecture of digital-IF receiver. The signal received from the antenna is filtered by a band-select band-pass filter to remove unwanted

spectrum. After amplified by the high-linearity LNA, the RF signal is then filtered by the image rejection band-pass filter to attenuate the interference around the image frequency. Then, the RF signal mixed by the LO signal converts down to the IF frequency (100 – 200 MHz) for which there is no specific standard. Followed by the VGA to amplify the signal large enough to be processed by the IF bnad-pass ADC, the IF band-pass filter attenuates the unwanted spectrums to avoid saturating the input of ADC. The use of IF frequency mitigates the problems of DC offset and flicker noise. The channel filtering, channel image-rejection, DC offset cancellation and calibration, standard configuration, and system adaptive tuning can be realized in digital domain by means of DSP. The digital-IF receivers are able to support for multi-standard receiver and perform excellent single-chip integration. However, the digital-IF receivers require an ADC with high resolution, usually 12 – 16 bits, and a sampling rate around several hundred MHz. These ADC requirements are very challenging for current CMOS technologies.

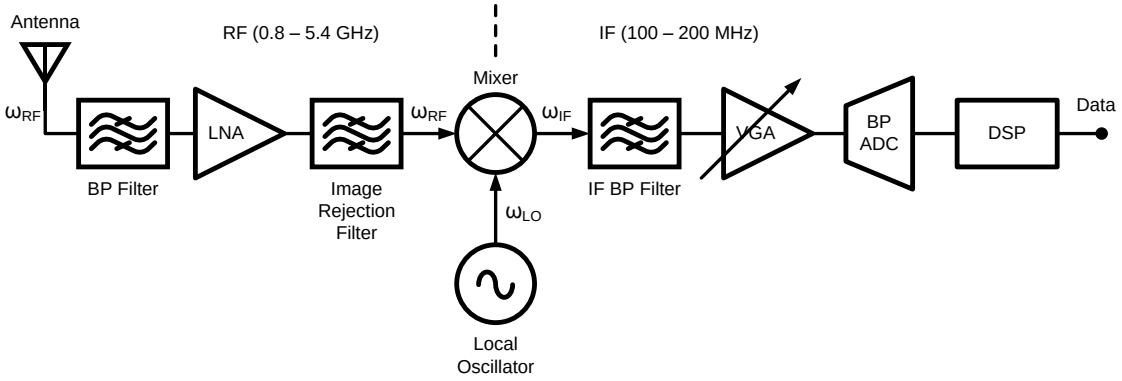


Fig. 2.9 Simplified architecture of digital-IF receiver.

2.3.6 Software Radio Receiver

The software radio was first introduced by Joseph Mitola III in 1991 [4]. The terminology of "software radio" means that the modulation and demodulation of signals is realized by the DSP and software and the radio operations can be reconfigured by the software programs. The ideal software radio architecture is shown in Fig. 2.10. The T/R (transmit/receive) switch multiplexes the RF signal between transmitting path and receiving path. In the receiving path, the RF ADC directly samples and digitizes the RF input signal received from antenna. The digitized data stream is then processed by the DSP to demodulate and reconstruct the information. The software radio receivers perform the analog-to-digital conversion as close to antenna as possible to use the digitals as more as possible. The approach matches the trends that digital circuits is getting prevailing analog ones in the modern and future development of CMOS technologies.

In ideal software radio architecture, the signals received from antenna are

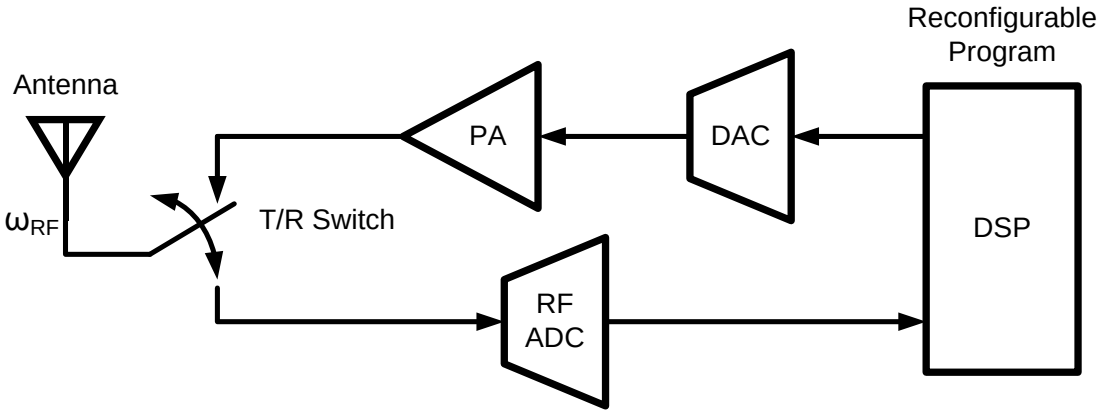


Fig. 2.10 Simplified architecture of ideal software radio.

usually very small (μW – mW range). Consequently, the RF ADC needs a resolution of more than 20 bits at sampling frequency to satisfy the requirement of receiver's dynamic range. The stringent requirements of RF ADCs are impossible to achieve in current CMOS technologies. Thus, signal amplification is needed before the ADC.

The practical realization of a software radio receiver is shown in Fig. 2.11. After filtered by RF band-pass filter, the RF signal is amplified by the LNA to relax the dynamic range requirement of RF ADCs. The ADC digitizing the amplified RF signal allows DSP to implement the demodulation, protocols and equalization in digital domain. The DSP can be reconfigured by the software programs to support multiple standards. It is also feasible to adapt the channel coding technique to suppress particular interferences. Key parameters such as data rate, channel and source coding, modulation schemes, and multiple access schemes can be adaptively tuned by software to obtain better communication quality. Thus, the software radio can cover broadband spectrums and support multiple wireless standards. The high digitization, excellent adaptive flexibility, and superior on-chip integration make software radio receiver a potential for the future broadband multi-standard communication.

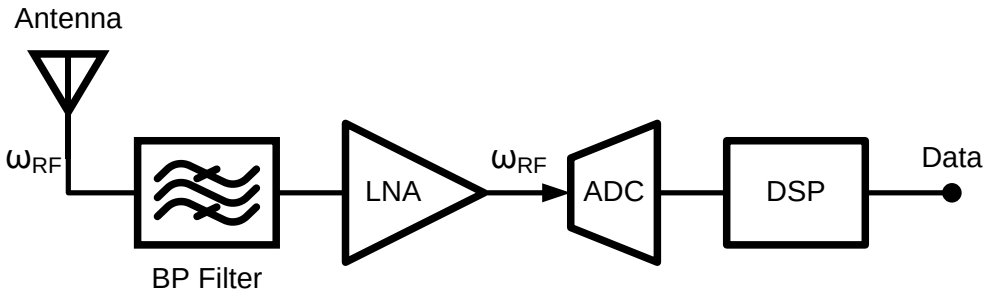


Fig. 2.11 Practical realization of software radio receiver.

2.4 Frequency Synthesizer

As presented in the previous section, a clock generator is a must in most wireless communications to up-convert or down-convert an informative signal. Frequency synthesizers that generate the programmable frequency to select the desired channel are ubiquitous in wireless transceivers. Usually, the core of frequency synthesizers is formed by a phase-locked loop (PLL). With a certain input reference frequency, usually provided by an off-chip temperature-controlled crystal oscillator (TCXO), a PLL can generate a programmable output frequency, rational times to the reference frequency.

2.4.1 Phase-Locked Loop

Oscillators are mostly utilized to provide a high performance clock in wireless transceivers. However, the clock frequency and phase of stand-alone oscillators can hardly be controlled and locked at a desired value. Therefore, a phase-locked loop (PLL), a negative feedback system, is used to solve the frequency and phase ambiguities of clock generation. Nowadays, PLLs have been widely used in almost all wireless transceivers.

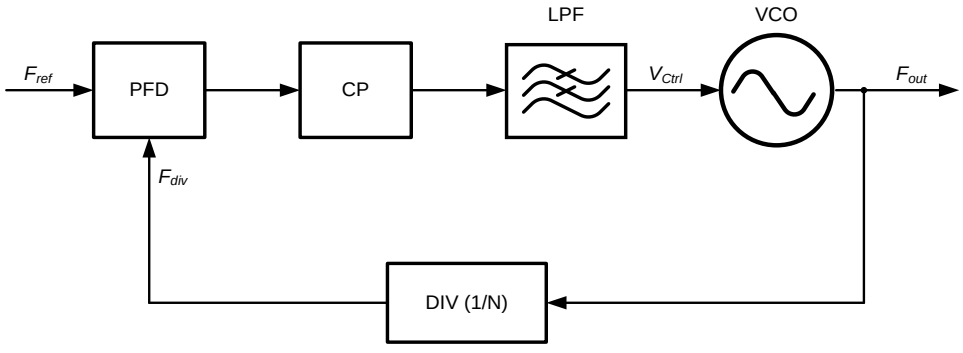


Fig. 2.12 Block diagram of a typical phase-locked loop.

Fig. 2.12 shows the block diagram of a charge-pump-based analog phase-locked loop which consists of a phase/frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO), and frequency divider (DIV). The PFD senses the phase error (the phase difference between the input reference clock and the output clock of dividers) and generates an analog signal proportional to the phase error. The charge pump converts the analog signal to charges integrated by the loop filter. The control voltage of the loop filter varies with the integrated charges based on the phase error continuously integrated; therefore, adjusts the output frequency of the VCO. The frequency dividers convert the VCO output frequency down and feedback the output clock of dividers to the PFD for comparing the frequency and phase with the reference clock. Ideally, when a PLL system is locked, phase difference between the reference clock and feedback clock should be a zero or fixed phase error existing. Usually, the reference clock is provided by an off-chip crystal oscillator (OSC). The output frequency of the oscillator (F_{out}) is a multiplication of the reference frequency (F_{ref}):

$$F_{out} = N \cdot F_{ref} \tag{2.1}$$

where N is the division ratio of dividers. It should be noticed that N can be integer or fractional and in most wireless communication applications N has to be programmable. Although the practical behavior of PLLs is non-linear and time-variant, time-invariant linear models are usually capable enough to describe the PLL system performance. However, the time-domain simulation, a time-consuming approach, would be necessary to accurately demonstrate the performance of a PLL system and each building block. The

more detail of PLL system design and system behavior model simulation can be found in [15, 16].

Table 2.3 Comparison of major WLAN standard specifications.

Standard	RX Band (MHz)	Channel Spacing	Frequency Accuracy	Phase Noise (dBc/Hz)
GSM	925-960	200 KHz	0.1 ppm	-118@0.6 MHz -128@1.6 MHz -138@3 MHz
DCS1800	1805-1880	200 KHz	0.1 ppm	-119@0.6 MHz -129@1.6 MHz -136@3 MHz
WCDMA	2110-2170	5 MHz	0.1 ppm	-108.8@7.6 MHz -120.8@15 MHz -150@130 MHz
Bluetooth	2400-2484	1 MHz	75 KHz	-81@1 MHz -111@2 MHz -121@3 MHz
802.11a	5170-5350 5725-5850	20 MHz	20 ppm	-90@10 KHz -100.2@20 MHz -116.2@40 MHz
802.11b	2400-2483.5	25 MHz	25 ppm	-90@10 KHz -121@14 MHz
802.11g	2400-2484	25 MHz	25 ppm	-90@10 KHz -100.2@20 MHz -116.2@40 MHz

2.4.2 Design Issues of Frequency Synthesizers

The specifications of frequency synthesizer are different in various wireless standards. Table 2.3 listed the specifications of the frequency synthesizer in most common wireless communication standards. These specifications bring a lot of design issues, and this section will discuss the most common design issues of frequency synthesizers.

- *Phase noise*:

  Phase noise is the most crucial and challenging specification in PLLs because worse phase noise would significantly degrade the receiver SNR. The definition of phase noise is the ratio between the total carrier power and the noise power found in a 1 Hz bandwidth at a frequency offset, f_m, from the carrier. The expression of phase noise is

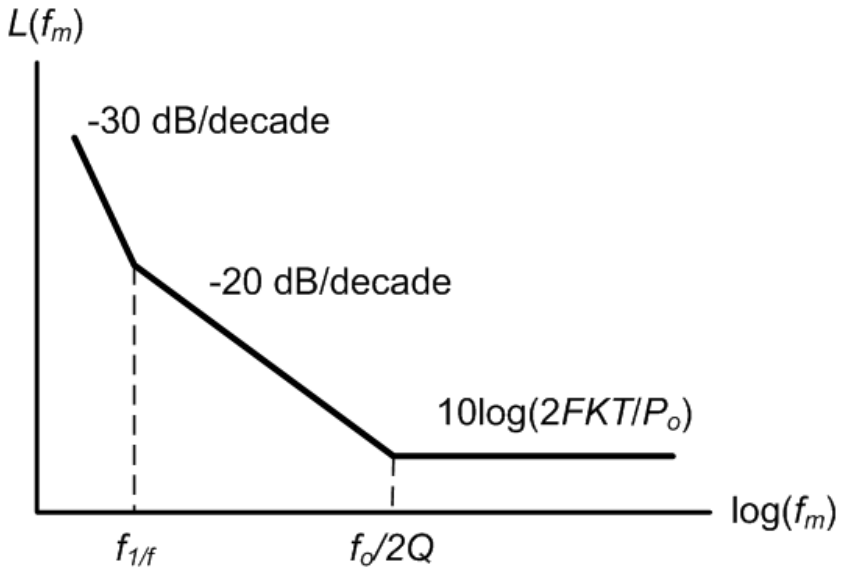
$$L(f_m) = 10\log\left(\frac{power\ in\ 1\,Hz\ bandwidth\ at\ f_m\ frequency\ offset\ from\ carrier\ f_o}{total\ carrier\ power}\right) \tag{2.2}$$

  where $L(f_m)$ is the phase noise in units of decibel per hertz (dBc/Hz), and f_o is the oscillating frequency. The phase noise spectrum in practical oscillators can be described in a first order approximation by Leeson's model:

$$L(f_m) = 10\log\left[\frac{2FKT}{P_o}\left(1+\frac{f_0^2}{4Q^2 f_m^2}\right)\left(1+\frac{f_{1/f}}{f_m}\right)\right] \tag{2.3}$$

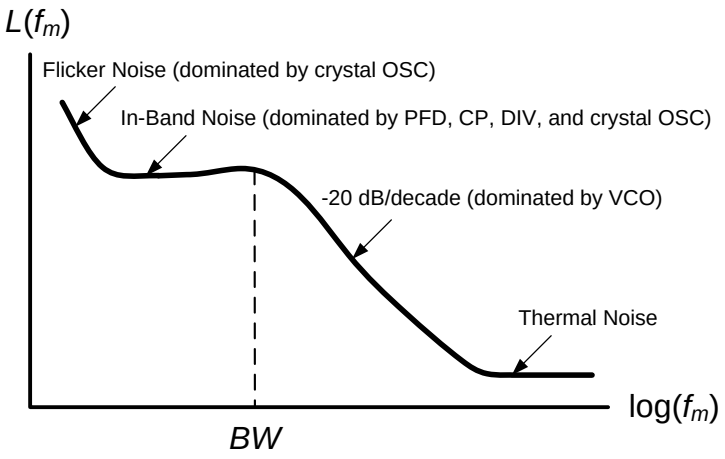
  where F is the excess noise factor, K is the Boltzmann constant, T is the absolute temperature, P_o is the power of carrier signal, Q is the quality factor of the LC tank, and $f_{1/f}$ is the corner frequency of flicker noise. The phase noise of oscillators can

be modeled by the impulse-response-based approach [17] or the phasor-based approach [18]. Fig. 2.13(a) shows the typical phase noise spectrum of oscillators while a phase noise spectrum of a PLL is shown in the Fig. 2.13(b). It should be noticed that the VCO noise contribution in a PLL is high-pass filtered but the PLL closed loop gain for the noise contributed from PLL reference clock, PFD, CP and DIVs is a low-pass characteristic. Thus, the PLL phase noise spectrum is dominated by VCO noise at the offset frequency much higher than the loop bandwidth while the PLL in-band (close-in) phase noise is mostly dominated from the PFD, CP, DIVs and crystal oscillator. Managing the bandwidth to compromise the contribution from various noise sources is important to optimize the jitter performance.



(a)

Fig. 2.13 Phase noise of (a) oscillator, (b) phase-looked.



(b)

Fig. 2.13 Continued.

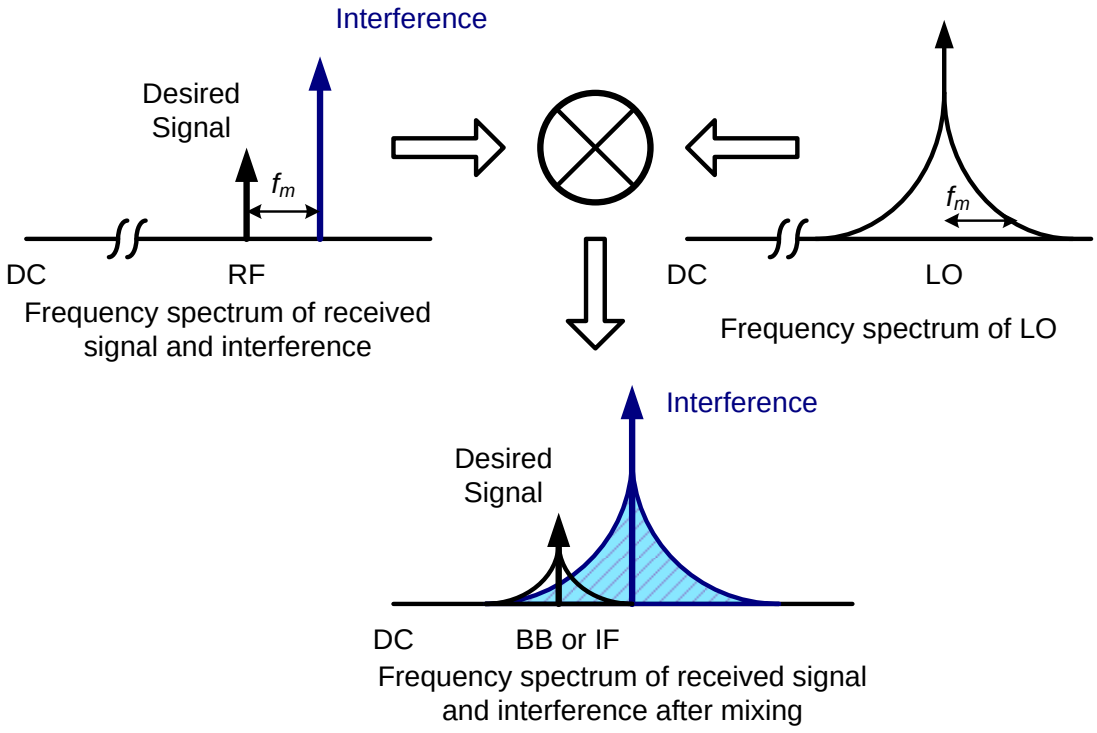


Fig. 2.14 Reciprocal mixing.

Fig. 2.14 illustrates the SNR degradation of a receiver system due to the phase noise of a local oscillator (LO) clock. In an RF receiver, the desired signal at RF is down converted to a baseband or an intermediate frequency (IF) by a mixer driven by the LO. The phase noise appears as a skirt shape centered at the carrier signal in the frequency spectrum. Suppose a strong interference (blocker) is located at an offset frequency f_m higher than the desired frequency (IF) by a mixer driven by the LO. The phase noise appears as a skirt shape centered at the carrier signal in the frequency spectrum. Suppose a strong interference (blocker) is located at an offset frequency f_m higher than the desired signal in the receiving path. The interferer modulates the phase noise at the offset frequency f_m higher than the clock center frequency and then the resulting product falls at the frequency the desired signal located; therefore, the desired signal would be corrupted by the phase noise. This effect is called reciprocal mixing and the phase noise has to be low enough to achieve a good system SNR [10, 19]. In RF transmitters, good phase noise will give a greater margin for the non-linearity in a PA. Also, the phase noise could increase the spectral emissions so the output spectrum of local oscillators must meet a mask requirement.

Lowering division ratio, increasing the charge current and fundamentally reducing the noise contribution from PFD, CP and DIV can improve the in-band phase noise of PLLs. To improve the phase noise at offset frequencies higher than PLL bandwidth, reducing the phase noise of oscillators is most critical.

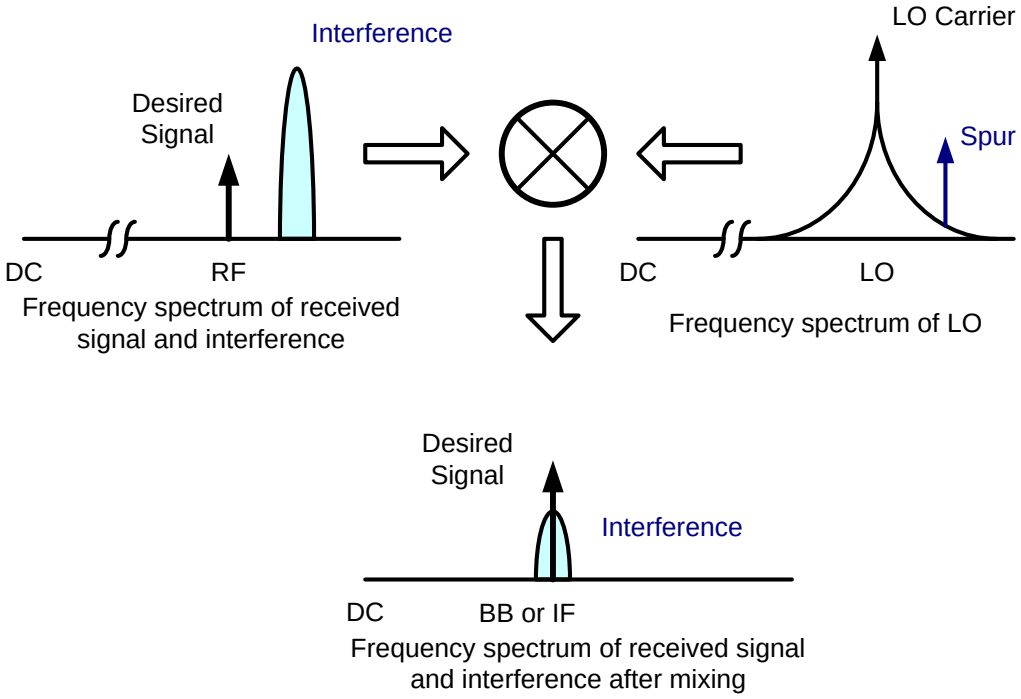


Fig. 2.15 The effect of spur degrading the SNR.

- *Spur*:

Spurious tones can be observed at offset frequencies deviated from the LO carrier frequency in the frequency spectrum of the LO clock as shown in Fig. 2.15. The formation of spurious tones in the frequency spectrum is from the periodical patterns/ripples in time-domain at the control voltage of the loop filter. These time-domain periodical patterns modulate the VCO frequency and then reside at the offset frequencies. The generation of spurs could be due to reference clock feedthrough, charge pump current mismatch, charge injection, leakage currents, mismatched propagation delay in PFD/CP up and down signals, fixed

phase error in PFD, ripples coupled from any clocks at control voltage or at ground and power supply, and fractional division operation. The effect of spurs in wireless transceiver is very similar to the phase noise. The desired signal would suffer from the SNR degradation after mixing operation because the interferers could mix with spurs and then translate to the frequency band of interest. In a transmitter, the spur levels must be low enough to ensure not to interfere with users in the same or a nearby channels.

The ratio of the power of the reference spur tone to the carrier power can be expressed as

$$Spur\left(dBc\right) = 20\log\left(\frac{\Delta V_{Ctrl} \cdot K_{VCO}}{2 \cdot F_{ref}}\right) \tag{2.4}$$

where ΔV_{Ctrl} is the peak amplitude of the ripple at the control voltage, K_{VCO} (Hz/V) is the VCO gain, and the F_{ref} is the reference frequency. A higher reference frequency and narrow PLL loop bandwidth gives a better spur performance. However, the higher reference usually leads to a larger frequency step and a narrow PLL bandwidth harms the settling time.

- *Frequency range*:

  Although most wireless standards are not wideband, while integrating several standards in one single chip, the wide frequency tuning range may be required. In addition, TV-tuners require an over 800 MHz frequency range and ultra-wide-band transceivers may require an over 8 GHz clock span. It is challenging to perform excellent performance in a wide frequency range.

- *Settling time (Locking time)*:

The lock time, also called settling time, acquisition time, or tracking time, is the time for a PLL to jump from one specified frequency to another specified frequency within a given frequency or phase tolerance. The lock time has to be smaller than the specification under the testing with the maximum frequency step in the allocated frequency band. The lock time, used to achieve the frequency locked, is valuable time that cannot be used for transmitting or receiving data. Hence, the lock time reduces the effective data rate achievable. Most PLLs in RF communication are required to have a lock time in the 0.1 to 1ms range. A larger PLL loop bandwidth will shorten the lock time. The total acquisition time, combining phase acquisition time t_{phase} and frequency acquisition time t_{freq}, can approximately be expressed as [15]

$$t_{phase} + t_{freq} = \frac{4.0}{\omega_n} + \frac{4.2(\Delta f)^2}{\left\{\frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)\right\}} \tag{2.5}$$

where ω_n is the nature frequency, Δf is the frequency step, and ζ is the damping factor. The more detail and discussion of lock time can be found in [15].

- *Bandwidth*:

The PLL loop bandwidth is a very important design parameter, significantly influencing the PLL performance. Bandwidth can compromise the phase noise contributed from additive noise sources. A larger bandwidth will shorten the locking time but increases the risk of loop instability. The reference

clock is usually 10 times higher than the bandwidth to ensure the loop stability. It should be noticed that the linear approach to analyze the nonlinear PLL system is effective when there is a high sampling ratio of reference clock frequency to the loop bandwidth. While the ratio is lower than 5, the linear approximation in system simulation may not accurately describe the real behavior of a PLL, accordingly, lead to errors to predict the stability of a PLL.

- *Integral and fractional division ratio*:

  The frequency step of an integral-N PLL is limited to the frequency of reference clock. While a small frequency step is required in a high-frequency PLL, a large division ration needed would increase the in-band noise because the noise at PFD/CP is multiplied to a ratio of $20\log N$ to appear at the PLL output frequency spectrum. Also, a narrow bandwidth required for smaller reference frequency would pay for an intolerably lengthy lock time. Fractional-N PLLs not only allow a larger reference clock frequency but also provide finer frequency spacing. Thus, the lock time and reference spur performance can be better in fractional-N PLLs due to a larger reference clock used. However, the fractional-N PLLs cause the generation of fractional spurs, mostly larger than the typical reference spur. Giving a better spur performance, the sigma-modulator implemented in the fractional-N PLLs can provide the averaging function (randomize the periodical phase error) and shape the quantization noise to higher frequencies [20]. However, the heavy digital circuitry and shaped quantization noise could contribute significant phase noise.

- *Stability*:

In a feedback system, phase margin is a key parameter to judge the loop stability. The phase margin is a function of bandwidth, pole locations and zero locations. In a type II PLL, to optimize the phase margin the bandwidth of loop gain can be designed as

$$Bandwidth = \sqrt{f_p \cdot f_z} \tag{2.6}$$

where f_p is the non-DC first dominate pole and f_z is the zero in a PLL. Fig. 2.16 shows the Bode Diagram based on this design approach and the sensitivity of phase margin is minimized. Since the bandwidth, pole locations and zero location are process-dependent, the phase margin would vary drastically with key parameters as shown in Fig. 2.17. Therefore, it is better to design a phase margin at least larger than 60 degree to ensure the PLL stability.

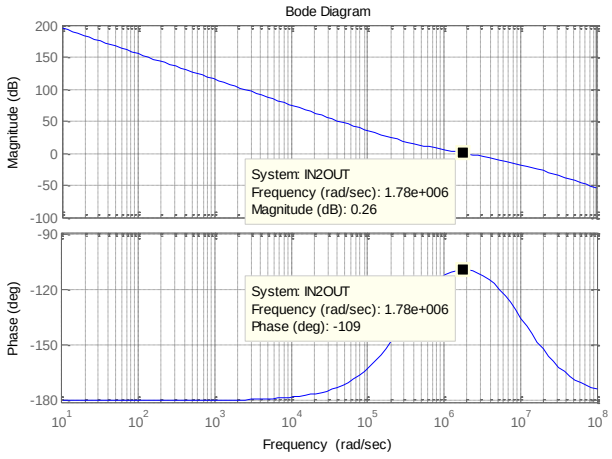
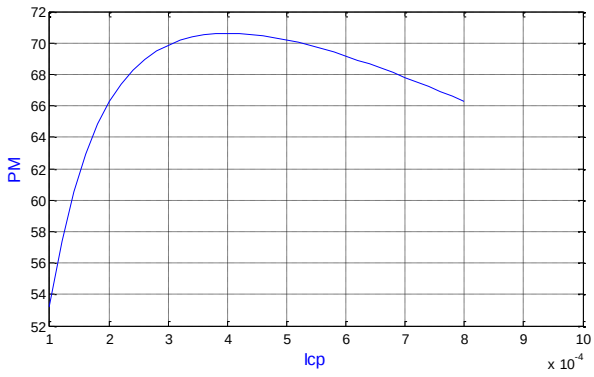
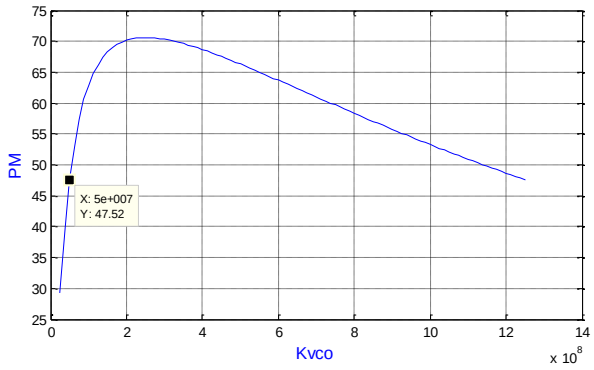


Fig. 2.16 Minimize the sensitivity of phase margin.



(a)



(b)

Fig. 2.17 Phase margin varies with (a) charge pump current, and (b) VCO gain.

- *Cost*:

  Low cost is always favorable in commercial RF IC design. Low cost means less power consumption, silicon area, and design complexity.

CHAPTER III

WIDEBAND FREQUENCY SYNTHESIZER FOR RF-TO-DIGITAL CONVERTER

3.1 Continuous-Time Band-Pass Delta-Sigma Analog-to-Digital Converter in Software Radio Receiver

Software radio receiver has been introduced as a potential architecture for the multi-standard broadband communications. In software radio receivers, the analog-to-digital conversion should occur as close to the antenna as possible to take the advantage of digital circuitry. The modulation/demodulation schemes, protocols, and equalization, are all determined in a software platform that runs in the digital signal processor (DSP). The ultimate goal is to digitize the RF signal at the output of the receive antenna at increasingly higher frequencies and wider bandwidths. The early digitization in the signal path eliminates the need for analog processing blocks, which theoretically results in significant reduction in power and silicon area. Software radio receivers not only perform the excellent ability of reconfiguration but also effectively minimize the cost. However, it is very challenging to digitize the RF signal received from an antenna and then processed by a BPF and an LAN at RF frequencies. The ADCs' requirement of a more than 10-bit resolution at several-gigahertz sampling frequency is very difficult to achieve in current CMOS technologies. The Nyquist-rate ADCs, such as flash, pipeline and successive approximation, may support up to GHz range, but the power consumption and achievable resolution are not acceptable. The performance of ADCs has become the bottle-neck of developing the software radio receivers.

Continuous-time (CT) Band-pass (BP) Delta-Sigma (ΔΣ) analog-to-digital converters have been acknowledged as one potentially ideal architecture for software radio receivers [6, 21]. Fig. 3.1 shows the architecture of broadband multi-standards software radio receiver using the CT BP ΔΣ ADC for digitizing the RF signals. The RF signals received from an antenna are first processed by an off-chip band-pass filter to remove/attenuate the unwanted out-of-band interferences. A high-linearity broadband low-noise amplifier (LNA) amplifies the RF signal up to the level that the followed ADC can process. The broadband multi-standards system requires a high linearity of LNA for mitigating the intermodulation of RF signals and the modulation between desired signal and interferences because those intermodulation products could fall into the signal bandwidth to degrade the SRN of system. The CT BP ΔΣ modulator directly converts the RF signals to the digitized data stream which can be demodulated and filtered by the digital signal processor. The wideband frequency synthesizer provides the sampling clock for the CT ΔΣ modulator to acquire the desired standard and channel.

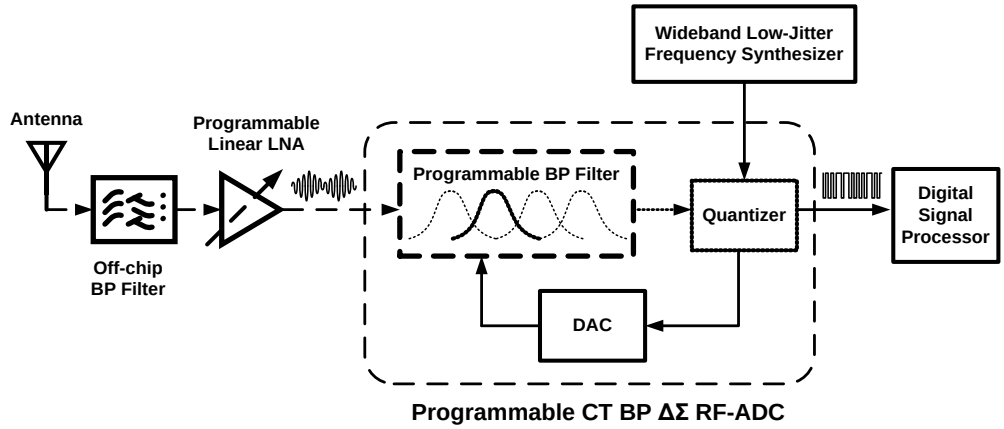


Fig. 3.1 RF Digitizer based on a band-pass continuous-time Sigma-Delta modulator.

The CT BP ΔΣ modulator consists of an N^{th} order continuous-time band-pass filter, a quantizer, and a DAC to form a closed feedback loop. The center frequency f_o of the band-pass filter is programmable/tunable to meet the required input RF signal frequency f_{RF} of various wireless standards. The desired information with a bandwidth f_b is enveloped within the RF signal ($f_b << f_{RF}$) and located around the center frequency of the band-pass filter. The sampling clock frequency f_s of the quantizer is just multiple times higher than the f_{RF} but several hundred times higher than f_b to obtain a high oversampling ratio of f_s to f_b in the CT BP ΔΣ modulator. The quantizer outputs a digitized data stream to DSP where the robust digital operations are executed. The DAC converts the digitized information back to analog domain and feedback the analog information into the input of CT BP ΔΣ modulator to form a closed loop. This negative feedback loop forms a band-pass transfer function for input signal while builds up a notch transfer function for quantization noise around the center frequency f_o.

The implementation of CT BP ΔΣ modulator in software radio receivers has several advantages. First, since the sampling operation is after the BP loop filter, the BP loop filter of CT BP ΔΣ modulator performs an inherent anti-alias filtering to relax the preceding filtering design of the ADC, to save both area and power consumption, and to minimize the effect of the out-of-band interferers. Second, the band-pass type signal transfer function and band-stop noise transfer function attenuate/shape the undesired noise and interference away from the band of interest to achieve excellent signal-to-noise ratio within the wanted narrow-band signal bandwidth. This unique feature is especially suitable for the wireless receiver where the narrow signal bandwidth is enveloped in the

high carrier frequency. Third, the receiver architecture avoids the use of analog mixing operations and base-band analog processors; instead, the robust digital operations dominate the signal processing. Besides, the continuous-time loop filter greatly improves the power consumption and enhances the signal bandwidth while compared with discrete-time switched-capacitor filter whose operation speed is usually limited to the settling time of charge redistribution and power consumption is considerably huge due to the required large gain bandwidth product of amplifiers.

3.1.1 Design Challenges of CT BP ΔΣ Analog-to-Digital Converter for Broadband Software Radio Receiver

The performance of CT BP ΔΣ ADCs are limited to some non-idealities such as, clock jitter, comparator metastability, excess loop delay, element mismatches of the feedback DAC, linearity of DAC feedback charge, finite quality factor of the band-pass filter, spurious tone, and frequency and quality factor tuning range of the BP loop filter. Because of the more than GHz range sampling clock and the broadband property, clock jitter [22] and excess loop delay [23] are remarkably critical non-ideality to degrade the ADC's performance when CT BP ΔΣ ADCs used for broadband software radio receivers.

The clock jitter occurs at both sampling operation and feedback DAC output as shown in Fig. 3.2. The sampling uncertainty due to clock jitter is mostly shaped outside the signal bandwidth by the loop characteristic so the sampling uncertainty has ignorable influence on SNR. However, clock jitter at DAC clock edges causes random

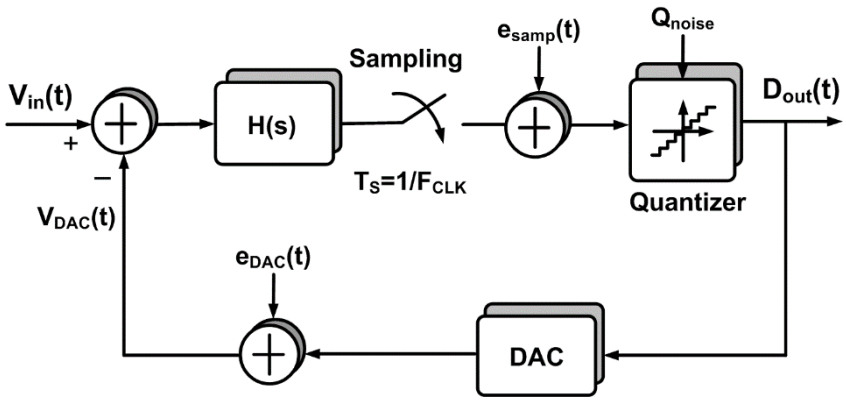
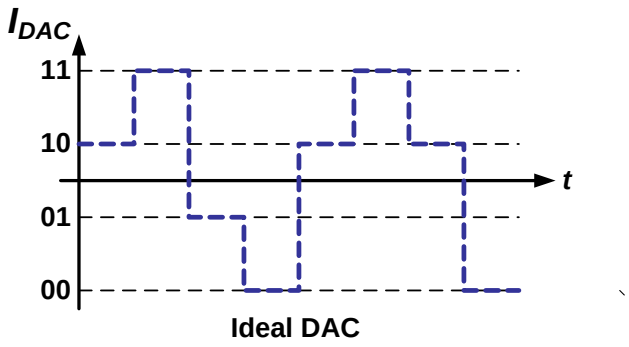
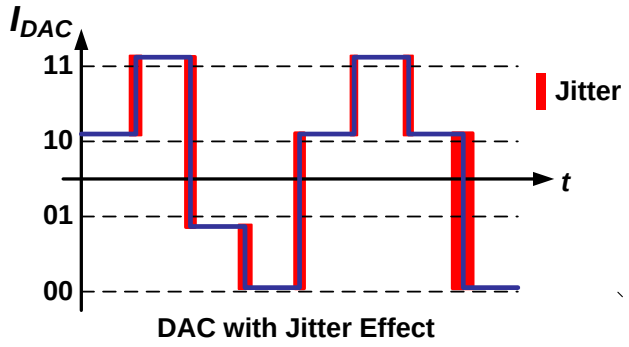


Fig. 3.2 Jitter behavior model of CT BP ΔΣ ADCs.



(a)



(b)

Fig. 3.3 DAC output waveform: (a) ideal case and (b) practical case with clock jitter.

variation of the integrated charge/voltage at the input of the loop filter. Fig. 3.3(a) shows an ideal two-bit DAC output waveform and Fig. 3.3(b) shows the practical DAC output waveform with clock jitter. Same as the input signal, the jitter-induced random variation of the integrated charge will be processed by the signal transfer function and presented at the output spectrum so the jitter noise results in the SNR degradation. It has been reported that a multi-bit non-return-to-zero (NRZ) DAC can relax the requirement of the clock accuracy.

Ideally, a DAC starts to inject current pulse into CT BP filter exactly when the sampling operation occurs so there is no delay between the sampling instant and the DAC current pulse. However, because of the finite switching time of transistors and the RC delay in the feedback path, the practical DAC current pulse is delayed in time. The delay between ideal DAC current pulse and real DAC current pulse is referred to excess loop delay. The excess loop delay modifies the loop transfer function and most importantly degrades the SNR of CT BP ΔΣ ADCs. The excess loop delay which increases the order of modulator may lead to the stability issue. Usually, one clock period delay would be purposely designed in the feedback loop to absorb the excess loop delay and accordingly to modify the transfer function of the CT BP ΔΣ ADC as shown in Fig. 3.4. In the broadband CT BP ΔΣ ADC, the excess loop delay has to be flexibly tunable to satisfy the requirement of one clock period which varies drastically to meet different wireless standards. Also, the PVT variation results in the uncertainty of excess loop delay. Fig. 3.5 shows the SNR vs. excess loop delay. It is evident that the excess loop delay can severely degrade the SNR and a design acquiring tunable excess loop delay to optimize the SNR

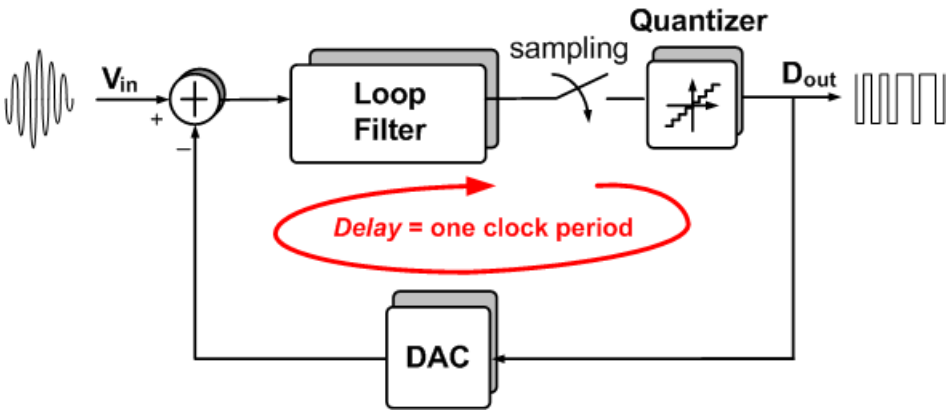


Fig. 3.4 One clock period delay in feedback loop.

Fig. 3.5 SNR vs. excess loop delay.

of ADC is necessary.

The output spectrum of clock generator usually has unwanted spurious tones. Those spurious tones would be from the non-linearity of clock signals, the PLLs' reference and fractional spurs and the coupling/modulating from the unwanted clocks. In the CT BP

ΔΣ ADC, these spurious tones modulates the input RF signals or interference and the intermodulation product could fall into the signal band and thus degrade the ADC's performance as shown in Fig. 3.6. Minimizing the spurious tones is essential for a broadband CT BP ΔΣ ADC.

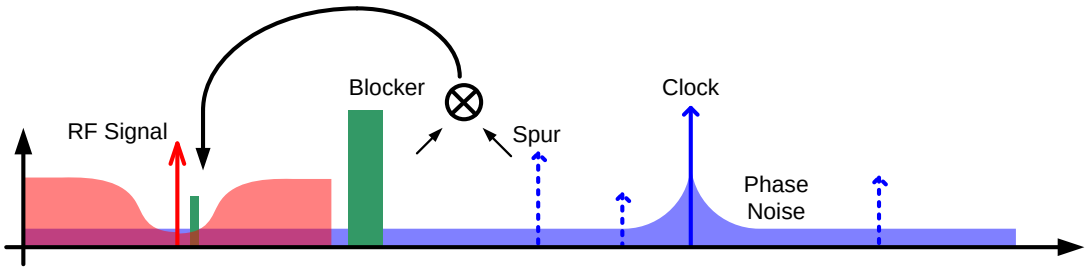


Fig. 3.6 The convolution product falling in signal bandwidth and degrading ADC SNR due to that spurious tones and phase noise convolve with quantization noise and blocker.

3.1.2 Design, Motivation and Objective of wideband Frequency Synthesizer in CT BP ΔΣ RF-to-Digital Converter

The frequency synthesizer acting as the sampling clock generation is the substantially critical building block in the CT SD ADC-based software radio receiver. For the broadband multi-standards software radio receiver, the frequency synthesizer has to output the frequencies several times higher than the signal frequencies, cover a frequency range more than a decade for multi-standards, and perform low-jitter and excellent SFDR. A tunable excess loop delay is also required optimizing the SNR and assuring the stability. These issues motivate the exploration and development of frequency synthesizer design. The objectives of the research are listed as below.

- Design a frequency synthesizer which can cover the frequency range more than a decade to support the software radio receiver used for multi-standard applications.
- Improve the purity of sampling clock to achieve excellent SJNR of CT BP ΔΣ ADCs and make the BP ΔΣ ADCs less sensitive to clock jitter.
- Design a delay-tunable clock generation/distribution network to adjust the excess loop delay to achieve optimized SNR for broadband system.
- Remove/attenuate the spurious tones to avoid the intermodulation products degrading the system SNR.
- Minimize the power consumption, circuit complexity and cost of frequency synthesizer.

3.2 2 – 16 GHz Broadband Frequency Synthesizer in *BP ΔΣ RF-to-Digital Converter*

Fig. 3.7 shows the architecture of a broadband software radio receiver realized by an LNA, a programmable ΔΣ modulator and a wideband frequency synthesizer. In the BP CT ΔΣ modulator, the programmable band-pass filter is implemented by two resonators (LC tanks) in which channel selection can be done by varying the resonance frequency of the resonators. As shown in Fig. 3.8, the inductors are fixed and programmable banks of capacitors are used for this channel selection. A 2-bit flash ADC is used as the 2-bit quantizer since this approach reduces the quantization noise by 6 dB and improves system stability.

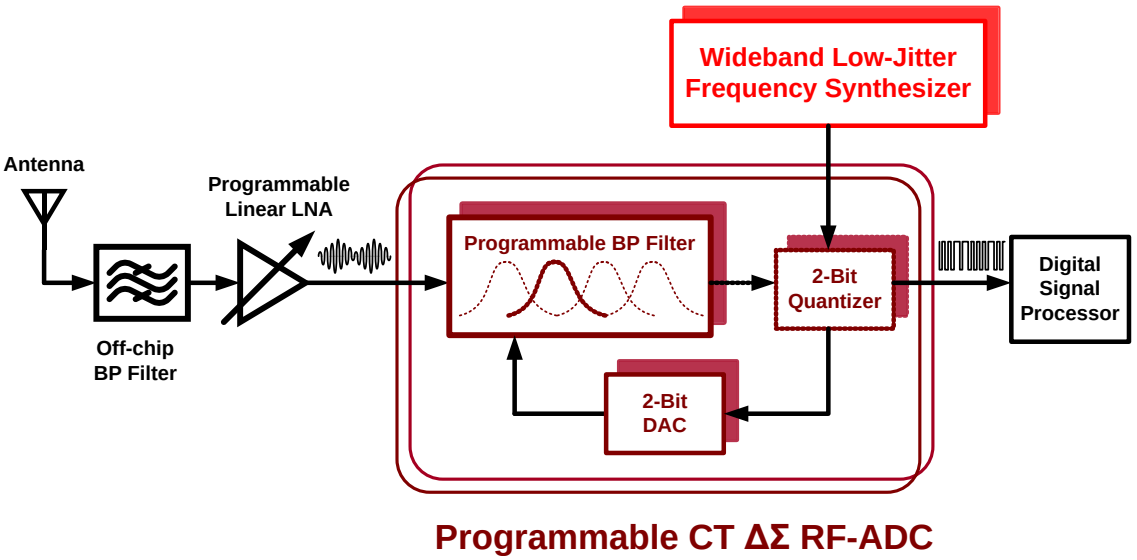


Fig. 3.7 RF Digitizer based on a band-pass continuous-time Sigma-Delta modulator.

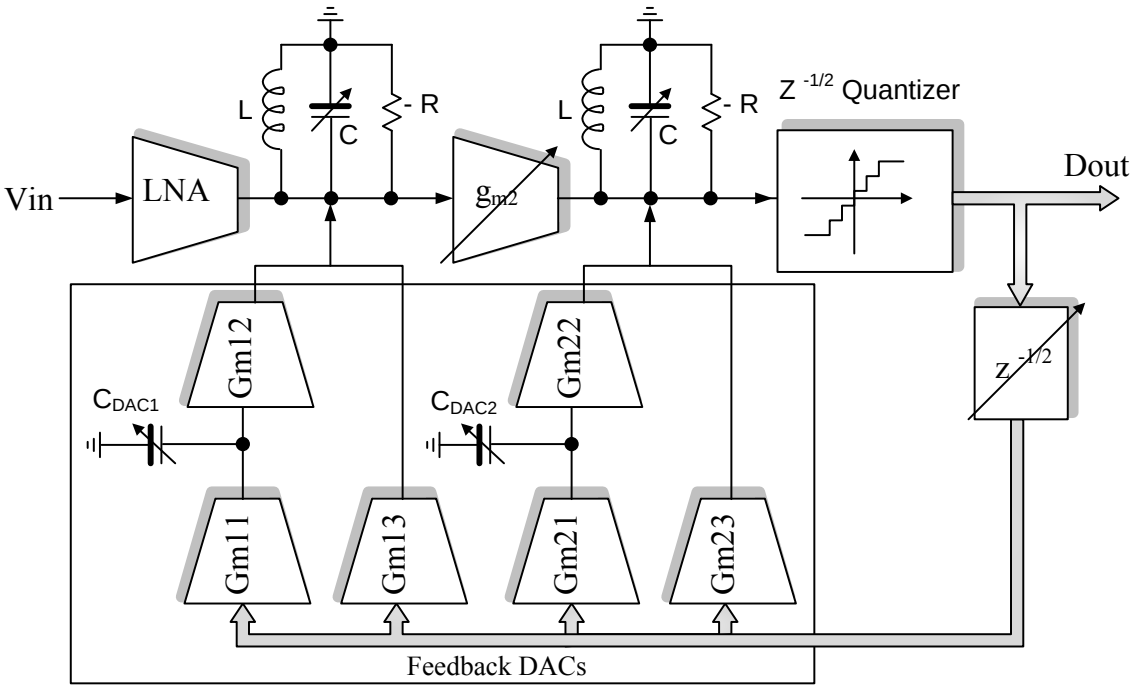


Fig. 3.8 CT BP ΣΔ ADC system Level block diagram.

A frequency synthesizer provides the sampling clock for the quantizer to select the desired channel. Choosing the clock frequency four times higher than the input RF carrier, the digitization of channels in the range of 0.5 – 4 GHz require the clock frequency to be in the range of 2 – 16 GHz. Based on system simulation, the clock jitter of this frequency synthesizer must be under 0.6ps to achieve 10-bit resolution in a 20MHz channel bandwidth. Since the loop filter provides limited blocker attenuation, the clock spurious tones convolve with the out-of-band channels. Parts of the resulting signals fall in-band and then degrade the system SNR. Therefore, the ratio of the power of the main clock signal to the power of the spurious tones must be > 40dB.

Fig. 3.9 shows the proposed 2 – 16 GHz integer-N frequency synthesizer. The type-two fourth-order charge-pump-based PLL outputs 10 – 12.8 GHz quadrature clocks. A single-sideband (SSB) mixer is used to expand the clock frequency range by means of the feed-forward and regenerative mixing techniques to get more than 100% frequency range while maintaining low jitter performance. In order to generate a low-jitter clock, a low-noise quadrature voltage-controlled oscillator with low I/Q phase mismatch is developed as the core of the phase-locked loop (PLL)-based frequency synthesizer to covering around 25% frequency tuning range. The QVCO design will be discussed in the next chapter.

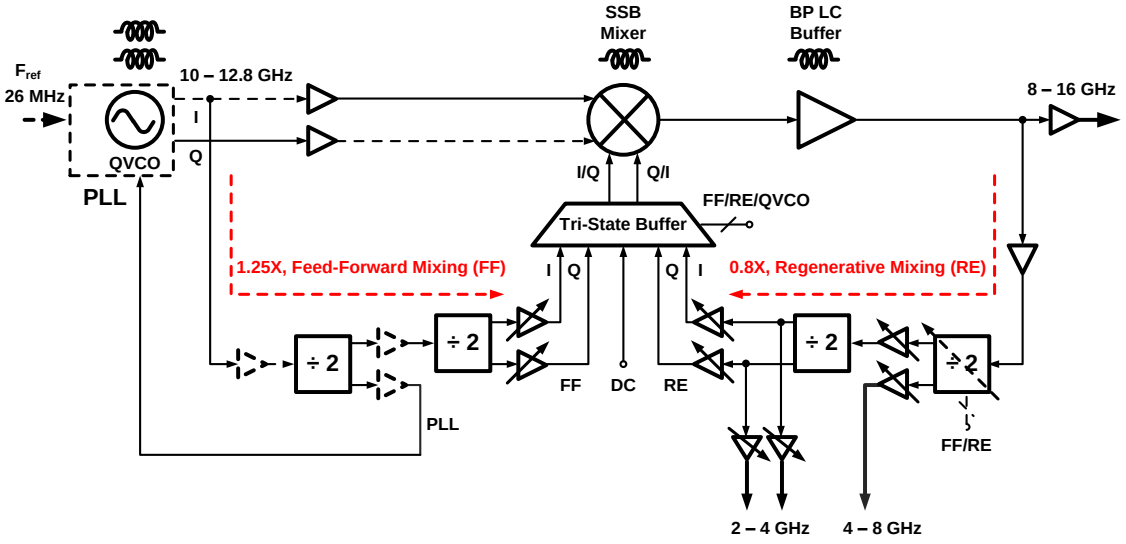
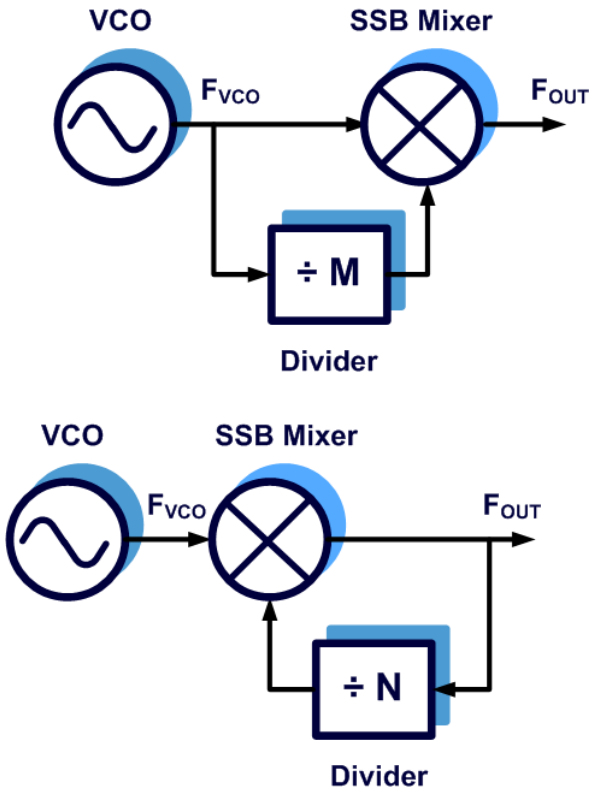


Fig. 3.9 Architecture of the proposed 2 – 16 GHz frequency synthesizer.

3.2.1 SSB-Mixer-Based Frequency Expansion Technique

It is known that a wider VCO frequency tuning range leads to a worse VCO phase noise due to the lower quality factor of LC tank. Thus, considering the fundamental trade-offs between the frequency range and noise performance in clock generation systems, SSB mixers would be attractive and show potential benefits for widening the frequency tuning range without sacrificing the phase noise/jitter performance. As shown in Fig. 3.10, a SSB mixer can add or subtract the fundamental or the harmonic frequency of any two clocks due to the frequency mixing operation to generate and expand the wanted output clock frequency which is usually selected by an analogy filter. Fig. 3.10(a) shows a feed-forward mixing by which the frequency output can be expressed as



(a) (b)

Fig. 3.10 Frequency conversions by (a) feed-forward mixing and (b) regenerative mixing.

$$F_{OUT} = \left(\frac{M \pm 1}{M} \right) F_{VCO} \tag{3.1}$$

where M is the division ratio in the feed-forward mixing path. And the frequency generated by regenerative mixing can be expressed as

$$F_{OUT} = \left(\frac{N}{N \pm 1} \right) F_{VCO} \tag{3.2}$$

where N is the division ratio in the regenerative mixing.

A continuously wide frequency range more than a decade can be realized by a 100% frequency-range clock generator covering the high-end frequencies which can be translated and expanded to lower frequencies by frequency dividers. By means of combining the feed-forward and regenerative mixings, the 100% frequency range can be obtained as shown in Fig. 3.11. A and B are the ratios to expand the frequency range to higher and lower domains, respectively. α is the percentage that a VCO frequency range should be able to cover to satisfy the 100% frequency range. The requirements of A, B and α to avoid uncovered frequency gaps can be obtained by the following set of equations,

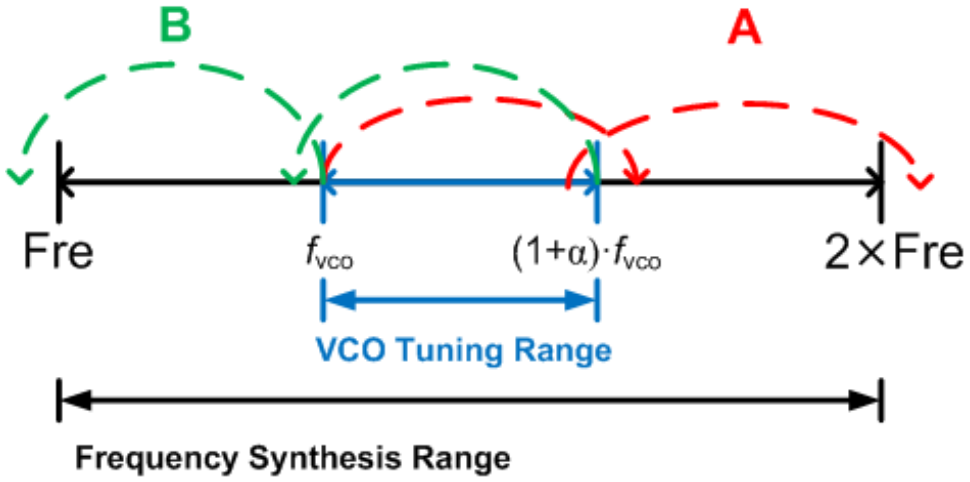


Fig. 3.11 100% frequency range generation.

$$\begin{cases} f_{vco} \times A < (1+\alpha) f_{vco} \\ (1+\alpha) f_{vco} \times A > 2Fre \\ (1+\alpha) f_{vco} \times B > f_{vco} \\ f_{vco} \times B < Fre \end{cases} \tag{3.3}$$

$$\Rightarrow (1+\alpha) > 2\left(\frac{B}{A}\right)_{\min} = 2(1+\alpha)^{-2}$$

where *Fre* is the lowest frequency the synthesizer has to cover and f_{vco} is the lowest frequency the VCO can cover. Since divide-by-two frequency blocks are usually easy to design and more efficient in terms of power consumption, area, and speed, it is better to use binary numbers for *M* and *N* ratios. Given *M* and *N* equal to 4, ratio A and ratio B will be 5/4 and 4/5 and then the required VCO tuning range α will be 25.9%. In current CMOS technologies, VCOs can cover this frequency range with good enough phase noise performance even though the very pessimistic process variation is given. It should be noticed that one SSB mixer can be shared by both feed-forward mixing and regenerative mixing.

Fig. 3.12 shows the simplified block diagram of the SSB mixer-based frequency band expansion architecture. The proposed QVCO integrated in a PLL-based frequency

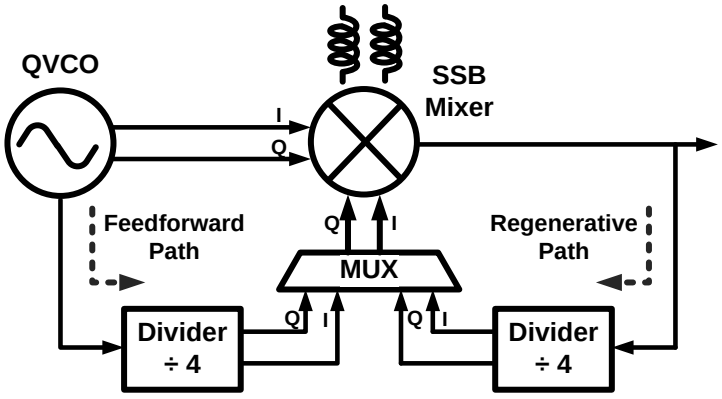


Fig. 3.12 Simplified block diagram of band expansion architecture.

synthesizer outputs a mid-frequency band, 10 – 12.8 GHz. The regenerative and feed-forward mixings are incorporated with the frequency synthesizer to achieve 100% frequency range. The low-frequency band, 8 – 10 GHz, is generated by the regenerative

mixing path which converts the input (mid-band) frequency to the low-frequency band by a ratio of 0.8. The high-frequency band, 12.5 – 16 GHz, is generated by the feed-forward mixing path which performs a frequency conversion by a ratio of 0.8. Current-mode-logic (CML) dividers are used to generate the required mixing frequency in either feed-forward or regenerative mixing path. A tri-state buffer works as the multiplexer to select either regenerative or feed-forward mixing path or act as a switch to turn off the mixing operation to allow the SSB mixer exhibits as a BP filter/buffer to output the mid-band.

The building block level of the entire band expansion architecture is shown in Fig. 3.9. Both the SSB mixer and band-pass (BP) *LC*-buffer provide the band-pass filtering and attenuation for the interference, spurs or phase noise at unwanted frequency range while amplify the clock signal at required frequency band. This band-expansion circuit design relaxes the concerns regarding the possible convolution between the blockers, spurs, and noise, so the ADC system is less influenced and vulnerable to the non-idealities from the frequency synthesizer. The dividers in the regenerative path are used for the further frequency extension to lower frequencies so the band-expansion circuits can output a frequency range from 2 to 16 GHz. The design of band expansion block saves considerable power and boosts the robustness of the ADC system.

3.2.2 False Frequency Locking in Regenerative Mixing

It is well known that the active feedback load of CML divider would lead to a self-oscillation. In the regenerative mixing path the first CML frequency divider would be also used as the first divider to down-convert the highest clock frequency generated from

the feedforward mixing, this CML divider has to be designed to have a self-resonant frequency at the half of the highest clock frequency to guarantee the functionality of this CML divider over temperature and voltage variation. However, when the regeneratative mixing is required, the divider which oscillates at its high resonant frequency would cause false locking issue. For example, when the frequency range from 6.4 to 8 GHz is required, the feed-forward mixing path is active and the first CML divider in the regenerative mixing path has to convert the output frequency range from 12.5 to 16 GHz into its half so ideally the self-resonate frequency of the CML divider should be designed as 8 GHz. However, when the regenerative mixing is active to generate an 8GHz output frequency from a 10GHz VCO clock as shown in Fig. 3.13, the CML divider could oscillate at the 8 GHz self-resonate frequency and then the second following divider translates

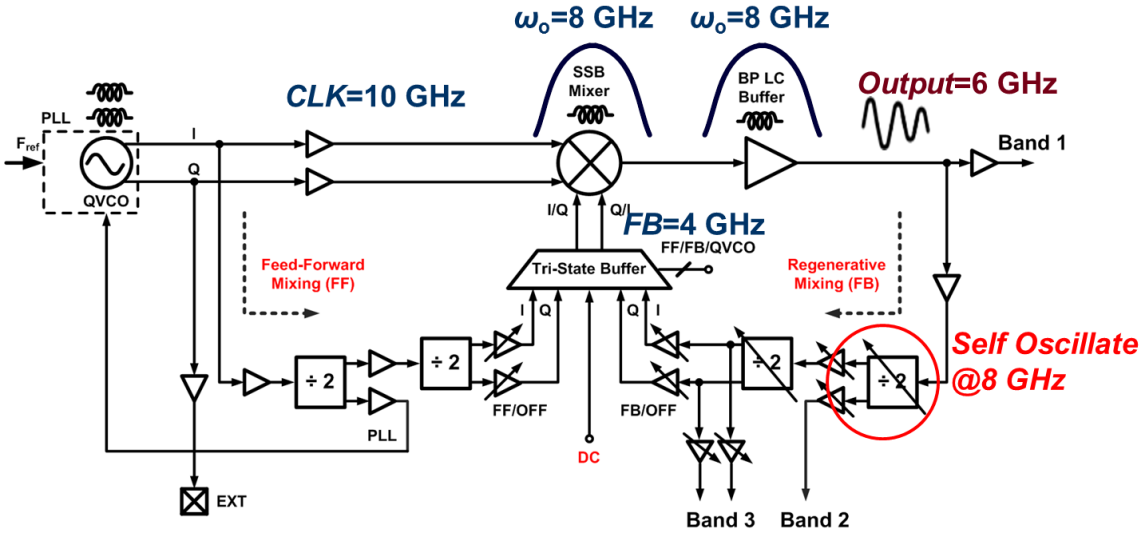
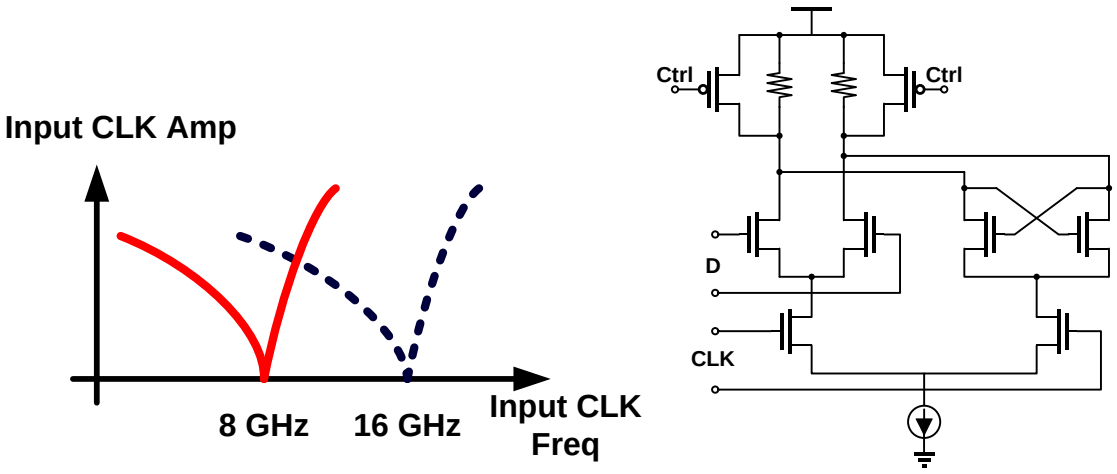


Fig. 3.13 False frequency locking in regenerative mixing path.



(a) (b)

Fig. 3.14 (a) Tunable self-resonate oscillation frequency of CML frequency divider; (b) schematic of CML divider with tunable resistor loading.

the frequency to 4 GHz. Therefore, the 6GHz output frequency of the SSB mixer would far deviate from an 8GHz pass-band of the SSB mixer and the output amplitude of SSB mixer would be too small to activate the division operation of the CML divider so the band expansion system would remain in the false locking condition as shown in Fig. 3.13.

In order to solve this problem, the CML frequency divider with tunable self-oscillation frequency is designed as illustrated in the Fig. 3.14(a). The resistive load of the latch in the CML divider consists of a resistor in parallel with a triode-region transistor as shown in Fig. 3.14(b). When the CML divider is required operating at high frequency, the triode-region MOS transistor provides a high self-resonate frequency. However, when the divider is operated forming the regenerative path, the triode-region MOS transistor is turned off and the CML divider operates with a lower self-resonate frequency would

oscillate at a frequency closer to the required frequency under proper frequency locking condition to avoid the false locking condition as shown in the Fig. 3.15.

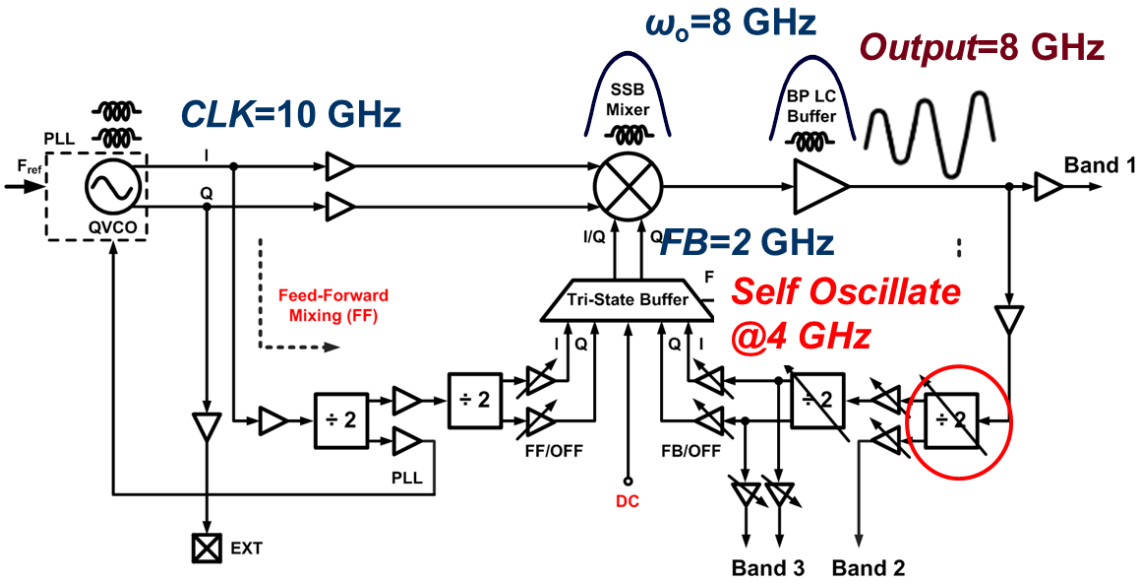


Fig. 3.15 Self-oscillation frequency of CML divider is tuned to avoid false locking.

3.2.3 Excess Loop Delay Control

The clocks generated by the proposed frequency synthesizer are used at the two-bit quantizer as the sampling clock at full frequencies which span from 4GHz to 16GHz, 4 times higher than the RF input signal. The excess loop delay has to be exactly one clock period T_{CLK} to ensure loop stability; accordingly, spanning from 62.5ps to 250 ps. The summation of loop delays given by quantizer, DAC, band-pass filter and routings should be close enough to T_{CLK}. This requirement of a wide and tunable excess loop delay is very challenging.

Fig. 3.16 shows the simplified block diagram of the two-bit NRZ quantizer. The pre-amplifier stage senses and amplifies the difference between the differential signals and reference voltages before the quantizer. It can also reduce the kickback noise from the output of the latched comparator. The latched comparator senses the output voltage of the pre-amplifier and regenerates it to logic voltage. The following latch stages are

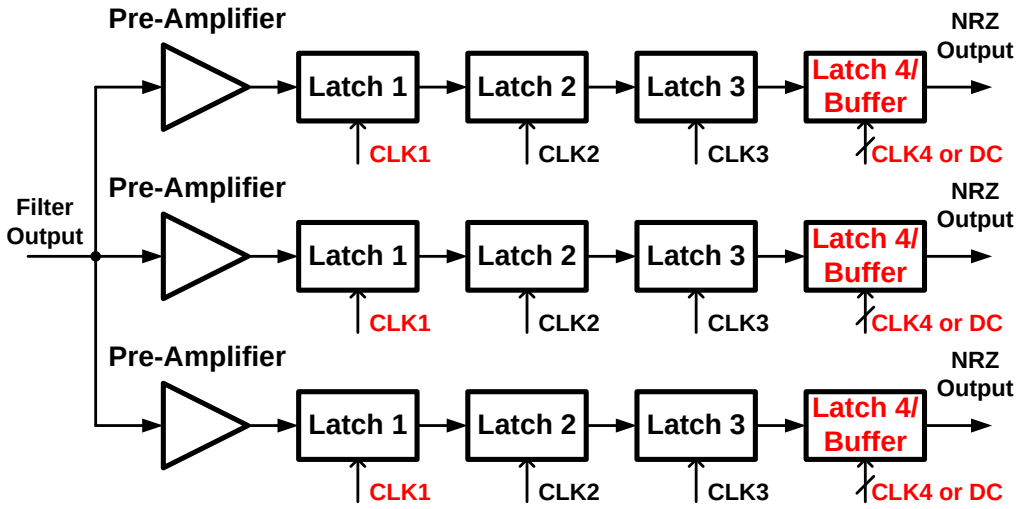


Fig. 3.16 Two-bit quantizer design.

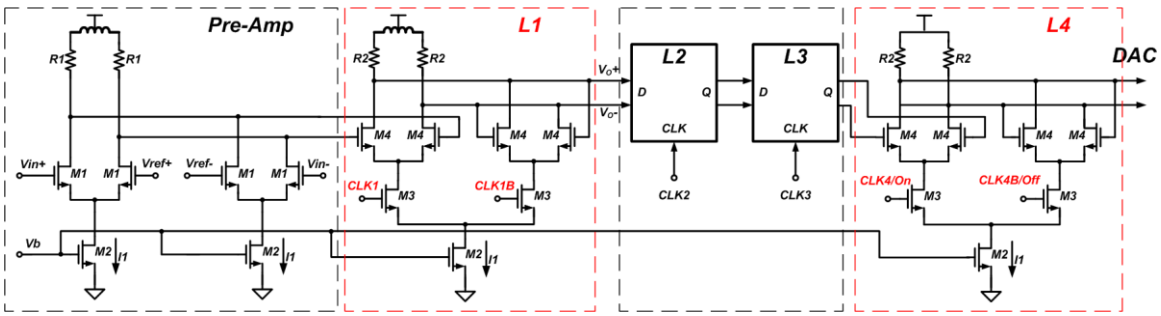


Fig. 3.17 Schematic design of quantization unit cell.

introduced to decrease the metastability issues and to make tunable the excess loop delay. The 2-bit quantization is recognized by the three unit bits in which a reference voltage is given in each pre-amplifier. Fig. 3.17 shows the design of each unit bit. The pre-amplifier is composed of two input differential pairs, load resistors and series peaking inductor. The differential pairs connect to the differential input signals and differential reference voltages directly. The pre-amplifier provides a finite DC gain to reduce the offset effect. However, the gain cannot be too high because of the Miller effect reducing the operation bandwidth. The bandwidth of the pre-amplifier should be high enough to reduce the signal delay. A series peaking inductor which improved the bandwidth by 50% is added at load to improve the bandwidth as shown in Fig. 3.17. A series peaking inductor is also added to increase the bandwidth in the first latch L1 while second latch L2 and third latch L3 do not use peaking inductors to extend the bandwidth.

The clocks CLK1, CLK2, CLK3, and CLK4 are the used in L1, L2, L3 and L4, respectively. The clocks CLK1 and CLK3 are in-phase but out of phase of CLK2 and CLK4. Define the total delay from DAC, band-pass filter and signal routing path as *TD* so the excess loop delay will be $T_{CLK} + TD$. Since *TD* is impossible to be zero delay, the

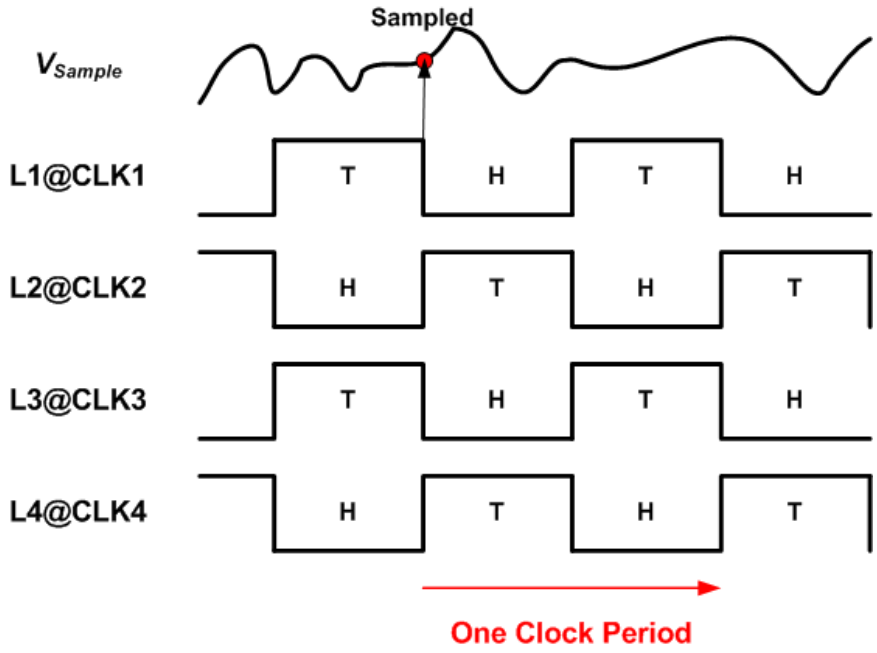


Fig. 3.18 Delay of quantizer without tunable delay control.

excess loop delay is definitely larger than the desired one clock period T_{CLK} as shown in Fig. 3.18.

In order to satisfy the requirement of excess loop delay, tunable delay control is implemented in L1 and L4. When the sampling clock frequency is low, 2GHz – 10GHz, a timing delay $\Delta T1$ is given in CLK1 and a timing advance $\Delta T4$ is given in CLK4 as shown in Fig. 3.19. The excess loop delay in this case can be expressed as

$$Excess\ Loop\ Delay = T_{CLK} - \Delta T1 - \Delta T4 + TD \tag{3.4}$$

The excess loop delay can be equal to one clock period T_{CLK} when $\Delta T1 + \Delta T4 = TD$. Usually, TD is around several tens ps so $\Delta T1$ and $\Delta T4$ are around 10 – 20 % of T_{CLK}.

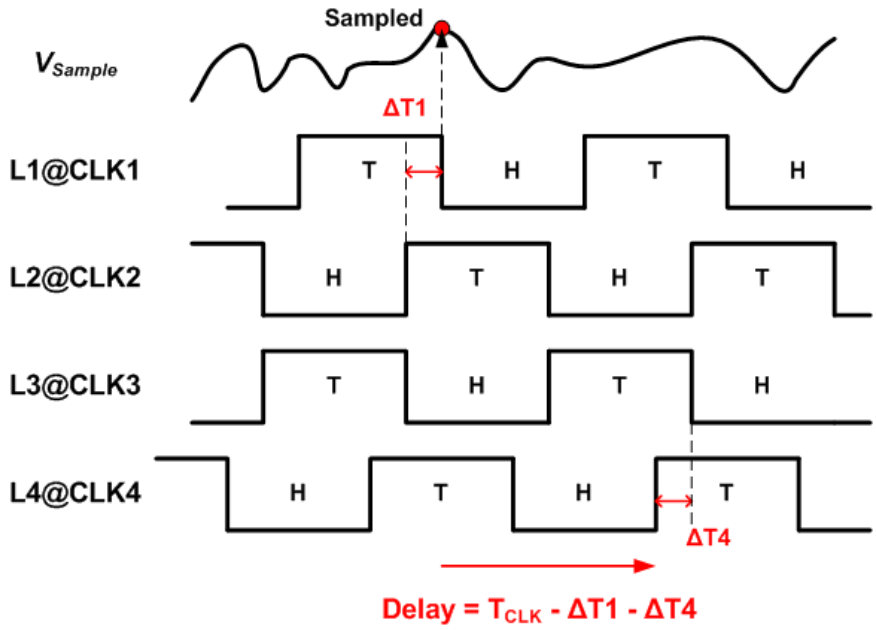


Fig. 3.19 Delay of quantizer with tunable delay control for low frequency operation.

However, when the sampling frequency is even higher, beyond 10GHz, $\Delta T1$ and $\Delta T4$ would not be acceptably small compared to T_{CLK}. While $\Delta T1 + \Delta T4 = TD$ is met, the quatizer cannot function well to properly recognize and amplifier the input signal. To satisfy the excess loop delay requirement beyond 10GHz sampling clock frequency, the active feedback part of L4 is turned off to obtain additional half clock period timing for the loop delay TD. As shown in Fig. 3.20, the excess loop delay can be expressed as

$$Excess\ Loop\ Delay = T_{CLK} + \Delta T1 + TD \tag{3.5}$$

It should be noticed that $\Delta T1$ can be either positive or negative depending on a timing delay or timing advance is required to meet the excess loop delay of one clock period. To satisfy this requirement, TD is equal to $T_{CLK}/2 + \Delta T1$.

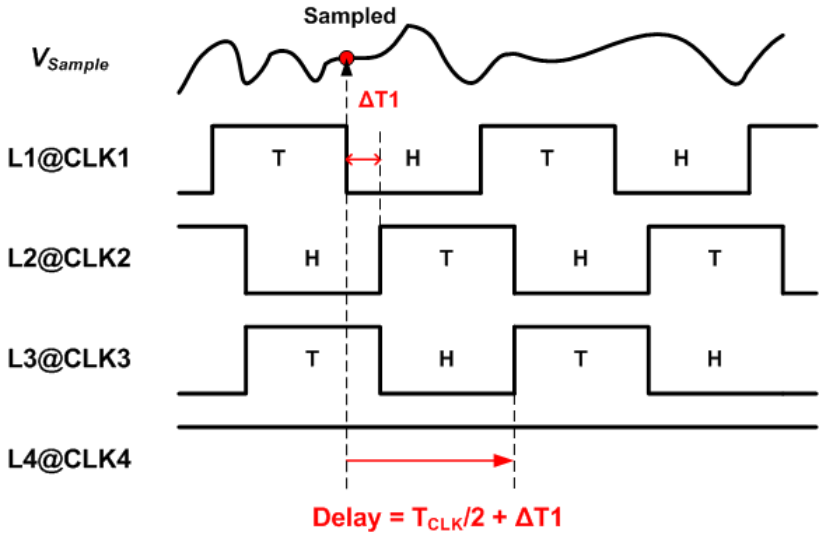


Fig. 3.20 Delay of quantizer with tunable delay control for high frequency operation.

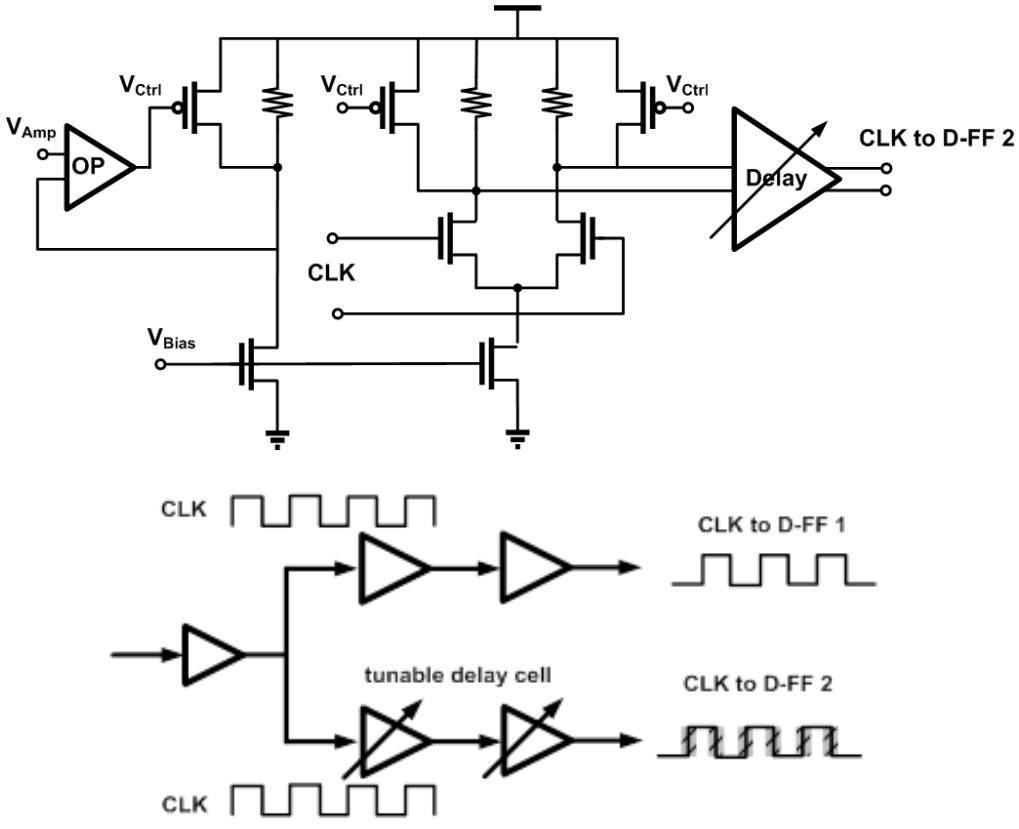


Fig. 3.21 Tunable delay cell with replica bias.

Fig. 3.21 shows the tunable delay cell with replica biasing circuitry. The delay can be controlled by the Vbias while the output swing amplitude of each delay cell can be controlled by V_{Amp} the replica bias circuit. This design can give ± 15% phase tuning.

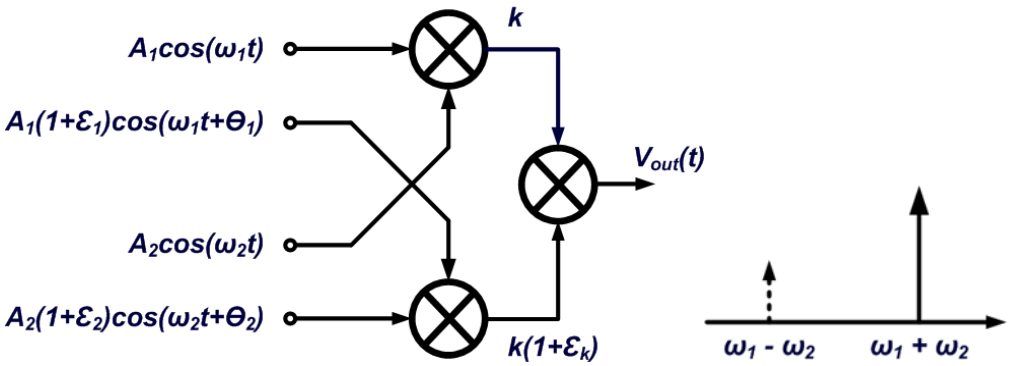


Fig. 3.22 Image sideband generation due to the I/Q mismatch

3.2.4 Low-noise Precise I/Q Phase Accuracy QVCO

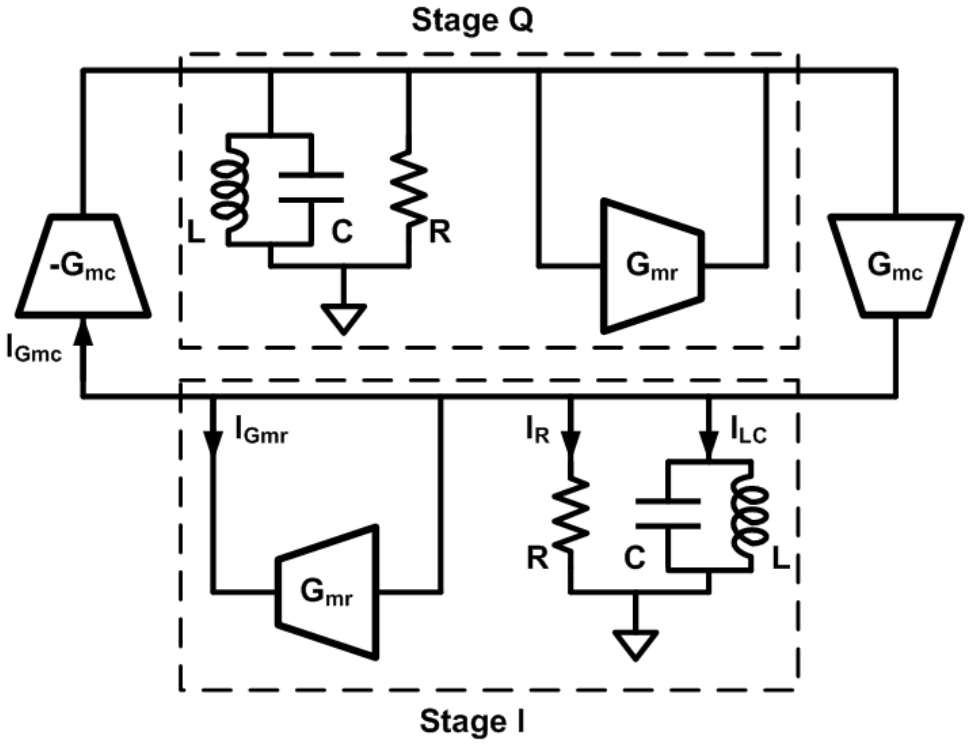
The quadrature voltage-controlled oscillator (QVCO) generates the I/Q phases for the SSB mixing. As shown in the Fig. 3.22, the phase and amplitude mismatches of the I/Q signals would produce the sideband image during the mixing operation and this sideband image can potentially convolve with the blockers to degrade the resolution of the ADC system, so a QVCO with low I/Q mismatch is desired. The sideband rejection can be expressed as

$$Sideband \quad rejection(dB) = 10\log_{10}\frac{1+2\frac{C_2}{C_1}\cos(\theta_1-\theta_2)+\left(C_2^2/C_1^2\right)}{1-2\frac{C_2}{C_1}\cos(\theta_1+\theta_2)+\left(C_2^2/C_1^2\right)} \tag{3.6}$$

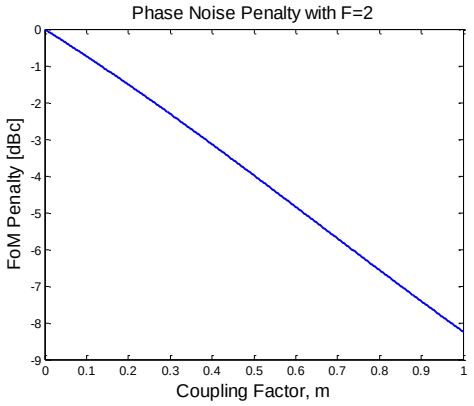
$$C_1 = kA_1A_2,\ C_2 = k(1+\varepsilon_k)A_1(1+\varepsilon_1)A_2(1+\varepsilon_2)$$

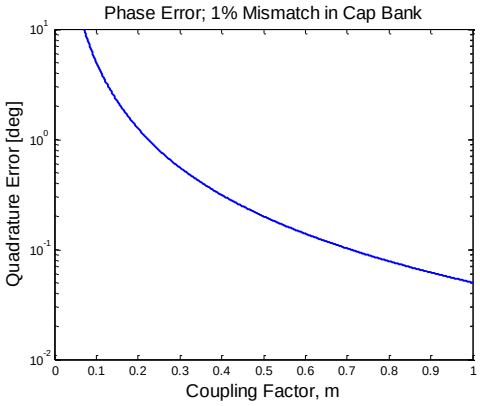
where A represents the signal amplitude and θ represents the phase. According to Eq. (3.6), a 1% phase mismatch and 1 % amplitude mismatch can generate a -40 dBc image sideband. Usually, I/Q phase mismatch results from the inherent device/component mismatch and asymmetric layout. Due to the limitation of process fabrication, the fact that a phase mismatch in a multi-gigahertz QVCO is more than several degrees usually produces considerable sideband image during the SSB mixing.

In a QVCO system, increasing the coupling factor, a ratio of the coupling transconductance, G_{mc}, to the negative-resistance transconductance, G_m, can better tolerate the mismatches between the two LC-VCOs. However, increasing the coupling factor to improve the phase mismatch comes with the phase noise penalty because the G_m and G_{mc} have 90 degree phase shift and this 90 degree phase shift causes a maximum current/noise of G_{mc} injecting into the oscillator at its most vulnerable zero-crossing timing. Fig. 3.23 shows the typical trade-off between the phase noise and phase mismatch in a QVCO system.



(a)





(b) (c)

Fig. 3.23 (a) A simplified block diagram of a QVCO; (b) phase noise vs. coupling factor; (c) phase mismatch vs. coupling factor.

As shown in the Fig. 3.24, a new QVCO is proposed to solve the dilemma of designing the coupling factor to manage the trade-off of the phase accuracy and phase

noise. In the proposed QVCO, since the coupling transconductance is out-of-phase controlled by a cascode topology which minimizes the injection current/noise of the G_{mc} during the zero-crossing of the oscillation to improve the phase noise. The design allows a larger coupling factor to improve the phase noise while not degrading the phase noise performance. Fig. 3.25 shows the simulated phase noise and phase accuracy vs. the coupling factor of the proposed and conventional QVCOs. Both phase noise and phase mismatch are improved in our proposed QVCO while increasing the coupling factor. The Monte-Carlo simulation shows the standard variation of the phase mismatch is less than 0.16 degree in our proposed QVCO. The more details of QVCO theory and design will be discussed in the next chapter.

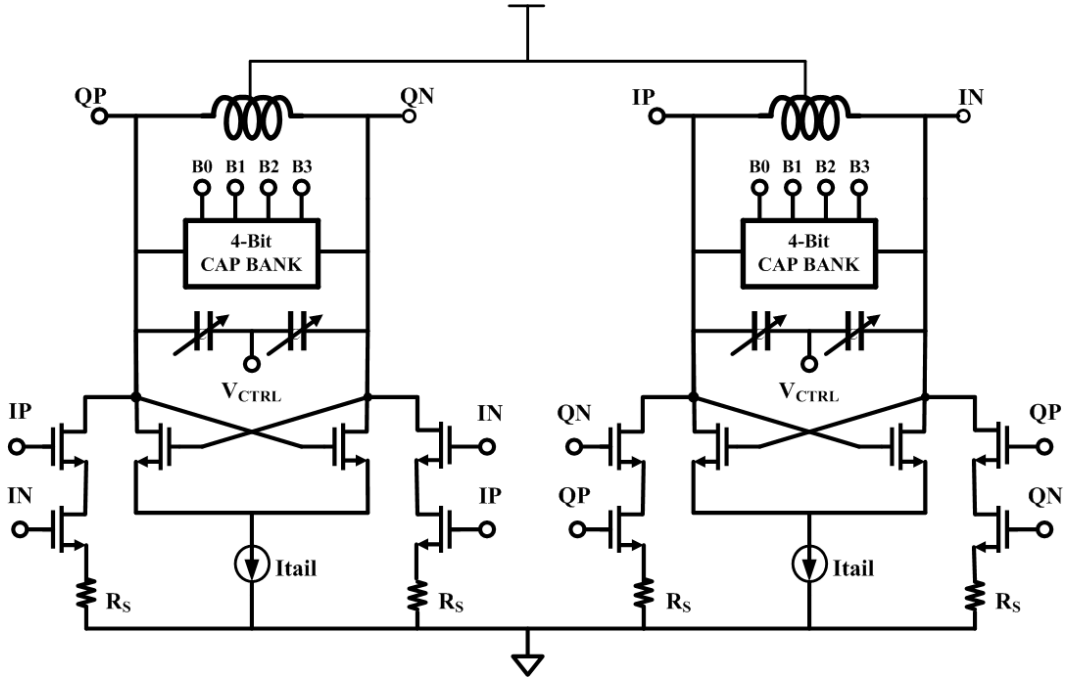
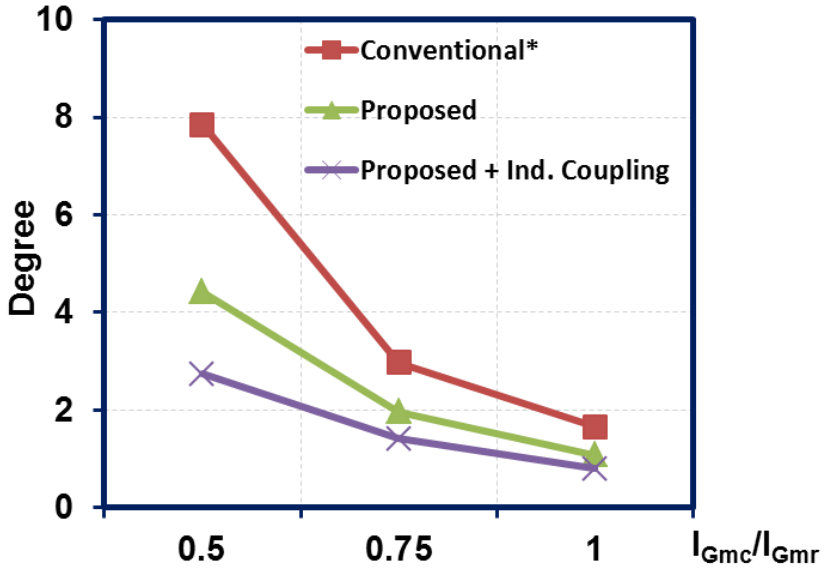
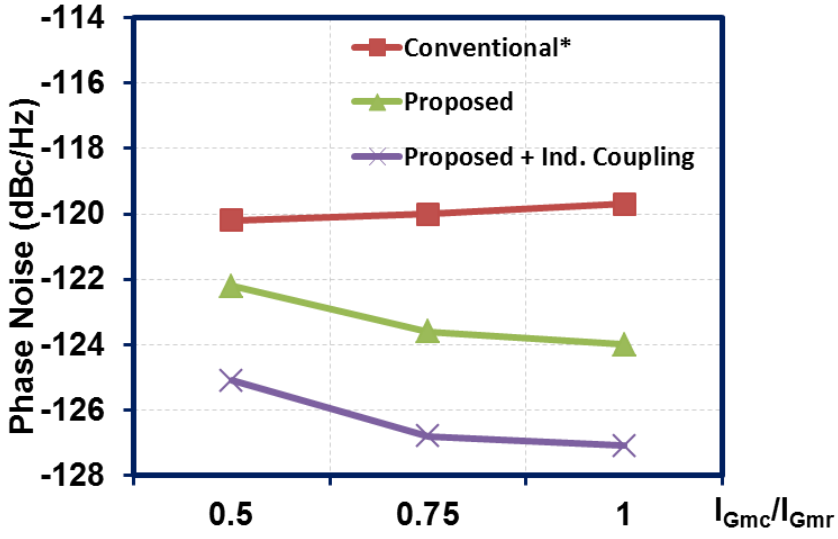


Fig. 3.24 Proposed quadrature voltage-controlled oscillator.



(a)



(b)

Fig. 3.25 (a) phase mismatch vs. coupling factor; (b) phase noise vs. coupling factor.

3.3 Experimental Results and Concluding Remarks

The 2–16 GHz frequency synthesizer was fabricated in a 0.13-μm CMOS technology. A die microphotograph of the chip is shown in Fig. 3.26. The chip area is 2.125 mm^2 while the active core area occupies 1.08 mm^2. Fig. 3.27 shows the simulated phase noise of the frequency synthesizer; as expected the high frequency noise is dominated by QVCO noise, ranging -114dBc at 1 MHz offset frequency. To relieve the signal attenuation from package, PCB, and parasitics, the phase noise is measured at lower frequency after halving the clock frequency. The measured phase noise is -119.7 dBc/Hz at 1 MHz offset when operating at 6 GHz. Clock jitter when phase noise is integrated from 1 KHz to 20 MHz yields 0.55ps. The measured SFDR is better than -41 dBc across 1–8 GHz. The maximum power consumption is 64mW. Table 3.1 compares the proposed architecture with previously reported broadband frequency synthesizers. This architecture shows the broadest frequency range. The proposed architecture is very cost-efficient and suitable for the modern emerging broadband communications RF transceivers.

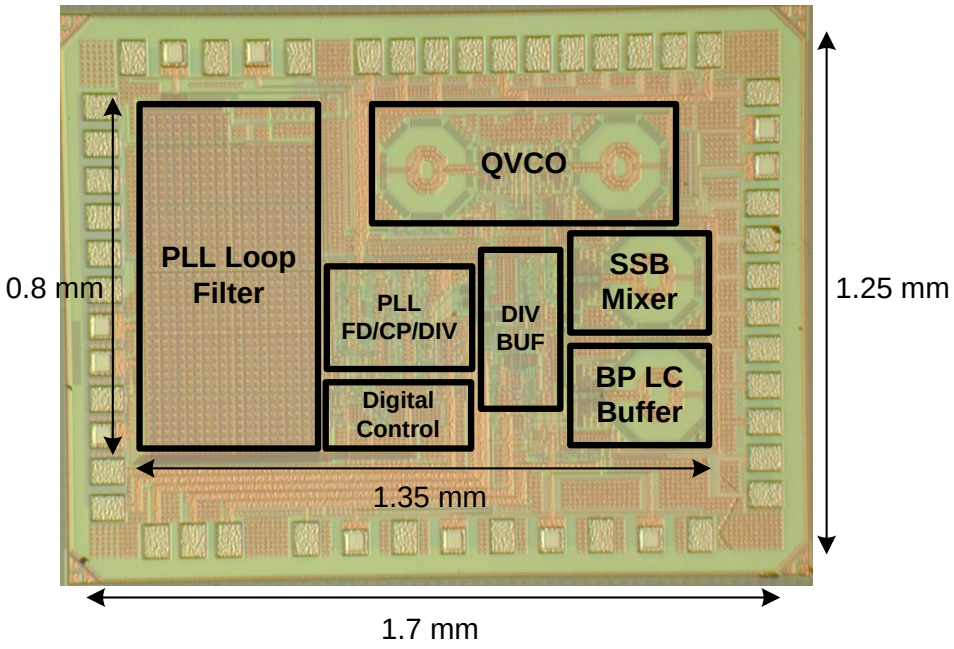


Fig. 3.26 Chip photomicrograph.

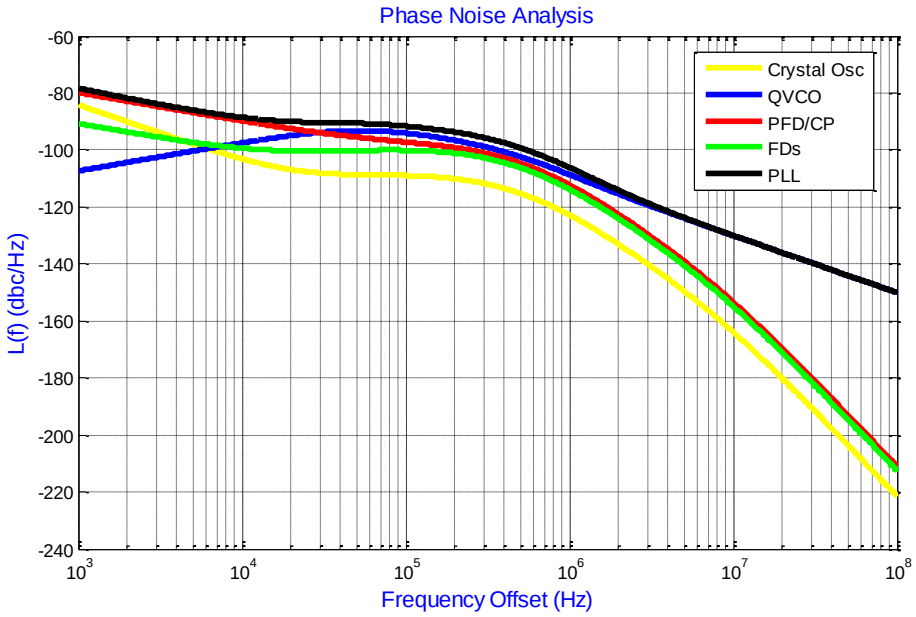


Fig. 3.27 Simulated close-loop phase noise.

Table 3.1 Performance comparison.

	RFIC `09 [4]	JSSC `11 [3]	This Work
Technology	45-nm CMOS	0.13-µm CMOS	0.13-µm CMOS
Power (mW)	21 - 31	36 – 53	32 - 64
Area (mm^2)	0.41	1.86	1.08
Frequency Range (GHz)	0.1 - 5	1.8 - 6	2 - 16
Phase Noise @1 MHz (dBc/Hz)	-112 (LO:7.2GHz)	-115 (LO:5.2GHz)	-120 (LO:6GHz)
SFDR (dBc)	NA	< -42.4	< -41

CHAPTER IV

LOW PHASE NOISE AND PRECISE QUADRATURE PHASE ACCURACY VOLTAGE-CONTROLLED OSCILLATOR*

4.1 Introduction

Recently, quadrature (I/Q) phase clock generation has been widely investigated and increasingly used in the modern wireless and wireline communication systems. In wireless communications, the low-cost fully integrated wireless transceivers mostly use the low intermediate frequency (IF) or zero-IF architecture; both architectures require quadrature signals for modulation/demodulation and superior image rejection [24]. Also, clock and data recovery (CDR) system applies the quadrature clocks to the half-rate phase sampling for lowering the maximum operation speed and power consumption [25]. Besides, the quadrature signals can be employed in single-sideband mixing to expand the frequency coverage of wideband frequency synthesis [26]. Quadrature phases can be generated by *RC* poly-phase filters, frequency dividers, ring oscillators, delay-locked loops, and *LC* quadrature voltage-controlled oscillators (QVCOs). Compared with the other approaches, *LC* QVCOs usually outperform in power consumption with the penalty of larger silicon area.

* Part of this chapter is reprinted with permission from Yung-Chung Lo et. al., "A 5-GHz CMOS LC Quadrature VCO With Dynamic Current-Clipping Coupling to Improve Phase Noise and Phase Accuracy," in IEEE Transactions on Microwave Theory and Techniques, pp. 2632-2640, July 2013, and Haitao Tong et. al., "An LC Quadrature VCO Using Capacitive Source Degeneration Coupling to Eliminate Bi-Modal Oscillation," in IEEE Transactions on Circuits and Systems Part I: Regular Papers, pp. 1871-1879, Sept. 2012.

Conventional QVCOs are formed by two identical cross-coupled *LC* oscillators where the *LC* oscillators are connected though passive components (passive coupling) [27, 28] or active devices (active coupling) [29]. The QVCOs using passive coupling, either inductive or capacitive, perform better phase noise because the passive components are almost noiseless. However, when component mismatches occur between the two *LC* oscillators, the passive coupling featuring a weak coupling strength commonly leads to a significant I/Q phase error. In contrast, the active coupling can be usually strong to well suppress the quadrature phase error due to the mismatches. However, strong active coupling usually degrades phase noise [30]. Several studies have analyzed how the coupling mechanism relates to phase noise and phase accuracy [30, 31, 32, 33, 34, 35]. As a conclusion, phase accuracy and phase noise have been recognized as a tradeoff in QVCOs [33, 34].

Inserting a phase shift in the coupling path has been used for improving the performance of phase noise and phase accuracy [34]. This approach was first proposed for improving phase noise because the optimum phase shift in the coupling path can make the *LC* resonators reach their peak effective quality factor [31]. Furthermore, Li et al [36] demonstrated that implementing the phase-shifted coupling helps eliminate the undesired bi-modal oscillation. In [34], a comprehensive analysis further proved that 90 degree phase shift in the coupling path not only improves phase noise, but also desensitizes the accuracy of quadrature phases to any mismatch between the two *LC* oscillators. Most reported phase-shift techniques utilize either cascode coupling structures [32, 35] or RC networks [31, 34, 35]; however, the cascode topologies provide an insufficient and limited phase

shift, and *RC* networks usually attenuate the coupling signals, add noise, and increase the solution's power consumption. Usually, the effective quality factor degrades when the *LC* oscillators are loaded with *RC* networks.

In this chapter, the approach to analyze bi-modal oscillation and phase accuracy is based on the phasor diagram of effective currents. This approach is simple and straightforward to model the conditions of bi-modal oscillation and analyze the sensitivity of phase accuracy to component mismatches. Moreover, a simplified time-variant approach based on the Impulse Sensitivity Function (ISF) is used to analyze the phase noise contribution from additive noise sources. The performance of phase accuracy and phase noise significantly depends on two critical parameters, the phase shift in coupling path and the coupling ratio. It will be shown that increasing the coupling ratio is a more effective way to assure excellent quadrature phase accuracy. However, a large coupling ratio usually results in higher power consumption and worse phase noise.

In this chapter, two QVCO topologies are proposed. The first QVCO applies the phase shift technique by using capacitive source degeneration (CSD). The capacitive degenerated differential pairs are used to couple the *LC* tanks to implement a phase-shifted transconductance and negative input resistance to compensate resonator losses, and to minimize the flicker noise contributions. The CSD technique not only introduces excess phase shift to eliminate undesired bi-modal oscillation, but inherently provides a large coupling ratio to improve quadrature phase accuracy. The second QVCO uses dynamic cascode coupling (DCC) technique to have more efficient phase-shifted coupling and avoid noise injection at the most vulnerable timings (around zero crossing points). The

DCC QVCO employs a large coupling ratio to improve phase accuracy without degrading phase noise; therefore, the general tradeoff between phase noise and phase accuracy is eliminated. The DCC QVCO coupling mechanism exhibits outstanding performance in power consumption, phase noise and phase accuracy.

4.2 Bi-Modal Oscillation, Quadrature Phase Accuracy and Phase Noise

The active-coupled quadrature *LC* oscillators usually consist of two stages, each of which is composed of a *LC* tank and a cross-coupled differential pair. The two coupling transconductors connect the two *LC* oscillators to form a closed feedback loop. The equivalent linear behavior model of conventional QVCOs is illustrated in the Fig. 4.1 where G_{mr} and G_{mc} represent the cross-coupled (regenerative) and coupling transconductances, respectively. The *LC* resonator is modeled as a parallel *RLC* circuit where R_p, C_p, L_p are the equivalent resistance, capacitance and inductance, respectively. The impedance of the *LC* resonator can be expressed as

$$Z_L(j\omega) = \frac{R_p}{1 + jQ\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)} \tag{4.1}$$

where Q is the quality factor of the *LC* resonator ($Q = \omega_o R_p C = R_p/\omega_o L$) and ω_o is its resonant frequency ($\omega_o = (L_p C_p)^{-1/2}$). A phase-shifter is placed in front of the coupling transconductor on the coupling path. The phase shifter model presented in the polar form can be expressed as

$$PS = \alpha \cdot e^{j\varphi} \tag{4.2}$$

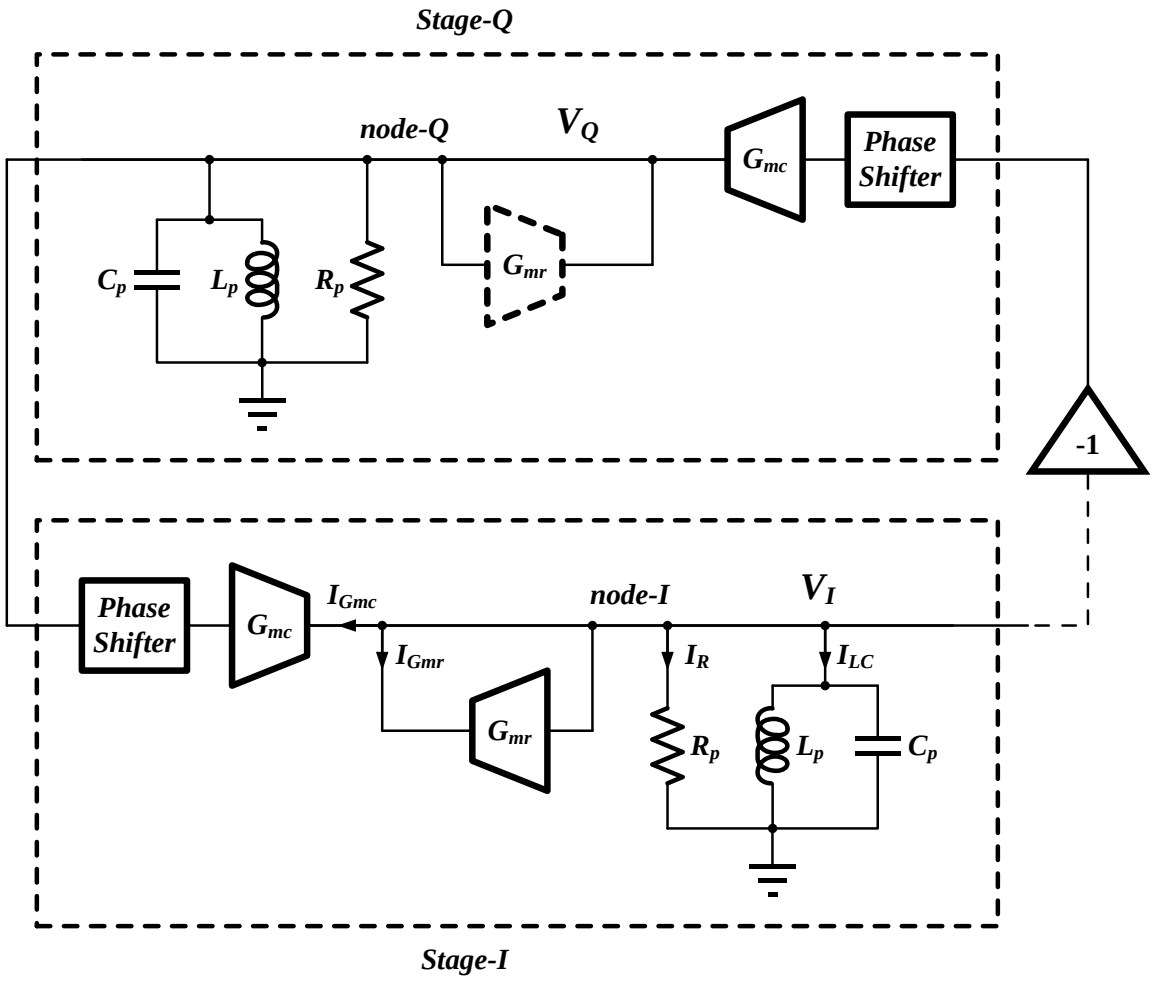


Fig. 4.1 QVCO linear model.

where α is the absolute gain of the phase shifter and φ is its phase shift. For a QVCO without the phase shifter, α is unity and φ is zero degree. I_{Gmr}, I_{Gmc}, I_R, and I_{LC} are the effective currents flowing through the regenerative transconductance, coupling transconductance, tank equivalent resistance, and *LC* network at node-*I*, as shown in the Fig. 4.1. The current components can be expressed as

$$I_{Gmr} = -V_I \cdot G_{mr} \tag{4.3}$$

$$I_{Gmc} = -V_Q \cdot G_{mc}\left(\alpha \cdot e^{j\varphi}\right) \tag{4.4}$$

$$I_R = V_I \cdot \frac{1}{R_p} \tag{4.5}$$

$$I_{LC} = V_I \cdot j\frac{Q}{R_p}\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right) \tag{4.6}$$

where V_I and V_Q are signals at node-I and node-Q, respectively. If stage-I perfectly matches stage-Q, V_I and V_Q are equal and the oscillation is stable. In order to satisfy the Barkhausen stability criteria, the phase shift of each I/Q stage has to be ± 90 degree and G_{mr} be equal to $1/R_p$. Although the linear small signal model may not precisely represent the real behavior of QVCOs, it helps to understand the operation of QVCOs and provide useful design insights.

4.2.1 Bi-modal Oscillation

A quadrature oscillator may have two different stable oscillations [36]. A QVCO could oscillate at one of two possible oscillation frequencies with one of two opposite quadrature phase sequences. Because the quadrature phases are usually used for image-rejection in wireless receiver, the ambiguity of two quadrature phase sequences would lead to an uncertainty on the selection of upper or lower sideband. The quadrature phase ambiguity could be also problematic while using the SSB mixer for clock frequency synthesis [26].

Because both ±90 degree phase shift in each I/Q stage can satisfy the Barkhausen criteria, the stage-I may either lead or lag the stage-Q by 90 degree. The two solutions

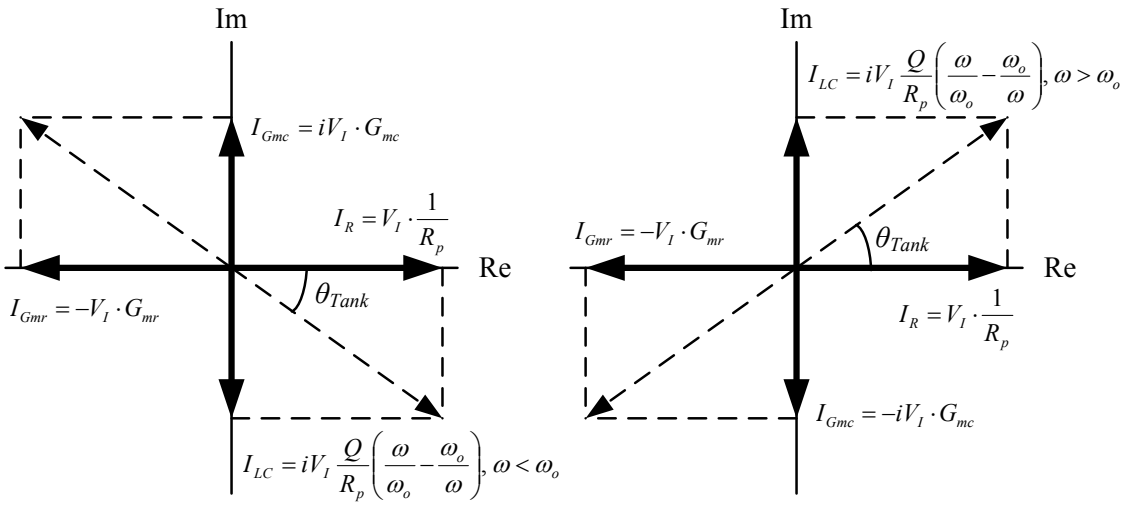


Fig. 4.2 Bi-modal oscillation interpretation by using a current phasor diagram with ideal *LC* tank and *PS* = 1.

lead to the bi-modal oscillation. The bi-modal oscillation can be illustrated by the current phasor diagrams shown in Fig. 4.2. If the oscillation is stable at the frequency ω_{osc}, the effective currents I_{Gmr}, I_{Gmc}, I_R, and I_{LC} at node-I can be plotted in a complex plane according to equations (4.3) – (4.6). The net effective current flowing out from the node-*I* must be zero to observe the Kirchhoff's current law. Assuming that G_{mr} and G_{mc} are both positive, the oscillation mode when stage-I leads stage-Q by 90 degree ($V_I = i \cdot V_Q$) is shown in the Fig. 4.2(a). The net zero current condition leads to

$$G_{mc} = -\frac{Q}{R_p}\left(\frac{\omega_{osc}}{\omega_o} - \frac{\omega_o}{\omega_{osc}}\right) \tag{4.7}$$

and

$$G_{mr} = \frac{1}{R_p} \tag{4.8}$$

Based on equation (4.7) and $\omega_o >> G_{mc}/C_p$, ω_{osc} is lower than ω_o, and ω_{osc} can be approximated as

$$\omega_{osc} \approx \omega_o - \frac{G_{mc}}{2C_p} \tag{4.9}$$

Similarly, Fig. 4.2(b) shows the case when stage-*I* lags stage-Q by 90 degree ($V_I = -i \cdot V_Q$), ω_{osc} is higher than ω_o, and accordingly ω_{osc} can be approximated as

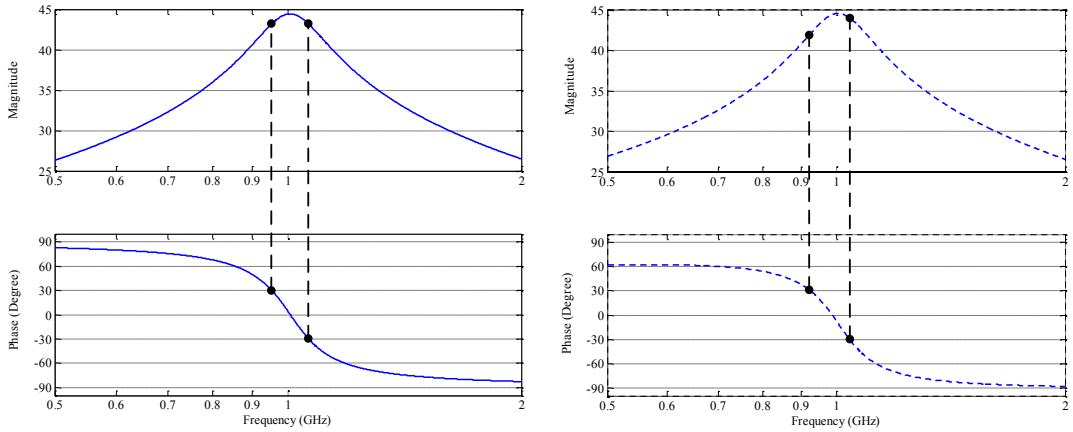
$$\omega_{osc} \approx \omega_o + \frac{G_{mc}}{2C_p} \tag{4.10}$$

Equations (4.9) and (4.10) show that two oscillation frequencies with the respective quadrature phase sequence would exist in QVCOs. It should be noticed that the sign of G_{mc} in (4.9) and (4.10) depends on the coupling transconductor topology.

I_{Gmc} injected into the *LC* tank is in quadrature phase with the output of each I/Q stage. Hence, this imaginary injection current I_{Gmc} induces the responding imaginary *LC* tank current and leads to a phase shift from the phase at resonant frequency. This phase shift of the *LC* tank can be expressed as

$$\theta_{Tank} = \pm \tan^{-1}\left(\frac{I_{Gmc}}{I_{Gmr}}\right) = \pm \tan^{-1}\left(\frac{G_{mc}}{G_{mr}}\right) = \pm \tan^{-1} m \tag{4.11}$$

where m is the coupling ratio of coupling transconductance to regenerative transocnductance. The positive and negative sign in (4.11) is from the uncertainty of the bi-modal oscillation. A larger coupling ratio m will result in more phase shift and meanwhile pull the oscillation frequency far away from the nature resonant frequency. Accordingly, the impedance magnitude of the *LC* tank will reduce.



(a) (b)

Fig. 4.3 Frequency response of (a) ideal *LC* tank, and (b) practical *LC* tank.

Fig. 4.3(a) shows that the frequency response of an ideal parallel *RLC* network is symmetric at the resonant frequency. Therefore, the same magnitude of the *LC* tank impedance with a phase shift $\pm\theta_{Tank}$ leads to the ambiguity of the bi-modal oscillation. However, in reality the unequal inductor series loss and capacitor series loss result in an asymmetric magnitude/phase response of an *LC* tank at the resonant frequency as shown in Fig. 4.3(b). With the $\pm\theta_{Tank}$ induced by the coupling transconductor, the magnitude of the *LC* tank impedance is different. The phase shift condition with a larger magnitude provides a larger loop gain to grow the oscillation and suppress the other condition. Therefore, the asymmetric frequency response of *LC* tank would overcome the bi-modal oscillation [37]. The inductor series loss and capacitor series loss of a practical *LC* tank can be modeled as an ideal parallel *RLC* network, adding a phase shift on the path of the coupling transconductor G_{mc} and the regenerative transconductor G_{mr} [35]. The effective

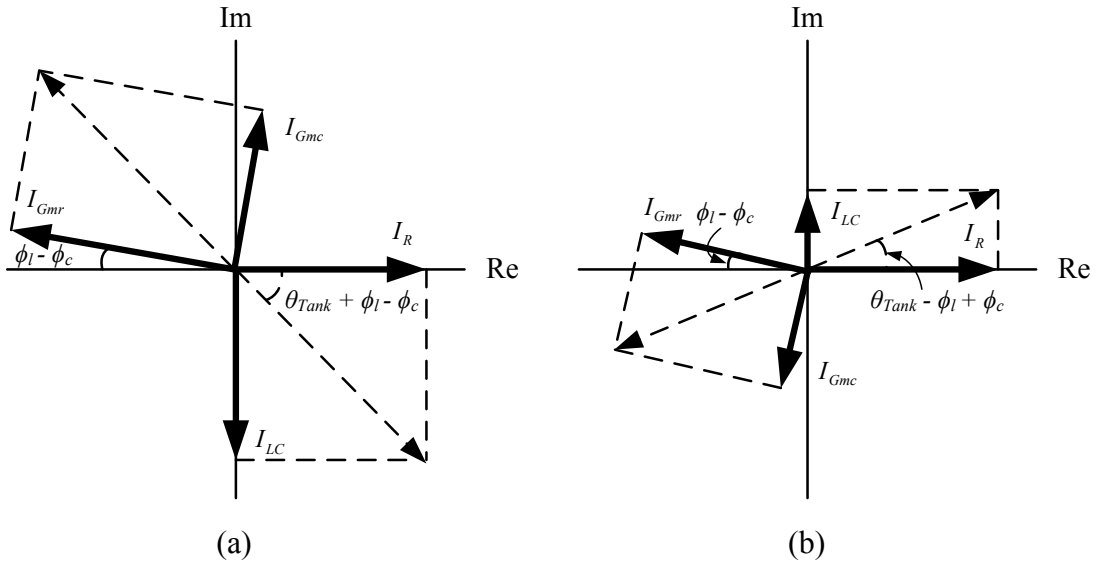


Fig. 4.4 A bi-modal oscillation interpreted by effective current phasor diagram with practical *LC* tank.

phase shifts ϕ_l and ϕ_c contributed by inductive loss and capacitive loss, respectively, can be approximated as

$$\phi_l \approx \tan^{-1}\left(\frac{r_L}{\omega_o L_p}\right) = \tan^{-1}\left(\frac{1}{Q_L}\right) \tag{4.12}$$

$$\phi_c \approx \tan^{-1}\left(r_C \omega_o C_p\right) = \tan^{-1}\left(\frac{1}{Q_C}\right) \tag{4.13}$$

where r_L and r_C are the series resistance of the inductor and capacitor, and Q_L and Q_C are the quality factors of inductor and capacitor in an *LC* tank, respectively. The total effective phase shift is then

$$\phi_{LC} = \phi_l - \phi_c \tag{4.14}$$

Fig. 4.4(a) and (b) show the phasor diagrams with a coupling ratio m > $\tan^{-1}(\phi_{LC})$, and $\phi_{LC} > 0$. This condition is usually the case if the quality factor of the inductor is lower

than that of the capacitor. Fig. 4.4 illustrates that the asymmetric magnitude/phase response, modeled as an effective phase shift, can guarantee a single oscillation mode. The oscillation frequency is closer to the resonant frequency and the *LC* tank impedance is larger at oscillation frequency (Fig. 4.4(b)). Fig. 4.4 also reveals that if the coupling ratio m is small, the LC tank impedances at oscillation frequencies in both (a) and (b) condition are very close, so two possible modes could occur due to PVT variations and non-idealities. If the series inductor loss dominates, it is recommended that the coupling ratio m is at least two or three times larger than $1/Q_L$ to avoid bi-modal oscillation. It should be also noticed that an inductor with a quality factor contributes with ϕ_l of 5.7 degrees.

A large effective phase shift ϕ_{LC} can resolve the bi-modal oscillation. However, there are several issues in relying on the asymmetric frequency response of an *LC* tank. First, various delays due to the coupling transconductor, regenerative transconductor, and the RC effects of interconnect, parasitics, and gate resistance may cancel the effective phase shift ϕ_{LC}. Second, in order to improve phase noise, higher quality factors of inductors and capacitors are always preferred. Higher quality factors of the passive components lead to a smaller ϕ_{LC} and consequently increase the possibility of bi-modal oscillation. Third, the trends of QVCOs towards wide tuning range, higher oscillation frequency, and lower power supply voltage result in lower the quality factor of the capacitor bank and varactor. On the other hand, the quality factor of the inductor keeps improving in modern CMOS technologis. Therefore, ϕ_c would be comparable to ϕ_l, and a large phase shift of ϕ_{LC} is no longer used for resolving the bi-modal oscillation in many situations.

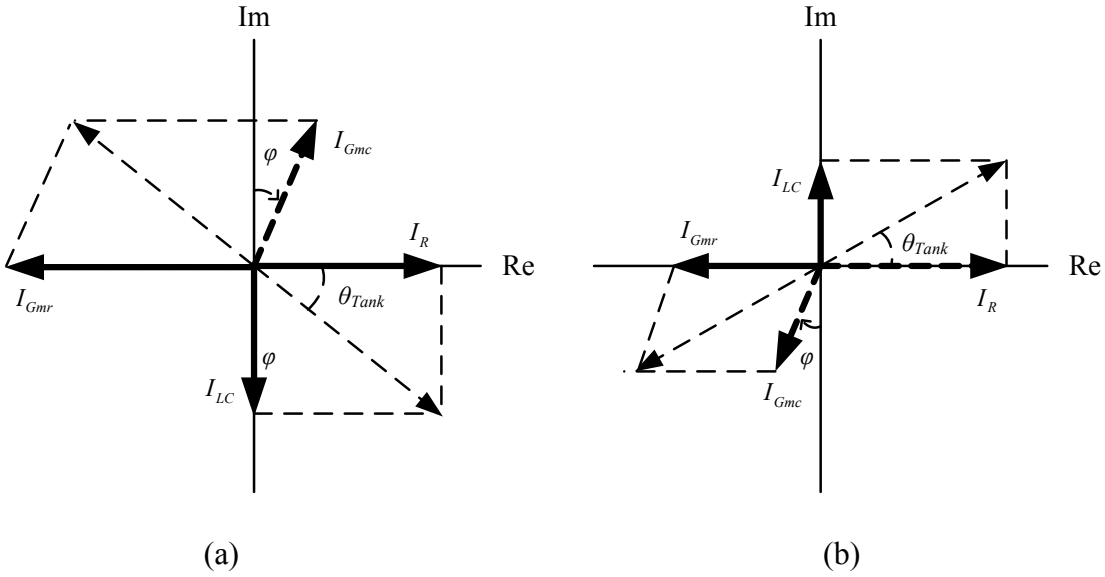


Fig. 4.5 Phase shift added to guarantee the oscillation mode.

Adding a phase shifter in the coupling path has been reported as an effective way to resolve the bi-modal oscillation and assure/select one of the four possible oscillation models [36]. Fig. 4.5 is an example of phasor diagram showing that adding a phase shift φ in the coupling path leads to an impedance magnitude difference between the two opposite quadrature phase sequences. Consequently, the oscillation will favor the mode which has a larger impedance/loop gain to grow the oscillation. Since the delays and non-idealities on the coupling and regenerative paths can be referred to an effective phase shift ϕ_{Gmc} in the coupling path and an effective phase shift ϕ_{Gmr} in the cross-coupled path, the boundaries of four QVCO oscillation modes are

$$\begin{cases} -\Delta\phi < \varphi < 90^\circ - \Delta\phi, & \Rightarrow \omega_{osc} > \omega_o, \text{and stage} - I \text{ lags stage} - Q \\ 90^\circ - \Delta\phi < \varphi < 180^\circ - \Delta\phi, & \Rightarrow \omega_{osc} < \omega_o, \text{and stage} - I \text{ lags stage} - Q \\ 180^\circ - \Delta\phi < \varphi < 270^\circ - \Delta\phi, & \Rightarrow \omega_{osc} > \omega_o, \text{and stage} - I \text{ leads stage} - Q \\ 270^\circ - \Delta\phi < \varphi < -\Delta\phi, & \Rightarrow \omega_{osc} < \omega_o, \text{and stage} - I \text{ leads stage} - Q \end{cases} \quad (4.15)$$

where

$$\Delta\phi = \frac{m+1}{m}\phi_{LC} + \phi_{Gmc} + \frac{1}{m}\phi_{Gmr} \tag{4.16}$$

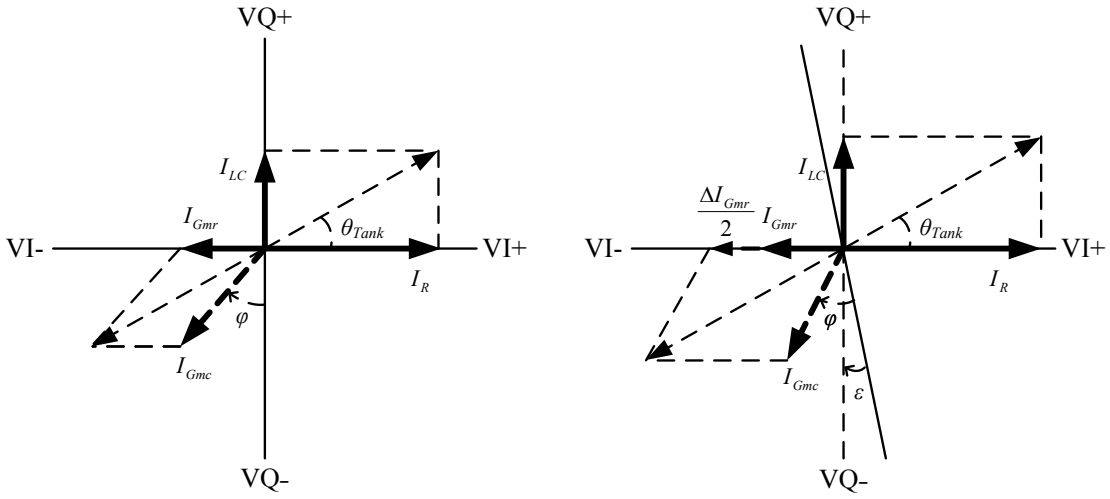
According to (4.15) and (4.16), implementing an optimized phase shift of ±90°-$\Delta\phi$ in the coupling path makes the QVCO oscillate at the resonant frequency with its peak effective quality factor [34]. It should be noticed that ϕ_{LC} = 5° and m = 0.5 contribute with 15 degrees to $\Delta\phi$. Aslo, ϕ_{Gmr} and ϕ_{Gmc} can be around 10–20 degrees in practical QVCOs. The value of $\Delta\phi$, which depends on QVCO topology, *LC* resonator, large-signal switching operation of G_{mr} and G_{mc}, and delays in G_{mr} and G_{mc}, has to be taken into account when designing the phase shifter.

4.2.2 Quadrature Phase Accuracy

Ideally, a QVCO generated the output waveforms that have 90 degrees phase difference. However, the device mismatches, unbalanced parasitics, and layout asymmetries between *I*/*Q* stages would lead to the quadrature phase/amplitude errors in the output waveforms. Several works have been dedicated to improving or calibrating the quadrature phase/amplitude error [38]. To understand the quadrature phase error due to various mismatches, an approach using the effective current phasor diagram is employed. Fig. 4.6(a) is the phasor diagram with an inserted phase shift in the coupling path. The effective coupling ratio m_{eff} is then rewritten as

$$m_{eff} = \frac{I_{Gmc}\cos\varphi}{I_{Gmr} + I_{Gmc}\sin\varphi} = \frac{m\cos\varphi}{1 + m\sin\varphi} \tag{4.17}$$

and the phase shift of *LC* tank is



(a) (b)

Fig. 4.6 Phase error analysis by effective current phasor diagram.

$$\theta_{Tank} = \tan^{-1} m_{eff} \tag{4.18}$$

Since the net current is zero in the phasor diagram, the oscillation frequency is accordingly computed as

$$\omega_{osc} = \omega_o \pm \frac{\omega_o}{2Q} \frac{m\cos\varphi}{1 \pm m\sin\varphi} \tag{4.19}$$

Assume the mismatches $+\Delta I_{Gmr}/2$ and $-\Delta I_{Gmr}/2$ are considered in stage-I and stage-Q, respectively, they produce a variation of θ_{Tank} in each stage. Because the mismatches are symmetric, the oscillation frequency remains invariant after introducing the mismatches. A phase error ε between I/Q outputs will appear to compensate the variation of θ_{Tank} induced by the I_{Gmr} mismatches and keep m_{eff} the same as shown in Fig. 4.6(b). This condition leads to the following equation:

$$m_{eff} = \frac{I_{Gmc}\cos\varphi}{I_{Gmr} + I_{Gmc}\sin\varphi} = \frac{I_{Gmc}\cos(\varphi + \varepsilon_{Gmr})}{I_{Gmr} + \frac{\Delta I_{Gmr}}{2} + I_{Gmc}\sin(\varphi + \varepsilon_{Gmr})} \tag{4.20}$$

The phase error ε_{Gmr} is small so as to approximate $\sin(\varepsilon_{Gmr}) = \varepsilon_{Gmr}$, and $\cos(\varepsilon_{Gmr}) = 1$. Rearranging Equation (4.20) gives the phase error due to the mismatch of I_{Gmr}

$$\varepsilon_{I_{Gmr}} = -\frac{\cos\varphi}{m + \sin\varphi}\frac{\Delta I_{Gmr}}{2I_{Gmr}} \tag{4.21}$$

Therefore, the phase error due to ΔI_{Gmr} decreases for larger m. Similarly, this approach can be applied to the phase error from mismatches in I_{Gmc}, leading to the following result:

$$m_{eff} = \frac{I_{Gmc}\cos\varphi}{I_{Gmr} + I_{Gmc}\sin\varphi} = \frac{\left(I_{Gmc} + \frac{\Delta I_{Gmc}}{2}\right)\cos(\varphi + \varepsilon_{Gmr})}{I_{Gmr} + I_{Gmc}\sin(\varphi + \varepsilon_{Gmr})} \tag{4.22}$$

The phase error induced by the mismatches in I_{Gmc} is

$$\varepsilon_{I_{Gmc}} = \frac{\cos\varphi}{m + \sin\varphi}\frac{\Delta I_{Gmc}}{2I_{Gmc}} \tag{4.23}$$

As shown in the Fig. 4.6, the effect of the mismatch ΔI_R is similar to that of $-\Delta I_{Gmr}$. Hence, substituting $-\Delta I_R$ and $-I_R = I_{Gmr} + I_{Gmc}\sin\varphi$ into (4.21) leads to the equation for the phase error from the mismatch of I_R

$$\varepsilon_{I_R} = -\frac{\cos\varphi(1 + m\sin\varphi)}{m + \sin\varphi}\frac{\Delta I_R}{2I_R} \tag{4.24}$$

The mismatches in capacitance and inductance of LC tank result in a variation in the imaginary part of tank impedance and accordingly a shift of resonant frequency. Consequently, these mismatches can be modeled as ΔI_{LC}. Based on the phasor diagram analysis, the expression of effective coupling ratio is

$$m_{eff} = \frac{I_{Gmc}\cos\varphi}{I_{Gmr} + I_{Gmc}\sin\varphi} = \frac{I_{Gmc}\cos(\varphi + \varepsilon_{Gmr}) + \dfrac{\Delta I_{LC}}{2}}{I_{Gmr} + I_{Gmc}\sin(\varphi + \varepsilon_{Gmr})} \tag{4.25}$$

Thus, the phase error due to ΔI_{LC} can be expressed as

$$\varepsilon_{I_{LC}} = \frac{1 + m\sin\varphi}{m + \sin\varphi}\frac{\Delta I_{LC}}{2mI_{Gmr}} \tag{4.26}$$

According to (4.1), the variation of reactance from the variation of resonant frequency can be expressed as

$$\frac{\Delta Z_X}{Z_X} = \frac{1}{\dfrac{\omega}{\omega_o} - 1}\frac{\Delta\omega_o}{\omega_o} \tag{4.27}$$

The variation in reactance of LC tank is equivalent to the variation in I_{LC}. Substituting (4.19) into (4.27) yields

$$\frac{\Delta I_{LC}}{I_{LC}} = \frac{\Delta Z_X}{Z_X} = \frac{1}{\dfrac{\omega}{\omega_o} - 1}\frac{\Delta\omega_o}{\omega_o} \tag{4.28}$$

Substituting $I_{LC} = I_{Gmc}\cos\varphi$ and (28) into (26) give the phase error due to the mismatch in the resonant frequency

$$\varepsilon_{I_{LC}} = Q\frac{(1 + m\sin\varphi)^2}{m(m + \sin\varphi)}\frac{\Delta\omega_o}{\omega_o} \tag{4.29}$$

Equations (4.21), (4.23), (4.24), and (4.29) agree with those expressions reported in [34] (based on the generalized Adler's equation and hard-limiting model) and [39] (dynamic equations established by the method of multiple time scales). However, the analysis based on the current phasor diagram provides more insights for understanding how those

mismatches induce the phase error. This approach can be extensively used for calculating phase error due to various mismatches and non-idealities.

The phase error expressions show that inserting a phase shift in the coupling path can desensitize the quadrature phase error to mismatches. A 90° degree phase shifter can achieve the minimum sensitivity to device mismatches. It can be explained by the phasor diagram in Fig. 4.7(a). While a 90° phase shift is given in the coupling path, I_{Gmc} aligns

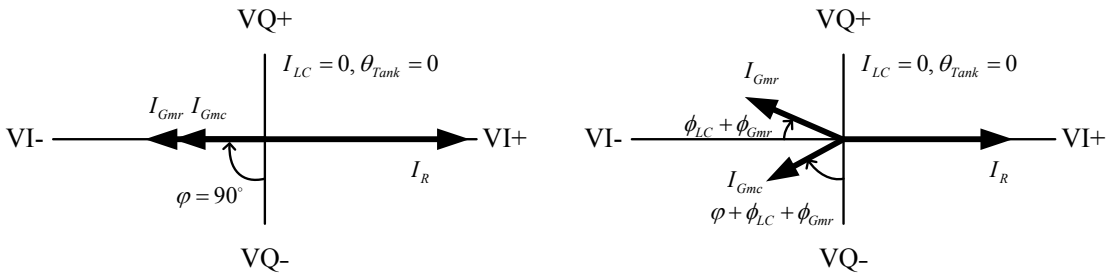


Fig. 4.7 Optimized phase shift to minimized phase error.

with I_{Gmr} and θ_{Tank} is 0 degree. Therefore, the mismatches in I_{Gmr}, I_{Gmc} and tank impedance would only produce variations on the output amplitude. Also, at $\theta_{Tank} = 0$, the oscillation frequency is equal to the nature resonate frequency and $\partial\theta_{Tank} / \partial\omega_o$ reaches maximum value. The phase variation in θ_{Tank} induced by any perturbation or component mismatch that can result in the variation of resonant frequency is minimized at $\theta_{Tank} = 0$. Hence, a minimum phase error will be produced accordingly.

However, this argument of inserting a 90° phase shift is based on an ideal *LC* tank. Also, the large signal behavior and the possible delays in the coupling and regenerative paths were ignored. These non-idealities can be modeled as adding the effective phase

shift $\phi_{LC} + \phi_{Gmr}$ in I_{Gmr} and $\phi_{LC} + \phi_{Gmr}$ in I_{Gmc} as shown in the Fig. 4.7(b). The optimized phase shift is then

$$\varphi_{opt} = \pm 90° - \Delta\phi \tag{4.30}$$

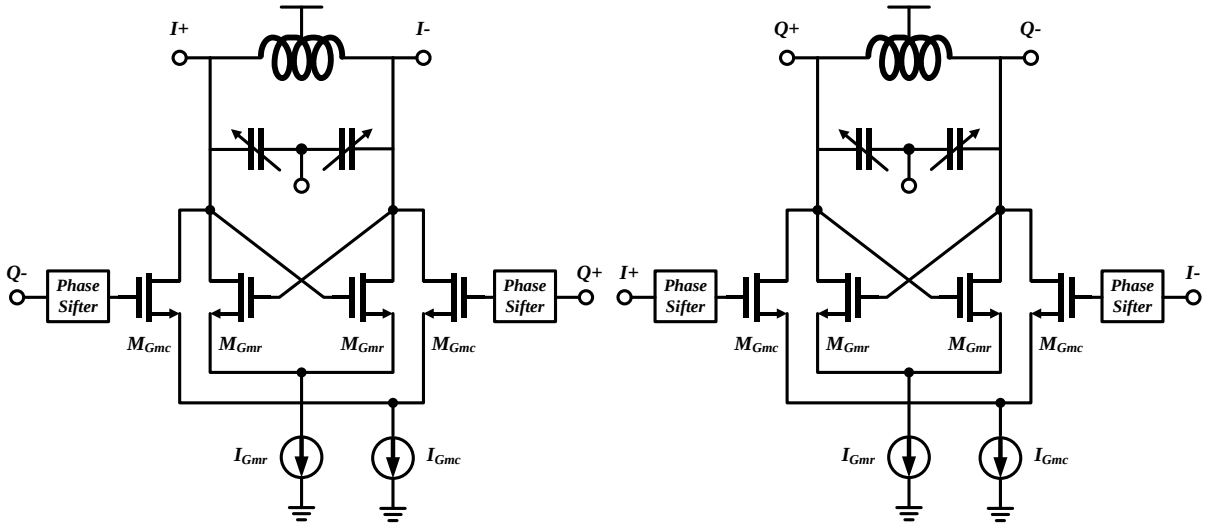
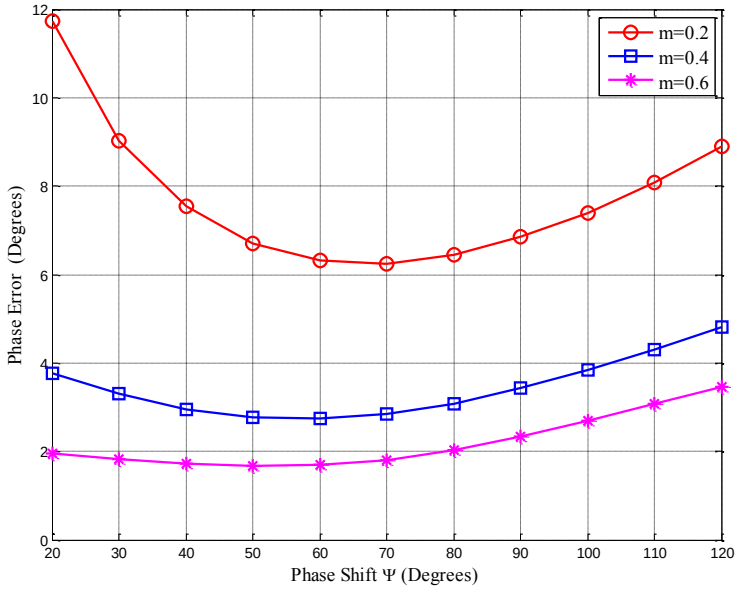


Fig. 4.8 Parallel-QVCO with ideal phase shifter.

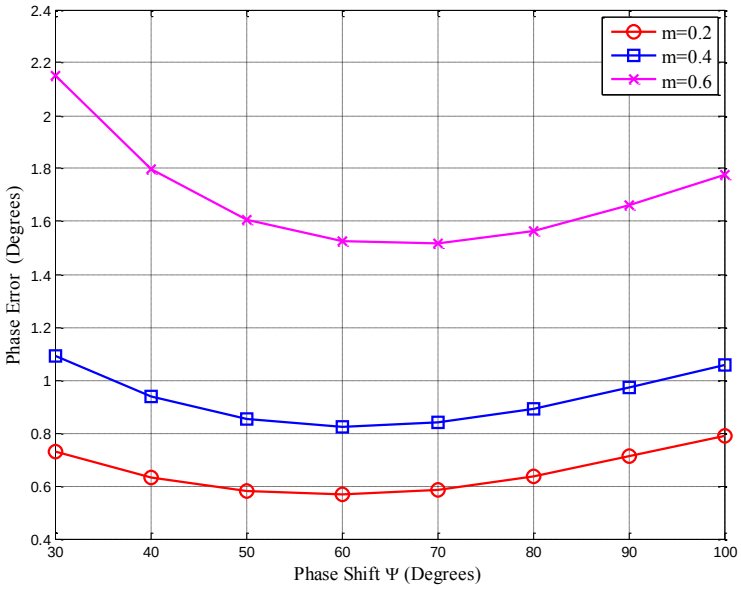
where $\Delta\phi$ is given in (4.16). A parallel-QVCO [29] has been simulated to verify (4.30) with a 0.5% mismatch between two tank capacitors, and 2% mismatches in the coupling currents and regenerative currents, respectively. The 2% mismatch means that the W/L ratio of the crossed-coupled transconductor or coupling transconductor and the DC biasing tail current are increased by 1% in one stage and decreased by 1% in the other stage. An ideal phase shifter is implemented in front of the coupling transconductor as shown in the Fig. 4.8. Fig. 4.9(a) – (c) show the simulated phase errors from mismatches as function of the phase shift φ and coupling ratio m. The simulation results agree with (29) and show

that a phase shift φ around 65° minimize the phase error sensitivity to the mismatches. More importantly, although optimizing the phase shift can improve the phase error, Fig. 9 shows that implementing a large coupling ratio m ($m > 0.5$) would be a more promising way to maintain low phase error sensitivity to mismatches. However, a large coupling ratio costs more power consumption and more importantly degrades the phase noise performance [30, 34].

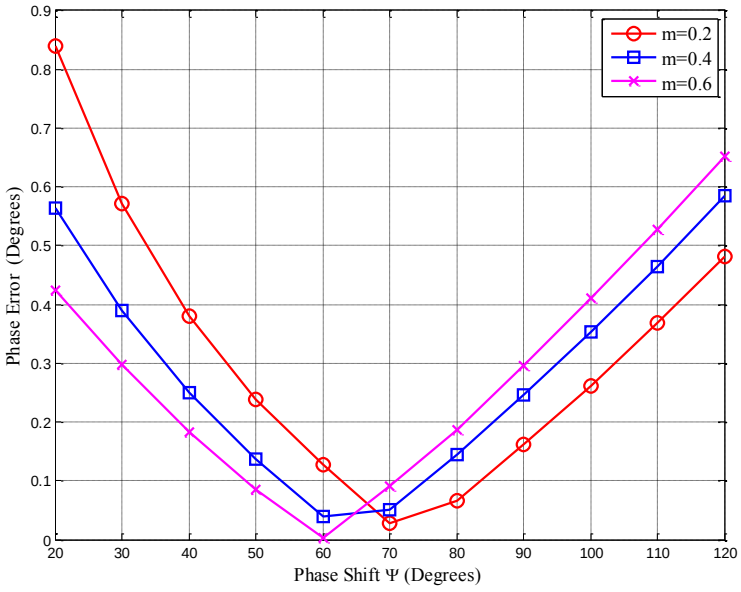


(a)

Fig. 4.9 Simulated phase error due to (a) 0.5% capacitor mismatch in *LC* tank, (b) 2% mismatch in cross-coupled transconductor and (c) 2% mismatch in coupling transconductor.



(b)



(c)

Fig. 4.9 Continued

4.2.3 QVCO Phase Noise

It is reported that quadrature oscillators have worse noise/power tradeoff than a stand-alone *LC* oscillator [33]. For example, if the power consumption of a QVCO is twice more than that of a stand-alone *LC* oscillator, the phase noise of a QVCO will not be 6-dB better than a stand-alone *LC* oscillator. While the optimized phase shift in the coupling path can improve the phase noise of a QVCO, the figure of merit (FoM) of a quadrature oscillator is worse than a stand-alone *LC* oscillator. Hence, it is necessary to analyze further the additive noise sources.

The impulse sensitivity function (ISF) is a useful linear-time-variant tool to calculate the phase noise [40]. The approximated ISF expressions for QVCOs have been already reported in [30]. Also, since the QVCO is symmetric and fully differential, the half-circuit analysis is used for calculating the total phase noise. The ISF for one branch of the parallel-QVCO with ideal phase shifters shown in the Fig. 4.8 can be expressed as

$$\Gamma(\phi) = \frac{1}{N\cos(\theta_{Tank})}\cos(\phi + \theta_{Tank}) \tag{4.31}$$

where $N = 4$, $\phi = \omega_{osc}t$, and θ_{Tank} is given in (4.18). The node voltage at the output of that branch can be expressed as

$$V(\phi) = V_o(1 + m\sin\varphi)\sin\phi \tag{4.33}$$

where V_o is the output amplitude of a QVCO when the phase shifter in the coupling path is removed. Since the noise source can be treated cyclo-stationary, the phase noise contributed by a noise source current i_n can be expressed as

$$L_n(\Delta\omega) = 10\log\left(\frac{N}{2q_{\max}^2}\Gamma_n^2\frac{1}{\Delta\omega^2}\right) \tag{4.35}$$

where $q_{max} = CV$ is the peak dynamic charge loaded onto C, and

$$\Gamma_n^2 = \frac{1}{2\pi}\int_0^{2\pi}\Gamma^2(\phi)\cdot\overline{i_n^2}(\phi)d\phi. \tag{4.35}$$

Γ_n^2 is defined as the effective integrated ISF noise power. Based on (4.35), the noise sources of tank loss R_{LC}, cross-coupled transconductor G_{mr}, coupling transconductor G_{mc} and tail transistor G_{tr} of cross-coupled differential pair and tail transistor G_{tc} of coupling differential pair are analyzed in the following section.

A. Tank Loss

The loss of LC tank can be presented by a parallel resistor R_{LC} whose noise current power spectral density can be expressed as

$$\overline{i_{n,R}^2} = 4kT\frac{1}{R_{LC}} \tag{4.36}$$

where k is the Boltmann's constant and T is the absolute temperature. As shown in Fig. 4.10(a), the ISF function would vary with the phase shift of LC tank θ_{Tank}, while the noise current power is invariant with θ_{Tank}. Combining (4.35) and (4.36) gives the effective integrated ISF noise power of tank loss

$$\Gamma_{n,R}^2 = \frac{4kT}{N^2\cos^2(\theta_{Tank})}\frac{1}{R} = \frac{4kT}{N^2}\left(1+m_{eff}^2\right)\frac{1}{R}. \tag{4.37}$$

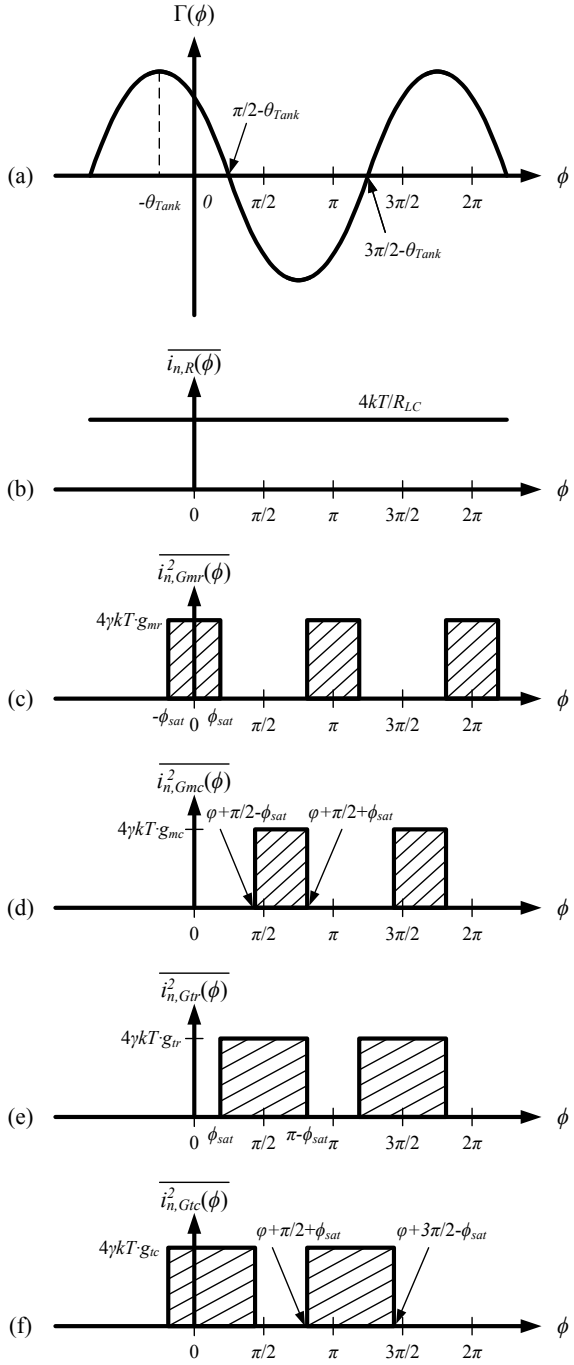


Fig. 4.10 Phase noise analysis by simplified linear-time-variant approach (a) approximated ISF, (b) noise of LC tank, (c) noise from cross-coupled differential pair, (d) noise from coupling differential pair, (e) noise from tail transistor of cross-coupled differential pair, (f) noise from tail transistor of coupling differential pair.

Substituting (4.37) into (4.34) gives the phase noise expression contributed from tank loss

$$L_{n,R}(\Delta\omega) = 10\log\left\{\left[1+\left(\frac{m\cos\varphi}{1+m\sin\varphi}\right)^2\right]\frac{KTR_{LC}}{2V^2}\left(\frac{\omega_{osc}}{Q\Delta\omega}\right)^2\right\} \tag{4.38}$$

where

$$V = V_o(1+m\sin\varphi) \cong \frac{4}{\pi} I_{Tail} R_{LC}(1+m\sin\varphi)\,. \tag{4.39}$$

Equation (4.38) gives the same result reported in [34]. If a 90 degree phase shift is given, the phase noise contributed by the tank loss will be minimized. Also, in terms of considering the tank loss only, QVCOs with optimized phase shift can perform equivalent phase noise performance as the stand-alone *LC* oscillators. In the case, increasing the coupling ratio *m* will not affect the noise contribution from the tank loss but increases the amplitude of the oscillation.

B. Noise from Cross-coupled Differential Pairs M_{Gmr} and *Coupling Differential Pairs M_{Gmc}*

In order to simplify the calculation, a couple of assumptions are made while computing the phase noise contributed by the cross-coupled differential pair noise. First, the differential pairs are operated at the hard-switching condition. Second, the noise appears at QVCO output only when both transistors of the differential pair are in the saturation region. When one of the two transistors is off, no noise from differential pair contributes to the output. Fig. 4.10(c) shows the simplified noise current power model when analyzing the crossed-coupled differential pair. For this case,

$$\overline{i_{n,Gmr}^2} = 4kT\gamma g_{mr} \tag{4.40}$$

and

$$\phi_{sat} = \sin^{-1}\sqrt{\frac{I_{Gmr}}{2\mu_n C_{ox} W_{Gmr} / L_{Gmr} V^2}}\,. \tag{4.41}$$

where I_{Gmr} is the tail current of the cross-coupled differential pair, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area and W_{Gmr} and L_{Gmr} are the width and length of the cross-coupled differential pair, respectively. Equation (4.41) is used to define the operation regions of differential pair [41]. Therefore, the effective integrated ISF noise power due to the cross-coupled differential pair is computed as

$$\Gamma_{n,Gmr}^2 = 2 \times \frac{1}{2\pi}\int_{-\phi_{sat}}^{\phi_{sat}} \frac{1}{N^2\cos^2(\theta_{Tank})}\cos^2(\phi + \theta_{Tank}) \cdot 4kT\gamma g_{mr} d\phi\,. \tag{4.42}$$

Since the energy compensated by the cross-coupled and coupling transconductors is equal to the loss of the LC tank while the oscillation is stable, g_{mr} can be expressed as

$$g_{mr}\frac{4\phi_{sat}}{2\pi}(1 + m\sin\varphi) = \frac{1}{R_{LC}}\,. \tag{4.43}$$

Thus, (4.42) can be rewritten as

$$\Gamma_{n,Gmr}^2 = \frac{8kT\gamma g_{mr}}{\pi N^2}\phi_{sat}\,. \tag{4.44}$$

Substituting (4.44) into (4.34) gives the phase noise expression contributed from cross-coupled differential pairs

$$L_{n,Gmr}(\Delta\omega) = 10\log\left[\left(\frac{1}{1 + m\sin\varphi}\right)\frac{\gamma KTR_{LC}}{2V^2}\left(\frac{\omega_{osc}}{Q\Delta\omega}\right)^2\right]. \tag{4.45}$$

Equation (4.45) shows that the phase noise contributed by the differential pair can be minimized when a 90-degrees phase shift is given.

Similarly, the noise generated by the coupling differential pairs is assumed contributing to the *LC* tank only when both transistors are in saturation region. Fig. 4.10(d) shows the noise current power of coupling differential pairs with a phase shift φ in the coupling path. Thus, the expression for the effective integrated ISF noise power of coupling differential pair is

$$\Gamma_{n,Gmc}^2 = 2 \times \frac{1}{2\pi} \int_{\varphi+\frac{\pi}{2}-\phi_{sat}}^{\varphi+\frac{\pi}{2}+\phi_{sat}} \frac{1}{N^2 \cos^2(\theta_{Tank})} \cos^2(\phi + \theta_{Tank}) \cdot 4kT\gamma g_{mc} d\phi \tag{4.46}$$

where g_{mc} is the transconductance of the coupling transistor M_{Gmc}. In this design, the W/L ratio of M_{Gmc} is scaled with the coupling ratio m (I_{Gmc}/I_{Gmr}) so ϕ_{sat} is unchanged. By using the integration by part, (4.46) is computed as

$$\Gamma_{n,Gmc}^2 = \frac{8kT\gamma g_{mc}}{\pi N^2} \left(\frac{m + \sin\varphi}{1 + m\sin\varphi} \right)^2. \tag{4.47}$$

Similarly to (4.43), g_{mc} must satisfy

$$g_{mc} \frac{4\phi_{sat}}{2\pi} \left(\sin\varphi + \frac{1}{m} \right) = \frac{1}{R_{LC}} \tag{4.48}$$

After combining (4.47), (4.48) and (4.34), the phase noise expression contributed from coupling differential pairs is computed as

$$L_{n,Gmc}(\Delta\omega) = 10\log\left[\left(\frac{m}{1 + m\sin\varphi} \right) \left(\frac{m + \sin\varphi}{1 + m\sin\varphi} \right)^2 \frac{\gamma KTR_{LC}}{2V^2} \left(\frac{\omega_{osc}}{Q\Delta\omega} \right)^2 \right] \tag{4.49}$$

where noise factor F can be defined as

$$F = \left(\frac{m}{1 + m\sin\varphi} \right) \left(\frac{m + \sin\varphi}{1 + m\sin\varphi} \right)^2. \tag{4.50}$$

It should be noticed that when φ is zero and 90 degrees, F will be m^3 and $m/(1+m)$, respectively. The 90-degrees phase shift does not help improve the phase noise when m is small (i.e., $0 < m < 0.6$) but shows significant improvement in phase noise when $m \geq 1$. Also, F increases with a larger m.

C. Noise from Tail Transistors

The noise of tail transistors affects the phase noise performance mainly when one of the differential pair transistors is on and the other one is off. When both differential pair transistors are in the saturation region, the noise of tail transistor is canceled and then it is ignored in this analysis. The assumption of a hard-switching operation in differential pairs is used in this case as well. Fig. 4.10(e) shows the noise current power of the tail transistor providing the biasing current for the cross-coupled differential pair where g_{tr} is the transconductance of the tail transistor. The effective integrated ISF noise power of the tail transistor for the cross-coupled transconductor can be written as

$$\begin{aligned}\Gamma_{n,Gtr}^2 &= 2\times\frac{1}{2\pi}\int_{\phi_{sat}}^{\pi-\phi_{sat}}\frac{1}{N^2\cos^2(\theta_{Tank})}\cos^2(\phi+\theta_{Tank})\cdot 4kT\gamma g_{tr}d\phi \\ &= \frac{2kT\gamma g_{tr}}{N^2}\left\{\left[1+\left(\frac{m\cos\varphi}{1+m\sin\varphi}\right)^2\right]-\frac{8\phi_{sat}}{2\pi}\right\}\end{aligned} \tag{4.51}$$

Similarly, as shown in the Fig. 4.10(f), the effective integrated ISF noise power of the tail transistor of the coupling transconductor can be expressed as

$$\Gamma_{n,Gtc}^2 = 2\times\frac{1}{2\pi}\int_{\frac{\pi}{2}+\phi_{sat}+\varphi}^{\frac{3\pi}{2}-\phi_{sat}+\varphi}\frac{1}{N^2\cos^2(\theta_{Tank})}\cos^2(\phi+\theta_{Tank})\cdot 4kT\gamma g_{tc}d\phi \tag{4.52}$$

where g_{tc} ($g_{tc} = m \cdot g_{tr}$) is the transconductance of the tail transistor providing the biasing current for the coupling differential pair. Solving (4.52) gives the expression:

$$\Gamma_{n,Gtc}^2 = \frac{2kT\gamma g_{tr}}{N^2} m \left\{ \left[1 + \left(\frac{m\cos\varphi}{1 + m\sin\varphi} \right)^2 \right] - \left[\left(\frac{m + \sin\varphi}{1 + m\sin\varphi} \right)^2 \frac{8\phi_{sat}}{2\pi} \right] \right\} \tag{4.53}$$

Equations (4.49) and (4.53) reveals that even though an optimized phase shift is given in the coupling path, while increasing the coupling ratio *m*, the effective noise contributed from the coupling network will increase. Hence, a large coupling ratio *m* leads to worse phase noise performance and power consumption, degrading the figure of merit (FoM) where the conventional FoM is defined as

$$FoM = 20\log(\omega_{osc}/\Delta\omega) - 10\log(L(\Delta\omega)) - 10\log(P\ mW) \tag{4.54}$$

It should be noticed that most phase shifters would generate additional noise and their limited bandwidth attenuates the strength of coupling transconductors, furthermore degrading the performance of QVCOs.

4.3 Capacitive Source Degeneration Coupling QVCO

The usage of capacitive source degeneration differential pairs not only delivers necessary phase shift to improve the phase noise, but also provides a phase-shifted coupling transconductance and negative input resistance to sustain the oscillation. The CSD QVCO has better phase accuracy due to its inherent large transconductance coupling ratio. An additional benefit of the proposed architecture is that the low-frequency noise present at the gates of the transistors implementing the negative resistor (due to noisy LO-signals and transistors) is inherently rejected since the capacitive source degeneration presents a high-pass like noise transfer function.

4.3.1 CSD-QVCO Design

A capacitive source degeneration QVCO (CSD-QVCO), shown in Fig. 4.11, is proposed to suppress bi-modal oscillation. The capacitive source degeneration provides the required amount of phase shift in the transconductance of the coupling pair, which can be derived as follows.

$$G_{mc} \approx \frac{sC_s}{1+s\left(\frac{C_s+C_{gs}}{g_m}\right)} \tag{4.55}$$

At high frequencies, the overall transconductance, G_{mc}, of the capacitive degeneration differential pair is approximated as where C_s is twice the source degeneration capacitance between the two source nodes plus the AC-grounded parasitic capacitors at the source of M_1, C_{gs} is the gate-to-source capacitance and gm is the transconductance of the input transistor M_1. The phase shift in the coupling pair is computed as,

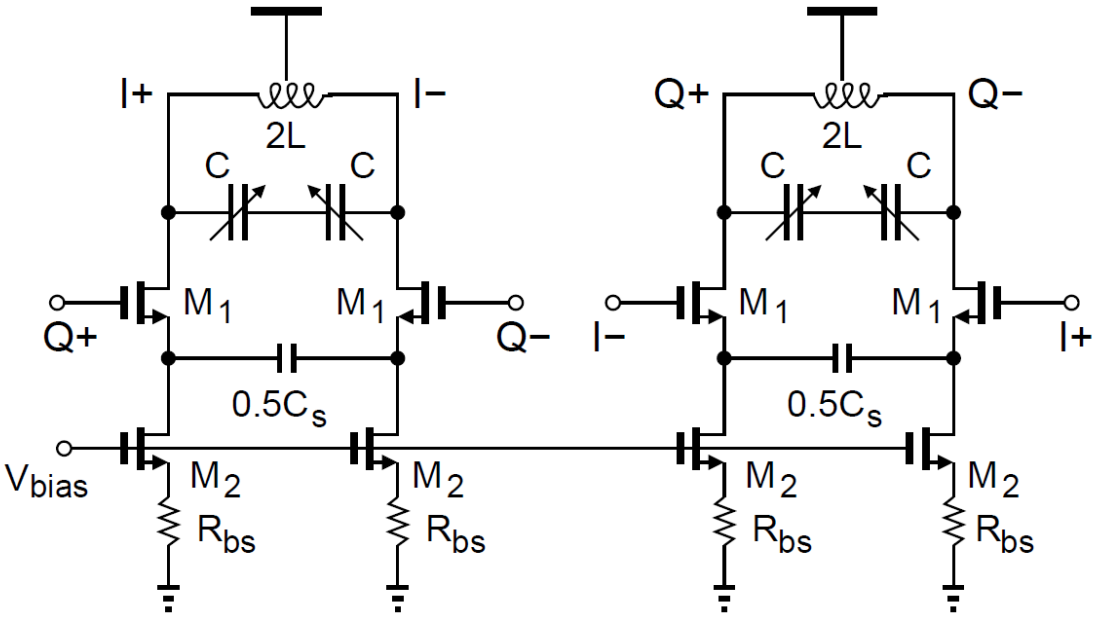


Fig. 4.11 Proposed CSD-QVCO.

$$\beta = \arctan\left(\frac{g_m}{\omega\left(C_s + C_{gs}\right)}\right)$$
$$\cong \arctan\left(\frac{g_m}{\omega \cdot C_{gs}\left(1+\frac{C_s}{C_{gs}}\right)}\right) = \arctan\left(\frac{\omega_T}{\omega}\frac{1}{\left(1+\frac{C_s}{C_{gs}}\right)}\right) \quad (4.56)$$

where ω_T is the input transistor's transition frequency expressed approximately as $\omega_T = g_m/C_{gs}$. According to (4.56), the phase shift is between 0◦ and 90◦, and it is determined by the ratios ω_T/ω and C_s/C_{gs}. Notice that the source degeneration capacitor C_s is noiseless and does not contribute any phase noise. The placement of the source degeneration capacitance between the two source nodes instead of from each source node to ground is chosen for the following reasons: (i) in the latter case, each

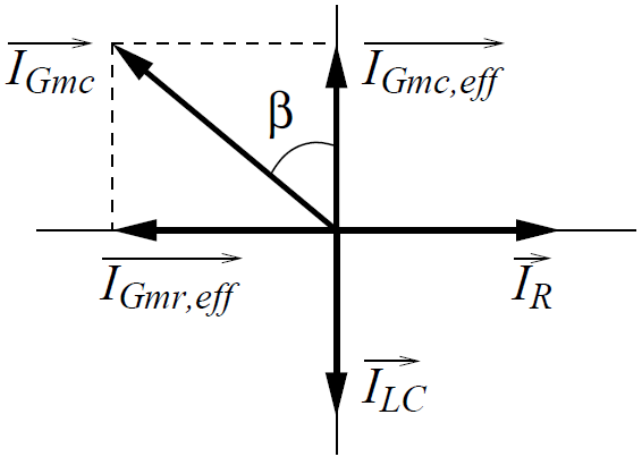


Fig. 4.12 Phasor diagram of the proposed CSD QVCO.

capacitance has to be doubled with area penalty, (ii) the oscillator would be subject to common-mode oscillation [42].

Fig. 4.12 shows the phasor diagram of the proposed CSD QVCO. The positive and smaller than 90° phase shift β allows only one oscillation, *Stage-I* lags *Stage-Q* and the oscillation frequency is lower than the resonance frequency. Intuitively, the current provided by the complex coupling transconductance can be decomposed as the effective negative transconductance current, $I_{Gmr,eff}$, and the effective coupling transconductance current, $I_{Gmc,eff}$, which can be expressed as

$$I_{Gmr,eff} = |I_{Gmc}| \cdot \sin(\beta) \tag{4.57}$$

$$I_{Gmc,eff} = |I_{Gmc}| \cdot \cos(\beta) \tag{4.58}$$

Similarly, according to (4.55), the effective negative transconductance, $G_{mr,eff}$, and the effective coupling transconductance, $G_{mc,eff}$, can be expressed as

$$G_{mr,eff} = \frac{\omega g_m^2 C_s}{g_m^2 + \omega^2 \left(C_s + C_{gs}\right)^2} \tag{4.59}$$

$$G_{mc,eff} = \frac{\omega^2 C_s \left(C_s + C_{gs}\right)}{g_m^2 + \omega^2 \left(C_s + C_{gs}\right)^2} \tag{4.60}$$

$G_{mr,eff}$ in (4.59) helps to compensate the loss of the LC tank. The input impedance Zin seen at the gate of M_1 can be obtained by

$$Z_{in} = \frac{1}{sC_s} + \frac{1}{sC_{gs}} + \frac{g_m}{s^2 C_s C_{gs}} = \frac{1}{sC_{eq}} + R_{eq} \tag{4.61}$$

where

$$C_{eq} = \left(\frac{C_s C_{gs}}{C_s + C_{gs}}\right), \quad R_{eq} = -\frac{g_m}{\omega^2 C_s C_{gs}} \tag{4.62}$$

The input impedance can be regarded as a capacitance C_{eq} series with a resistance R_{eq}, and the quality factor of the input impedance can be approximated as

$$Q = \frac{1}{\omega R_{eq} C_{eq}} = \frac{\omega\left(C_s + C_{gs}\right)}{g_m} \cong \frac{\omega}{\omega_T}\left(1 + \frac{C_s}{C_{gs}}\right) \tag{4.63}$$

The quality factor can be presented as the cotangent of phase shift β in equation (4.56). With the series-parallel transformation, the equivalent negative input resistance R_{in}, which serves as $1/G_{mr}$ for the preceding stage, is expresses as,

$$R_{in} = -\frac{1}{G_{mr}} = R_{eq}\left(1 + Q^2\right) = -\frac{g_m}{\omega^2 C_s C_{gs}}\left(1 + \frac{\omega^2 \left(C_s + C_{gs}\right)^2}{g_m^2}\right) \tag{4.64}$$

The equivalent parallel input capacitance C_{in} is expressed as

$$C_{in} = C_{eq}\frac{Q_{in}^2}{Q_{in}^2 + 1} = \left(\frac{C_s C_{gs}}{C_s + C_{gs}}\right)\cos^2\beta \tag{4.65}$$

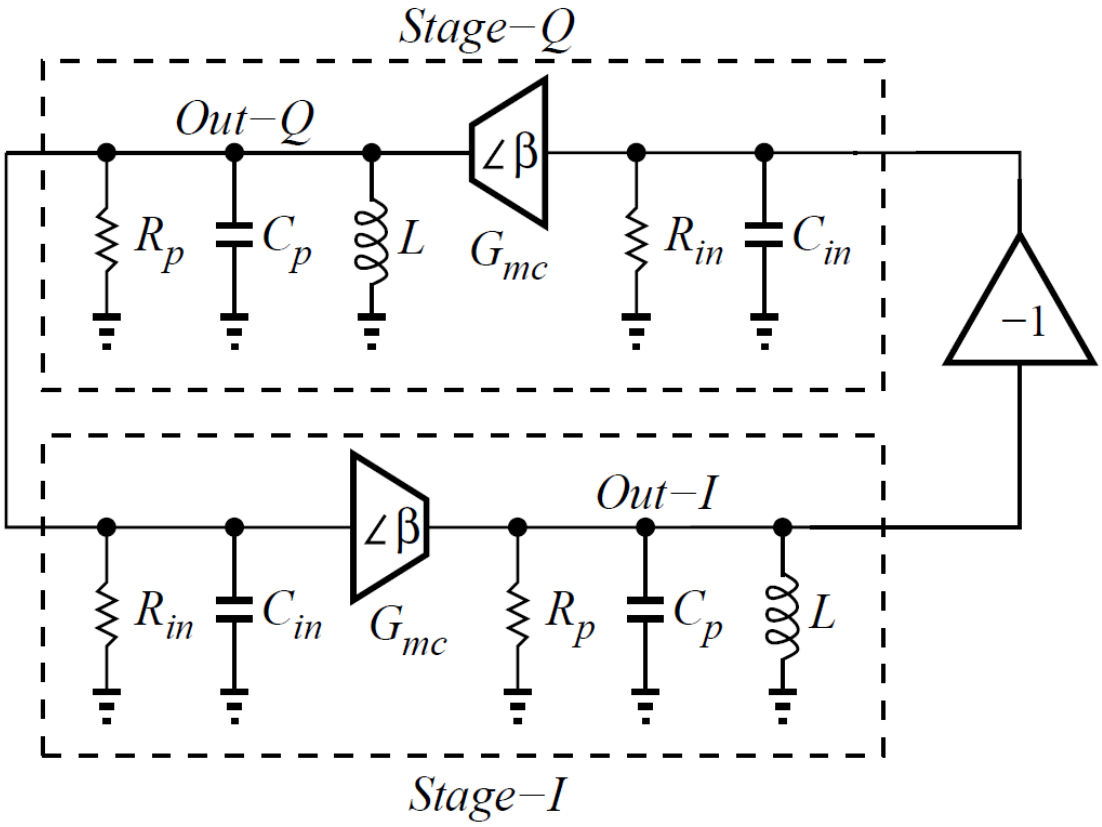


Fig. 4.13 Small signal model of the proposed CSD QVCO.

The proposed CSD-QVCO architecture can be modeled as shown in Fig. 4.13, where R_p, C_p and L are the equivalent parallel resistance, capacitance and inductance in the standalone LC tank, respectively. Using the CSD technique, the effective load resistance and capacitance, and the quality factor of the resonator can be expressed as

$$R_{eff} = R_p // R_{in} \tag{4.66}$$

$$C_{eff} = C_p + C_{in} \tag{4.67}$$

$$Q_{p,csd} = R_{eff}\sqrt{\frac{C_{eff}}{L}} \tag{4.68}$$

Note that R_{eff} is usually positive because it is very difficult to design R_{in} to compensate the loss of LC tank by itself. Besides, C_{in} is small compared to C_p, so the CSD-QVCO presents a large frequency tuning range.

The remarkable benefit present in the proposed architecture is that the commonly used positive feedback pairs are removed whereas the capacitive source degeneration differential pairs provide negative input impedance and phase shift for the coupling transconductance to compensate the energy loss in the LC tank.

Since the phase shift in both I and Q stage has to be 90◦ to meet the Barkhausen's phase criteria, the phase shift from the coupling transconductance and the resonator are complementary. Hence, the resonator phase shift can be written as

$$\phi = 90° - \beta = \tan^{-1}\left(\omega \frac{C_s + C_{gs}}{g_m}\right) \tag{4.69}$$

Equation (4.69) shows that making β closer to 90◦ reduces the resonator phase shift, so the oscillation frequency will be closer to the resonance frequency, and the effective quality factor of the LC tank will be larger, as long as the loop has enough gain to support the oscillation. The effective quality factor of the LC resonator can be approximated as

$$Q_{eff,csd} \approx Q_{p,csd} \cos\phi = \frac{Q_{p,csd}}{\sqrt{1 + \left(\omega_{osc} \frac{C_s + C_{gs}}{g_m}\right)}} \tag{4.70}$$

where ω_{osc} is the QVCO oscillation frequency. Equations (4.69) and (4.70) reveal that the effective quality factor of LC resonator is higher with β approaching 90◦.

A major advantage of the proposed QVCO is that it has low sensitivity to flicker noise present at the gate of transistors M_1 in Fig. 4.11. The capacitive degeneration makes

the differential pair to inherently reject the low frequency signals; the noise is shaped by an intrinsic high-pass filtering. In [43,44], it is found that flicker noise in bias transistors could be a main source for $1/f^3$ close-in phase noise. To reduce this noise, R_{bs} is inserted as source degeneration resistor in Fig. 4.11 to each bias transistor. Therefore, the noise current at bias transistor output is reduced by a factor of $(1+g_{mb}/R_{bs})^2$. Although increasing bias transistor size helps to reduce flicker noise also, the drain capacitance is increased with the penalty of smaller β and being more prone to common mode oscillation.

4.3.2 Phase Error

In the proposed CSD-QVCO, there is no negative cross-coupled transconductance but the coupling transconductance with capacitive source degeneration forms an active feedback to produce a negative transconductance G_{in} (=$1/R_{in}$) as shown in Fig. 4.13. The effect of the negative G_{in} is equivalent to that of the negative cross-coupled transconductance. Therefore, according to [34] the phase errors from the mismatch of resonant frequency ($\Delta\omega$) and the mismatch of coupling transconductance (ΔG_{mc}) in the CSD-QVCO can be approximated as

$$\Delta\phi_{\tan k} = Q_p \frac{1+m_{csd}^2+2m_{csd}\sin\beta}{m_{csd}\left(m_{csd}+\sin\beta\right)}\frac{\Delta\omega}{\omega} \tag{4.71}$$

$$\Delta\phi_{gmc} = \frac{\cos\beta}{m_{csd}+\sin\beta}\frac{\Delta G_{mc}}{2G_{mc}} \tag{4.72}$$

where

$$m_{csd} = \left|\frac{G_{mc}}{G_{in}}\right| \approx \frac{g_m}{\omega_{osc}C_{gs}}\sqrt{1+\omega_{osc}^2\left(\frac{C_s+C_{gs}}{g_m}\right)^2} \tag{4.73}$$

Equation (4.73) shows that if a fixed magnitude of G_{mc} is given for comparison, the coupling ratio m_{csd} of CDS-QVCO is much larger than mc of conventional QVCOs because the magnitude of negative transconductance in CSD-QVCO is smaller than the required G_{mr} in conventional QVCOs. Therefore, the quadrature phase accuracy of CSD-QVCO is less sensitive to mismatches in both tanks and coupling transconductances.

Table 4.1 shows the comparison of simulated phase errors between CSD-QVCO and the conventional QVCO with an ideal phase shifter (θ_{Tank} = 0◦) with no signal attenuation, and a coupling ratio m_c = 1 (strong coupling ratio). A 1% mismatch is given to the capacitance, coupling transconductance Gmc and negative cross-coupled transconductance G_{mr} between two *LC* oscillators. The simulation results show that CSD-QVCO has better phase accuracy even though an optimized phase shift and strong coupling are used in the conventional QVCO. It reveals that while most QVCOs burn more power to have a larger coupling ratio mc to improve the phase accuracy, the inherent large coupling ratio of CSD-QVCO can achieve excellent phase accuracy without paying the penalty of power consumption. Hence, in terms of performing good phase accuracy, CSD-QVCO is a very power-efficient solution.

The simulated phase errors of CSD-QVCO caused by mismatches in devices such as varactors, differential pairs and source degeneration capacitors are shown in Figs. 4.14, 4.15 and 4.16. If the phase error, for example, is required to be below 1◦, the mismatch of

Table 4.1 Phase accuracy comparison between conventional QVCO and CSD-QVCO.

	QSD-QVCO	Conventional QVCO $m_c = 1, \theta_{tank} = 0°$
1% mismatch in C	$0.64°$	$3.89°$
1% mismatch in G_{mc}	$0.26°$	$0.46°$
1% mismatch in G_{mr}	N/A	$1.34°$

the varactor and differential pair cannot surpass 4%, which can be easily achieved in this technology. The phase error resulting from the source degeneration capacitor mismatch is almost one order less than others.

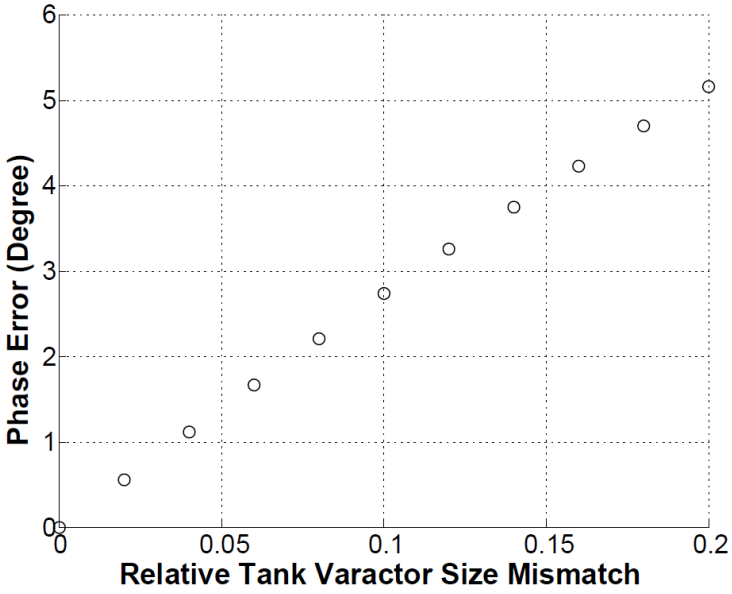


Fig. 4.14 Simulated phase error versus varactor size mismatch.

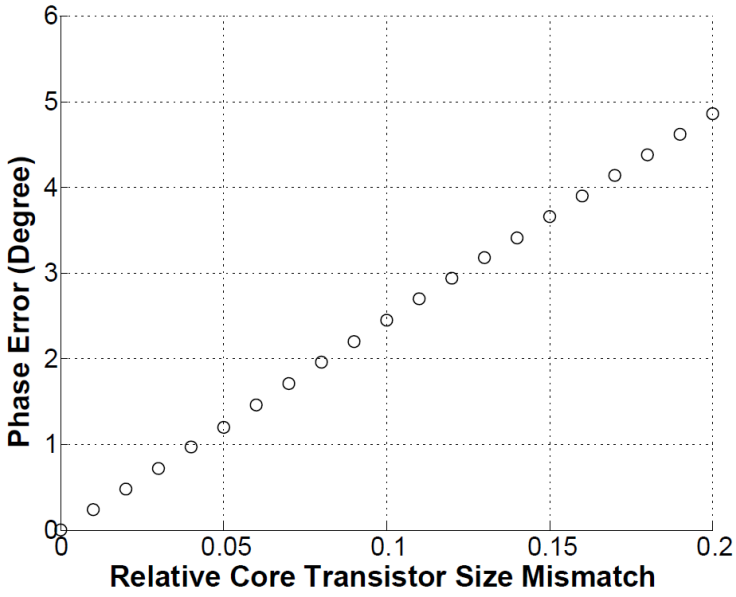


Fig. 4.15 Simulated phase error versus core transistor W/L mismatch.

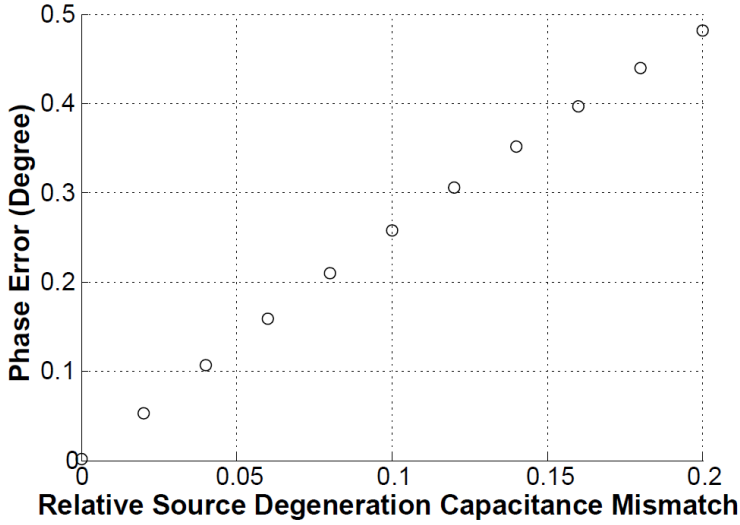


Fig. 4.16 Simulated phase error versus source degeneration capacitor mismatch.

4.3.3 Measurement Results

The simulated quality factor of the inductor is around 12 at 5 GHz. Fig. 17 shows the micro photograph of the 5-GHz CSD-QVCO with buffers, fabricated using TSMC 0.18-μm CMOS process. The CSD-QVCO is powered by a 1.2-V supply and consumes 5.2-mA current. The total chip area is 930 × 2000 μm^2 including the contact pads. The oscillator occupies 550 × 1100 μm^2. The measurement was performed on a standard FR4 PC board. One of the four CSD-QVCO outputs was picked up by a SMA connector, with other outputs each terminated with a 50 resistor. A voltage regulator was mounted to provide clean supply voltage. The CSD-QVCO presents a phase noise of -120 dBc/Hz at 3-MHz offset from 5-GHz center frequency, with a power consumption of 6.4 mW from a 1.2-V supply. Compared to existing phase shift *LC* QVCOs, the CSD-QVCO presents excellent phase accuracy and power efficiency.

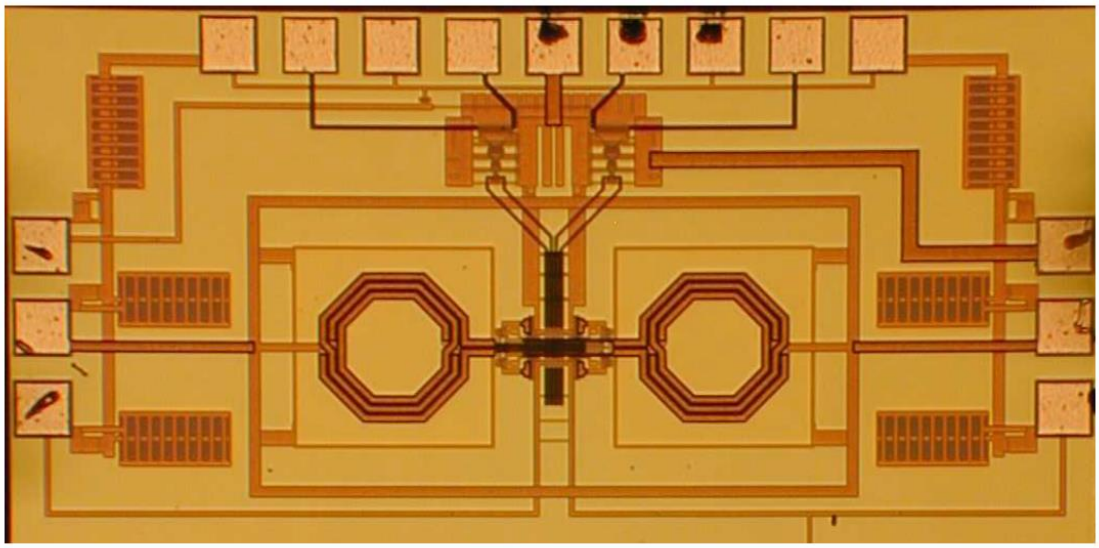


Fig. 4.17 5-GHz CSD-QVCO chip microphotograph.

4.4 QVCO Using Dynamic Current-Clipping Coupling

It has been shown that implementing a larger coupling ratio can reduce the sensitivity of the quadrature phase error with respect to the mismatches between the two oscillator stages. However, as aforementioned, a larger coupling ratio usually makes the coupling network increase more noise, harming the phase noise performance. Therefore, a coupling element design to break the tradeoff between phase noise and phase accuracy is desirable. Since a phase shift around 90 degree is needed in the coupling to not only improve the phase noise performance but also minimize the quadrature phase sensitivity to mismatches, as shown in the Fig. 4.18(a), the ISF should be shifted by 90 degree as well. Hence, if the noise generated by the coupling element can be confined at the less

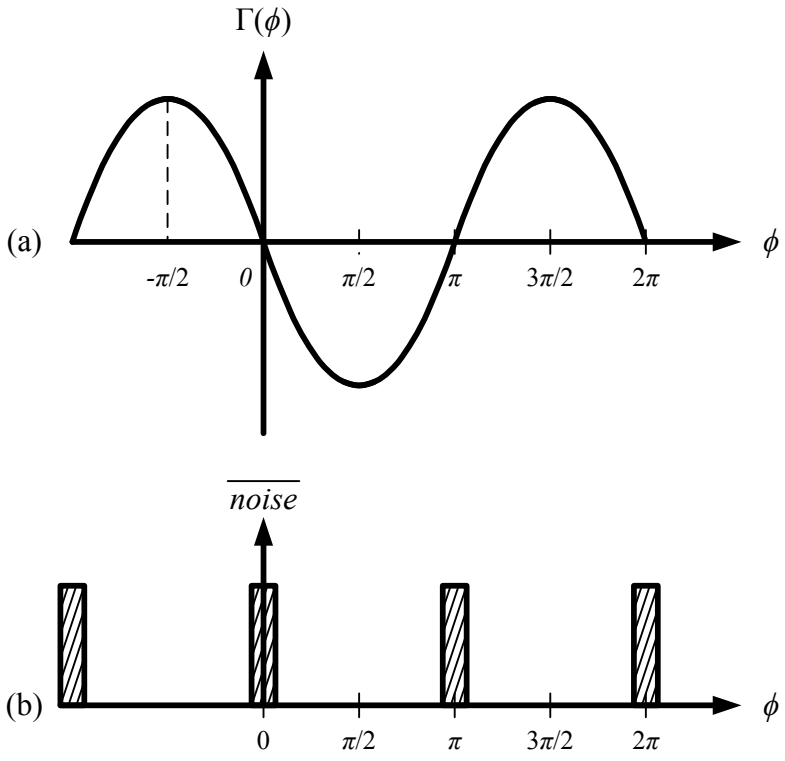


Fig. 4.18 Minimized noise from coupling network.

sensitive VCO timings as shown in the Fig. 4.18(b). As a result, increasing the coupling ratio will has less impact on VCO phase noise performance.

4.4.1 Dynamic Current-clipping Coupling QVCO Design

Fig. 4.19 shows the proposed QVCO which has two conventional *LC* oscillators with dynamic current-clipped coupling branches. The coupling branch is built up by two cascoded transistors and a source degeneration resistor. The gate terminal of the transistor M_{Cup} and M_{Cdn} are connected to the outputs of the other oscillator stage such that this branch is active during the crossing times of the signals connected to the gates. The operation of the coupling network can be roughly divided into four regions as

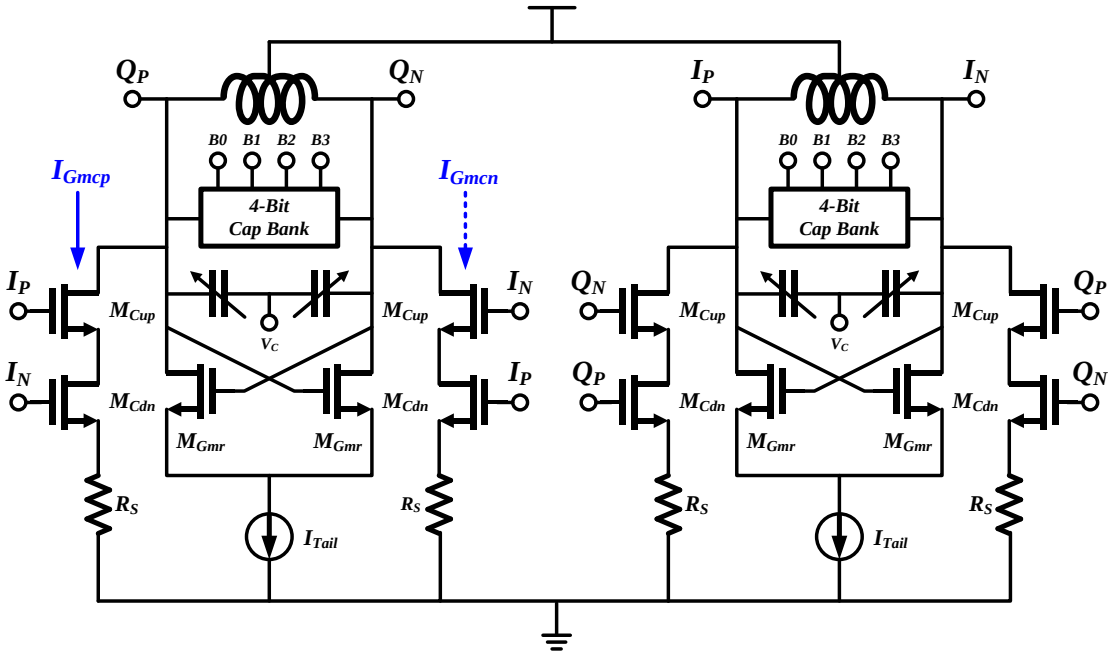


Fig. 4.19 Proposed QVCO with dynamic current-clipping coupling technique.

shown in the Fig. 4.20. In the Region I, the upper transistor connected to I_P is on but the bottom transistor connected to I_N is off so no coupling current I_{Gmcp} in the left branch will inject into the *LC* oscillator. Meanwhile, in the right branch, the upper transistor connected to I_N is off block the coupling current I_{Gmcn} flowing into the *LC* oscillator. Similarly, with the condition reversed, no current injects into *LC* tank in the Region III. The coupling network only injects the current into the LC oscillator in the region II and

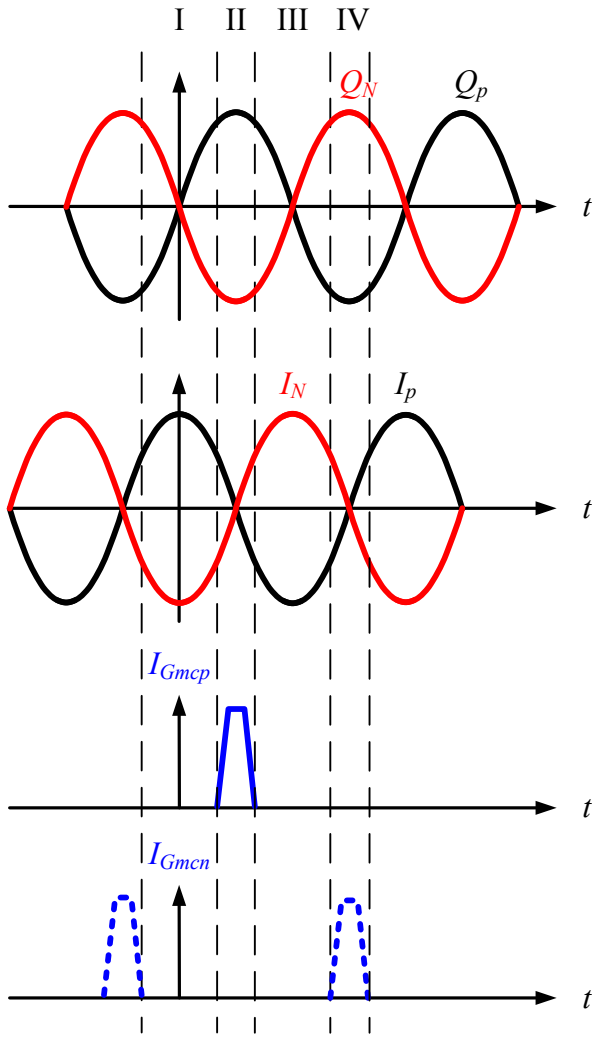


Fig. 4.20 Operation regions of coupling element.

IV where both transistors are on. In the Region II, the Q_P reaches its maximum voltage so large I_{Gmcp} injects into LC tank through the left branch while Q_N approaches its lowest voltage and little I_{Gmcn} appears. Similarly, the major current injecting into the LC tank in the Region IV is from I_{Gmcn}. Hence, as shown in Fig. 4.21, the coupling network injects the differential current around the peaks of the oscillator outputs and shifts the coupling current by around 90 degrees to enhance both phase noise and phase accuracy performance. The proposed coupling topology also exhibits better power-efficiency because the 90-degree phase-shifted coupling transconductance assists the regenerative transconductance to compensate the loss of LC tank and only dynamic power is dissipated. Unlike that some RC phase shifters would load a resistor at LC tank, the proposed coupling architecture does not significantly degrade the quality factor of LC tank. In this design, the coupling ratio is defined as the ratio of the power consumption dissipated by the coupling network to that dissipated by the LC oscillator.

The noise mechanism of the coupling branch is illustrated in Fig 4.22. In Region I, M_{Cdn} is off, so M_{Cup} seems to tie with a huge source degeneration resistor. The noise of M_{Cup} will circulate in M_{Cup} itself and output almost zero noise current into the LC tank. On the other hand, while M_{Cup} is off in the Region III, M_{Cup} blocks the noise current generated by M_{Cdn}. Therefore, almost no noise current flows into the LC tank at the most vulnerable timings, the zero-crossing points of the oscillator's differential outputs. The noise contribution from coupling network only occurs at the region II; however, the noise has less impact on the phase noise according to the ISF of the oscillator. The source degeneration resistor R_S is used to further reduce the flicker noise and assist

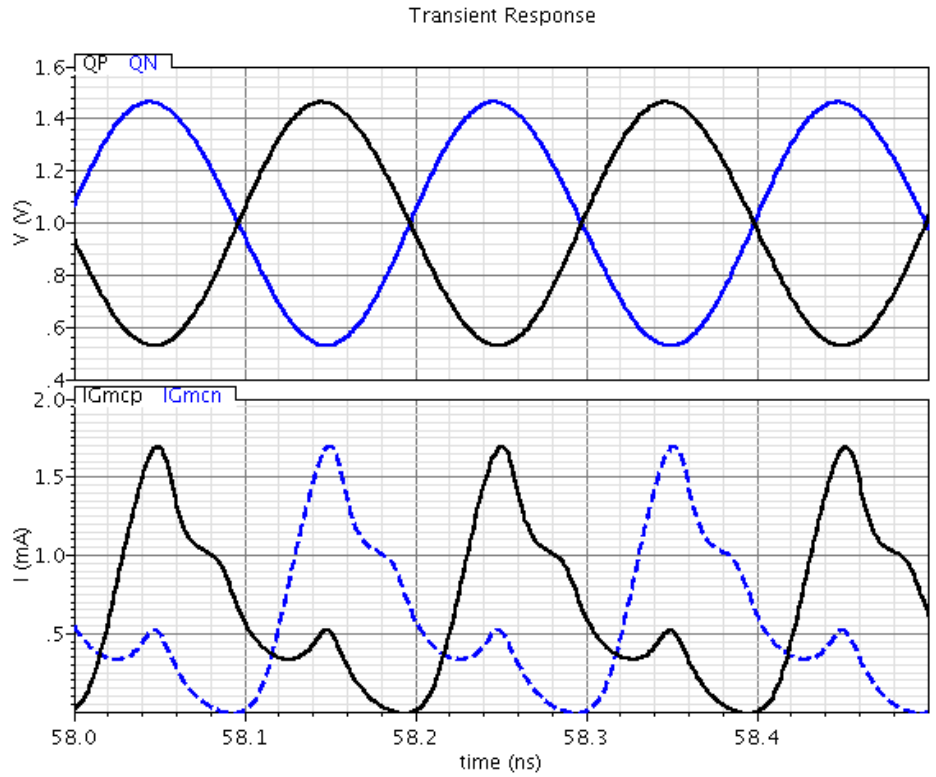


Fig. 4.21 The simulated output voltages (top trace) and coupling currents (bottom trace).

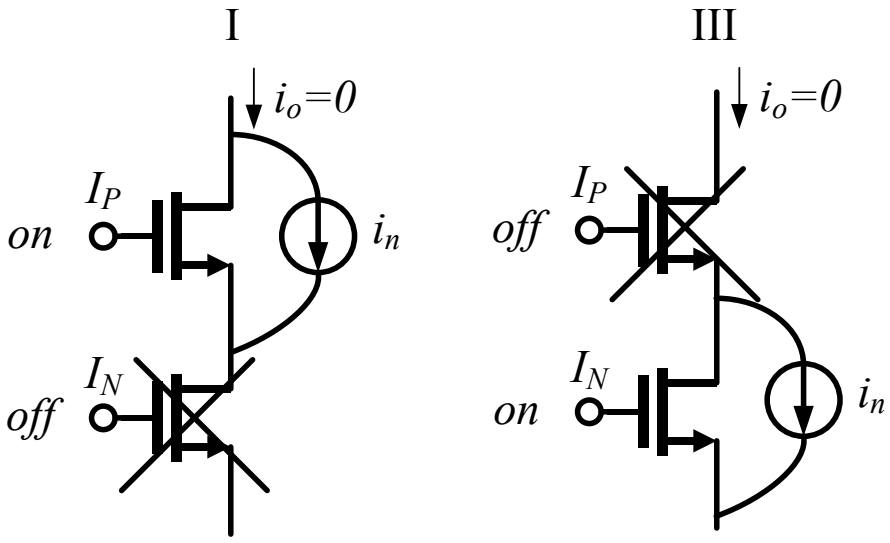


Fig. 4.22 Noise behavior of coupling element.

turning off the M_{Cdn} faster when in Region I. Thus, the noise from the coupling network does not drastically degrade the phase noise performance. This sophisticated coupling network not only provides a phase shift around 90 degree to make the QVCO less sensitive to noise and mismatches, but also allows the use of large coupling ratio to improve the phase accuracy without suffering the phase noise penalty. The proposed coupling network consuming only dynamic power make it a low-power solution for quadrature signal generation.

4.4.2 DCC QVCO Measurement Results

The proposed QVCO was fabricated 0.13-μm CMOS technology. The die microphotograph of the chip is shown in Fig. 4.23. The core area of the QVCO is 0.27 mm^2. The simulation results show a center-tapped inductor quality factor of around 15. A 4-bit capacitor bank and a 125-fF varactor are implemented in the QVCO to achieve a frequency tuning range from 4.4 GHz to 5.4 GHz. The coupling ratio *m* is designed as 0.8 to suppress the sensitivity to mismatches. Monte-Carlo simulations show that quadrature phase error standard deviation is around 0.1 degree. The coupling network provides at least around 75 degrees phase shift over the PVT variations.

The power consumption of the QVOC is 4.2 mW with a 1-V power supply. Fig. 4.24 shows the measured phase noise response measured at a frequency of 5 GHz. The phase noise is -120.9 dBc/Hz at 1MHz offset. The flicker noise corner is around 20 KHz, showing that the flicker noise contribution is confined to very low frequencies; phase noise is around -70 dBc at 10KHz offset frequency. Fig. 4.25 shows the measured output

waveforms of quadrature signals. Table 4.2 compares the proposed QVCO with prior works using various phase shift techniques. The proposed QVCO shows outstanding phase noise performance and power consumption, reaching an excellent FoM of 189 dBc.

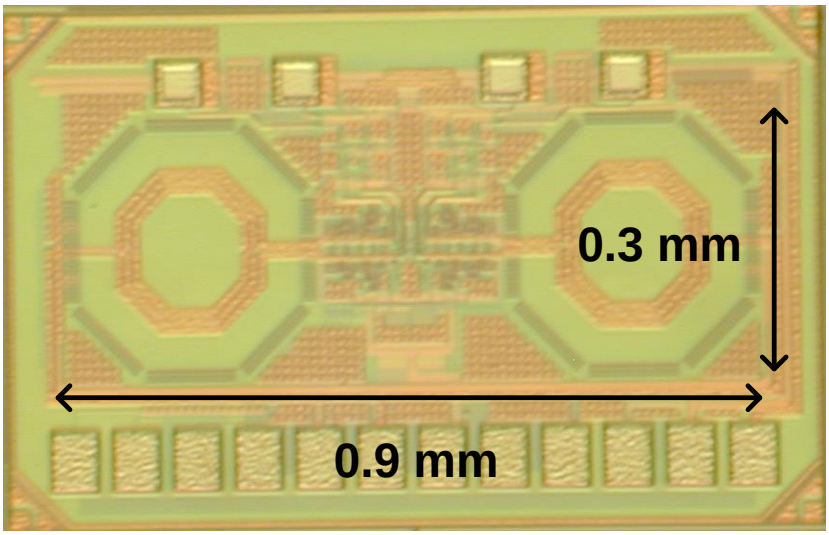


Fig. 4.23 Chip microphotograph.

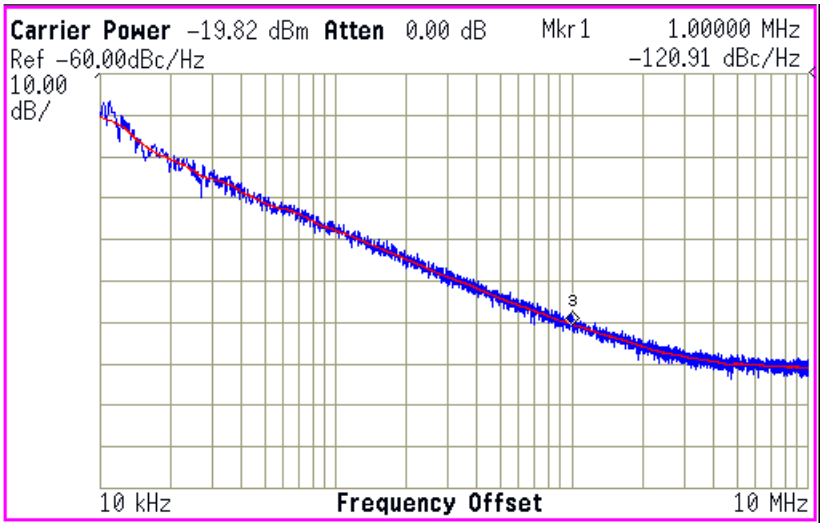


Fig. 4.24 Measured phase noise.

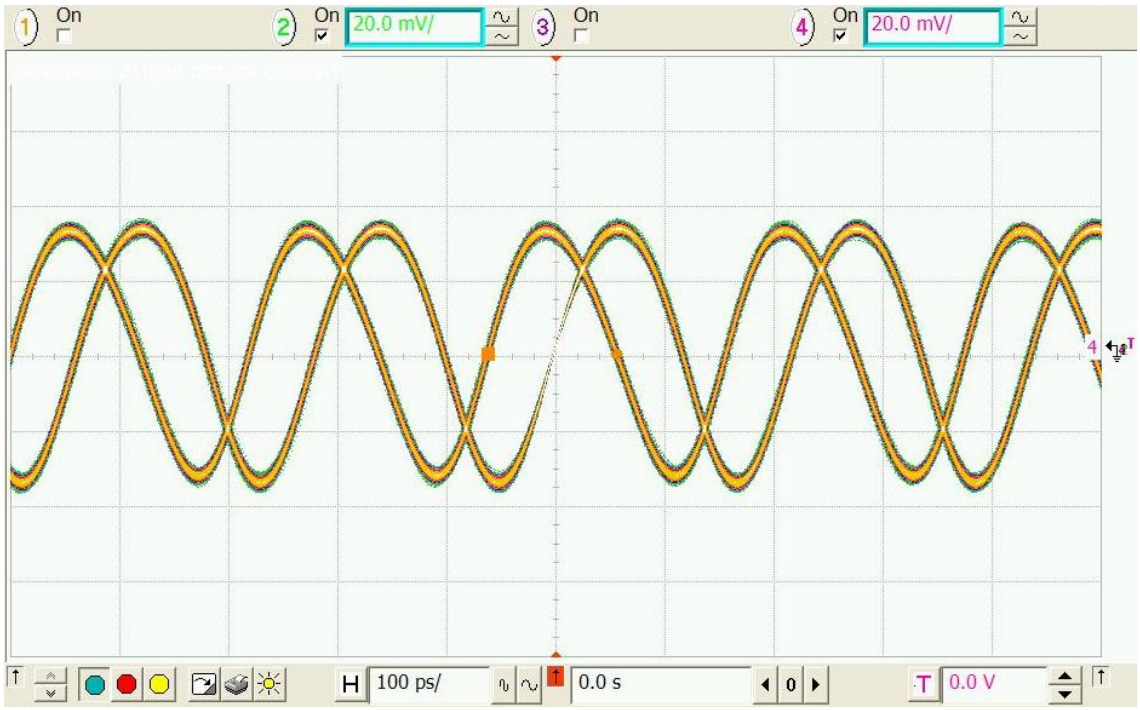


Fig. 4.25 Measured quadrature signals.

Table 4.2 Comparison with previously reported QVCOs.

	Technology (μm)	Frequency (GHz)	Supply Voltage (V)	Power (mW)	Phase Noise (dBc/Hz)	FoM (dBc)
2008 MWCL [45]	CMOS 0.18	7	1	2.2	-111.2@1MHz	185
2011 JSSC [26]	CMOS 0.13	5.2	1.2	7.7	-115@1MHz	179.5
2012 TCAS [46]	CMOS 0.18	5	1.2	6.4	-120@3MHz	176
This work	CMOS 0.13	5	1	4.2	-121@1MHz	189

CHAPTER V

COMPLIMENTARY INJECTION-LOCKED FREQUENCY DIVIDERS*

5.1 Introduction

Frequency dividers (FDs) are a basic but critical building block of phase-locked loops (PLLs) in various high-speed wireline and wireless communication systems. In addition to frequency transition, FDs may have to provide various division moduli and multiple phases for certain applications. Conventional flip-flop-based FDs are robust and broadband but their power consumption are excessive especially for high-speed operations. Injection-locked frequency dividers (ILFDs) [47, 48] are a low-power alternative for applications in the range of several tens of gigahertz. The concept of injection locking was originated from the phenomenon of VCO pulling. It is illustrated in Fig. 5.1 where an injection signal whose frequency is close to the oscillation signal's frequency. The injection would disturb the oscillation signal and generate spurious tones. If the injection frequency is close to the oscillation frequency or its harmonic, and the injection signal is large enough, the oscillation frequency can be pulled away by the injection signal and locked at the frequency of the injection signal.

The injection-locking phenomenon was used to implement frequency division [48]. The operation of injection-locked frequency dividers can be illustrated by Fig. 5.2. An injection signal fin and a feedback signal generated by the divider output were given

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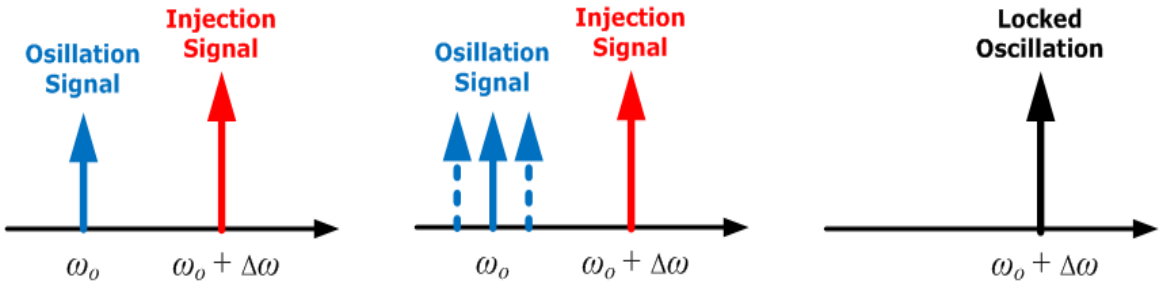


Fig. 5.1 Illustration of injection-locking phenomenon.

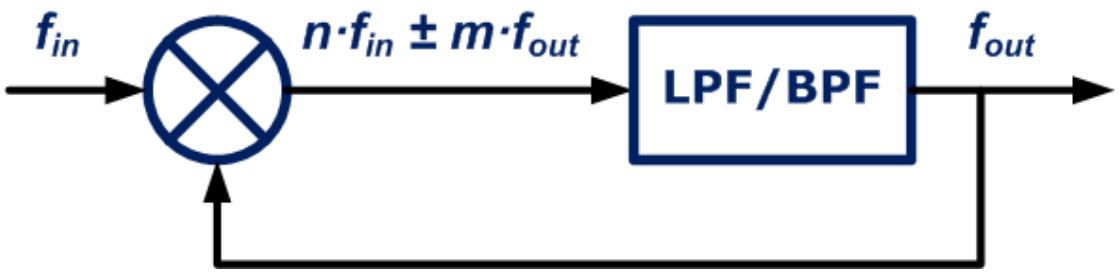


Fig. 5.2 Injection-locked frequency divider.

in the mixer inputs. The mixer would generate the combination (summation or subtraction) of the harmonics of the injection signal and divider output signal. A filter is implemented after the mixer to select the desired signal and attenuate the unwanted signals. The output frequency of the injection-locked frequency divider can be expressed as

$$f_{out} = \frac{n}{1 \pm m} f_{in} \tag{5.1}$$

Injection-locked dividers can be classified into LC-based ILFDs and Ring-oscillator-based ILFDs. LC-based ILFDs (LC-ILFDs) can usually operate at very high speed [49, 50] and they have more optimal noise performance due to their band-pass LC filtering characteristic. However, the area penalty is significant due to the inductor used;

furthermore, the division ratio cannot be large within one LC tank load. Small division ratio implies that several LC-ILFDs are needed for converting very high frequency down to the desired frequency. Also, the low quality factor Q of the LC tank to widen the locking range costs additional power consumption. Even if a low-Q LC tank is used, the locking range usually cannot cover the PVT variations; thus, some additional control or feedback circuits are required to adjust the free running frequency to ensure the LC-ILFDs locked. These expensive and complicated controls make the LC-ILFDs unfavorable for practical applications.

Ring-oscillator-based ILFDs (Ring-ILFDs) feature wider locking ranges, smaller silicon area and larger division moduli [51, 52, 53, 54]. Ring-ILFDs' operation frequencies are mainly determined by the dimension of the devices and the power consumption. Although the phase noise of the conventional ring-oscillator is poor, the noise performance of ring-ILFDs can be further improved by injecting a clean signal [55]. In order to widen the locking range, to overcome PVT variations, the multiple-input injection technique for Ring-ILFDs with even division ratios has been proposed [52, 53]. However, the locking range of Ring-ILFDs with odd division ratios can rarely overcome the PVT variations. Usually when the number of ring-oscillator stages increases, the locking range shrinks drastically [56]. Since large division ratios can relax the speed and power in the following building blocks, to widen the locking range of large odd-division-moduli Ring-ILFDs is still desired. Table 5.1 summarizes the comparison between LC –ILFDs and Ring-ILFDs.

In this chapter, a new ring-oscillator-based complementary-injection-locked frequency divider (CILFD) is presented. The multiple-input complementary-injection

achieves large odd division ratios and wide enough locking range to overcome the process variations without tuning the free running frequency. The power consumption overhead is negligible for larger division modulus. The CILFDs provide differential outputs due to the cross-connected inverters.

Table 5.1 Comparison between LC-ILFDs and Ring-ILFDs.

	Power Consumption	Speed	Locking Range	Area	Noise	Odd Modulus	Multiple Phases
***LC* Type**	**Low**	**High**	**Smaller**	**Large**	**Better**	**No**	**No**
Ring Type	**High**	**Low**	**Small**	**Small**	**Worse**	**Yes**	**Yes**

5.2 Complementary Injection-Locked Frequency Dividers

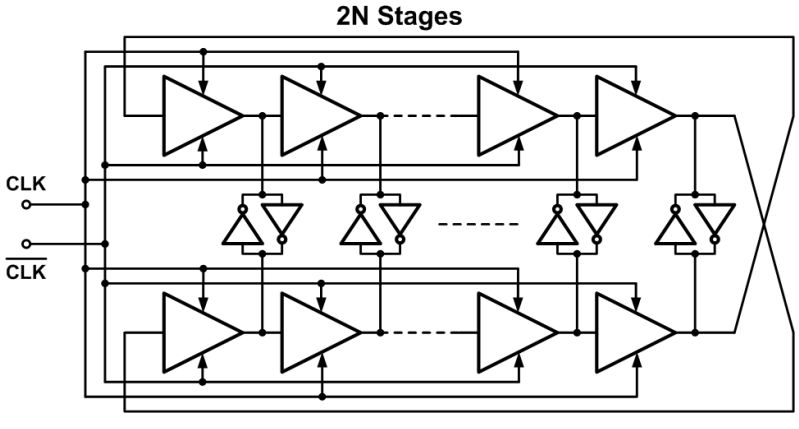
It is extremely difficult to have an odd-modulus Ring-ILFDs whose locking range can overcome PVT variations. When an ILFD is under locking, the ILFD has to satisfy "Barkhausen Criteria"

$$\left|H\left(j\omega_{inj}\right)\right|>1,\ \angle H\left(j\omega_{inj}\right)=180° \tag{5.2}$$

From small signal analysis perspective, the Ring-ILFD can be expressed as

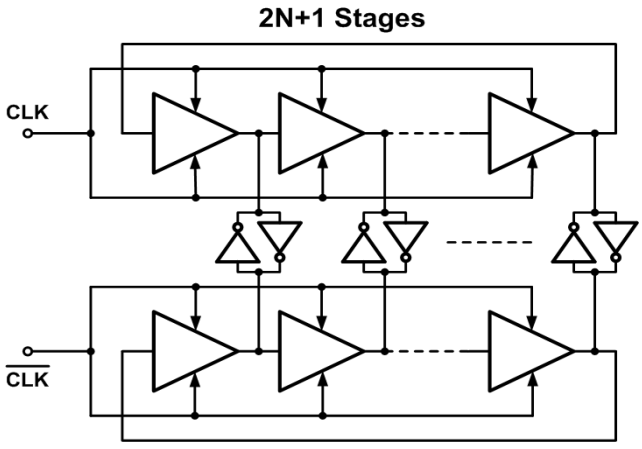
$$H\left(j\omega_{inj}\right)=\left(-1\right)^{n}\frac{A_0^n}{\left(1+\frac{j\omega_{inj}}{\omega_p}\right)} \tag{5.3}$$

It can be observed that if a wider locking range is required, the pole location in equation (5.3) has to be tunable for satisfying the phase criteria of the Barkhausen Criteria under different injection signal frequency. It can be also interpreted from a large signal perspective. The delay of each ring oscillator stage has to be varied with the injection signal frequency.

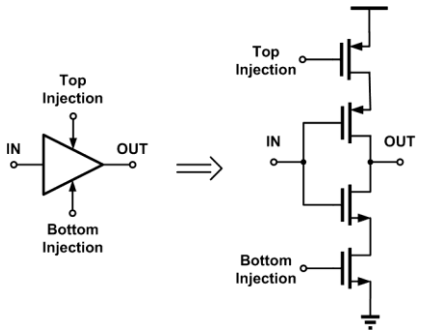


(a)

Fig. 5.3 (a) even-modulus CILF; (b) odd-modulus CILFD; (c) unit delay cell.



(b)



(c)

Fig. 5.3 Continued.

The proposed over 100% locking range complimentary injection-locked frequency dividers are shown in Fig. 5.3. Fig. 5.3(a) shows CILFD with even-modulus. 2N-stage unit delay cell is needed for the division operation of 2N. The odd-modulus CILFD is shown in Fig. 5.3(b). The unit delay cell is shown in Fig. 5.3(c).

The operation of odd-modulus CILFD can be simply explained in Fig. 5.4. Fig. 5.4 shows the proposed divide-by-3 complementary-injection-locked frequency divider. The divide-by-(2N+1) CILFD can be realized by using (2N+1) ring-oscillator stages (N is a prime number). Every ring-oscillator stage (delay cell) has an upper tail-injection

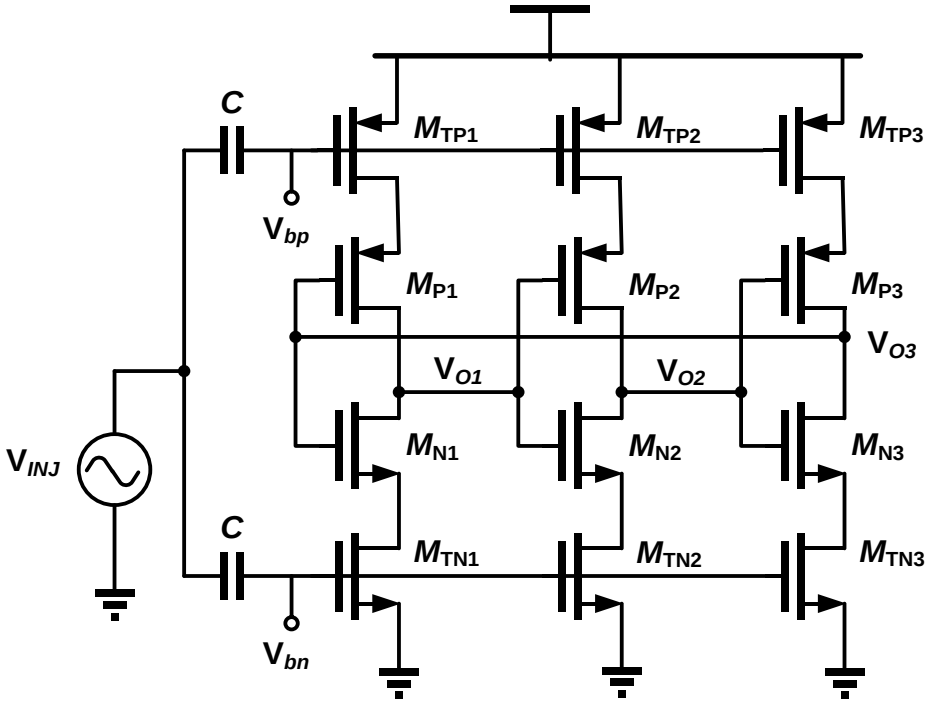


Fig. 5.4 Divide-by-3 complementary injection-locked frequency divider.

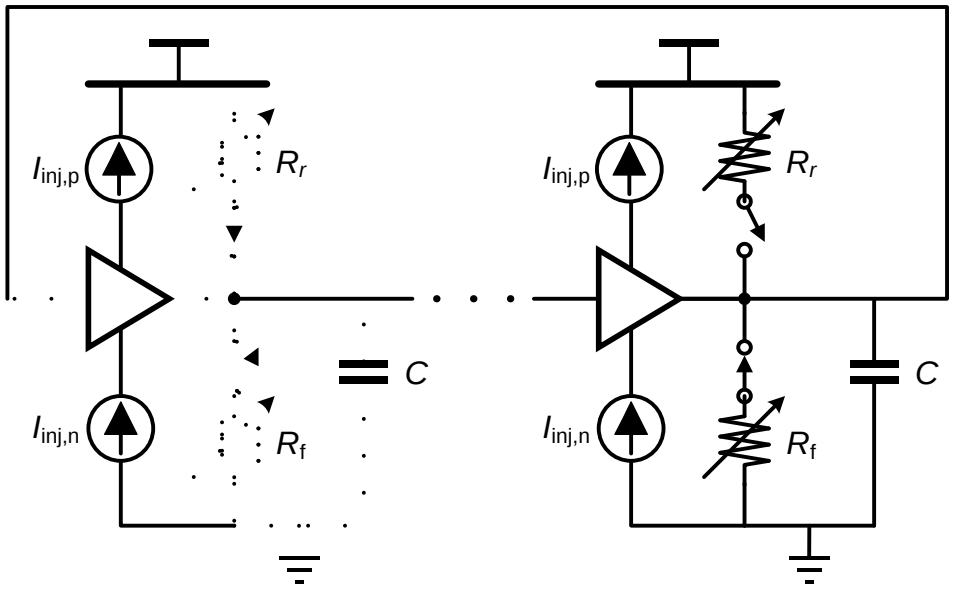


Fig. 5.5 Simplified circuit model of a CILFD.

transistor, $M_{TP,n}$, and a bottom-injection transistor, $M_{TN,n}$. The inverter, $M_{P,n}$ and $M_{N,n}$, is placed between the upper and bottom tail transistors. The free-running frequency of the ring-oscillator is controlled through the DC bias voltage at the gate terminals of tail transistors. Increasing the $|V_{gs}|$ of tail transistors draws more tail current and hence reduces the delay of each ring-oscillator stage to increase the oscillating frequency. The injection signal is coupled by the capacitors connected to the gate terminals of the tail transistors.

The conceptual circuit model of a divide-by-(2N+1) CILFD is shown in Fig. 5.5 Each ring-oscillator stage consists of a transconductor, an effective current-controlled resistor R_f that discharges the load capacitor C and an effective R_r that charges the load capacitor. In order to simplify the analysis, the time-variant characteristic of R_r and R_f is ignored. Instead, R_r and R_f stand for the effective time-average resistance values during the rising and falling transitions; this approximation allows us to obtain simpler expression for propagation delay computations. $I_{inj,n}$ and $I_{inj,p}$ represent the injection currents from a bottom NMOS tail transistor and an upper PMOS tail transistor, respectively. The injection through NMOS and PMOS is named complementary injection. Notice that the equivalent values of R_r and R_f vary with the tail currents. If the loop gain satisfies the Barkhausen criteria, the free-running frequency of the (2N+1)-stages ring-oscillator can be approximated as

$$f_{osc} \cong 1/[(2n+1)(t_{pdr} + t_{pdf})] \tag{5.4}$$

where t_{pdr} and t_{pdf} are the rising and falling propagation delays and can be modeled as R_rC and R_fC, respectively.

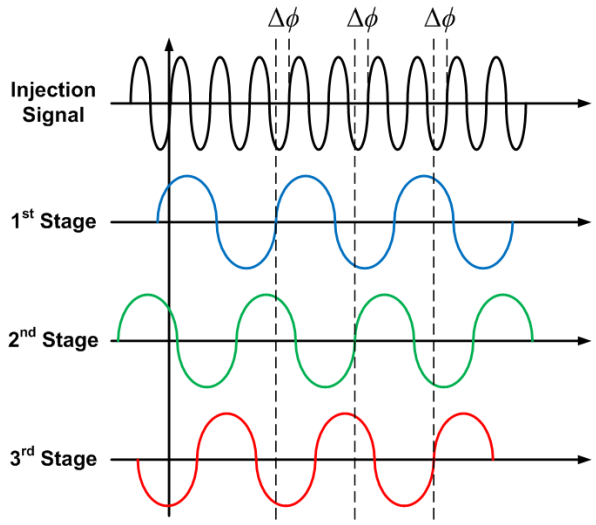


Fig. 5.6 The output waveforms of injection signal and each ring stage when CILFD is under locking.

While the signal is injected, it produces both amplitude and phase variations at the outputs of CILFD and alters the load impedance of each stage. If the negative-feedback loop is able to reach steady state, the CILFD will be locked to a sub-harmonic of the injection signal. Since the division ratio is usually the same as the number of ring-oscillator stages, the fixed phase shift $\Delta\varphi$ is between each ring oscillation stage output and injection signal as shown in Fig. 5.6. Also, an equal phase shift Φ exists between each inverter and its tail transistor as shown in Fig 5.7.

Also, an equal phase shift Φ exists between each inverter and its tail transistor as shown in Fig 5.6. If I_T is defined as the tail current in free-running state, I_{INJ} as the current drawn by the injection signal and I_{OSC} as the effective tail current while the system is locked. The phase shift Φ can increase or decrease the effective upper or bottom tail currents as shown in Fig. 5.7. The variation of the effective tail currents

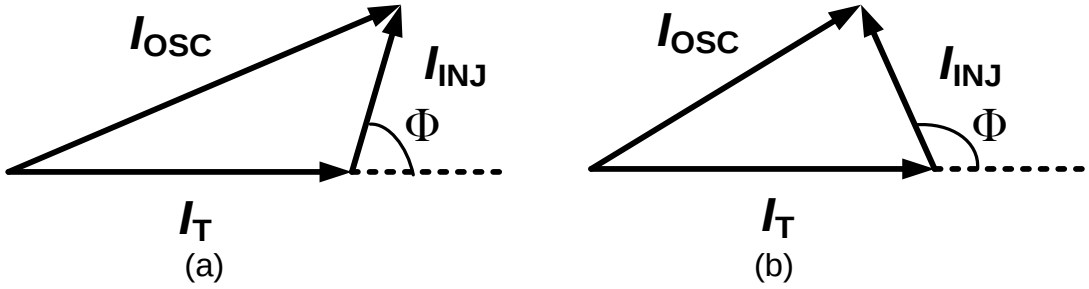
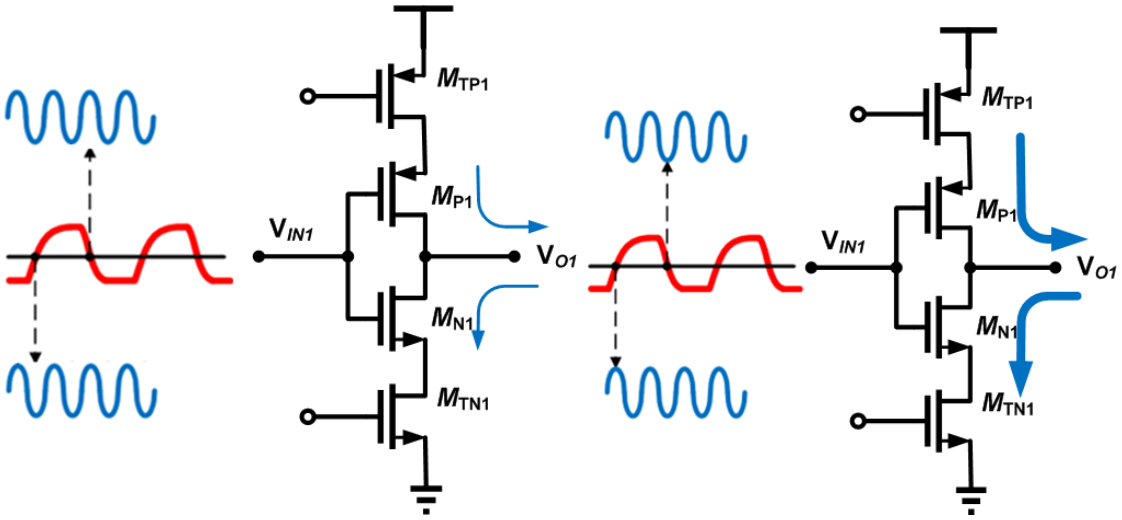


Fig. 5.7 Geometrical interpretation of complementary injection. A phase shift (a) to increase oscillation frequency (b) to decrease oscillation frequency.

changes the effective R_r and R_f, or equivalently the rising and falling propagation delay to meet the injection frequency. Intuitively, the boundaries of locking range can be obtained from the geometrical interpretation. The existing smallest and largest phase shifts determine the maximum and minimum locking oscillation frequencies, respectively. Fig. 5.7 also illustrates how increasing the ratio of I_{INJ} to I_T widens the percentage of locking range. Since the amplitude of injection signal is limited, a proper selection of I_T optimizes the tradeoff between the locking range and operating frequency. Due to the characteristic of ultra-wide locking range, the CILFD is able to cover PVT variations with a small I_{INJ} to save power on the buffer stages. Fig. 5.8 shows the operation of CILFD under maximum and minimum oscillation frequencies. The peak tail current is given at maximum oscillation frequency and the minimum current is given at minimum oscillation frequency.

In order to realize a differential-input and output CILFD structure and to take full advantage of the differential nature of *LC* VCOs, auxiliary cross-connected inverter pairs are used to couple two CILFDs as shown in the Fig. 5.9. The cross-connected inverters



(a) (b)

Fig. 5.8 CILFD is operated at (a) maximum frequency and (b) minimum frequency.

provide current injection to each other to vary the phases and force the two CILFD outputs to stay out of phase during steady state conditions.

The CILFDs' wide locking range is a result of the use of complementary and multiple-input signal injection. The N-and-P complementary-injection scheme not only increases the effect of the injected signal into the ring-oscillator but also simultaneously drives both the rising and falling propagation delays, unlike the conventional injection mechanisms that vary the falling propagation delays only [56, 57]. Therefore, the complementary injection offers the advantages of more control on the ring-oscillator oscillation frequency and wider locking range. Simulations results for a divide-by-7 CILFD are shown in Fig. 5.10; notice that the injection currents complement each other and occur only during rising and falling transitions.

The combination of the complementary injection and multiple-input injection points avoids the interference from stage to stage, attenuates the injection signal at the

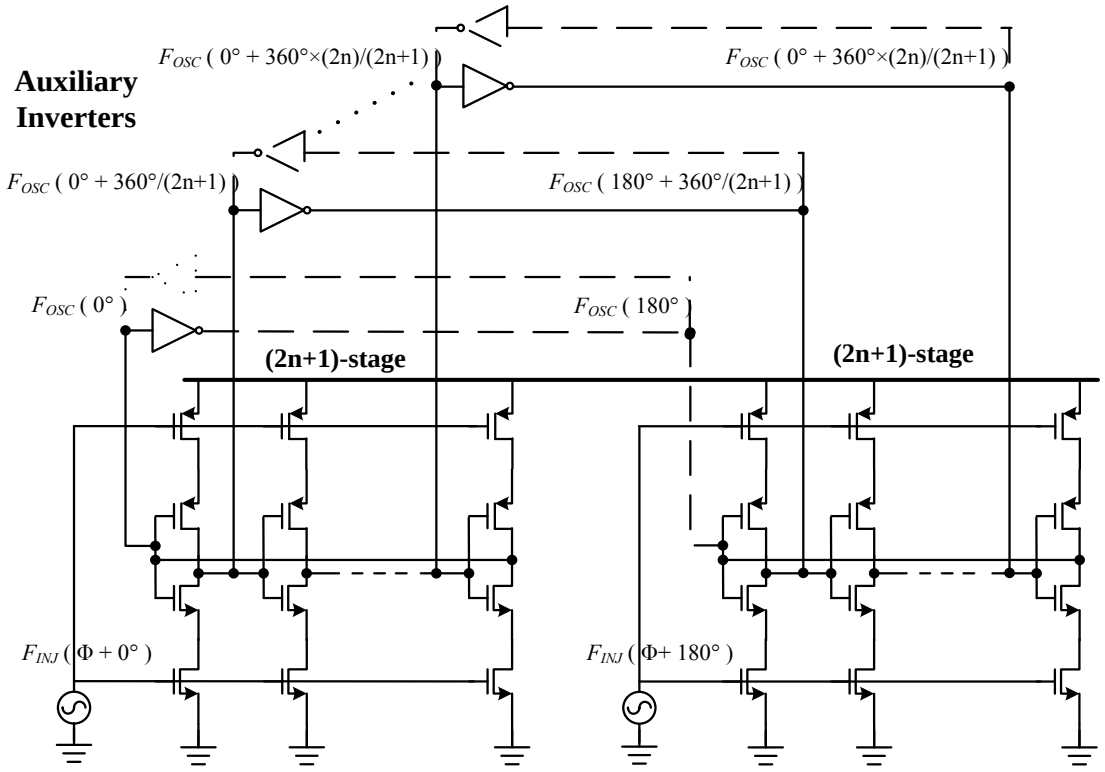


Fig. 5.9 A divide-by-(2n+1) differential CILFD.

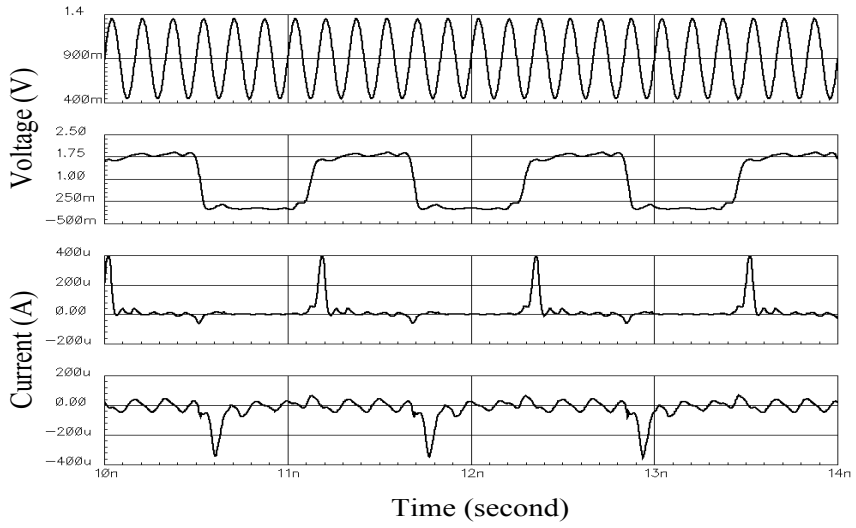


Fig. 5.10 Simulated waveforms from top to bottom (a) injection signal, (b) voltage in one of the nodes of the ring-oscillator, (c) NMOS tail transistor current, (d) PMOS tail transistor current.

unwanted timings, blocks the crosstalk between upper and bottom tail transistors, and allows us to control both transition times t_{pdr} and t_{pdf}. As a result, wider locking range is achieved even in the case of large-division-ratios CILFDs.

The CILFD consumes dynamic power only due to the nature of the complementary injection locking scheme. The power consumption of a single ring-oscillator stage under locking with a divide-by-(2n+1) ratio can be approximated as

$$P_{stage} \cong 2CV_{DD}^2 f_{inj} /(2n+1) \tag{5.5}$$

Equation (5.5) multiplied by the number of ring-oscillator stages gives the total power consumption of the CILFD:

$$P_{total} \cong 2CV_{DD}^2 f_{inj} \tag{5.6}$$

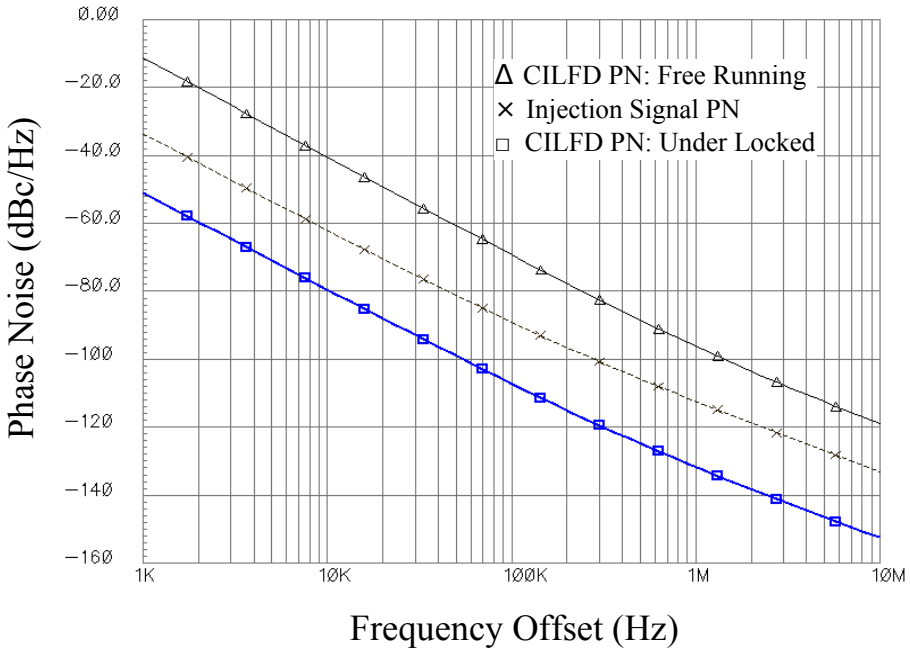


Fig. 5.11. Simulated phase noise. From top to bottom (a) free running CILFD, (b) injection signal, and (c) locked CILFD.

Expression (5.6) shows that the power consumption of the CILFD is independent of its division ratio (the number of ring-oscillator stages) but proportional to the frequency of the injected signal. The CILFDs are then favorable for the use of large division ratios. It is well known that the ring-oscillators present poor phase noise due to their inherent low-Q of each stage. However, Ring-ILFDs' internal stages phase noise is high-pass filtered by the loop dynamics. When locked, the phase noise of Ring-ILFDs is mainly determined by the phase noise of the injection signal [55]. The close-in phase noise of a CILFD can then be approximated as

$$PN(ILFD) \cong PN(Injection) - 10\log(2n+1)^2 \tag{5.7}$$

This equation fits well with the simulated phase noise of a modulus-7 CILFD shown in Fig. 5.11. The phase noise under free running condition is -97 dBc/Hz at 1MHz frequency offset. Locked by an injection signal generated from a 6-GHz LC VCO with a

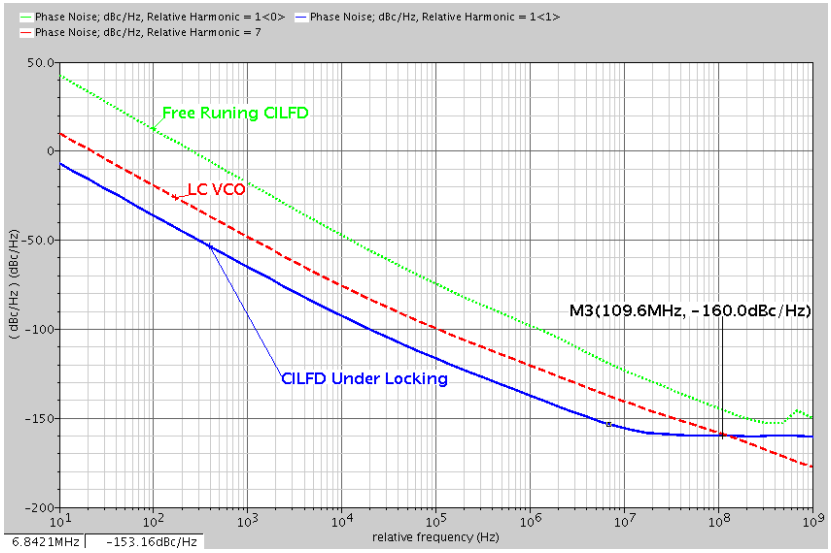


Fig. 5.12 Simulated phase noise (from top to bottom): free running CILFD, injection signal (LC VCO), and locked CILFD.

phase noise of -112 dBc/Hz at 1MHz offset frequency, the modulus-7 CILFD shows a phase noise of -130 dBc/Hz at 1MHz offset.

The more detail phase noise behavior of CILFDs can be expressed as the sum of the phase noise of the free-running CILFD with high pass-filtering characteristic and the phase noise of the injection signal with low-pass filtering characteristic:

$$L_{\phi,\,CILFD}(\Delta\omega) = L_{\phi,\,free}(\Delta\omega)\cdot\frac{\Delta\omega^2}{\Delta\omega^2+\omega_p^2} + L_{\alpha,\,ext}(\Delta\omega)\cdot\frac{(\omega_p/M)^2}{\Delta\omega^2+\omega_p^2} \tag{5.8}$$

where M is the division ratio and ω_p is the pole frequency of the CILFD. The above equation indicates that the noise filtering characteristic significantly depends on the location of ωp. A wider locking range gives rise to a higher ω_p in the injection-locked dividers and a better noise performance because the noise coming from the injection signal is filtered for a larger extent of offset frequencies as depicted by equation (5.8). Therefore, the proposed wideband CILFD can fully take advantage of the high-purity clock generated by the LC VCO and lower the noise floor. Fig. 5.12 shows the phase noise plots of a free-running CILFD, the injection signal generated with the LC VCO, and a CILFD locked by LC VCO injection. The simulated noise floor is at least 12 dB lower than that with the conventional CML dividers used.

5.3 Applications of Complementary Injection-Locked Frequency Dividers

CILFDs can be used in various applications. Because of the nature of frequency division and multiple phase generation, CILFDs can be used in a programmable multi-modulus phase-switching frequency divider as shown in Fig. 5.13. The use of CILFD will lower the power consumption and give better far-out phase noise.

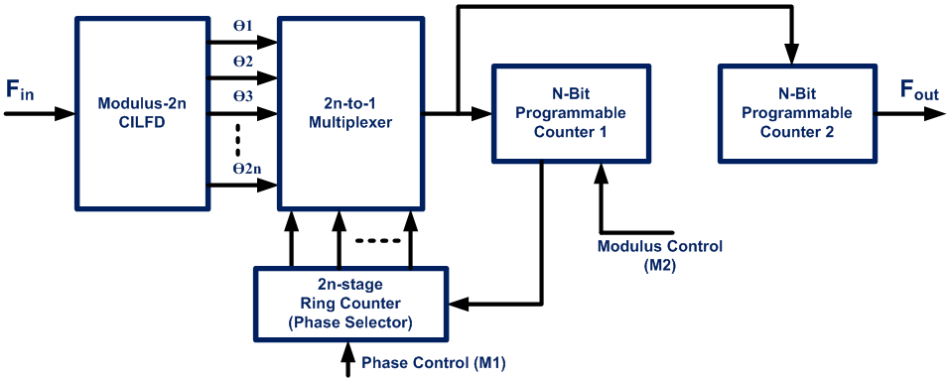


Fig. 5.13 Programmable multi-modulus phase switching divider based on CILFD.

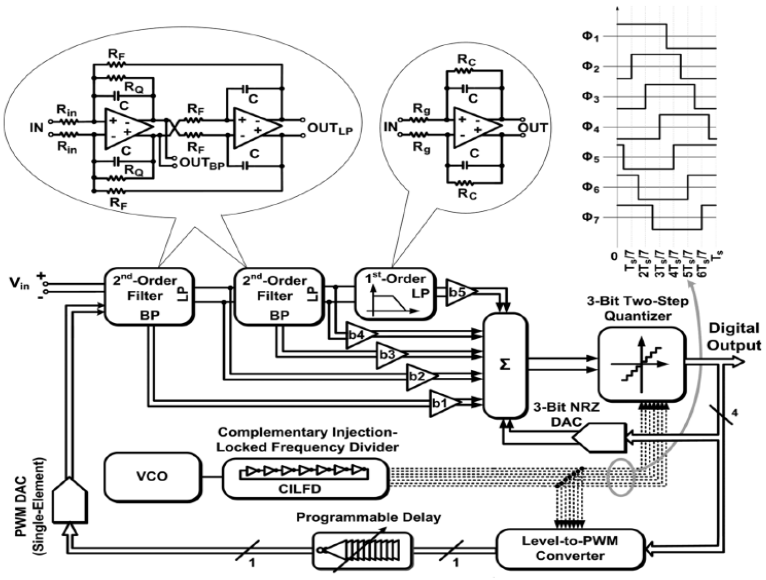


Fig. 5.14 3-bit time-domain quantization based on a divide-by-7 CILFD.

The CILFD can be also used in time-interleave ADC and multiple-phase sampling. Fig. 5.14 shows an example that CILFD used for time-to-digital quantization [58]. Also, as shown in Fig. 5.4 and 5.6, the CILFD can be used as a phase tuning or phase alignment circuits by controlling the DC bias of V_{bp} and V_{bn}.

5.4 Measurement Results

Two differential CILFDs with division moduli of three and seven were implemented in a standard TSMC 0.18-μm technology. Two-stage buffers are used for driving the 50-Ω external loads. Fig. 5.15 shows the microphotogragh of the CILFDs and their buffer stages. The chip area is 1×1 mm^2 including all testing pads; the core of the divide-by-3 and divide-by-7 differential CILFDs occupies 40×120 μm^2 and 90×120 μm^2, respectively.

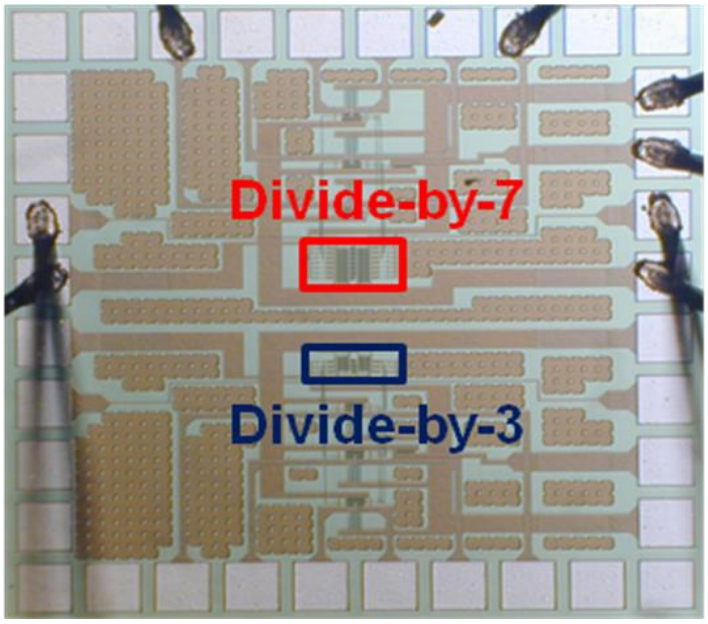


Fig. 5.15 Micorphotograph of the fabricated CILFDs.

The measured average free-running frequency of the divide-by-3 and divide-by-7 CILFDs is 1.15 GHz and 540 MHz, around 10% below the simulated values. The injection signal is generated from a HP 8673C synthesized signal generator. Fig. 5.16 shows the output spectrum of the divide-by-7 CILFD locked by an input frequency of 1.4 GHz. The output frequency of the CILFD is center at 200MHz. When the CILFD is locked, the output signal tone is much sharper and the skirt of the output signal tone in free-running oscillation state is eliminated.

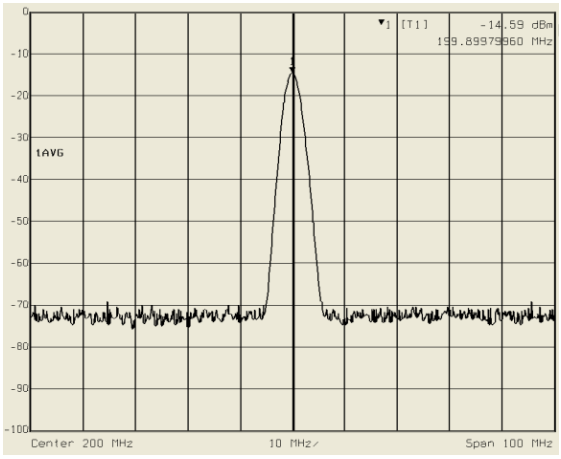


Fig. 5.16. Measured output spectrum of a divide-by-7 CILFD locked by a 1.4 GHz input frequency.

The measured input sensitivity curves of divide-by-3 and divide-by-7 CILFDs are shown in Fig. 9. With an input injection power of -4 dBm, the measured locking range of the divide-by-3 CILFD spans approximately from 1.2 to 4.9 GHz, while the frequency locking range of the divide-by-7 CILFD spans from 1.4 to 4.4 GHz. The measured locking ranges are around 20 % smaller than the ones predicted by schematic simulations. The power consumption of the divide-by-3 and divide-by-7 CILFDs locked by an input

frequency of 4.5 GHz is 0.74 and 0.88 mW, respectively. The performance of the measured CILFDs is summarized in Table 5.2. Table 5.3 presents a comparison of this work with previously published Ring-ILFDs. The proposed CILFD performs excellent power consumption and wide locking range. It resolves the difficulty of generating odd division ratios and exhibits robust functionality over PVT.

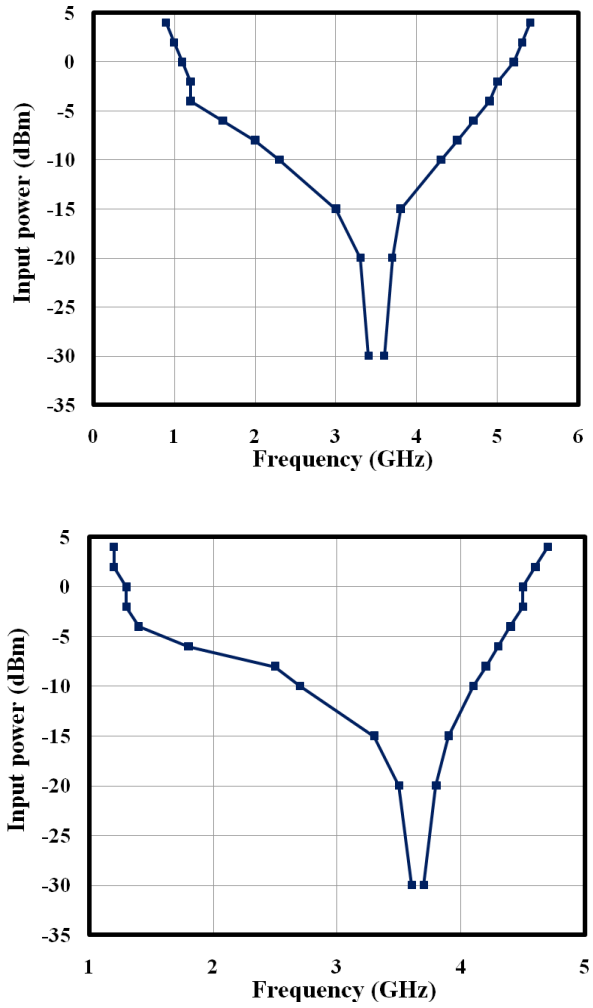


Fig. 5.17. Measured input sensitivity curves of (a) top divide-by-7 and (b) bottom divide-by-3 CILFDs.

Table 5.2 Summary of measured performance

	Divide-by-3	Divide-by-7
Free Running Frequency	1.15 GHz	540 MHz
Locking Range@ -4 dBm Input Power	1.2 ~ 4.9 GHz	1.4 ~ 4.4 GHz
Power Consumption@4.5 GHz Input Frequency	0.74 mW	0.88 mW
Power Consumption@1.5 GHz Input Frequency	0.31 mW	0.36 mW
Core Area	$40 \times 120\ \mu m^2$	$90 \times 120\ \mu m^2$

Table 5.3 Performance comparison of existing works

Ref	Technology	Div. Ratio	Input Power (dBm)	Locking Range (GHz)	Power (mW)
This Work	0.18μm CMOS	3 7	-4	1.2 ~ 4.9 1.4 ~ 4.4	0.74 0.88
[6]	0.18μm CMOS	2 4	0	15 ~ 22 37.4 ~ 38.6	24
[7]	0.13μm CMOS	2 6	NA	0.05 ~ 1.65 0.25 ~ 1.22	0.9 2.7
[8]	0.18μm CMOS	8	3	9.2 ~ 12.3	3.6

Fig. 5.18 shows the chip photos with odd-modulus single-ended and differential CILFDs and even-modulus CILFDs.

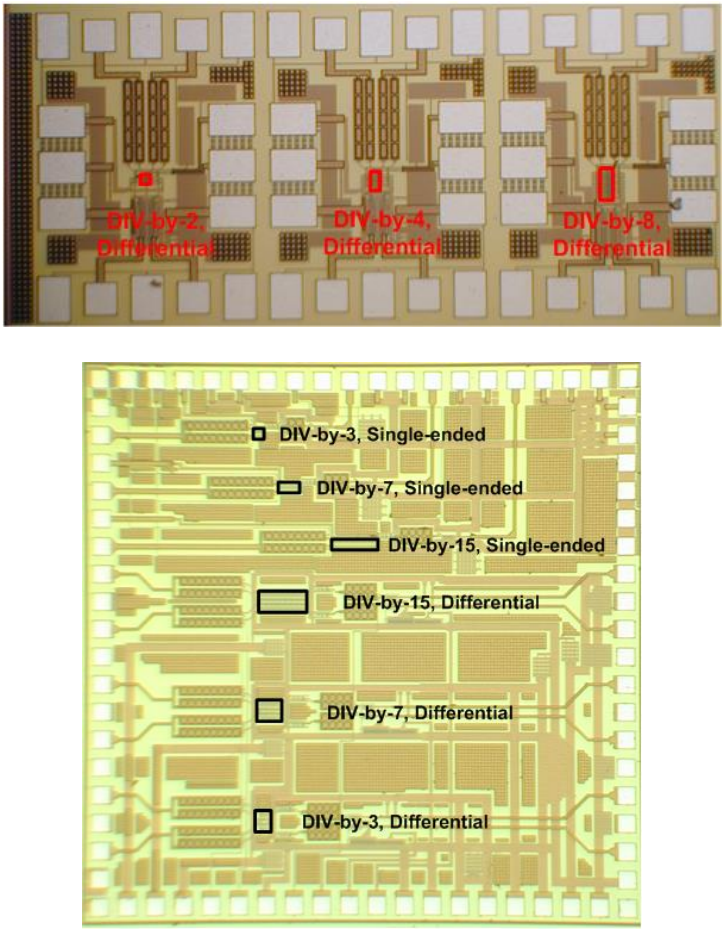


Fig. 5.18 Micorphotograph of the even-modulus and odd-modulus CILFDs.

5.5 Conclusion

This chapter presents low-power ring-oscillator-based complimentary injection-locked frequency dividers (CILFDs) which employ a complimentary delay-tuned injection technique to widen the frequency locking range. The proposed complimentary injection-locked frequency dividers (CILFDs) are composed by a current-starved inverter-based ring oscillator whose delay of each current-starved inverter can be effectively tuned by the injection signal to achieve a wide frequency locking range. The wide locking range characteristic of CILDs inherently excels at the robustness to overcome the PVT variation, a large jitter tracking bandwidth for low jitter filtering, less influence from power supply noise, and a more flexible phase tuning of deskewing. The pseudo-differential structure can be realized using cross-coupled inverters to couple each two opposite phases of the two ring oscillator. The CILFDs can accomplish both odd and even division ratios and generate a multi-phase output. The phase mismatch improved by injection locking The divide-by-2, 3, 4, 5, 7, 8, and 15 CILFDs have demonstrated a locking range from 0.8 to 4 GHz with an input incident power of -5 dBm in a 0.18-μm CMOS technology while the power consumption is less than 1 mW from a 1.8-V power supply.

CHAPTER VI

CONCLUSIONS

This dissertation first discusses the design and implementation of clock generation for a programmable continuous-time bandpass ΣΔ modulator in a software radio receiver system. A continuously 2-16 GHz wideband frequency synthesizer is proposed, using a single-sideband mixer combines feed-forward and regenerative mixing techniques to achieve the wide frequency range. Only one VCO with a reasonable and achievable frequency tuning range is needed to obtain good phase noise. In order to well control the excess loop delay in the wideband system, a phase-tunable clock distribution network and a clock-controlled quantizer are implemented. A replica bias circuitry is used in the phase-tunable cell to maintain appropriate swing. Also, the false locking in the regenerative mixing path is resolved by controlling the self-oscillation frequency of the CML divider. The proposed frequency synthesizer performs 0.6ps rms jitter and consumes lower power compared to the other existing works.

Phase noise and quadrature phase accuracy are the major concerns while using the quadrature voltage-controlled oscillator to generate the quadrature signals. To eliminate these issues, a dynamic current-clipped QVCO is proposed. The sophisticated coupling network reduces injecting noise into LC tank at most vulnerable timings (zero crossing points). Hence, it allows the use of strong coupling ratio to minimize the quadrature phase sensitivity to mismatches without degrading the phase noise performance. The proposed DCC QVCO is implemented in a 130nm CMOS technology. The measured phase noise is

-121 dBc/Hz at 1MHz offset from a 5GHz carrier. The QVCO consumes 4.2mW with a 1-V power supply, resulting in an oustanding FoM of 189 dBc/Hz. In order to achieve excellent phase accuracy, a capacitive source degeneration QVCO is proposed. Removing the conventional cross-coupled transconductor gives inherently large coupling ratio to obtain excellent phase accuracy.

Frequency divider is one of the most power hungry building blocks in a PLL-based frequency synthesizer. The complementary injection-locked frequency divider is proposed to be a low-power solution. With the complimentary injection schemes, the dividers can realize both even and odd division modulus, performing a more than 100% locking range to overcome the PVT variation. The proposed dividers feature excellent phase noise. They can be used for various applications such as multiple-phase generation, programmable phase-switching frequency dividers, and phase-skewing circuits.

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