# HIGH-ISOLATION LOW-POWER ACTIVE QUASI-CIRCULATOR FOR 44GHZ TRANSCEIVER WITH POWER AND NOISE OPTIMIZATION IN 0.18 MICROMETER BICMOS

A Thesis

by

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# ABSTRACT

Circulator is an important directional component in RF, microwave and millimeter wave communication front ends for certain communications, which requires transmitting and receiving signal simultaneously in the same band without switching of antenna from transmitter to receiver. As modern trend of wireless communication, conventional ferrite circulator is huge, bulky and heavy to be integrated with analog and digital baseband processing circuits. Active circulators provide a compact high isolation solution for low power application with smaller size and less cost with compatibility with modern IC. Previous works are majorly working at low frequency and paid little attention to power and noise requirement of active quasi-circulator working at the front end of a transceiver. A BiCMOS active quasi-circulator at 44GHz is designed in 0.18 μm process to provide high isolation low cost solution, which is comprised of in-phase divider and out-of-phase active combiner, with noise and power optimization. Moreover, techniques employed to improve isolation such as high Common mode rejection ratio(CMRR) balun design, common mode feedback, and novel method of power splitting and noise optimization, impedance matching scheme are discussed.

High isolation of cascode structure is analyzed and major tradeoffs among characteristics are investigated, such as: gain and transmission-reception isolation; output impedance, matching and noise; linearity, power and efficiency. The circulator operates around 44 GHz with 3dB bandwidth of 4.53GHz, achieves maximum

2.897dBm input and 2.32dBm output power. Noise Figure (NF) is 10.62dB for reception path, only 0.03dB higher than $NF_{min}$.

Linearity is reasonable for both in-phase divider and out-of-phase active combiner. OIP3 of in-phase divider is 8.15dBm, IIP3 is 4.48dBm, $P_{1dB,in}$ is -5.97dBm. OIP3 of out-of-phase active combiner is 5.18 dBm, IIP3 is 3.85dBm, $P_{1dB,\ in}$ is -2.79dBm.

All the isolations better than -37 dB are achieved and forward gains better than 4 dB are achieved with power consumption 56.83mW. Large signal TX-RX isolation is 51.837dB. The circuit takes merely 1.415mm*1.014mm area. This active quasi-circulator offers a low cost substitute solution for circulator in low power applications.

# DEDICATION

To all the pure, the bright, the beautiful, the invaluable.

To faith, family, friends.

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Finally, thanks to my mother and alumni for their support.

# NOMENCLATURE

| | |
|---|---|
| Balun | Balance unbalance |
| BiCMOS | Bipolar and Complementary metal–oxide–semiconductor |
| BJT | Bipolar junction transistor |
| CMRR | Common mode rejection ratio |
| IIP3 | Input third order interception point |
| LNA | Low noise amplifier |
| NF | Noise figure |
| OIP3 | Output third order interception point |
| PA | Power amplifier |
| PAE | Power added efficiency |
| PE | Power efficiency |
| PVT | Process Voltage Temperature |
| RF | Radio Frequency |
| RX | Receiver |
| TX | Transmitter |

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CHAPTER I

INTRODUCTION

## 1.1 Background

A circulator is generally a three-port microwave device with ports arranged in a circular sequence such that signal entering one port circulates in only clockwise or counter clockwise direction to next adjacent port, but not to the non-adjacent ports if all ports are matched. Thus all non-adjacent ports are isolated from each other.

As shown in Figure 1. When a signal enters port 1, it will be delivered to port 2 but not to port 3, port 3 is isolated from port 1. When a signal enters port 2, it will be delivered to port 3 but not to port 1, port 1 is isolated from port 2 reversely. The arrows show the direction of signal flow, it is a counter clockwise circulator in this case.

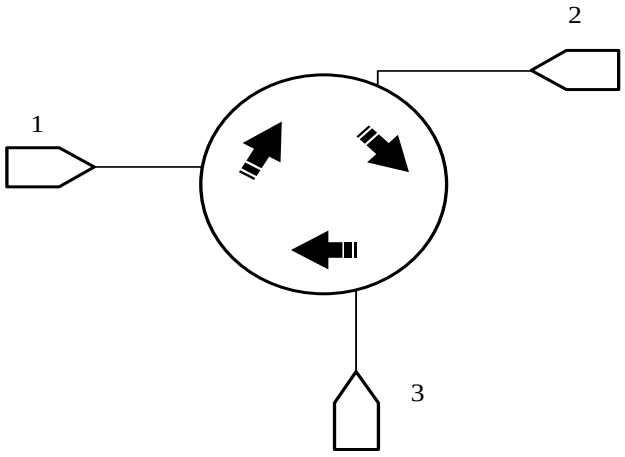


**Figure 1.** Circulator diagram.

Circulator for general applications has three ports. An ideal three-ports-circulator thus has scattering matrix of the following form:

$$\boldsymbol{S}=\begin{pmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix}, \tag{1.1}$$

The key parameters of a circulator are:

Insertion loss

Reverse isolation

Bandwidth and center frequency

Power handling

Noise Figure (for the receiving path)

Linearity

Size, weight and cost

The main property of circulator is its non-reciprocal characteristic, which can be used to separate incident and reflected waves. Among different characteristics, isolation is the most critical one to alleviate blocking caused by transmission path to the reception path.

### 1.2 Conventional passive circulator

Conventional passive circulator is made of ferrite material based on non-reciprocal characteristic of gyromagnetic, which is bulky and heavy, not compatible with monolithic integration, renders it an expensive solution for a modern transceiver system.

The first ferrite circulator was the Faraday rotation phase shifter as shown in Figure 2.

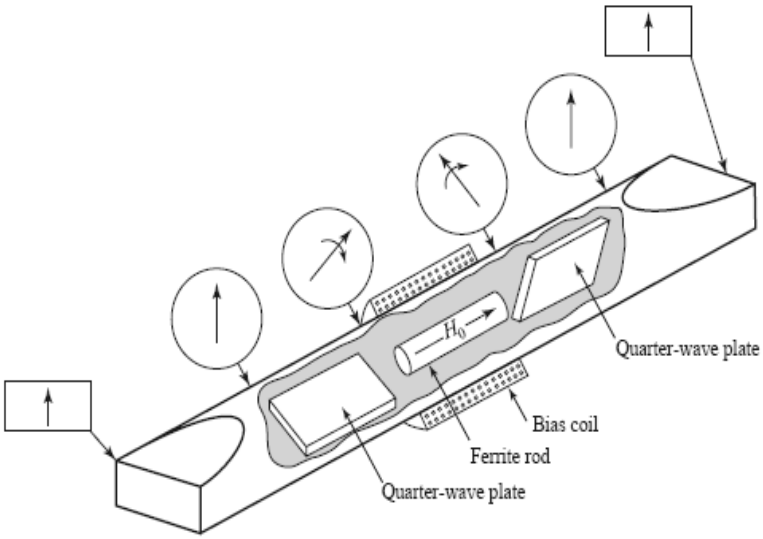


**Figure 2.** Nonreciprocal Faraday rotation phase shifter [1].[1]

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Modern junction circulator is more compactly designed, as shown in Figure 3, but still too large to be integrated [1].

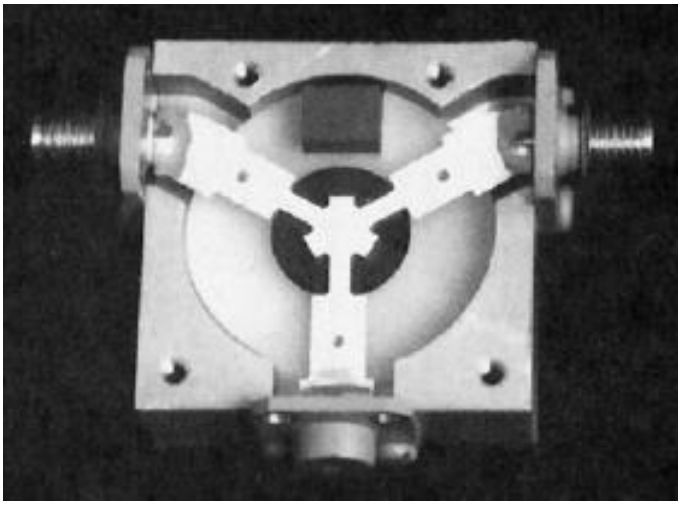

**Figure 3.** Disassembled ferrite junction circulator [1].[2]

An application of this type of circulator is in UHF RFID system [2] as shown in Figure 4.

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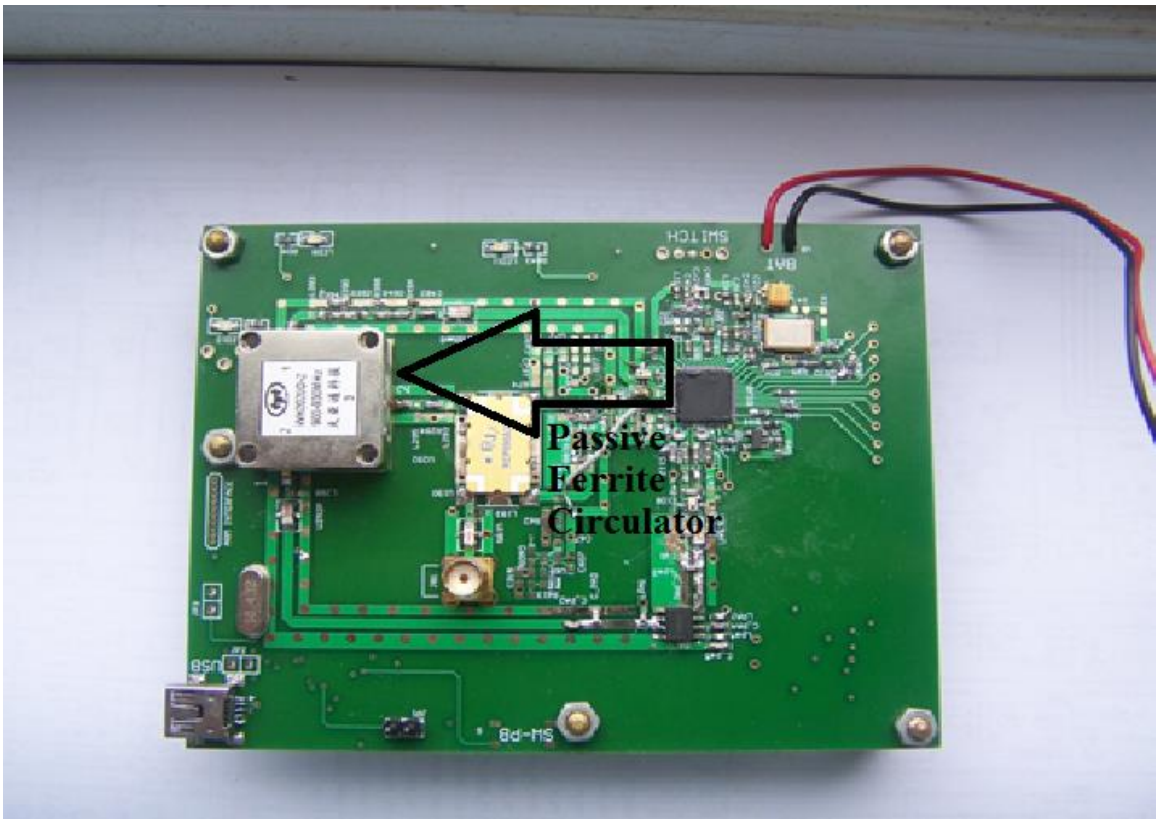


**Figure 4.** A demo application of circulator in UHF RFID reader.

### 1.3 Active circulator

Several active circulators were developed to overcome the disadvantage of passive circulators, as inherent solution with small size, light weight and low cost, compatible with modern IC fabrication.

S. Tanaka, N.Shimomura and K.Ohtake proved the possibility of realization of active circulators with transistors by taking advantage of the “unilateral” characteristic of transistors, and derived the conditions for signal circulating and impedance patching at

low frequency[3], as shown in Figure 5. A frequency extended GaAs modification of this circuit is proposed in [4].

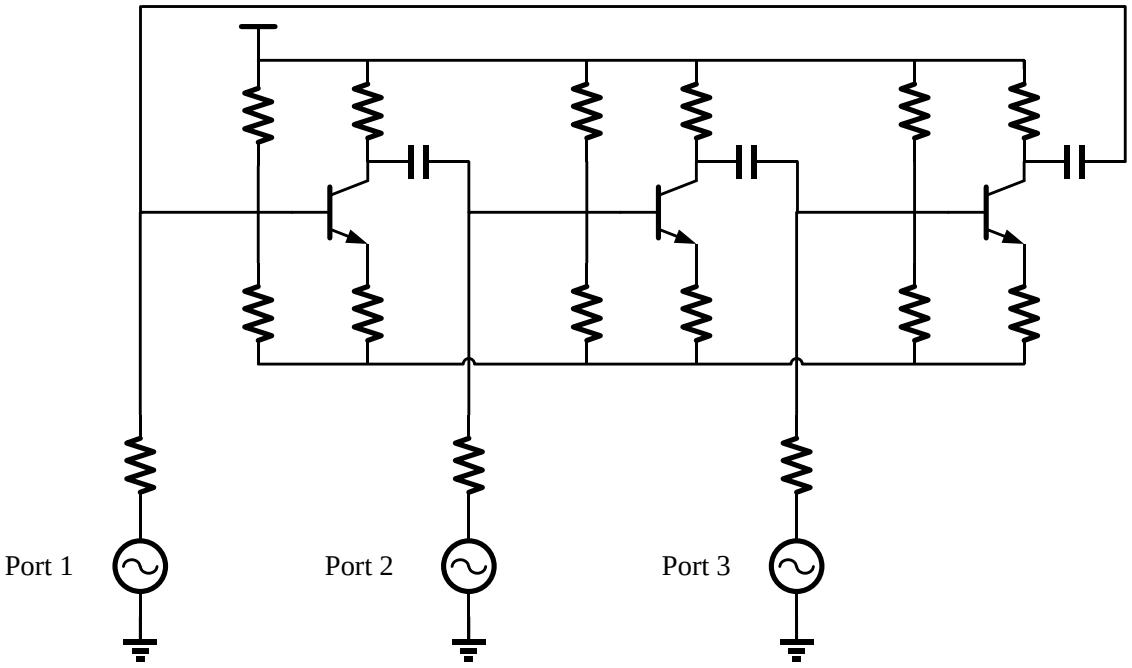


**Figure 5.** Circuit diagram of an active circulator proposed in [3].

### 1.4 Active quasi-circulator

As shown in Figure 6, a quasi-circulator is a simplified circulator in which there is no power transfer from port 3 to port 1.

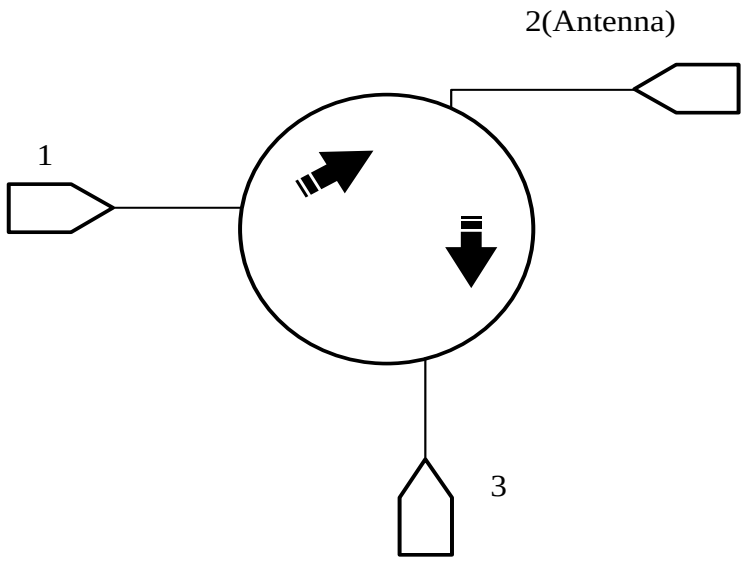


**Figure 6.** Quasi-circulator for transceiver front ends.

The S parameter of an ideal quasi-circulator thus would be:

$$\boldsymbol{S}=\begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix}, \tag{1.2}$$

Three quasi-circulators can form a complete circulator circuit in a ring configuration at the expense of larger chip area.

For transceiver applications, only two signal paths are needed. Also, power handling and noise are extra concerns for signal circulating for active circulator.

Active circulator have the capability of providing gain, in addition to compatibility with modern process integration, active quasi-circulator is a good

substitute for passive circulator in low power low cost transceiver applications. One of the simplest designs of active quasi-circulator is shown in Figure 7.

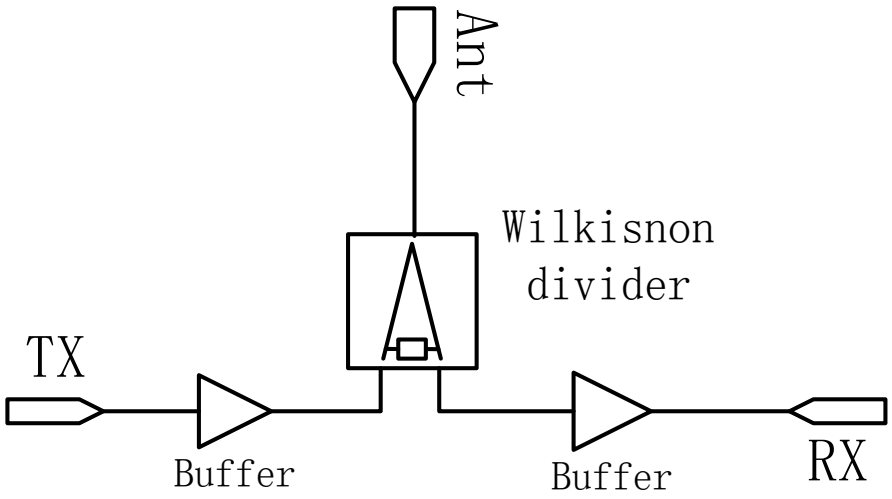


**Figure 7.** Simple active quasi-circulator design with Wilkinson divider [5].

An active quasi-circulator architecture based on out-of-phase divider and in-phase combiner is developed by Shinji Hara[6], with tradeoff between receiving gain, NF and impedance matching at the antenna port connection node. Ahmed Gasmi developed a circuitry, which receives signal by one common gate transistor, while common gate structure is not good for low noise application [7], and Antenna impedance

matching is a problem because the way how antenna port is connected cannot guarantee matching for both transmission and reception signal. Modified version of [7] with better power and noise performance are presented in [8][9]. Still, these designs are difficult to guarantee layout parasitic symmetry of two signal paths due to inherent asymmetric structure nature. R.Bahri gave detailed analysis based on matrix model [10], but less insight into circuit design techniques. Chia-hao Chang developed a 30GHz current reuse active quasi-circulator [11], which was a current reuse version of [12], both paid little attention to matching and noise performance, and offered no gain. Two other design at 24 GHz and below 6 GHz providing no gain were proposed by Ding-lie Huang[13][14]. Geert Carchon analyzed power and noise limitation of different schemes of active circulators[15]. Y. Zheng developed a lumped design in [16] without consideration of noise either from the power splitting or amplifier noise figure, and much of the isolation relies actually on the isolation of slow wave direction couplers. A scheme based on in-phase divider, in-phase combiner and phase shifter is proposed in [5], still paid no attention to antenna port matching. Two schemes based on distributed amplifiers are introduced in [17][18] focusing on wide band while ignored noise issue. An OTA based design working only at low frequency is proposed in [19]. Siu K. Cheung proposed a novel way of using direction coupler combining transmission signal, but taking too much area[20][21]. Hsien-shun Wu employed digital feed forward cancellation achieved very high large signal isolation but noise figure and power consumption were also high[22]. A hybrid design based on passive directional device offering average performance was proposed by Mirko Palomba[23]. Most of the previous work only

cared small signal TX-RX isolation, but for transceiver front end, large signal isolation should be the concern.

Active circulator can be achieved by connecting three active quasi-circulators in a loop as shown in Figure 8 [6]. Active circulator designed in [24] can be viewed as a loop of the active quasi-circulator in [16].

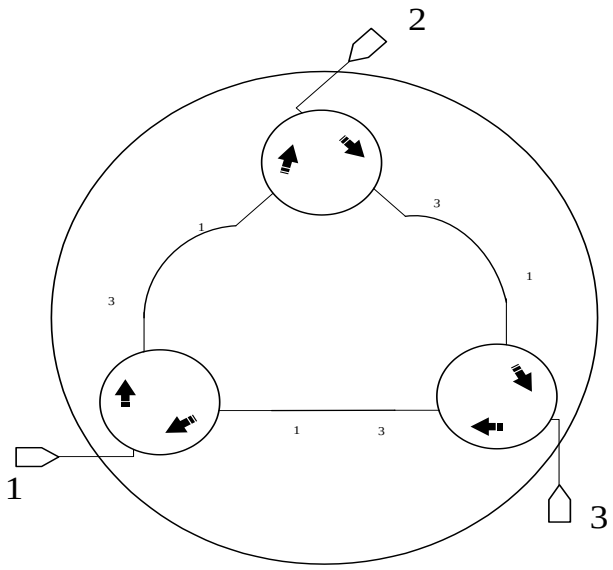


**Figure 8.** Three quasi-circulator forming a circulator.

### 1.5 Application of active circulator

Active circulator and active quasi-circulator, which are compatible with modern MMIC and RFIC technology, have applications as a part of the whole microwave

transceiver front ends. Circulator can be used as isolator for sensitive device such as oscillators if one port is terminated with a matched load.

As shown in Figure 9, circulator can be used as: (a) an isolator; (b) a duplexer; (c) a phase shifter; (d) an amplifier circuit in reflection amplifiers [25]. If an electromagnet is used for the biasing of the ferrite circulator, it can operate in a single-pole double-throw switch. A circulator can also be used as an isolator by terminating one of the ports with a matched load.

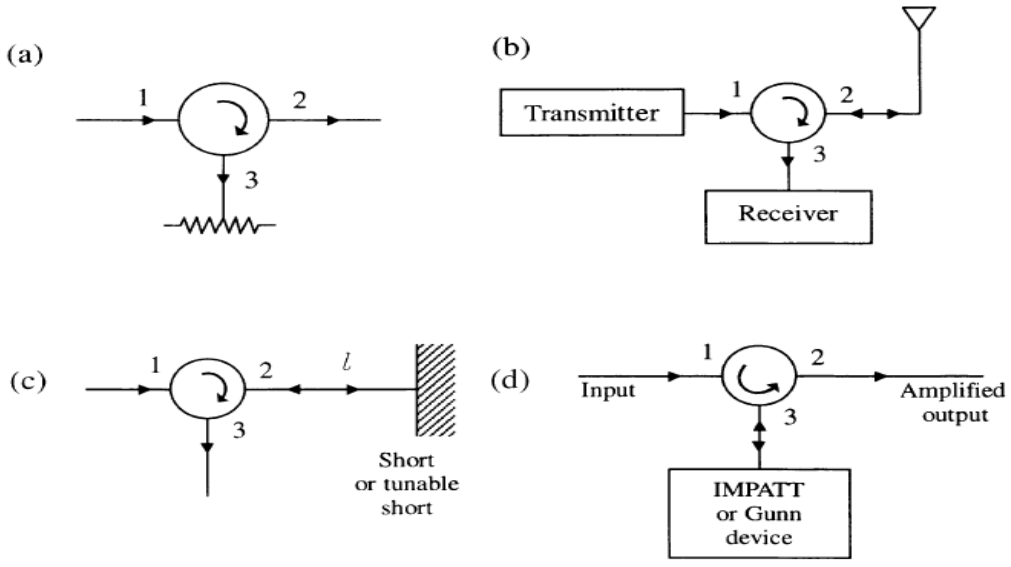


**Figure 9.** Typical applications of circulators [25].[3]

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The capability of circulating signal allows circulator to be used as a duplexer. A duplexer is a device that separates transmission signal and reception signal sharing an antenna to either a transmitter or a receiver so that the same antenna can be used for both transmission and reception. An application of using circulator as duplexer is shown as Figure 9(b).

Several duplexers can be cascaded to build a multiplexer. A multiplexer is a device composed of interconnected filters which can combine many different narrow band channels into one wide channel. The inverse process is de-multiplexing, which split one wideband channel into many narrow band channels.

The simultaneous transmission and reception differentiate circulator from solutions based on switches.

Circulator can also be used in the construction of narrow-band phase shifter with a connection example shown in Figure 9(c). This type of phase shifter simply changes the phase of reflective wave via mechanical or electrical tuning of short location. Large amount of phase shifter is used in phased array to shape particular beam according to algorithm.

## 1.6 Scope of research

For transceiver front end, the purpose of circulator is to separate transmission and reception signal, thus, an active quasi-circulator is enough in a transceiver.

Previous works on the design of active quasi-circulator were majorly small signal designs, most of the structures are only applicable at low frequency, and paid little attention to the impedance matching. Also, power and noise performance with respect to

transmission and reception signal and the isolation of transmission and reception are in a small signal sense[11][12][19].

The research is conducted first to study topics such as microwave frequency on-chip PA, LNA, balun and active circulator design and analysis, then clarify advantage and disadvantage of active circulator in contrast to conventional circulator. Second, Investigate circuit methodology of realizing active quasi-circulator, and identify tradeoffs limiting the key front end performance. Third, propose a design of BiCMOS active quasi-circulator at 44GHz in 0.18 μm process to provide high isolation between transmission and reception signals at such high frequency with small area, which is comprised of Class AB in-phase output stage and low noise input stage, with high CMRR balun design to fulfill differential to single ended conversion.

### 1.7 Outline of thesis

Chapter 2 discusses the top level design of the active quasi-circulator scheme proposed and analyses the interconnection with Antenna port, and calculates reverse isolation of cascode structure. Chapter 3 describes the design of in-phase power divider and technique used to lower the noise contribution of it. Chapter 4 describes the design of low noise out-of-phase active combiner including high CMRR balun. Chapter 5 describes the entire design, gives post layout simulation results. Chapter 6 concludes and discusses potential work in future.

CHAPTER II

TOP LEVEL DESIGN

## 2.1 Introduction

The circulator is basically comprised of Class AB active in-phase power divider and low noise out-of phase combiner, as shown in Figure 10.

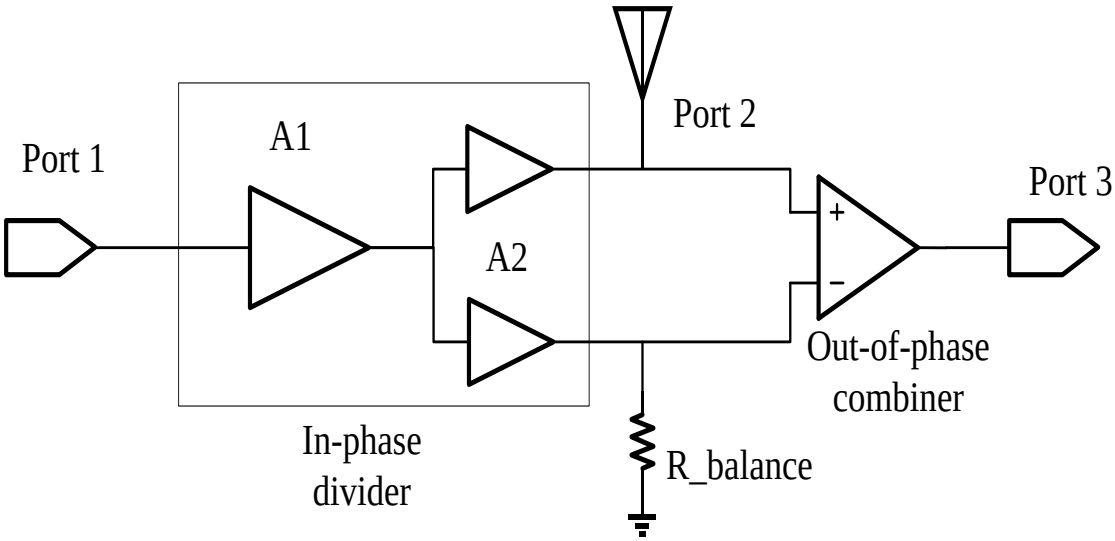


**Figure 10.** Basic scheme of Active quasi-circulator proposed.

### 2.2 Impedance matching at antenna port node and $R_{\_balance}$ node

The impedances at the three way nodes of the active quasi-circulator, which are the antenna node and balance port node, are critical nodes for impedance matching. The relationship among these resistors: output impedance of in-phase divider $R_{tx}$, antenna impedance $R_a$ and input impedance of out-of-phase active combiner $R_{rx}$, can be represented as shown in Figure 11.

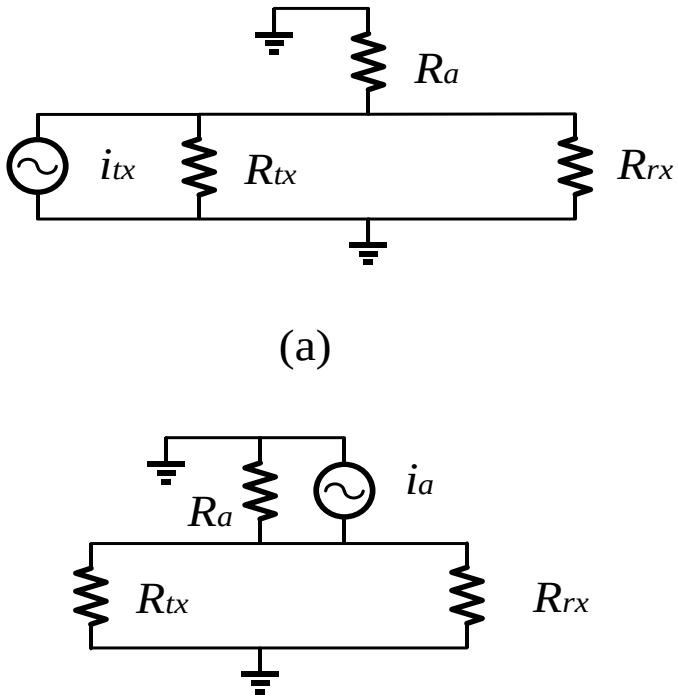


**Figure 11.** Models of relationship among impedances.

$R_{rx}$ has different value to transmission signal and reception signal. For differential mode signal, which is reception signal, $R_{rx}$ is designed to be the matched impedance value as the same way of an LNA design. For common mode signal, which is the transmission signal, it sees a higher value $R_{rx}$ due to larger emitter degeneration inductor which only shows up to common mode signal. This will be discussed in detail in chapter 4.

For reception signal, ideally, the output impedance of the in-phase divider should be as large as possible, which is represented by $R_{tx}$ in Figure 11, the input impedance seen by the antenna, whose signal is differential to the out-of-phase active combiner, is dominant by the input impedance of the out-of-phase active combiner $R_{rx}$. In other words, the output impedance of the antenna port, which is port 2 in the symbol view above in Figure 9(b) , is virtually the differential mode input impedance of out-of–phase combiner, therefore, even though this node is a three way node, impedance is matched for reception.

Practically, the output impedance of the cascode structure is finite, though high at low frequency, but rather low in microwave frequency due to negligible parasitic capacitance, in combination of finite Q of loading inductors, the output impedance of the in-phase divider hardly goes beyond several hundred Ohms.

In order to approximate the design concept discussed above closer, the differential mode input impedance of the out-of-phase active combiner is chosen to be 40 Ohms rather than 50 Ohms as antenna is, so there is an impedance transforming network from 50Ohm antenna port to the Port 2 of active quasi-circulator.

There are 4 reasons for 40 Ohm.

1. The smaller the input impedance of the out-of-phase active combiner, the better the approximation of above design concept in a relative sense. However, to satisfy impedance matching, the antenna impedance is also transformed to a smaller value, the output power of in-phase divider is lowered too, so 40 Ohm is chosen to balance this tradeoff.

2. Output swing limitation due to low supply voltage of cascode Class AB active in-phase power divider, the loading resistance should be in a range which keeps the transistors in linear range.

3. Noise consideration of low noise out-of-phase active combiner favors small input impedance. Smaller input impedance requires smaller emitter degeneration inductor, which results in less noise contributed by non-ideal inductor and less gain degeneration. This would be further illustrated in chapter 4.

4. Q of impedance matching network from antenna to the three way connecting node reduces the bandwidth. The larger difference the impedance is transformed, the larger Q, and hence less bandwidth of the impedance transforming network. From 50 Ohm transforming to 40 Ohm the Q of the matching network would be the square root of 50/40=1.118, negligible effect on the bandwidth of the active quasi-circulator, while still provides extra filtering to nonlinear harmonics.

### 2.3 Principle of isolation of cascode structure

Not only does cascode structure attenuate Miller effect of the input transistor and provide higher output resistance, but also provides higher reverse isolation. As depicted

in Figure 12, a test voltage is applied to the output or the collector of $Q_2$, and voltage delivered to the source impedance $R_s$ is calculated.

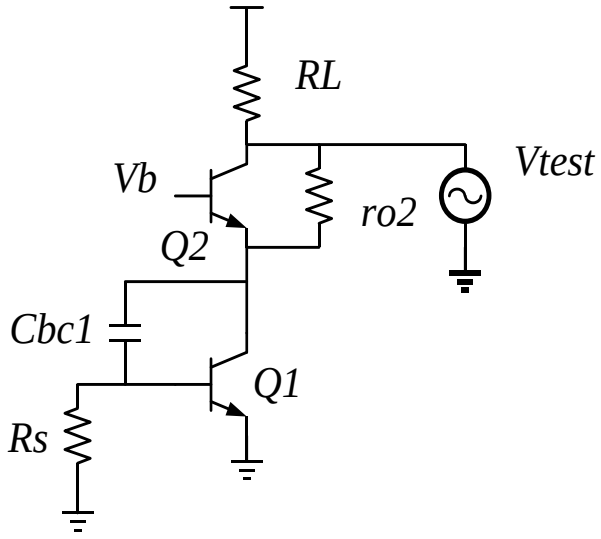


**Figure 12.** Reverse isolation in cascode structure.

Consider only $r_{o2}$ and $C_{bc1}$ as the leakage path, assume $gm_2 >> 1/r_{o2}$, $gm_2 >> 1/r_{\pi 1}$, which are true when the transistor is biased at amplifying region, after solving KCL and KVL of small signal model, yields:

$$\frac{V_{Rs}}{V_{test}} \approx \frac{C_{bc1}s}{(gm_1R_s + gm_2R_s + 1)C_{bc1}s + gm_2} \cdot \frac{R_s}{r_{o2}}, \tag{2.1}$$

This value is the “reverse isolation” of cacode structure. In typical design, $C_{bc1}$ is very small, the denominator is approximately equal to $gm_2$, thus,

$$\frac{V_{Rs}}{V_{test}} \approx \frac{C_{bc1}\omega}{gm_2} \cdot \frac{R_s}{r_{o2}}, \tag{2.2}$$

Therefore, reverse isolation can be improved by increasing the intrinsic gain of transistor $Q_2$, and lowering the size of layout potentially contributes to $C_{bc1}$. Equation (2.2) also explains why isolation is worse at high frequency.

### 2.4 Isolation from transmission to reception

The signal path of transmission signal to the receiver can be shown in Figure 13:

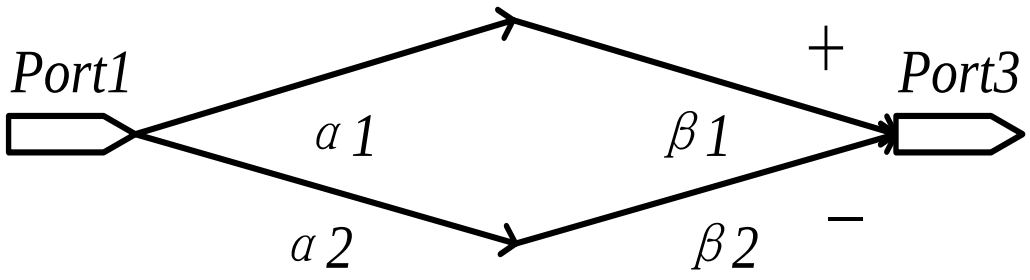


**Figure 13.** Signal flow chart.

$$\text{Isolation} = -20\log|\alpha_1\beta_1 - \alpha_2\beta_2|, \tag{2.3}$$

$\propto_1$, $\propto_2$ are the voltage gain of in-phase divider, and $\beta_1$, $\beta_2$ are gain of out-of phase combiner to each signal path. Taking random and deterministic asymmetry caused by mismatch into consideration,

$$\alpha_2=\alpha_1+\Delta\alpha, \tag{2.4}$$

$$\beta_2= \beta_1+\Delta\beta, \tag{2.5}$$

Then:

$$\begin{aligned}\text{Isolation}&=-20\log|\alpha_1\beta_1-\alpha_2\beta_2|\\ &= -20\log|\alpha_1\beta_1-(\alpha_1+\Delta\alpha)(\beta_1+\Delta\beta)|\\ &= -20\log|-\alpha_1\Delta\beta-\Delta\alpha\beta_1-\Delta\alpha\Delta\beta|,\end{aligned} \tag{2.6}$$

Thus, the isolation of transmission to reception trades with in-phase divider gain and out-of-phase active combiner gain. $\Delta\alpha$ may come out from impedance mismatch and random mismatch from layout. $\Delta\beta$ may come out from finite balun CMRR and layout mismatch. To improve transmission to reception isolation, low gain and symmetric design need to be employed, or make $\Delta\alpha$ have different sign of $\Delta\beta$ and tune $-\alpha_1\Delta\beta-\Delta\alpha\beta_1=0$; assumes $\Delta\alpha\Delta\beta$ is negligible. In other words, $S_{21}$, $S_{32}$ trade with $S_{31}$.

# CHAPTER III

# CLASS AB ACTIVE IN-PHASE POWER DIVIDER

## 3.1 Introduction

Class AB active in-phase power divider is a modification of Class AB power amplifier with consideration of impedance matching and noise between antenna and the low noise out-of-phase active combiner. Key characteristics of in-phase divider are:

Output impedance

Reverse isolation

Linearity

Efficiency

Power gain

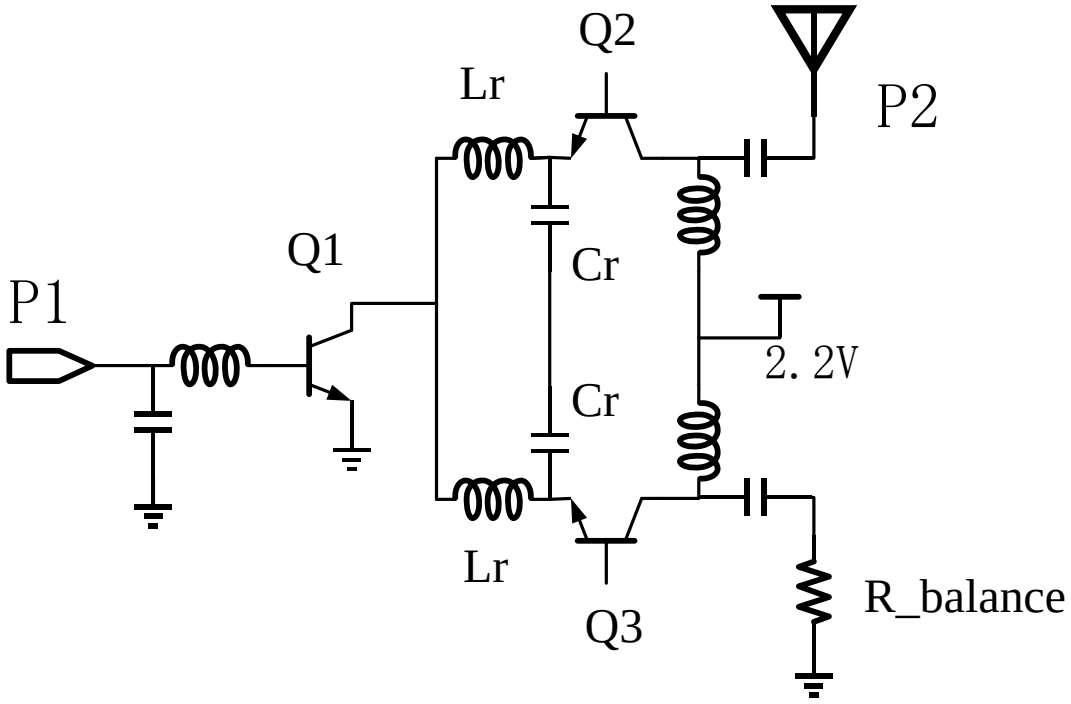


**Figure 14.** Class AB active in-phase power divider.

As shown in Figure 14, transmission signal gets amplified by transistor Q1 and splits into two parallel cascode transistors Q2 and Q3, and be delivered equally to antenna and balance port R_balance. By splitting power this way, potential impedance matching problem of passive splitting network can be avoided.

### 3.2 Output impedance

The inductors Lr between the input common emitter amplifier Q1 and cascodes Q2, Q3 are for high output impedance at high frequency and low noise purpose, and to compensate the gain drop cause by parasitic capacitance to ground at the emitter of Q2,

Q3 and collector of Q1.However, the higher the Lr the higher the loss due to finite Q of the inductor.

High output impedance of this in-phase divider is necessary to allow final output impedance of the circulator to the antenna is dominant by the input impedance of low noise out-of-phase active combiner, thus improves the impedance matching at this three branch node.

*R_balance* has the same impedance as the antenna in order to keep the two paths of transmitting signal symmetric. Two rather than one resonating capacitors $C_r$ are there for the same purpose of symmetric signal path if parasitic capacitance of them are taken into consideration.

### 3.3 Noise

The noise concerns of Class AB active in-phase power divider are two folds.

First, the higher the output impedance of the Class AB active in-phase power divider, the less waste of antenna signal on the transmitting side of active quasi-circulator. Therefore the signal from antenna or port 2 of the circulator goes to out-of-phase divider mostly, thus SNR degrades very less.

The other fold of noise concern is that the output noise of active in-phase power divider needs to be relevant at each input of the out-of-phase active combiner for noise cancellation. In order to make the noise going into the out-of-phase active combiner relevant, the output noise of in-phase divider has to be dominant by the noise of input transistor Q1; then, ideally the output noise of active in-phase power divider can be cancelled at out-of-phase active combiner. However, the noise of two cascode transistors

are irrelevant to each other, and the emitter degeneration of one cascade transistor, say Q2, is 1/gm3, which is majorly the small input impedance of the other common base cascode transistor , Q3, if Cr is not introduced.

The capacitors $C_r$ are thus introduced in the middle of the active in-phase power divider and resonating with inductors to enhance resistance of emitter degeneration to lower the output noise of cascode transistors. In other words, the noise of cascode transistors Q2 and Q3 are greatly attenuated due to high emitter degeneration resistance which comes out of resonance of tank formed by $L_r$, $C_r$. Therefore, the dominant noise comes from the common emitter input stage, which is relevant to the receiver front end, low noise out-of phase combiner, in this case.

Large inductor $L_r$ brought low NF to the receiver because the emitter degeneration is better for cascodes. However, too large $L_r$ would cause greater loss of signal comes out of Q1 due to finite Q of inductor, and the voltage at collector of Q1 will exceed the breakdown voltage [26]. Thus the inductor and break down voltage of $V_{ce}$ limit the maxim current of the in-phase divider. Therefore, there is tradeoff between output power, NF of out-of-phase divider, and reverse isolation.

### 3.4 Power and efficiency

Since the transmitter front end needs to deal with large output power, so the power handling capability and efficiency are important to active quasi-circulator.

Output stages are grouped into classes depending on conduction angle of their collector or drain current waveforms. The conduction angle is defined as the percentage of the signal period during which the transistor remains on multiplied by 360 ° [27]. The

efficiency gets better as the conduction angle get smaller from 360 °to 0 °, as shown in Figure 15. Besides, the achievable fundamental output power is nearly the same for a class A, class AB, or class B stages and would drop as the conducting angle goes smaller than 180 °[28].

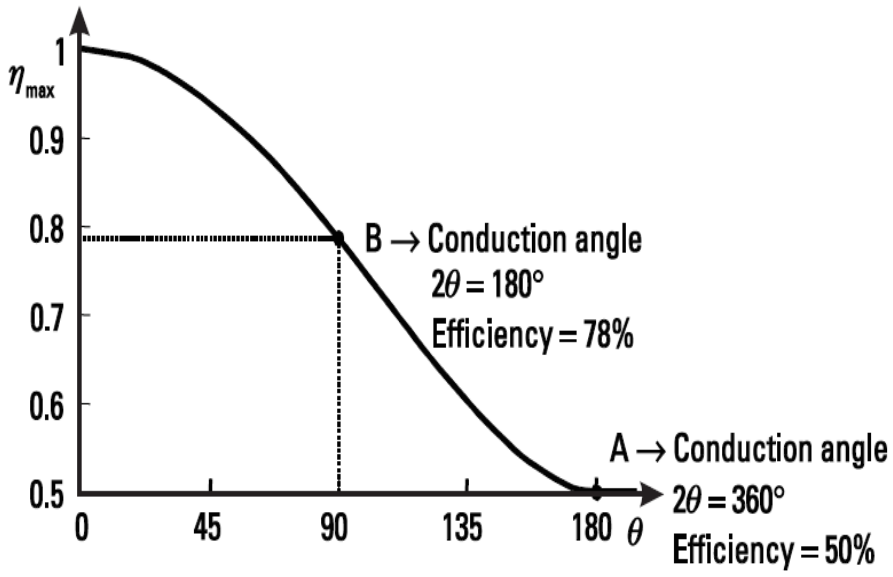


**Figure 15.** Maximum efficiency versus conduction angle [28].
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The in-phase divider is designed to work in class AB condition. Class AB is generally used to refer to common emitter stage whose conduction angle is between 180 ° and 360 °. In other words, the common emitter transistor turns off for less than half of a period. A class AB stage is less linear than a class A stage but more linear than a class B stage. Also, class AB output stage is a good balance between power and efficiency.

Furthermore, the conducting angle is chosen to be 240 °, since theoretically the output power of the fundamental is largest at this sweet point, which gives 1.15 times larger power than that of Class A output, as shown in Figure 16.

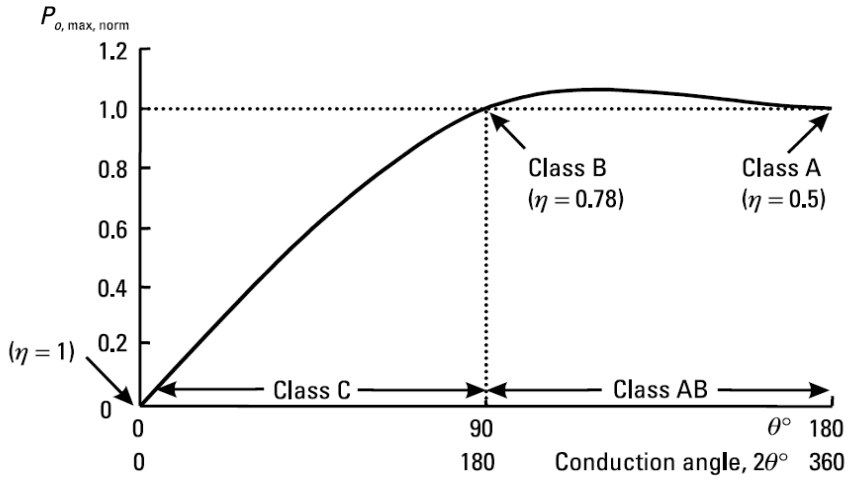


**Figure 16.** Maximum output power versus conduction angle [28].
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# CHAPTER IV

# LOW NOISE OUT-OF-PHASE ACTIVE COMBINER

## 4.1 Introduction

The low noise front end shown in Figure 17 is an out-of-phase active combiner which can be viewed as a differential input LNA with balun that performs differential to single ended output.

The key characteristics of low noise front end are:

Noise Figure

Gain

Linearity

Impedance Matching

CMRR

Reverse Isolation

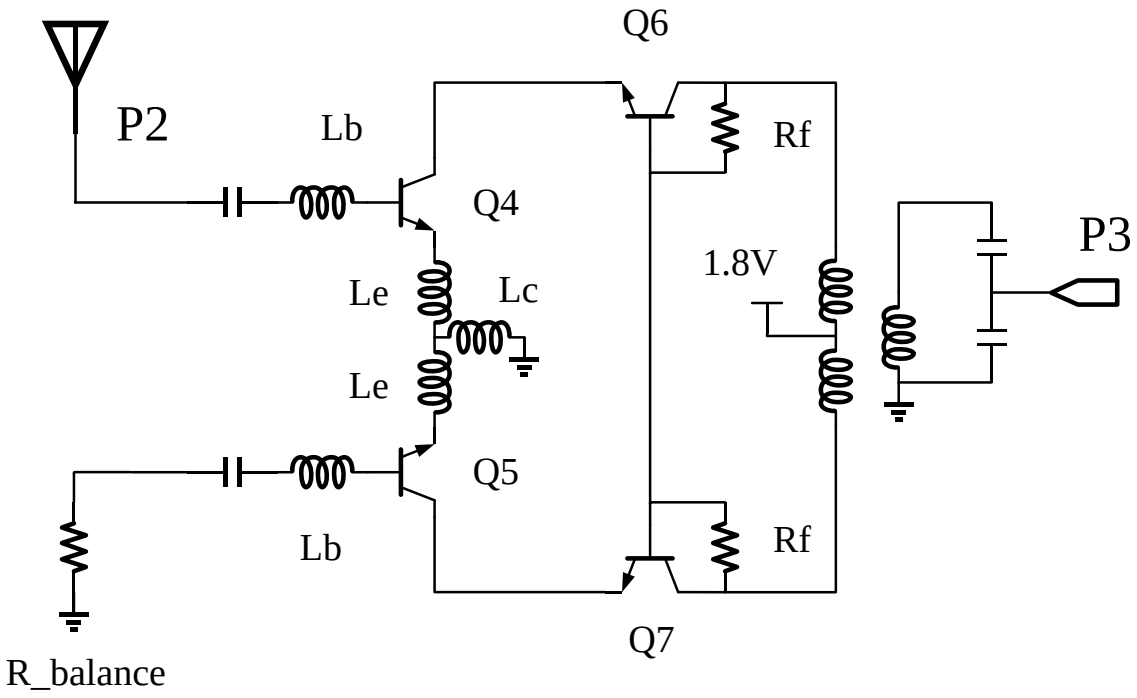


**Figure 17.** Low noise out-of-phase divider.

For receiving signal, it functions like a differential LNA, with only Le to be the emitter degeneration inductor for matching purpose. For transmitting signal from the in-phase divider, it functions as one highly emitter degenerated amplifier, with half $L_e$ in series with $L_c$ as the degeneration inductor. $L_c$ is 280 pH and Le is 44 pH in this design. Therefore the common mode gain is lower than differential mode gain, and also input impedance of common mode is larger than that of differential mode.

Another common mode feedback is introduced to the cascode transistors, as shown in Figure 17, to further attenuate the residual common mode signal from the output of differential pair, since normally transmitting signal is very large. Ideally no signal is delivered to the load since balun does not deliver common mode signal. Not only does common mode feedback at cascade transistors further attenuates the common mode signal from transmitter, it also enhances reverse isolation from port 3 to port 2.

### 4.2 Low noise out-of-phase active combiner design

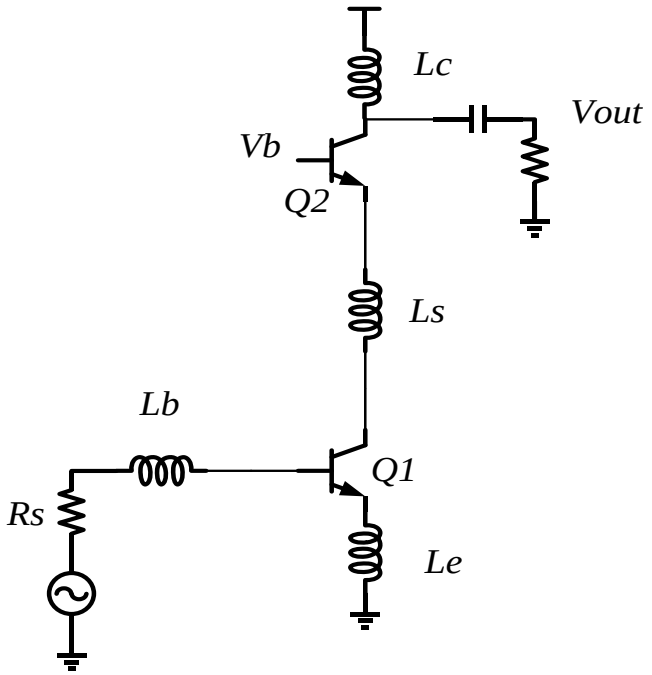


**Figure 18.** Schematic of classic inductor degenerated common emitter LNA.

Since the in-phase divider functions as a differential LNA, it can be simplified to the half circuit as show in Figure 18, assuming the output impedance of the in-phase divider is large enough to be ignored. Therefore, minimum noise figure design is still the same as LNA design. The only difference is extra noise coming out of active in-phase power divider would raise the minimum of NF.

As the Low noise out-of-phase active combiner is the first stage in the receiver chain, the input must be matched to 50 Ohms [28]. The most popular method requires two inductors $L_b$ and $L_e$ to provide the power and noise match at the same time [27][29], as shown in Figure 18. While for this active quasi-circulator it is designed to match to 40 Ohms as mentioned in chapter 2.

There are two folds of low noise matching.

First, for minimum noise figure, the transistor Q1 requires source impedance to be a specific value. This best source impedance value and $F_{min}$ can be derived from the noise parameters of the transistor[30].

$$F_{\min} \approx 1 + (\frac{\omega}{\omega_t})\sqrt{2g_m(r_b + r_e)} \tag{4.1}$$

$$Zopt \approx (\frac{\omega}{\omega_t})\sqrt{\frac{2(r_b + r_e)}{g_m}} + \frac{j}{\omega(C_\pi + C_\mu)} \tag{4.2}$$

$R_{opt}$ =Re{$Z_{opt}$}can be chosen as 40 Ω by the size of transistor via $C_\pi$ and $r_b$ while keep Fmin remain the same with biasing fixed at a value giving highest $\omega_t$ . Thus, for a device of that size, a source impedance of 40 Ω would give the minimum noise figure.

Second, the low noise out-of-phase active combiner thus should have a $Z_{in}$ equal to the complex conjugate of the best source impedance, $Z_{opt}$. The input impedance for

this structure (assuming that the Miller effect is negligible and that $r_\pi$ is not significant at the frequency of interest) is:

$$Z_{in} = j\omega L_e - j\frac{1}{\omega C_\pi} + j\omega L_b + L_e\omega_t \ , \tag{4.3}$$

The real part of the input impedance must be equal to the source resistance $R_s$ to be matched for maximum signal power transfer.

Therefore, for differential mode signal:

$$\mathrm{Re}\{\ Z_{in,dm}\} = L_{e,dm}\omega_t = R_s \ , \tag{4.4}$$

Since the imaginary part of the deferential mode input impedance must equal to zero. Therefore, $L_b$ and $L_{e,dm}$ resonate with $C_\pi$, then:

$$L_b = \frac{1}{C_\pi\omega^2} - \frac{R_s C_\pi}{gm_1}, \tag{4.5}$$

While for common mode signal,

$$L_{e,cm} > L_{e,dm}, \tag{4.6}$$

Therefore,

$$Re\{Z_{in,cm}\} \ > \ R_s, \tag{4.7}$$

Besides less gain for common mode signal, large $Re\{Z_{in,cm}\}$ caused by large Lc also allows more transmission signal power goes to the antenna and less into the out-of-phase active combiner. This also means that for the same output power, less power is wasted at cancellation in contrast to conventional active quasi-circulator designs. Also the extra reactance of $Z_{in,cm}$ further reduces the power can be consumed by $\mathrm{Re}\{Z_{in,cm}\}$.

Based on the above analysis, the simple design procedure for simultaneously matching for power and noise for the Low noise out-of-phase divider was created. It can be summarized as follows [28]:

1. Find the current density in the process that enables the lowest minimum NF, and bias the transistor at this current density value regardless of the size of the device.

2. After the current density is settled, then is the length of the transistor. Scale emitter length such that $R_{opt}$ = 40Ω, scale the emitter length to make the real part of the optimum source impedance for lowest noise figure equal to 40Ω, while at the same time keep the current density the same.

3. Size Le, the emitter degeneration inductor, to create real part of the input impedance is 40 Ω for power match.

4. Place an inductor in series with the base $L_b$. This inductor is sized to resonate with $L_e$ and $C_\pi$ at the center frequency. This is to make the resultant input impedance equal to 40Ω without additional reactive component.

This technique achieves simultaneous noise and power matching of the transistor by selecting the emitter degeneration to form the real part of the input impedance as 40 Ω and then by selecting the size of the transistor to make $R_{opt}$ 40 Ω as well.

*Ls* is added to compensate the gain drop cause by parasitic capacitance at the emitter of $Q_2$ and collector of $Q_1$.

It should be mentioned that since the antenna is the only input, while there are two symmetric paths contributing noise power, thus, the NF of low noise out-of-phase

active combiner is 3dB higher than a conventional differential LNA design. Extra noise figure raise are contributed by noise comes from in-phase divider.

### 4.3 Balun design

Rat race is a conventional choice for differential to single ended conversion at microwave frequency because they offer good phase effectively, however, it takes much more area since it would take space in the scale ¾ effective wavelengths. A two single turn coupling “horseshoe” balun was designed and the two coupling “horseshoe” are staggered in two layers layout to reduce common mode capacitive coupling as shown below in Figure 19.

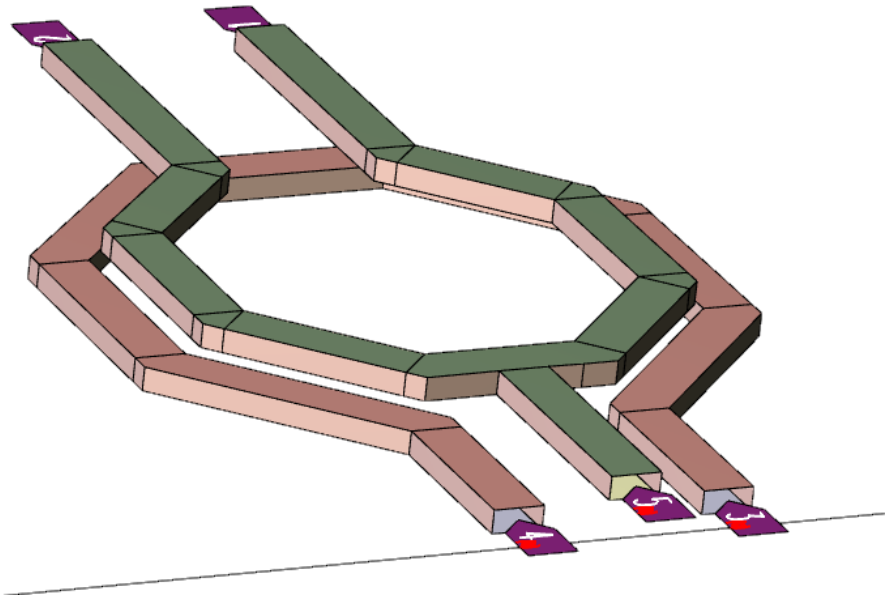

**Figure 19.** Staggered balun design.

### 4.3.1 CMRR of Balun

With Port 4 and Port 5 grounded, the CMRR of Balun is defined as:

$$CMRR = 20\log\left|\frac{S_{dm}}{S_{cm}}\right| = 20\log\left|\frac{S_{31} - S_{21}}{S_{31} + S_{21}}\right| , \tag{4.8}$$

Conventional overlapping balun can only reaches a CMRR in the range of 20-30dB, the proposed staggered balun reaches a CMRR 47dB at target frequency as shown in Figure 20.

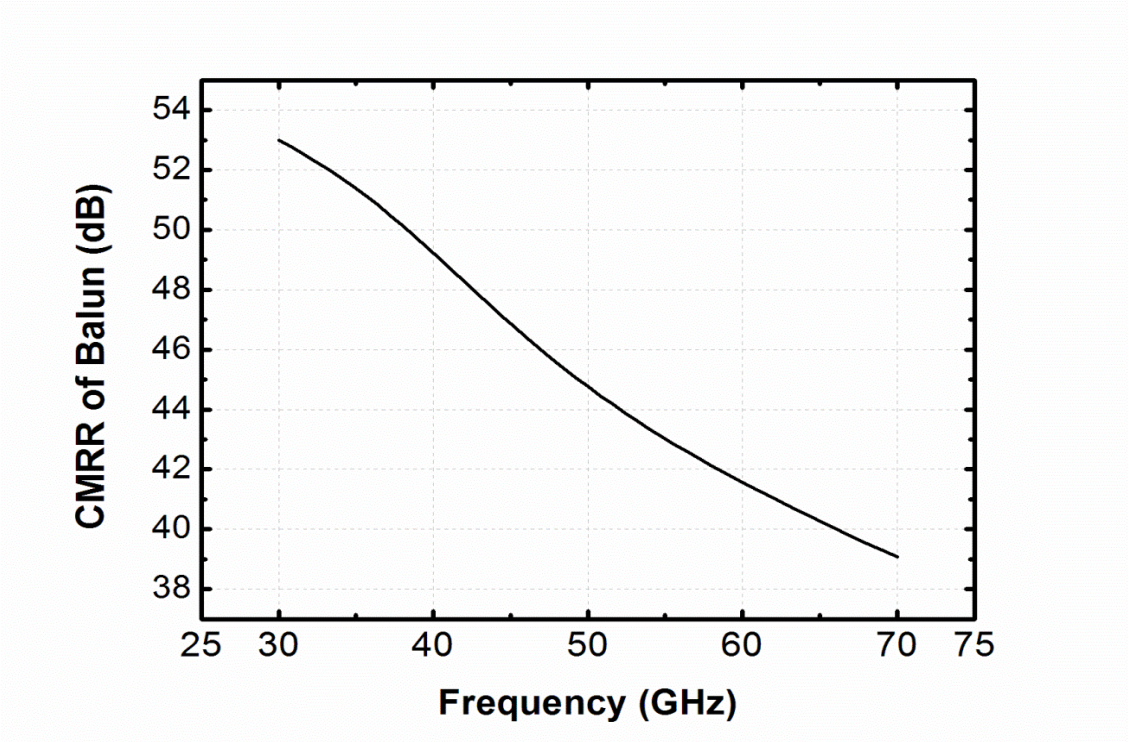


**Figure 20.** CMRR of staggered balun.

The performance of balun and all the inductors, RF pads and transmission lines are extracted from IE3D EM simulation.

CHAPTER V

ACTIVE QUASI-CIRCULATOR DESIGN AND RESULTS

## 5.1 Active quasi-circulator design

The circulator is comprised of Class AB active in-phase power divider, low noise out-of phase combiner discussed above and an L matching network to transform 50 Ohm antenna impedance to 40 Ohm as shown in Figure 21.

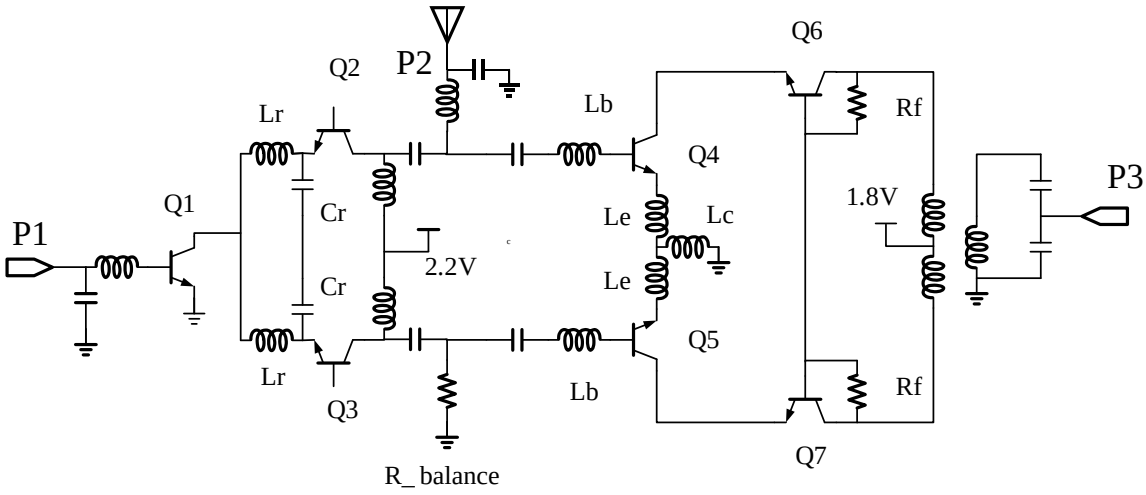


**Figure 21.** Full schematic of active quasi-circulator

In the layout Figure 22, transmission input (Port 1) is in the left, antenna port (Port 2) is in the upper side, reception output is at the right side. DC biasing and supplies are at the bottom.

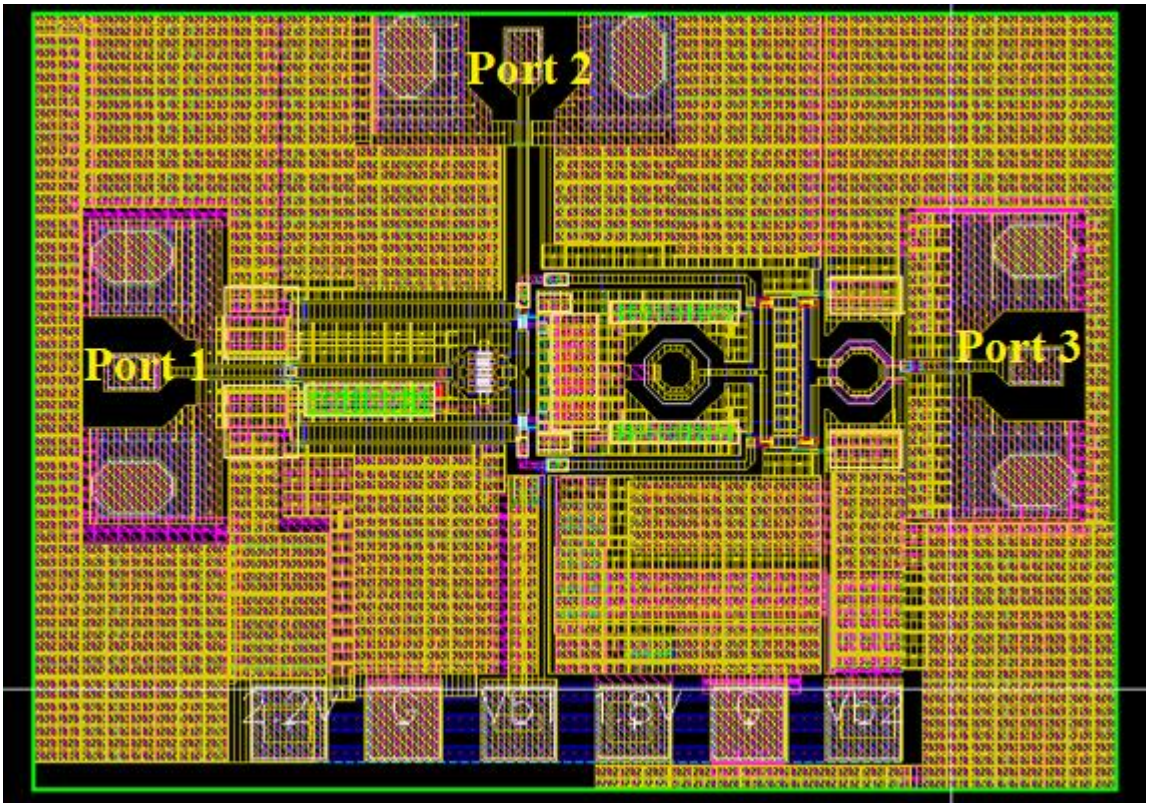


**Figure 22.** Full layout of active quasi-circulator in Jazz 0.18 µm BiCMOS [26].

### 5.2 Results

Post layout simulation results show that the circulator provides:

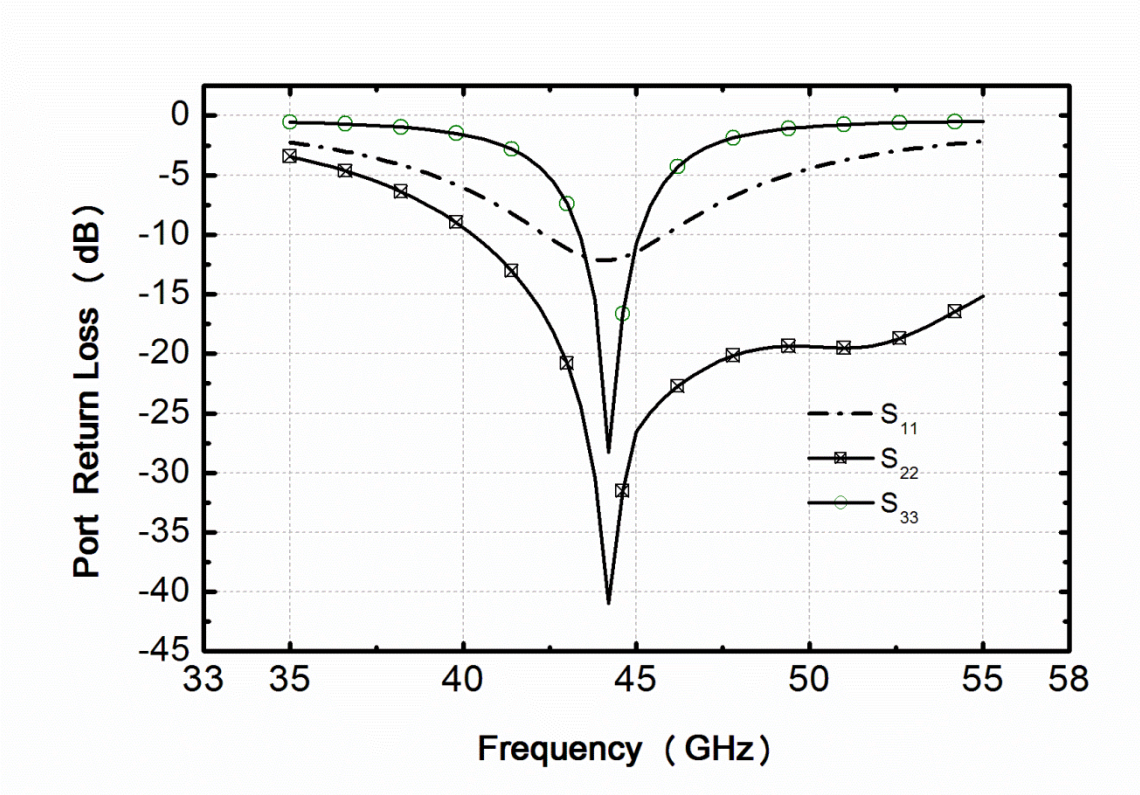


**Figure 23.** Return loss at each port.

Figure 23 shows the simulated return losses of each port. All the ports are well matched. The circulator achieves return loss of -12.08dB, -37.48dB, -18.05dB at port 1, 2 and 3 respectively at 44GHz.

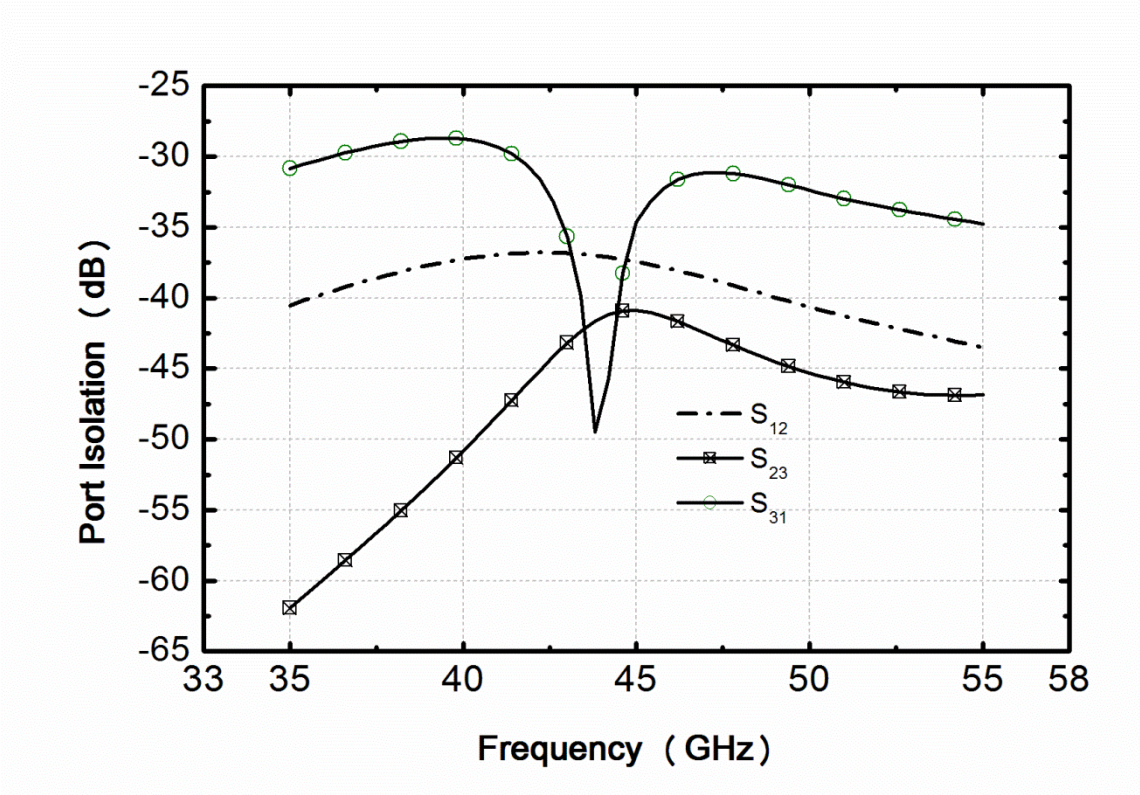


**Figure 24.** Port Isolations.

Figure 24 shows that $S_{12}$=-37.05dB, $S_{23}$=-41.43dB, $S_{31}$=-46.41dB at 44GHz.

Since $S_{31}$ is a critical performance based on symmetry, a Monte Carlo analysis based statistical models of foundry, which in most cases represent a more accurate prediction than corner models of expected impact of process variations on circuit-level figures of merit [26], is performed to investigate the effect of process variation and mismatch.

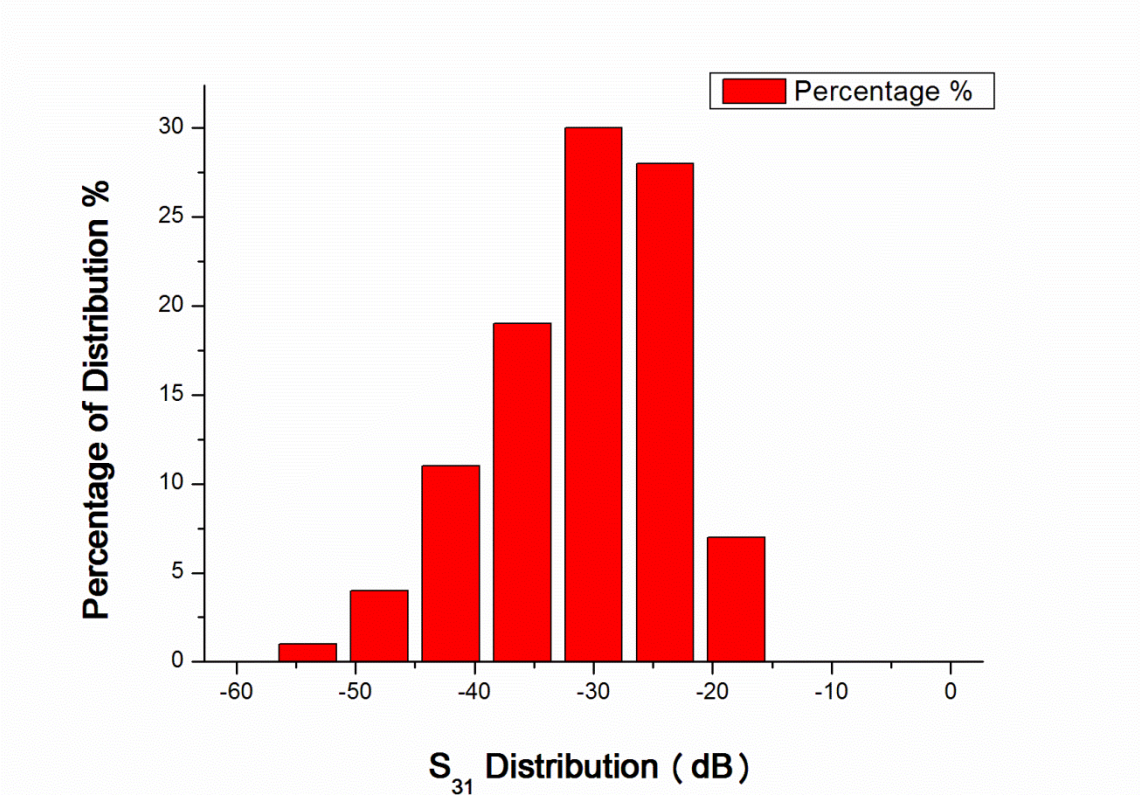


**Figure 25.** $S_{31}$ Distribution of Monte Carlo analysis at 44GHz.

As shown in Figure 25, after 100 runs of Monte Carlo analysis, the best $S_{31}$ can reaches -57dB, the worse S31 is -12dB and about 65% of the $S_{31}$ is better then -30dB. The main reason is that impedance of Port 2 doesn't vary together with the on chip R_balance, also the variation of L matching network impacts the impedance transforming and thus the symmetry.

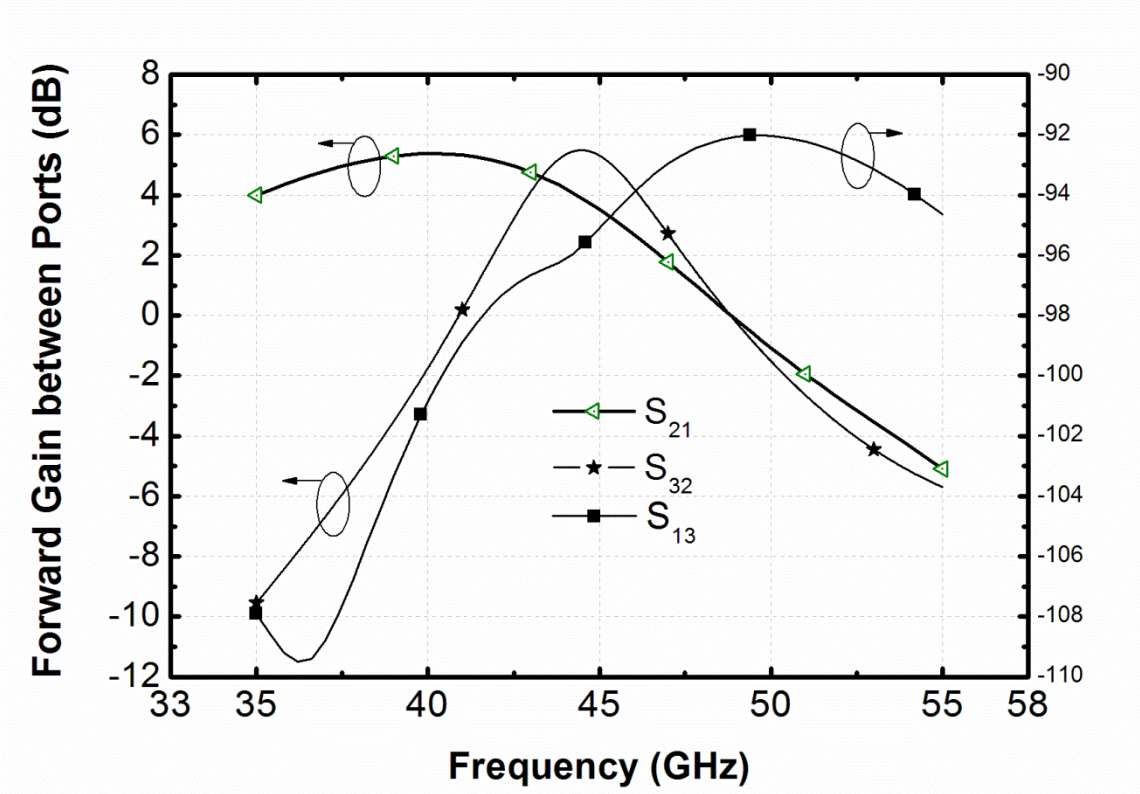


**Figure 26.** Forward Gain.

Figure 26 shows that $S_{21}$=4.213dB, $S_{32}$=5.314dB at 44GHz. Another forward gain is $S_{13}$, which is not needed for quasi-circulator. $S_{13}$ =-96.05 at 44GHz, which indicates a very low leakage from reception to transmission if there is reflection.

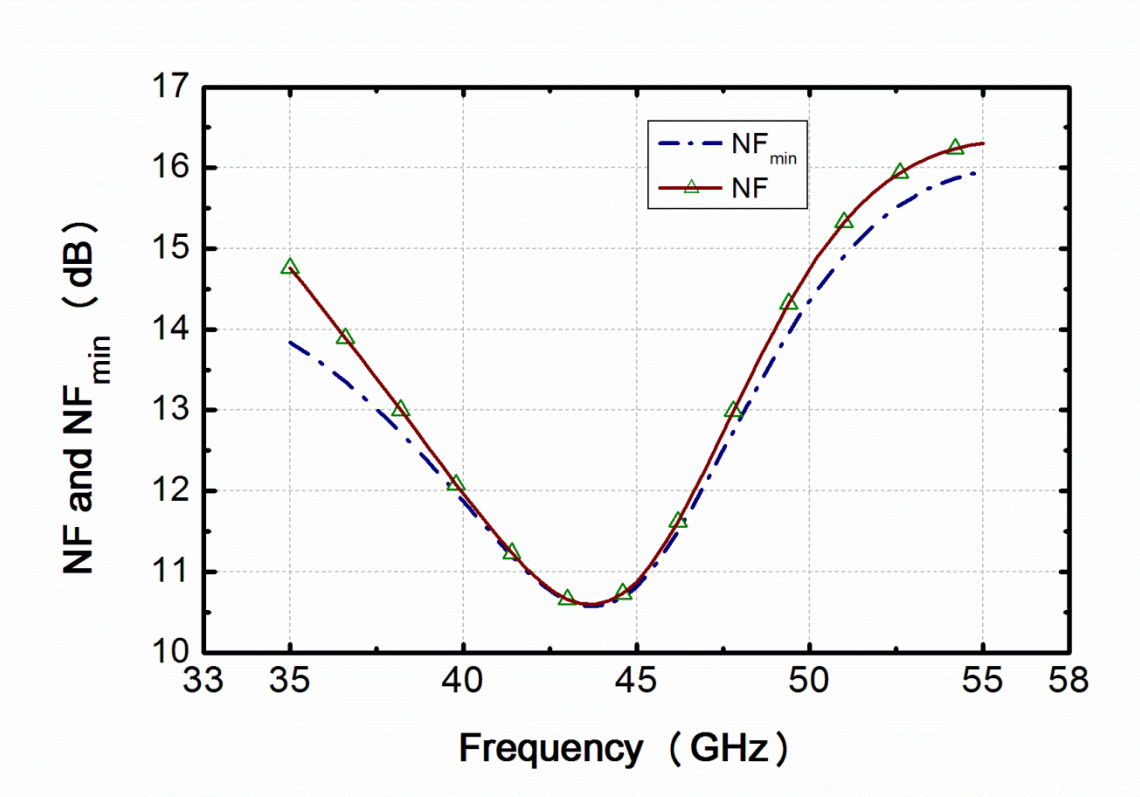


**Figure 27.** NF and $NF_{min}$, the circuit is designed very close to $NF_{min}$.

NF=10.62dB, only 0.03dB higher than $NF_{min}$. The NF value is relatively high because the extra contribution of active in-phase power divider and doubled reception paths with noise while only one reception path for signal in contrast to a normal low noise amplifier design.

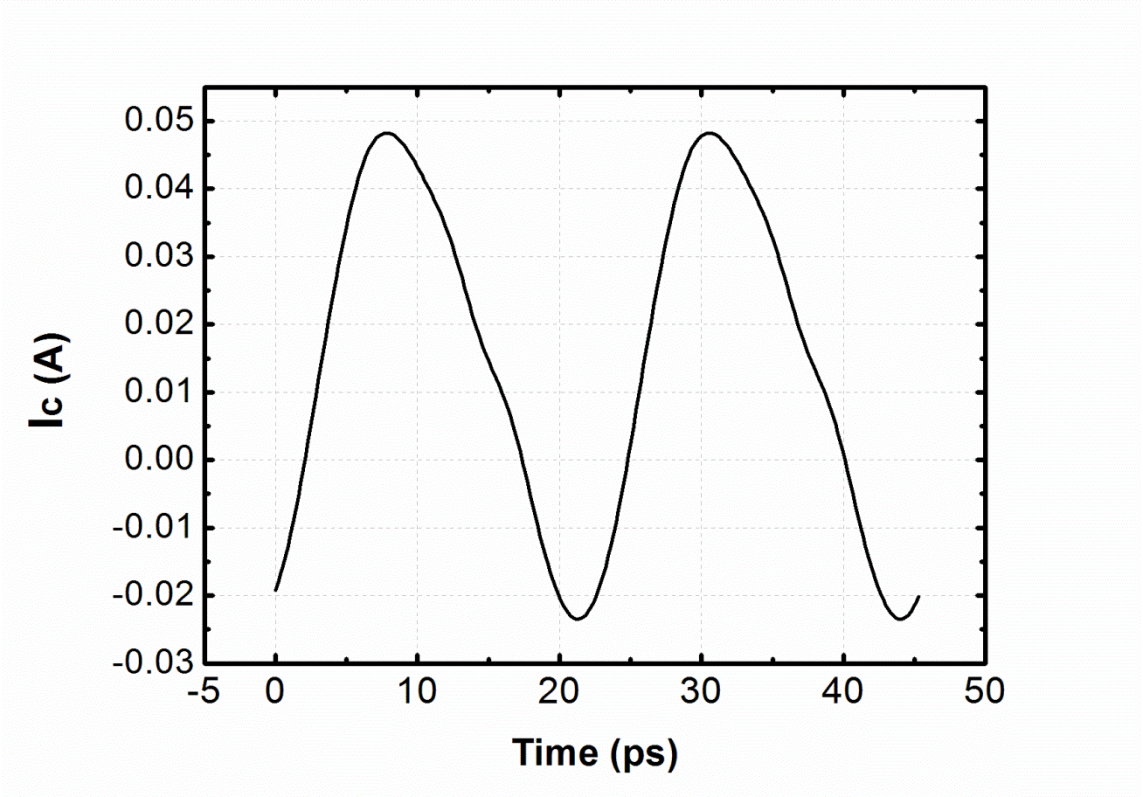


**Figure 28.** Collector current of Class AB active in-phase power

Class AB active in-phase power divider collector current shows the conduction angle is around 243 °, very close to the best value of 240 °. 2.32dBm output power to antenna is obtained at 3dBm power input at port 1.

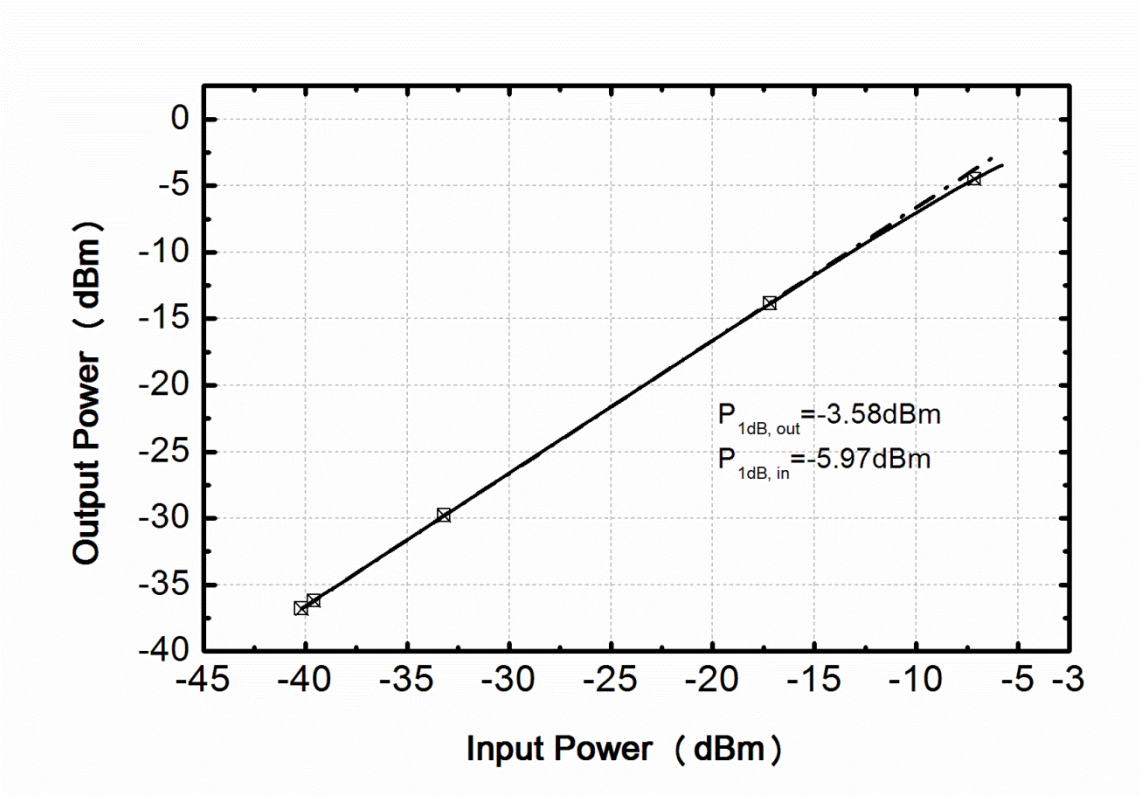


**Figure 29.** P1dB of active in-phase power divider.

The dotted line is ideal curve for output power versus input power, the solid line is practical curve with gain compression. The input P1dB compression is at -5.97dBm.

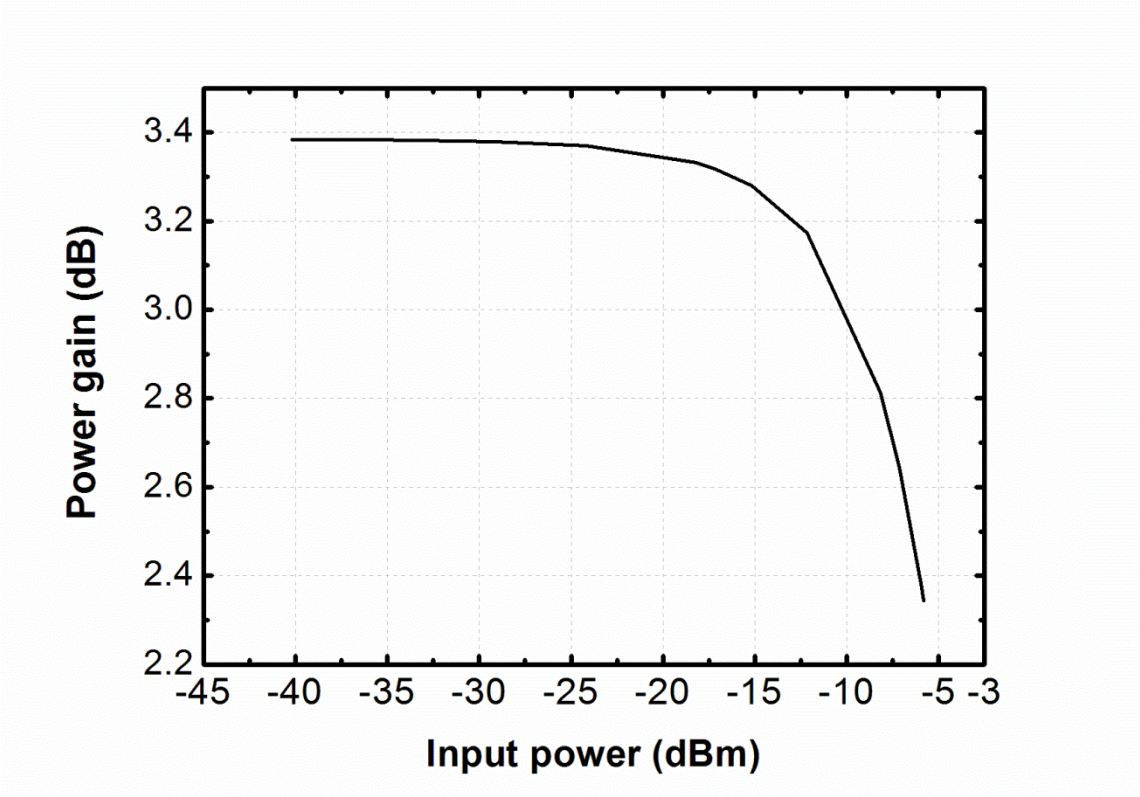


**Figure 30.** Gain compression of active in-phase power divider.

Figure 30 shows the gain compression of in-phase power divider as the input P1dB at -5.97dBm.

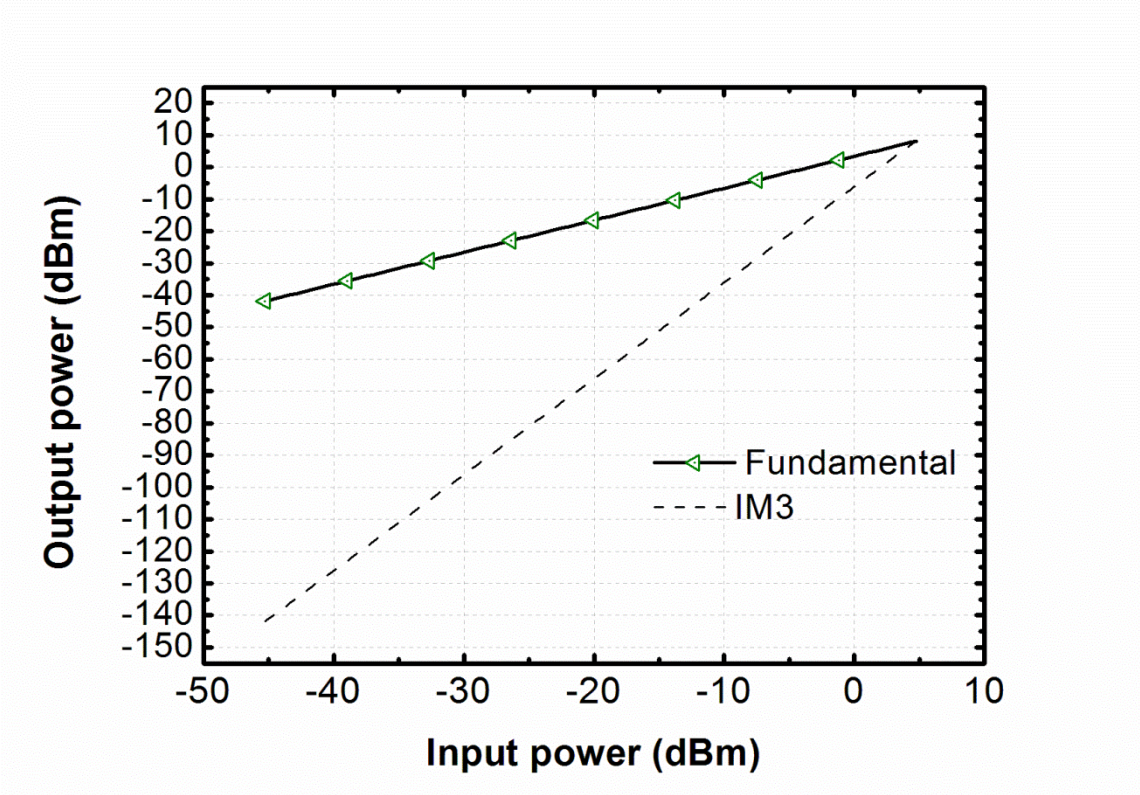


**Figure 31.** Linearity of active in-phase power divider.

Figure 31 shows that the IIP3 of the in-phase power divider is 4.48 dBm.

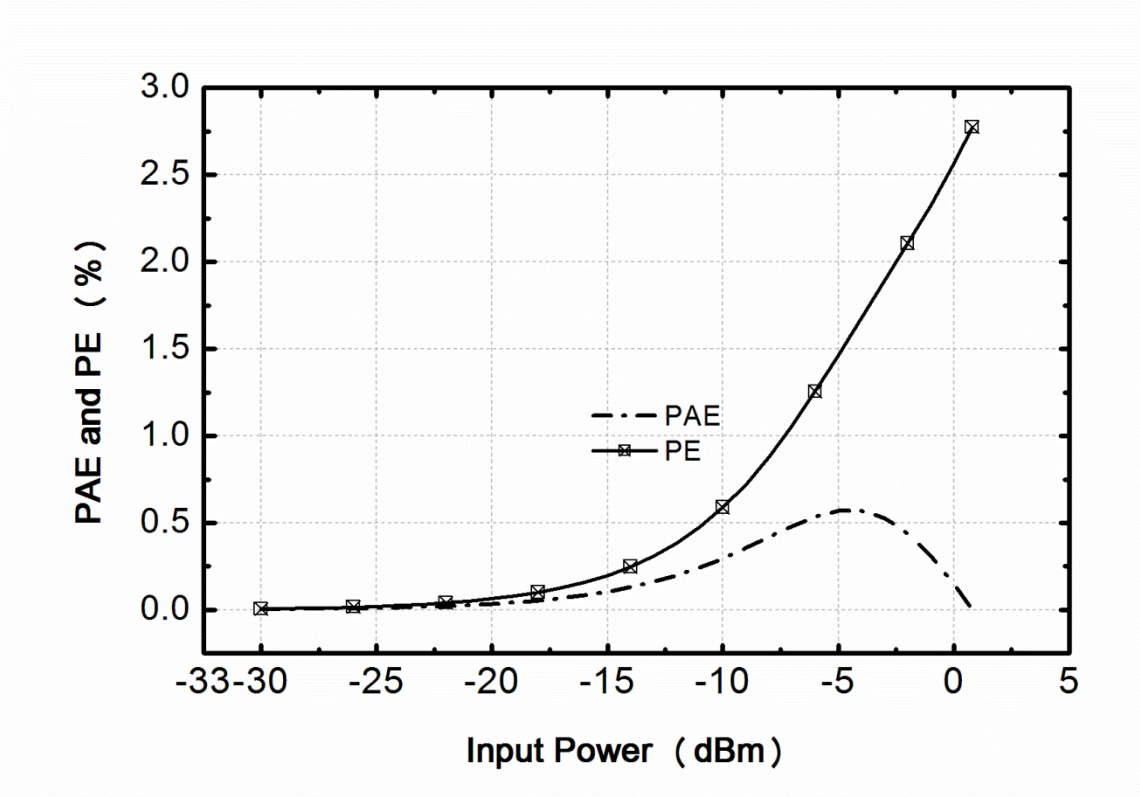


**Figure 32.** PAE and PE of in-phase divider.

The efficiencies are calculated from port 1 to port 2, so it doesn't count in the power in the R_balance and that going into out-of-phase active combiner.

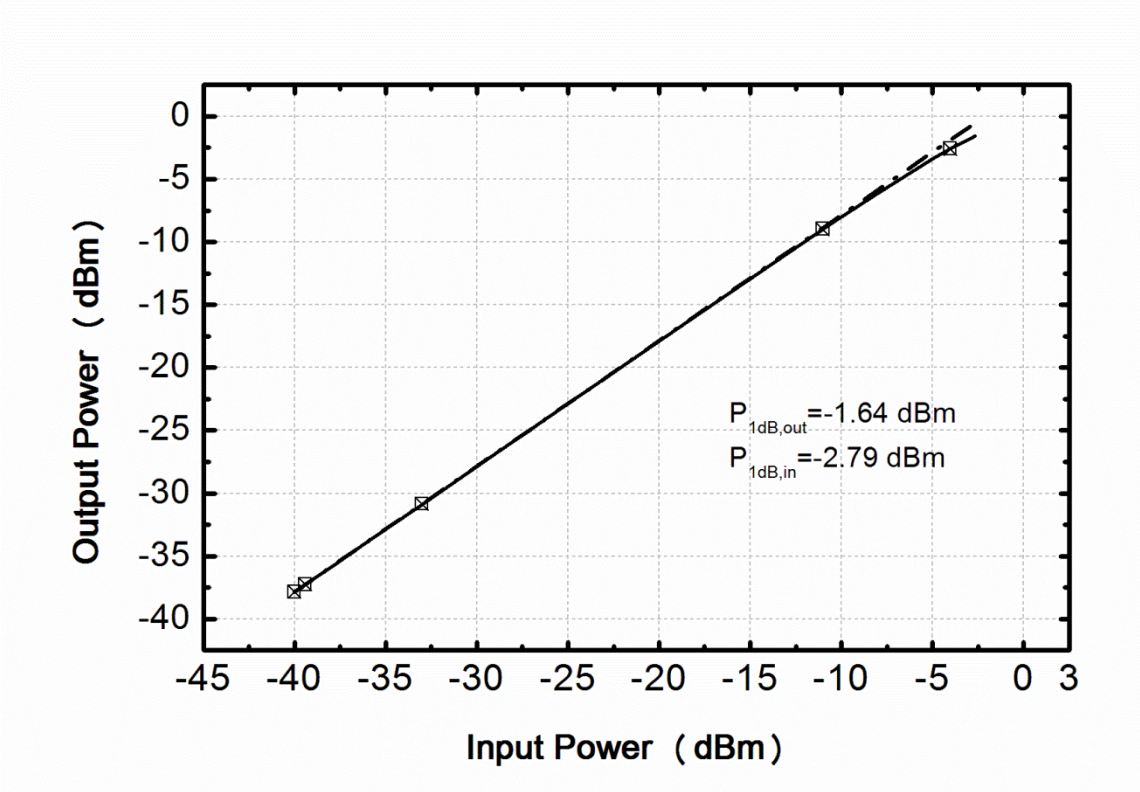


**Figure 33.** P1dB of out-of-phase active combiner.

The dotted line is ideal curve for output power versus input power, the solid line is practical curve with gain compression. The input P1dB compression is at -2.79dBm.

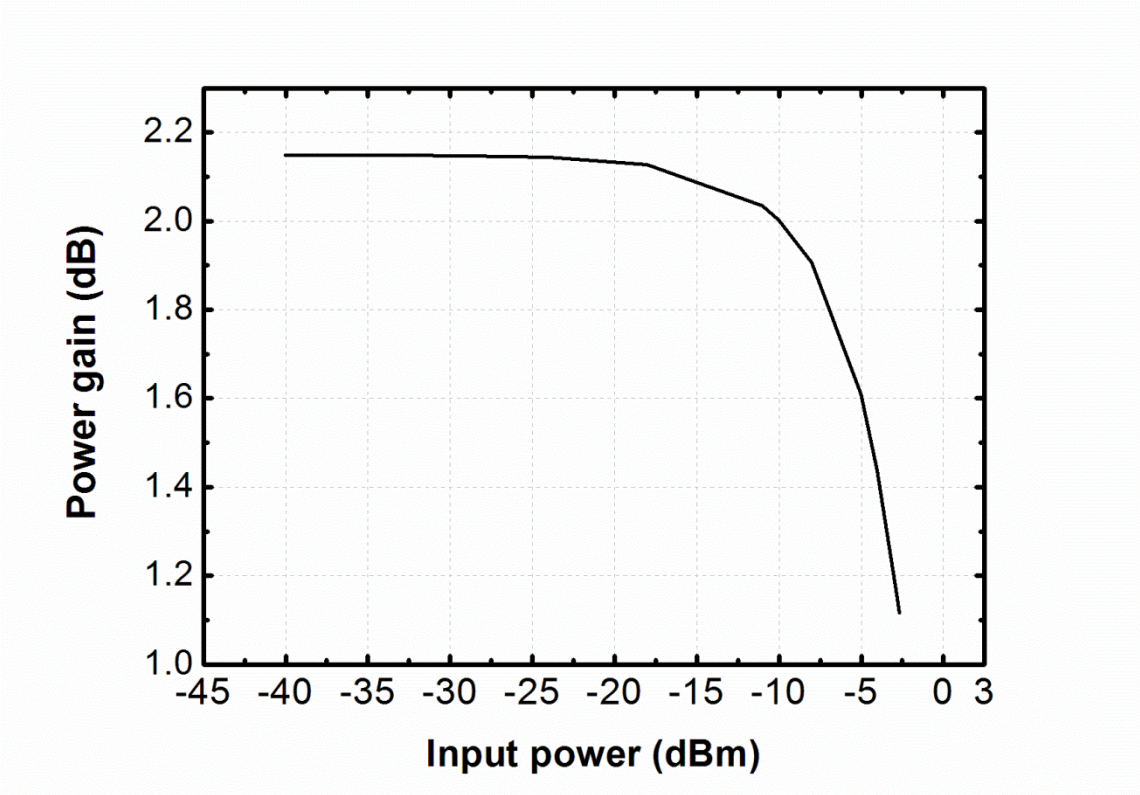


**Figure 34.** Gain compression of out-of-phase active combiner.

Figure 34 shows the gain compression of in-phase power divider as the input P1dB at -2.79dBm.

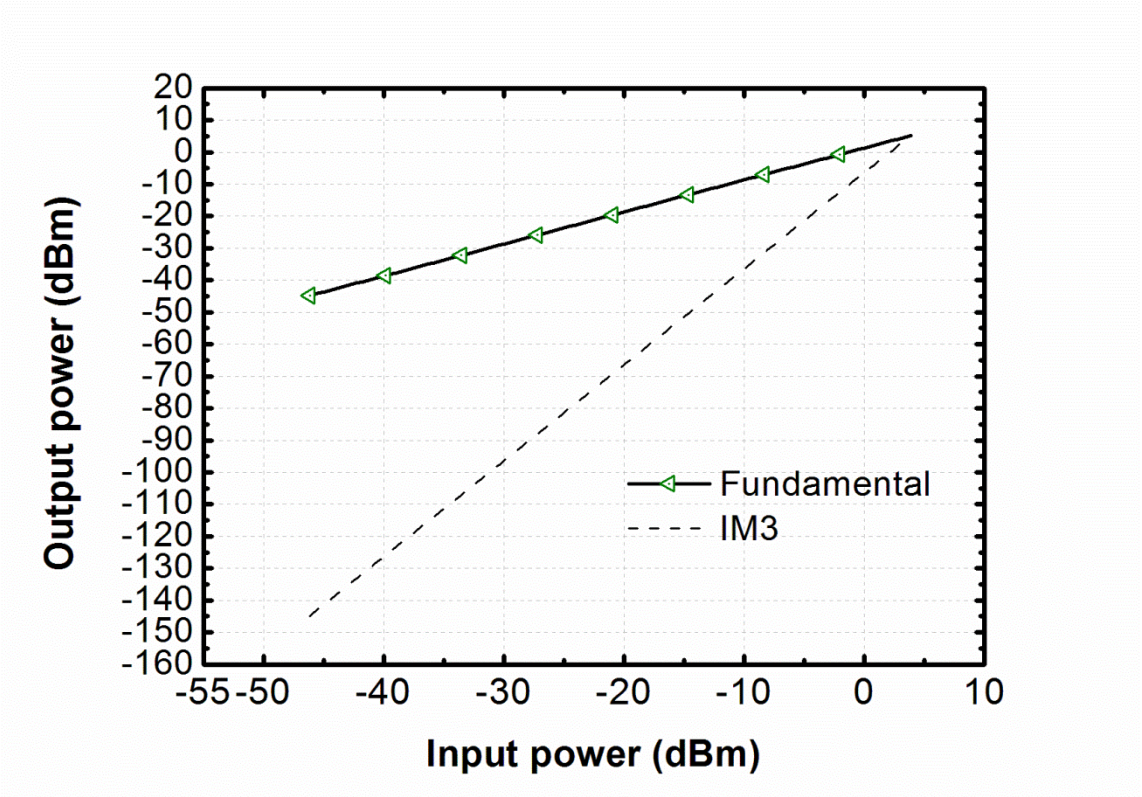


**Figure 35.** Linearity of out-of-phase active combiner.

Figure 35 shows that the IIP3 of the out-of-phase active combiner is 3.85 dBm.

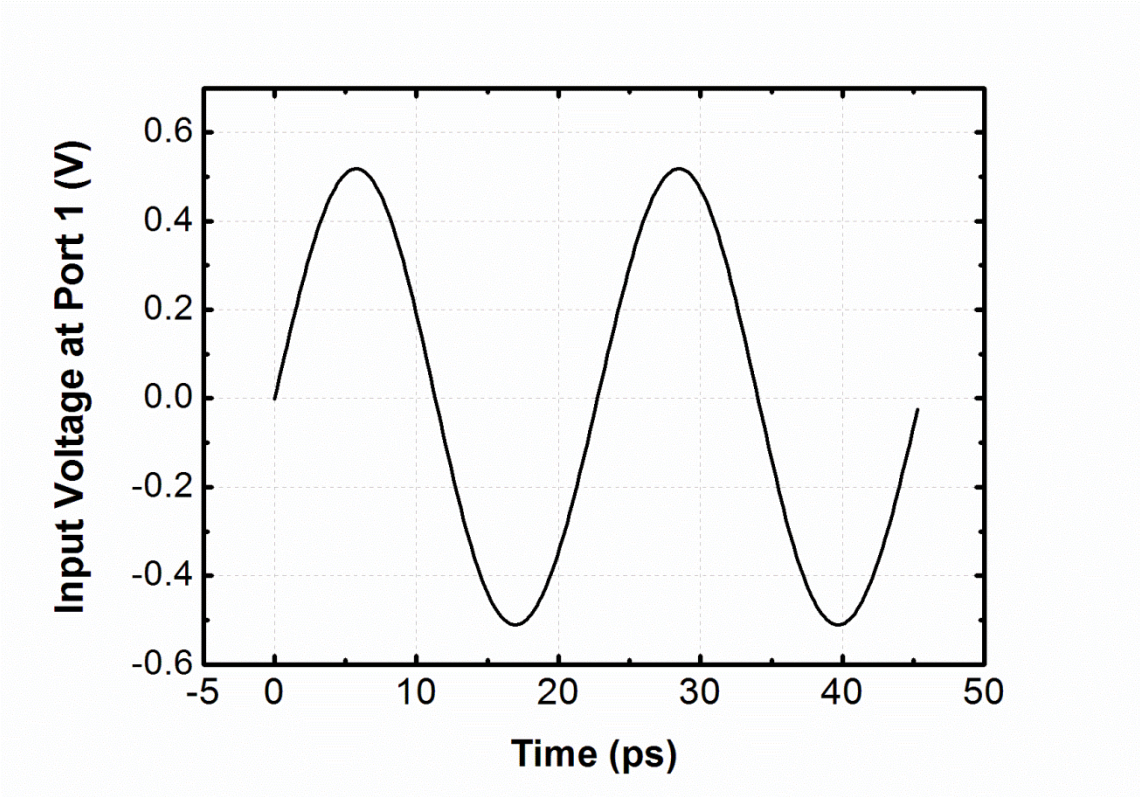


**Figure 36.** Input voltage waveform at Port 1.

The power actually gets into port one is 2.897dBm due to finite $S_{11}$.

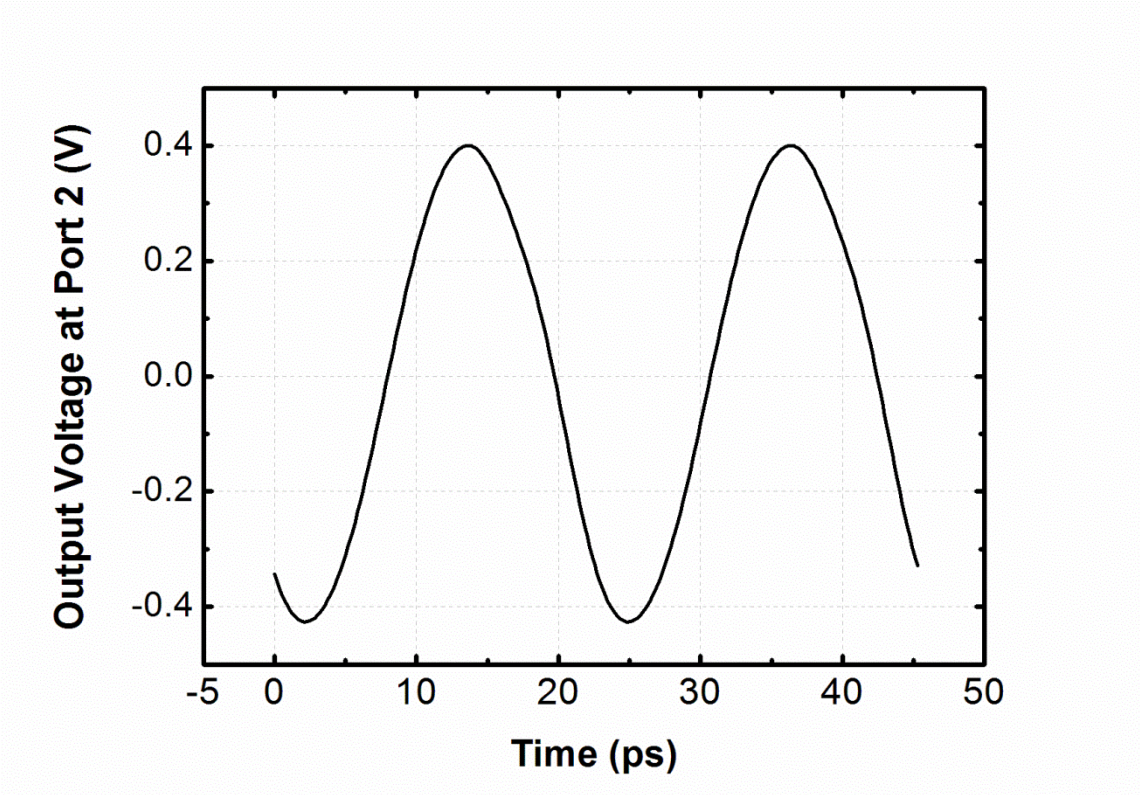


**Figure 37.** Output voltage waveform at port 2.

The output power from Port 2 is 2.32dBm, tiny degradation from input power when the gain is already saturated.

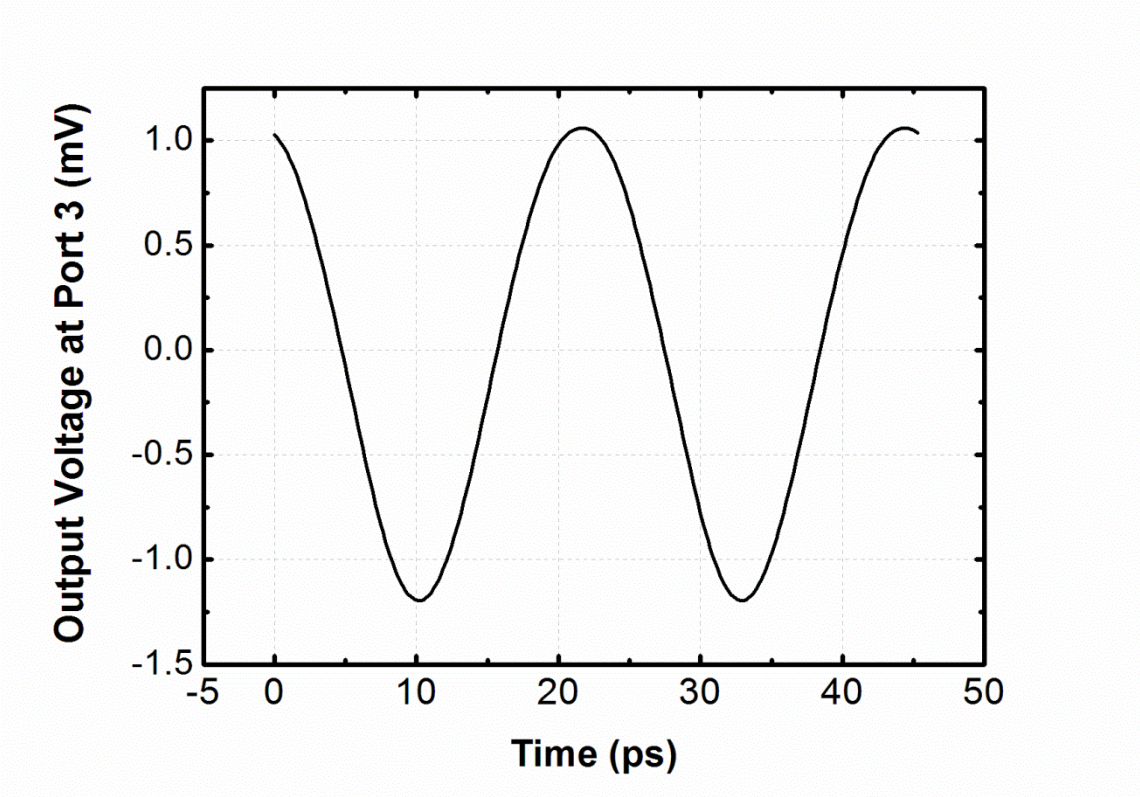


**Figure 38.** Residual transmission output voltage waveform at port 3.

With 2.897dBm power of transmission signal at Port 1, the leaked power of the transmission signal to the output of the out-of-phase active combiner is -48.94dBm, the $V_{pp}$ is 2.254mV over 50 Ohm load. Therefore large signal TX-RX isolation is 51.837dB. The reason why large signal isolation is better than small signal isolation is majorly due to gain drop of both in-phase divider and out-of-phase active combiner as large signal experience less gain.

The key performance of the active quasi-circulator at 44 GHz is summarized in Table 1.

**Table 1**. Performance summary table

| $S_{11}$ | $S_{12}$ | $S_{13}$ | NF | Pout |
|---|---|---|---|---|
| -12.08dB | -37.05dB | -96.05dB | 10.06dB | 2.32dBm |
| $S_{21}$ | $S_{22}$ | $S_{23}$ | Size | PDC |
| 4.213dB | -37.48dB | -41.43dB | 1.145mm*1.014mm | 56.83mW |
| $S_{31}$ | $S_{32}$ | $S_{33}$ | Large signal isolation | 3-dB Band width |
| -46.41dB | 5.314dB | -18.05dB | 51.837dB | 42.15GHz-46.68GHz |

# CHAPTER VI

# CONCLUSIONS

## 6.1 Conclusion

Directional couplers, switches, phase shifters and circulators would be deployed for future 60 GHz wireless communication [31] involving adaptive array antennas. These applications with directional device such as circulator are convenient but bulky for the demand of low cost, compact solution in modern and future wireless communication, especially in those mobile handsets favoring miniaturization.

In this thesis, a 44GHz low cost 0.18μm BiCMOS solution of active quasi-circulator is proposed, and several techniques to enhance isolation are presented, major parameters and tradeoffs are discussed. Such as: $S_{21}$, $S_{32}$ and $S_{31}$ are tradeoffs, the improvement of $S_{21}$, $S_{32}$ would degrade $S_{31}$. $S_{21}$ and NF are tradeoff. $S_{31}$ depends on techniques proposed, symmetric layout and deduction tuning, $S_{12}$, $S_{23}$ relies on good isolation of cascode structure.

The active quasi-circulator takes merely 1.415mm*1.014mm, operates around 44 GHz with 3dB bandwidth 4.53GHz.

Forward gain $S_{21}$=4.213dB, $S_{32}$=5.314dB. $S_{13}$=-96.07dB.

Reverse isolation $S_{12}$=-37.06dB, $S_{23}$=-41.43dB, $S_{31}$=-46.62dB. Large signal TX-RX isolation is 51.837dB.

NF=10.62dB, only 0.03dB higher than $NF_{min}$.

Maximum 2.897dBm input and 2.32dBm output power, which is limited by breakdown voltage in one node in the circuit. OIP3 of in-phase divider is 8.15dBm IIP3 is 4.48dBm, $P_{1dB,in}$ is -5.97dBm. OIP3 of out-of-phase active combiner is 5.18 dBm, IIP3 is 3.85dBm, $P_{1dB,in}$ is -2.79dBm.

Power consumption is 56.83mW, with in-phase divider consuming 32.47mW, out-of-phase active combiner consuming 24.36mW. This active quasi-circulator offers a low cost substitute solution for circulator in low power applications.

### 6.2 Suggestions for future work

In this thesis, the major design concerns are isolation and impedance matching at antenna port, with medium optimization of power and NF. Major tradeoffs among characteristics are discussed. There are many electrical performances that can be considered for improvement, such as frequency response, bandwidth, linearity, efficiency, power handling capability, noise figure. Therefore, detailed analysis of minimum noise figure design with finite output impedance of in-phase divider and investigation of avoiding the tradeoffs mentioned are good research topic in the future.

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