ADVANCES IN INTEGRATED CIRCUIT DESIGN AND IMPLEMENTATION FOR NEW GENERATION OF WIRELESS TRANSCIEVERS

A Dissertation

by

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ABSTRACT

User's everyday outgrowing demand for high-data and high performance mobile devices pushes industry and researchers into more sophisticated systems to fulfill those expectations. Besides new modulation techniques and new system designs, significant improvement is required in the transceiver building blocks to handle higher data rates with reasonable power efficiency. In this research the challenges and solution to improve the performance of wireless communication transceivers is addressed.

The building block that determines the efficiency and battery life of the entire mobile handset is the power amplifier. Modulations with large peak to average power ratio severely degrade efficiency in the conventional fixed-biased power amplifiers (PAs). To address this challenge, a novel PA is proposed with an adaptive load for the PA to improve efficiency. A nonlinearity cancellation technique is also proposed to improve linearity of the PA to satisfy the EVM and ACLR specifications.

Ultra wide-band (UWB) systems are attractive due to their ability for high data rate, and low power consumption. In spite of the limitation assigned by the FCC, the coexistence of UWB and NB systems are still an unsolved challenge. One of the systems that is majorly affected by the UWB signal, is the 802.11a system (5 GHz Wi-Fi). A new analog solution is proposed to minimize the interference level caused by the impulse Radio UWB transmitter to nearby narrowband receivers. An efficient 400 Mpulse/s IR-UWB transmitter is implemented that generates an analog UWB pulse with in-band notch that covers the majority of the UWB spectrum.

The challenge in receiver (RX) design is the over increasing out of blockers in applications such as cognitive and software defined radios, which are required to tolerate stronger out-of-band (OB) blockers. A novel RX is proposed with a shunt N-path high-Q filter at the LNA input to attenuate OB-blockers. To further improve the linearity, a novel baseband blocker filtering techniques is proposed. A new TIA has been designed to maintain the good linearity performance for blockers at large frequency offsets. As a result, a +22 dBm IIP3 with 3.5 dB NF is achieved.

Another challenge in the RX design is the tough NF and linearity requirements for high performance systems such as carrier aggregation. To improve the NF, an extra gain stage is added after the LNA. An N-path high-Q band-pass filter is employed at the LNA output together with baseband blocker filtering technique to attenuate out-of-band blockers and improve the linearity. A noise-cancellation technique based on the frequency translation has been employed to improve the NF. As a result, a 1.8dB NF with +5 dBm IIP3 is achieved. In addition, a new approach has been proposed to reject out of band blockers in carrier aggregation scenarios. The proposed solution also provides carrier to carrier isolation compared to typical solution for carrier aggregation.

To My Mother, Father and Brother

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CHAPTER I

INTRODUCTION

As the market and user demand for higher data rates increases, new architectures and building blocks are needed to support higher performance mobile handsets. The first step requires more complicated system design together with complicated modulation schemes such as OFDM 256 QAM. These modulations will force stringent requirements on the implementation of the building blocks inside the handset receiver and transmitter. Furthermore, the battery life of the mobile handsets should not degrade by the sophisticated circuit architectures added for higher performance capability. Figure 1.1 shows the block diagram of a typical frequency division duplexing (FDD) radio frequency (RF) transceiver architecture.

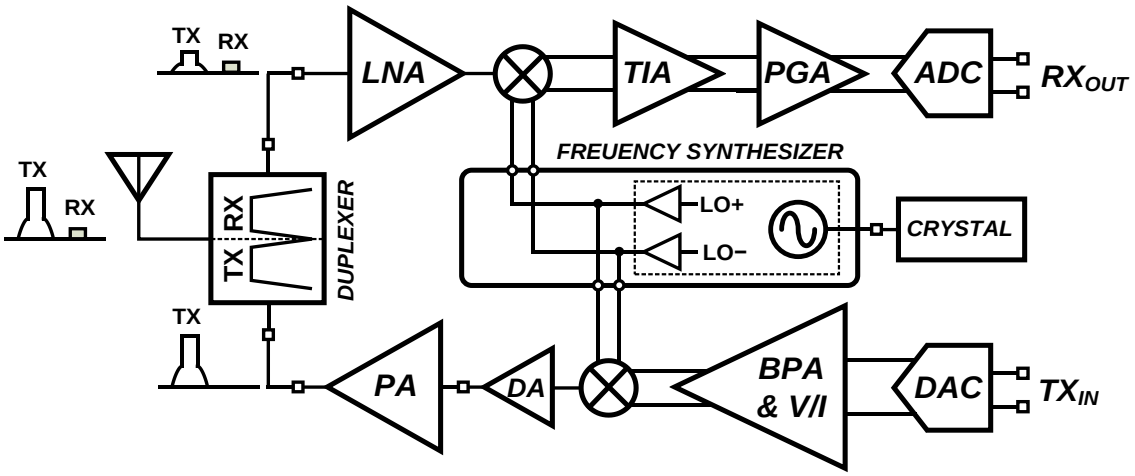


Figure 1.1. Block diagram of a typical FDD RF transceiver.

One of the most important building blocks of the transceiver is the power amplifier (PA). A PA with very large power consumption degrades the efficiency of the handset considerably. As an example, a typical PA consumes 2-3W DC power to deliver a 1W RF power to the antenna, which is more than 90% of the power consumption of the entire transceiver. Table 1. 1 shows the power consumption of a typical transceiver. Therefore, a very small improvement in the efficiency of the PA, can save tens of mAs which is very hard to save while designing other blocks inside the transceiver. Furthermore, PA non-linearity limits the performance of the system. As the signal modulation becomes more complicated, error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR) requirements for the PA becomes more and more stringent which can no longer be met by typical PA architectures in the literature [1]-[2].

Table 1. 1. Power consumption of a typical RF transceiver

Transceiver Blocks	TX				RX		LO Generation		Digital
	PA	DA	TX BB	Mixer	LNA + Mixer	RX BB	Frequency Synthesizer	LO Chain	ADC + DAC
Power (W)	2.5	0.05	0.02	0.03	0.015	0.02	0.03	0.02	0.15

Another emerging technology for high-data rate low range wireless applications is the Ultra wide-band (UWB) transceivers [3]. UWB systems are attractive due to their ability for high data rate, low power consumption, low complexity, and low cost communications. Unlike NB systems, UWB is transmitting narrow pulses for

communication, with simple modulation techniques such as ON OFF keying. Due to FCC regulation, the transmit power cannot be greater than -41.3 dBm/Hz. Therefore, in most cases no PA is being employed, which makes UWB transmitter very efficient, and the power consumption is usually dominated by the receiver side.

Three different UWB architectures have been proposed in the literature. Multi Band Orthogonal Frequency Division Multiplexing (MB-OFDM), Impulse Radio UWB (IR-UWB), and Direct Sequence UWB (DS-UWB) [3]. UWB systems need to work at the presence of many high power systems such as IEEE 802.11a/g. The FCC mask provided for UWB communications is for avoiding any disturbance to other operating narrow-band (NB) systems within the UWB band. For an IEEE 802.11a system working in a Line of Sight (LOS) environment, the effect of UWB interferer is negligible, but if the environment is non-Line of Sight (NLOS), then 802.11a receiver will be easily jammed by the UWB interferer. By increasing the number of UWB users, the performance of the NB system would be greatly degraded even in LOS environment. For a UWB system working at the presence of an 802.11a interferer, irrespective of the environment (LOS or NLOS), the UWB system is quite vulnerable to NB interference [4]-[6]. It can be concluded that in spite of the limitation assigned by the FCC, the coexistence of UWB and NB systems is still an unsolved challenge.

Let's assume that in an IEEE 802.11a system, the minimum detectable signal must have a bit error rate (BER) of 10^{-5} to achieve a data rate of 54 Mbps. In the presence of a UWB TX (r=1m) to maintain the same data rate, the minimum detectable signal drastically degrades, and the NB RX has to decrease the data rate (SNR) to

increase the range of detectable NB TXs. In the absence of a UWB interferer, it can be calculated that the NB RX could maintain a 24 Mbps data rate (assuming 10 dB SNR) up to 30 meters communication range from the NB TX. This range decreases to 25 and 10 meters in the presence of UWB TX for r=5m and r=1m, respectively [7]-[8]. Therefore, it is very crucial to find a solution in which, the performance of the 5 GHz Wi-Fi is not affected by the transmission of the UWB pulses.

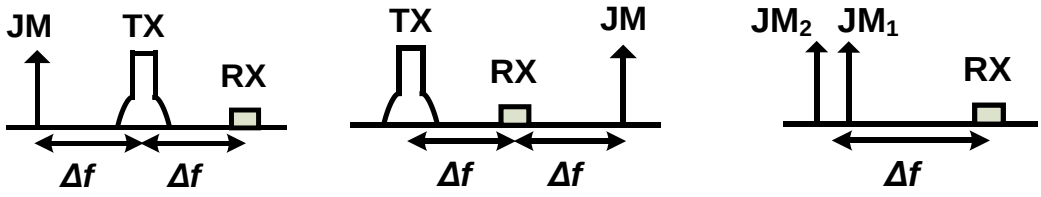
The PA not only limits the performance of the transmitters, but also significantly affects the design of the receiver. The PA out-of-band noise can severely degrade the sensitivity of the receiver [9]. In FDD systems, the average output power is 20dBm. If the duplexer provides 50dB isolation from TX to RX, the TX leakage to the receiver is -30dBm [9]. This leakage forces stringent linearity requirements on IIP3 and IIP2 of the receiver. Also, the receiver noise figure (NF) will be degraded by the continuous large TX leakage at the RF input. Therefore, the stand-alone NF performance of the receiver is no longer valid in FDD systems.

One of the major impacts of high data rate systems on receiver is the larger signal to noise ratio (SNR) requirements. As the SNR increases, the receiver requires a much smaller NF. The required SNR is close to 25dB in state of the art receivers. The sensitivity of an RF receiver is calculated using [9]

$$Sensitivity = -174 \frac{dBm}{Hz} + NF + 10\log(BW) + SNR_{min} \quad (1\text{-}1)$$

For 4G LTE standard with 10MHz signal bandwidth (BW=10 MHz) and -87 dBm receiver sensitivity, the required NF is less than 2dB. On the hand, many out of

band jammers together with the TX leakage provide very stringent linearity requirements on the receiver. Figure 1.2 shows 3 different linearity scenarios. As an example the IIP3 (Figure 1.2(a)) is required to be better than 0dBm. There are two different IIP2 test which is shown in Figure 1.2(b), and (c). IIP2 in case (b) is limited by the LNA non-linearity and usually needs to be better than 20dBm across the corners and temperatures. While IIP2 in case (c) is limited by mixer mismatch and mixer switches non-linearity and typical numbers are 40-50 dBm.



(a) (b) (c)

Figure 1.2. Linearity test scenarios (a) in-band resulted IM3 (IIP3), (b) in-band resulted IM2 (IIP2), (c) in-band resulted IM2 (IIP2).

As a result of these stringent linearity and NF requirements, the architectures are limited to multi narrow-band receivers to cover a large frequency band. Narrowband receivers use inductive source degenerated LNAs which has a very good noise performance due to noise-less matching. Furthermore low-loss off-chip elements is used for matching and blocker filtering at the input of narrowband receivers which improves both linearity and NF. In order to achieve a small NF of 2dB for the entire receiver, the

I/Q mixer can no longer be active. The mixer after the LNA needs to be passive with zero DC current to minimize 1/f noise contribution from the mixer to the RX NF. The mixer needs to be drived with non-overlapping LO signals to improve NF and linearity. With 50% duty cycle LOs, the noise contribution from the mixer is almost two times. Also the non-linearity's from the baseband I/Q will be up-converted to RF frequency and then down-converted to Q/I baseband again, which will degrade linearity. The drawback of using non-overlapping LOs for the mixer driver is the increase in the power consumption of the LO generation and the LO distribution. The second drawback is high LO harmonics feed through at the passive mixer input which may degrades the receiver linearity and should be carefully investigated.

In order to improve data rate, the signal bandwidth (BW) needs to increase to 40-100MHz. Since it is very hard to find an unused 100MHz spectrum for mobile handsets, carrier aggregation (CA) has been proposed. When continuous bandwidth in 1 carrier is not available, the signal BW can be increased through simultaneous transmission in different carriers. Therefore, multiple carriers are used to transmit the signal from the baseband station to the user to increase the signal bandwidth. As a result the handset receiver should be capable of simultaneous reception of the signal in all the carriers. The receiver is required to have separate paths with certain LO frequencies for each carrier. Simultaneous operation of all the carriers put extra linearity and NF requirements on the receiver and makes the design very challenging.

Increasing the signal BW in single carrier makes the baseband design very challenging. Previously for mobile communications, the signal BW was 10MHz, which

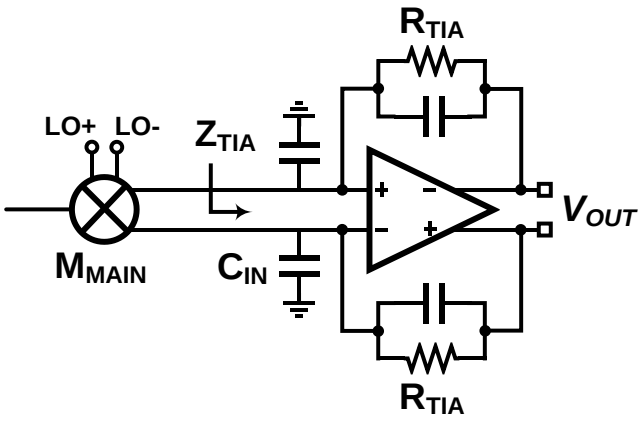
is increased to 20-40 MHz in 4G LTE (single carrier). To maintain a very good NF across the signal BW, the baseband unit (TIA) needs to have a very good loop-gain throughout the baseband signal, otherwise the receiver integrated NF increases. Maintaining a very good gain in an OP-AMP up to 20MHz (RF 40MHz) is very challenging. Furthermore the TIA should maintain a good loop-gain at the frequency of the jammers (which are down-converted to baseband with an offset from the LO frequency) to maintain a good receiver linearity performance. All these specifications require the TIA to have a unity gain bandwidth of close to 1GHz, with a very good loop-gain. It is very challenging to make the TIA stable with such a large GBW.

Figure 1.3 (a) shows a typical TIA architecture. R_{TIA} and C_{TIA} are usually set to the 3dB signal BW. Due to smaller 3dB BW of the OTA, the input impedance starts to increase as the gain drops, and peaks at higher frequencies (Figure 1.3(b)). The input impedance peaking of the TIA increases the voltage swing at the TIA input. If passive mixers are used, the same swing will be translated to RF, which will degrade LNA and mixer linearity as well as the TIA. To decrease this effect, a parallel capacitor C_{IN} is added at the TIA input which lowers the peaking value and the peaking impedance (Figure 1.3(b)).

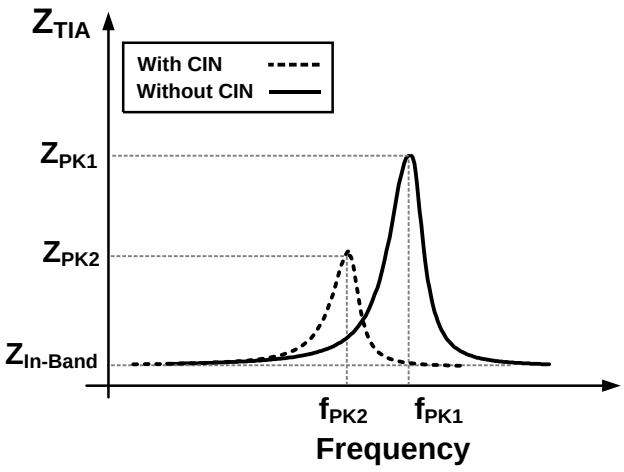
Summary of challenges in wireless transceiver design:

- Challenge 1: Efficiency improvement in wireless PAs for 4G-LTE.
- Challenge 2: Linearity improvement in wireless PAs for 4G-LTE.
- Challenge 3: NF improvement in WB receivers for 4G-LTE applications.

- Challenge 4: Blocker filtering and linearity improvement in software defined radios, cognitive radios, and 4G LTE applications
- Challenge 5: Blocker filtering for carrier aggregation.
- Challenge 6: Solving the coexistence problem between NB and UWB transceivers.



(a)



(b)

Figure 1.3. (a) TIA architecture with the input capacitance, (b) TIA input impedance with and without the input capacitor C_{IN}.

Dissertation organization

The dissertation consists of 5 chapters as follows:

Chapter II presents a new reconfigurable matching network technique in a fully integrated class AB PA in 0.25 µm SiGe:C BiCMOS technology The PA delivers 23 dBm maximum output power with simultaneous efficiency and linearity improvement. Efficiency improvement is achieved by switching the biasing states of the transistors based on the input power level of the signal which is monitored by an envelope detector. The gain of the PA in transition remains constant by implementing a reconfigurable matching network for both high and low input signal levels. The linearity is greatly enhanced based on a feed forward non-linear cancellation technique. Therefore, the proposed PA can improve both PA efficiency and linearity in high data rate standards such as WiMAX, and 4G LTE for handsets, and can be tuned to the desired frequency band.

In chapter III, an IR-UWB TX with in-band notch implementation is presented. The TX generates an analog UWB pulse that covers the majority of the UWB spectrum. It employs the frequency characteristics of a Gaussian monocycle pulse and features a tunable notch in the frequency of the in-band NB system. Due to the unique pulse generation technique, the proposed UWB TX causes a small interference power (~ -78 dBm/MHz) for the IEEE 802.11a RX; while the bandwidth of the signal is larger than 5.5 GHz. The TX data rate can reach to 400 Mpulse/s with energy of 65 pJ/Pulse at maximum data rate. We have designed and implemented a new approach to minimize the interference caused by the UWB transmitter to nearby narrowband receivers. He

employs a new analog solution to solve the mutual interference challenge between IR-UWB and NB systems. He proposed an efficient IR-UWB transmitter with in-band notch implementation. The transmitter generates an analog UWB pulse that covers the majority of the UWB spectrum. The transmitter employs the frequency characteristics of a Gaussian monocycle pulse and features a tunable notch in the frequency of the in-band NB system. Due to the unique pulse generation technique, the proposed UWB transmitter causes the smallest interference power reported in the literature (~ -74 dBm) for the IEEE 802.11a receiver; while having a bandwidth larger than 5.5 GHz. The transmitter has a high data rate of 400 Mpulse/s and energy of 65 pJ/Pulse. Therefore, the 5 GHz Wi-Fi receiver can fully maintain its performance even in the presence of the proposed UWB transmitter.

In chapter IV, a novel wideband receiver has been designed to replace bulky narrow-band receivers in 4G LTE applications. In order to cover a certain bandwidth, multiple NB receivers are usually employed in industry. While a wideband receiver can replace all the NB counterparts, the inferior performance of wideband receivers is the key factor. In this chapter multiple linearity and noise improvement techniques has been employed to wideband receivers without adding any off-chip elements. By using a high-Q on-chip band-pass filter to attenuate blockers, the linearity is significantly improved. A noise-cancelling approach has been used to cancel the noise from the selective network. The receiver is implemented in 40nm CMOS technology. As a result, a wideband receiver with 1.8 dB NF and 5 dBm IIP3 has been achieved.

In chapter V, a wideband blocker tolerant receiver has been designed for software defined and cognitive radios. To achieve a good linearity, blockers and jammers are rejected prior to the LNA stage by a high-Q N-path filter. The noise contribution of the added network is cancelled out through the main path. A baseband blocker filtering technique is added to further improve the linearity. Another blocker rejection technique is added inside the mixer, by using a dual mixer architecture. A particular TIA has been to mitigate the TIA input impedance peaking issue to higher frequencies. As a result of several linearity improvement techniques, the receiver achieved an out of band IIP3 of +22 dBm with 3.5 dB NF.

CHAPTER II

HIGHLY EFFICIENT HIGHLY LINEAR RF POWER AMPLIFIER*

II.1. Introduction

Modern communication systems target higher data rates for portable devices such as personal communication systems (PCS) and satellite communications. High data rate applications require modulation techniques such as Orthogonal Frequency-Division Multiplexing (OFDM). These systems implemented in handsets, should employ power amplifiers with both high linearity to achieve the required signal-to-noise ratio (SNR) for low bit-error-rate (BER $=10^{-6}$), and high efficiency for long battery life in portable devices. In these systems, peaks occur for a small amount of time, and most of the time the signal envelopes are below the peak power. Class A or AB are typically used in highly linear power amplifiers (PAs), however they have a poor efficiency due to the larger peak to average power ratio (PAPR) of the signal. The higher the data rate, the larger the PAPR is, which requires a large back off to maintain a good linearity. This results in much lower efficiency [10]. For possible application in portable devices, the efficiency should be greatly improved. On the other hand, as the technology scales down, lower breakdown voltages and more nonlinear behavior of transistors lead to an

inferior signal to distortion ratio (SDR) that limits the data rate in linear PAs. Therefore, both linearity and efficiency should be improved in modern communication systems.

Recent reported PAs can be roughly categorized into three different sections, 1) highly efficient, 2) highly linear, and 3) highly linear and efficient amplifiers. In [11]-[12] the efficiency of a class A PA is improved up to 10% by modifying the power supply based on the signal envelope at the price of linearity degradation. In [13], the efficiency of the PA at power back offs is improved to 30% by manual adaptation of the output matching network. In [14], a linearizer circuit has been used to increase the bias value of the input bipolar transistor at high input powers which compensates for the gain drop. In [15]-[16], envelope elimination and restoration method has been used to increase PAE with a reasonable linearity performance. Other linearization techniques such as cancelling gm3 (third order coefficient of non-linearity) employing Dohorty operation [17], or suppressing the input harmonics of a class AB PA [18] are also reported in the literature. In [19], a combination of class A and class B PAs has been used to improve both linearity and efficiency. In [20], a class AB/F PA has been proposed to work in two modes, one efficient mode (class F) and one linear mode (class AB) suitable for multiple systems on chip. In [21], it has been shown that the deep n well (DNW) of NMOS transistor lowers the harmonic distortion generated from the gate-source capacitance which improves the linearity of the PA by 7 dB. In [22], by an optimum transistor gate bias and second harmonic termination, the IM3 level is improved by 7 dB. In [23]-[25], the outputs of multiple PA stages are combined as

voltages in series by employing transformers. In this case, the efficiency of the PA can be improved at power back offs by turning off one or two stages.

This chapter presents a new reconfigurable matching network technique in a fully integrated class AB PA in 0.25 µm SiGe:C BiCMOS technology [26]-[27]. The PA delivers 23 dBm maximum output power with simultaneous efficiency and linearity improvement. Efficiency improvement is achieved by switching the biasing states of the transistors based on the input power level of the signal which is monitored by an envelope detector. The gain of the PA in transition remains constant by implementing a reconfigurable matching network for both high and low input signal levels. The linearity is greatly enhanced based on a feed forward cancellation technique. Therefore, the proposed PA can improve both PA efficiency and linearity in high data rate standards such as 4G LTE for handsets, and can be tuned to the desired frequency band.

At first the fundamentals of the proposed PA and different modes of operation is explained. Then later on the proposed linearization technique for high output powers and the circuit implementation is discussed in details. The proposed efficiency improvement technique and the theory behind the technique are extensively evaluated. The measurement results and the conclusion are summarized at the end.

II.2. System Implementation

In an OFDM system, a high data rate is achieved with multicarrier modulation in which the transmitted power may vary greatly. Therefore, it suffers from a large PAPR.

In a practical RF transmitter, PAPR determines the linear dynamic range requirement for the PA. A potentially large PAPR will result in the following disadvantages [28]:

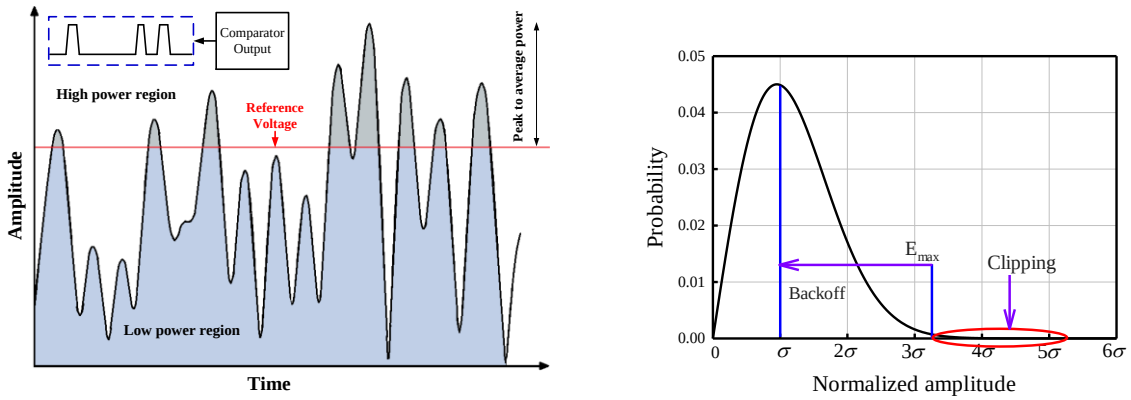
a) If the peak power exceeds the dynamic range of the PA, the transmitted signal will be clipped and gives rise to out of band radiation;

b) In OFDM systems, the biasing point of the designed PA should be optimized for the performance at P1dB, even though the efficiency is dominated by the efficiency of the average output power which is 8 to 10 dB lower.

Figure 2.1(a) shows a time domain OFDM signal that has a large PAPR and Figure 2.1(b) shows the probability of a peak power occurrence in an OFDM signal [29]. The graph shows that the probability of having a peak power is really small in these systems. Therefore as shown in Figure 2.1(a), the transmitter operation can be divided into two different regions, a low-power and a high-power region, in which decreasing the power consumption in lower input powers would result in a great efficiency improvement.

Figure 2.2 shows the system implementation of the proposed PA in which the efficiency is improved by switching between two different modes of operation based on the input power signal. The input signal is being monitored by an on-chip envelope detector. Based on the comparison between the input signal and a reference voltage, which is usually 6 dB below the peak input power, a decision signal is generated at the output of the comparator. The signaling determines if the amplifier is in high or low-power mode. For the high output power, the amplifier DC biasing is switched to higher values to deliver higher output powers with good linearity. In the low-power mode, the

biasing is decreased in order to enhance the efficiency. While the g_m of the amplifier is decreased due to lower DC biasing values, the output load (R_L) is increased through a switchable matching network to sustain a constant output voltage g_mR_L for both modes. Therefore, the PA maintains the linearity performance of a constant DC bias PA. A pre-amplifier is designed to derive the high input capacitance of the main amplifier. Also, the linearity of the main amplifier is greatly enhanced based on a feed-forward cancellation technique. An auxiliary path is added to the main amplifier to cancel out the non-linear terms of the main amplifier. Since the linearity of the main amplifier is sufficient enough for low input power signals, the auxiliary path can be switched off to further increase the PAE of the entire PA.



(a) (b)

Figure 2.1. (a) PA operation mode is divided into two regions for the transient OFDM signal based on the reference voltage, (b) envelope amplitude distribution for IEEE 802.11a OFDM signal.

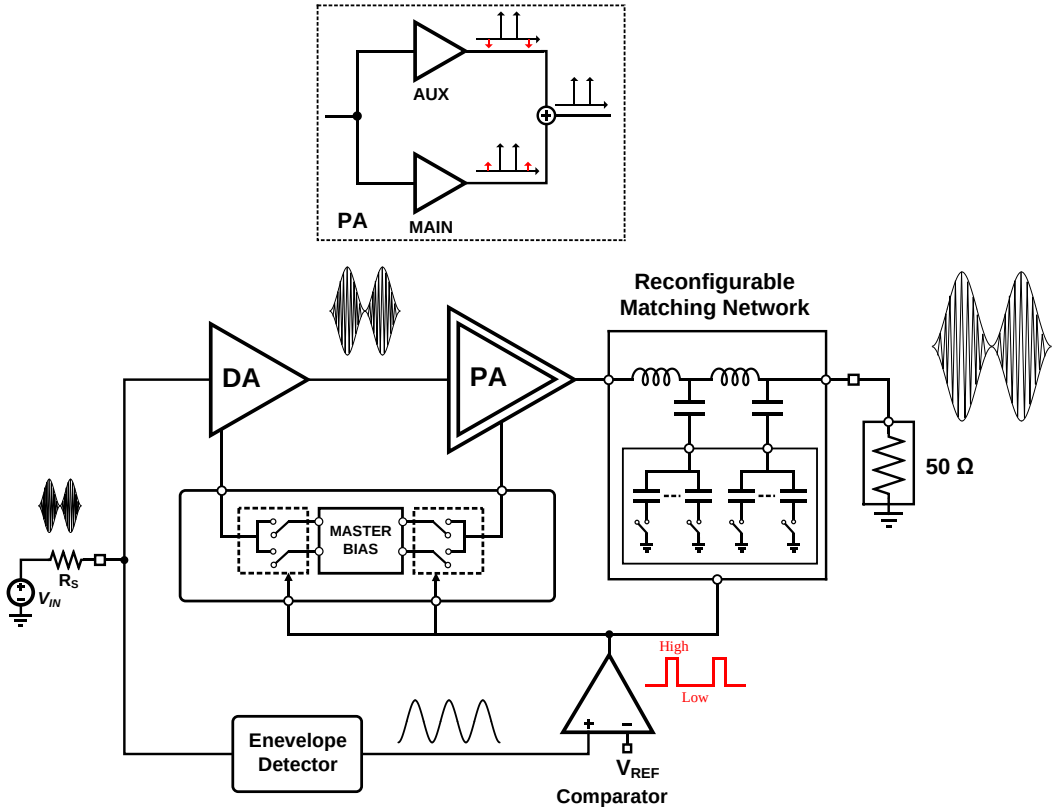


Figure 2.2. The system implementation of the proposed PA.

II.3. Linearity Improvement Technique

II.3.1. Fundamentals

Nonlinear current-voltage relationship in transistors is the major factor for nonlinear behavior of the RF blocks and as the technology scales down it is further degraded. The voltage-current relationship of a transistor can be written as follows:

$$i=g_{m1}v+g_{m2}v^2+g_{m3}v^3 \qquad (2\text{-}1)$$

where g_{mi} (i=1,2,3) is the i^{th} order term coefficient. In narrowband systems, g_{m2} causes some out of band second order inter-modulation terms which would be filtered through the output matching network. Input-referred third-order intercept point (IIP3) is one of the parameters for monitoring the linearity performance of the circuit and can be found as follows [9]:

$$A_{IIp3}=\sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \tag{2-2}$$

therefore, g_{m3} is the main source of nonlinearity in PAs, and the linearity can be greatly improved by cancelling out g_{m3}. The current of a bipolar transistor can be approximated as follows [30]:

$$i_{ce}=\alpha_1 v_{be}+\alpha_2 v_{be}^{\,2}+\alpha_3 v_{be}^{\,3} \tag{2-3}$$

$$i_{CE}=I_{S0}e^{\frac{V_{BEQ}+v_{be}}{\phi_t}}=I_Q e^{\frac{v_{be}}{\phi_t}} \tag{2-4}$$

$$\alpha_3=\frac{I_Q}{6\phi_t^{\,3}} \tag{2-5}$$

where V_{BEQ} is the base-emitter bias voltage, I_{S0} is the saturation current, and ϕ_t is the thermal voltage. As shown in (5), the third-order power coefficient for bipolar transistors is positive due to exponential relationship between collector current and the base-emitter voltage [30].

CMOS transistors biased in saturation have a negative third-order coefficient. The current of an NMOS transistor in strong inversion can be approximated as follows [30]:

$$i_{ds}=\beta_1 v_{gs}+\beta_2 v_{gs}^2+\beta_3 v_{gs}^3 \tag{2-6}$$

$$i_{DS}=\frac{x^2}{1+\theta x} \tag{2-7}$$

$$x=2\eta\phi_t \ln\left(1+e^{\frac{v_{GS}-v_{th}}{2\eta\phi_t}}\right) \tag{2-8}$$

$$\beta_3=-\frac{\theta K}{\left(1+\theta V_{eff}\right)^4} \tag{2-9}$$

where v_{th} is the threshold voltage, ϕ_t is the thermal voltage, θ is the normal field mobility degradation factor, η is the ratio of the exponential increase of the drain current with V_{gs} in sub-threshold region, $K = 0.5\mu_n C_{ox} {}^{W}/_{L}$ [21], Veff = Vgs0 – Vth, and Vgs0 is the DC gate-source bias voltage [31]. By adding a current with positive gm3 to the NMOS transistor, it can be linearized. The goal is to linearize the PA with minimum number of transistors since any increase in the number of the transistors would degrade the PAE. Therefore, the current in bipolar and NMOS transistors can be added at the output to cancel out the g_{m3} of the entire PA as follows:

$$\begin{aligned} i_O &= (\alpha_1+\beta_1)v_{in}+\left(\alpha_2+\beta_2\right)v_{in}^2+(\alpha_3+\beta_3)v_{in}^3 \\ &= g_{m1}v_{in}+g_{m2}v_{in}^2+g_{m3}v_{in}^3 \end{aligned} \tag{2-10}$$

The phase and the magnitude of the g_{m3} are a function of the DC biasing, and the size of the transistors. Figure 2.3 shows the simulation results for g_{m3} as a function of the DC biasing for both BJT and NMOS transistors for a particular size. As it is highlighted in the figure, for certain biasing voltages, α_3 is positive, while β_3 is negative, and the total gm3 can be cancelled out.

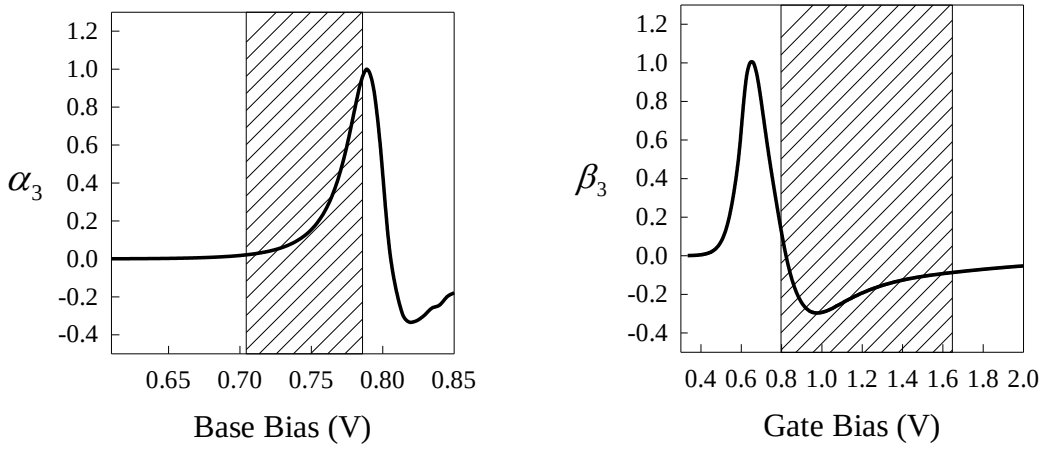


Figure 2.3. (a) Normalized α_3 coefficient versus base bias voltage of the bipolar transistor, (b) normalized β_3 coefficient versus gate bias voltage of the NMOS transistor.

II.3.2. Main Core PA

Figure 2.4(a) shows the schematic of the core PA. If the output load is connected to V_{DD} through an RF choke or an LC tank which doubles the output swing, the output power will be:

$$P = \frac{1}{2}\frac{V_{DD}^{\ 2}}{R_L} \tag{2-11}$$

The DC supply voltage used in the amplifier is 2.5 V. If 0.5V margin is considered for the saturation voltage in the transistors and the losses, the output peak-to-peak swing is 4 V. To achieve output power of 25 dBm, the required load (R_L) will be 10 Ohms.

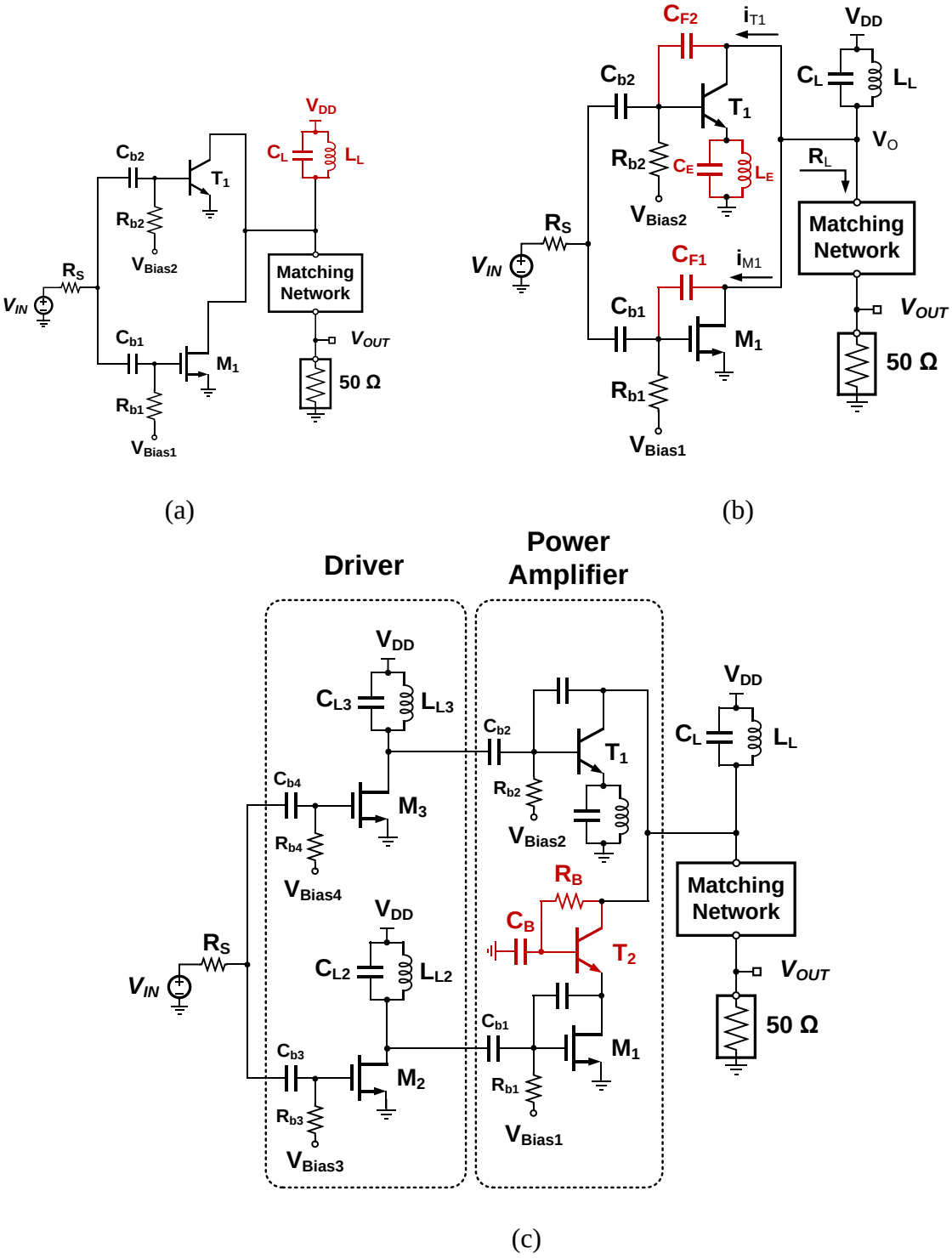


Figure 2.4. (a) The schematic of the core PA, (b) the core PA with 2nd harmonic rejection and IM_3 phase adjustment, (c) the Core PA with the pre-amplifier stage.

As shown in Figure 2.4(a), the signal is applied to both T_1 and M_1, and the output currents are combined. Since BJT is capable of providing a higher amount of current compared to its NMOS counterpart, T_1 is employed as the main amplifier. Although the third order coefficients (α_3 and β_3) are out of phase, the signals are in phase for both transistors and the output power would be combined similar to a parallel power combination topology [23]-[25].

In order to achieve a higher PAE, both transistors are biased in class AB region. T_1 works as a linear amplifier and has a large gm which provides most of the gain, while M_1 is providing a small g_m compared to T_1, leading to α_3 much larger than β_3. To be able to cancel out the third order coefficient terms (α_3 and β_3), transistor M_1 is intentionally forced to be mostly in non-linear region. Therefore, transistor M_1 linearizes the bipolar transistor T_1 while increasing the output power by providing in phase fundamental current component. DC biasing adjustment and sizing of the transistors are based on perfect cancellation of the third order coefficients at the peak input signal power. For high output power (25 dBm), the base of T_1 is biased at 765 mV while the gate of M_1 is biased at 1V, the size of the transistors are included in Table 2.1 and 2.2 The currents are added at the output and applied to the matching network. Instead of using an off-chip RF choke, a parallel LC network (C_L and L_L) has been employed at 2 GHz resonance frequency. L_L is designed to be 1nH while C_L is set to be 3 pF. The loss of the tank decreases the voltage swing which degrades the maximum output power to 24 dBm.

Table 2.1. The NMOS transistor parameters used in the core PA.

	Length	Width	No. of Stripes	No. of Parallel cells
NMOS Transistor	0.25µm	133µm	14	6

Table 2.2. The bipolar transistor parameters used in the core PA.

	Emitter Length	Emitter Width	No. of Emitters	No. of Repeated cells
BJT Transistor	35µm	0.4µm	3	3

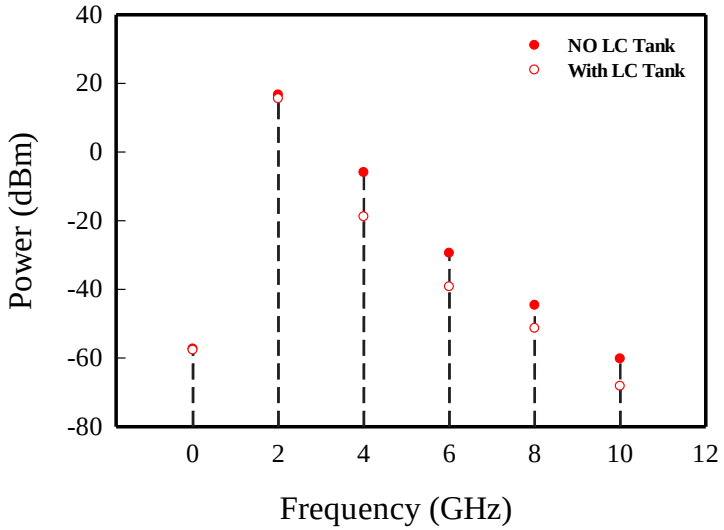


Figure 2.5. The 2nd and higher harmonic rejection of the output power while employing the LC tank in the emitter of the bipolar transistor.

II.3.3. Non-Linear Base Capacitance

Although the bipolar transistor has high power handling capabilities, it has a highly non-linear capacitance at the base junction [32]. This capacitor results in a large

second-order harmonic current and lowers the available output power to 16 dBm. To overcome this issue, a parallel LC network (C_E and L_E) in Figure 2.4(b) is employed in the emitter of T_1, resonating at the second harmonic of the fundamental tone. This LC tank acts as a source degeneration circuit and decreases the current at 4 GHz. L_E should be small since the inductor will degenerate the fundamental tone, which will result in a lower output power. L_E is chosen to be 140 pH while C_E is 8 pF including the parasitic capacitance in the emitter of T_1. The circuit is simulated with and without the LC tank and as shown in Figure 2.5, the LC tank attenuates the higher harmonics and especially the second harmonic by 19 dB. Since L_E is small, the Q of the inductor is larger than 9 at 2 GHz, therefore 0.8 dB gain drop is mostly because of the impedance of the tank at the fundamental tone rather than the inductor loss. As shown in [32], second harmonic degradation can improve the linearity of the PA by decreasing IM_3 and IM_5 levels.

II.3.4. IMD Phase Adjustment

The nonlinear base-emitter capacitance of T_1 at high output powers will change the phase of both α_3 and β_3. This will degrade the feed-forward cancellation technique. The phase of α_3 and β_3 can be adjusted by adding feedback capacitors, C_{F1} (300 fF) and C_{F2} (150 fF), in parallel with the gate-drain and base-collector capacitors, respectively (Figure 2.4(b)). Due to non-linear base capacitance in T_1, the input base voltage, the currents i_{T1} and i_{M1} are given by (Figure 2.4(b)):

$$V_{b\text{-}T_1}=\sigma_1 v_{in}+\sigma_2 v_{in}^{\,2}+\sigma_3 v_{in}^{\,3} \tag{2-12}$$

$$i_{T1}=(v_O-\sigma_1 v_{in}-\sigma_2 v_{in}^2-\sigma_3 v_{in}^3)C_{F2}s+\alpha_1 v_{in}+\alpha_2 v_{in}^2+\alpha_3 v_{in}^3 \quad (2\text{-}13)$$

$$i_{M1}=(v_O-v_{in})C_{F1}s+\beta_1 v_{in}+\beta_2 v_{in}^2+\beta_3 v_{in}^3 \quad (2\text{-}14)$$

$$v_O \cong -\{(\alpha_1+\beta_1)\times R_L\}v_{in} \quad (2\text{-}15)$$

$$A_{IIP3}=\sqrt{\frac{3}{4}\left|\frac{j\omega(-(\alpha_1+\beta_1)\times R_L\times(C_{F1}+C_{F1})-C_{F1}-\sigma_1 C_{F2})+\alpha_1+\beta_1}{-j\omega C_{F2}\sigma_3+\alpha_3+\beta_3}\right|} \quad (2\text{-}16)$$

Therefore, the phase difference between α_3 and β_3 can be compensated through the feedback capacitors and the IM_3 of the main amplifier would be cancelled out. As can be seen in (16), the fundamental currents are no longer in phase which will cause a small drop at the output power.

II.3.5. Self-Biased Cascode Unit

To increase the output power, the power supply should be as large as possible (2.5V in this technology). The collector and the drain of the BJT and NMOS transistors are connected together and share the same DC voltage. Because of the low gate-drain breakdown voltage of the NMOS transistor at this technology (1.7V), the power supply cannot be connected directly to the drain. To overcome this issue, a self-biased cascode structure [33] is employed to divide the output swing between the two transistors. As shown in Figure 2.4(c), transistor T_2 is added to the circuit as a cascode device. The values of R_B and C_B are set not to affect the phase of the current in transistor M_1. The average current consumption of the main amplifier stage is 105 mA.

II.3.6. Pre-Amplifier Stage

Large input transistors (M_1 and T_1) result in a large input capacitance in the order of 1-2 pF. To drive the main transistors, a pre-amplifier stage is employed. The transistors in this stage are biased in class A region to provide sufficient linearity. As shown in Figure 2.4(c), the pre-amplifier stage is realized using NMOS transistors to make the input capacitance smaller. For further improving the efficiency and also preventing the NMOS transistors from breakdown, the supply voltage for this stage is lowered down to 1.7 V. L_{L1} (1.6 nH) and LL2 (2 nH) are employed to tune out with the input parasitic capacitance of the main amplifier stage at 2 GHz. Resistors R_{L1} and R_{L2} are added to eliminate large peaking and potential oscillation. The current consumption in this stage is around 38 mA, which results in a small efficiency degradation.

II.3.7. Gain of the PA

The total gain of the system is the sum of the two stage gains which can be written as follows:

$$Gain = \left(g_{m_{M1}} + g_{m_{T1}}\right) R_L \times \left[g_{m_{M2}} \left(Q_{L1}{}^2 R_{S_{L1}} /\!/ R_{L1}\right) + g_{m_{M3}} \left(Q_{L2}{}^2 R_{S_{L2}} /\!/ R_{L2}\right)\right] \qquad (2\text{-}17)$$

in which g_m is the trans-conductance of the transistors, Q_{L1} and Q_{L2} are the quality factor of the inductors L_{L_1} and L_{L_2} at 2 GHz, respectively. $R_{S_{L1}}$ and $R_{S_{L2}}$ are the series losses associated with the inductors L_{L_1} and L_{L_2}, and R_L is the impedance seen form the matching network. Considering R_L to be 8 ohms, the total gain is calculated as follows:

$$Gain=[(290mS+100mS)\times 8]\times[(40mS\times 21)+(40mS\times 23)]\cong 5.11\ (14dB) \quad (2\text{-}18)$$

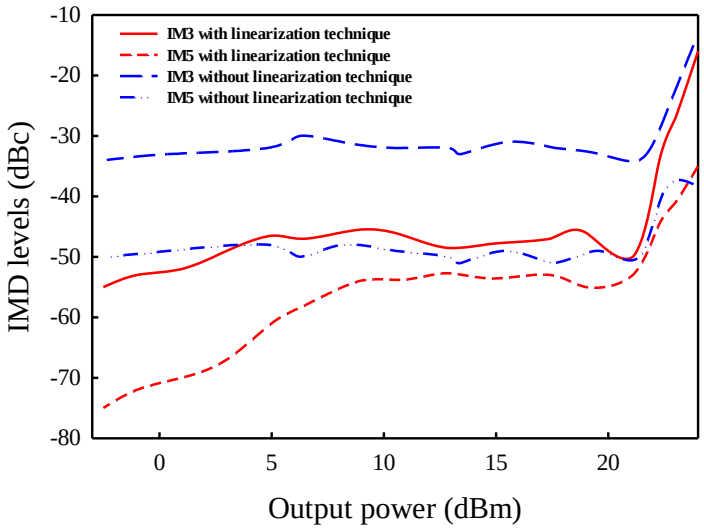


Figure 2.6. IMD levels at 20 dBm average output power with and without linearization technique.

The gain of the pre-amplifier is only 4 dB to minimize nonlinearity degradation by this stage.

II.3.8. Two-Tone Linearity Test

In order to simulate the effect of linearity improvement technique, two tones are applied to the PA, and the output IM_3 and IM_5 are monitored for different output powers. The DC biasing values are adjusted to get the best IM_3 cancellation at the highest output power. The test has been performed for 1MHz frequency spacing between the two tones, with and without the feed-forward cancellation technique versus the output power. The

simulation results are shown in Figure 2.6. This technique improves the IM_3 levels by 10-20 dB, and as the frequency spacing becomes smaller, a better IM_3 cancellation is achieved. In this approach, the IM_5 levels are also improved especially for output powers below 5 dBm.

II.3.9. Effect of Temperature, Bias Value and Supply Voltage Variations

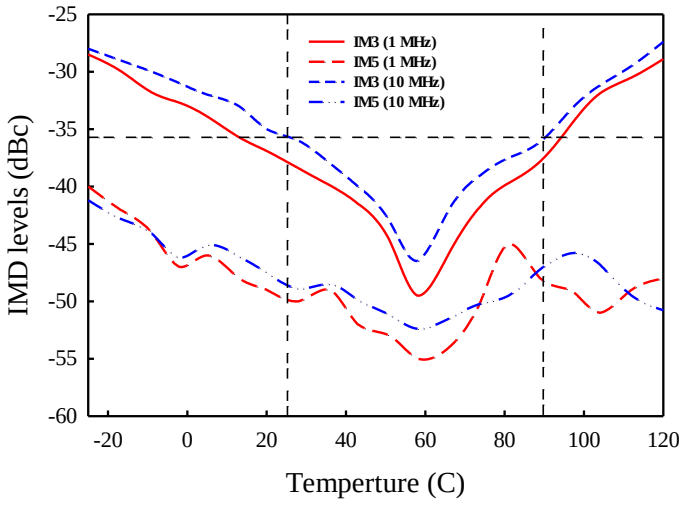
In 0.25 µm BiCMOS NXP process, the substrate thermal resistance is 125 K/W. Based on the dissipated power in the power amplifier, the temperature of the die can be calculated using the following equation [34]:

$$T_{die}=T_{ambient}+R_{Th\text{-}substrate}\times P_{dissipated} \tag{2-19}$$

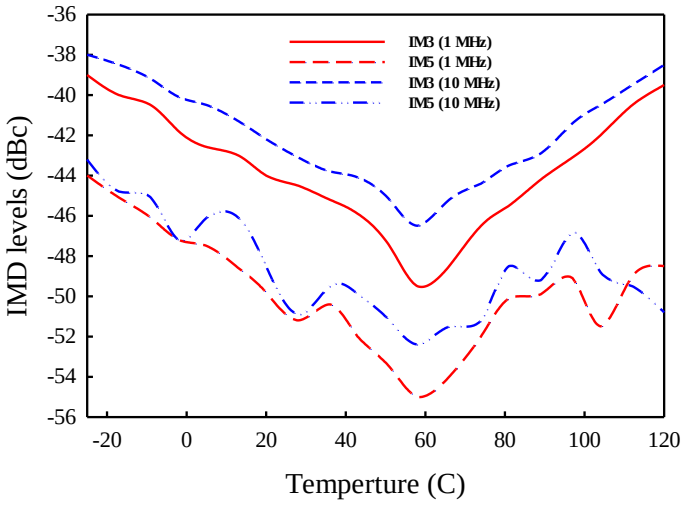
$$T_{die}=303K+125\frac{K}{W}\times 250mW=333K=60\ ^{\circ}C \tag{2-20}$$

Therefore the nominal temperature of the die is 60 ºC, and all the designs, and simulations have been performed in the same temperature. Since the threshold voltage of NMOS transistors and base-emitter on-voltage of bipolar transistor are temperature dependent, a change in the temperature can degrade the IM_3 cancellation. As a result the IM_3 level increases. Figure 2.7(a) shows the simulated IM_3 and IM_5 levels at the output of the PA for high power mode, versus the temperature variations. The two-tone test has been performed for the average output power of 20 dBm, and two different frequency spaces (1 and 10 MHz). As the temperature increases, by keeping the same biasing values, the transistors M_1, and T_1 move toward saturation region causing the output signal to show a more nonlinear behavior. On the other hand, as the temperature

decreases the transistors M_1, and T_1 move toward triode and linear region, respectively, and the performance of the IM_3 cancelation technique degrades.



(a)



(b)

Figure 2.7. (a) The effect of temperature variations on IM_3 cancellation technique (20 dBm average output power). (b) The effect of temperature variations on IM_3 cancellation technique after readjusting the biasing values of transistors T_1 and M_1.

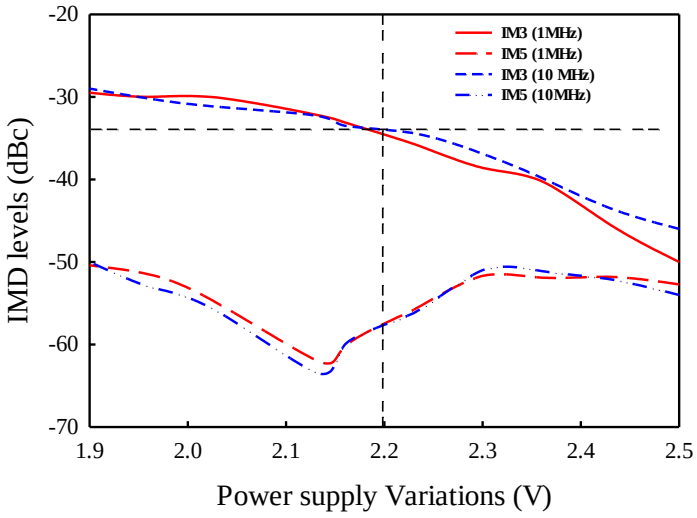
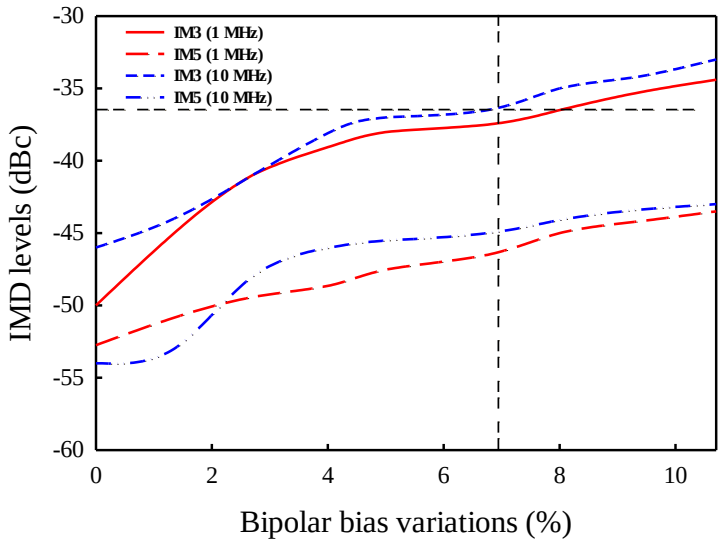
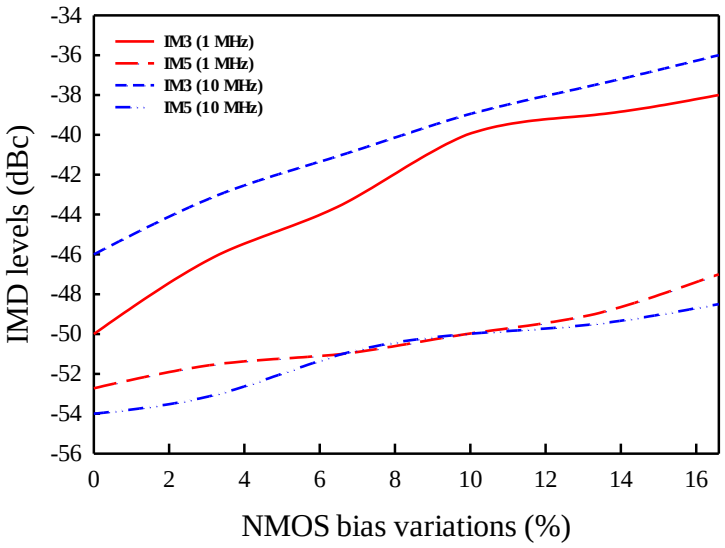


Figure 2.8. The effect of power supply variations on IM_3 cancellation technique (20 dBm average output power).

Automatic calibration can be done when temperature changes significantly. By readjusting the biasing values of M_1 and T_1 to be far from saturation (decreasing the base and the gate DC values of T_1 and M_1 for higher temperatures and increasing them for lower temperatures), the effect of temperature variations can be compensated, and the output power can be linearized as shown in Figure 2.7(b). IM_3 level below -36 dBc is considered a reasonable value for 20 dBm output power, (it results in an OIP3 of 38 dBm). Therefore, this technique can tolerate 23º -89º C temperature variations. By readjusting the bias values, the linearization technique covers the temperature range of -25º to 120º C.



(a)



(b)

Figure 2.9. The effect of bias variations on IM_3 cancellation technique, (a) bipolar transistor, (b) NMOS transistor.

The IM_3 cancellation technique is not strongly dependent on the power supply as far as the variations in the power supply do not cause any clipping at the output signal. Figure 2.8 shows the simulated IM_3 levels for different power supply values at different frequency spaces (1 and 10 MHz) for the two-tone test (the average output power : 20 dBm). Since there is a large voltage swing at the output, lowering down the power supply below 2.2V, will cause clipping at the output, and degrades the linearity of the PA.

The robustness of the linearization approach over transistor DC bias value variations is also tested with the two-tone test. The DC biasing of NMOS transistor M_1, and bipolar transistor T_1 are swept and the effect of the variations are shown on the IM_3 and IM_5 levels in dBc in Figure 2.9. Since the collector current of bipolar transistor is an exponential function of the input base voltage, it is more sensitive to base DC biasing variations compared to its NMOS counterpart. For a reference IM_3 level of -36 dBc, the linearization technique can tolerate 16% biasing variations for the NMOS transistor, and 7% biasing variations for the bipolar counterpart. Based on the linearity requirement in the system, the linearization technique can be readjusted to achieve a better IM_3 cancellation for temperature and voltage bias variations.

II.3.10. The Ground Bond-Wires

Although the ground bond-wires are connected to the package plate, and the inductance is smaller than the pin bond-wires (close to 500 pH), it decreases the gain of the amplifier, and changes the resonance frequency of the LC tank used in the emitter of

T_1. These effects are considered in the design of the circuit. Also, one of the main reasons for oscillation in PAs is the same ground for the multiple stages (Figure 2.10). To overcome this problem, the grounds for the two stages are isolated in the chip layout, and have been connected through different bond-wires to the package plate. Also multiple pads are assigned for grounds to minimize the bond wire inductance.

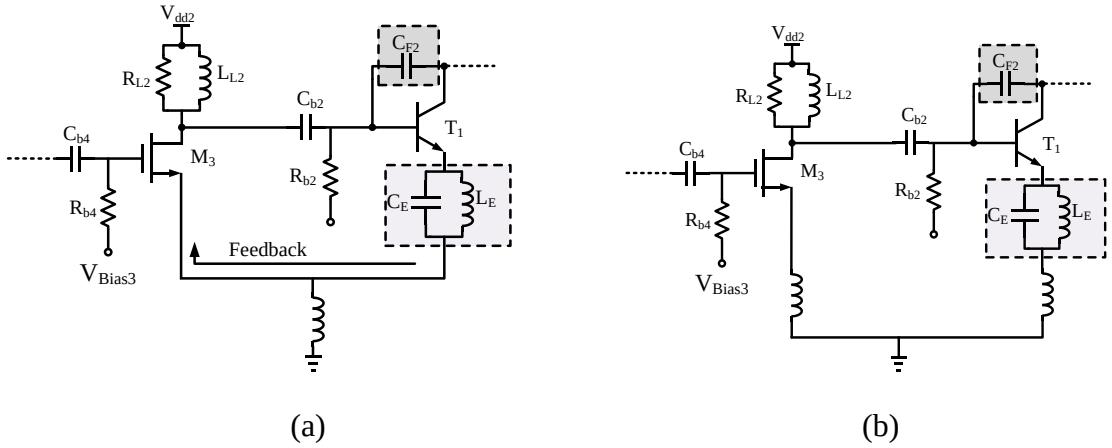


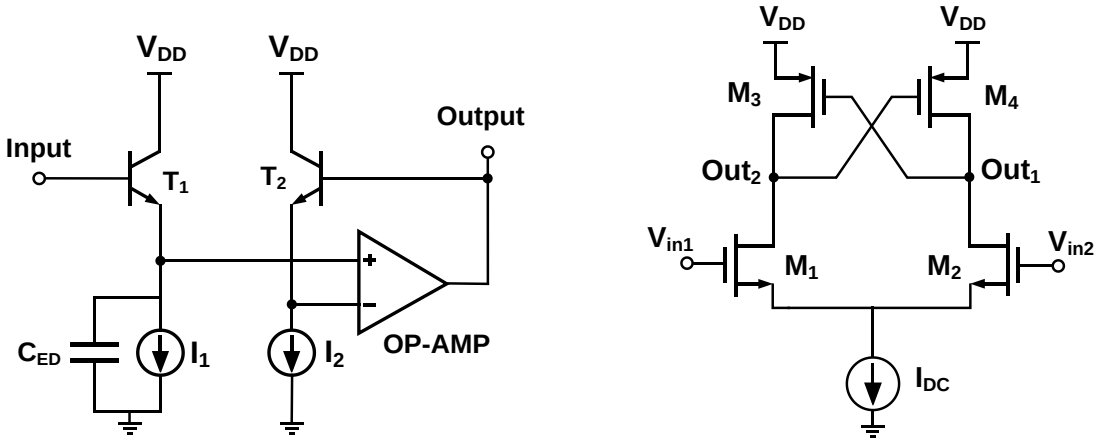
Figure 2.10. (a) Same chip ground for both stages in the PA causing a feedback loop, (b) different chip grounds for the two stages of the PA.

II.4. Efficiency Improvement Technique

II.4.1. On-Chip Envelope Detector and Comparator

As mentioned before, in OFDM systems, due to large PAPR, the signal envelope is mostly below the peak, resulting in a poor efficiency for constant bias class A PAs. The efficiency of the PA can be improved by adjusting the transistor DC current based

on the input signal. Suppose the input envelope is equally divided into N different levels which require N-step biasing schemes, and different output loads. If the difference between each two levels is ΔV, $\Delta V \rightarrow 0$ results in an infinite number of levels with infinite biasing schemes and output loads. This assumption is equivalent to a continuous biasing scheme in which the gate bias is adjusted continuously based on the input envelope. In this case, the PA power consumption is a linear function of the input signal, and therefore the PA efficiency will greatly improve. On the other hand, since this approach requires continuous tuning of the matching network, the linearity of the matching network will be very difficult to maintain using analog tuning, since gain matching between all the levels should be preserved over a wide analog tuning rang. Therefore, the overall linearity will be degraded drastically comparing to the two-step biasing scheme based on the envelope detector.



(a) (b)

Figure 2. 11. (a) The schematic of the envelope detector employed in the peak detector, (b) the schematic of the comparator for decision signal generation.

An on-chip envelope detector shown in Figure 2. 11(a) monitors the input signal level. Transistor T_1 acts like a diode, and the OP-AMP forces the base of transistor T_2 to follow the emitter of T_1. T_2 and I_2 are the replicas of T_1 and I_1 to cancel out the distortion through the OP-AMP [15]. The total power consumption of the envelope detector is 500 uA. The output of the envelope detector is compared to a reference voltage, V_{ref} (6 dB below the peak input signal) by a comparator shown in Figure 2. 11(b). This comparator consumes 400 uA current. The comparator output generates a decision signal which determines the appropriate biasing for the transistors by turning on and off the required switches. Figure 2.12(a) shows a 4QAM OFDM signal in the time domain generated using MATLAB[†]. The simulated output of the envelope detector and the comparator are shown in Figure 2.12(b) and (c), respectively.

II.4.2. Reconfigurable Output Matching Network

Switching to a smaller DC current will reduce the gm of the transistors, and will cause a drop in the gain. This will cause a discontinuity in the output waveform, and severely degrades the linearity. To keep the gain of the system constant, the output load should be increased to compensate for the gm drop. In the high-power mode, the 50 ohms load is converted to an 8 ohms load through an on-chip impedance transformer to maintain a gain of 14dB as shown in (18). To reduce the power consumption in the low-power mode, the DC voltage biasing is decreased for both the pre and the main

[†] http://www.ece.gatech.edu/research/labs/sarl/tutorials/OFDM/Tutorial_web.pdf

amplifier. The current consumption of the main amplifier stage is decreased to 52 mA, and the pre-amplifier to 20 mA. The gain in the low-power mode is as follows:

$$Gain=[(130mS+70mS)\times 8]\times[(25mS\times 21)+(25mS\times 23)]\cong 1.76 \ \ (5dB) \qquad (2\text{-}21)$$

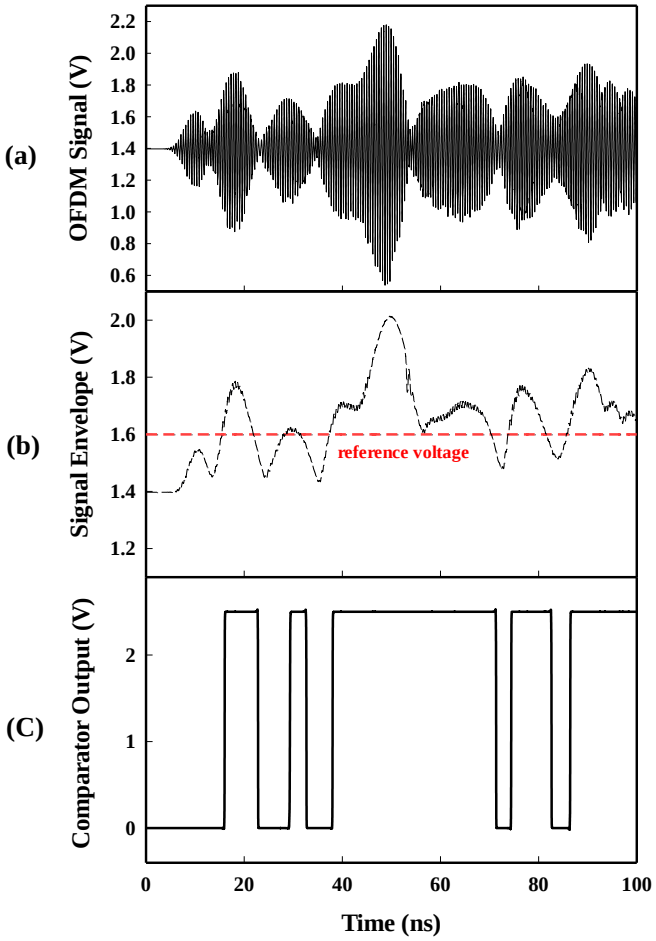


Figure 2.12. (a) 4QAM OFDM time domain signal at the input of the envelope detector, (b) the output signal of the envelope detector, (c) the output of the comparator based on the reference voltage.

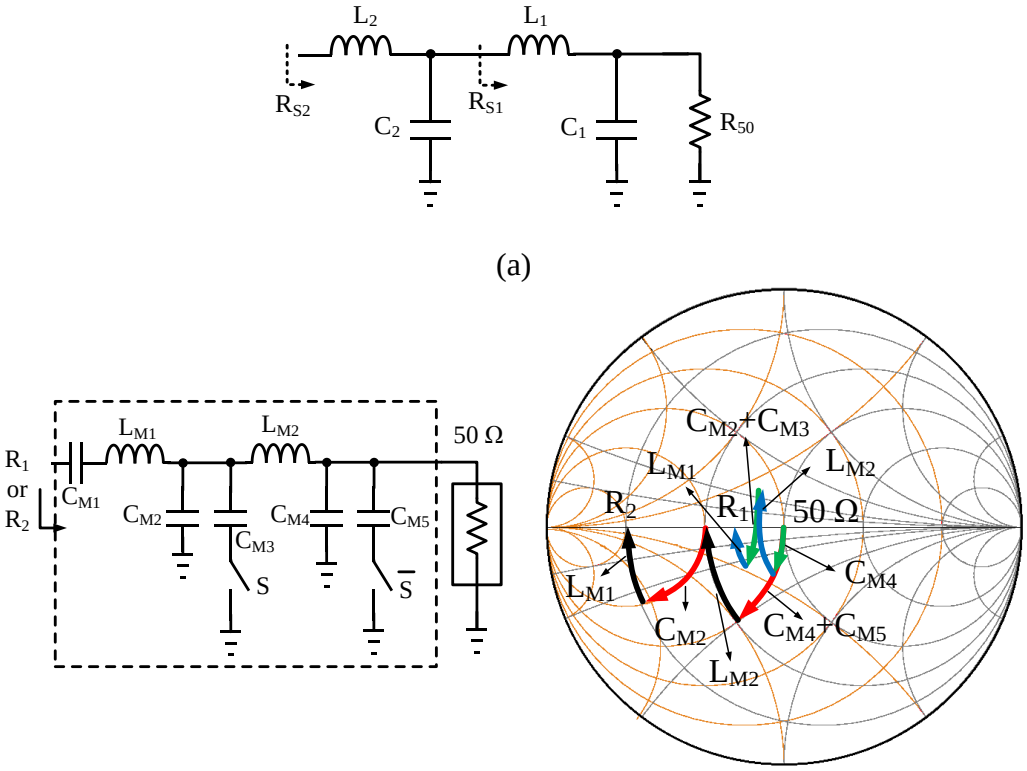


Figure 2.13. (a) The low-pass L-Match resistive transformer, (b) the schematic of the output matching network, (c) the smith chart of the proposed matching network for the two modes.

In order to compensate for this gain drop, the impedance seen from the matching network (R_L) should be increased to 25 Ohms. Therefore, matching network should be able to transform R_{50}=50 ohms to R_1=8 ohms in the high-power mode and R_{50}=50 ohms to R_2=25 ohms in the low-power mode based on the signal generated at the output of the comparator. Considering the low pass L-match network shown in Figure 2.13(a), the

input resistance, R_{S2}, can be calculated as follows ($Q_{C1} = \omega_0 C_1 R_{50}$, $Q_{L1} = \frac{L_1 \omega_0}{R_{L_1}}$, $Q_{L2} = \frac{L_2 \omega_0}{R_{L_2}}$ and $\omega_0 = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$):

$$R_{S1}=R_{L_1}+\frac{R_{50}}{Q_{C1}^{\ 2}}=\frac{L_1\omega_0}{Q_{L1}}+\frac{R_{50}}{(\omega_0 C_1 R_{50})^2} \tag{2-22}$$

$$Q_{C2}=\omega_0 C_2 R_{S1}=\omega_0 C_2\left(\frac{L_1\omega_0}{Q_{L1}}+\frac{R_{50}}{(\omega_0 C_1 R_{50})^2}\right) \tag{2-23}$$

$$R_{S2}=R_{L_2}+\frac{R_{S1}}{Q_{C2}^{\ 2}}=\frac{L_2\omega_0}{Q_{L2}}+\frac{R_{S1}}{\left(\omega_0 C_2\left(\frac{L_1\omega_0}{Q_{L1}}+\frac{R_{50}}{(\omega_0 C_1 R_{50})^2}\right)\right)^2} \tag{2-24}$$

$$R_{S2}=\frac{L_2\omega_0}{Q_{L2}}+R_{50}\left(\frac{C_1}{C_2}\right)^2\frac{1}{\frac{R_{50}}{R_{L2}Q_{L1}Q_{L2}}\left(\frac{C_1}{C_2}\right)+1} \tag{2-25}$$

$$R_{S2}=R_{L_2}+R_{50}n^2\frac{1}{\frac{R_{50}}{R_{L2}Q_{L1}Q_{L2}}n+1} \tag{2-26}$$

where n is the ratio between the two capacitors ($\frac{C_1}{C_2}$) and R_{L_k} is the resistive loss of the inductor k (k=1,2), Q_{L1}, Q_{L2}, Q_{C1} and Q_{C2} are the quality factor of inductors L_1, L_2, and capacitors C_1 and C_2, respectively . If the inductors are assumed to be loss less, then the input resistance would be $R_{50}n^2$. Therefore by changing the ratio of the capacitors the input resistance can be changed. In practical cases, because of the parasitic of inductors and MIM capacitors, the impedance transformation from 50Ω to 8Ω or 25Ω is really difficult to be achieved just by switching one of the capacitors. The reconfigurable matching network is realized as shown in Figure 2.13(b). Both CM_3 and CM_5 are

switching for accurate resistive transformation in the two modes. Due to the large current flow through the matching network, switches are avoided in series configuration. The actual impedance transfer diagram is shown in Figure 2.13(c). The inductors in series will cause a 0.5 dBm drop in the output power. The capacitor and inductor values are shown in Table 2.3 The matching network is designed to provide R_1=8-10Ω or R_2=23-25Ω output load for the high and the low input powers, respectively, by digitally calibrating 5 bit switch capacitors CM2 and CM4 to achieve the highest output power. The designed output load range can also be compensated for any gain mismatch between the two modes of the PA, and maintain a good linearity in PVT variations. Signal S is high for input signal envelopes larger than the reference voltage, while $\bar{S}$ is high for envelopes smaller than the reference voltage. Capacitor C_{M1} is used as a DC block.

Table 2.3. The calculated values for the elements employed in the matching network.

C_{M1}	L_{M1}	C_{M2}	C_{M3}	L_{M2}	C_{M4}	C_{M5}
7 pF	1.36 nH	0.75 pF	1.35 pF	1.91 nH	0.75 pF	1.55F

II.4.3. Circuit-Level Representation of the Entire PA

In the low-power mode, the larger load resistance, R_2, can be affected by the transistors small output impedance. Due to large base-collector and gate-drain capacitances added (C_{F1} and C_{F2}) for phase equalization at the high-power mode; the

output impedance of the main transistors is in the order of 50 ohms at 2 GHz, which will shunt the output current in the low-power mode. Therefore, more DC current needs to be provided by the transistors T_1 and M_1 to provide the same output power, which degrades the efficiency improvement. By adding a switch in the path of both C_{F1} and C_{F2} and turning both switches 'OFF' in the low power mode, the output impedance of the main transistors are increased; the associated switches (SW_{CF1} and SW_{CF2}) are implemented by transmission gates. The final PA schematic is shown in Figure 2.14 where both linearity and efficiency improvement techniques are shown. The envelope of the signal in OFDM systems varies with a low frequency in the order of 1-10 MHz, the AC coupling capacitors and resistor, C_{bi} and R_{bi} (i=1,2,3,4) for the biasing of each transistor will form a low pass filter for the decision signal generated by the comparator. For proper system operation, the cut off frequency of each low pass filter should be larger than the frequency variation of the envelope. There is a transient at the input of each stage due to the change of the DC bias values, when the PA operation mode switches. At the input of the pre-amplifier stage, the bias voltage experiences a smooth first order transition. For the main amplifier stage, there is some ringing due to the nature of the second order system (due to the inductors in the load of the pre-amplifier stage). The added parallel resistors (R_{L2} and R_{L1} in Figure 2.14) lower the quality factor of the second order transition, avoiding any large ringing at the base and the gate of T_1 and M_1, respectively. R_{b3} and R_{b4} are set to be 100 Ohms to provide 50 ohms matching at the input.

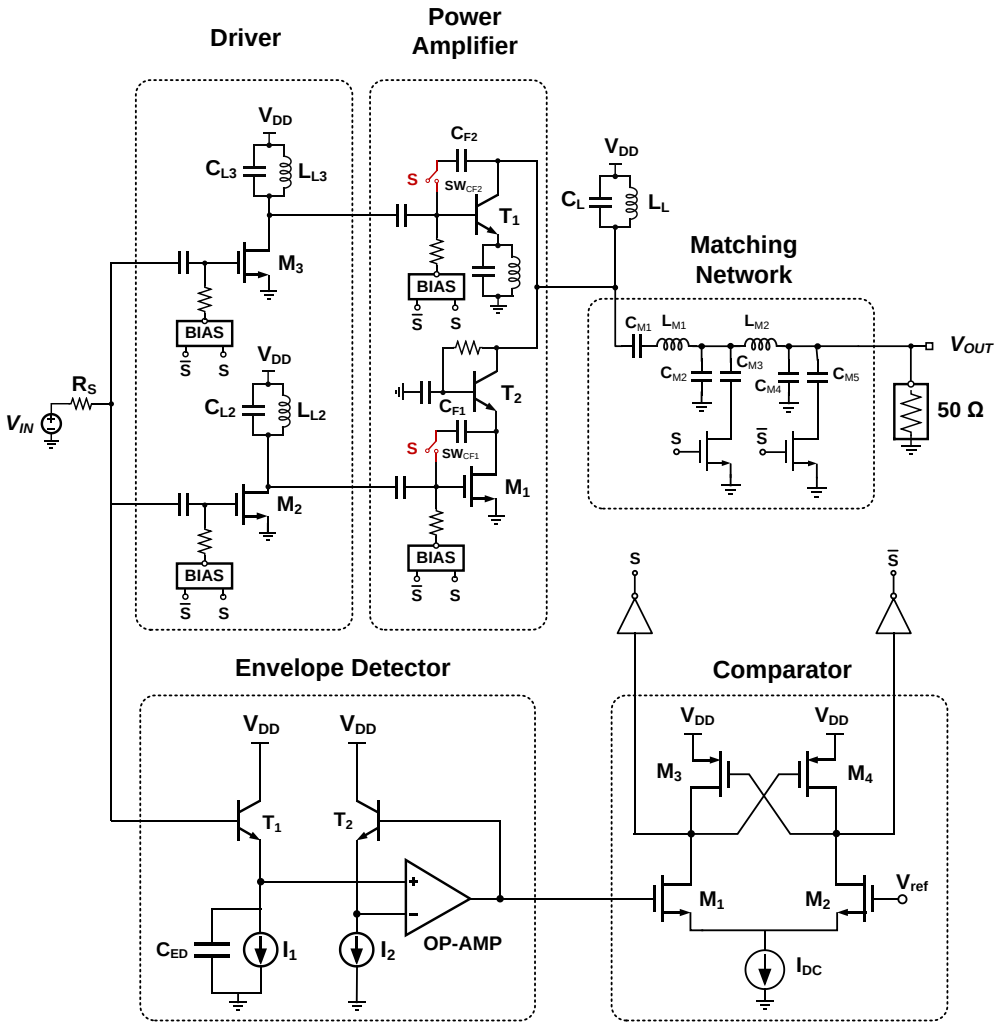


Figure 2.14. The circuit level schematic of the entire PA.

II.4.4. Effect of Switch Non-Idealities on the Matching Network

The effect of switch non-idealities in the reconfigurable matching network is considered in high and low-power modes separately. In high-power mode, switch SW_1 is ON, and SW_2 is OFF, and the output impedance of the matching network (R_{S2} in Figure

2.15) can be written as follows: (R_{SWk} and C_{SWk} (k=1,2) are the switch on-resistance and the off-state parasitic capacitance) ($Q_{C_{M4}+C_{SW2}} = \omega_0(C_{M4} + C_{SW2})R_{50}$, $Q_{LM1} = \frac{L_{M1}\omega_0}{R_{L_{M1}}}$, $Q_{LM2} = \frac{L_{M2}\omega_0}{R_{LM_2}}$, $C_{M5} \gg C_{SW2}$,):

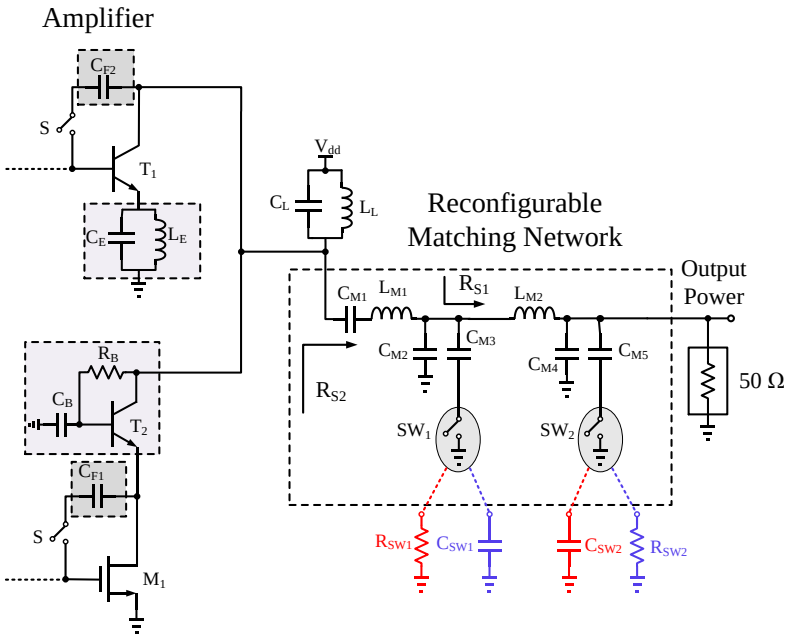


Figure 2.15. The reconfigurable matching network to study the effect of switch non-idealities in both low-power and high-power modes.

$$R_{S1} = \frac{L_{M2}\omega_0}{Q_{LM2}} + \frac{R_{50}}{(\omega_0(C_{M4}+C_{SW2})R_{50})^2} \tag{2-27}$$

$$Q_{CM2+CM3} = \omega_0(C_{M2}+C_{M3})R_{S1}$$
$$= \omega_0(C_{M2}+C_{M3})\left(\frac{L_{M2}\omega_0}{Q_{LM2}} + \frac{R_{50}}{(\omega_0(C_{M4}+C_{SW2})R_{50})^2}\right) \tag{2-28}$$

$$R_{S2}=\frac{L_{M1}\omega_0}{Q_{LM1}}+\frac{1}{\omega_0^2(C_{M2}+C_{M3})^2\left(\frac{L_{M2}\omega_0}{Q_{LM2}}+\frac{R_{50}}{(\omega_0(C_{M4}+C_{SW2})R_{50})^2}\right)}+\left(\frac{C_{M3}}{C_{M2}+C_{M3}}\right)^2 R_{SW1} \quad (2\text{-}29)$$

As shown in (29), the effect of the OFF-state parasitic capacitance can be compensated (C_{SW2}) by decreasing CM_4. The switch ON resistance (R_{SW1}) appears at the output load (R_{S2}) with a factor of $\left(\frac{C_{M3}}{C_{M2}+C_{M3}}\right)^2$. Since the output load should be small (10Ω) in the high power mode, this resistance should be as small as possible not to affect R_{S2}. Therefore, R_{SW1} need to be included in the design of the matching network.

In the low-power mode, switch SW_2 is ON, and SW_1 is OFF. For this case, the switch ON resistance (R_{SW2}) in series with the CM_5 capacitor, is translated into a resistance in parallel to the 50 ohms antenna impedance. Therefore, the output load in this mode can be calculated as follows (R'_{50} is the new antenna impedance):

($Q_{C_{M4}+C_{M5}}=\omega_0(C_{M4}+C_{M5})R_{50}$, $Q_{LM1}=\frac{L_{M1}\omega_0}{R_{L_{M1}}}$, $Q_{LM2}=\frac{L_{M2}\omega_0}{R_{LM_2}}$, $C_{M3}\gg C_{SW1}$):

$$R'_{50}=R_{50}/\!/\frac{1}{\omega_0^2 C_{M5}^2 R_{SW2}} \quad (2\text{-}30)$$

$$R_{S2}=\frac{L_{M2}\omega_0}{Q_{LM2}}+\frac{1}{\omega_0^2(C_{M2}+C_{SW1})^2\left(\frac{L_{M1}\omega_0}{Q_{LM1}}+\frac{R'_{50}}{\left(\omega_0(C_{M4}+C_{M5})R'_{50}\right)^2}\right)} \quad (2\text{-}31)$$

$$R_{S2}=\frac{L_{M2}\omega_0}{Q_{LM2}}+R'_{50}\left(\frac{C_{M4}+C_{M5}}{C_{M2}+C_{SW1}}\right)^2\frac{1}{\frac{R'_{50}}{R_{LM_2}Q_{LM1}Q_{LM2}}\left(\frac{C_{M4}+C_{M5}}{C_{M2}+C_{SW1}}\right)+1} \quad (2\text{-}32)$$

As shown in (32), the output load impedance is not too sensitive to the effect of R_{SW2} in the low power mode. The effect of C_{SW1}, can be compensated by decreasing capacitor C_{M2}. Table 2.4 shows the characteristics of the switches SW_1 and SW_2 in the matching network in Figure 2.15. The effect of parasitic capacitance has been absorbed in C_{M2} and C_{M4} capacitors. The switch on resistance will also affect the output power level, and this loss will degrade the output power by 0.3 dB. Therefore, the total loss of the reconfigurable matching network increases to 1.5 dB. The two-tone test simulation (1 MHz frequency spacing) has been performed to investigate the effect of the switch non-idealities on the PA performance. The IM_3 level degrades by less than 0.5 dB for 20 dBm average output power, by adding the switches to the reconfigurable matching network.

Table 2.4. The characteristic of the switches SW_1 and SW_2 in the matching network of **Figure 2.14**.

SW_1		**SW_2**	
R_{ON}	C_{OFF}	R_{ON}	C_{OFF}
1.7 Ω	730 fF	3.2 Ω	280

II.4.5. S-Parameter Evaluation of the PA

The input port of the PA is matched to 50 ohms through the biasing resistors, R_{b3} and R_{b4} in Figure 2.14. S-parameter simulations have been performed (PSS and PSP analysis in Cadence Spectre) to simulate the frequency response of the PA over the

desired band. Figure 2.16 shows the input return loss versus frequency. The input matching shows a narrow-band response due to the feedback from the LC tank load of the pre-amplifier stage through the gate-drain parasitic capacitance.

The output return loss depends on the PA operation mode. To determine the output return loss, the output impedance of the PA without the matching network should be calculated for both modes of operation. As shown in Figure 2.17, this impedance (R_{OPA}) is translated into the impedance of R_{out} through the matching network. If the effect of the capacitor loss compared to inductor loss is neglected, the output return loss is then calculated as follows:

$$R_P = Q_{LM1}^{\,2} R_{OPA} \tag{2-33}$$

$$Q_{L1} = \frac{L_{M1}\omega_0}{R_{OPA}} \tag{2-34}$$

$$R_{out} = Q_{LM2}^{\,2} R_P \tag{2-35}$$

$$Q_{L2} = \frac{L_{M2}\omega_0}{R_P} \tag{2-36}$$

$$R_{out} = \left(\frac{L_{M2}}{L_{M1}}\right)^2 R_{OPA} \tag{2-37}$$

For high power mode, R_{OPA}= 25 ohms. Because of the matching network:

$$R_{out} = \left(\frac{1.91nH}{1.36nH}\right)^2 25 = 49.3\ \Omega \tag{2-38}$$

$$S_{22} = 20 \times \log\left(\frac{50\text{-}49.3}{50+49.3}\right) = \text{-}39\ dB \tag{2-39}$$

For low power mode R_{OPA}= 45 ohms. Because of the matching network:

$$R_{out}=\left(\frac{1.91nH}{1.36nH}\right)^2 45=88.7\ \Omega \tag{2-40}$$

$$S_{22}=20\times log\left(\frac{88.7-50}{50+88.7}\right)=-11.7\ dB \tag{2-41}$$

Therefore, the output return loss is really small for high output power mode, which is more critical than the low power mode. Figure 2.16 shows the simulated S_{22} of the PA when the PA operates in both high-power and low-power modes. As expected, S_{22} degrades in low-power mode, the simulation results are in close agreement with the mathematical derivations. The simulated gain (S_{21}) of the PA is also shown in Figure 2.16. Since the entire matching network and the output loads are implemented on-chip, the 3-dB bandwidth of the PA is around 700 MHz.

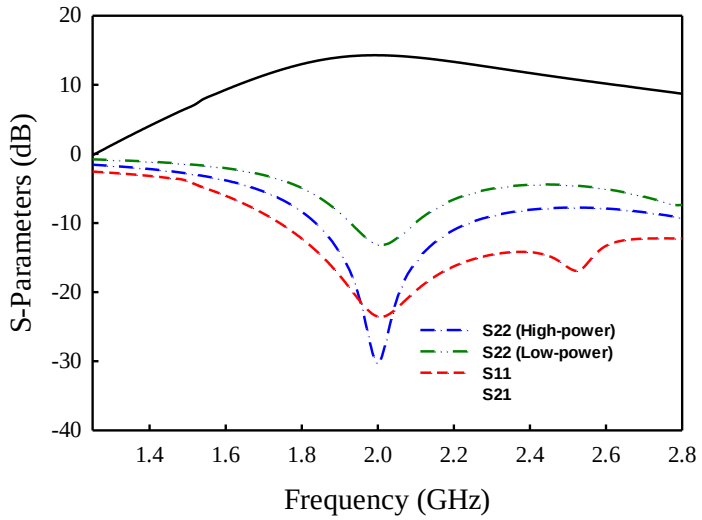


Figure 2.16. Simulated S-parameters for the proposed PA.

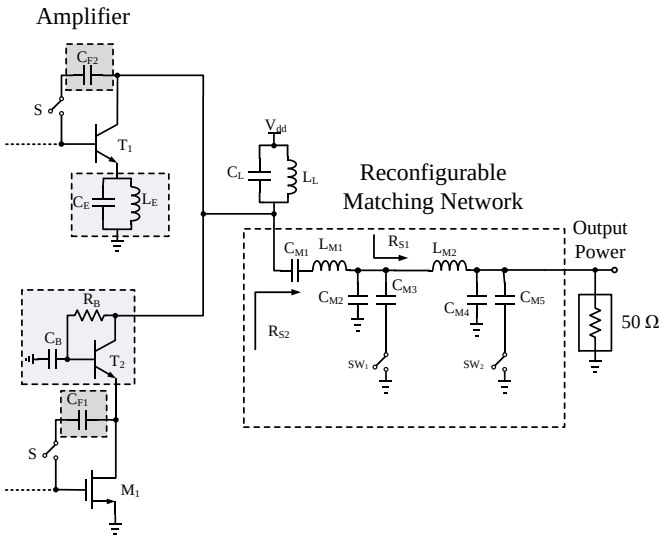
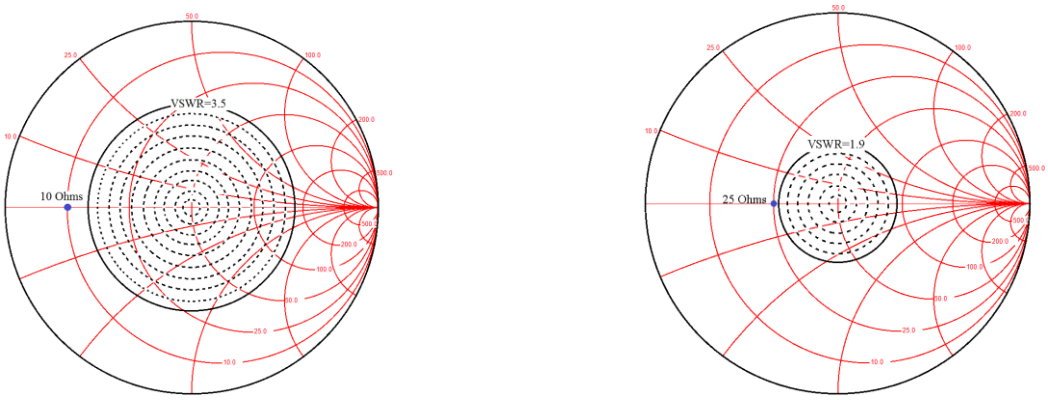


Figure 2.17. The reconfigurable matching network.

II.4.6. Load Mismatch Analysis

One of the critical factors in handset PAs which impacts linearity, power efficiency, and maximum output power is the load impedance mismatch. As the handset is used in different positions, the antenna load no longer provides the nominal input impedance of 50 Ohms, and it varies within a certain voltage standing wave ratio (VSWR) circle in the smith chart. In order to evaluate the PA performance under load mismatch condition, the translated antenna load trough the reconfigurable matching network has been derived for different antenna loads. The matching network provides 10 Ohms for high-power mode, and 25 Ohms for low-power mode. As long as the matching network adapts itself to provide the same output load in two modes under mismatch condition, the PA performance will be preserved. The matching network consists of two cascaded L network. Assuming all the capacitors (C_{M2}, C_{M3}, C_{M4}, and C_{M5}) are tunable,

by changing the ratio between the two capacitors, C_{M2}+C_{M3} over C_{M4} in the high-power mode, and C_{M2} over C_{M4}+C_{M5} in the low-power mode, the load mismatch effect can be compensated within a certain VSWR circle. Simulation results in Figure 2.18(a)-(b) show that all the impedances inside the VSWR =3.5:1 circle are matched to 10 Ohms in the high power mode, while the tuning range is decreased to VSWR =1.9:1 in the low power mode since it is matched to 25 Ohms.



(a) (b)

Figure 2.18. (a) The VSWR circle matched to 10Ω for the of antenna load mismatch inside the circle (high-power mode), (b) the VSWR circle matched to 25Ω for the of antenna load mismatch inside the circle (low-power mode).

II.4.7. Effect of Timing Misalignment on Linearity Performance

There are three switching blocks in the PA, two for switching the bias values of the pre-amplifier and the main amplifier, and one for switching the reconfigurable matching network. These blocks should be switched based on the input signal timing

pattern in each stage. Figure 2.19 shows the possible delays between the PA stages, τ_{a1} is the delay of the input RF signal between preamplifier and the main amplifier stage, and τ_{a2} is the delay of the RF signal between the amplifier and the matching network. τ_{s1} is the delay of the decision signal, between the output of the comparator and the main amplifier , and τ_{s2} is the delay of the decision signal between the main amplifier and the matching network. If $\tau_{a1}= \tau_{s1}$, and $\tau_{a2}= \tau_{s2}$ the PA performance would be preserved. On the other hand, if the delays are not equal, for example, if $\tau_{a2}< \tau_{s2}$, then the amplifier switches to the low-power mode, while the matching network is still in the high-power mode. Therefore the gain drops until the matching network is switched to the low-power state as well. This will cause signal discontinuity at the output, which degrades the linearity.

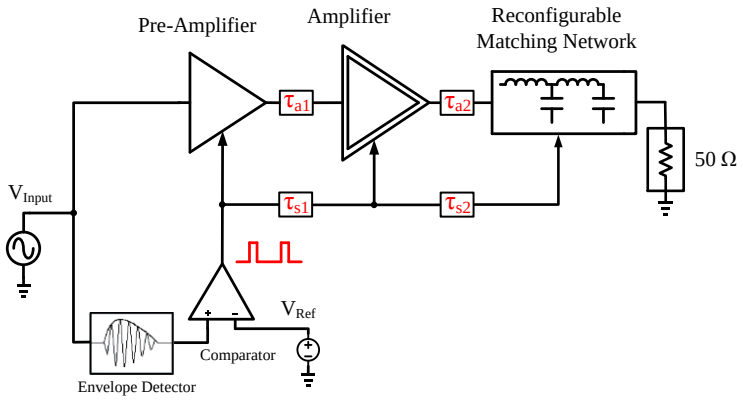
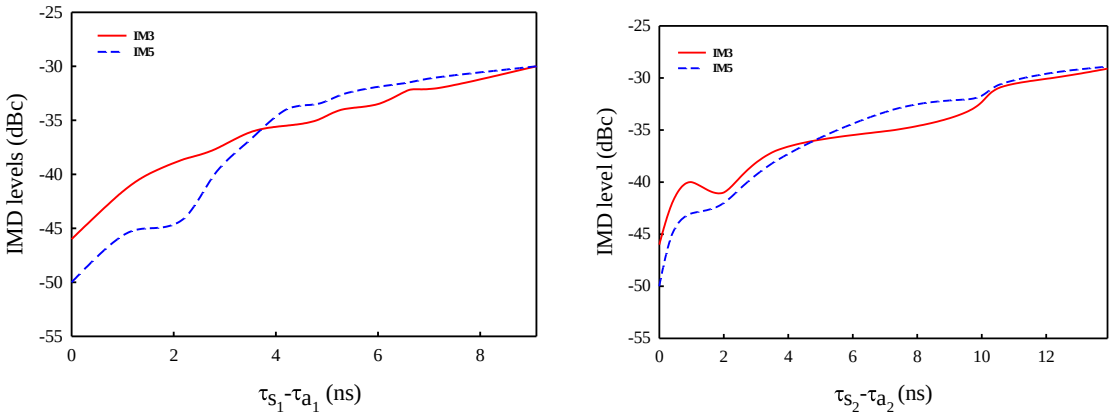


Figure 2.19. Timing delays between different stages of the PA.

The output of the comparator will be directly applied to the pre-amplifier stage. This signal is routed throughout the chip until it switches the amplifier stage, and finally

it switches the matching network. The effect of τ_{s1}-τ_{a1}, and τ_{s2}-τ_{a2} delays on IM_3 and IM_5 levels has been simulated. Figure 2. 20 shows the simulation results of the two-tone test, for the two delays and frequency spacing of 10 MHz. As can be seen, the system is more sensitive to the delay τ_{s2}-τ_{a2}. Especially, IM_5 level degrades as the delay increases. The delays up to 3 ns can be tolerated for a 10 MHz input signal envelope. The effect of the delay for lower frequency signal envelopes is smaller, and the linearity of the PA is not too sensitive as the envelope frequency decreases. In order to apply the comparator output, and the RF signal to each stage simultaneously, the routing of the input RF signal and the switching signal has been performed along with each other throughout the entire chip. By careful layout and post layout simulations, the delays between the two signals are minimized.



(a) (b)

Figure 2. 20. Effect of timing misalignment on PA linearity performance (a) IMD levels vs τ_{s1}-τ_{a1}, and (b) IMD levels vs τ_{s2}-τ_{a2}.

II.4.8. Automatic Gain Calibration

The most important mismatch factor in the linearity performance of the PA, is the gain mismatch between the two modes of operation. To adjust the gain using an automatic calibration mechanism, two different signal amplitudes can be applied to the PA at low-power and high-power modes, respectively, and the biasing values are adjusted until equal gains in both modes are achieved. This can be performed with the aid of the available Digital Signal Processing (DSP) unit required for OFDM modulation. The block diagram of the automatic gain adjustment is shown in Figure 2.21. The biasing values are set for low-power or high-power mode through the DSP as follows: in the PA initial setup for gain matching calibration, a single tone signal is up-converted to the frequency of operation. By turning on the switch S_1 at the output of the PA, the signal is down-converted back to the DSP by employing a replica of the up-conversion mixer. Therefore the gain of the PA can be measured directly using the DSP for each mode of operation, and then the biasing values are adjusted to achieve the best gain matching in the two modes, which translates to better linearity. After the calibration is performed, the switch S_1 is turned off, and the PA works with an OFDM modulated signal generated by the DSP Unit.

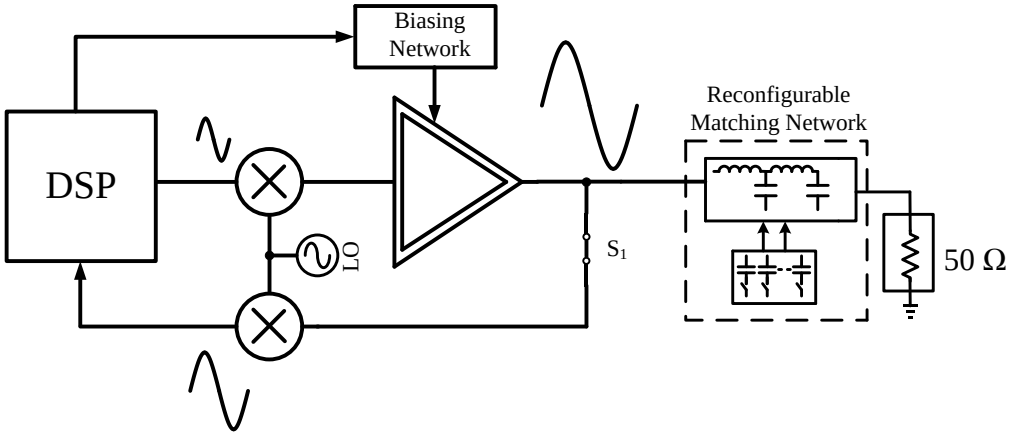


Figure 2.21. The block diagram of the gain mismatch automatic calibration.

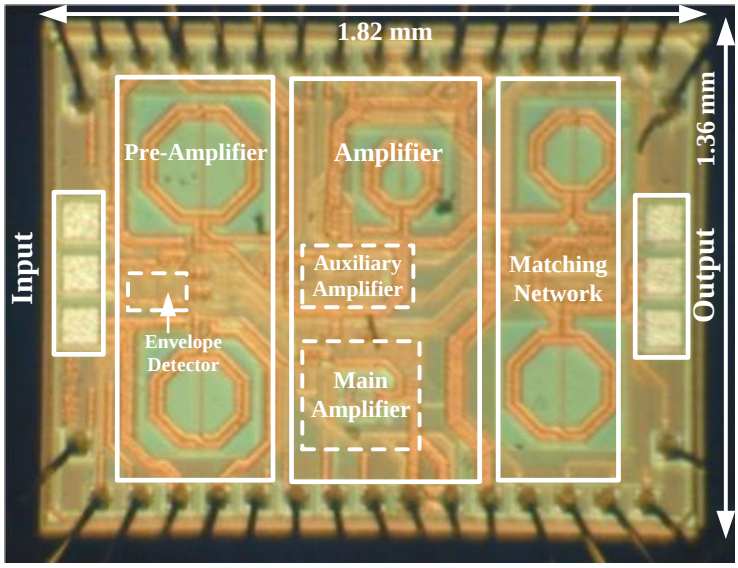


Figure 2.22. The die micrograph of the fabricated PA in 0.25 μm SiGe:C BiCMOS Technology.

II.5. Measurement Results

The PA has been fabricated using 0.25 µm SiGe:C BiCMOS Technology from NXP semiconductors‡. All the components including the matching network and the envelope detector are integrated and no off-chip element has been used. The PA is designed to be single-ended to avoid any baluns in the circuit. The chip has been open-packaged using 56 pin HVQFN package. To remove the effect of the package parasitic and bond wire inductance, ground-signal-ground (GSG) RF probes are landed on the input and output pads. The die micrograph is shown in Figure 2.22 with the dimensions of 1820 µm × 1360 µm including the wire-bonding pads. Supply voltages for the main amplifier and the pre-amplifier are 2.5 V and 1.7 V, respectively. S-parameter measurements have been performed for the designed PA using the Agilent N5230A PNA series Network Analyzer, and the results are shown in Figure 2.23. The measured gain of the PA is 13 dB, which is 1 dB lower than the simulation results. The gain drop is mostly because of inaccurate modeling of the ground bond- wires. The 3-dB gain BW is around 600 MHz, and the maximum output power is at 2.03 GHz. The input match is better than -9.5 dB in the desired frequency band. The input matching has a frequency shift; this shift is mostly because of the effect of the bond-wires through the switches for two different biases. The output matching for high-power and low-power modes is better than -14 dB and -13 dB, respectively, in the desired frequency band (2GHz).

‡ http://www.nxp.com/

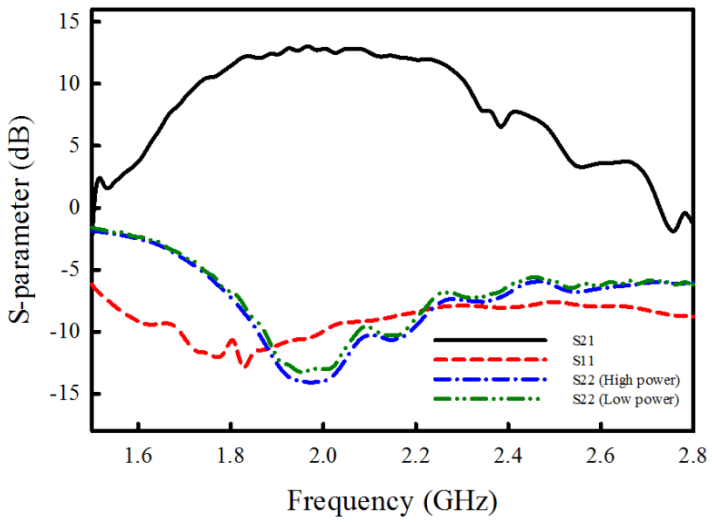


Figure 2.23. Measured S-parameters for the designed PA.

The input signal is swept from -20 to 13 dBm, while the output power is monitored using a spectrum analyzer. Figure 2.24 shows the output power and the PAE of the PA versus the input power. Output P_{1dB} of the PA is 21 dBm with PAE of 32%. The saturating output power is 23 dBm in which the PAE is increased to 38%. Since P1dB happens to be at 9 dBm input power (the peak input power), the system is switched to a low-power mode when the input is 6 dB lower than the peak input power, or 3 dBm, in which there is a small difference between the output powers at the transition (< 0.2 dB). For 21 dBm output power, the measured current consumption for the amplifier and pre-amplifier stages are 110 mA and 40 mA, respectively. The current consumption lowers down to 54 mA and 22 mA for 15 dBm output power. The PAE at 6 dB back-off from P1dB is 23%, therefore the efficiency improvement employing switching biasing technique is more than 10%.

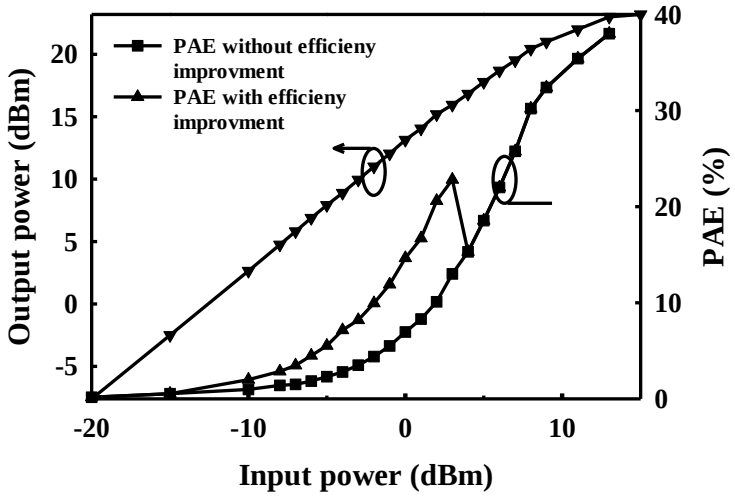


Figure 2.24. PA output power and PAE measurement results versus the input power. PAE is shown with and without efficiency improvement technique.

The linearity of the PA is measured first by employing the two tone test. The tones are located at 2.03 GHz with a 1 MHz space. The bias values of each transistor are tuned for the maximum IM_3 cancellation for the highest output power. Figure 2.25 shows the measurement results for the output IM_3 and IM_5 versus the average output power. The IM_3 and IM_5 are 41 dB and 44 dB below the fundamental tone for the entire non-saturated output power. By turning off the transistor M_1, IM_3 is increased by more than 10 dB, which shows the effectiveness of the feed-forward cancellation approach. The two-tone test has also been performed for 10 MHz frequency spacing, and the results are very close to the 1 MHz frequency spacing with a small degradation in IM_3 cancelation (less than 1 dB). Since the main amplifier transistors, T_1 and M_1 are in class AB region, the level of the IM_5 is not small, and as the linearization technique is tuned for IM_3 cancellation, minor improvement can be seen at the output power IM_5. An extra

NMOS transistor can be added to the output in parallel to T_1 and M_1 [35], with a certain biasing for each mode of operation. By characterizing the biasing and the size of the added transistor, the IM_5 level at the output can also be cancelled out to further improve linearity, error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR).

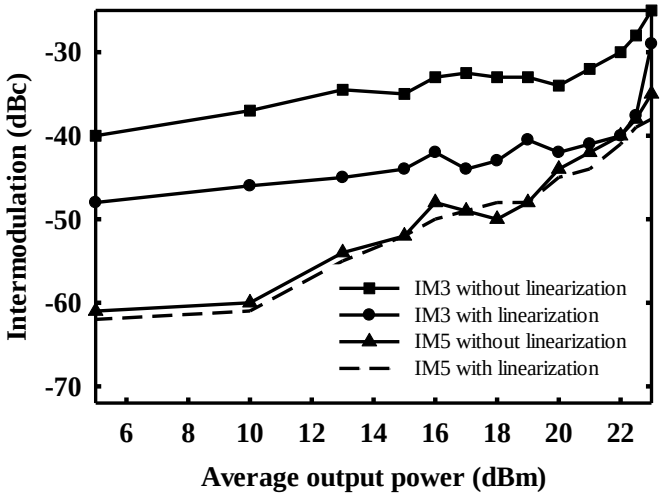


Figure 2.25. The measured difference between fundamental tone, IM_3 and IM_5 in dBc in a two- tone test with 1 MHz spacing at 2.03 GHz with and without linearization technique.

For the low input powers (Pin < -8 dBm) the gm of T_1 is almost 6 times larger than its NMOS counterpart (M_1) and it provides most of the gain. On the other hand, the linearity of T_1 is sufficient for the low input power levels since the IM_3 levels are small at the output (below -45 dBc). Therefore, for further improvement of the PAE, M_1 and the pre-amplifier transistor M_2, can be turned off without sever degradation in the

linearity performance of the PA. As shown in Figure 2.26, this will result in further efficiency improvement in larger power back-offs.

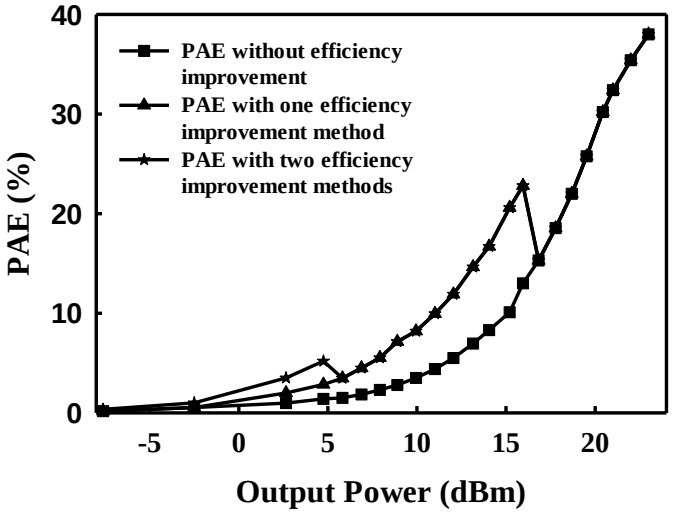


Figure 2.26. PAE measurement results versus the input power with different efficiency improvement techniques compared to a fixed bias PA.

Figure 2.27(a) and (b) show the time domain signals for the two tone test. Figure 2.27(a) shows a smooth transition which is accomplished by achieving an equal gain between the two modes, while in Figure 2.27(b) a mismatch is intentionally applied between the two modes by introducing mismatch in the voltage biases. As a result, the gain in the low-power mode is higher than the gain in the high-power mode. IM_3 level is degraded from -40 dBc to -26 dBc with introducing the mismatch (Figure 2.27(c) and (d)). These results prove the effectiveness of the reconfigurable matching network

technique to improve linearity and efficiency by setting the gains of the two modes of the PA to be equal.

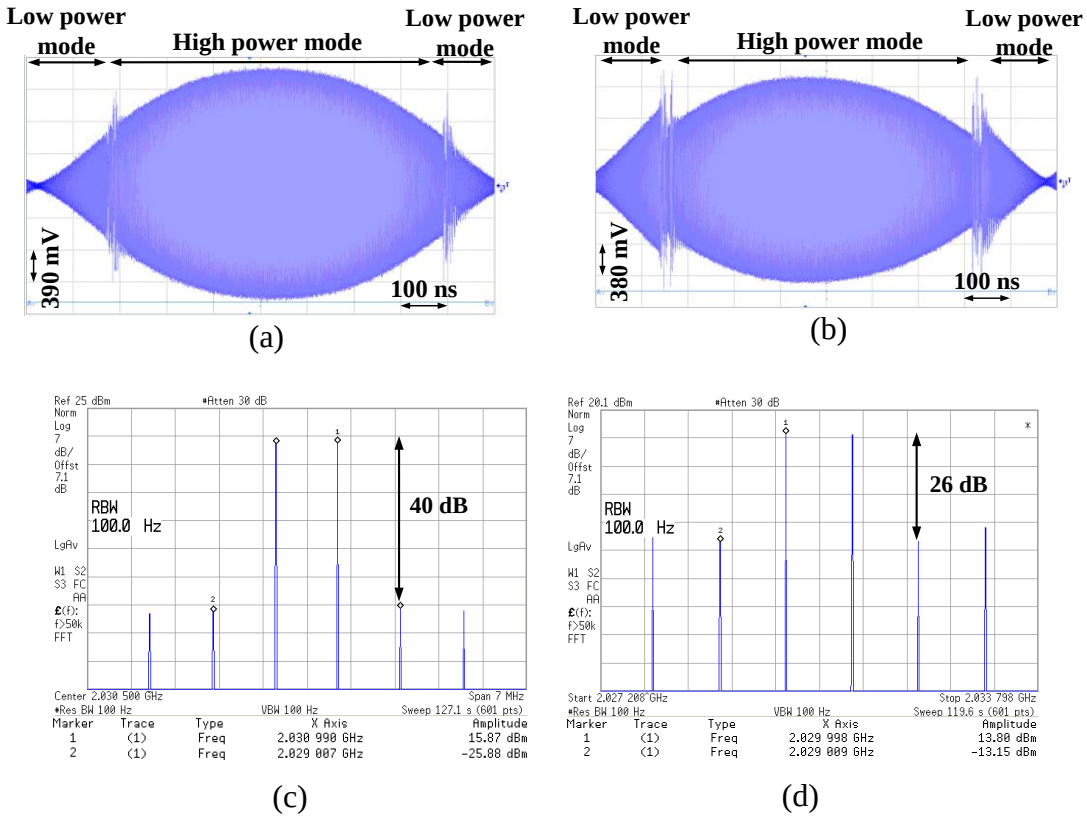


Figure 2.27. Time domain measurement of the two tone test with 1 MHz spacing at 2.03 GHz: (a) Equal gain in the transition between the two modes, (b) unequal gain in the transition between the two modes, (c) spectrum of the signal at (a), (d) spectrum of the signal at (b).

The EVM has been measured to determine the linearity of the designed PA using the IEEE 802.16e WiMAX standard with OFDM 64-QAM modulation at a carrier frequency of 2 GHz (Figure 2.28). For WiMAX standard, 56 Mbps and 10 MHz channel

bandwidth PAPR is around 12dB. The average rate for a 10MHz WiMAX packet is varying between 1-15 MHz, and the stages are switched with the same rate. The measured EVM is below -30 dB for the output powers below 15.5 dBm. Figure 2.29 shows the measured output spectrum of the PA for 14 dBm output power, ACLR of -36 dBc is achieved. Also, the average efficiency of the PA with efficiency improvement technique at -28 dB EVM (15.9 dBm average output power) is 19%, which drops to 11% as the efficiency technique is switched off. In order to realize how much improvement is achieved by using the IM3 cancellation technique, ACLR and EVM have also been measured without applying the linearization technique as shown in Figure 2.28 and Figure 2.29. To measure ACLR, and EVM without linearization technique, the NMOS path is turned off by grounding the biasing values. Since turning off one path, drops the output power by 5-6 dB, for fair comparison, the PA gain is increased by increasing the bias values in the bipolar path. In order to only observe the effect of linearization technique, the reference voltage in the comparator is set to maximum value, to avoid the effect of reconfigurable matching switching and gain mismatch on linearity. As can be seen in Figure 2.29, the ACLR improves from -31 to -36 dBc using the IM3 cancellation technique for a 10 MHz bandwidth WiMAX 64QAM signal with 14 dBm average output power. The EVM is also measured for different output powers, and the linearization technique improves the EVM by 4.5 dB at 14 dBm average output power.

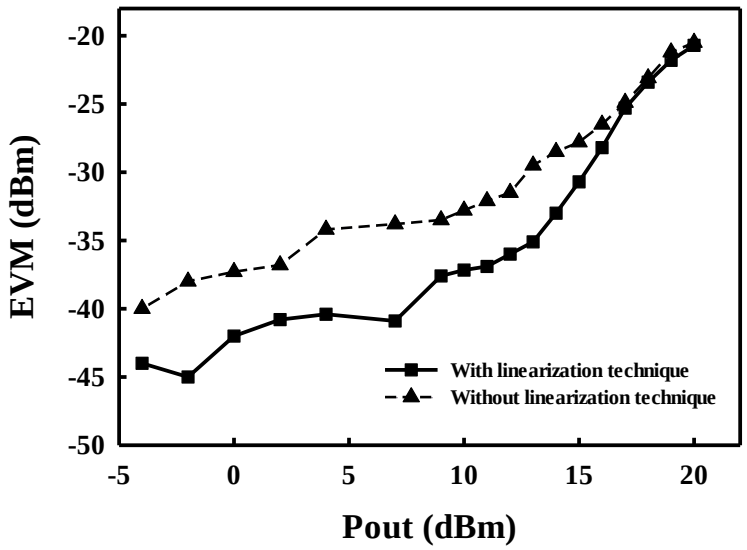


Figure 2.28. Measured EVM as a function of average output power for WiMAX standard with 64QAM modulation and 10 MHz BW signal with and without linearization technique.

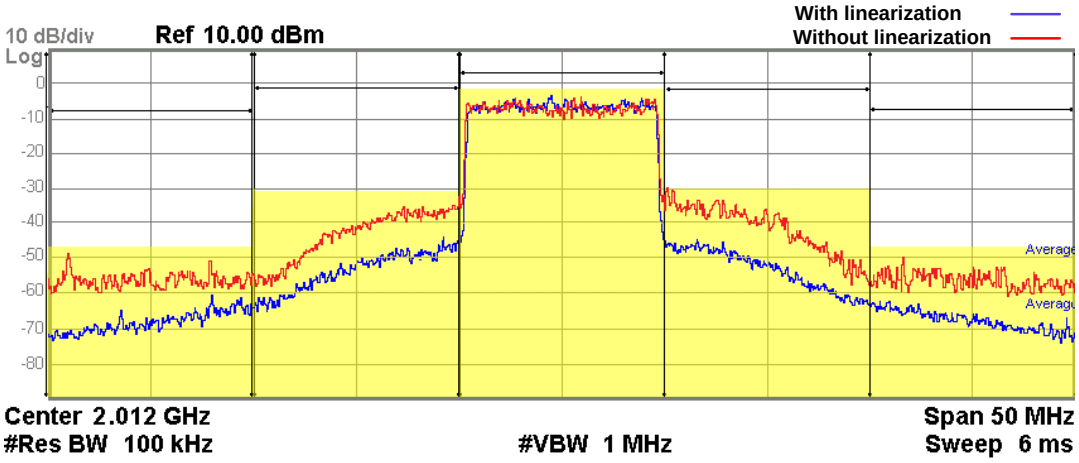


Figure 2.29. Output spectrum of the PA excited for WiMAX standard with 64QAM modulation and 10 MHz BW signal (14 dBm average output power) with and without linearization technique.

As discussed before, the gain of the PA in the low and high power modes needs to be matched. Any gain mismatch between the two operating modes degrades the linearity performance of the linearized PA. On the other hand, maintaining equal gains in both modes is really challenging due to PVT variations. In order to evaluate the performance of the PA under gain mismatch, several measurements have been performed. Gain mismatch is achieved by changing the bias values and reconfigurable matching network. Figure 2.30(a) shows the effect of gain mismatch on IMD levels at 20 dBm output power, the IM_3 levels are still below -36 dBc for 1.3 dB gain mismatch while the total PA gain is 13dB. Figure 2.30(b), and (c) show the EVM and ACLR performance under gain mismatch for a WiMAX 64QAM signal (BW=10MHz) with 14 and 10 dBm output power, respectively. For 14 dBm output power, the EVM degrades by 3 dB in 1.2 dB gain mismatch. For 10 dBm output power, the EVM under gain mismatch up to 2.8 dB is always below -30 dB. The gain mismatch of 1.2 dB also degrades ACLR by 4 dB at 14 dBm output power, while for 10 dBm output power; ACLR is always below -36 dBc for gain mismatch up to 2.8 dB.

In Table 2.5, the performance of the PA is compared with recently reported linear efficient PAs. Based on the comparison, it is concluded that the implemented PA has a superior performance compared to the state-of the-art in case of linearity and efficiency in both 1dB compression point and power back offs. In case, the technology could tolerate a larger power supply, the output power, and the average PAE would be increased with the same EVM achieved for WiMAX 64QAM signal with 10 MHz BW.

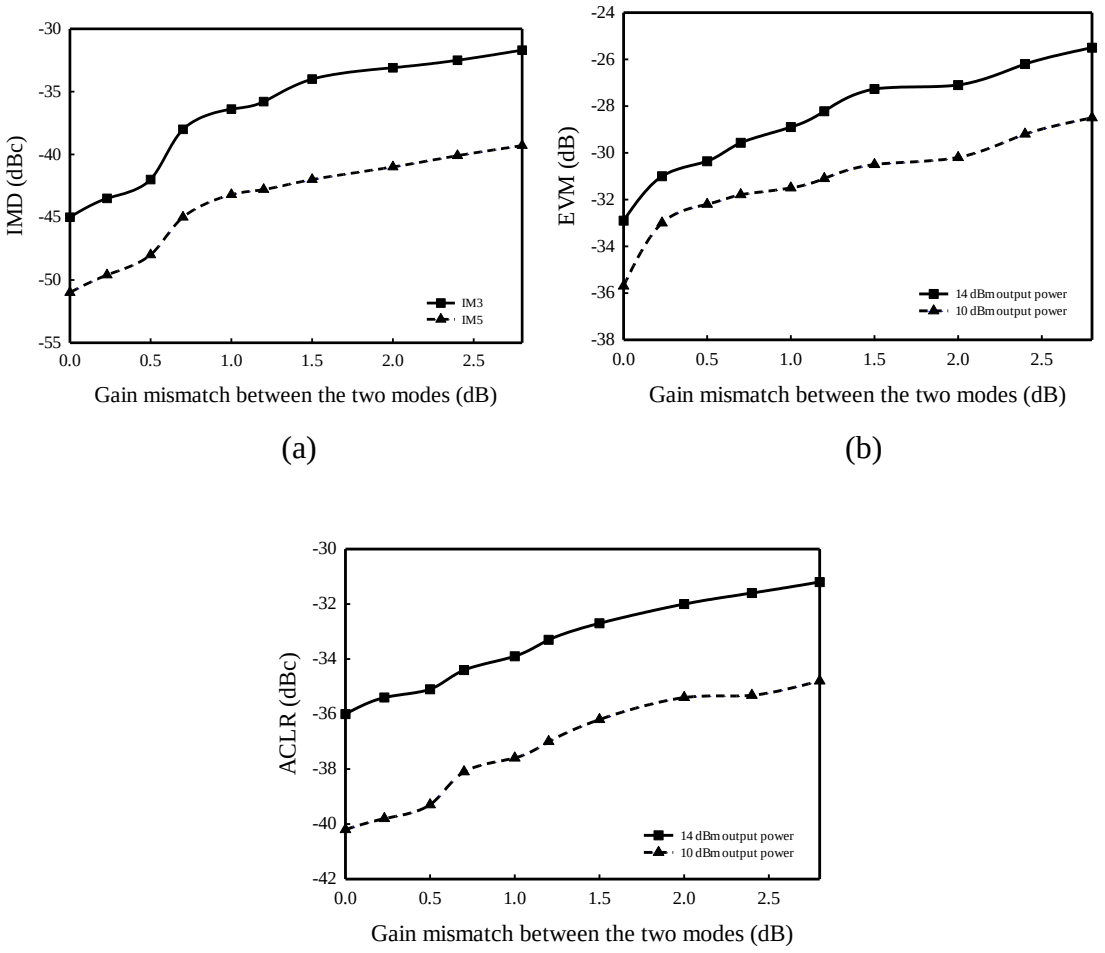


Figure 2.30. Effect of gain mismatch between the two PA operating modes on linearity performance, (a) IMD levels under gain mismatch, (b) EVM under gain mismatch for a WiMAX 64QAM 10 MHz BW signal with 14and 10 dBm output power, (c) ACLR under gain mismatch for a WiMAX 64QAM 10 MHz BW signal with 14and 10 dBm output power.

Table 2.5. Performance summary and comparison of the linearized efficient PA compared to the state of the art PA designs.

	Technology	Frequency (GHz)	Power Supply (V)	Gain (dB)	P_{1dB} (dBm)	PAE (%)		Inter-modulation levels at P1dB		EVM @ average P_{out}	Average PAE (%)	Modulation (Signal BW)
						P_{1dB}	6dB BO	IM_3 (dBc)	IM_5 (dBc)			
[18] JSSC 04	0.5 µm CMOS	1.75	3.3	21	20.2	13.5	5	-45	N/A	-	-	-
[19] JSSC 05	0.18 µm CMOS	N/A	N/A	12	20	36	15	-25	N/A	-25 dB @ 14.5 dBm	-	-
[21] JSSC 06	0.18 µm CMOS	2.45	2.5	18.9	20.2	35	13	-28	-45	-	-	-
[22] JSSC 06	0.18 µm CMOS	2.45	N/A	17.5	20.5	37	14	-27	-43	-27 dB @ 15 dBm	14	WLAN 64QAM (20 MHz)
[36] JSSC 07	0.18 µm SiGe BiCMOS	2.4	3.3	11	25	30	13	-	-	-26 dB @ 20dBm	28	WLAN 64QAM (20 MHz)
[23] JSSC 08	0.18 µm CMOS	2.4	1.2	17	24	31.5*	16*	-29**	-36**	-27 dB @ 14.5 dBm	9*	WLAN 64QAM (200KHz)
[24] JSSC 09	90 nm CMOS	2.4	3.3	28	28	25	14	-34***	-42***	-25.3 @ 22.7 dBm	12.4	WiMAX 64QAM (10 MHz)
[37] JSSC 09	0.13 µm SOI CMOS	1.92	1.2	15	-	-	-	-	-	-36.47 @ 15.3 dBm	22	WiMAX 64QAM (5MHz)
[38] TCASI 11	0.18 µm SiGe BiCMOS	2.3	4.2	10.5	20	49	10	-	-	-26.19 @ 17.4 dBm	30.5	WiMAX 64QAM (8.75 MHz)
[25] JSSC 11	0.18 µm CMOS	2.5	3.3	31.3	28	30	19	-	-	-31 @ 17 dBm	8	WLAN 64QAM (10 MHz)
This Work	0.25 µm SiGe:C BiCMOS	2	2.5	13	21	32	23	-41	-44	-30.7 @ 15 dBm	16	WiMAX 64QAM (10 MHz)

* Drain Efficiency

** At 18 dBm output power

*** At 23 dBm output power

II.6. Summary

In this chapter, a fully integrated linear and efficient PA in 0.25 µm SiGe:C BiCMOS technology is presented. A new technique based on reconfigurable matching network has been proposed to improve the efficiency at power back offs. The efficiency is improved by decreasing the DC bias values during the low input power signal, which has a higher probability over high input power during normal operation. To maintain the same gain during the transition from low to high input power, an on chip reconfigurable matching network is implemented. Using this technique, the efficiency is improved by 10%. The linearity is greatly improved by adding a linearizer NMOS transistor to the main BJT to cancel out gm3. A second harmonic current degradation is used to improve both output power and the linearity. By adding this feed-forward path, the IM_3 of the PA is 41 dB below the fundamental during the entire output power, which shows 10 dB improvement compared to the case of a single bipolar transistor. P_{1dB} of the PA is 21dBm with a PAE of 32%. By employing the linearization technique, EVM and ACLR are improved by 4.5 and 5 dB, respectively, for a WiMAX 64QAM signal at 14 dBm average output power. By increasing the number of comparator levels, the input signal will be divided into more levels. Therefore, the PA will have more modes of operation each with a specific biasing value, and output load provided by the reconfigurable matching network. By increasing the number of PA operation modes, the power consumption will be a more linear function of the input signal; therefore, the PAE will increase at the price of having a more challenging reconfigurable matching network.

Also, the automatic gain control loop can be added to the PA to tune the gain in different modes to achieve the best gain match, which will result in a better linearity.

CHAPTER III

CMOS UWB IMPULSE RADIO TRANSMITTER WITH IN-BAND NOTCH AT IEEE 802.11A SYSTEM*

III.1. Introduction

Ultra wide-band (UWB) systems are attractive due to their ability for high data rate, low power consumption, low complexity, and low cost communications. High data rate communications can be used in Wireless Personal Area Networks (WPANs), cell phones, laptops, tablets and wireless Universal Serial Buses (USBs), especially for video communications as a substitution for cables. Low power UWB transceivers are good candidates for applications such as positioning, identification and sensor networks. Three different UWB architectures have been proposed in the literature. Multi Band Orthogonal Frequency Division Multiplexing (MB-OFDM), Impulse Radio UWB (IR-UWB), and Direct Sequence UWB (DS-UWB) [3]. Since typical UWB systems can achieve data rates of 10 Mbps, they are good candidates for replacing Bluetooth in future laptops, tablets and cell phones. Therefore, UWB systems need to work in the presence of systems such as IEEE 802.11a/g. The FCC mask provided for UWB communications is for avoiding any disturbance to operating narrow-band (NB) systems within the UWB band. The coexistence problem of UWB and NB systems, especially 802.11a, is

extensively evaluated in [4]-[7]. UWB transmitter (TX) can severely degrade the performance of an IEEE 802.11a transceiver in a Non-Line of Sight (NLOS) communication. For a UWB system working in the presence of an 802.11a interferer, irrespective of the transmission (LOS or NLOS), the UWB system is quite vulnerable to the NB interference. It can be concluded that in spite of the limitation assigned by the FCC, the coexistence of UWB and NB systems is still an unsolved challenge.

Different solutions have been proposed in the literature to suppress the effect of an IEEE 802.11a system on UWB receivers (RX). Since the interferer can saturate or even desensitize the low-noise amplifier (LNA) of the UWB front-end, filtering needs to be performed in the RF domain. In [39]-[40], a tunable notch filter has been implemented inside the LNA and before the baseband unit. In [41], a dual-antenna UWB transceiver is implemented for group 1, which is employing antenna diversity and integrated RF selectivity techniques to null out the NB interferer. In [42], a channelizing technique has been used to resolve the interferer problem in the lower UWB band.

Since most of the time a UWB system is considered to be a victim of coexistence with a 5-6 GHz Wi-Fi signal, UWB TXs are not implemented in a way to protect the Wi-Fi RX. The coexistence problem is more challenging for an IR-UWB TX, as the IEEE 802.11a signal can be inside the pulse spectrum. Since employing the entire UWB spectrum results in a better resolution in positioning systems, and a higher data rate in data communications, it is interesting to cover the entire UWB spectrum with a single UWB pulse. However, transmission in the 5-6 GHz ISM band will degrade the sensitivity of an IEEE 802.11a system. In the literature, to avoid the NB system, mostly

the lower or the higher UWB band has been chosen for signal transmission. In [43]-[45], the TX power (the interference) by the UWB TX in the frequency of the NB system is lowered to -82 dBm/MHz, but only the lower band of UWB spectrum (3.1-5 GHz) has been used. In [46], the higher band of UWB has been used to achieve a larger bandwidth. In this case the interference level for the NB system is larger than -60 dBm/MHz. In [47], in spite of employing a dual-band topology to avoid the 5-6 GHz WLAN signal while exploiting 4 GHz BW, the interference level for the NB system is still larger than -65 dBm/MHz. Other reported TXs that are targeting larger than 5 GHz bandwidth [48]-[49] are providing even larger interference power (>-52 dBm/MHz) for the NB system. This work proposes a solution to suppress the effect of UWB TX as an interferer on a NB RX while covering a large BW inside the UWB spectrum.

In this chapter, an IR-UWB TX with in-band notch implementation is presented. The TX generates an analog pulse that covers the majority of UWB spectrum. It employs the frequency characteristics of a Gaussian monocycle pulse and features a tunable notch in the frequency of the in-band NB system [50]-[51]. Due to unique pulse generation technique, the proposed TX causes a small interference power (~ -78 dBm/MHz) for the IEEE 802.11a RX; while the bandwidth of the signal is larger than 5.5 GHz. The TX data rate can reach to 400 Mpulse/s with energy of 65 pJ/Pulse at maximum data rate.

At first the motivation behind the work has been explained, and the effect of UWB transmitter on Wi-Fi receiver sensitivity is investigated for different scenarios. Then, the theory behind the analog pulse generation technique has been explained. For the circuit implementation of the UWB pulse, a novel architecture has been proposed

and the output is verified with circuit level equations. At the end, the measurement result of the proposed transmitter is shown and verified with simulation results.

III.2. UWB Transmitter Design

III.2.1. Motivation

In an IEEE 802.11a system, the minimum detectable signal must have a bit error rate (BER) of 10-5 to achieve a data rate of 54 Mbps, which acquires a minimum signal to noise ratio (SNR) of 21 dB [9]. If the NF requirement for the system is 10 dB, the sensitivity of the NB system (P_{Sen}) for SNR of 21 dB is as follows:

$$P_{Sen}=-114\ {}^{dBm}/_{MHz}+10\log(NF)+10\log\left(BW_{(20\ MHz)}\right)+SNR=-70\ dBm \tag{3-1}$$

The power of the UWB signal received by the NB RX, P(r), can be calculated from the following equation [7]:

$$P(r)=P_{UWB}\left(\frac{\lambda}{4\pi r}\right)^2\left(\frac{d_{Bp}}{d_{Bp}+r}\right)^2 \tag{3-2}$$

where PUWB is the transmitted power of the UWB pulse, r is the distance between the UWB TX and the NB RX, λ is the wavelength of the signal (geometric mean of the UWB pulse 3-dB frequencies), and d_{Bp} is the break point distance, which is considered to be 1m for indoor applications. It can be calculated from (2) that for a UWB signal, the transmitted path loss is 50 dB for r=1 m and 75 dB for r=5 m. If we assume the UWB TX operates with its full effective isotropic radiation power (EIRP) of

-41.3 dBm/MHz, the UWB interferer will affect the noise floor of the NB RX, and the modified sensitivity of the NB RX will be as follows:

$$For\ 5m \Rightarrow P_{Sen} = 10\log\left(10^{-11.4} + 10^{(-41.3-75)/10}\right) + 10\log(NF) + 10\log(BW) + SNR = -67.8\ dBm \quad (3\text{-}3)$$

$$For\ 1m \Rightarrow P_{Sen} = 10\log\left(10^{-11.4} + 10^{(-41.3-50)/10}\right) + 10\log(NF) + 10\log(BW) + SNR = -47\ dBm \quad (3\text{-}4)$$

Therefore, in the presence of a UWB TX (r=1m) to maintain the same data rate, the minimum detectable signal drastically degrades, and the NB RX has to decrease the data rate (SNR) to increase the range of detectable NB TXs. In the absence of a UWB interferer, it can be calculated that the NB RX could maintain a 24 Mbps data rate (assuming 10 dB SNR) up to 30 meters communication range from the NB TX. This range decreases to 25 and 10 meters in the presence of UWB TX for r=5m and r=1m, respectively. The situation is worse when UWB system is considered a 3.1 to 10.6 GHz wideband noise. Therefore, due to LO harmonics (in the NB RX) and non-linearity of the NB front-end, UWB noise will be folded down into the base-band signal of the NB RX, and the system performance will be degraded even more. This is one of the reasons why industry shows less attention to UWB transceiver implementation recently. It can be concluded that UWB TXs must provide negligible interference level to a NB system for practical applications.

III.2.2. UWB Pulse Design

IR-UWB communication is performed by transmitting and receiving short duration pulses (in the order of nanoseconds). Different UWB pulse generation methods have been presented in the literature, which can be categorized into basic and advanced pulse generation techniques. Gaussian and Gaussian derivate pulses are popular pulses in UWB systems. The implementation of these pulses have been reported in [52]-[54]. On the other hand, Modified Hermite and Prolate Spheroidal Wave Functions (PSWF) based pulse generation are more advanced approaches. Although, the implementation of these advanced pulses are more complex, they have better power spectral density and frequency selectivity in the UWB spectrum [55]-[57].

The proposed UWB pulse has a process tolerant tunable frequency notch and covers the entire UWB spectrum. The pulse is based on Gaussian pulse characteristics. The first derivative of the Gaussian pulse (Gaussian monocycle) is given by:

$$Y(t)=K\frac{-2t}{\tau^2}e^{-(t/\tau)^2} \tag{3-5}$$

$$Y(f)=K\tau\sqrt{\pi}(j2\pi f)e^{-(\pi\tau f)^2} \tag{3-6}$$

where Y(t) and Y(f) are the time and frequency domain (pulse power) representation of the Gaussian monocycle, respectively. As can be seen in (6), Gaussian monocycle has no DC component. Therefore, the up-converted monocycle pulse would generate a notch in the frequency of up-conversion [58]. This notch is fixed to the frequency of up-conversion, and it can be easily tuned by changing the up-conversion frequency. The bandwidth of the pulse can vary by changing the parameter τ. FCC regulations limits the

allowable UWB bandwidth to 3.1-10.6 GHz, and considering a narrowband interferer within 5-6 GHz range, the pulse should be up-converted to 5.5 GHz. Due to the pulse symmetry around DC, the bandwidth of the generated pulse is extended from 3.1-5.5 GHz and 5.5-7.9 GHz. Therefore, the pulse cannot cover UWB band from 7.9-10.6 GHz. Covering the entire UWB spectrum is essential in ultra-high-resolution radars and positioning systems. To cover the entire spectrum, two Gaussian monocycle pulses are generated with different values of τ (τ_1 and τ_2) and both pulses are up-converted to the same frequency f_{LO} (5.5GHz). The frequency representation of the resulting pulses are:

$$Y_1(f)=K\tau_1\sqrt{\pi}\left[j2\pi(f-f_{LO})\right]e^{-[\pi\tau_1(f-f_{LO})]^2} \tag{3-7}$$

$$Y_2(f)=K\tau_2\sqrt{\pi}\left[j2\pi(f-f_{LO})\right]e^{-[\pi\tau_2(f-f_{LO})]^2} \tag{3-8}$$

where f_{LO} is the frequency of up-conversion, which is the same frequency as the NB system. For $\tau_1 > \tau_2$, $Y_1(f)$ has a narrower bandwidth compared to $Y_2(f)$. If the lower side-band of $Y_1(f)$ and the higher side-band of $Y_2(f)$ are selected by appropriate filtering and then added together (Figure 3.1(a),(b)), the following pulse is achieved:

$$Y_{Pulse}(f)=H_{filter}(3.1GHz-f_{Lo})\times Y_1(f)+H_{filter}(f_{Lo}-10.6GHz)\times Y_2(f) \tag{3-9}$$

H_{filter} is the band-pass filter with the frequency range shown in brackets in (9). The final frequency and time domain responses of the pulse are shown in Figure 3.1(c), (d), respectively. The pulse covers the entire UWB spectrum while generating a tunable notch (LO frequency) in the frequency of the NB system. Therefore, the interference caused by the UWB TX is extensively decreased.

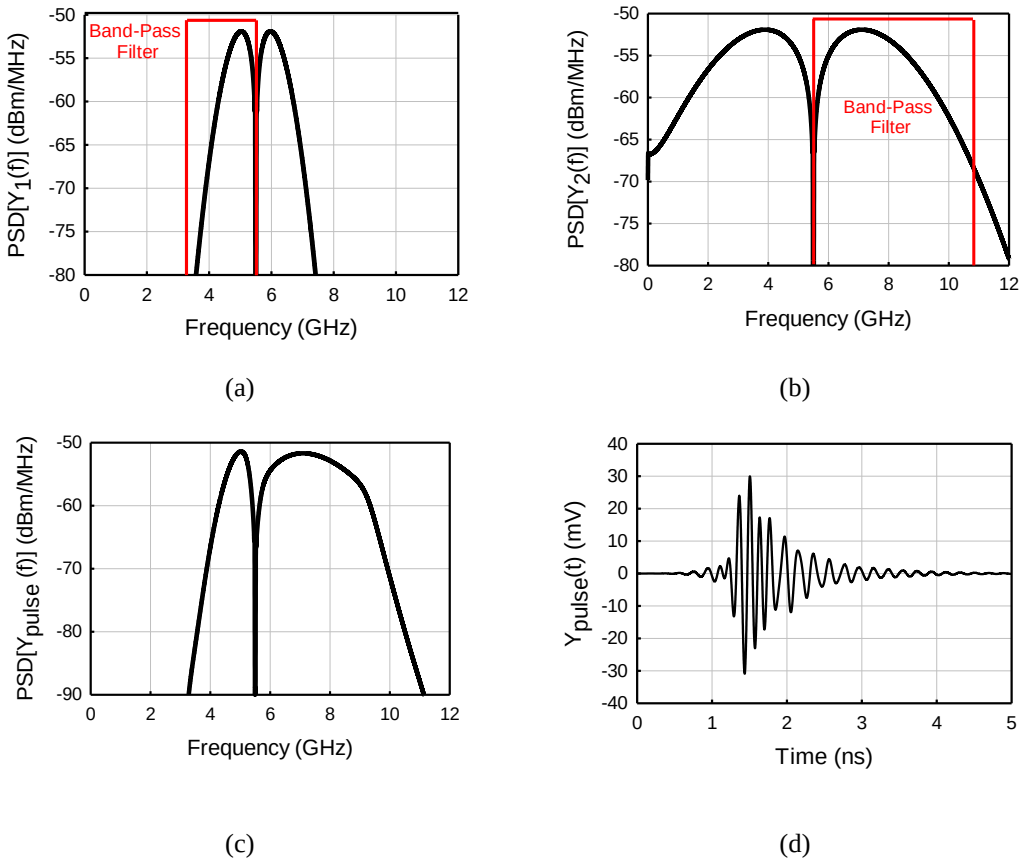


Figure 3.1. (a) Narrow BW up-converted monocycle pulse, (b) wide BW up-converted monocycle pulse, (c) frequency response of the final UWB pulse, (d): time domain response of the final UWB pulse.

III.3. UWB Pulse Generator Circuit Implementation

Different UWB pulse generation circuits have been reported in the literature. The architectures can be divided into three different categories:

1) In [44]-[46], [48], [59]-[60], digital circuits have been employed to generate a UWB pulse that is FCC compatible without any up-conversion. The challenge in digital implementation is pulse shape and spectrum deviation due to PVT variations. In addition, due to the pulse's large low frequency components, the FCC regulations are mostly violated.

2) In [49], [61]-[62], a very wide bandwidth pulse is generated and the pulse has been shaped employing band-pass filters. In this case, a large attenuation is needed to filter the low-frequency components. Low Q on-chip filtering results in a smaller pulse bandwidth. For a larger pulse bandwidth, an off-chip filter is required.

3) In [63]-[65], the base-band pulse is up-converted to higher frequencies, which is FCC compatible. The narrow base-band pulse is generated using gated or analog circuits.

A combination of all three techniques has been used in the design of the proposed UWB pulse.

III.3.1. Baseband Pulse Generation

III.3.1.1. Gaussian and Gaussian Monocycle Pulse Generation

In order to generate the pulse derived in (9), an analog Gaussian pulse needs to be generated. Gaussian function implementation using analog CMOS circuits is challenging. Previously reported Gaussian pulse generators employ a bipolar transistor (inherent exponential characteristic) [52], digitally gated circuits [53], or a step recovery

diode-based circuit [54]. A Gaussian pulse is a combination of quadratic and exponential functions. For quadratic generation, intrinsic characteristic of MOS transistor can be employed. In [58] by applying a triangular pulse to a long channel nMOS transistor, a quadratic voltage is generated. However, for very short duration pulses, the nMOS transistor cannot follow the abrupt slope change in the triangular pulse.

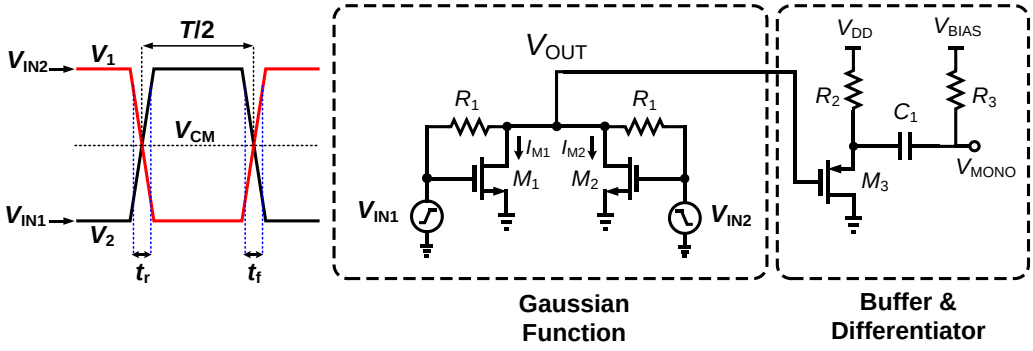


Figure 3.2. Gaussian monocycle pulse generation circuit.

Figure 3.2 shows the proposed approach of the Gaussian pulse generator using short-channel CMOS transistors. A differential structure has been used to generate a Gaussian pulse, while avoiding any abrupt slope change at the input of the transistors. To generate a pulse, symmetric differential input pulses are applied to the circuit, which acts as a voltage ramp in the transitions. A UWB pulse is generated in each transition, and the pulse rate is twice the input pulse frequency. The Gaussian pulse is applied to a wideband differentiator to generate the Gaussian monocycle pulse. The circuit operation is divided into three regions. The output voltage V_{OUT} in Figure 3.2 can be found as follows:

$$\frac{2V_{OUT}(t)-(V_{IN1}(t)+V_{IN2}(t))}{R_1}+I_{M1}(t)+I_{M2}(t)=0 \tag{3-10}$$

$$V_{IN1}(t)+V_{IN2}(t)=constant\ in\ transitions=V_{CM} \tag{3-11}$$

$$V_{OUT}(t)=-\frac{R_1}{2}(I_{M1}(t)+I_{M2}(t))+V_{CM} \tag{3-12}$$

Suppose transistor M2 is ON and VIN2 starts decreasing (M2 is in triode region), while VIN1 increases at the same time (M1 is still OFF).

$$M_1\ is\ off \rightarrow V_{OUT}(t)=-\frac{R_1}{2}I_{M2}(t)+V_{CM} \tag{3-13}$$

$$I_{M2}(t)=K'(V_{IN2}(t)-V_{th}) \tag{3-14}$$

$$V_{OUT}(t)=-\frac{R_1}{2}K'(V_{IN2}(t)-V_{th})+V_{CM}=-\frac{R_1}{2}K'V_{IN2}(t)+V_{CM}+V_{Cons} \tag{3-15}$$

where V_{th} is the threshold voltage. Figure 3.3 shows the simulation results of the Gaussian pulse generator and compares it with the mathematical derivation. As shown in (15), V_{OUT} follows the input signal when one of the transistors is in the triode region. As M_2 enters the saturation region, the linear relationship still holds due to the short channel device characteristics in this region. As V_{IN2} further decreases (V_{IN1} increases at the same time in transition), M_1 and M_2 both enter the sub-threshold region. Therefore, I_{M1} and I_{M2} are exponential functions of the input ramp signal. Based on (12) the output voltage can be written as follows:

$$V_{OUT}(t)=-\frac{R_1 I_{DS0}}{2}\left(e^{\frac{V_{IN1}(t)-V_{th}}{nV_T}}+e^{\frac{V_{IN2}(t)-V_{th}}{nV_T}}\right)+V_{CM} \tag{3-16}$$

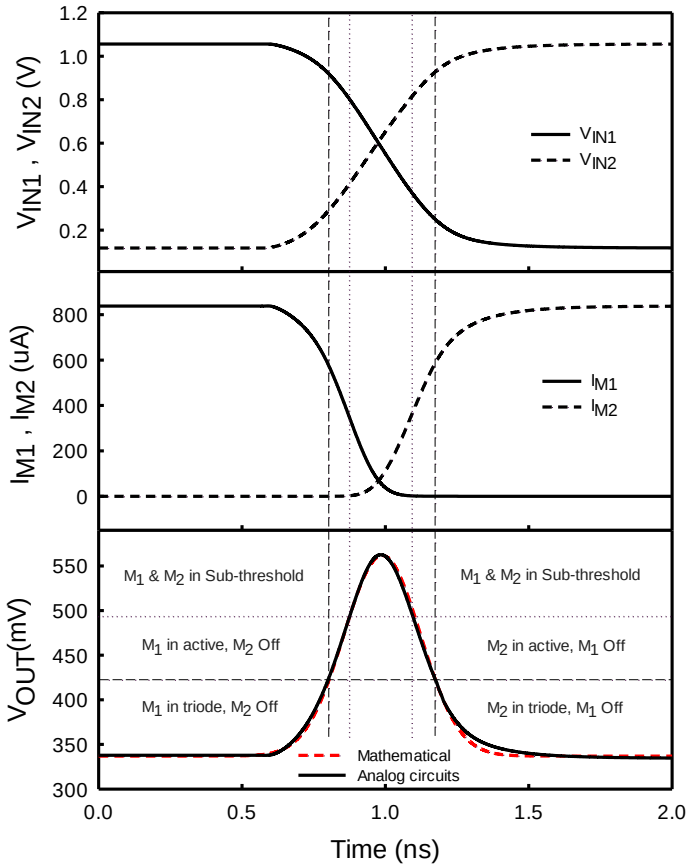


Figure 3.3. Voltage and current simulation of the Gaussian pulse generator circuit.

where n is the slope factor, I_{DS0} is the zero bias current, and V_T is the thermal voltage. I_{M1} and I_{M2} are shown in Figure 3.3 for all three regions as both V_{IN1} and V_{IN2} are changing. Due to the exponential characteristics of the circuit, the generated Gaussian pulse using CMOS analog circuits is in close agreement with the mathematical representation.

A Gaussian monocycle pulse is generated by taking the first derivative of the Gaussian pulse. Therefore, V_{OUT} is followed by a wideband differentiator to generate the

Gaussian monocycle pulse as shown in Figure 3.2. This differentiation is realized by an R-C circuit (R_3=300 Ω and C_1=80 fF for wide pulse and R_3=100 Ω and C_1=50 fF for narrow pulse). The differentiator is isolated from the previous stage by a pMOS source follower buffer (M_3). The only drawback of this configuration is the loss due to the passive high-pass R-C filter since small values of R_3 and C_1 are required for implementing a wideband differentiator.

III.3.1.2. Symmetric Differential Ramp Generation

The input voltages applied to the pulse generator circuit are two differential ramp voltages. On each falling and rising edge of the differential input signal, a Gaussian monocycle pulse is generated. The smaller the rising and falling times, the larger the bandwidth is and vice versa. The proposed UWB pulse is a combination of two pulses; to cover the entire UWB spectrum, the wide pulse covers 3.1-5.5 GHz, while the narrow pulse covers 5.5-10.6 GHz. Therefore, the wide and narrow monocycle pulses should have a base-band bandwidth of 2.4 GHz and 5.1 GHz, respectively. In order to generate these two pulses, the input ramp should have a specific rising and falling times. The rising and falling times can be expressed based on the pulse generator circuit parameters and the bandwidth that needs to be covered by the Gaussian monocycle pulse. The rising time, tr can then be found as follows (The complete derivation of the rising time formula has been addressed in Appendix A):

$$t_r = \frac{1}{\pi}\left(\frac{0.8(V_2 - V_1)}{nV_T K}\right) \times \sqrt{\frac{1}{BW_{Mono}\left(f_{-3dBH} + f_{-3dBL}\right)} Ln\left(\frac{f_{-3dBH}}{f_{-3dBL}}\right) \frac{R_1 I_{DS0} e^{\frac{V_{CM} - V_{th}}{nV_T}}}{2}} \quad (3\text{-}17)$$

where BW_{Mono} is the 3dB bandwidth of the Gaussian monocycle pulse, and f_{-3dBH} and f_{-3dBL} are the higher and the lower 3dB corner frequencies of the Gaussian monocycle pulse, respectively. For the higher band of UWB, t_r is calculated as follows:

$$BW_{Monocycle} = 5.9\ GHz - 0.8\ GHz = 5.1\ GHz \quad (3\text{-}18)$$

$$R_1 = 750\Omega, \quad \frac{R_1 I_{DS0} e^{\frac{V_{CM} - V_{th}}{nV_T}}}{2} = 10\ mV \quad (3\text{-}19)$$

$$n = 2.89, \quad V_T = 25\ mV, \quad K = 350\ mV \quad (3\text{-}20)$$

$$t_{r(Higher\ Band)} = 216\ pS \quad (3\text{-}21)$$

For the lower band of UWB, t_r is calculated as follows:

$$BW_{Monocycle} = 2.9\ GHz - 0.5\ GHz = 2.4\ GHz \quad (3\text{-}22)$$

$$R_1 = 600\Omega, \quad \frac{R_1 I_{DS0} e^{\frac{V_{CM} - V_{th}}{nV_T}}}{2} = 5\ mV \quad (3\text{-}23)$$

$$n = 2.89, \quad V_T = 25\ mV, \quad K = 250\ mV \quad (3\text{-}24)$$

$$t_{r(Lower\ Band)} = 393\ pS \quad (3\text{-}25)$$

Since the pulse generator circuit is sensitive to asymmetry at the differential input ramp, one of the challenges is providing fully symmetric differential input signals to the circuit with the same synchronized rising and falling times. The input ramp

generator should also be able to drive the pulse generator circuit. Figure 3.4 shows the implemented on-chip single-ended to differential converter. The input clock waveform is generated by the same reference frequency of the input data bit streams. The frequency of the input clock determines the maximum achievable data rate by the TX. The clock is converted to differential output through a differential inverter and a CML buffer after a chain of buffers. Back to back inverters synchronize the two pulses at the end. The last inverters are driving the pulse generation stage. The driver stage is a large inverter capable of sourcing and sinking large currents (~ 1 mA) for nMOS and pMOS transistors. In order to change the slope of the ramp signal, a 4-bit switched-capacitor bank is connected to the ramp generator output. By adjusting the capacitive load, the slope of the ramp and therefore the bandwidth of the UWB pulse can be set.

III.3.1.3. Differential Gaussian Monocycle Generator

Modulation schemes for IR-UWB TXs can be divided into on-off keying (OOK), pulse position modulation (PPM), and bi-phase modulation (BPM). Among these modulations, BPM has an advantage due to an inherent 3-dB increase between the constellation points, while it needs a coherent RX [52]. To be able to employ bi-phase modulation in the TX, the differential Gaussian monocycle pulse needs to be generated. For differential implementation of the Gaussian pulse, a pMOS version of the pulse generator is added to the circuit with an NMOS source follower buffer as shown in Figure 3.5. To provide maximum symmetry in the design, a capacitor is added in the nMOS version (C_D in Figure 3.5) to compensate for large parasitic of pMOS transistors.

Figure 3.6 shows the simulation results for differential wide and narrow Gaussian and Gaussian monocycle pulses. Figure 3.7 shows the simulated normalized spectrum at base-band for both wide and narrow Gaussian monocycle pulses.

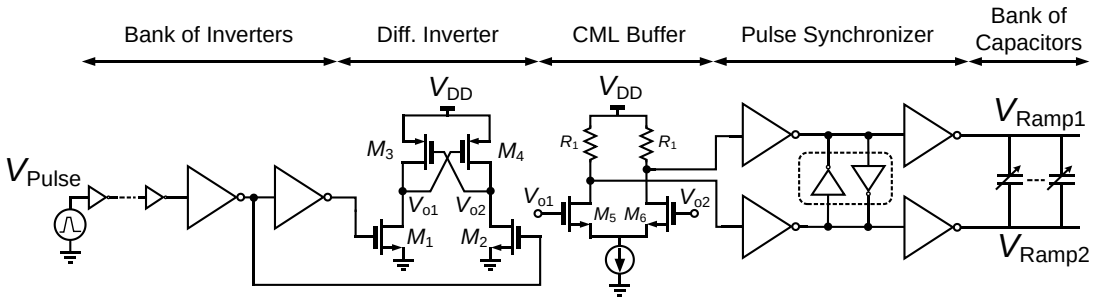


Figure 3.4. Gaussian monocycle pulse generation circuit.

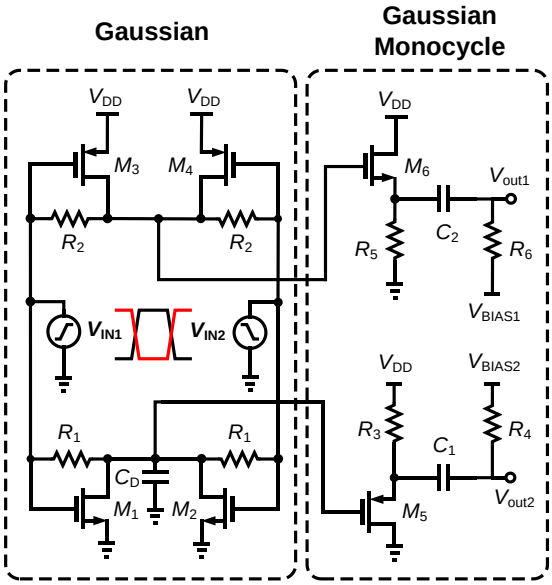


Figure 3.5. Differential implementation of the Gaussian and Gaussian monocycle pulse generator.

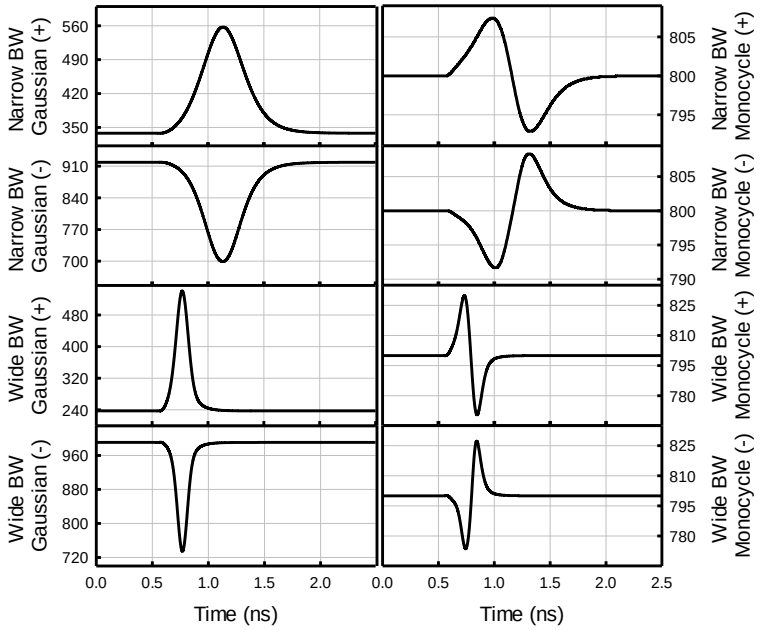


Figure 3.6. Simulation results of the differential Gaussian and Gaussian monocycle pulse generator (The vertical axis unit is mV).

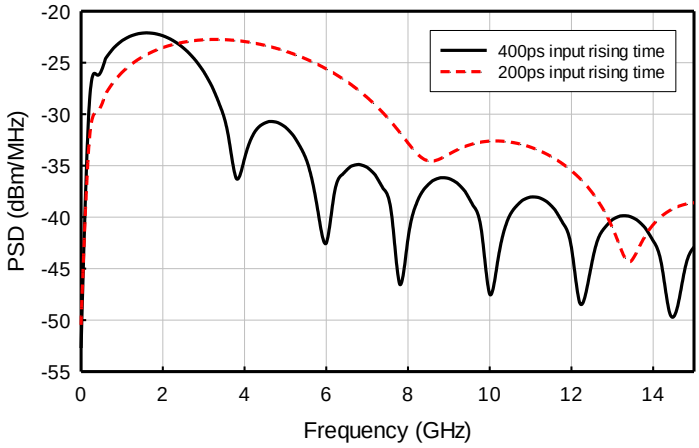
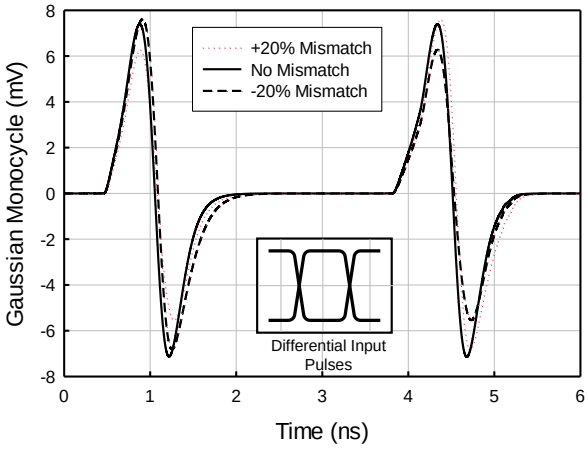
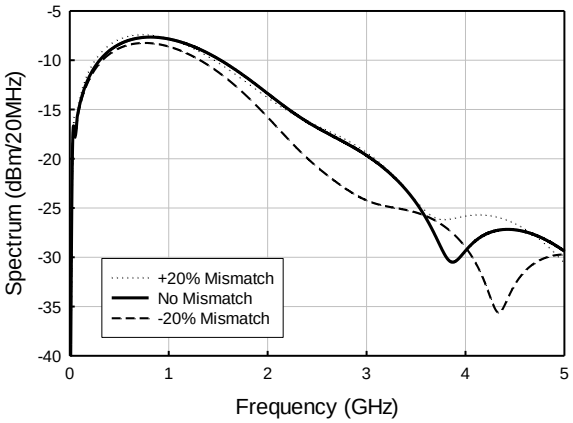


Figure 3.7. Frequency response of the two Gaussian monocycle pulses for each UWB band.



(a)



(b)

Figure 3.8. (a) Time response of the Gaussian monocycle pulse with mismatch between t_r and t_f. (b) Frequency response of the Gaussian monocycle pulse with mismatch between t_r and t_f.

III.3.1.4. Effect of Mismatch between t_r and t_f

When the rising and falling times of the input pulse are not the same, the shape of the output pulse deviates from a pure Gaussian pulse. Figure 3.8(a) shows the shape of

the pulse with and without the mismatch between the rising and falling times of the input pulse signal. The two pulses that are generated in the transitions are no longer symmetric with mismatches in the rising and falling times. If the shape of the Gaussian monocycle pulse is preserved, the mismatch does not have major effect on the output pulse spectrum. By simulation, the change in the output spectrum (Figure 3.8(b)) can be tolerated up to 20% mismatch between t_r and t_f.

III.3.1.5. Multiplexer and VGA

In IR-UWB TX, the pulse repetition rate (PRR) is typically larger than the actual data rate, since multiple pulses are required to build up the data in the analog correlator-based RX for each transmitting bit. However, for different PRRs the output power changes. To keep the power below the FCC spectral mask, the TX should have gain control capability. To meet the FCC mask in all PRRs. two variable gain amplifies (VGAs) are added in the pulse path. One VGA is added to the transmission path of the wide pulse, and one is added to the transmission path of the narrow pulse. A differential Gaussian monocycle pulse is applied to each VGA stage with a 4 bit gain controllability. The VGA is a differential circuit with source degeneration resistor banks for gain control (0-15 dB) as shown in Figure 3.9(a). The nonlinearities of the VGA and mixer should not degrade the level of the generated notch at the output pulse spectrum. Therefore, the two-tone linearity test has been performed, in which the resulted IM_3 level should be 10 dB below the notch level. Based on this test, the linearity of the VGA is optimized for an IIP3 of 5 dBm at maximum gain.

To be able to transmit bi-phase modulation data, four 2×1 multiplexer gates have been employed prior to VGA stage. The multiplexer changes the polarity of the signal applied to the VGA based on the input data as illustrated in Figure 3.9(b). Figure 3.10 shows the VGA outputs for the narrow pulse as the data changes from +1 to −1. The same result is valid for the wide pulse.

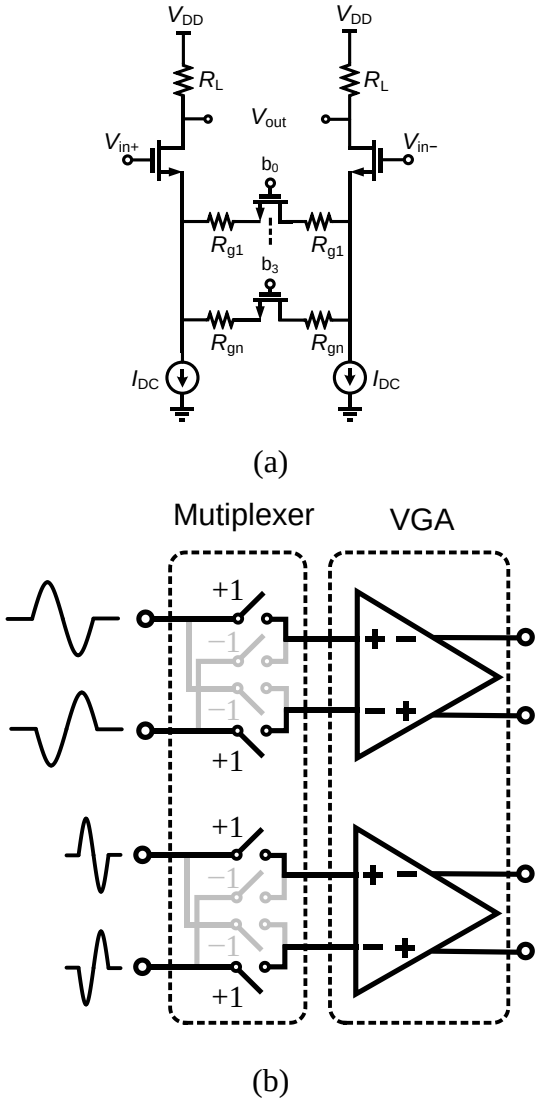


Figure 3.9. (a) The schematic of the variable gain amplifier. (b) Bi-phase modulation implementation using a multiplexer.

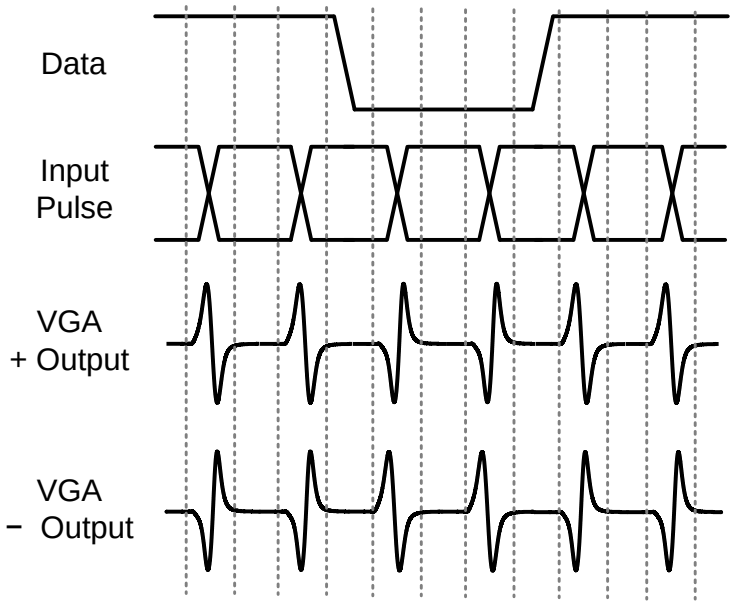


Figure 3.10. VGA outputs for different DATA inputs.

III.3.2. Up-Conversion and Band-Pass Filters

Figure 3.11 shows the block diagram of the entire UWB TX. As shown in the figure, up-conversion mixers are needed for each transmission path to up-convert the Gaussian monocycle pulses to the frequency of the IEEE 802.11a system. The UWB mixer design has two major design challenges, 1) the LO-output feed-through, 2) linearity of the mixer. Since the LO frequency is the frequency of the NB system, any LO feed-through appears at the notch frequency and degrades the notch level. On the other hand, due to the ultra-wide bandwidth of the pulse, any second or third order non-linearity in the mixer will result in out of band transmission. In typical Gilbert cell mixers, the most important parameter for the LO to output feed-through is the DC current mismatch in the trans-conductance stage, which results in a large LO-output

feed-through. The feed-through can be improved by AC-coupling the switching and the trans-conductance stages. Figure 3.12 shows the schematic of the UWB mixer. The DC bias of both G_m and switching stages are isolated using decoupling capacitor C_1. The Gm stage is a self-biased inverter. The trans-conductance of the stage is increased by adding the pMOS transistor, which results in a larger gain. In addition, combining both nMOS and pMOS transistors currents at the output cancels out the second order distortion of the Gm stage results in much better linearity.

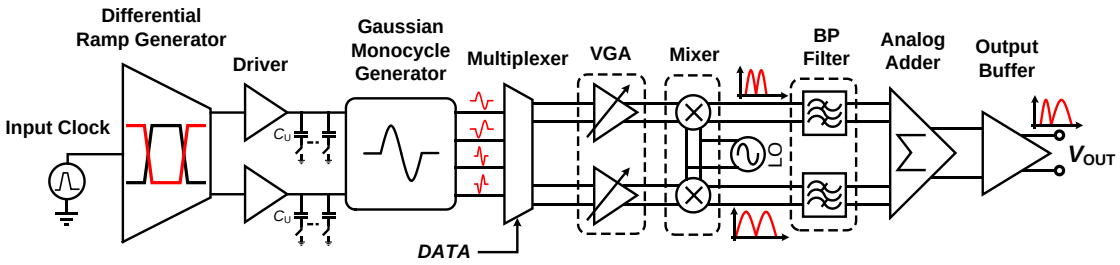


Figure 3.11. The block diagram of the UWB transmitter, the higher path generates the wide pulse for the lower UWB side-band while the lower path generates the narrow pulse for the higher UWB side-band.

Mismatch in the transistors of the switching stages also results in LO-output feed-through. To compensate for the mismatches, two pairs of constant (I_{of1} and I_{of3}) and variable current sources (I_{of2} and I_{of4}) are added to the mixer as shown in Figure 3.12. For the designed UWB mixer, the effect of threshold voltage mismatch in the switching transistors (M_3) on the LO to output feed-through is shown in Figure 3.13. This feed

through is calibrated by tuning the variable currents, which improves the LO to output feed-through by more than 20 dB for less than 12% threshold voltage mismatch.

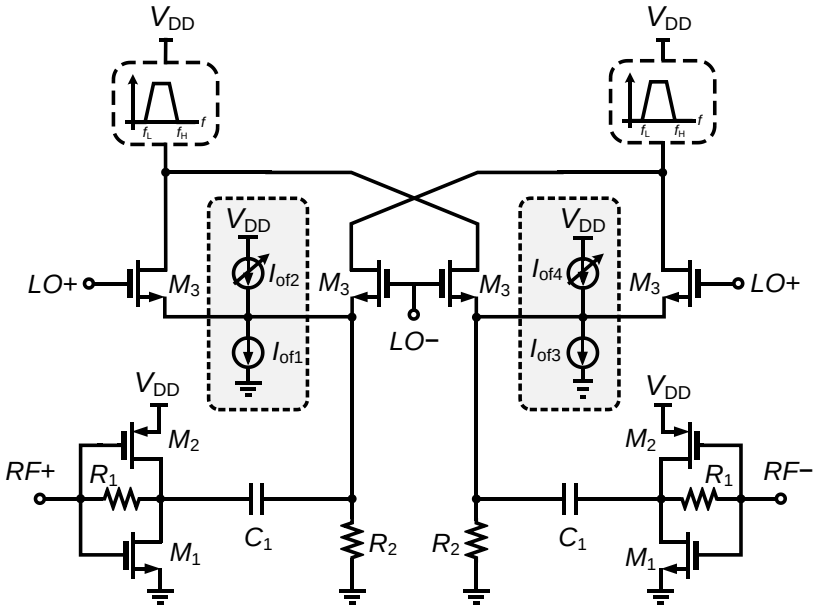


Figure 3.12. The designed UWB mixer with the band-pass filter load.

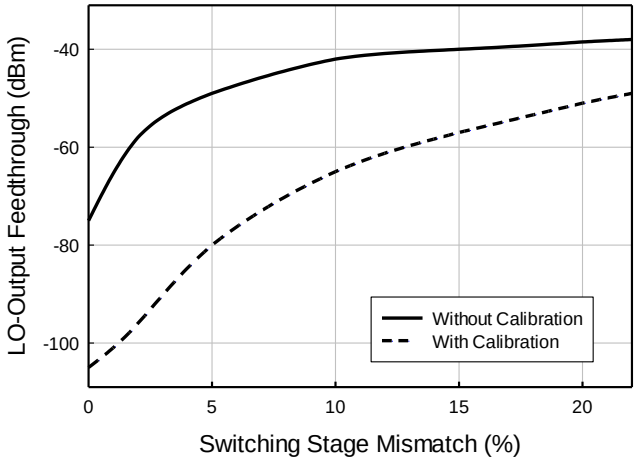
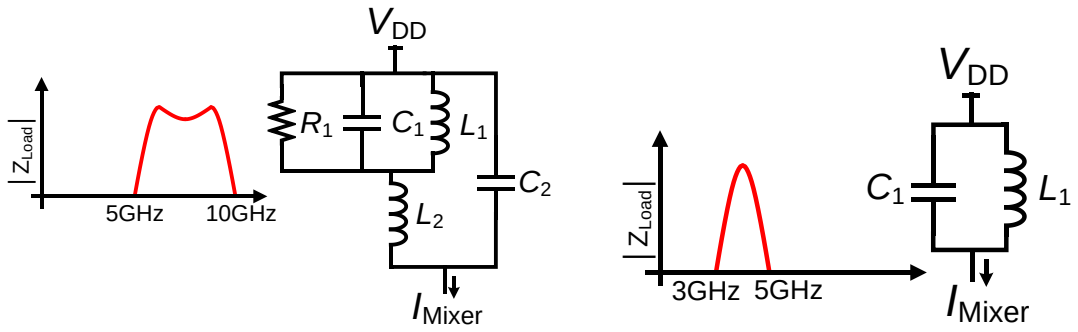


Figure 3.13. Effect of threshold voltage mismatch in the switching stage of the proposed mixer on the LO-Output feed-through before and after calibration.



(a) (b)

Figure 3. 14. (a) The mixer load for higher band filtering. (b) The mixer load for lower band filtering.

By adding two band-pass filters in the load of each mixer, lower and higher band of the wide and narrow UWB pulses are being selected, respectively. Figure 3. 14 shows the output load for the mixer in the higher (narrow pulse), and the lower band (wide pulse). In order to implement a band-pass passive filter with 4 GHz bandwidth and acceptable out-of-band rejection (>20 dB) and minimum number of on-chip inductors, the topology of Figure 3. 14(a) has been chosen [66]. To avoid complexity, resistor R_1 is not considered in calculations. The load impedance can then be calculated as:

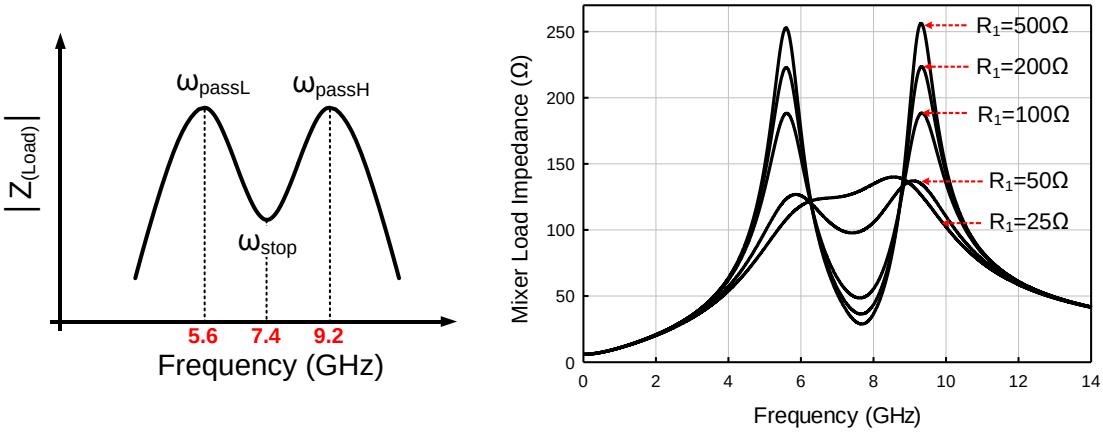
$$Z_{Load}(s)=\frac{s(1+s^2.L_1/\!/L_2.C_1)}{s^4L_1L_2C_1C_2+s^2(L_1C_1+L_1C_2+L_2C_2)+1} \quad (3\text{-}26)$$

As shown in Figure 3.15(a), $|Z_{Load}(j\omega)|$ has double peaks with a notch in the middle. For fully symmetric impedance response of the filter, the following relations should hold:

$$f_{Stop} = \frac{1}{2\pi\sqrt{(L_1 /\!/ L_2)C_1}} \tag{3-27}$$

$$f_{PassL,\ H} = \frac{1}{4\pi\sqrt{(L_1+L_2)C_2}}\left(\sqrt{\frac{L_1}{L_2}+4} \pm \sqrt{\frac{L_1}{L_2}}\right) \tag{3-28}$$

To cover the desired range of 5-10 GHz, the peaks are placed at 5.6 and 9.2 GHz, respectively, while the notch is at 7.4 GHz. In order to compensate for the capacitive parasitics at higher frequencies, the filter impedance at f_{passH} is designed to be larger. To realize a flat-band filter response and minimize the effect of the stop-band notch, resistor R_1 has been added to the filter to decrease the quality factor (Q) of the notch and the resonators simultaneously. Figure 3.15(b) shows the load impedance for different values of R_1. By selecting the proper value of R1 (50Ω), an almost flat band-pass filter can be realized.



(a) (b)

Figure 3.15. (a) The Mixer higher band load impedance. (b) Effect of R1 in the peaking of the mixer load impedance.

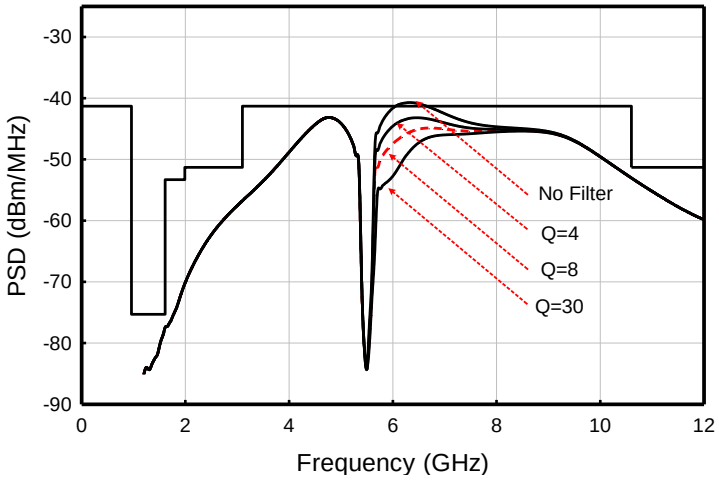


Figure 3.16. Effect of Q of the lower band filter on the transmitted power.

The lower band filter is realized by employing a simple LC tank centered at 4.5 GHz (Figure 3. 14(b)). The simulated normalized output spectrum of the pulse has been shown in Figure 3.16 for different values of the Q for the LC tank. Without the LC tank the output pulse spectrum is not satisfying the FCC mask, but an LC tank with a Q>5 is enough to keep the spectrum below the FCC mask. The values of the band-pass filter components are summarized in Table 3. 1 In order to further filter the low frequency components, all the signals are AC-coupled to the next stage.

Table 3. 1. The element values for low-band and high-band filters inside the mixer.

Low-Band		**High-Band**				
C_1	**L_1**	**C_1**	**L_1**	**R_1**	**C_2**	**L_2**
0.65 pF	1.2 nH	2 pF	300 pH	50 Ω	400 fF	1.1 nH

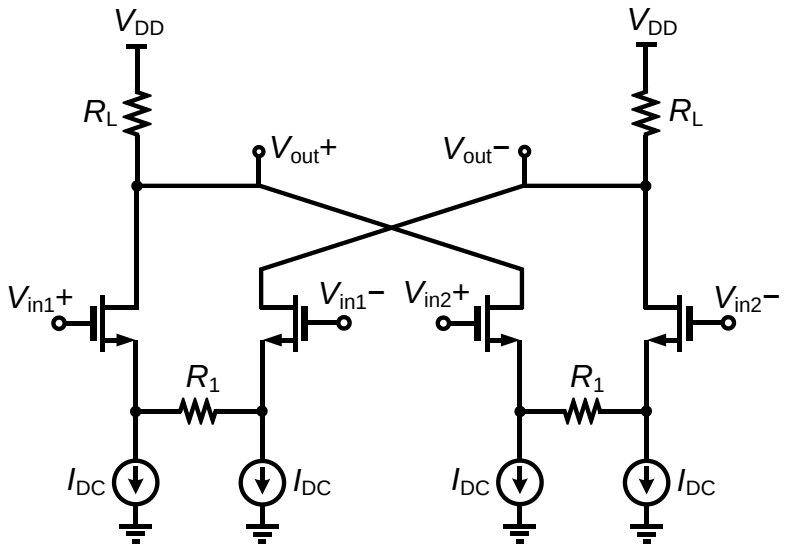


Figure 3.17. The schematic of the analog adder.

III.3.3. Output Stage

The signals in the two paths are combined together by adding the currents of two differential stages as shown in Figure 3.17. Source degeneration is used in the differential pair to increase the linearity of the stage. Since LO feed-through at the output of the mixer is a common mode signal, small devices have been used to decrease parasitic and, therefore, increase the common mode rejection at high frequencies. The UWB pulse is then applied to the output stage buffer to drive the 50-Ω output antenna. A cascode stage has been used to protect the transistors from breakdown as the drain is connected to the output pads. Since the signals have high frequency components up to 10 GHz, each routing in the layout has been shielded using ground strips. The layout should be perfectly symmetric to achieve maximum common mode rejection, otherwise the

common mode LO signal will appear as a differential output and cannot be compensated by the offset calibration in the mixer. Figure 3.18 shows the simulated output pulse for both +1, and −1 input data. As shown, the two pulses are 180 degrees out of phase, which is suitable for bi-phase modulation.

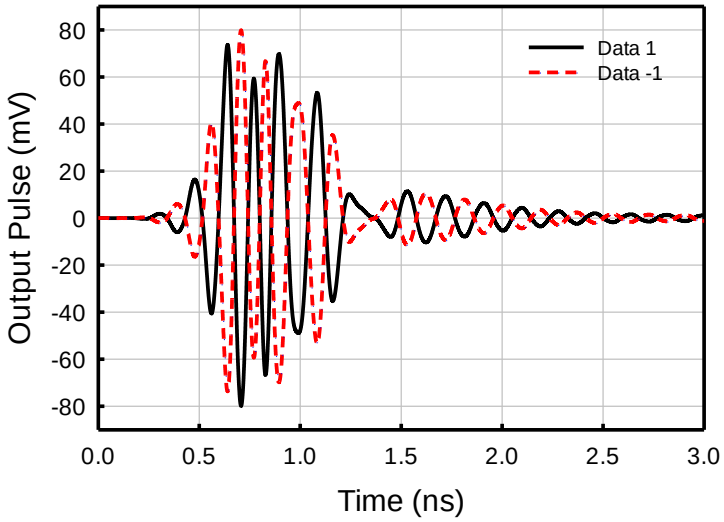


Figure 3.18. Time domain simulation results of the output pulse for data 1, and -1.

III.3.4. Low Data Rate, Low Power Operation

Due to the complexity of the system (notch implementation), the current consumption for low pulse rates is higher than typical IR-UWB systems. One remedy to reduce the power consumption is to make the current consumption a function of the pulse rate as shown in Figure 3.19. By applying the pulse (A), and a delayed version of it (B: output of chain of inverters in symmetric pulse generation block) to an XOR stage, a short pulse (C) will be generated in each pulse transitions (during which the UWB pulse

is generated). For lower pulse rates (below 100 Mpps), by employing this pulse to turn ON and OFF some of the blocks inside the transmitter, the current consumption can be significantly reduced. These blocks include Gm stage of the mixer, the VGA, the analog adder and the output buffer. The blocks are turned OFF while there is no transition, and no pulse is generated. As an example, the current consumption of the TX is reduced to 3 mA at 10 Mpps pulse rate. For higher than 100 Mpps, this unit is disabled because of the short time available to turn ON and OFF the current sources.

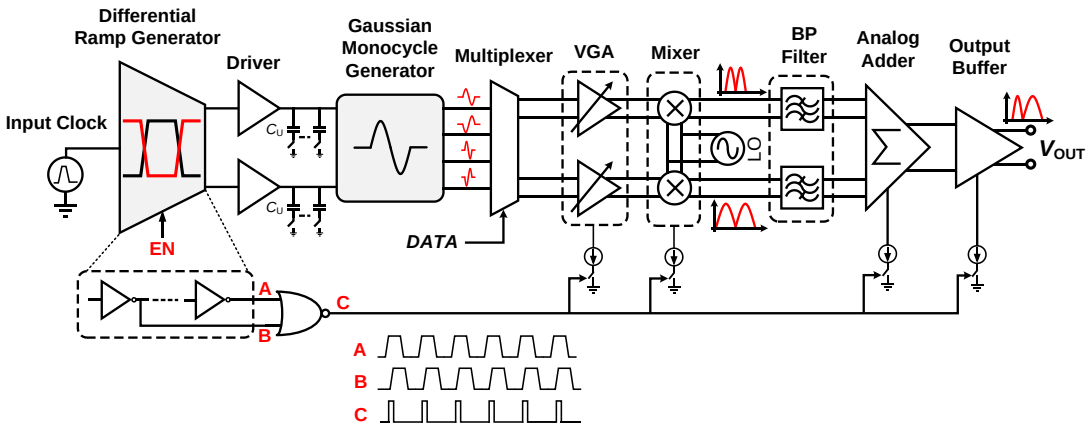


Figure 3.19. The transmitter block diagram with the proposed circuit to reduce the current consumption in low pulse rates.

III.4. Measurement Results

The UWB TX has been fully fabricated in 90nm CMOS technology. The die is semi-packaged using 48 QFN package and RF probes are landed on the output pads to eliminate the effect of bond-wire inductance and package parasitics. The die micrograph

is shown in Figure 3.20. The die area is 1380μm × 1380μm including the wire-bonding pads.

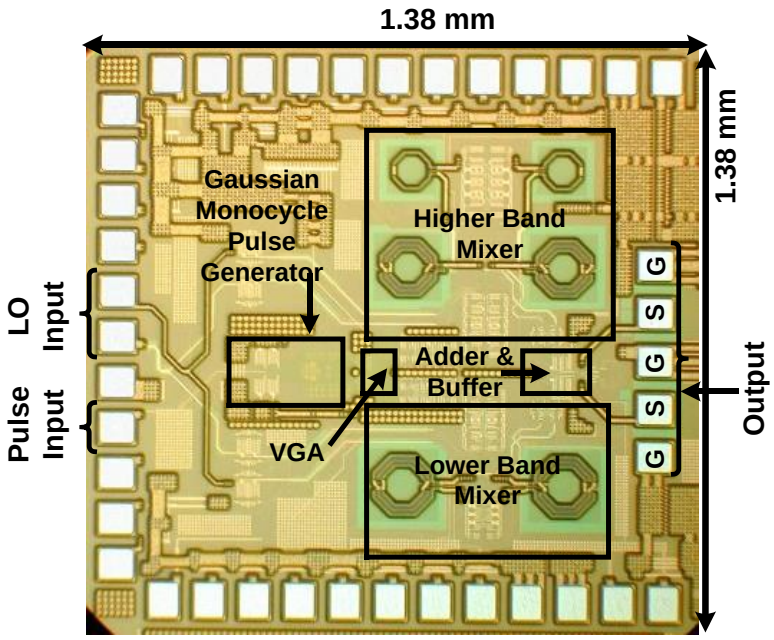


Figure 3.20. The die micrograph of the fabricated UWB TX.

A single-ended pulse is applied to the input of the TX in which a differential pulse is generated in each transition. The differential LO is an off-chip signal generator (Agilent E8267D PSG Vector Signal Generator, and Balun) at 5.5 GHz frequency to up-convert the base-band pulse to the frequency of the NB system. At the TX output, the differential pulse is converted to single-ended by a wideband off-chip balun. Figure 3.21 shows the spectrum of the pulse measured by an Agilent E4446A Spectrum Analyzer for 100Mpps (50MHz input frequency) at 1MHz resolution bandwidth. The gain of the VGA is adjusted to keep the transmitted output power below the FCC mask. As shown, the measurements are in close agreements with the simulated spectrum. The bandwidth

of the pulse is smaller than the simulation because of the extra parasitics on the routings (not showed up in the post-layout simulations) and the process variations on the band-pass filters at the mixer output. A 30dB notch depth is achieved at the frequency of the NB system, which is limited by the LO-output feed-through. The frequency of the notch can be fine-tuned by changing the frequency of the LO signal. The maximum pulse rate of the TX is measured by increasing the input pulse frequency until the notch depth is degraded from 30 dB. At 200 MHz, which corresponds to 400 Mpulse/s, the depth of the notch starts to degrade. At this pulse rate, in order to satisfy the FCC mask, in addition to set the VGA gain to minimum (0 dB), the supply voltage of the driver for the Gaussian pulse generator circuit is lowered to 1V to further decrease the amplitude of a single UWB pulse.

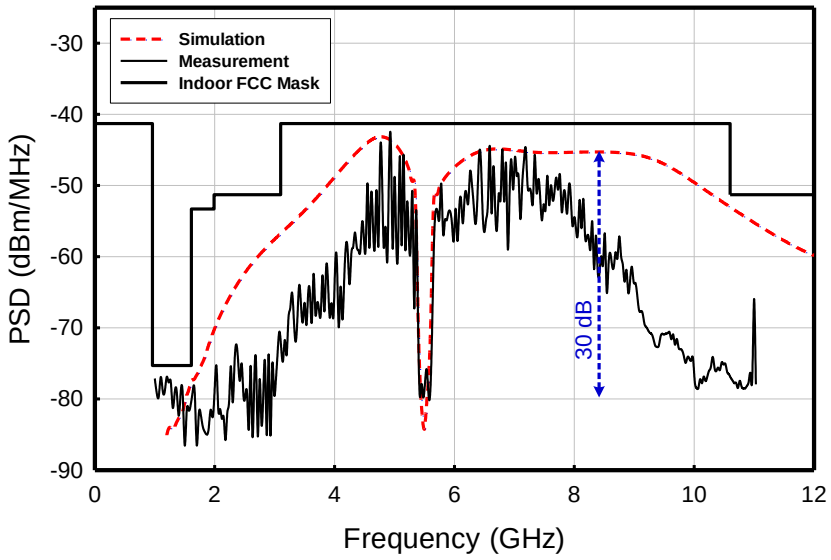
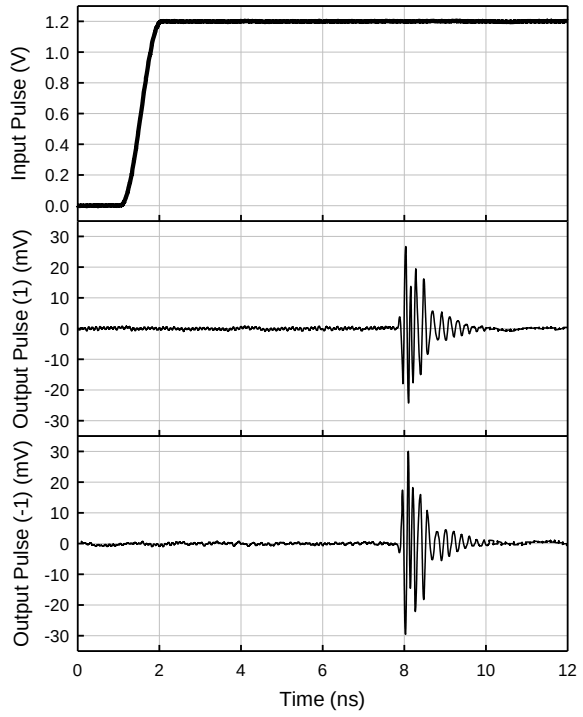


Figure 3.21. The simulated and measured spectrum of the UWB pulse (100 Mpps), LO-output feed-through has been calibrated.

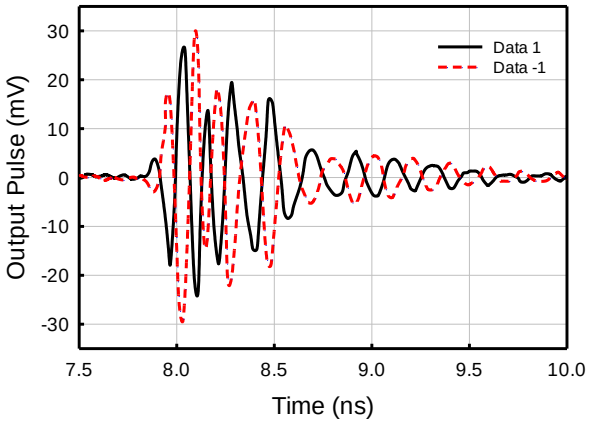
The LO-output feed-through of the TX, which appears at the frequency of the notch, is -55 dBm without any calibration in the mixer. By calibrating the currents I_{of2} and I_{of4}, LO feed-through is decreased by 21 dB (-78 dBm). There is another feed-through to the output of the TX, which is at the second harmonic of the LO (11GHz in this case). The second harmonic of the LO is a common mode signal at the output of each mixer, which due to the mismatches in the differential stages and especially the off-chip balun appears at the output. The second harmonic feed-through in the measurements was -45 dBm. The reason for the large second-harmonic feed-through is the mismatch in the off-chip balun (10% mismatch at 11GHz) employed to convert the differential output pulse to single ended. During the measurements, an off-chip filter with cut off frequency of 10 GHz is used to decrease the feed-through level to -65 dBm.

Figure 3.22(a) shows the time domain measurement of the TX +1, and −1 data. The output pulse is measured by an Agilent DSA91304A oscilloscope. As shown, a UWB pulse is generated on each rising and falling edges of the input pulse. Figure 3.22(b) shows close caption of the measured output pulses for +1, and −1 data. The output peak amplitude of the pulse is attenuated to 30 mV compared to simulation (~ 80 mV) because of the loss inside the off-chip balun and the RF cables. The total current consumption of the entire TX (without the LO generation) is 22 mA, and Table 3.2 summarize the current consumption of each block. At maximum pulse rate of 400 Mpulse/s, the TX has energy of 65 pJ per pulse. In Table 3.3, the performance of the proposed TX is compared with recently reported state of the art. Based on the comparison, this work has a superior performance in notch implementation, and presents

a very low interference power of -78 dBm/MHz at the frequency of the IEEE 802.11a system while providing considerably large pulse bandwidth (5.5 GHz).



(a)



(b)

Figure 3.22. The time domain measurements of the UWB pulse for data +1 and data −1.

(b) The close caption of the bi-phase modulation for data +1 and −1.

Table 3.2. Current consumption of each block inside the TX for the maximum pulse rate of 400 Mpulse/s.

Transmitter Blocks	Current Consumption
Input Ramp Generator	1 mA
Gaussian Monocycle Generator	2 mA
Mixer 1 & 2	8 mA
VGA	3 mA
Analog Adder	3 mA
Output Buffer	5 mA
Total	22 mA

In addition, the RX sensitivity of an 802.11a system 1 m away from the designed UWB TX can be found as follows:

$$For\ 1m \Rightarrow P_{Sen} = 10\log\left(10^{-11.4} + 10^{(-78-50)/10}\right) + 10\log(NF) + 10\log(BW) + SNR = -69.82\ dBm \quad (3\text{-}29)$$

Therefore, the proposed UWB TX degrades the sensitivity of the NB RX less than 0.5 dBm when r=1m, which is improved by 22 dB compared to the sensitivity in (4).

Table 3.3. Performance summary and comparison of the proposed UWB architecture compared to the state of the art transmitters.

	Technology	Power Supply (V)	Center Freq. (GHz)	Bandwidth (GHz)	Maximum Data rate	Power Cons. (mW)	Energy per Pulse	Modulation	Notch Implementation	Transmitter Power @ 5.5 GHz WiFi [1]
[47] ISSCC 07	0.18 µm CMOS	1.8	6	4	800 Mpulse/s	99	123 pJ/Pulse	DS	YES (25 dB)	>-65 dBm/MHz
[59] JSSC 07	0.18 µm CMOS	2.2	4.05	1.4	60 Mpulse/s	29.7	495 pJ/Pulse	DBPSK	NO	>-65 dBm/MHz
[53] JSSC 08	0.18 µm CMOS	1.8	3.6	4	1.16 Gpulse/s	21.6	19 pJ/Pulse	-	NO	>-53 dBm/MHz
[48] JSSC 08	90 nm CMOS	1	6	6	1.8 Gpulse/s	227	126.1 pJ/Pulse	BPSK+ PPM	NO	>-52 dBm/MHz
[46] JSSC 09	0.18 µm CMOS	1.8-2.2	8	4	750 Mpulse/s	24	12 pJ/Pulse	BPSK	NO	>-60 dBm/MHz
[44] JSSC 09	90 nm CMOS	1	3 to 5	<0.5	15.6 Mpulse/s	0.123	17.5 pJ/Pulse	BPSK+ PPM	NO	>-82 dBm/MHz
[49] MTT 10	0.13 µm CMOS	1.2	6.5	6.8	100 Mpulse/s	3.84	9 pJ/pulse	OOK	NO	>-44 dBm/MHz
This Work	90 nm CMOS	1.2	6.5	5.5	400 Mpulse/s	26.4 [3]	65 pJ/Pulse [3]	BPSK	YES (30 dB)	-78 dBm/MHz

[1] The numbers are estimated based on the reported EIRP.

[2] For reported bands close to 5GHz the interference level goes up to -76 dBm/MHz.

[3] Does not include LO generator.

III.5. Summary

A novel analog approach has been proposed to solve the coexistence problem of UWB with NB systems (i.e. 802.11a). The fully integrated UWB TX generates an analog pulse that features a tunable notch with 30dB attenuation at the frequency of the NB system. Therefore, the interference power level caused by the UWB TX is lowered down to -78 dBm/MHz, which is 20 dB lower than typical Gaussian pulse generator reported in the literature. A method has been employed to cancel out the LO to output feed-through which improves the isolation by more than 20 dB. The UWB pulse has a 5.5 GHz bandwidth and can operate with a maximum pulse rate of 400 Mpulse/s and energy of 65 pJ per pulse.

CHAPTER IV

LOW NOISE LINEAR WIDEBAND RECEIVER FOR 4G LTE AND CARRIER AGGREGATION APPLICATIONS*

IV.1. Introduction

Wideband receivers (WB RXs) have recently been the focus of industry and state of the art researches for two main reasons. A) The increasing demand for higher data rates pushes industry to use a larger band of operation for 4G LTE systems. Furthermore as shown in Figure 4.1 the wireless RX operates simultaneously with a transmitter (TX) within the same communication device (frequency division multiplex (FDD) systems). Because of the limited isolation between TX and RX in the duplexer (55dB), there is a strong TX leakage (-30 dBm) at the RX input. Different techniques are proposed in the literature to attenuate TX leakage inside the transceiver [67]-[69]. The TX leakage and SNR requirements for 4G LTE, puts stringent linearity and noise requirements (NF<2dB, IIP3>5dBm) on the RX. Because of the superior performance of narrowband (NB) RXs (both in NF and linearity), the entire band of operation is covered with multiple NB RXs. Each NB RX employs off-chip components to provide high-Q selectivity which increases the total cost and area. While WB RXs are very attractive to be employed in high performance systems, due to worse noise and linearity performance

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of current WB RXs, replacing all the NB RXs with a single or two WB counterparts is not feasible. In carrier aggregation scenarios, in which the receiver requires to have more than one downlink paths [70]-[72], the number of NB RXs increases by two or three times. Therefore a high performance wideband receiver with similar power consumption to NB counterparts can result in a considerable saving of chip and board area and cost.

B) The other area of interest for WB RXs, are the saw-less RXs for cognitive and software defined radios. Cognitive radio enables its users to efficiently use the unoccupied spectrum without any data collision with licensed users [73]. With no off-chip filtering prior to the front-end, the major challenge in cognitive radios, are the strong nearby interferers that can severely degrade the receiver SNR. Comparing to 4G LTE, the NF requirements (NF<7dB) are relaxed, while the linearity requirements are considerably more challenging (IIP3>15dBm).

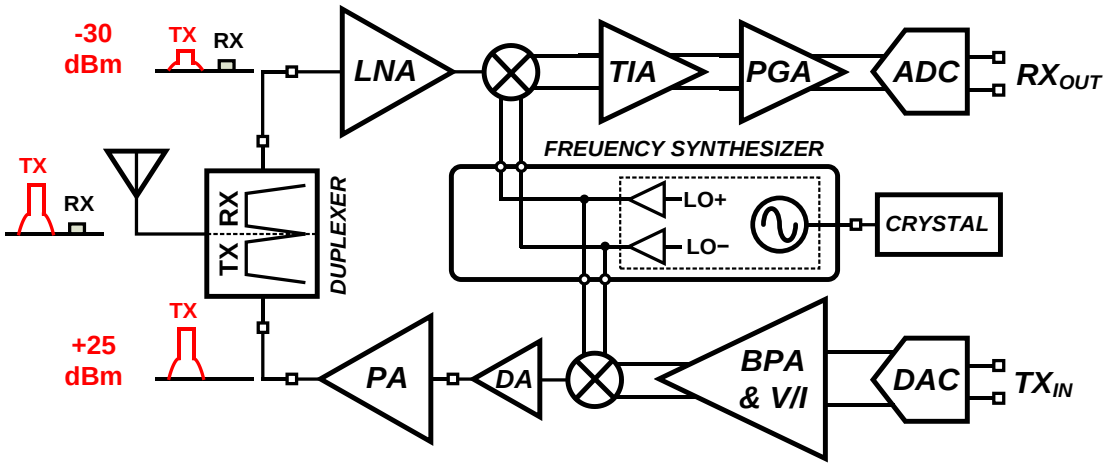


Figure 4.1. TX leakage in the FDD transceiver architecture.

The common demand in both types of WB RXs, is the ability to tolerate strong blockers. One remedy to tolerate strong blockers is to minimize the RF front-end (RFFE) gain, and keep the input voltage swing across the frequency band of operation as small as possible. The mixer first architectures [74]-[77] are an example of these kind of front-ends, the small switch resistance of the mixer keeps the input voltage swing small for close-by frequency offsets. The major drawback is the inferior noise performance due to loss in the front end stage (2-3 dB loss in non-overlapping passive mixers). Another solution to poor blocker rejection in such RFFE, is to employ a tunable filter (on-chip or off-chip) at the RX that sufficiently attenuates blockers before the mixer or LNA. such a blocker filters can be implemented as a Q-enhanced tunable LC filter [78]-[79], but it is very sensitive to process variations, and may require factory Calibration and process monitor. In [80] passive mixers has been used to feedback the baseband output to the LNA input, which eventually provides input matching, while the linearity is degraded because of the two times blockers voltage swing at the LNA input. In [81] an active cancellation technique has been used to cancel out of blockers after the LNA. Due to the large bandwidth requirements in the designed TIA, the noise performance of the receiver is limited to 7dB.

Another Possible choice to attenuate blockers is band-pass N-path filters [82]-[85]. The frequency response of these filers are automatically centered at the LO frequency, and are capable of providing high-Q filers. In [86] an N-path filter has been used to attenuate blockers prior to the LNA. Due to the noise from the N-path filter, the RX NF is limited to 3dB. Therefore, the RX is not suitable for type A receivers. A

frequency translated noise cancelling technique has been employed in [87]-[88] to cancel the noise of the N-path filter which is employed as a matching network prior to the LNA. In spite of using an N-path filter at the input, this technique does not provide a very good rejection at the input since most of the antenna matching is provided by the switch resistance. While the RX proposed by Murphy is well suited for type B receivers, it cannot be employed in 4G LTE systems because of the following drawbacks: 1) Due to the mismatch in the passive mixer switches, there is a strong LO leakage from the N-path filter to the antenna (>-69 dBm), which must be less than -76dBm for 3GPP2 radios. 2) By doubling the number of the mixers and the TIAs, the current consumption from the LO distribution, mixer buffers and the baseband is increased by at least 15 mA, which is an extra current usage comparing to the NB RX counterparts. Other reported WB RXs [89]-[91] are all using passive mixers either to lower the voltage swing at the LNA output or to reject blockers by providing a high Q band filter. The performance is still not comparable to high performance NB RXs (with the same current consumption), or they violate the 3GPP2 radios standard.

In this chapter, two RF and baseband blocker filtering techniques have been proposed employing high-Q N-path filters to improve RX linearity. Based on the proposed technique a WB RX has been implemented. A very low noise, linear WB RX is designed for 4G LTE systems. The noise from the N-path filter is cancelled with minimum increase in power consumption. New mixer architecture is employed to further attenuate blockers in the two WB RXs. To achieve a very good linearity for type B receivers, a particular low-impedance TIA has been designed. Section II discuss the RF

blocker filtering, and the N-path noise cancelling technique. The baseband blocker filtering technique and the mixer architecture is explained in section III. The TIA design for type B RX, and the remaining blocks in the RX is discussed in section IV. The measurement results are shown in section V, and the summary concludes the chapter.

IV.2. Receiver Design

One of the major challenges in 4G LTE systems is the TX leakage at the RX input. Considering +25 dBm power at the PA output, and 55dB Duplexer isolation, the leakage at the RX input is -30dBm. The leakage affects both RX linearity and NF. Because of the high SNR requirements in 4G LTE systems, and the TX leakage, the linearity and NF specifications are very challenging. Although 4G LTE band of operation is very wide, to satisfy the specs, industry is forced to employ many narrow-band receivers to cover the bands of interest as it is shown in Figure 4.2. Due to employing narrow-band LNA architectures, each RX is required to use multiple off-chip elements. As a result, the area and the cost are significantly increasing. Therefore it is very attractive to replace all the narrowband RXs with a single or two wideband counterparts to eliminate the drawbacks. Current performance of 4G LTE systems with narrowband implementation is 1.7 dB NF and +3dBm IIP3. It is very challenging to design a wideband receiver that can achieve such a good performance while meeting 3GPP2 standard requirements.

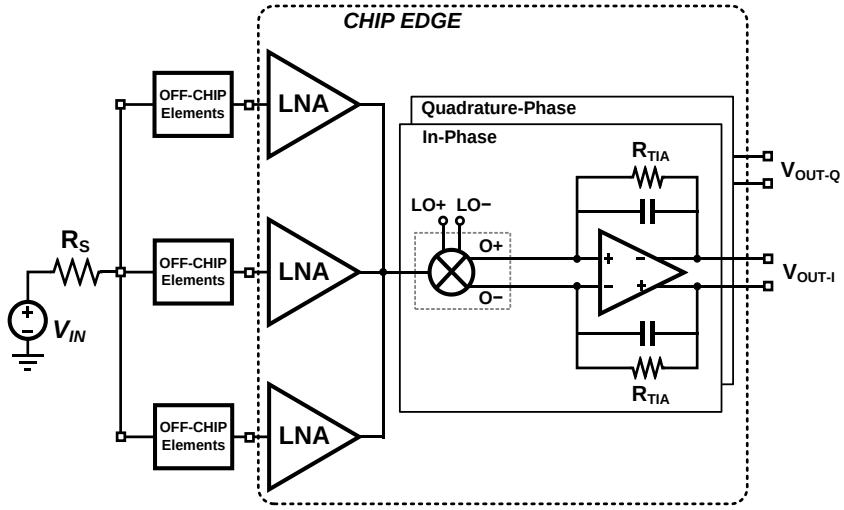


Figure 4.2. Narrow band implementation of current 4G LTE receivers.

Figure 4.3 shows the blocks diagram of the typical wideband receiver. The LNA, which provided the matching for the duplexer and antenna, the passive mixer (with non-overlapping LOs), and the TIA at the input which converts the current to output voltage. Passive mixers with non-overlapping LOs, improved the receiver NF since the I and Q switches are not ON at the same time. Also since there is no DC current, there is no 1/f noise contribution from the mixer, which further improves NF. On the hand non-overlapping LOs, minimize the non-linearity feed-though from the I baseband to the Q baseband and vice versa. Employing the TIA, provides a low impedance to the mixer, and later on for the LNA, the blocker voltage swing is smaller in all receiver nodes, and much better linearity can be achieved.

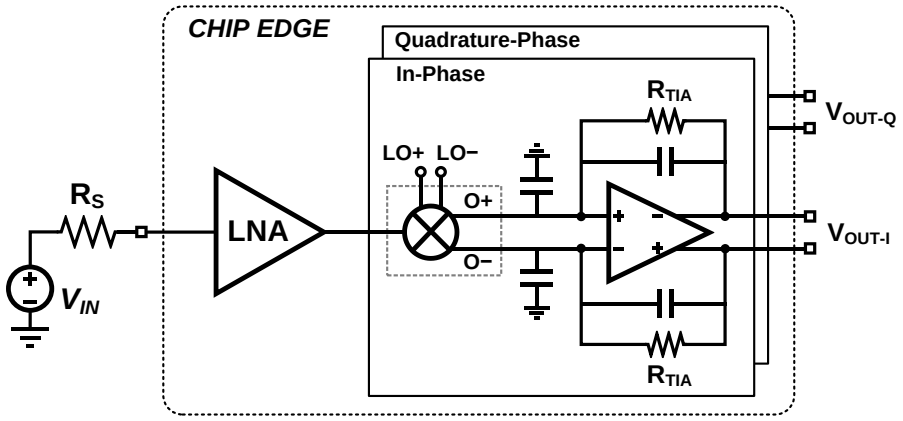


Figure 4.3. Typical architecture of a wideband receiver.

LNA is the most important part of the receiver, which determines the minimum limit for the linearity and NF. One of the advantages of narrowband receivers is the option for choosing high performance source degenerated LNA as shown in Figure 4.4. Because of the noise-less matching, and the passive voltage gain through the LC match, this LNA can achieve a superior NF and linearity. The challenging design for wideband LNAs, is providing input matching with enough voltage gain, and very good linearity despite no blocker rejection at the input. Figure 4.5 shows the wideband LNA architecture that is chosen as a starting point. Because of multiple trans-conductance through both NMOS and PMOS transistors, the LNA can achieve a very good NF. Adding up NMOS and PMOS currents at the output also cancels out the second order non-linearity of the transistors, and can significantly improve IIP2. One of the key points in designing LNAs is the size of the transistors. The width and length of the transistors should be optimized to achieve the minimum NF. On the hand, based on the LNA current, the biasing of the transistors should be optimized for maximum linearity (IIP3

and IIP2) achievement. The chosen size of the transistors is shown in Table 4.1 and Table 4.2 summarizes the performance of the wideband LNA. The LNA has a very good NF, and linearity. The matching is provided through resistive feedback.

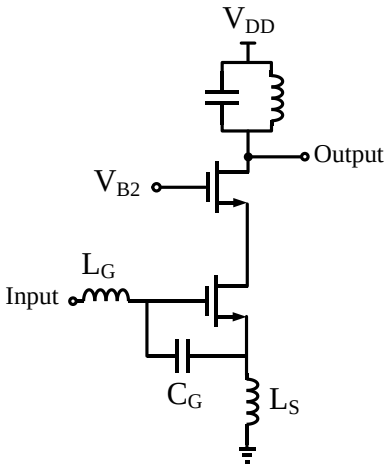


Figure 4.4. Inductive source degenerated LNA employed in narrow-band receivers.

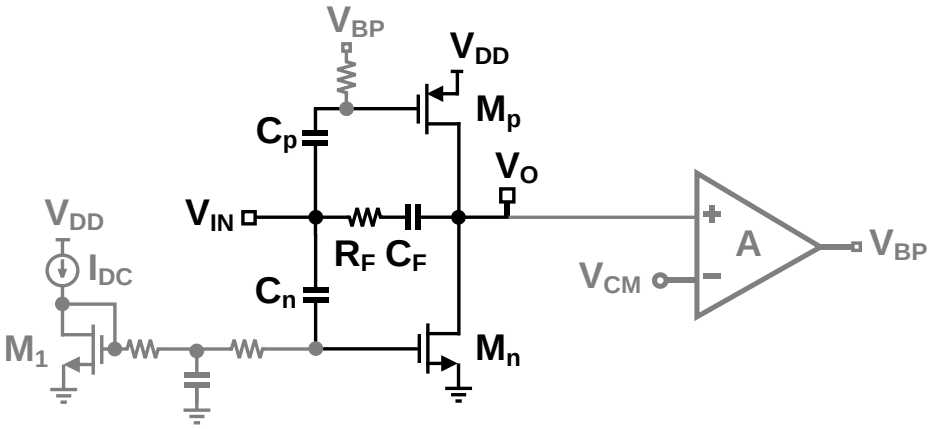


Figure 4.5. CMOS wideband LNA architecture with RF feedback for matching.

Table 4.1. The sizing of the CMOS transistors inside LNA.

	Length	Width	No. of Fingers	No. of Multipliers
NMOS	65 nm	910 nm	28	16
PMOS	65 nm	950 nm	32	20

Table 4.2. Performance of the designed LNA.

Gain	NF	S11	IIP3	IIP2	Current
12 dB	1.2-1.3	-11 dB	0 to +5 dBm	+70 to +80 dBm	11 mA

The second important block inside the RX, is the mixer. The LNA output is connected to the mixer by an AC-coupling capacitor. Non-overlapping LO signals have been used to improve NF and linearity. The switch size of the passive mixers is very critical. Smaller switch resistance (larger switch size) decreases the noise contribution from the mixer to overall RX NF. On the hand, the larger switch size increases the capacitive parasitic at the LNA output, which decreases the LNA gain and RX NF. Furthermore, more current is required in the mixer buffers to drive larger switches. The passive mixer switch sizes chosen in this design is 60u/40nm.

The last block inside the RX, is the baseband. The baseband is simply a trans-impedance amplifier (TIA), which convert the signal current to signal voltage. Since the voltage swing at the TIA stage is no longer small, the final stage should be very linear, and capable of providing large swings. On the hand, the noise contribution form the TIA to the overall NF should be minimized. Since this stage is already in baseband, it has

major contribution in 1/f noise of the RX. To minimize 1/f noise, the input stage of the OTA has been designed using very large PMOS transistor which has smaller 1/f noise comparing to NMOS counterpart. The second stage of the OTA is a class AB CMOS inverter that is capable of driving the capacitive feedback load. The OTA has been used in a feedback loop, to minimize noise, and improve linearity. The RC feedback (single pole at signal 3dB bandwidth) provides a single pole rejection, and helps with the OTA stability. Putting all the blocks together, the WB RX performance is summarized in Table 4.3.

Table 4.3. Performance of the wideband RX shown in **Figure 4.3**.

Gain	NF	S11	IIP3	IIP2	Current
45 dB	2.7	-11 dB	-5 dBm	+40 dBm	25 mA

As shown in Table 4.3 the performance of the WB RX is not sufficient to be employed in 4G LTE systems, and both NF and linearity needs to be improved. In order to improve NF, the front-end gain needs to be increased. NF improvement in wideband receivers is limited by the LNA gain requirement for 50 Ohms input matching. Therefore the gain of the LNA cannot be increased furthermore. To achieve a very good NF and break the trade-off between gains and input matching, and extra gain stage has been added after the LNA (GM stage) as shown in Figure 4.6. The GM stage minimizes the noise effect of the passive mixer (MMAIN), and the TIA referred back to the RX input and improves the RX NF. The GM stage is also a CMOS base trans-conductance which can provide much better NF and linearity. Table 4.4 shows the performance of the

new RX after adding the GM stage. Although the receiver NF significantly improved, the linearity is degraded by 15 dB.

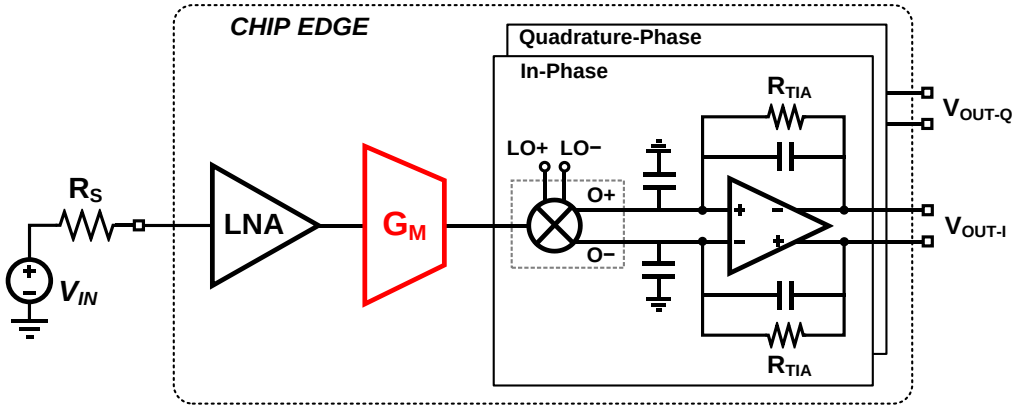


Figure 4.6. Revised wideband receiver to improve NF.

Table 4.4. Performance of the wideband RX shown in **Figure 4.6**.

Gain	NF	S11	IIP3	IIP2	Current
50 dB	1.6	-11 dB	-15 dBm	+15 dBm	28 mA

The drawback of adding a gain stage after the LNA is the high impedance node at the output of the LNA, which causes a large voltage swing for the TX leakage and the out of band (OB)-blockers which severely degrades the linearity. To attenuate these blockers before the GM stage, a tunable on-chip band-pass filter needs to be added as shown in Figure 4.7 the block should be noise-less not to degrade the 1.6 dB NF achieved by adding the GM stage.

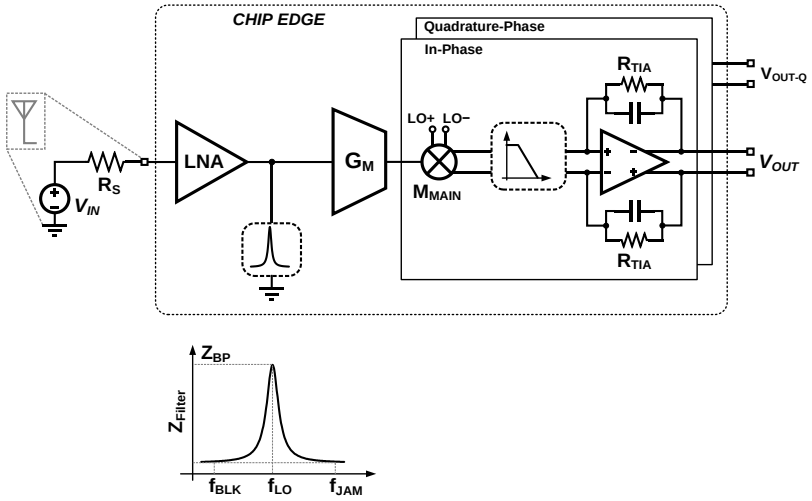


Figure 4.7. Wideband RX with an on-chip tunable band-pass filter for blocker rejection.

To implement an on-chip high-Q tunable band-pass the reciprocal properties of the passive mixers is employed. The high-Q N-path filter is shown in Figure 4.8. The filter is implemented as a quadrature passive mixer, driven by 4 non-overlapping 25%-duty-cycle LOs. Due to reciprocal properties of passive mixers, the low-pass R-C load of the mixer shows high-Q band-pass impedance at the mixer input [92]. Intuitively it can be assumed that the low-pass filter at the baseband is up converted to RF frequency. The attenuation of blockers using the filter is approximately equal to ($\Delta\omega=2\pi(fLO-fBLK)$)

$$Z_{\mathrm{AUX}\,(f_{\mathrm{LO}})} \cong R_{\mathrm{SW}} + {}^{2}\!/_{\pi^2}\, R_{\mathrm{IN}} \tag{4-1}$$

$$Z_{\mathrm{AUX}\,(f_{\mathrm{BLK}})} \cong R_{\mathrm{SW}} + {}^{2}\!/_{\pi^2}\, Z_{\mathrm{IN}}(\Delta\omega) \approx R_{\mathrm{SW}} \tag{4-2}$$

$$Blocker_{\mathrm{Atten}} \cong 20\log\left(1 + {}^{2}\!/_{\pi^2}\, {}^{R_{\mathrm{IN}}}\!/_{R_{\mathrm{SW}}}\right) \tag{4-3}$$

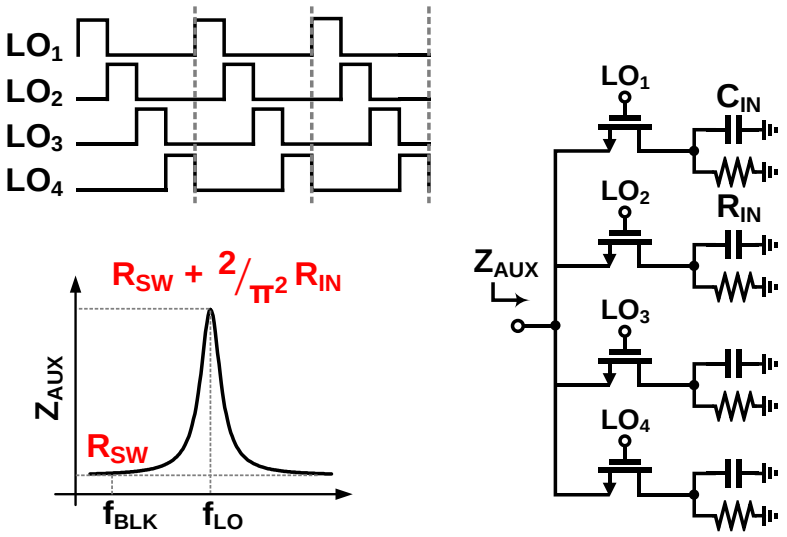


Figure 4.8. High-Q filter implemented with 25% non-overlapping quadrature passive.

where R_{SW} is the ON resistance of the AUX passive mixer, and R_{IN} is the baseband load resistance. R_{IN} and C_{IN} determine the RX 3-dB bandwidth. So, the rejection of OB-blockers at the filter input is limited by the nonzero R_{SW}. To improve the rejection, the output impedance of the LNA is increased by adding a buffer stage as shown in Figure 4.9. The proposed filter is added to the RX as shown in Figure 4.10. As expected, because of the N-path filter, the blockers see much smaller impedance at the GM stage input, which results a smaller voltage swing, and significantly increases linearity. Table 4.5 shows the performance of the new RX after adding the N-path filter.

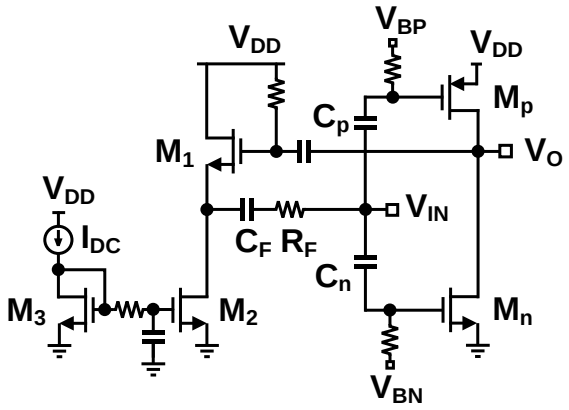


Figure 4.9. Revised design of the LNA to improve output impedance.

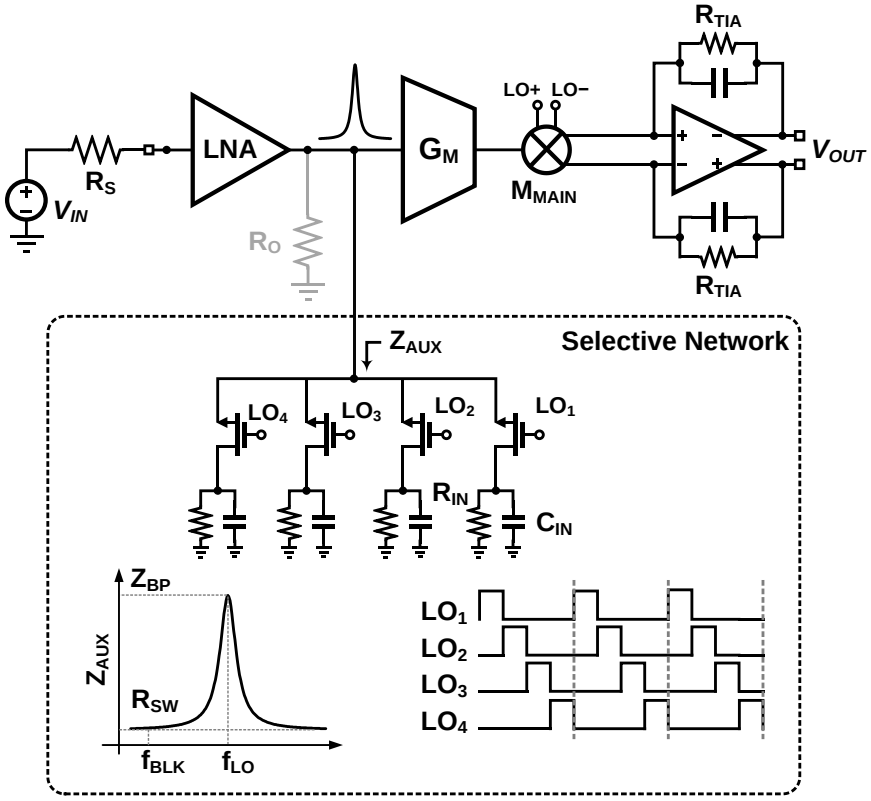


Figure 4.10. Revised wideband receiver with added N-path filter to improve linearity.

Table 4.5. Performance of the wideband RX shown in **Figure 4.10**.

Gain	NF	S11	IIP3	IIP2	Current
50 dB	2.3	-11 dB	-4 dBm	+40 dBm	31 mA

As it is shown in Table 4.5, adding the N-path filter significantly degrades the RX NF. As a result, the added feature does not seem to be appealing as the noise performance is similar to typical WB RX shown in Figure 4.3. As it is shown in Figure 4.11, the noise sources of the AUX path can be represented by a single noise current I_N flowing into LNA output. This noise current creates a negative voltage drop $-I_N R_O$ across R_O. The voltage converts to a negative current through the GM stage, which shows up at the TIA output. The same down converted current noise also flows into the R_{IN} at the output of the AUX path. By adding the same noise current back to the TIA input (shown in Figure 4.12) the current noise from the AUX path will be trapped in the loop, and does not show up at the TIA output. As a result the noise from the N-path filter can be cancelled out. For perfect noise cancellation, the GM should be equal to $1/R_O$. At the same time, by the RX current also flows into the R_{IN} load, and will be added positively to the current from the MAIN path, which increases the gain from of the RX, and further improves NF. Table 4.6 shows the performance of the receiver after employing the noise-cancelling technique.

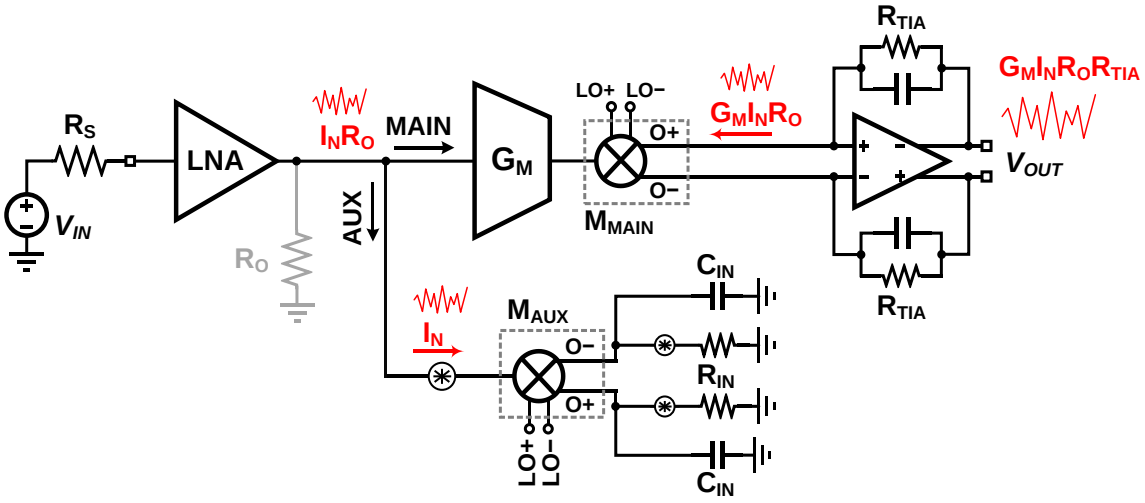


Figure 4.11. Noise sources from the N-path filter in the proposed two-path wideband receiver.

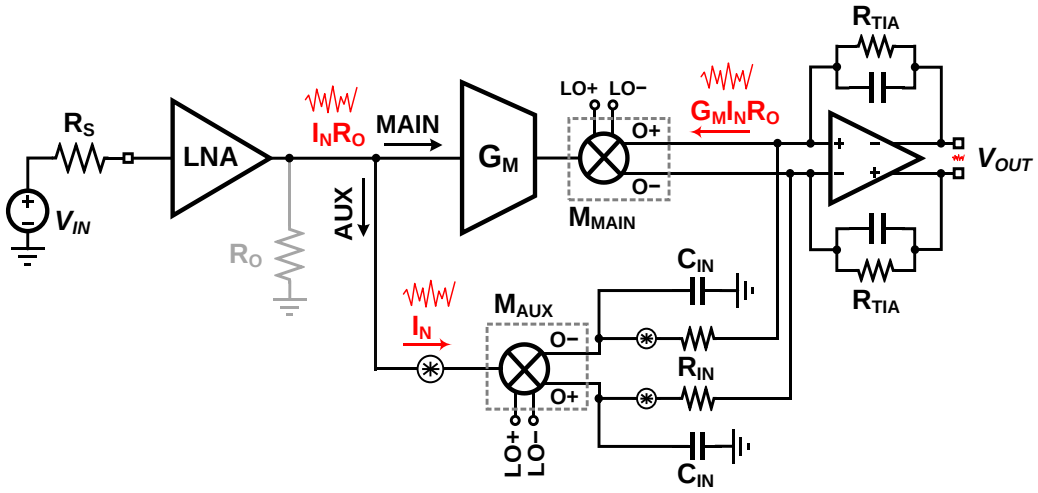
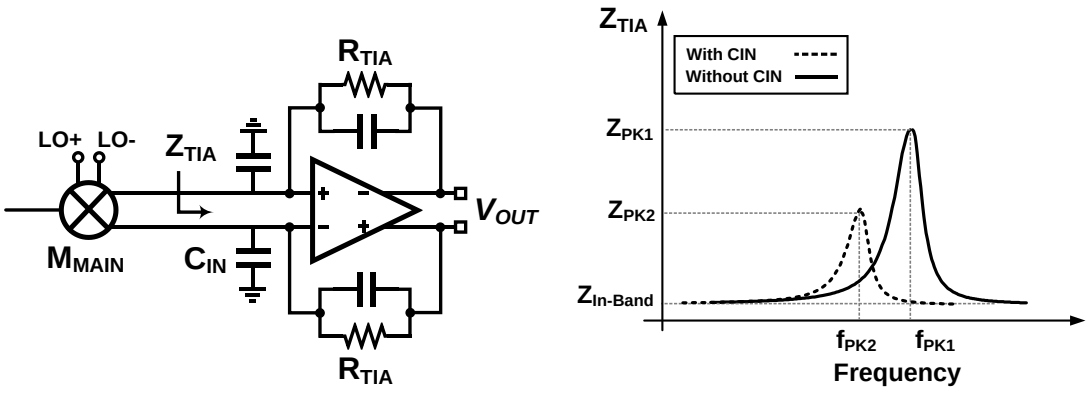


Figure 4.12. Noise cancelling approach in the proposed two-path receiver architecture.

Table 4.6. Performance of the wideband RX shown in **Figure 4.12**.

Gain	NF	S11	IIP3	IIP2	Current
50 dB	1.8	-11 dB	-4 dBm	+40 dBm	31 mA

The performance of the RX in Figure 4.12 still suffers from bad linearity and requires improvement as a candidate for 4G LTE systems. One of the main reasons for bad linearity, is the lack of gain in the OTA of the RX baseband. Figure 4.13(a) shows the TIA connected to the output of the passive mixer. Because of the limited gain-bandwidth of the OTA (inside the TIA), the input impedance of the TIA starts to increase, and peaks in a certain frequency offset (shown in Figure 4.13(b)), and the TIA input is no longer a virtual ground. As a result, the blockers and the TX leakage which are located at certain offset generate a large voltage swing at the TIA input, and degrades the RX linearity. Adding a C_{IN} at the TIA input, decreases both the peaking impedance and peaking frequency, and can partially improve linearity.



(a) (b)

Figure 4.13. (a)RX baseband connection (b) TIA input impedance with and without C_{IN}.

In case the receiver sees two signals, desired signal (RX) and blocker (BK), the current distribution of the two-path RX is shown in Figure 4.14. The RX current outputs

of the MAIN and AUX paths are weighted and combined at the input of the shared TIA. Notice that in the MAIN path both signal and blocker currents flow from the mixer to the TIA inputs, while in the AUX path most of the signal current goes through resistor R_{IN} to the TIA input, and most of the blocker current goes through the capacitor C_{IN} into the ground. To further improve blocker rejection, the blocker current in the AUX path, can be combined out-of-phase with the blocker current of the MAIN path by connecting the AUX path capacitors C_{IN} to opposite-polarity inputs of the TIA as shown in Figure 4.15. This anti-phase capacitive coupling between the two paths further rejects the blocker components outside the RX band and greatly enhances the receiver linearity. We call this coupling the base-band blocker filtering (BBBF) to differentiate it from the RF blocker filtering by the up-converted BB impedance of the AUX path. Since the TIA input impedance is virtual ground, the band-pass selectivity of the AUX path is still preserved after combining the two paths. The current I_{OUT} at the output of the LNA has two components as follows:

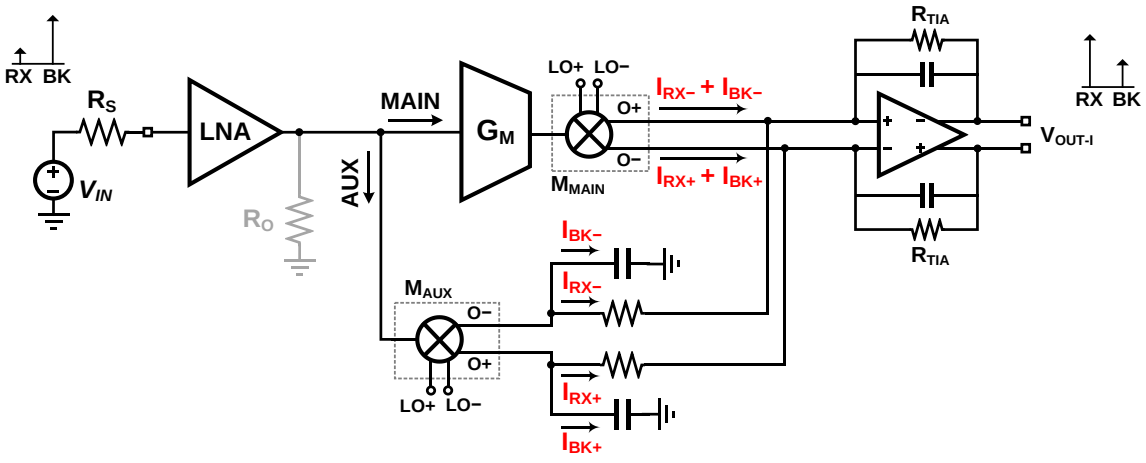


Figure 4.14. Current distribution of the two-path WB RX for RX and BK signals.

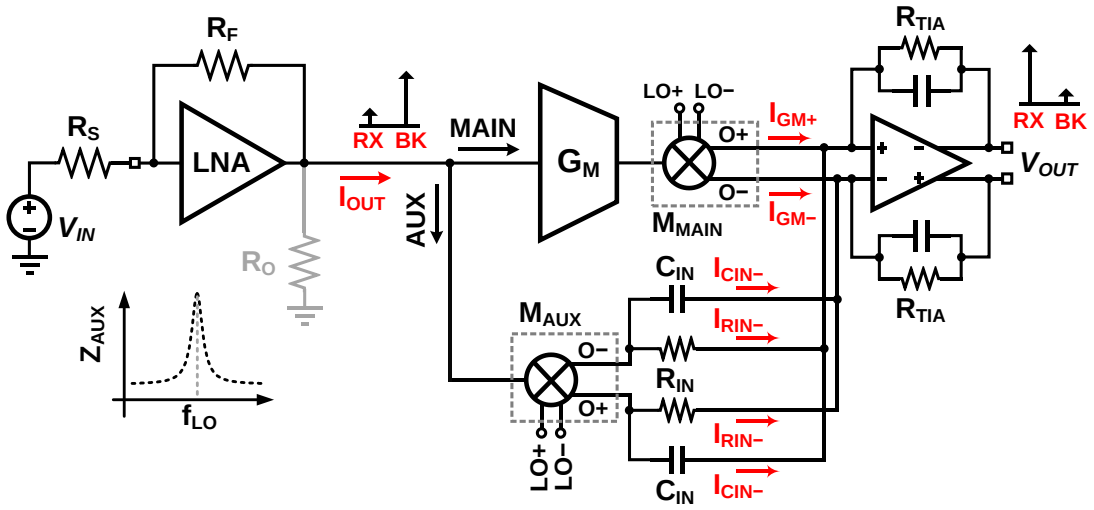


Figure 4.15. Baseband blocker filtering (BBBF) technique in the proposed two-path receiver architecture.

$$I_{OUT} = I_{RX} + I_{BLK} \tag{4-4}$$

where I_{RX} and I_{BK} are the RX and the blocker currents at the LNA output, respectively. The currents at the output of the MAIN and the AUX mixers are also given by:

$$I_{G_{M^+}} = -I_{G_{M^-}} \cong G_M \times \sqrt{2}/\pi \tag{4-5}$$

$$\times \left(R_S I_{RX}/2 + \left(Z_{AUX\,(f_{BLK})} \parallel R_O \right) I_{BLK} \right)$$

$$|I_{CIN+}| = |I_{CIN-}| \cong \sqrt{2}/\pi \, I_{BLK} \times \frac{R_O R_{IN} C_{IN} \Delta\omega}{\sqrt{(R_O + R_{SW})^2 (R_{IN} C_{IN} \Delta\omega)^2 + 4R_O^2}} \tag{4-6}$$

where R_O is the output impedance of the LNA. For perfect blocker current cancellation at the TIA input, G_M can be found as ($Z_{AUX(f_{BLK})} = R_{SW}$):

$$|G_M| \cong \frac{R_{IN} C_{IN} \Delta\omega}{R_{SW}\sqrt{(R_{IN} C_{IN} \Delta\omega)^2+1}} \quad (4\text{-}7)$$

If C_{IN} is large enough, then G_M should be equal to $1/R_{SW}$ to achieve the perfect blocker current cancellation at the TIA inputs. Therefore, the OB-blockers are rejected through the AUX path both in RF and baseband, while the associated noise is simply cancelled through the MAIN path at the TIA input. In this design, the G_M is selected to be $1/R_{SW}$ to achieve the best NF. Table 4.7 shows the performance of the RX after adding BBBF technique. The technique improves IIP3 by 5-7 dB.

Table 4.7. Performance of the wideband RX shown in **Figure 4.15**.

Gain	NF	S11	IIP3	IIP2	Current
50 dB	1.8	-11 dB	+3 dBm	+45 dBm	31 mA

To improve the OB rejection even further, an extra switch with out-of-phase clock and a series capacitor C_B has been added to the passive mixers of both MAIN and AUX paths as shown in Figure 4.16 [93]. As the input frequency deviates from the LO-frequency, the blocker current through C_B increases and the combination of out-of-phase currents attenuates the blocker current at the mixer output. Furthermore, this technique decreases the input impedance at the blocker frequency at the LNA load and therefore, improves blocker rejection at the output of the LNA. At the offset frequency, the two switches are in parallel, and the equivalent resistance is almost half. However, the auxiliary switch is high impedance at LO frequency, therefore it does not affect the performance at RX frequency.

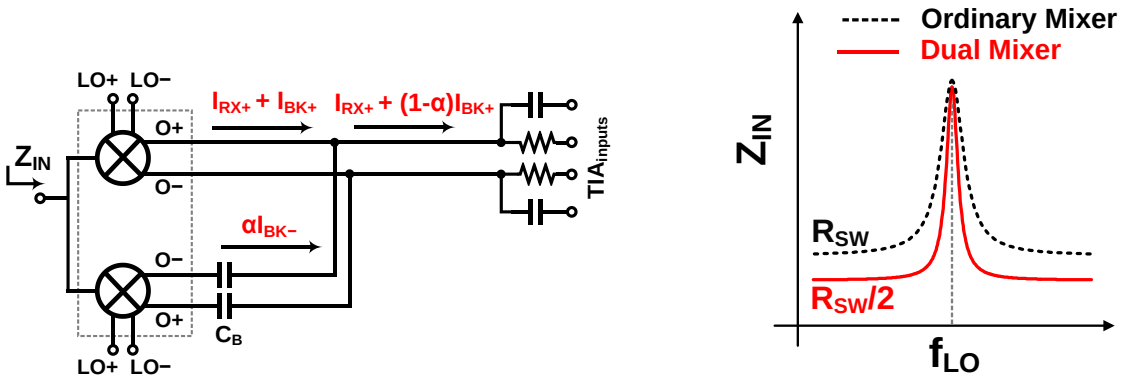


Figure 4.16. (a) Dual mixer architecture to further reject the blockers, (b) input impedance of the ordinary and dual mixer architecture.

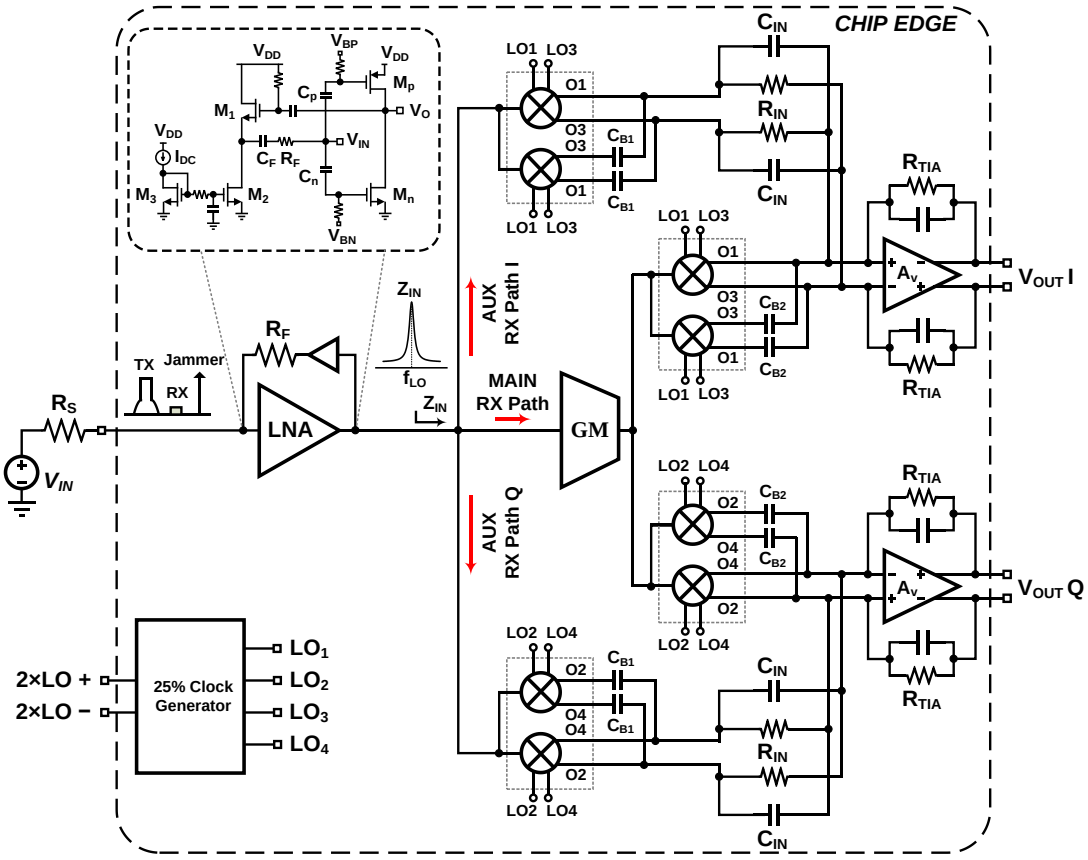


Figure 4.17. Block diagram of the low-noise blocker filtering wideband receiver.

Figure 4.17 illustrates the implemented low-noise blocker rejection wideband receiver. The LNA design is shown in Figure 4.17 inset. It uses the inverter M_n/M_p CMOS architecture both for LNA and the GM stage to improve linearity and NF. The matching feedback network is connected to the LNA output through a source-follower buffer to prevent reduction of the LNA output impedance, which would have degraded the blocker rejection by the AUX path. It also helps to keep the LNA gain relatively high. Table 4. 8 shows the performance of the entire noise cancelling, blocker filtering wideband receiver.

Table 4. 8. Performance of the wideband RX shown in **Figure 4.17**.

Gain	NF	S11	IIP3	IIP2	Current
50 dB	1.8	-11 dB	+5 dBm	+45 dBm	33 mA

One of the critical blocks is the LO generator. As it has been discussed, the mixers are drived by 25% duty cycle LOs. Figure 4.18 shows the schematic of the divider. The input signals are at double the LO frequency [94]. The resulting outputs are 25% duty cycle pulses at LO frequency. By biasing the first inverter buffer different overlapping between the signals can be achieved. The nominal biasing condition is 3 to 1 resistor values. This stage has significant contribution in the overall 1/f noise of the RX. Therefore the device sizes should be large enough to minimize 1/f noise. The drawback is the increase in current consumption of this stage. Furthermore the AC coupling capacitors should be small enough to filter 1/f noise.

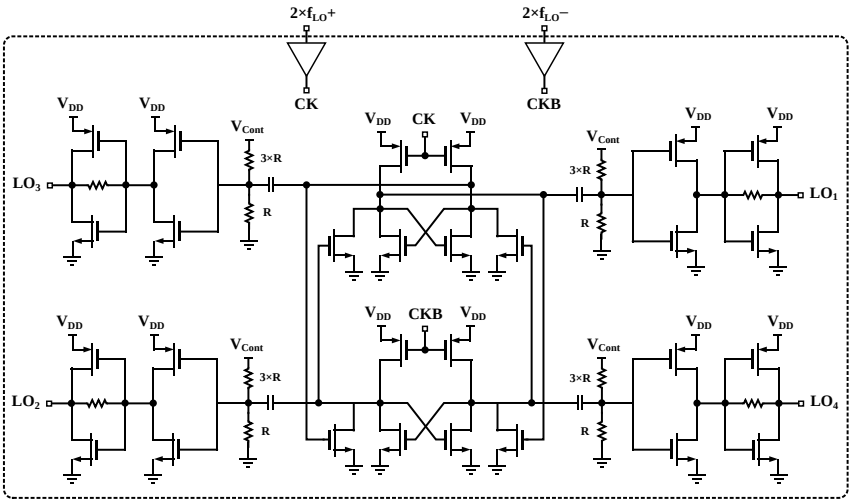


Figure 4.18. Schematic of the 25% LO generator.

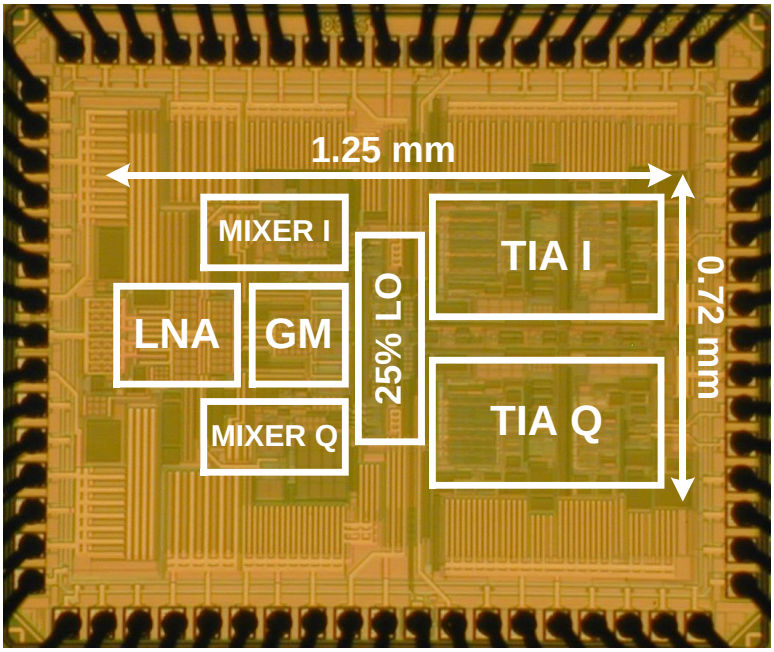


Figure 4.19. Die micrograph of the test chip in 40nm CMOS.

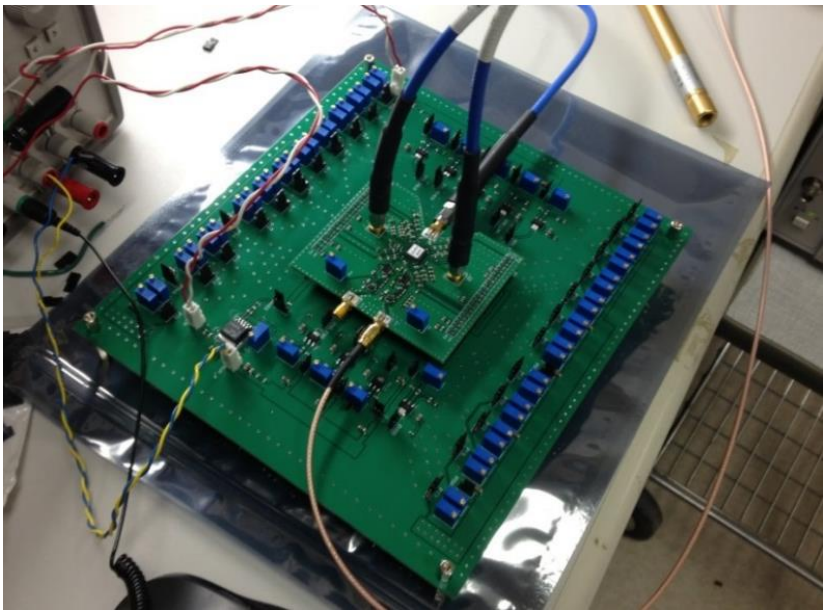


Figure 4.20. RF and DC boards for testing the proposed WB RX.

IV.3. Measurement Results

The test chip was fabricated in standard 40nm 1P8M CMOS. The die micrograph is shown in Figure 4.19. The active die area is 1.25 mm by 0.72 mm. The DC and the RF board are separated to minimize noise contribution from the DC board, and have more flexibility in the RF board (Figure 4.20). The receiver can operate from 100-2800 MHz. Figure 4.21 shows the measured S_{21} and S_{11} curves for two arbitrary LO frequencies (1 and 2GHz). The rejection is improved by 5-13 dB (Δf=50-200MHz) when the AUX path is ON. S_{11} is below -10 dB inside the signal bandwidth (10MHz). Due to the high-Q band-pass impedance presented by the AUX path to the LNA output at the LO frequency, and the LNA's negative feedback, the input match is very narrowband and

always centered at the LO frequency. In-band S_{21} is nearly 50 dB, and drops sharply away from the LO frequency due to the TIA's low-pass response and the additional attenuation by the AUX filtering path. Figure 4.22 shows the receiver in-band NF with the MAIN path ON and OFF for different LO frequencies. Due to noise-cancellation technique, the achieved NF is below 2 dB up to 2300 MHz LO frequency. As the MAIN path is turned OFF, the NF degrades by more than 3 dB that shows the effectiveness of noise cancellation technique.

In order to evaluate the noise performance of the RX with blocker, a blocker is placed at the RX input at 50 MHz offset. As the blocker power goes up the RX NF degrades. Up to -18 dBm, the NF degradation is less than 0.5 dB (shown in Figure 4. 23). The performance is limited by the LNA input transistors. As the input swing increase, the input transistors start to switch into triode region which degrades gain and NF.

To measure OB-IIP3 to tones are applied with Δf and $2\Delta f$ offset from the LO frequency. The power of each tone is -30 dBm, which is equivalent to the power from the TX leakage. Figure 4.24(a) shows the receiver OB-IIP3 measured for different frequency offsets of two blockers from the 2GHz LO frequency. With AUX path off the O-IIP3 is -15 dBm. By turning ON AUX path, due to the rejection provided by the high-Q filter, the IIP3 is improved to -2 dBm. Finally by turning ON, the BBBF technique, the OB-IIP3 is further improved to +5 dBm. The OB-IIP2 was measured using two different methods; (1) two blockers separated by 1 MHz (the IM_2 response lands at the baseband frequency) and (2) two blockers separated by the LO frequency (the IM_2

response lands at the LO frequency). In case the IIP2 is limited by the mixer mismatches, while in case 2, the LNA second order nonlinearity limits the RX IIP2. The OB-IIP2 measured by the first method for the swept offset frequency is shown in Figure 4.24(b). The IIP2 is greater than +45 dBm without any calibration, and is degraded more than 20 dB as the AUX path is OFF. The IIP2 from the second method is +23 dBm when f_{LO} = 1.96GHz, f_{BLK1}=1.88GHz, and f_{BLK2}=3.84GHz (AUX OFF: +4 dBm). This IIP2 is typically much smaller than the IIP2 for case one, and is improved in this receiver because of the complimentary LNA design and the attenuation provided by the AUX path. The LO path consumes 3-11 mA depending on the LO frequency, the LNA draws 12 mA, the G_M cell consumes 3 mA, and TIA draws 7 mA from a 1.1 V supply voltage.

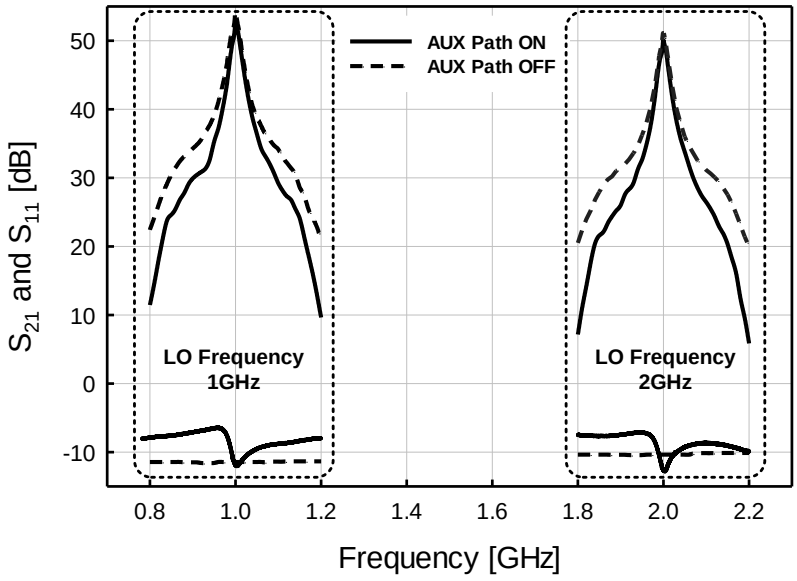


Figure 4.21. Measured S21 and S11 in two different frequency bands with AUX ON and OFF.

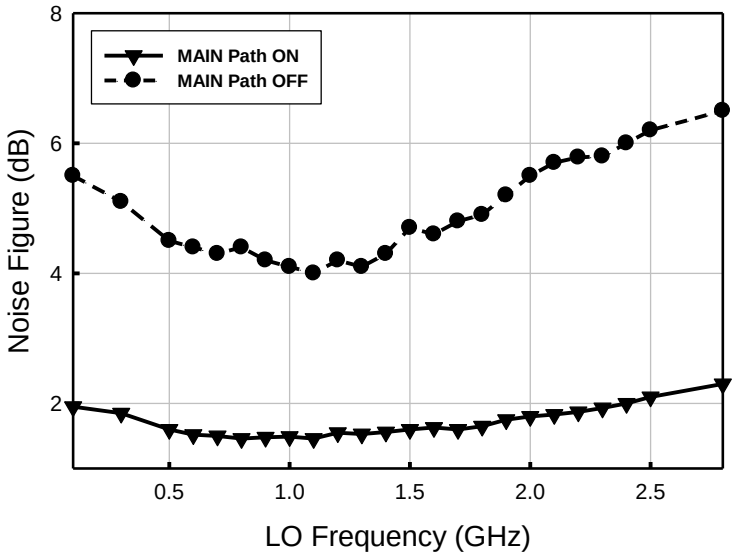


Figure 4.22. Measured receiver NF in 100-2800 MHz frequency range with MAIN path ON and OFF.

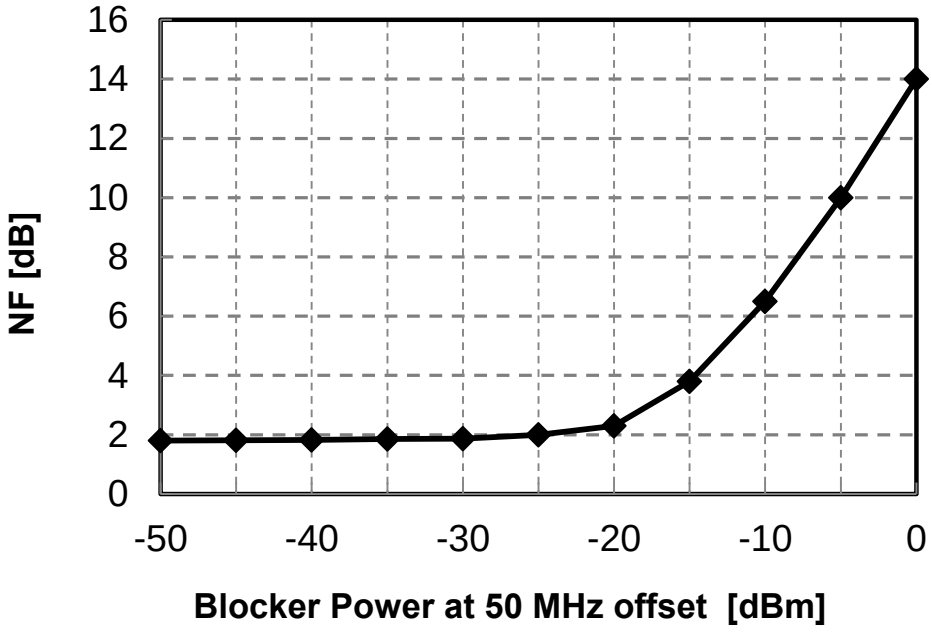
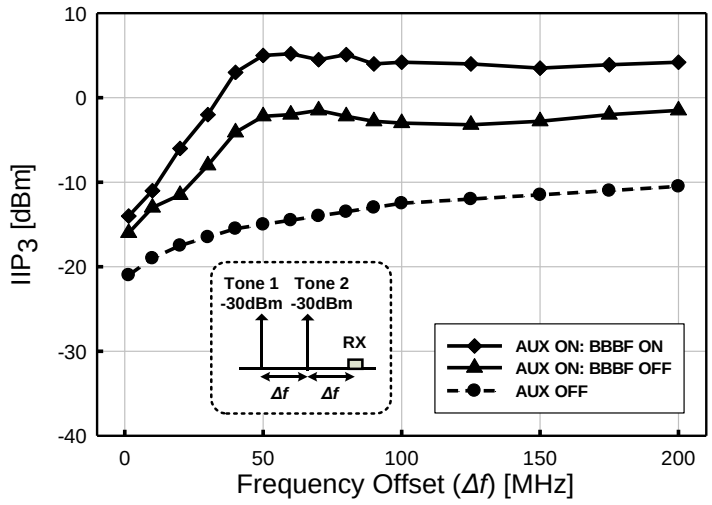
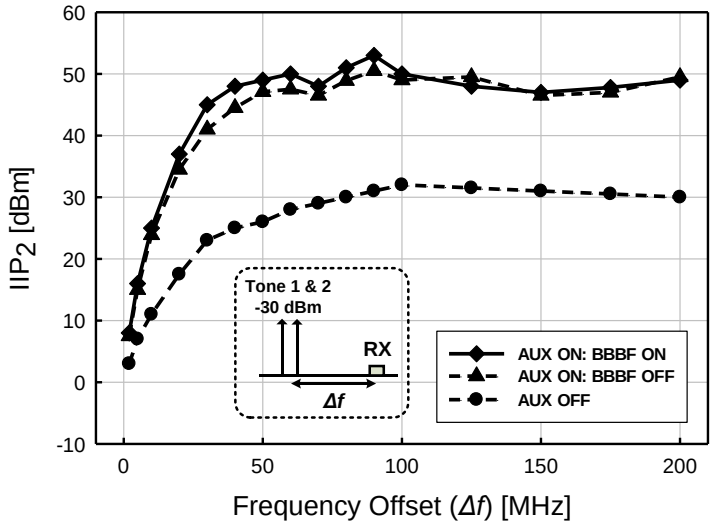


Figure 4. 23. Measured NF with blocker at 50 MHz offset frequency at 2 GHz LO.



(a)



(b)

Figure 4.24. (a) Measured IIP3 at 2GHz LO for different frequency offsets with base-band blocker filtering ON and OFF. (b) Measured IIP2 at 2GHz LO for different frequency offsets with base-band blocker filtering ON and OFF.

Table 4.9 compares this work with the recently published state of the art receivers. While consuming a lower power and occupying a smaller area due to the TIA sharing, this design achieves a lower NF (1.8 dB) than the previous works with an OB-IIP3 of +5 dBm. It also provides a very low LO leakage of -82 dBm to the antenna port (<-76dBm for 3GPP2 radios). Also, the addition of the AUX path improves OB-IIP3 by 20 dB with a very small penalty in power (3mW) and NF, making the RX more tolerable to OB-blockers.

Table 4.9. Measurement summary and state of the art comparison.

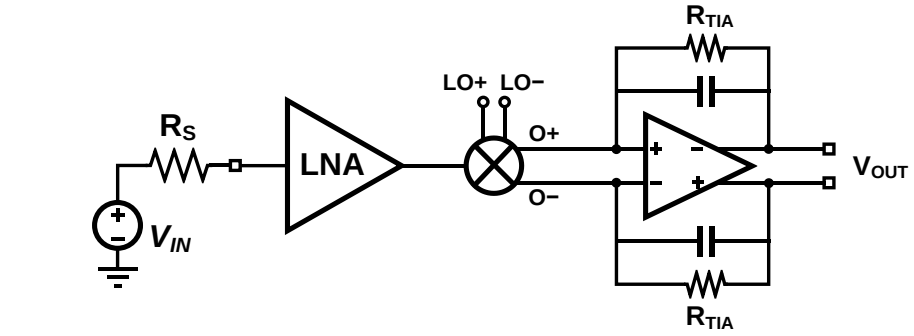
Specification	[75]	[87]	[89]*	This Work
Range [GHz]	0.1-2.4	0.08-2.7	0.4-3	0.1-2.8
Gain [dB]	40-70	72	70	50
NF @ 2GHz [dB]	7	1.9	> 2.3**	1.8
OB-IIP3 [dBm]	+25	+13.5	+3	+5
LO Leakage to RX Input [dBm]	N/A	N/A	N/A	-82
Active Area [mm^2]	2	1.2	0.6	0.8
Supply Voltage [V]	1.2/2.5	1.3	0.9	1.1
RX Power [mW]	37-70	35.1-78	< 40	27-40
CMOS Technology	65nm	40nm	28nm	40nm

* The results are for low band (LB).

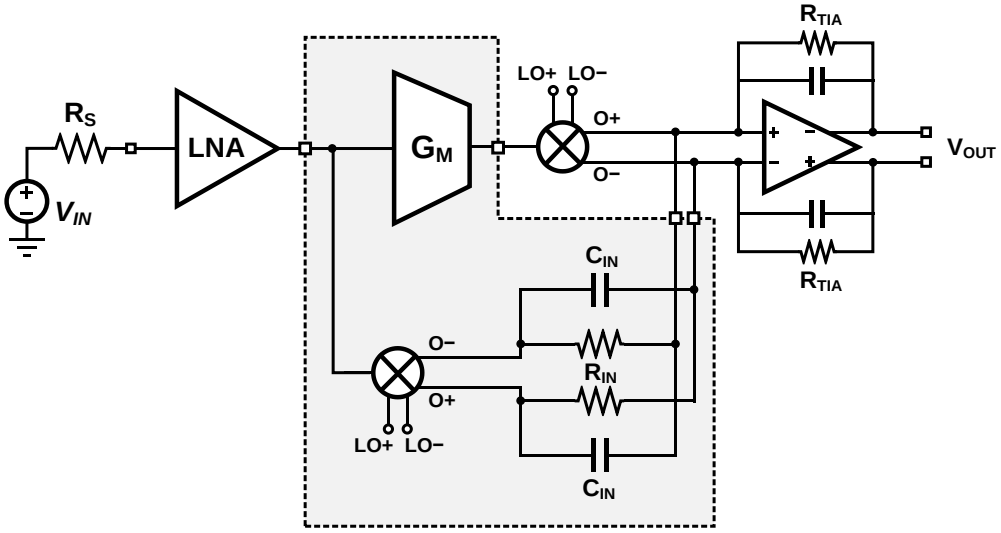
** Off-chip balun can result in an additional 1-1.2 dB NF degradation.

IV.4. Summary

The proposed techniques can be applied to any wideband receiver to improve linearity and NF. As shown in Figure 4.25(a) if the WB RX has a bad NF because of a small front-end gain, the block shown in Figure 4.25(b) can be added to the RX to improve NF without degrading linearity. In fact the added block also improves linearity.



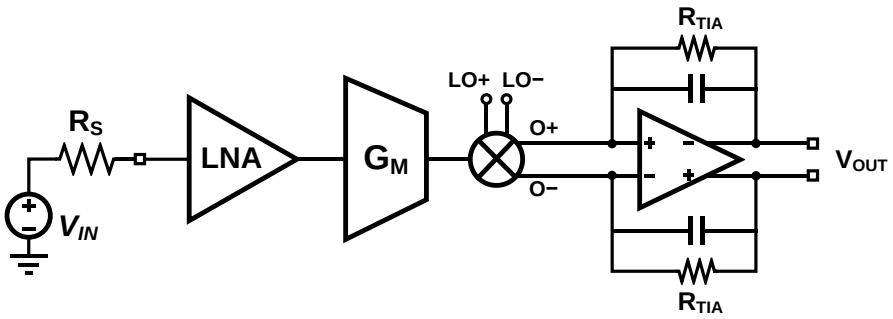
(a)



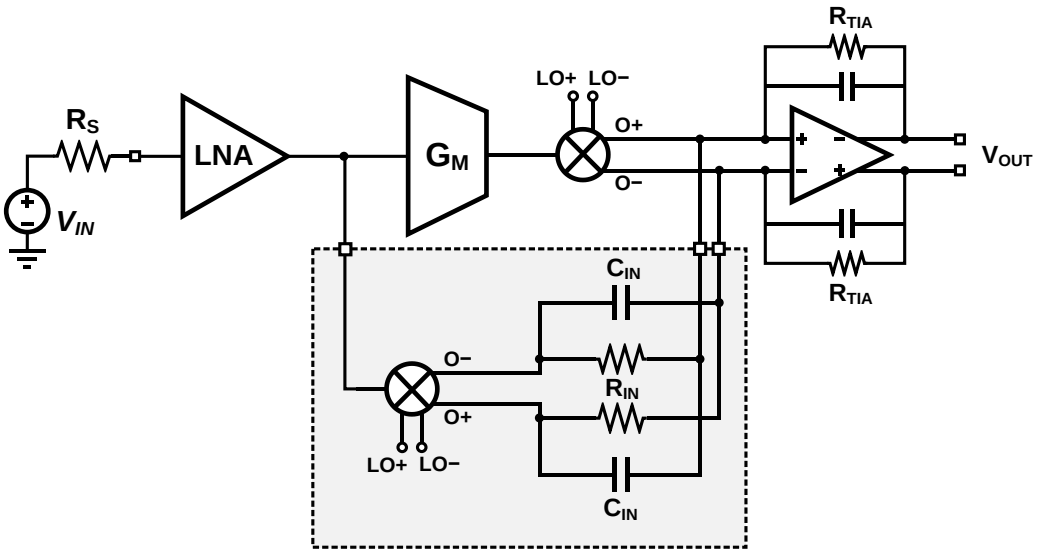
(b)

Figure 4.25. (a) WB RX with bad NF (b) the added block for improving NF without any linearity degradation.

In a different case shown in Figure 4.26(a) if the WB RX has bad linearity because of some high impedance nodes in the signal path, by adding the block shown in Figure 4.26(b) the linearity is significantly improved with very small degradation in NF.



(a)



(b)

Figure 4.26. (a) WB RX with bad linearity (b) the added block for improving linearity with almost no NF degradation.

The proposed wideband blocker-rejecting noise-canceling receiver achieves a NF of 1.8dB with +5dBm OB-IIP3 while consuming 36 mW. The proposed linearity improvement techniques are suitable for receivers with insufficient front-end attenuation of OB-blockers, which demand higher linearity without sacrificing NF, power consumption and area.

CHAPTER V

HIGHLY LINEAR LOW-NOISE WIDEBAND RECEIVER FOR COGNITIVE AND SOFTWARE DEFINED RADIOS*

V.1. Introduction

As discussed in chapter IV, type B receivers are focused on high linearity for cognitive and software defined radios. In this chapter these types of RXs will be investigated in details. As shown in Figure 5.1 type B RXs are SAW-less since they have to cover a wide frequency range. SAW-less or tunable RF front ends demand a wideband (WB) receiver (RX) that can tolerate stronger out-of-band (OB) blockers with low Noise Figure (NF). The strong blocker can be as large as -20 to -10 dBm which put stringent linearity requirements on the RX.

Here the goal is to provide an on-chip solution to greatly enhance the linearity of WB RXs with minimum increase in power consumption and NF. In this proposed two-path RX, four linearity improvement techniques are utilized in RF and baseband sections: 1) blocker signal rejection prior to LNA stage using an N-path filter (AUX path), 2) baseband blocker filtering technique, 3) dual mixer architecture, and 4) smaller voltage swing in the RX chain by a very low input impedance TIA, and therefore, better linearity. The N-path filter noise is partially cancelled throughout the MAIN path.

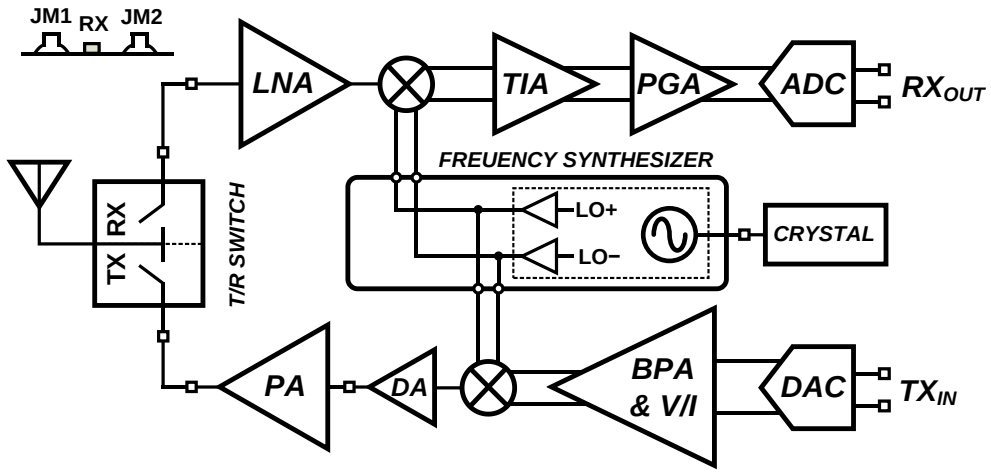


Figure 5.1. A typical software defined radio transceiver with TR switch.

V.2. Receiver Architecture with Blocker Filtering

The design of the WB RX is in 0.18 um CMOS IBM technology. In order to realize how much linearity and noise improvement is required to design in 0.18 μm CMOS technology, first a typical WB RX is designed as shown in Figure 5.2. After the Antenna, the signal is amplified through the LNA, down-converted through passive mixers, and the output current is converted to voltage at the end. The mixer is switching with 25% duty cycle LOs. The size of the mixer is optimized to achieve best linearity.

The LNA is the most important of the receiver and it should be carefully designed. Figure 5.3 shows the wideband LNA architecture that is chosen as a starting point. Because of multiple trans-conductance through both NMOS and PMOS transistors, the LNA can achieve a very good NF. Adding up NMOS and PMOS currents at the output also cancels out the second order non-linearity of the transistors, and can

significantly improve IIP2. One of the key points in designing LNAs is the size of the transistors. The width and length of the transistors should be optimized to achieve the minimum NF. On the hand, based on the LNA current, the biasing of the transistors should be optimized for maximum linearity (IIP3 and IIP2) achievement. The chosen size of the transistors is shown in Table 5. 1 and Table 5. 2 summarizes the performance of the wideband LNA. The LNA has a very good NF, and linearity. The matching is provided through resistive feedback.

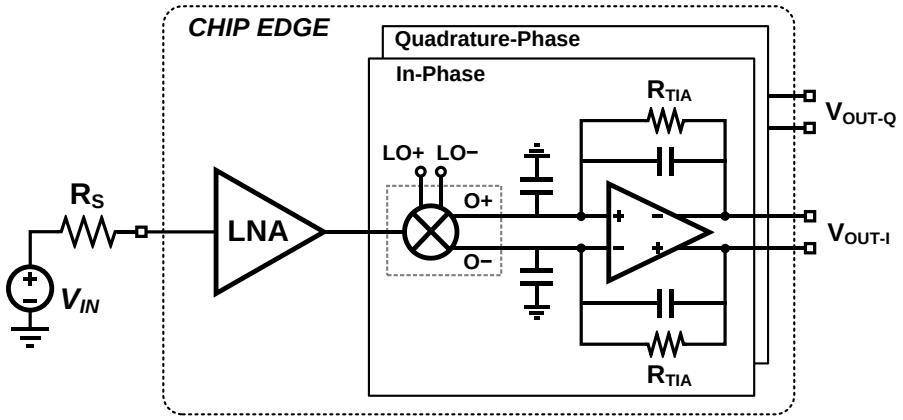


Figure 5.2. A typical architecture for wideband receivers.

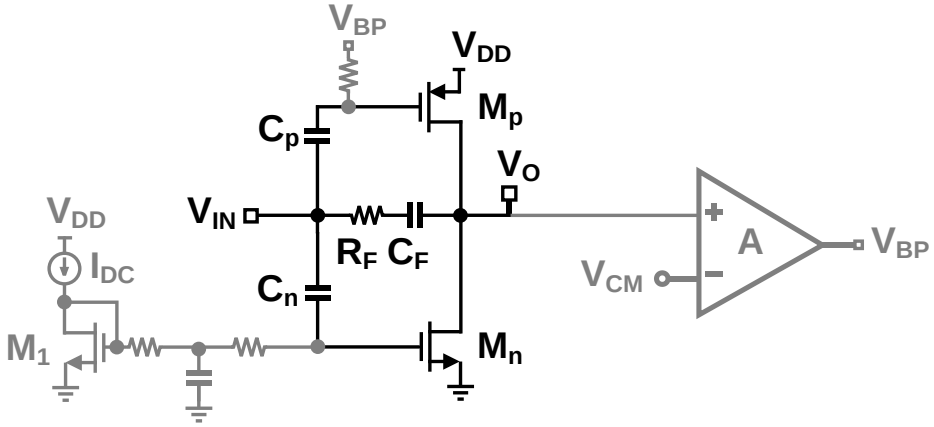


Figure 5.3. CMOS wideband LNA architecture with RF feedback for matching.

Table 5. 1. The sizing of the CMOS transistors inside LNA.

	Length	Width	No. of Fingers	No. of Multipliers
NMOS	180 nm	1.9 µm	20	16
PMOS	180 nm	1.98 µm	24	20

Table 5. 2. Performance of the designed LNA.

Gain	NF	S11	IIP3	IIP2	Current
12 dB	1.4	-11 dB	0 dBm	+80 dBm	10 mA

The LNA output is connected to the mixer by an AC-coupling capacitor. Non-overlapping LO signals have been used to improve NF and linearity. Since the LOs are 25% non-overlapping, just one AC-coupling capacitor is enough between the LNA and the mixer. The passive mixer switch sizes chosen in this design is 90u/180nm.

The last block inside the RX, is the TIA. The TIA is very similar to WB RX in chapter IV. Since the voltage swing at the TIA stage is no longer small, the final stage should be very linear which is guaranteed with high bandwidth feedback circuit. On the hand, the noise contribution form the TIA to the overall NF should be minimized. Since this stage is already in baseband, it has major contribution in 1/f noise of the RX. To minimize 1/f noise, the input stage of the OTA has been designed using very large PMOS transistor which has smaller 1/f noise comparing to NMOS counterpart. The second stage of the OTA is a class AB CMOS inverter that is capable of driving the capacitive feedback load. The OTA has been used in a feedback loop, to minimize noise,

and improve linearity. The RC feedback (single pole at signal 3dB bandwidth) provides a single pole rejection, and helps with the OTA stability. Putting all the blocks together, the WB RX performance is summarized in Table 5. 2.

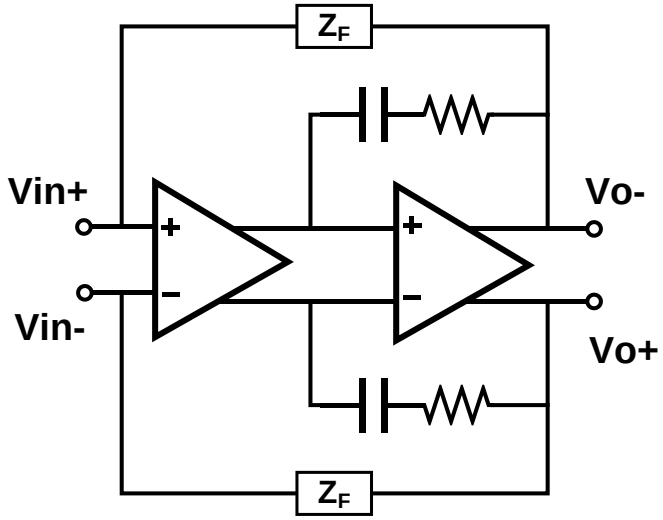


Figure 5.4. The TIA architecture for WB RX type B.

Table 5.3. Performance of the wideband RX shown in **Figure 5.2**.

Gain	NF	S11	IIP3	IIP2	Current
45 dB	3	-11 dB	-2 dBm	+40 dBm	26 mA

As shown in Table 5.3 the performance of the WB RX is not sufficient to be employed in software defined radios, and linearity needs a significant improvement. One of the main reasons why the linearity is not good is the input LNA stage. As shown in Figure 5.5, the CMOS LNA cannot tolerate large swings at the input. As the input swing

becomes large, due to opposite larger swing at the output, the transistors are no longer in saturation at the peak input voltage swing. Therefore, in a full period both NMOS and PMOS transistor are entering the triode region, which distort the signal and significantly degrades linearity. In order to improve the linearity, the blocker swing at the input should be minimized. Figure 5. 6 shows an addition of a high Q band-pass filter at the input to improve the linearity.

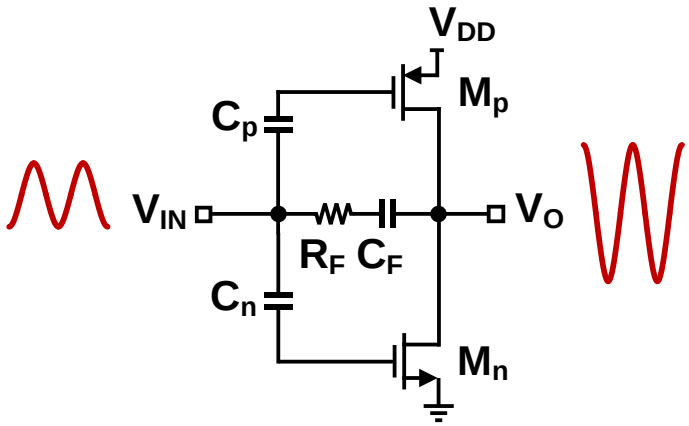


Figure 5.5. Sensitivity of WB LNA to large input swings.

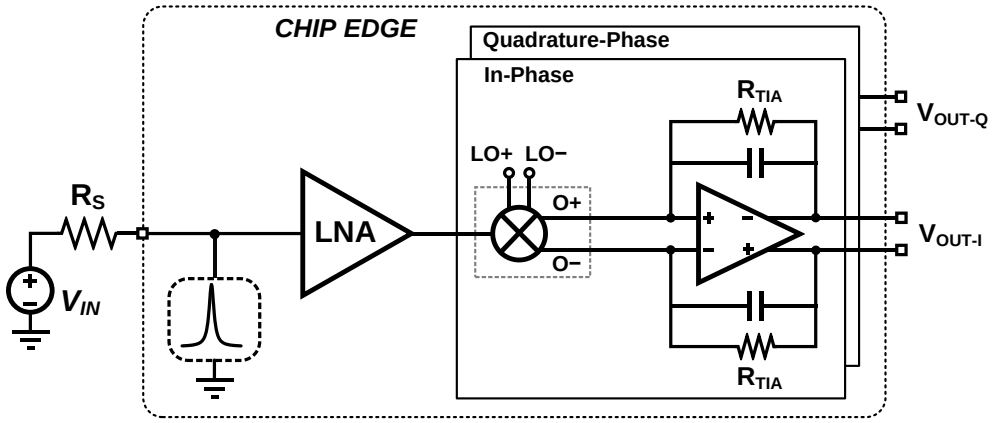


Figure 5. 6. Addition of a high Q band-pass filter at the input of the WB RX.

To implement an on-chip high-Q tunable band-pass the reciprocal properties of the passive mixers is employed as was also employed in Chapter IV. The high-Q N-path filter is shown in Figure 5.7. The filter is implemented as a quadrature passive mixer, driven by 4 non-overlapping 25%-duty-cycle LOs. Due to reciprocal properties of passive mixers, the low-pass R-C load of the mixer shows high-Q band-pass impedance at the mixer input [92]. Since the filter is added at the input, it should also provide 50 ohms input matching for the receiver. The attenuation of blockers using the filter is approximately equal to ($\Delta\omega=2\pi(f_{LO}-f_{BLK})$)

$$Z_{AUX\,(f_{LO})} \cong R_{SW} + {}^{2}/_{\pi^2}\, R_{IN} = R_S \tag{5-1}$$

$$Z_{AUX\,(f_{BLK})} \cong R_{SW} + {}^{2}/_{\pi^2}\, Z_{IN}(\Delta\omega) \approx R_{SW} \tag{5-2}$$

$$Blocker_{Atten} \cong 20log\left(1 + {}^{50}/_{R_{SW}}\right) \tag{5-3}$$

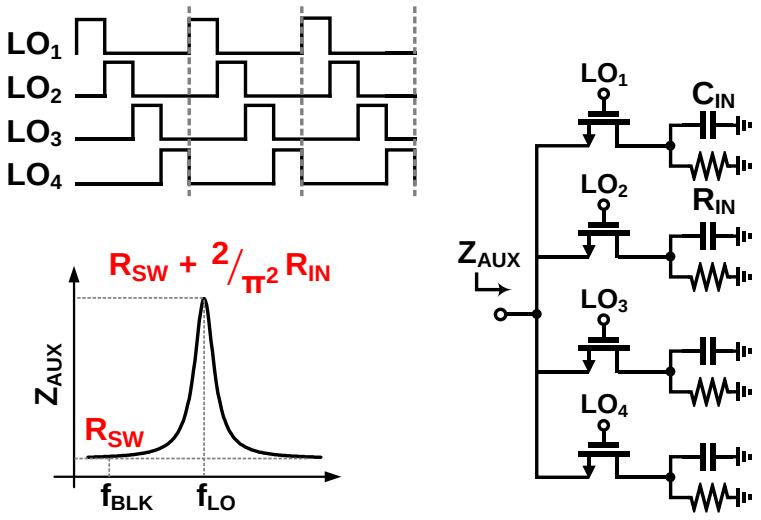


Figure 5.7. High-Q filter implemented with 25% non-overlapping quadrature passive.

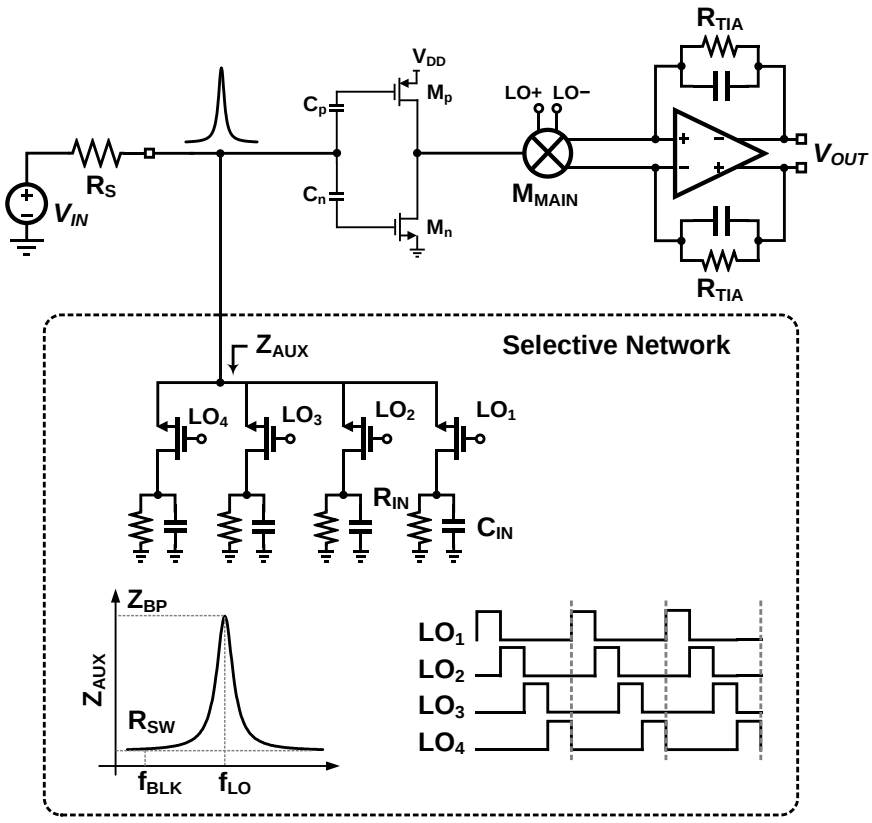


Figure 5.8. The WB RX with high Q N-path filter at the input.

where R_{SW} is the ON resistance of the AUX passive mixer, and R_{IN} is the mixer baseband load resistance. R_{IN} determines the input impedance of the N-path filter at the frequency of operation (LO). R_{IN} and C_{IN} determine the RX 3-dB bandwidth. So, the rejection of OB-blockers at the filter input is limited by the nonzero RSW. As expected, because of the N-path filter, the blockers see much smaller impedance at the LNA input, which results a smaller voltage swing, and significantly increases linearity. Table 5.4 shows the performance of the new RX after adding the N-path filter.

Table 5.4. Performance of the wideband RX shown in **Figure 5.8**.

Gain	NF	S11	IIP3	IIP2	Current
45 dB	4.7	-28 dB	+8 dBm	+60 dBm	29 mA

As it is shown in Table 5.4, adding the N-path filter significantly improves linearity while the NF degrades by 1.7 dB. One of the interesting features of adding the N-path filter before the LNA, is the ability to tune the input impedance of the receiver to get the maximum power in case the antenna impedance changes. As the ambiance of the antenna changes (by touching the cellphone) the antenna impedance also changes. Since the receiver is designed for 50 ohms input matching, this mismatch results in 1-2 dB sensitivity degradation. By retuning the input impedance of the RX through the N-path filter and providing the input matching, the sensitivity degradation can be recovered.

One of the important parts of designing a blocker tolerant receiver is making sure that the blocker swing is attenuated. If a designer just pays attention to the input reflection coefficient as design metric for blocker rejection at frequency offsets, the design may actually degrade the linearity. An example of such a design is shown in Figure 5.9(a), where the feedback to input is applied from the output of the TIA. If just input reflection coefficient is taken into account, due to the feedback at the LO frequency, the reelection coefficient is very narrow. But this does not mean the receiver is blocker tolerant. In fact, since the signal is feedback from the output of the TIA, the receiver input impedance at frequency offsets (where the blocker is located) is high impedance (since the signal is already filtered). As a result the blocker swing at the input

of the receiver is two times, and the receiver linearity can be comprised. Therefore, for improving linearity, the designer should make sure that the input impedance at the blocker frequency is very small, which minimizes the voltage swing.

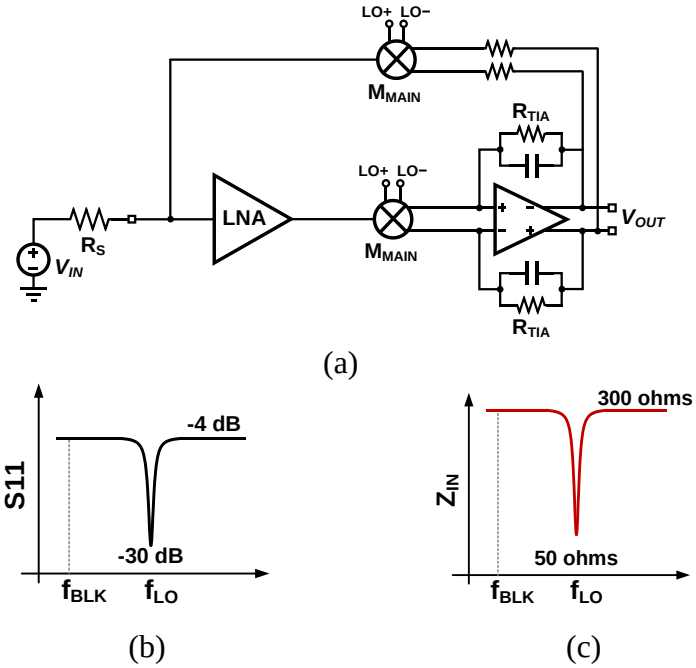


Figure 5.9. (a) The WB RX with feedback from the TIA output, (b) S_{11} of the RX, (c) the input impedance of the RX

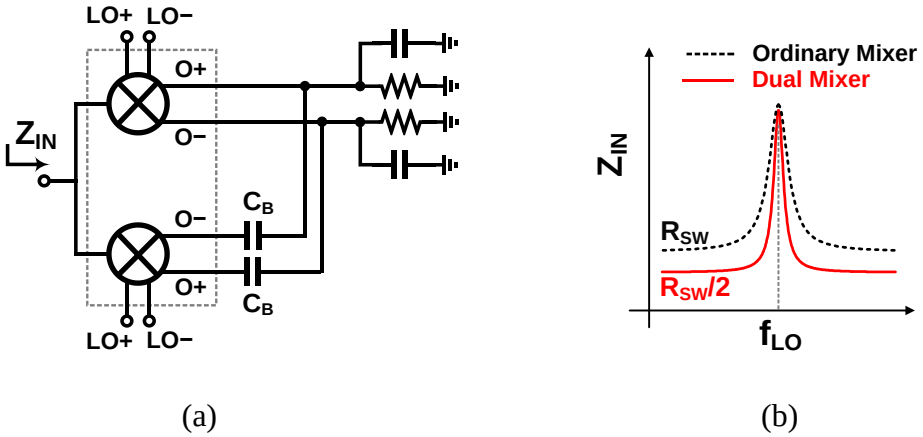
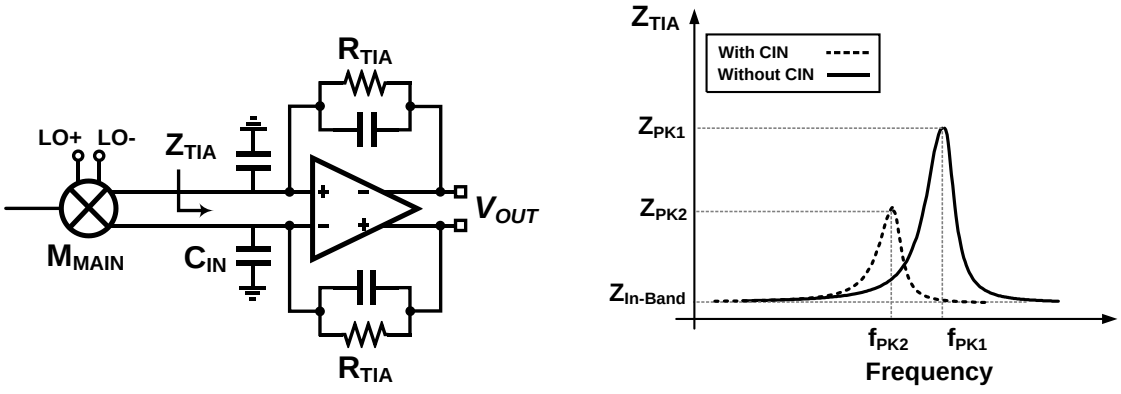


Figure 5. 10. (a) Implementation of the dual mixer architecture, (b) the input impedance of the typical and dual mixer architecture.

As it is shown in Table 5.4, the linearity is still not good enough for cognitive radios. In order to improve rejection at the input a double mixer architecture can be used as in Chapter IV. Figure 5. 10 shows a double mixer architecture. As a result, the input impedance at the blocker frequency is lowered down to 6 ohms, and the rejection is improved by 3 dB. As a result IIP3 is improved by 2 dB.

One of the main limitations of achieving a very good linearity is the RX baseband. One of the reasons is the TIA input impedance peaking. Figure 5. 11(a) and (b) shows the input impedance of the TIA. Because of the limited GBW of the OTA shown in Figure 5.4, the input impedance starts to increase as the OTA gain drops, and it peaks at higher frequencies. As a result, the blocker voltage swing (which is not in-band) at the TIA input is large and it degrades the linearity. To further investigate the effect of the TIA input impedance on the linearity, IIP3 of the receiver is simulated for different impedances at blocker frequency at the LNA output (a large portion of the LNA output impedance is dependent to the TIA input impedance). As shown in Figure 5.12, the RX linearity is significantly degraded as the LNA output impedance increases.



(a) (b)

Figure 5. 11(a) RX baseband connection (b) TIA input impedance with and without C_{IN}.

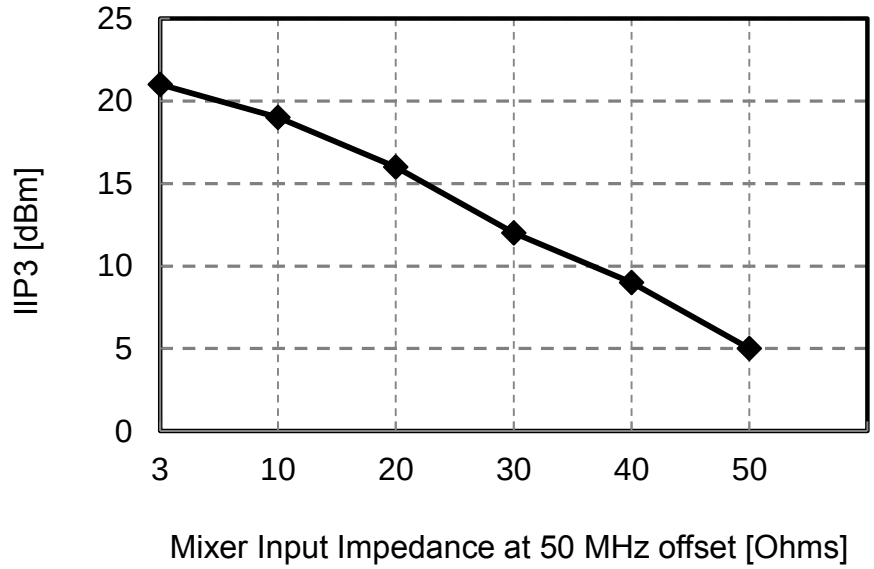


Figure 5.12. Sensitivity of RX IIP3 to the LNA output impedance which is loaded by the mixer input impedance.

To improve the linearity of the WB RX further, a new TIA should be designed that can provide a very small impedance up to higher frequencies, with small frequency peaking values. As shown in Figure 5.13(a) a gm-boosted approach is used in the TIA design, in which the TIA impedance peaking is shifted to much higher frequencies. Since there are two parallel impedances at the TIA input, one through the typical feedback resistor over gain, and the other through the common gate gm boosted stage, whenever the gain of the OTA drop, the input impedance stays low due to the addition of the common gate stage. The input impedance of the TIA is found to be:

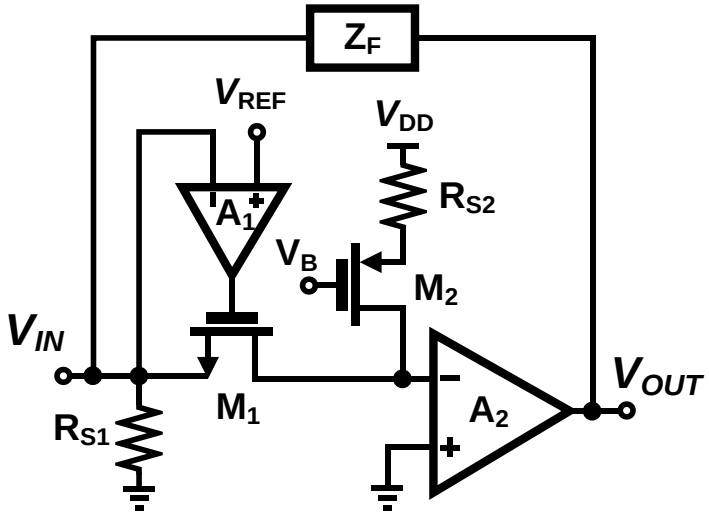
$$Z_{TIA} \approx \frac{Z_F}{1 + g_{m1} A_1(s) A_2(s) Z_{O1}} \tag{5-4}$$

As shown in (10), the input impedance is decreased by adding the g_m-boosted stage, which results in lower voltage swing through the entire receiver chain, and therefore significantly improve linearity, has been achieved in the LNA and the mixers. Figure 5.13(b) compares the input impedance of the new TIA to the typical TIA shown in Figure 5.4. Table 5.5 shows the performance of the RX with the addition of the new TIA. As a result the RX IIP3 is improved by 6dB, and the IIP2 is improved by 10 dB. One of the drawbacks of the new TIA, is the inferior noise performance. The current noise of the PMOS transistor M2 goes through the feedback resistor and directly shows up at the RX output. To minimize the 1/f noise contribution of the M_2 transistor, a resistor is added at the source of the transistor.

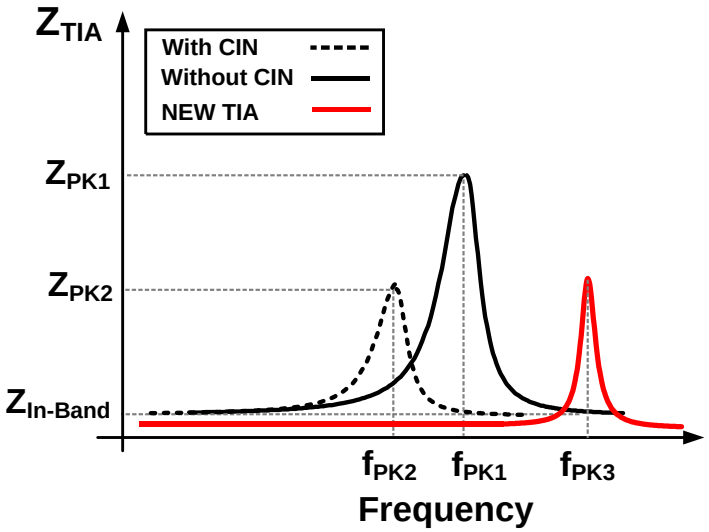
One of the drawbacks of typical TIA architectures is the mixer loading effect on the TIA loop gain. As shown in Figure 5.14(a), the TIA loop gain drops almost 20dB in the presence of an actual switching mixer. Since the new TIA provides low impedance to the feedback network, most of the feedback current feedback flows back into the TIA input, and as a result the loop gain is not affected that much by the switching mixers (Figure 5.14(b)).

Table 5.5. Performance of the wideband RX shown in **Figure 5.8**.

Gain	NF	S11	IIP3	IIP2	Current
45 dB	5	-28 dB	+16 dBm	+70 dBm	31 mA



(a)



(b)

Figure 5.13. (a) New common gate TIA architecture, (b) The input impedance of the new TIA comparing to the typical approaches.

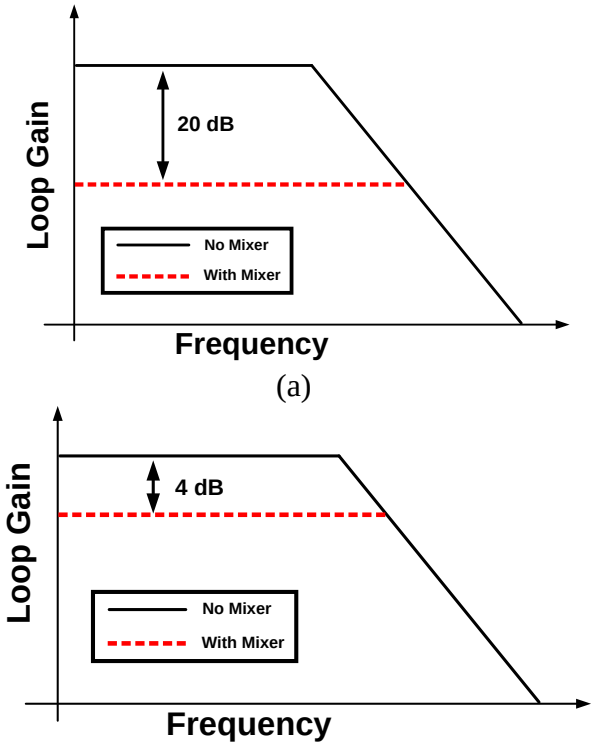


Figure 5.14. (a) Loop gain of the typical TIA with and without loading from the mixer, (b) Loop gain of the new TIA with and without loading from the mixer.

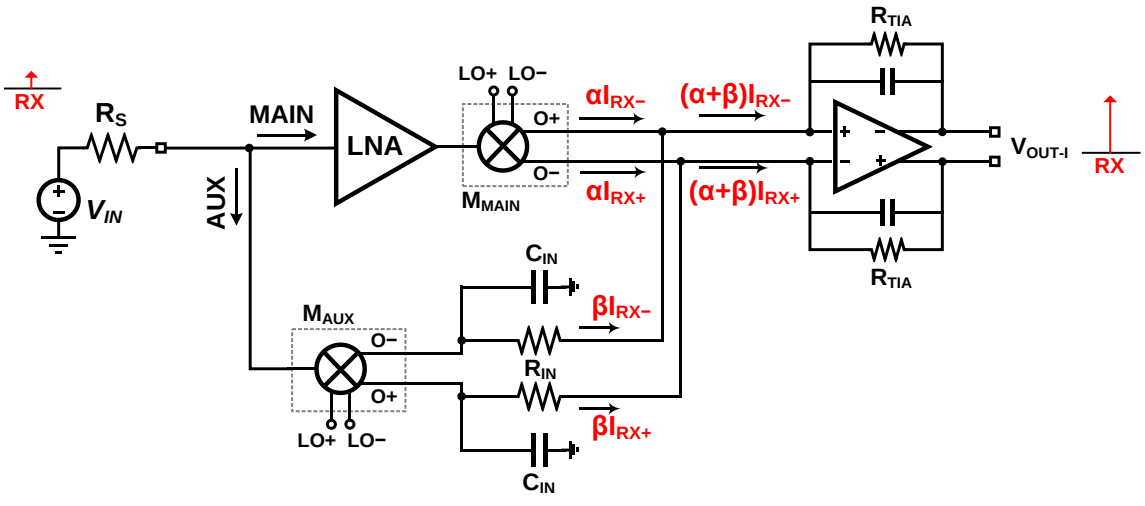


Figure 5.15. Addition of the linear RX current from the AUX path to the MAIN path.

The interesting property of the AUX mixer shown in Figure 5.8, is the separation of the RX and the blocker or TX leakage currents at the baseband through R_{IN} and C_{IN} loads. The down-converted RX current from the antenna mostly flows through R_{IN}. The current through R_{IN}, is generated by the division of the voltage at the RX input and the input impedance. Since the AUX mixer switches are very small, most of the input impedance at RX frequency is coming from R_{IN}. R_{IN} is linear resistor that is not dependent on the voltage swing. As a result the current through is very linear, and adding this RX current from the AUX path to the MAIN path can improve overall linearity. Figure 5.15 shows the addition of the two currents at the input of the shared TIA.

As it has been discussed, the down-converted RX current from the antenna mostly flows through R_{IN}, while the blocker current mostly flows through C_{IN}. While this separation occurs at the AUX mixer, in the MAIN mixer both currents flow without any separation. Based on this property, a base-band blocker filtering (BBBF) approach has been proposed in Figure 5. 16. Instead of connecting the AUX mixer load C_{IN} to ground, the outputs of C_{IN} is connected to the inputs of the TIA of the main path in a way to cancel out the blocker currents. For perfect blocker current cancellation at the TIA input, G_M of the LNA is found as ($\Delta\omega=2\pi(f_{LO}-f_{BLK})$):

$$|G_M| \cong \frac{R_{IN}C_{IN}\Delta\omega}{R_{SW}\sqrt{(R_{IN}C_{IN}\Delta\omega)^2+1}} \tag{5-5}$$

Because of the reciprocal property of passive mixers, minimizing the blocker voltage swing using BBBF technique at TIA inputs, also results in smaller swing at the

output of the LNA. Therefore, in addition to the TIA and mixer's linearity, LNA's linearity is also improved.

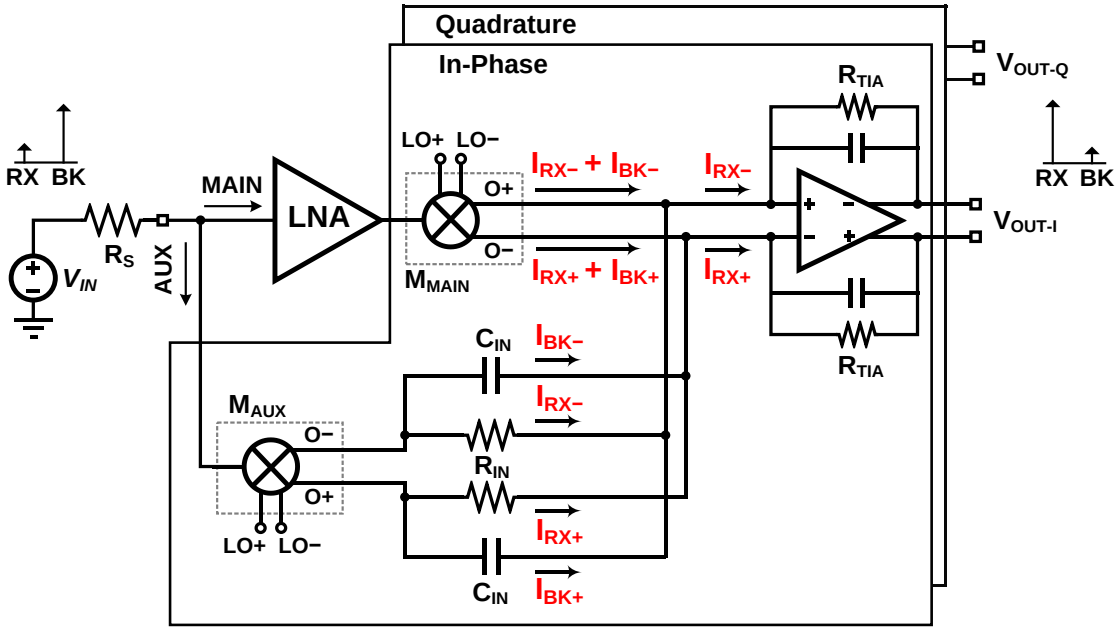


Figure 5. 16. Baseband blocker filtering technique (BBBF).

Connecting the AUX path to the MAIN path through the shared TIA, also improves the receiver NF by first increasing the gain, and then canceling out the AUX path noise. Similar to noise cancellation technique in Chapter IV, the noise sources of the AUX path creates a negative voltage drop across the impedance R_S. The LNA stage converts this negative voltage to a negative current at the TIA input, which cancels the positive AUX noise current if $G_M=1/R_S$. In this design, G_M is set for perfect blocker cancellation, while at least 25% of the AUX path noise is cancelled through the MAIN path.

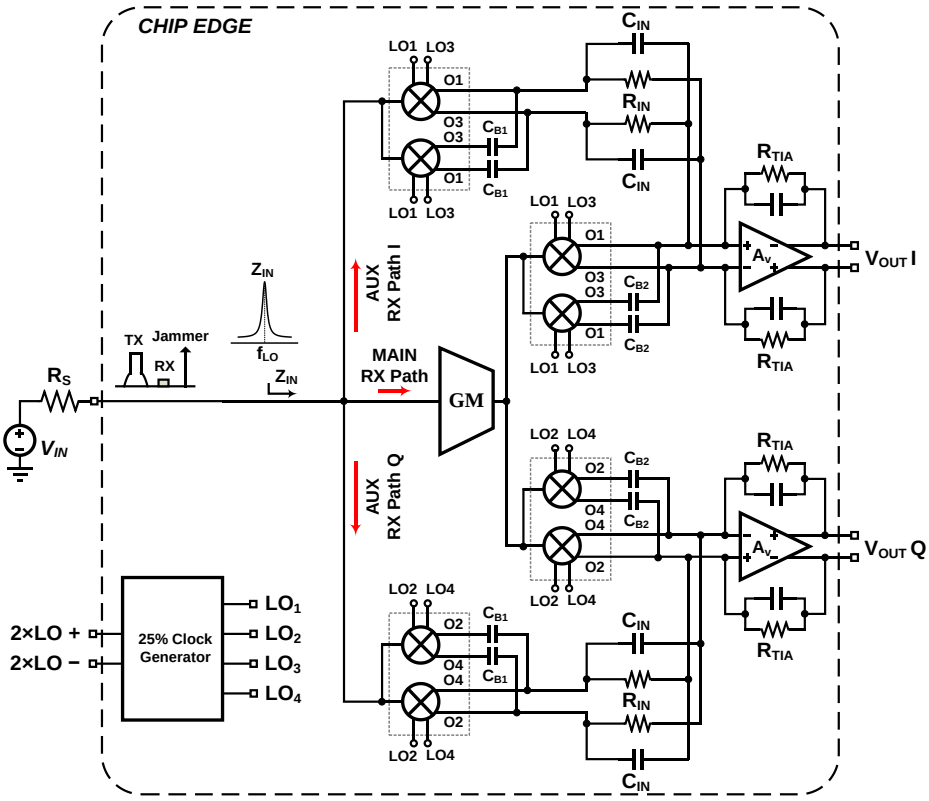


Figure 5.17. Block diagram of the highly linear blocker filtering wideband receiver.

Figure 5.17 illustrates the implemented highly linear blocker rejection wideband receiver. The LO divider (25% LO generation) is the same circuit as Chapter IV with the same criteria on the design. Table 5. 6 shows the performance of the entire noise cancelling, blocker filtering wideband receiver.

Table 5. 6. Performance of the wideband RX shown in **Figure 5. 16**.

Gain	NF	S11	IIP3	IIP2	Current
48 dB	3.5	-28 dB	+22 dBm	+70 dBm	31 mA

V.3. Experimental Results

The test chip was fabricated in standard 180nm CMOS. The die micrograph is shown in Figure 5.18. The active area is 0.65 by 1.2 mm. Figure 5. 19 shows the RF and DC boards for the test chip. The RX operates from 0.1-1.8 GHz. Figure 5.20(a) shows the measured S_{21} (from the LNA input to the TIA output) and S11 curves for f_{LO}=1GHz. The rejection is improved by 11 dB (Δf>50MHz) when the AUX path is ON. S_{11} is below -26 dB inside the signal bandwidth (2MHz). Due to the high-Q band-pass impedance presented by the AUX path, the input match is very narrow and centered at f_{LO}. In-band S_{21} is nearly 48 dB, and drops sharply away from f_{LO} due to the attenuation by the AUX filtering path, and the TIA's low-pass response. Figure 5.20(b) shows the RX in-band NF with the noise canceling ON and OFF for different LO frequencies. Due to noise-cancellation, the achieved NF is below 4 dB up to 1.8GHz LO frequency.

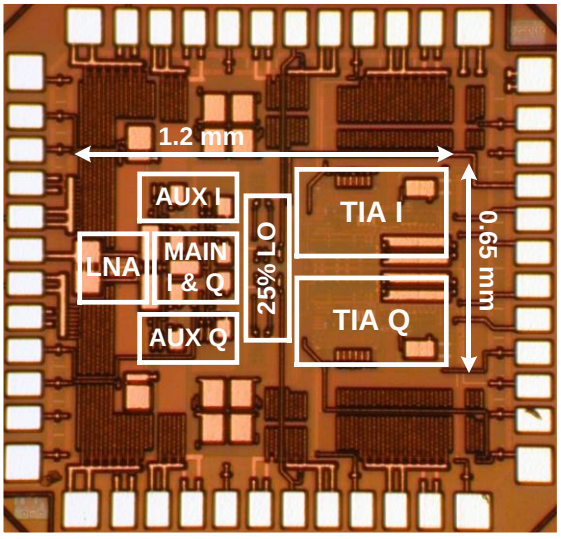


Figure 5.18. Die micrograph of the test chip in 180nm CMOS.

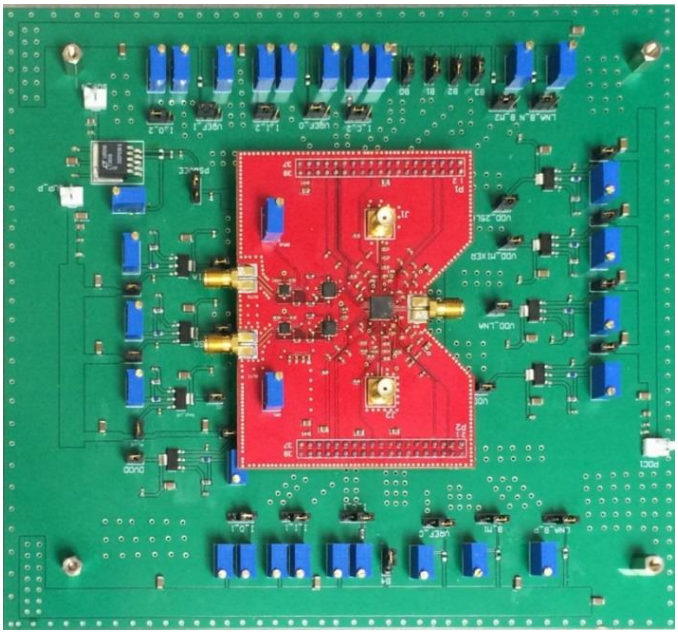
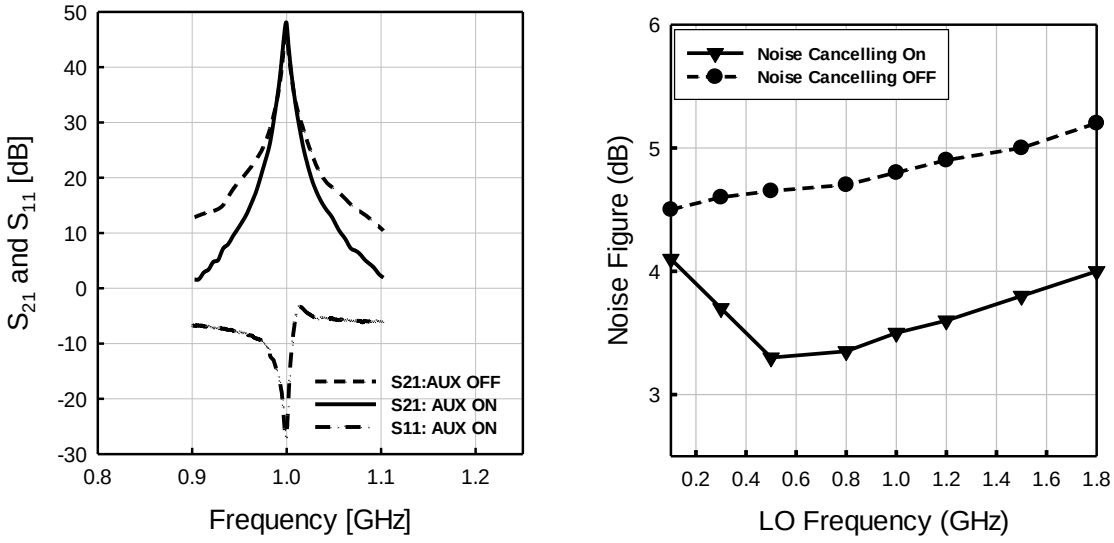


Figure 5. 19. RF and DC boards for testing the proposed WB RX.



(a) (b)

Figure 5.20. (a)Measured S_{11}, and S_{21} of the RX at f_{LO}=1GHz.(b) Measured RX NF with noise cancellation ON and OFF.

Figure 5.21 shows the RX OB-IIP3 measured for different frequency offsets of two blockers from the 1GHz f_{LO}. OB-IIP3 is +22 dBm with BBBF ON, +13 dBm with BBBF OFF, and 1dBm with the AUX path OFF. The OB-IIP2 measured to be >+70 dBm without any calibration, and it is degraded more than 10 dB as the AUX path is OFF. The measured NF at f_{LO}=1GHz, at the presence of a blocker with 50MHz offset is shown in Figure 5.22. Even for a 0dBm blocker, the RX NF is below 9dB, which goes up to 29dB when AUX path is OFF. The LO path consumes up to 16 mA depending on the LO frequency, the LNA draws 11 mA, and TIA draws 9 mA.

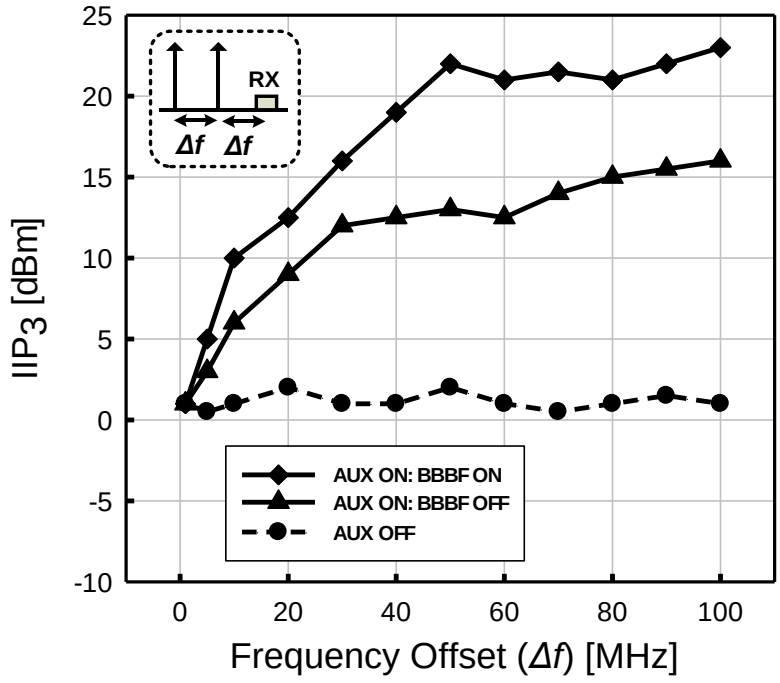


Figure 5.21. Measured RX IIP3 at 1GHz with AUX and BBBF ON and OFF, f_{LO}=1GHz.

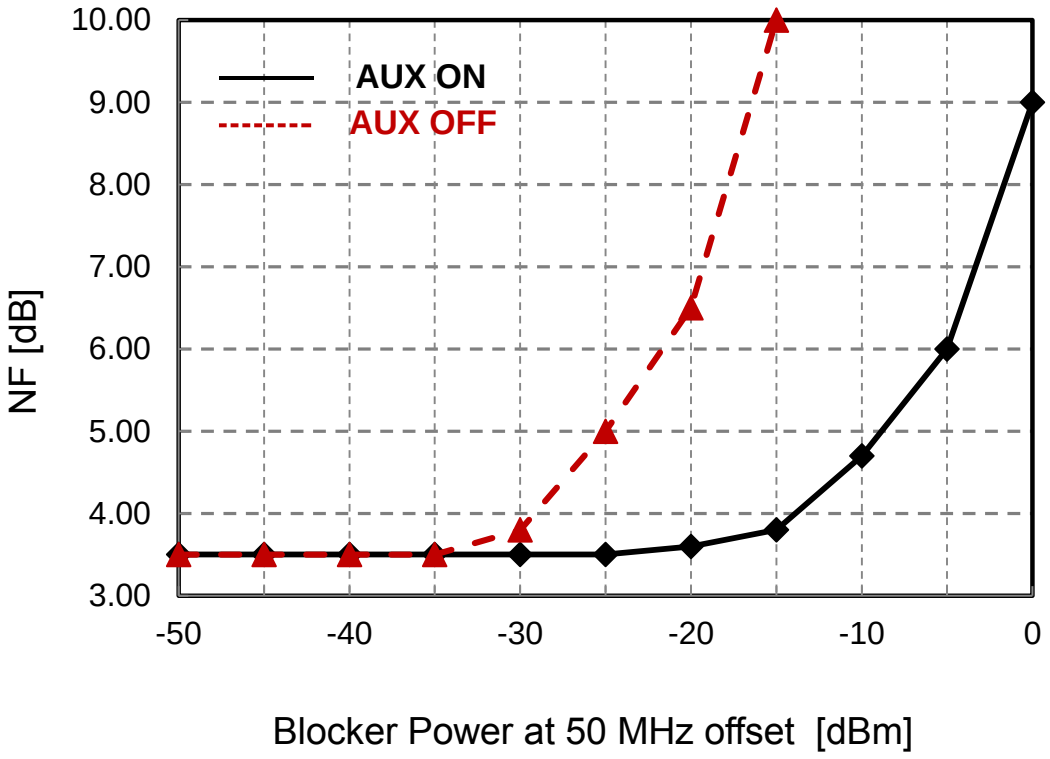


Figure 5.22. Measured RX NF with input blocker at 50MHz offset at f_{LO}=1GHz.

Table 5.7 compares this work and recently published wideband receivers. While utilizing a slower process (180nm) the proposed RX has an excellent OB-IIP3 of +22 dBm, with a NF of 3.5dB, a small die area, and comparable RX current consumption. The addition of the AUX path, making it much more tolerable to OB-blockers. The proposed blocker-tolerant noise-canceling RX can be used in radios with insufficient front-end attenuation of OB-blockers, and demand higher linearity without sacrificing area and power consumption.

Table 5.7. Measurement summary and state of the art comparison.

Specification	[75]	[87]	[89]*	This Work
Range [GHz]	0.1-2.4	0.08-2.7	0.4-3	0.1-1.8
Gain [dB]	40-70	72	70	48
NF @ 1GHz [dB]	>5.2	>1.6	> 2.2**	3.5
OB-IIP3 [dBm]	+25	+13.5	+3	+22
OB-IIP2 [dBm]	+56	+54	+85	+70
Active Area [mm^2]	2	1.2	0.6	0.8
Supply Voltage [V]	1.2/2.5	1.3	0.9	1.8
DC Current [mA]	37-70***	27-60	< 44	24-37
CMOS Technology	65nm	40nm	28nm	180nm

* The results are for low band (LB).

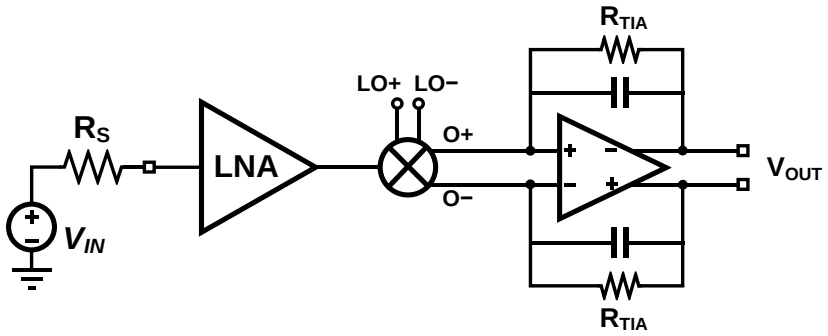
** Off-chip balun can result in an additional 1-1.2 dB NF degradation.

*** The numbers are for RX power consumption in mW.

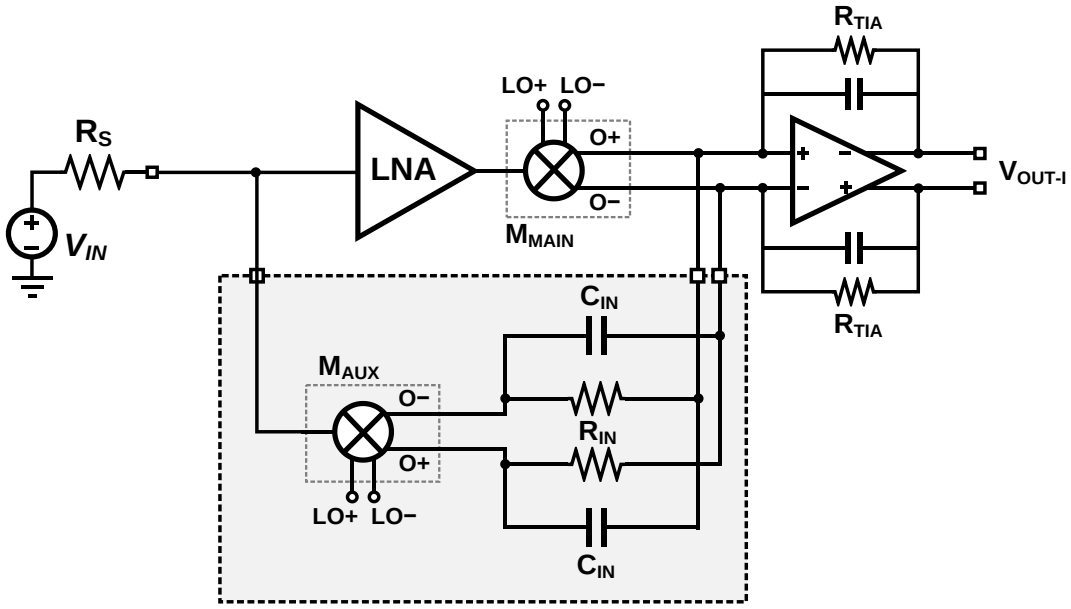
V.4. Summary

The proposed techniques can be applied to any wideband receiver to significantly improve linearity. As shown in Figure 5.23(a) if the WB RX has a bad linearity because of lack of front-end rejection, the block shown in Figure 5.23(b) can be added to the RX

to improve NF without significant degradation in NF. The NF degradation is minimized because of the noise-cancellation technique.



(a)



(b)

Figure 5.23. (a) WB RX with bad linearity (b) the added block for improving linearity without significant degradation in NF.

The proposed wideband blocker-rejecting noise-canceling receiver achieves an OB-IIP3 of +22dBm OB-IIP3, with 3.5 dB NF while consuming 37 mA. The proposed linearity improvement techniques are suitable for receivers with insufficient front-end attenuation of OB-blockers, which demand higher linearity without sacrificing NF, power consumption and area.

CHAPTER VI

CONCLUSION

This dissertation is focused on improving the performance of new generation wireless transceivers. Both transmitter and receiver blocks are investigated. One of the most critical blocks in transceiver is the power amplifier. The efficiency of the transceiver is almost dominated by the efficiency of the power amplifier. Because of the new modulation techniques, such as 128 QAM, the peak to average power ratio is becoming larger. Since the PA needs to be in linear region (not to degrade linearity) for the RF signal peaks, the larger the PAPR, the more DC current need to be fed into the PA which translates to worse efficiency. To improve the efficiency of the PA, we first detect the peaks, and then change the state of the PA to be able to handle the large input peak. Therefore, normally the PA works in normal state (Low power mode), in case a peak detected, the PA state is switched to peak mode (High power mode). In high power a large DC current is fed to the PA, while in low power mode, by changing the biasing of the transistors inside the driver amplifier and the power amplifier, the DC current consumption is significantly smaller (the DC current should be large enough not to degrade the linearity), Therefore, since most of the time the PA work in low power mode, the efficiency can be improved by 10%. The peak rate is low frequency, and in the range of 1-10 MHz which makes it possible to switch between the PA states.

The main challenge in the proposed approach is the change of the gm inside the DA and the PA due to the change in the biasing. Change the gm will change the gain of

the PA, in low power mode, which causes a discontinuity in the output waveform in the transitions. The jump in the transitions severely degrades linearity. To compensate the gain drop, a reconfigurable matching network is designed to increase R_L whenever the gm drops to keep g_mR_L constant.

As the modulation techniques become more complicated, such as 256 QAM, not only it degrades the efficiency, but also requires more stringent specifications for EVM and ACLR to avoid distorting the signal and degrading the SNR. To further improve linearity, a feed-forward cancellation technique has been proposed based on combination of bipolar and CMOS transistors. NMOS and Bipolar transistor can be sized and biased in a way to have phases for third order coefficient output current. By proper sizing and biasing of the two transistors, the third order coefficient of the output currents can be 180 degrees out of the phase. By applying the input to both transistors, and combining the output currents the third order non-linearity can be cancelled out. As a result the EVM is improved by 6 dB.

One of the new technologies that has a very good potential for low-range high data rate communications, is the ultra-wide band communications (UWB). UWB communications are typically low-power, low cost, and low range. Due to employing very short pulses for communication, UWB has the capability of reaching to a data rate as large as 1Gb/s. One of the major challenges of the UWB technology is the interference caused by the UBW system, to the NB receivers inside the band of operation. The main system inside the UWB band is 802.11a Wi-Fi, which is located at 5.2-5.8 GHz. As an example if a UWB transmitter is as close as 1m to a Wi-Fi receiver,

the sensitivity of the receiver can be degraded by as much as 25 dB, which significantly drops the range communication for Wi-Fi. The situation is even worse when the UWB transceiver is placed inside a cellphone or a tablet. In this case the maximum distance of the Wi-Fi and UWB antenna is less than 30cm.

In this dissertation, a novel impulse radio UWB (IR-UWB) transmitter has been proposed to suppress the interference caused by the UWB transmitter to the Wi-Fi receiver. Based on the properties of the Gaussian pulse, an analog pulse is generated in the baseband which has zero DC components. Therefore, if the pulse is up-converted to the frequency of the NB Wi-Fi system, there is a notch at the transmitted output. The notch depth can be as large as 30dB. Therefore, the interference caused by the UWB transmitter will be 30dB smaller. Since LO feed-through will be at the frequency of the Wi-Fi system, a DC offset cancellation block has been implemented inside the mixer. The block sets the differential DC current of the mixer to minimize LO feed-through. As a result LO-output feed-through is improved by 20dB. Measurement results shows the interference power level caused by the UWB TX is lowered down to -78 dBm/MHz at maximum EIRP, which is 20 dB lower than typical Gaussian pulse generator reported in the literature. The UWB pulse has a 5.5 GHz bandwidth and can operate with a maximum pulse rate of 400 Mpulse/s and energy of 65 pJ per pulse.

To improve the performance of the wireless handsets such as data rate and coverage in mobile handsets, though specifications push the design performance in to their limits. In the receiver, specifications such as sensitivity, noise figure and linearity are so stringent, that in today's state of the art designs there is almost no margin. In 4G

LTE design, the receiver has to cover a wide frequency range of almost from 700MHz to 2.7 GHz. In order to pass the specifications, still narrow-band receivers are used due to excellent NF and linearity performance inside the LNA. The well-known common source degenerated LNA, can provide a NF as low as 1.1 dB with 0 dBm IIP3. Although employing wideband receivers will save many off chip components and decrease die cost comparing to using many NB receivers, industry still prefers NB receivers for their superior performance. Lack of selectivity is one of the major challenges in wideband receivers. Since there is no off-chip components to filter the out-of band blockers (such as TX leakage) the linearity of the wideband receiver should be much better than the NB receiver. If the NB filter provides X dB attenuation, the linearity of the wideband receiver should be X dB better. Typical filter rejection is close to 10 dB. 10 dB improvement in the WB receiver IIP3 is very challenging to meet.

The other major challenge in wideband receiver design is inferior noise performance. Typically the gain of the wideband LNA is 1-2 dB smaller that NB LNA, which degrades the noise performance. Furthermore, due to the wideband matching requirement in the LNA, resistive feedback architecture is required inside LNA. The noise generated by the feedback element further degrades the noise performance. The NF of wideband LNAs are limited to 1.3-1.5 dB. Since the LNA gain is also smaller comparing to the NB receiver, more there will be more noise contribution from the mixer switches and the baseband at the output. The NF of wideband receiver is typically limited to 2.5-2.7 dB best case.

In order to improve NF in wideband receivers, the gain of the front end should be increased. The matching inside the wideband LNA is strongly related to the gain. Increasing the gain degrades the matching and input reflection coefficient. In this dissertation, in order to break this strong tradeoff between noise and matching, an extra gain stage (GM stage) is added after the LNA. The GM stage improves NF by 0.8-1 dB while the input matching remains untacked. The major drawback is the high impedance node between the LNA output and the GM stage input. Therefore, the out of band blockers generate a large voltage swing at the LNA output and severely degrades linearity (IIP3 limited to -15 dBm).

In order to attenuate blockers at the LNA output, and therefore, improve linearity, a high Q tunable on-chip band-pass filter is proposed. Passive mixers have reciprocal properties, in which the RF signal is down-converted to baseband, and on the other hand baseband signal is up-converted to RF. One of the most important effects of this property is the reflection of the baseband load to the RF frequency. As a result the input impedance of a passive mixer drived with non-overlapping LOs is the reflection of the baseband load of the mixer. Since the bandwidth of the baseband load can be very narrow, the resulted input impedance at RF is the up-converted baseband load impedance to RF frequency. If the load of the passive mixer is a parallel RC, the input impedance will be a high-Q band-pass filter. The N-path filter will load the LNA output, and as a result the out of band blockers will be attenuated. By the proposed approach the receiver IIP3 is improved by 10 dB. One of the main drawbacks of the added filter is the noise degradation due to the passive elements and the mixer switches. By adding the

output of the passive load of the mixer to the TIA input, the noise generated by the filter will be trapped in a loop and does not show up at the TIA output. While the noise from the filter is cancelled out, the signal is signal will be added through both paths which increases the gain. Therefore a very good NF of 1.8 dB is achieved for the entire receiver.

In order to decrease the blocker voltage swing at the TIA input, a base-band blocker filtering technique is proposed. While in the main path both blocker and the signal is passed through the GM stage, in the AUX path, the signal goes through the resistive load, while the blocker goes through the capacitive load. By proper connection of the N-path filter load to the TIA input, the blocker signal will be cancelled at the TIA input while the signal is amplified. As a result, the receiver IIP3 is improved by 7 dB. To further improve the linearity a dual mixer architecture is used for all the mixers in which the gain of the mixer for blockers is smaller than the signal path gain. Employing dual mixer approach enhances IIP3 by 2 dB.

CHAPTER VII

FUTURE WORKS

VII.1. CMOS PA Efficiency Improvement

Due to the inferior efficiency performance of the CMOS PAs, it is still not being implemented inside a transceiver chip. Therefore, the PA is a separate chip on GaAs, or InGaAs, etc. The CMOS PA efficiency is limited to 20%. Therefore, there is still a lot of room for improvement of the efficiency in CMOS PAs. Envelope tracking and polar PAs are very interesting approaches to improve efficiency. By proper design and innovation inside the feed forward path (envelope tracking path) the efficiency can be significantly improved.

VII.2. Wireless UWB Communications for 22-29 GHz

One of the major issues for UWB communications at 3.1-10.6 GHz frequency range is the interference caused by the UWB system to the other NB counterparts. While UWB offers a large data rate with a very low cost, crowded environment at low frequencies limits the capability of the system. UWB communication at 22-29 GHz recently has gained a lot of attention. With certain change in the configuration of the UWB transceiver, the large bandwidth can be used to significantly increase the data rate (1Gb/s). The new system requires a power amplifier to increase the range of operation

up to 100m. Adding a power amplifier changes the UWB system to a high-power system. Many large companies have already started working on the higher frequency range for data transmission. UWB at 22-29 GHz seems to be a very good candidate to implement the car to car radios or to be a substation to Wi-Fi at 5GHz.

VII.3. Blocker Filtering Technique for Carrier Aggregation

Today's new cellphones are equipped with carrier aggregation technology. In carrier aggregation multiple carriers are used to transmit the data to the user to increase the signal bandwidth and therefore the data rate. There can be as many as three carriers in the receiver side, which translates into three LO chains, mixers, and the TIAs. While still a wide frequency range should be covered, the number of the LNAs needs to be tripled to be able to handle all three carriers with NB LNAs with enough rejection through the off-chip elements. Replacing all the LNAs with a single wideband LNA can save a large power, area and cost. The challenge is the inferior performance of the wideband receiver both in linearity and NF comparing to NB counterparts. This effect is more sever in carrier aggregation. Furthermore blocker filtering technique using N-path filters can no longer be met with a single passive mixers. It is because a single filter will attenuate the signals in the other carriers. Therefore, at least three passive mixers are required to act as blocker filtering. On the hand, when the filters are connected to the same node (LNA output) due to loading effect of each N-path filter on each other, the blocker rejection capability of the N-path filter is significantly degraded. Therefore, a

new technique should be proposed to reject out of band blockers in carrier aggregation scenarios.

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APPENDIX A

Derivation of Rising Time vs. Pulse Bandwidth and Pulse Generator Circuit Parameters

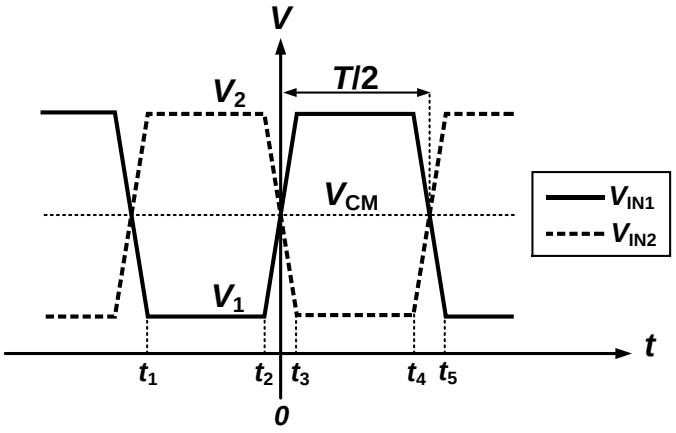

Figure A. 1. The input pulse signal (V_{IN1} and V_{IN2}) driving the pulse generation circuit.

Figure 3.2 shows the Gaussian monocycle pulse generator and the differential input signal applied. As shown in Figure A. 1, the input signal driving the pulse generator can be represented in more detail as follows:

$$V_{IN1}(t) = \begin{cases} V_1 & t_1 \le t \le t_2 \\ V_{CM}+\alpha t & t_2 \le t \le t_3 \\ V_2 & t_3 \le t \le t_4 \\ V_{CM}-\beta\left(t-T/2\right) & t_4 \le t \le t_5 \end{cases} \quad \text{(A-1)}$$

$$t_1 = -T/2 + \frac{1.25}{2} t_f = t_5 - T \quad \text{(A-2)}$$

$$t_2 = -t_3 = \frac{1.25}{2} t_r \quad \text{(A-3)}$$

$$t_4 = T/2 - \frac{1.25}{2} t_f \tag{A-4}$$

$$\alpha = \frac{0.8(V_2 - V_1)}{t_r} \tag{A-5}$$

$$\beta = \frac{0.8(V_2 - V_1)}{t_f} \tag{A-6}$$

$$V_{CM} = V_1 + \frac{(V_2 - V_1)}{2} \tag{A-7}$$

in which t_r and t_f are the rising and falling time of the ramp signal, and V_2 and V_1 are the maximum and minimum voltage of the input ramp, respectively. For $t_2 \leq t \leq t_3$:

$$V_{IN1}(t) = V_{CM} + \alpha t \tag{A-8}$$

$$V_{IN2}(t) = V_{CM} - \beta t \tag{A-9}$$

$$if\ t_r = t_f \rightarrow \alpha = \beta \longrightarrow V_{IN1}(t) = V_{IN2}(t - T/2) \tag{A-10}$$

Inside the sub-threshold operation of the pulse generator circuit, the output voltage is given by:

$$V_{OUT} = -\frac{R_1 I_{DS0}}{2}\left(e^{\frac{V_{IN1}(t) - V_{th}}{nV_T}} + e^{\frac{V_{IN2}(t) - V_{th}}{nV_T}}\right) + V_{CM} \tag{A-11}$$

$$V_{OUT} = -\frac{R_1 I_{DS0}}{2} e^{\frac{V_{CM} - V_{th}}{nV_T}}\left(e^{\frac{\alpha t}{nV_T}} + e^{\frac{-\alpha t}{nV_T}}\right) + V_{CM} \tag{A-12}$$

The Taylor series expansion for V_{OUT} at t=0 is expressed as:

$$V_{OUT} = -R_1 I_{DS0} e^{\frac{V_{CM} - V_{th}}{nV_T}}\left(1 + \frac{1}{2}\left(\frac{\alpha t}{nV_T}\right)^2 + \frac{1}{24}\left(\frac{\alpha t}{nV_T}\right)^4 + \ldots\right) + V_{CM} \tag{A-13}$$

If we represent the Gaussian pulse as:

$$V_{Gaussian}=Ke^{-\left(\frac{t}{\tau}\right)^2} \tag{A-14}$$

$$V_{Gaussian}=K\left(1-\left(\frac{t}{\tau}\right)^2+\frac{1}{2}\left(\frac{t}{\tau}\right)^4+\ldots\right) \tag{A-15}$$

Ignoring the higher order terms, and equating the quadratic terms of V_{OUT} and $V_{Gaussian}$ results in:

$$-\frac{R_1 I_{DS0} e^{\frac{V_{CM}-V_{th}}{nV_T}}}{2}\left(\frac{0.8(V_2-V_1)}{nV_T t_r}\right)^2=-K\left(\frac{1}{\tau}\right)^2 \tag{A-16}$$

$$t_r=\tau\sqrt{\frac{R_1 I_{DS0} e^{\frac{V_{CM}-V_{th}}{nV_T}}}{2}}\left(\frac{0.8(V_2-V_1)}{nV_T K}\right) \tag{A-17}$$

For Gaussian signal, the bandwidth of the pulse is calculated as:

$$f_{3dB}=\frac{\sqrt{Ln(2)}}{\pi\tau} \tag{A-18}$$

$$t_r=\frac{1}{f_{3dB}}\sqrt{\frac{Ln(2)R_1 I_{DS0} e^{\frac{V_{CM}-V_{th}}{nV_T}}}{2}}\left(\frac{0.8(V_2-V_1)}{nV_T K\pi}\right) \tag{A-19}$$

For Gaussian Monocycle pulse:

$$V_{Monocycle}=K\frac{-2t}{\tau^2}e^{-\left(\frac{t}{\tau}\right)^2} \tag{A-20}$$

$$Y(f)_{Mono}=K\tau\sqrt{\pi}(j2\pi f)e^{-(\pi\tau f)^2} \tag{A-21}$$

To find out the 3-dB bandwidth of the pulse spectrum, first the frequency (f_{MAX}), at which $Y(f)_{Mono}$ has its maximum value should be calculated as:

$$\frac{dY(f)_{Mono}}{df}=0 \longrightarrow f_{MAX} \tag{A-22}$$

The 3-dB bandwidth of the pulse is as follows:

$$\frac{Y(f_{MAX})_{Mono}}{2}=-K\tau\sqrt{\pi}(j2\pi f)e^{-(\pi\tau f)^2} \longrightarrow \begin{cases} f_{-3dBH} \\ f_{-3dBL} \end{cases} \tag{A-23}$$

$$BW_{Monocycle}=f_{-3dBH}-f_{-3dBL} \tag{A-24}$$

$$\tau=\frac{1}{\pi}\sqrt{\frac{1}{BW_{Mono}(f_{-3dBH}+f_{-3dBL})}Ln(\frac{f_{-3dBH}}{f_{-3dBL}})} \tag{A-25}$$

$$t_r=\frac{1}{\pi}\left(\frac{0.8(V_2-V_1)}{nV_TK}\right)\times\sqrt{\frac{1}{BW_{Mono}(f_{-3dBH}+f_{-3dBL})}Ln(\frac{f_{-3dBH}}{f_{-3dBL}})\frac{R_1I_{DS0}e^{\frac{V_{CM}-V_{th}}{nV_T}}}{2}} \tag{A-26}$$

If the rising and the falling times are not matched, the output pulse changes as follows:

$$V_{OUT}=-\frac{R_1I_{DS0}}{2}e^{\frac{V_{CM}-V_{th}}{nV_T}}\left(e^{\frac{\alpha t}{nV_T}}+e^{\frac{-\beta t}{nV_T}}\right)+V_{CM} \tag{A-27}$$

The Taylor series expansion for V_{OUT} at t=0 is as follows:

$$V_{OUT}=-\frac{R_1I_{DS0}e^{\frac{V_{CM}-V_{th}}{nV_T}}}{2}\left(2+\frac{(\alpha-\beta)t}{nV_T}+\frac{1}{2}(\frac{\alpha t}{nV_T})^2+\frac{1}{2}(\frac{\beta t}{nV_T})^2+\ldots\right)+V_{CM} \tag{A-28}$$

When the rising and falling times of the input pulse, are not equal, the term $\frac{(\alpha-\beta)t}{nV_T}$ starts dominating, and the shape of the signal deviates from a pure Gaussian pulse.