SI-CMOS-LIKE INTEGRATION OF ALGAN/GAN DIELECTRIC-GATED HIGH-ELECTRON-MOBILITY TRANSISTORS

A Dissertation

by

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ABSTRACT

GaN is a promising material for power and radio-frequency electronics due to its high breakdown electric field, thermal conductivity, and electron saturation velocity. Additionally, strong spontaneous and piezoelectric polarization properties enable the engineering of high mobility, high carrier density channels at III-Nitride heterointerfaces. In order to seize market share from silicon, the cost of manufacturing GaN-based devices must be further reduced. With the successful realization of 200mm GaN-on-Si wafers, one promising path for cost-reduction is parallel utilization of existing 200mm Si CMOS infrastructure. Additionally, leveraging of CMOS processing techniques (such as high-κ/metal gate, Si_3N_4 spacers, and self-aligned S/D contacts) would further reduce development and manufacturing costs and would lower technology learning curves enabling GaN to seize a significant market share in emerging markets such as renewable energy, electric vehicles, Smart Grid, telecommunications, and space electronics.

This work tackles the problems inhibiting the implementation of a Si-CMOS-like AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistor (MOSHEMT) technology. The primary roadblocks to a gate-first, CMOS-like flow are the lack of a viable self-aligned contact process and the lack of a robust gate dielectric capable of enduring the contact module.

The reported research began with the development of a Si-compatible baseline transistor technology in a 200mm Si CMOS environment and an exploration of the

impact of parallel integration of GaN and Si product. The ohmic alloy anneal was found to present the primary contamination hazard. Then, a self-aligned contact process was developed while simultaneously investigating dielectrics for low-leakage performance. Investigation of gate stacks indicated that ozone sourced ALD Al_2O_3 is most promising for minimization of interface trapping, while ALD BeO is best able to endure the ohmic anneal and enable low leakage performance. Finally, an initial self-aligned, gate-first MOSHEMT technology was implemented and challenges for future research were uncovered. Integration of the self-aligned contact module led to estimated cost savings of $170 (1% of front end fabrication cost) per wafer. As GaN power electronic production is projected to consume ~100,000 wafers per year by 2015 (Yole Development, "Power GaN – 2012 Edition"), this manufacturing breakthrough represents potential savings of ~$17 million per year.

To Morgan, Emsley, and Smudge… A man couldn't ask for a more loving family.

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NOMENCLATURE

ALD	Atomic layer deposition
AlGaN	Aluminum Gallium Nitride
CV	Capacitance-voltage measurement
CVD	Chemical vapor deposition
DI	Deionized
E_g	Bandgap energy
ε_r	Relative electric permittivity
ε_0	Electric permittivity of vacuum
E_c	Critical breakdown electric field
GaN	Gallium nitride
GV	Conductance-voltage measurement
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
IPA	Isopropyl Alcohol
IV	Current-voltage measurement
μ_n	Mobility of electrons
MBE	Molecular beam epitaxy
n_i	Intrinsic electron density
PDA	Post-deposition anneal
RIE	Reactive ion etching

SEM	Scanning electron microscope
Si-CMOS	Silicon complementary metal-oxide-semiconductor technology
TLM	Transfer-Length Method
TXRF	Total reflection X-ray fluorescence
Θ	Thermal conductivity
v_{sat}	Saturation velocity of electrons
XPS	X-ray photoelectron spectroscopy
XRR	X-ray reflectivity

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1. INTRODUCTION

1.1 Motivation

1.1.1 Material Properties

High-frequency, high-power switches are key components in modern power electronics and communication systems. The switching loss and output ripple of power converters and amplifiers are directly related to switching frequency making faster switches with high blocking voltage and current density all the more desirable. GaN-based transistors have received considerable attention for these high-frequency and power electronics applications. GaN is a wide bandgap material (E_g = 3.4 eV) with a critical electric field of over 3 MV/cm. This combined with its high electron saturation velocity and the large carrier sheet densities afforded by the polarization properties of the nitride material system enable power amplifiers with high power added efficiency, high output power, and high power density. The material properties of several competing material systems are compared in Table 1.

Table 1: Electronic and physical properties of competing material systems.

	Si	GaAs	GaN	AlN
E_g (eV)	1.1 (Indirect)	1.42	**3.39**	**6.2**
ε_r	11.7	12.9	8.9	8.5
μ_n (cm^2/V-s)	1350	8500	**2000 (2DEG)**	300
v_{sat} (10^7 cm/s)	1.0	1.0	**2.5**	1.4
E_{br} (MV/cm)	0.3	0.4	**3.3**	15
Θ (W/cm-K)	1.3	0.43	1.3	2.85
Hardness (Gpa)	11.5	7	13.4	11.8
Melting Point (°C)	1414	1238	2400	3200

The III-Nitride material system also enables extreme scalability. The high density of states in GaN combined with the large potential barrier of AlGaN enables formation of a well-confined channel with high free carrier density [1]. This enables vertical scaling. The high breakdown field, carrier mobility and saturation velocity (Table 1) enable lateral scaling while avoiding short channel effects. Extreme lateral scaling reduces parasitics and increases the cutoff frequency. The Johnson figure of merit (f_T x breakdown voltage) of GaN-HEMTs surpasses that achieved by SiGe, GaAs, and even InP HBTs [1].

1.1.2 Market Potential

GaN devices have applications in several emerging markets, providing the opportunity for explosive growth over the next ten years. These markets include Smart Grid power systems, renewable energy systems, electric vehicles, radio frequency and satellite communication systems, RADAR, and space electronics [2]. According to market analysis firm marketsandmarkets.com, the GaN power market alone (excluding optoelectronics) is expected to exceed $1.75 billion by 2022 by growing 60-80% annually over the next ten years [2]. However, another market research firm, Yole Devéloppement, had this to say regarding the present state of GaN technology, "GaN is not yet mature enough for the power electronics market – GaN needs technical enhancements in the manufacture process [3]." While excellent GaN-based transistor performance has been realized, the primary roadblock to widespread adoption is the high-volume manufacturability of the technology.

Improvement of GaN transistor technology with respect to manufacturability will both decrease the cost as well as ease the difficulty of integrating GaN products with the entrenched Si-based power electronics. As the silicon complementary metal oxide semiconductor (Si-CMOS) industry moves to larger substrates (300 mm in production, 450 mm in qualification), the utilization of older 200 mm fabrication infrastructure decreases. This provides an opportunity for younger technologies to enter high volume manufacturing with minimal equipment costs if compatible substrates and processes are developed. Additionally, larger substrates have the inherent benefit of driving down the processing cost per die. In order for GaN to take advantage of this infrastructure, 200 mm substrates must be developed and transistor technology must be adapted to employ only Si-CMOS-compatible materials. Integration costs of GaN could be furthered reduced through leveraging of standard Si-CMOS processing techniques and the implementation of a similar process flow (fewer development and learning costs). All of these manufacturing improvements would combine to make GaN-based power electronics more cost-effective and provide a stepping stone toward same-wafer integration of Si and GaN electronics.

1.2 Background

Now that the motivation and market potential of GaN-based electronics is clear, the device operating principles and prior work will be discussed.

1.2.1 Fundamental Physics

GaN-based high-electron-mobility transistors rely heavily upon inherent polarizations of the III-Nitride material system. III-Nitrides have an asymmetric crystal

structure resulting in dipole formation. This dipole leads to the formation of a spontaneous polarization field. III-Nitrides are also piezoelectric. An additional polarization field forms when nitride films are strained. Thus, through heterostructure engineering, high carrier density planes of charge can be realized at III-N interfaces. The majority of GaN-based transistor research focuses on the utilization of these interfacial charge planes as conduction channels.

1.2.2 Prior Work

As mentioned in Section 1.1, the current performance of AlGaN/GaN transistors is excellent. Enhancement mode high voltage switching has been realized for blocking voltages greater than 1 kV [4, 5]. Additionally, high frequency performance has been realized. Millimeter wave performance was realized back in 2010 with a breakdown voltage of 42V [6]. By 2013, f_{max} in excess of 500 GHz had been reported [1]. Efforts to balance frequency and breakdown voltage performance led to a transistor with 120 GHz f_{max} and 176V breakdown [7].

Having realized excellent performance, research is turning towards cost savings through optimization of the manufacturing process. 200 mm GaN-on-Si substrates were developed in 2012 to help make GaN more cost-effective [8]. This opens the door to taking advantage of the massive existing 200 mm Si-CMOS fabrication infrastructure. Implementation of Si-CMOS compatible technologies began in 2011 and remains heavily researched [8-13]. In particular, realization of low, uniform contact resistance, and uniform enhancement mode threshold voltage remain challenging. The next step after optimization of compatible technology is determination of the impact of actual

integration: cost, tool contamination, processing hazards. Preliminary investigations into these factors began over the past two years. Ga (a *p*-type dopant in Si) can arise from backside contamination in epitaxy chambers, from etch processes, and from anneal processes [14]. The thick silicon substrates required to maintain low wafer warp can cause calibration problems with wafer loading robots [8]. The full and long term impact of GaN integration into Si-CMOS lines remains to be determined.

In addition to compatibility, similarity to current Si-CMOS processing is also desired. Similar process flows will set the foundation for same-wafer integration of Si logic and GaN power switches. Additionally, the use of standard Si processes will decrease development times (lower costs) and decrease the learning curve for device engineers accustomed to Si technology. Little research thus far has been aimed toward a Si-CMOS-like GaN technology. Current Si transistors start with isolation, then process the gate module to set device geometries. A Si_3N_4 spacer is combined with self-aligned contacts to maintain extreme lateral scaling. Gate-first processing is not common within GaN technologies for two reasons. First, an affordable, manufacturable self-aligned contact process does not exist. A self-aligned process has been reported [1, 6, 7], but the process requires molecular beam epitaxy (MBE) GaN regrowth in the contact windows. MBE systems are extremely expensive and limit throughput to about 1 wafer per day. This is not a high volume manufacturable solution. Second, the high temperature anneals typically required for ohmic contact damage the dielectric/GaN interface leading to large leakage currents. Significant work on dielectric/GaN interfaces has transpired [12, 15-21], but the primary focus has been on as-deposited interfaces.

2. PROPOSED DEVICE

The aim of this research is to lower manufacturing costs of GaN-based HEMTs through refinement of Si-CMOS-compatible technology and by leveraging standard CMOS processing techniques while maintaining performance similar to presently available HEMT technology. A cross-section of the proposed technology is shown in Figure 1. The technology will implement a gate-first process flow with a dielectric spacer and self-aligned contact module. The bulk of the research will focus on developing an Au-free self-aligned ohmic contact process (Figure 1C) and improving the dielectric / AlGaN interface (Figure 1A) to minimize interface trap density and maintain low gate-leakage current while enduring an ohmic contact anneal.

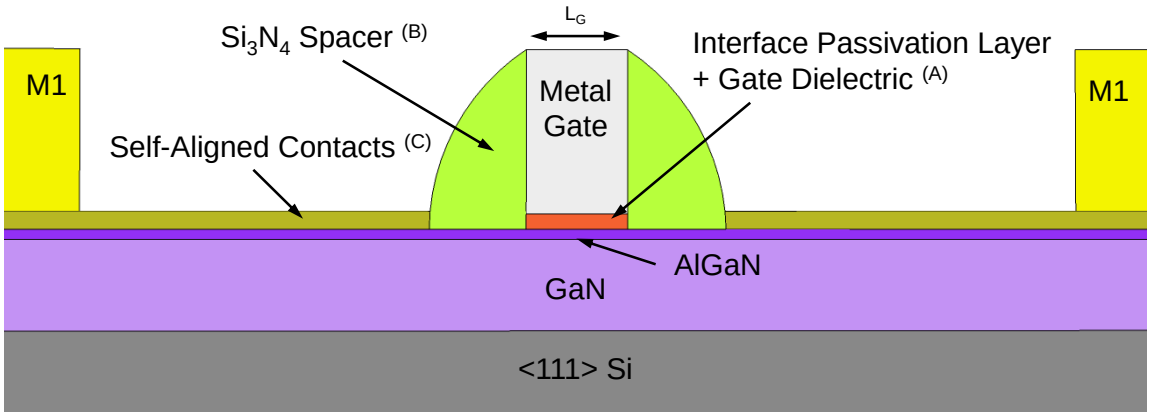

Figure 1: Cross-section of proposed device technology.

General technology performance goals are detailed below (Figure 2). The cutoff frequency and on-resistance are closely related as the cutoff frequency is limited by on-

resistance. The cutoff frequency and breakdown voltage provide a design trade-off. The most common method for increasing the breakdown voltage is to increase the gate-to-drain spacing. Increased spacing leads unavoidably to a higher on-resistance and lower cutoff frequency. Self-aligned processes lend themselves to extreme lateral scaling, so high frequency, and low on-resistance are expected at the cost of break down voltage. Leakage current should also be minimized in order to keep off-state power dissipation low.

Performance Goals	
f_T (GHz)	>20 GHz
R_{ON} (Ohm*mm)	<5
R_C (Ohm*mm)	<1
$I_{D,max}$ (A/mm)	>0.2
V_{br} (V)	>10
$I_{G,leak}$ (A/cm^2)	<1E-5

Figure 2: Performance goals of proposed technology.

This research progressed in the following manner. First, a gold-free, gate-last baseline transistor technology was integrated with performance similar to present state of the art power HEMTs. Second, an Au-free self-aligned contact module was developed. In general for GaN technology, higher temperature anneals lead to lower contact resistances; however, high temperature anneals also damage the dielectric / AlGaN interface and lead to high leakage currents. In parallel to contact development, a variety of dielectric / AlGaN interfaces will be explored via XPS and electrical characterization

to determine their temperature stability. Interface trap density (determined through *CV* methods) and gate leakage will be monitored and compared to the baseline technology in order to select the most favorable gate dielectric. Finally, after developing a low resistance self-aligned contact module and robust gate stack, a Si-CMOS-like technology will be integrated to demonstrate the viability of the processes.

3. BASELINE AU-FREE TECHNOLOGY DEVELOPMENT*

3.1 Process Integration

Figure 3 shows the cross-section of a baseline transistor technology that was integrated in an active 200 mm Si-CMOS line during the spring and summer of 2012. Similar to prior reports, the technology employed a gate-last process flow including an Au-free contact module, depletion mode switching operation, and an atomic layer deposition (ALD) HfO_2 gate dielectric to ensure low gate-leakage performance. The novelties of the work included processing in an active Si-CMOS fab, a low-temperature (575 °C) Ta-based contact module, and enhancement mode operation through interface charge trapping. Most deposition and etch processes were developed in line on 4-in GaN-on-Si wafers using 200 mm Si pocket wafers, and tool contamination was monitored via TXRF. The exception was the gate module (ALD HfO_2, electron beam evaporated nickel) which was processed at Texas A&M University.

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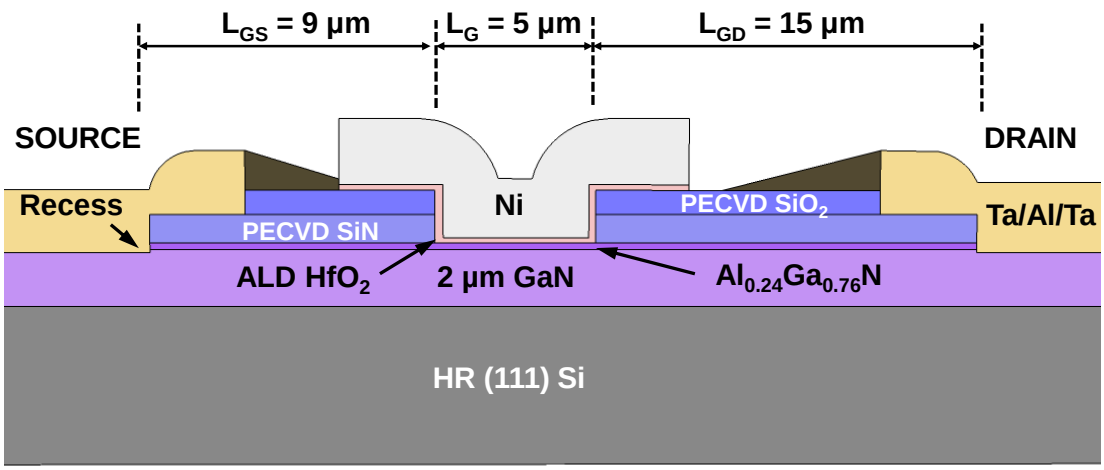

Figure 3: Cross-section of Au-free, gate-last baseline transistor technology.

An overview of the process flow is illustrated in Figure 4. The flow was a short-loop flow consisting of 5 mask layers containing primarily test structures. Processing began with inter-device isolation, moved into the ohmic source/drain contact module, and concluded with the gate module. The development of the individual modules will be discussed in detail below.

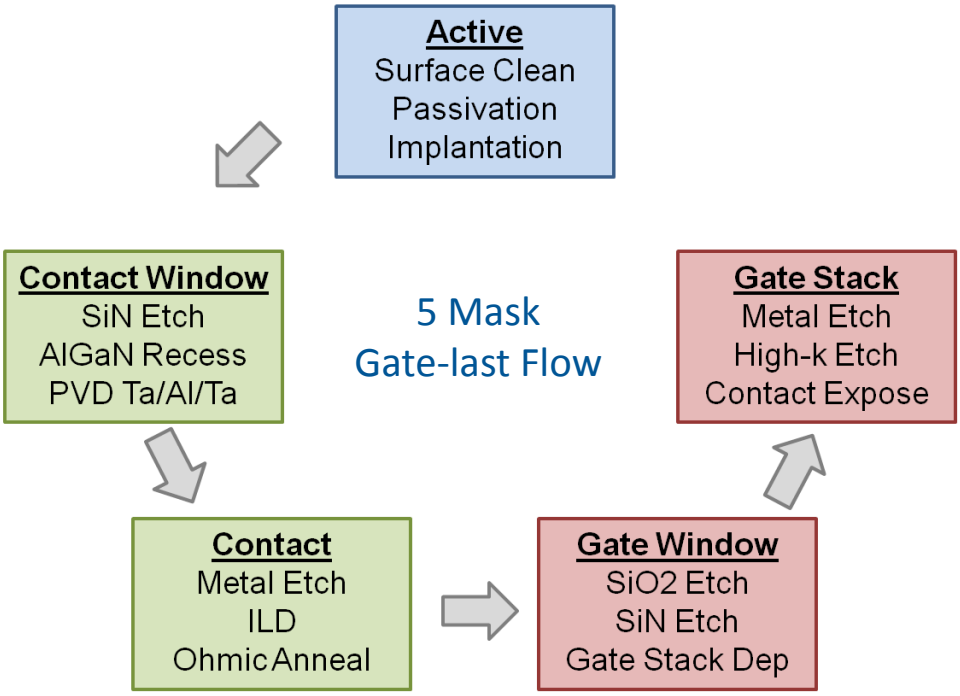

Figure 4: Process flow overview.

3.1.1 Isolation Module

The isolation module includes initial wafer cleaning, surface state passivation, and inter-device isolation. The process flow began with a solvent clean (Acetone / IPA / DI water, 2 min each) to remove carbon contaminants, and a 10 minute dilute HCl (10:1 DI H_2O:HCl) native oxide strip. Finally, wafers were rinsed in DI water and blown dry with N_2. Immediately after clean, the wafers were loaded into an Applied Materials Precision 5000 for PECVD deposition of 90 nm of SiN_x at 410 °C for surface state passivation. Silicon nitride has been demonstrated to act as an effective barrier between moisture and AlGaN surface states thereby improving the channel carrier concentration and limiting current collapse and virtual gate effects [22-24]. Wafers were then patterned

with the active layer and the SiN_x was etched using buffered oxide etch (BOE). After etch, the photoresist was left in place to act as a mask for the subsequent ion implantation isolation.

The two most commonly employed methods for inter-device isolation in GaN technologies are ion implantation and mesa isolation (shallow trench isolation). Little systematic research has been performed into mesa isolation for GaN; the performance impacts of sidewall surface states and methods for passivating these states are not well understood. Most of the prior research has focused on implantation due to its simplicity and the way it lends itself toward planar devices without the need for chemical mechanical polishing (CMP). The little comparative work that has been reported has shown implantation to also yield better transistor performance [25]. Electrical isolation has been demonstrated using hydrogen, helium, boron, nitrogen, oxygen, phosphorus, argon, iron, titanium, and chrome ion implantation [26-31]. Implantation relies on two different mechanisms leading to isolation. First, radiation damage creates mid-gap carrier traps. Second, mid-gap energy levels can be created by chemical incorporation/substitution of the implanted species. This second component typically leads to better thermal stability of the high-resistance isolation. For these reasons, ion implantation was selected for use in this process.

Nitrogen implantation has been frequently reported in literature along with typical energy and dose parameters. Typical schemes target vacancy densities of ~5E20 cm^{-3} to a depth of more than 500 nm to ensure that the 2DEG is fully removed and conduction down through the GaN buffer is suppressed. Stopping Range of Ions in

Matter (SRIM) simulations were used to confirm the necessary energy and ion doses (Figure 5). After implantation a 1 min piranha clean (3:1:1 H_2SO_4:H_2O_2:H_2O) at 80 °C was employed to ensure removal of the implant-hardened resist. The sheet resistance of the implanted region was on the order of 10^{12} Ω/sq and is expected to be stable up to 600 °C [32-34].

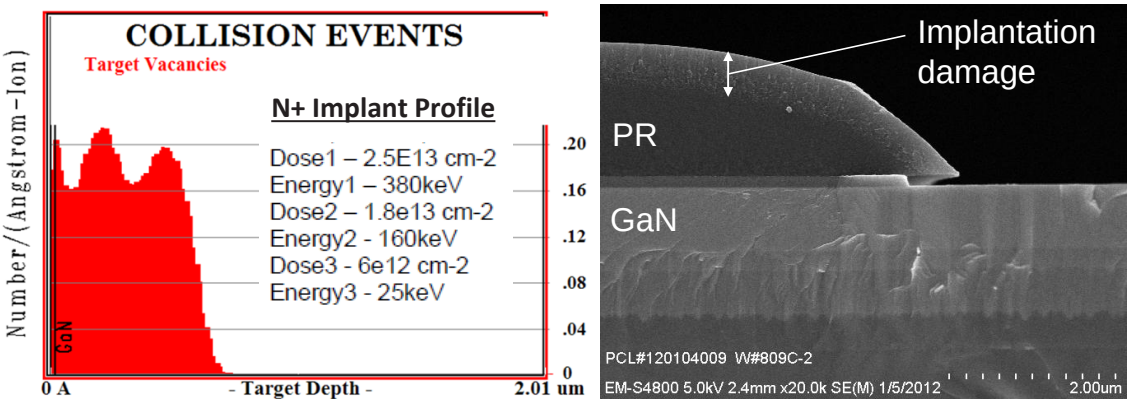

Figure 5: A) Vacancy profile from triple energy N+ implantation generated by SRIM simulation. Dose and energy details are shown (inset). B) Cross-section SEM micrograph taken after implantation showing the ion penetration depth into the masking layers.

3.1.2 Contact Module

The contact module includes the contact window lithography, a SiN_x plasma etch, an AlGaN recess etch, contact metal sputtering, metal patterning, metal etch, and ohmic alloying anneal. Process development began with the SiN_x plasma etch. An Applied Materials Centura Super E system was used for reactive ion etching. Etch development focused on the realization of the following goals: high etch rate selectivity

to SiN_x over III-Nitrides, steep sidewalls (>45°) and limited undercut for accurate pattern transfer, and low bias power to avoid plasma damage of the AlGaN barrier (especially critical for the gate module). CF_4 plasmas are commonly used to etch SiN_x and are not expected to etch GaN [35]. For these reasons, etch development began with the following plasma conditions: 150 sccm CF_4, 30 mtorr, 750W ICP power, room temperature. Bias power was varied from 5W to 80W.

The first problem we ran into during etch development was photoresist reticulation. Due to the decreased thermal conductivity between the live wafer and the pocket wafer, the photoresist burned during long or high power etches (Figure 6). In order to address this problem, we adopted a cyclical etch scheme: 30 seconds of etching followed by two minutes of rest before resuming the etching for another 30 seconds. A cross-section SEM micrograph of a cyclically etched sample is shown in Figure 6D.

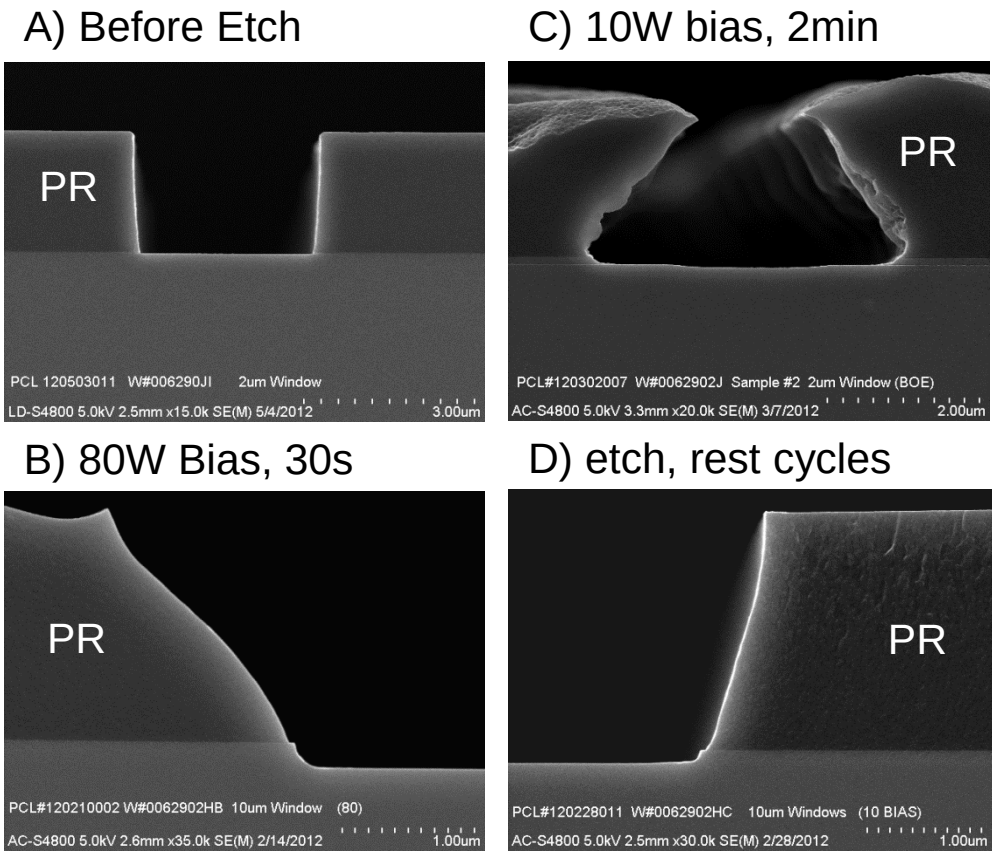

Figure 6: A) Cross-section SEM of photoresist profile before etching. B) Photoresist profile after an 80W etch showing the beginning of resist reflow. C) Resist profile after long, low power etch showing extreme reflow and burning. D) Resist profile achieved using 10W 30s etch + 2min rest cycles.

After overcoming the photoresist reticulation issue, we ran a low bias power split to find the minimum bias power at which pattern transfer was maintained. Prior studies have shown that fluorine-based plasmas with less than 10W of bias power are sufficiently gentle to avoid damaging the AlGaN surface [32]. We ran etch tests at 10W, 7W, and 5W bias. SEM images of the resulting profiles are shown in Figure 7. Images in row 1 show that photoresist reflow was avoiding in all three cases. Row 2 contains high-

magnification images showing the SiN_x sidewall angles. The 7W plasma was the lowest power etch to also achieve steeper than 45° sidewalls. For this reason, it was selected for use in both the contact and gate modules. The tilted images in row 3 show that no "grass" or polymer residue is left behind by the etch.

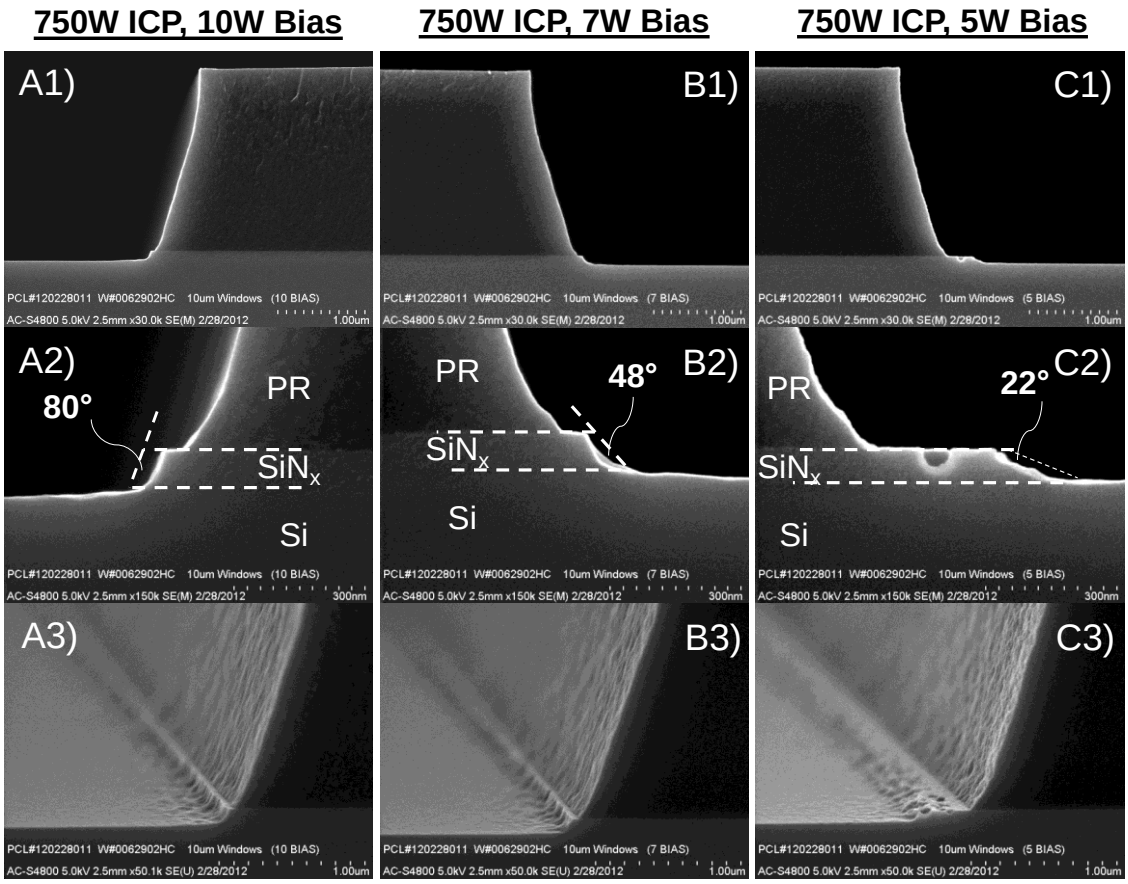

Figure 7: All etches were performed with 150sccm CF_4 and 750W ICP power at 30mtorr and room temperature. Total etch time was 78 seconds. Bias power was varied: 10W (Column A), 7W (Column B), and 5W (Column C).

After completion of SiN_x etch development, we began process development on the AlGaN barrier recess etch. Recessing the AlGaN barrier exposes the 2DEG for contact and has been shown to improve the contact resistance and uniformity [8, 10]. The same Applied Materials Centura Super E etching system that was used for the SiN_X etch was used for the AlGaN etch. The following etching conditions were employed: 25 sccm Cl_2, 25 sccm Ar, 20 mtorr, 300W ICP, 50W bias, and room temperature. Low power was used to avoid resist burning and because we believed a shallow slope would improve contact metal adhesion at the AlGaN/GaN interface. Previous reports indicated risk of Ga tool contamination when etching GaN [14], so dummy silicon wafers were processed (one face up, and one face down) after GaN etches and analyzed using TXRF to monitor contamination. Ga concentrations in excess of $5x10^{10}$ atoms/cm^2 were deemed failures. No failures were observed after recess etching, so we concluded that this plasma simultaneously removed Ga byproduct from the chamber walls while etching the GaN film. The target etch depth was 20 nm to ensure full removal of the AlGaN barrier.

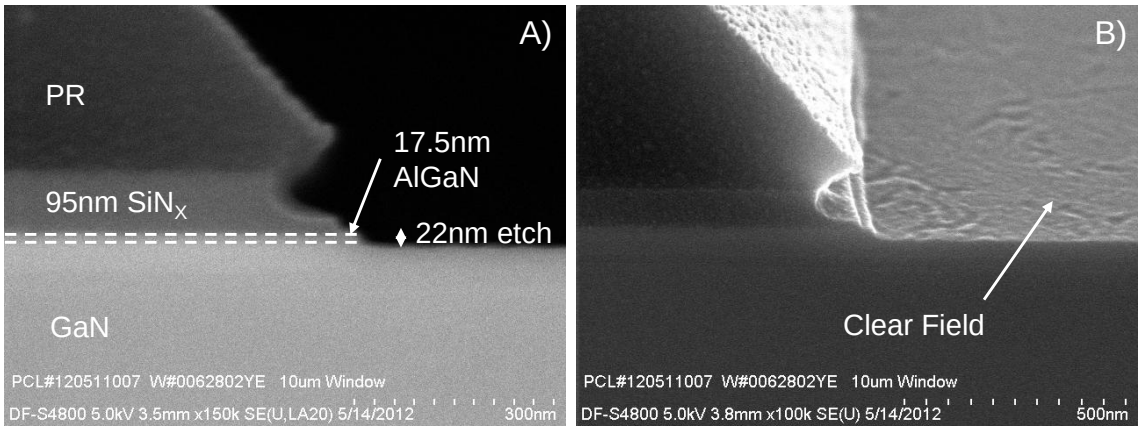

Figure 8: A) Cross section SEM of the developed AlGaN recess etch. About 100 nm of undercut by the Cl_2 plasma into the SiN_x is observed. B) No grass is visible in the field region, and the roughness is similar to the starting GaN surface roughness.

After completion of the AlGaN recess, the focus of development shifted to the contact metal etch. Before deposition of the contact metal, the photo resist was ashed in an O_2 plasma and wafers were cleaned for 2 minutes in 10:1 DI-H_2O: HCl. A Canon Anelva C-7100 system was used to sputter 7 nm / 200 nm / 20 nm of Ta / Al / Ta. Tuning of the metal dry etch turned out to be challenging due to the large difference in material properties between Ta and Al. A purely chlorine-based plasma was initially employed, but etches led to large Al undercut (Figure 9A). We found the Cl_2 / BCl_3 ratio to be critical in combating this undercut. We broke the etch into two steps: a main etch step with 1:1 Cl_2:BCl_3 ratio and an over etch step with 1:2 Cl_2:BCl_3 ratio. Both steps used 200W ICP, 75W bias, and 10 mtorr chamber pressure. SEM images of the optimized etch are shown in Figure 9B and C. The back-scatter image in Figure 9B highlights the removal of all metal residue. After etching, the photoresist was stripped using an oxygen plasma.

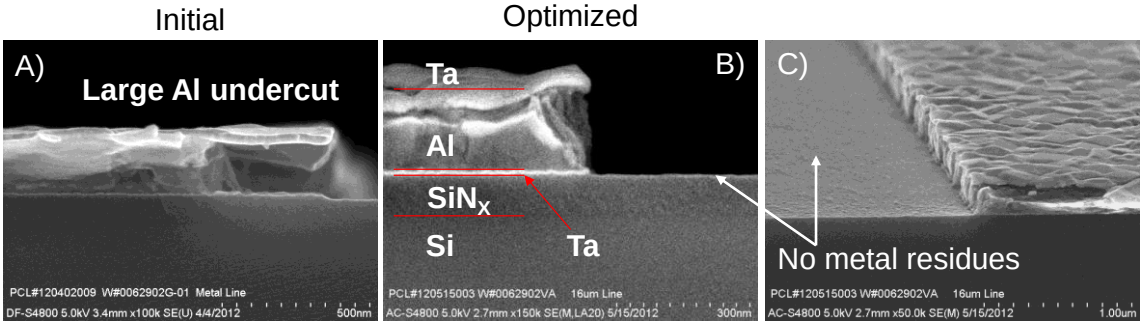

Figure 9: A) Cross-section SEM of initial contact stack RIE. B) Cross-section SEM of the optimized etch. C) Tilted SEM showing a smooth, clear field after etch.

The next step in the contact module was the ohmic contact alloying anneal. In addition to alloying the metal stack, annealing enables gettering of nitrogen from the III-Nitride surface resulting in nitrogen vacancies which act as n-type dopants [36-38]. Initial attempts to utilize a flash anneal process led to wafer breakage due to the large thermal expansion coefficient mismatch between GaN and Si. In order to avoid breakage, a cylindrical rapid thermal processing (RTP) system was used. Cross-section SEM images are shown before and after anneal in Figure 10. Anneal without encapsulation led to tool contamination with Ga and Ta (as determined by TXRF). Encapsulation with either PECVD SiO_2 or Si_3N_4 mitigates the contamination; however, oxygen was found to out-diffuse from the SiO_2 into the ohmic metal during anneal and make the contact vulnerable to BOE etching during subsequent interconnect processes. For this reason, Si_3N_4 is recommended for use as an encapsulation dielectric.

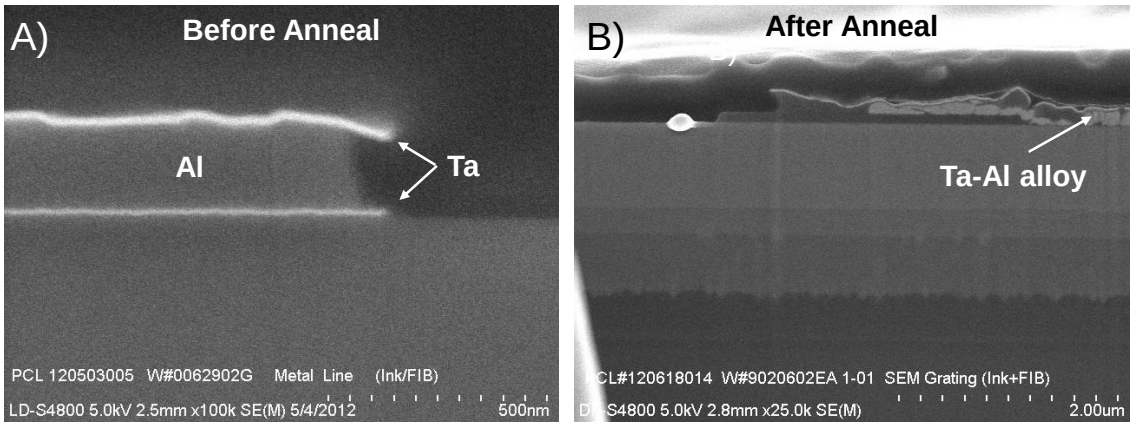

Figure 10: A) Sputtered Ta-Al-Ta contact stack before anneal. B) Contact edge after ohmic anneal (575 °C, 4 min, N_2 ambient). Agglomeration and formation of bright Ta-Al alloyed regions are visible.

Upon completion of the contact module, electrical measurements were performed on TLM test structures to extract contact resistance. After the initial short loop through the contact module, the electrical measurements revealed a major problem. Figure 11 shows the resistance (normalized by contact width) versus TLM spacing plot for the devices fabricated as described above. Reference TLM data without nitride passivation on a similar nitride heterostructure is included where no superfluous effects are observed. Although ohmic behavior is observed, the extracted contact resistance is negative, indicating an error in spacing estimation or a secondary, parallel conduction path.

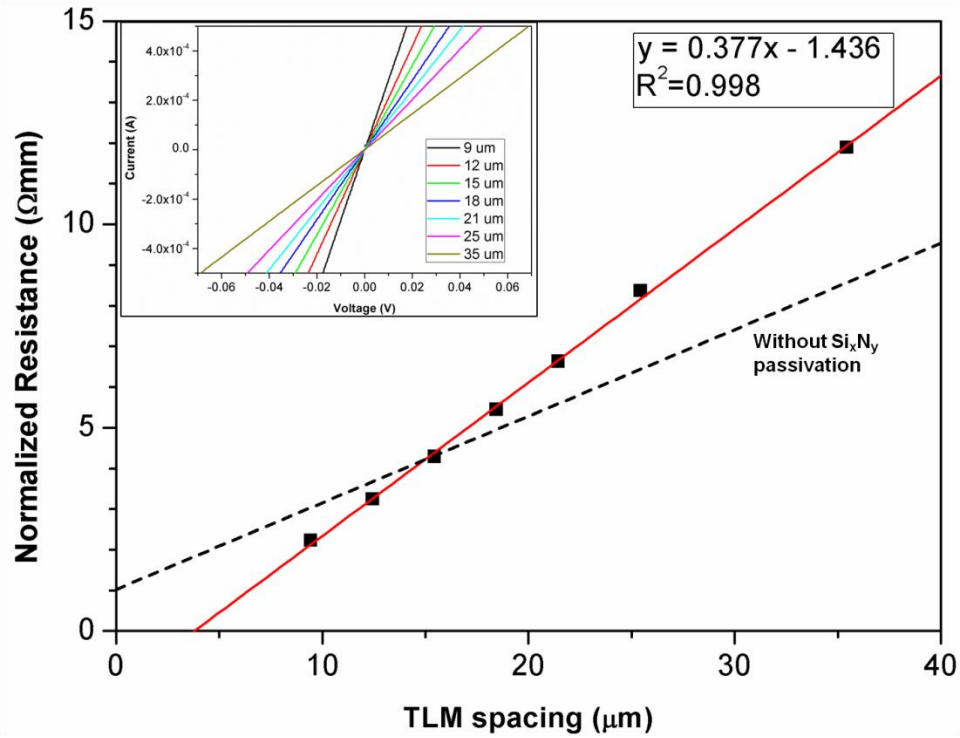

Figure 11: Plot of normalized resistance versus TLM spacing for ohmic contact structures integrated with (solid line) and without Si_xN_y passivation (dashed line). The y-intercept, which gives twice the contact resistance, is negative. Inset: I-V data for sample with passivation.

Figure 12 shows a STEM image and corresponding EDX line scan acquired along the line shown near the contact window edge after the post-metallization anneal. Since there is overlap between the Ta-M and Si-K lines, we report the Ta-L signal to aid in the decoupling of Si and Ta composition. Hence, an increase in the Si-K signal without a simultaneous increase in the Ta-L signal is attributed to a true increase in silicon composition. Similarly, a Ta Auger line interferes with the Ga-L line leading to an increase of the Ga signal in Ta-rich regions (far right of Figure 12C). Aluminum has diffused into the Si_xN_y passivation layer forming a layer of aluminum-diffused silicon

nitride (abbreviated as Al-Si-N). The Al is believed to originate from the Ta-Al ohmic metal alloy, not from the AlGaN. SIMS profiles collected before and after anneal indicated little change in the Al concentration of the AlGaN. Additionally, the Al diffusion is observed to taper off in regions further from the contact metal edge. The nitrogen signal observed throughout the EDX linescan is physical and arises from multiple sources. Ta is expected to getter nitrogen from the III-N during alloy anneal due to the low enthalpy of formation of TaN, and nitrogen may have out-diffused out from the Si_xN_y.

Figure 13 shows another STEM image and corresponding EDX linescan captured outside the contact metal edge. Again, Al has diffused into the Si_xN_y layer forming Al-Si-N, in this region, preferentially along the Si_xN_y/AlGaN interface. Hence, from the STEM image and EDX scans it is clear that there is significant Al diffusion into the Si_xN_y passivation layer, more than 0.5 μm beyond the metal overlay (~3 μm). The observation of nitrogen out diffusion and aluminum in-diffusion calls the quality of the PECVD Si_xN_y into question.

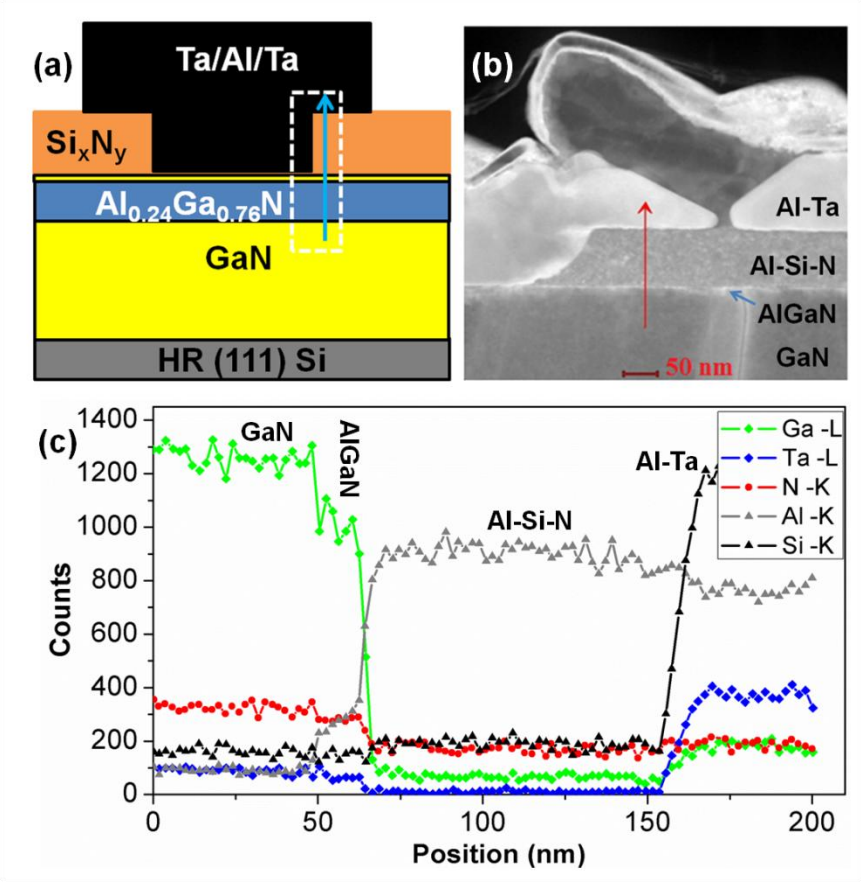

Figure 12: (a) Cross section schematic showing the position (contact window edge) of the STEM image and the EDX linescan. (b) STEM image at the contact window edge. Agglomeration and formation of multiple Ta-Al phases due to the alloying anneal are visible. (c) EDX linescan along the line marked in (b). Aluminum has diffused into the Si_xN_y layer forming Al-Si-N.

Diffusion of Al has been previously reported in Si_xN_y containing oxygen impurities and has been extensively studied by H. Ogata *et al*. [39]. The in-depth aluminum diffusion profiles observed by Ogata *et al*. reveal that Al diffuses completely through a 50 nm thick Si_xN_y film after a 60 min anneal at 530 °C. Oxygen impurities are common in PECVD films and likely contribute to the Al diffusion; however, in our

study, the STEM image of Figure 13B indicates that aluminum has diffused more than 0.5 µm after just a 4min anneal at 575 °C. Hence, the rate of aluminum diffusion is significantly accelerated (greater than 50 times) as compared to the rate observed in reference [39]. This suggests an additional mechanism driving the formation of Al-Si-N.

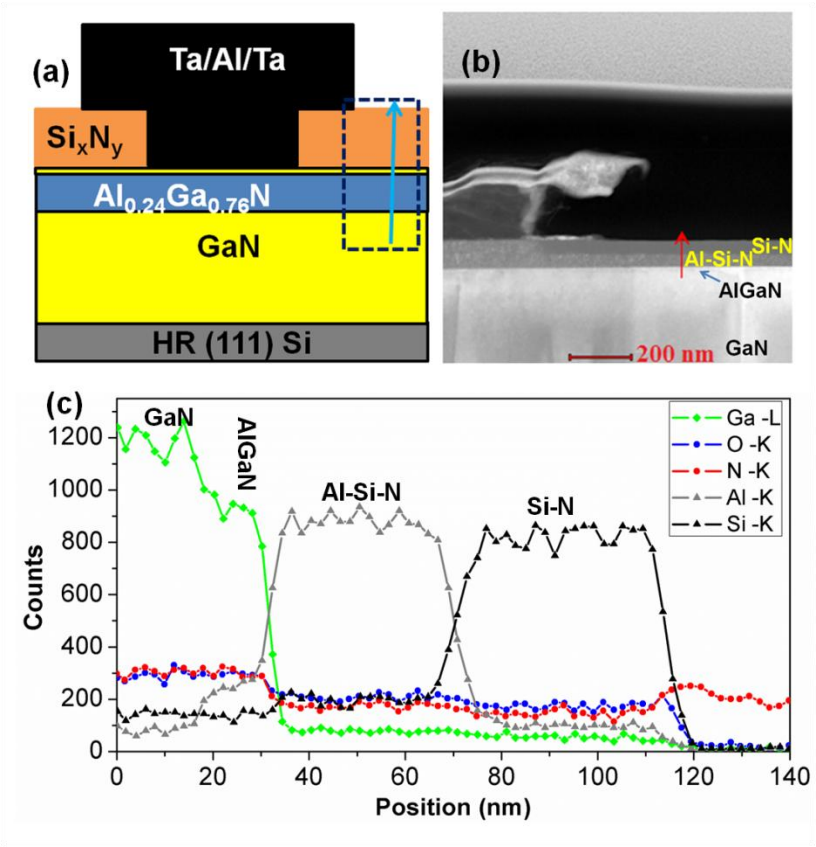

Figure 13: (a) Cross section schematic showing the position (outside the metal overlay) of the STEM image and the EDX linescan. (b) STEM image outside the contact metal overlay (c) EDX linescan along the line marked in (b). Instead of a single Si_xN_y layer, there is also a thin Al-Si-N layer in contact with the AlGaN/GaN heterostructure implying a density and/or compositional gradient in the Si_xN_y.

Formation of Al-Si-N affects the extraction of contact resistance through TLM in the following manner. The conducting channel length (effective TLM spacing) is no longer defined by lithography. The diffusion of Al enables contact beyond the contact window which reduces the channel length. Here we see as much as a 7 μm reduction: 2 x 3 μm metal overlay + 2 x 0.5 μm Al diffusion beyond overlay. Hence, instead of using the designed TLM spacing, a reduced spacing must be used in the contact resistance extraction. This spacing is difficult to accurately determine as the conductivity of the Al-Si-N layer is unknown and presumably varies with the Al content. Obtaining a negative value for contact resistance is sufficient for suspecting Al-Si-N formation, but it is not a necessary condition. Since, the TLM spacing reduction depends on the amount of diffusion of Al into the Si_xN_y film, it is also possible to obtain seemingly low values for contact resistance (non-negative). It should also be noted here that the non-uniformity of extracted contact resistance across the wafer is yet another indication of the poor quality of the deposited Si_xN_y. Figure 14 shows *R* versus *d* plot from a different region of the wafer. The extracted contact resistance is 0.01 Ω·mm which can be incorrectly interpreted as an extremely good ohmic contact. Moreover, further processing could include the formation of a gate for use as a HEMT. If Al diffusion into Si_xN_y goes unnoticed, breakdown voltage will degrade due to reduced gate-to-source and gate-to-drain lengths. In the case of extreme lateral scaling, the device may even be shorted. Hence from a process development standpoint, it is crucial to ensure that Al-Si-N is not formed during process integration.

XRR performed on blanket as-deposited silicon nitride on an AlGaN/GaN substrate revealed that the density of the Si_xN_y layer was around 4.4 $g \cdot cm^{-3}$ indicating a highly Si rich layer [40]. Also, the calculated N/Si ratio from the EDX linescan (Figure 13C) is around 0.5, congruent with the conclusion made from XRR. Hence, we infer that a Si-rich Si_xN_y passivation layer leads to accelerated diffusion of Al, resulting in inaccurate extraction of contact resistance. It was also observed that the Si_xN_y density on a Si control sample (also processed in a pocket wafer) was approximately 2.5 $g \cdot cm^{-3}$. This value is similar to the qualified value for the standard 200mm CMOS process, indicating that the change in thermal conduction due to the pocket wafer is not the primary cause of the density change. Moreover, post deposition anneal of Si_xN_y in nitrogen ambient, prior to the ohmic contact module, did not inhibit Al diffusion. Hence Si_xN_y PECVD (and likely all CVD processes) must be optimized on AlGaN/GaN directly, separate from the standard Si process, to achieve a proper index of refraction, density, and etch rates.

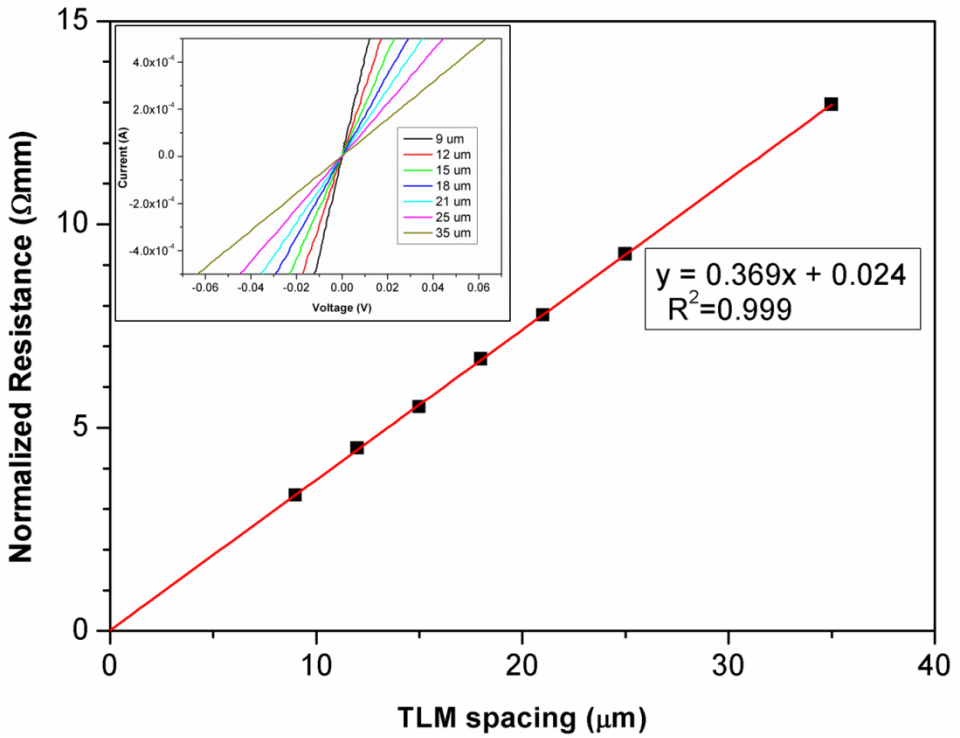

Figure 14: TLM plot from an alternate region of the substrate. The contact resistance can be incorrectly interpreted as being extremely low due to Al diffusion. Inset: I-V data for corresponding test structures.

In order to ensure accurate contact resistance extraction, the PECVD Si_xN_y was optimized on AlGaN/GaN on Si substrates using index of refraction and BOE etch rate as controlling variables. Initial pump down and N_2 purge times were increased to 10 minutes each to minimize residual oxygen in the chamber. Final deposition conditions employed were 600 mtorr, 125 sccm 1% SiH_4/N_2, 700 sccm N_2, 15W RF power, and 350 °C. The resulting film had an index of refraction of 1.98 and a BOE etch rate of ~50 nm/min. The Si-rich film had a higher index of refraction and a negligible BOE etch rate. Further increasing the nitrogen content decreases the index of refraction [40-42]

and quickly increases the etch rate. Extremely nitrogen rich PECVD Si_xN_y (BOE etch rate of ~150 nm/min), while mitigating the Al diffusion issue, was found to increase leakage currents. A resistance versus TLM spacing plot is shown in Figure 15 for ohmic contacts integrated using the optimized PECVD Si_xN_y film. Mean contact resistance of 0.20 Ω*mm was achieved, and the effective sheet resistance (slope of the fit line) increased relative to the previous data (Figure 11 and Figure 14), confirming removal of the secondary conduction path. The sheet resistance observed here (402 Ohms/sq) also matches the initial sheet resistance observed through Hall measurements before processing (~400 Ohm/sq).

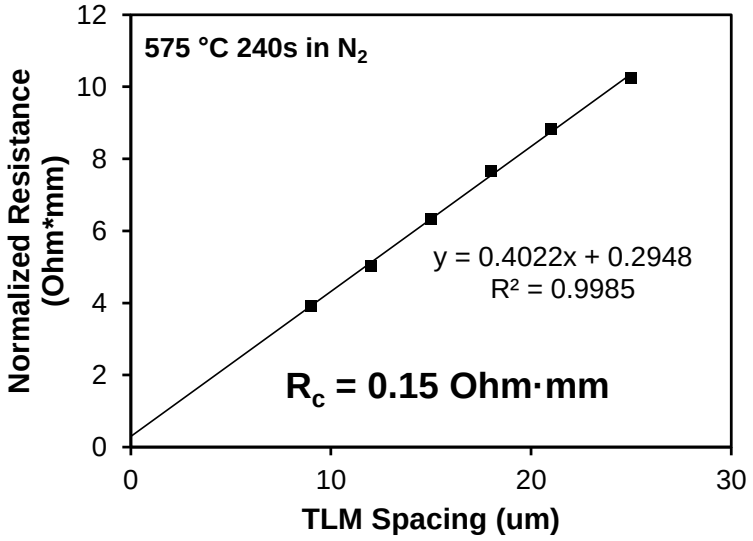

Figure 15: TLM plot from short loop ohmic contacts integrated using the re-optimized PECVD Si_xN_y.

3.1.3 Gate Module

The gate module includes the gate window lithography, etch, gate stack deposition, and gate stack patterning. Before processing of the gate module, 50 nm of SiO_2 was deposited by PECVD at 400 °C to protect the contact module. As mentioned in the previous section, we later found that oxygen from SiO_2 diffused into the contact metals making them vulnerable to etching in BOE. This resulted in thinning of the metal traces during removal of the isolation dielectric after processing of the gate module. The performance impact of the diffusion will be discussed in more detail in Section 3.1.4.

Process development began with the gate window etch. After lithography, 50 nm of SiO_2 and 90 nm of Si_xN_y needed to be etched. In order to avoid resist burning, a wet etch was used to remove the SiO_2: 3 minutes and 45 seconds in 1:30 HF:DI-H_2O. The wet etch was followed by the same Si_xN_y plasma etch developed for the contact module. The etch time had to be increased slightly to account for densification during the ohmic contact anneal. The resulting profile is shown in Figure 16. After opening the gate window, the photoresist was ashed in an oxygen plasma.

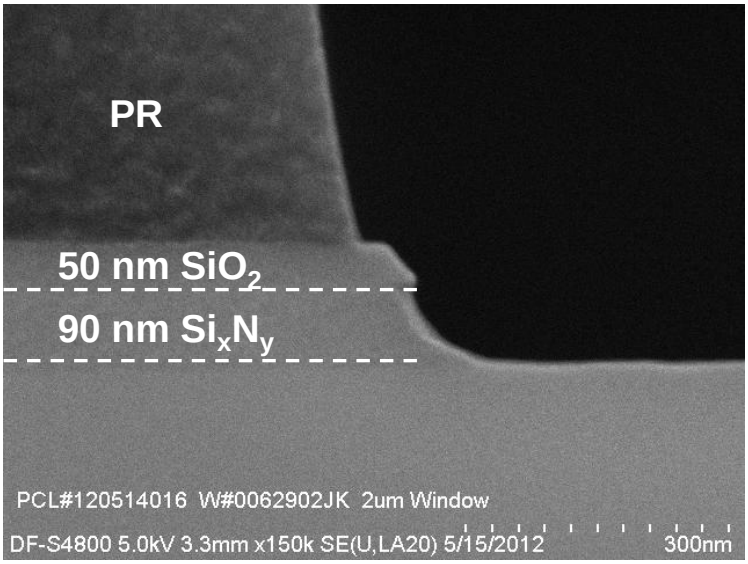

Figure 16: Cross-section SEM of the gate window after dry etching the Si_xN_y. No undercut or field residue is observed.

The next step in the process was the deposition of the gate dielectric. Due to the high electric fields induced by large blocking voltages, gate dielectrics are necessary to keep leakage currents low. Atomic layer deposition was performed using DI-H_2O and Tetrakis-(ethylmethylamino)hafnium (TEMAH) precursors to deposit 150 cycles of HfO_2 at 200 °C. Samples were cleaned in 1:10 HCl:DI-H2O for 2 minutes immediately prior to introduction to the ALD system. No post-deposition anneal was used. An interfacial GaO_xN_y was observed at the HfO_2 / GaN interface using TEM (Figure 17A). The composition of the interlayer was confirmed by performing XPS on blanket samples with thin (3 nm) HfO_2 (Figure 17B). A lower energy GaO_xN_y (Ga^{1+}) binding state was observed in the Ga 2*p* spectrum, 0.4 eV below the GaN core peak. The impact of this state will be discussed in more detail in Section 3.1.4.

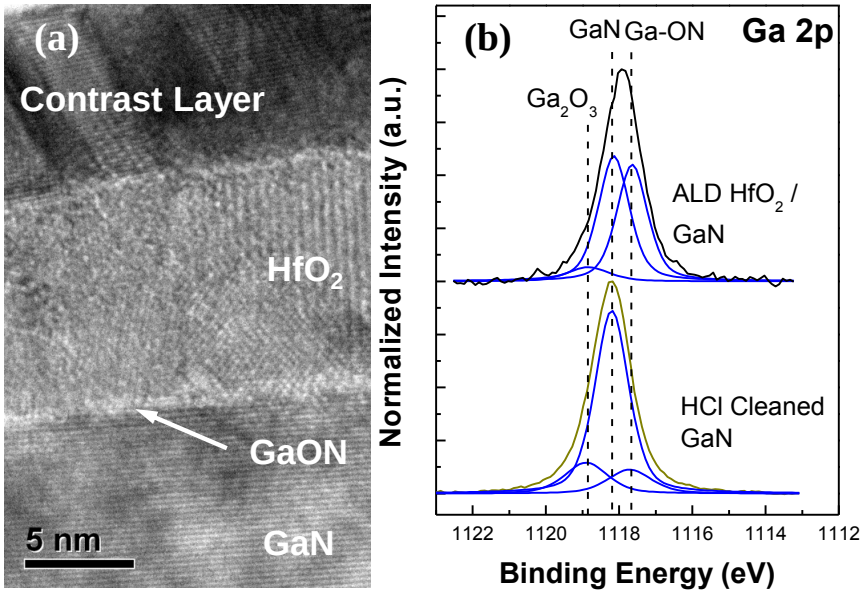

Figure 17: A) Cross-section TEM of the HfO_2 / GaN interface showing the presence of a 2 nm GaO_xN_y interlayer. B) XPS spectra of the Ga 2*p* region before and after ALD deposition.

Nickel was evaporated, patterned by liftoff, and used as a masking layer to etch the HfO_2 gate dielectric. GaN HEMTs typically employ high work function metal gates in an attempt to shift the threshold voltage toward the positives [43]. An Oxford Plasmalab 100 RIE system was used to etch the HfO_2. The etch conditions were 20 sccm SF_6, 10 sccm Ar, 50 W RF Bias, 500W ICP, 10 mtorr, and 23 °C. This plasma etches ALD HfO_2 at 23 nm / min. Finally, the wafers were soaked in BOE to strip the remaining SiO_2 isolation dielectric so that the ohmic contacts could be probed. The electrical performance of the baseline transistor technology is discussed in the following section.

3.1.4 Baseline Performance

Upon completion of the process, electrical measurements were made to provide a baseline to compare future experiments against. C-V and G-V measurements were performed using an Agilent E4890A precision LCR meter in parallel mode. Step size of 0.05 V, dwell time of 90 ms, and AC magnitude of 20 mV were used. A Hewlett-Packard 4145 parameter analyzer was used for I-V measurements. In all cases, measurements were performed in the dark at room temperature, and voltage was swept from low to high.

Figure 18 presents the I_D-V_D and I_D-V_G (inset) performance of the baseline transistor. Maximum drain current is found to be 236 mA/mm at V_G-V_T = 4.5V and V_{DS} = 10 V. Sub-threshold slope (SS) of 67 mV/dec was achieved with I_{on} / I_{off} ratio greater than 10^8 when measured at V_{GS} = +/- 5 V. Off-state gate leakage current was less than 10^{-9} A/mm (1 x 10^{-6} A/cm^2). Maximum transconductance was 55 mS/mm, and R_{ON} was 41.3 Ω·mm (L_{DS} = 29 μm). The increased R_{ON} is primarily due to the increased parasitic resistance of the thinned source / drain traces. The breakdown voltage was > 100 V, the limitation of the measurement system. This performance is comparable to that of other Au-free technologies (See Figure 24) [8-10, 12, 44]. Additionally, contact resistance of 0.79 Ω*mm was realized despite using a low-temperature anneal. In a similar report, Ti-based contacts using a similar anneal temperature were implemented but resulted in a contact resistance of ~1 Ohm*mm [8].

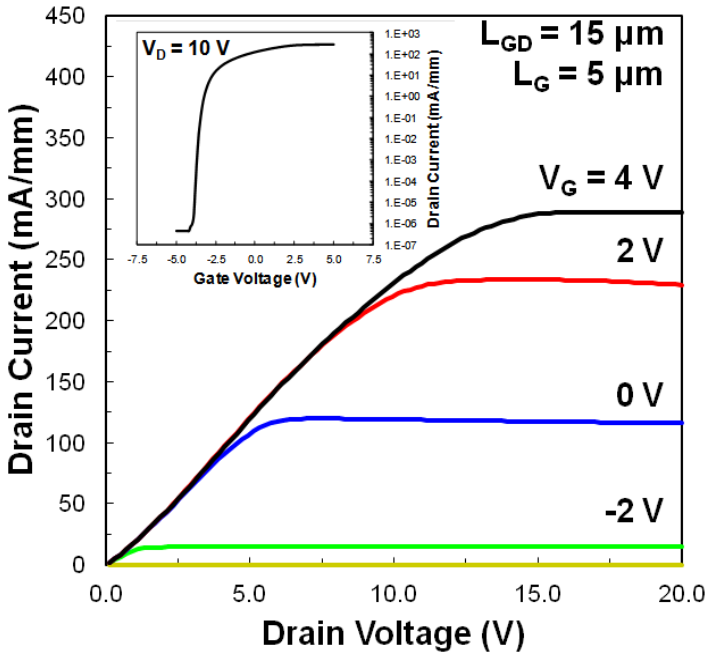

Figure 18: *IV* performance of baseline HEMT operating in depletion mode.

Capacitance – voltage analysis of gate stack capacitors processed simultaneously with the transistors described above revealed two accumulation-like regimes (Figure 19A). The sharp conductance peak near -3 V corresponds to the field-dependent modulation of the 2DEG at the AlGaN/GaN interface. A second conductance peak is visible near +3 V; we attribute this peak to the conduction loss associated with charge injection and subsequent trapping at the HfO_2/AlGaN interface. Numerical simulation of the vertical band diagram in the gate region of the MOSHEMT structure confirms that the onset of barrier accumulation occurs at or near 2 V gate-to-channel bias (Figure 19B).

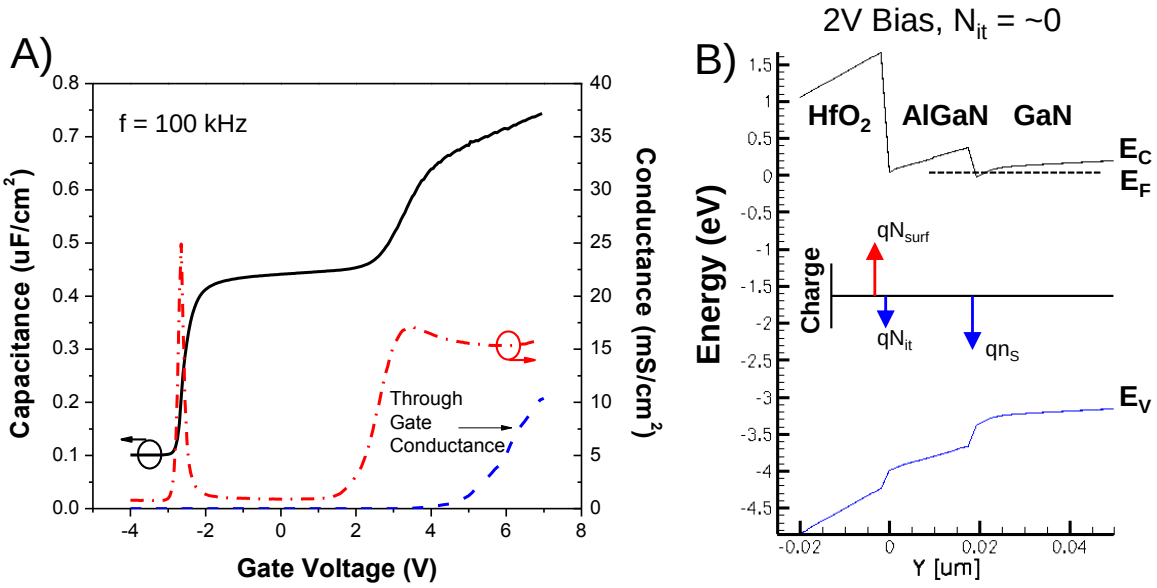

Figure 19: A) C-V and G-V of a circular capacitor (radius = 30 µm). B) Numerically solved band diagram of MOSHEMT gate structure at the onset of interface charge trapping. AlGaN surface charge of ~2.4x10^{13} cm^{-2} was added to match the experimental threshold condition.

The capacitance does not saturate after interface charging for two reasons. First, higher bias voltages align additional near-conduction-band interface states (presumed to be in the interfacial GaO_xN_y layer, discussed above) with the 2DEG, enabling accumulation of additional charge at the interface. Second, the onset of through-gate leakage current occurs at +5 V. It is important to note that this leakage does not permanently break down the dielectric. Channel control is maintained in subsequent measurements, and off-state gate leakage does not increase. Sweeping up to these voltages does induce significant charge trapping, the nature of which will be discussed in the following paragraphs. The oxide/AlGaN interface potentially provides a secondary conduction path between the drain and source. However, we do not see a secondary hump in the I_D-V_G (Figure 18 inset) as we do in the C-V, so we assume the oxide/AlGaN conduction path does not contribute significantly to drain current.

Sweeping the capacitor gate voltage above 2 V induces large hysteresis and threshold shift (Figure 20). Several important phenomena are observed in this data. First, initial forward/back hysteresis is observed at the 2DEG modulation region (ΔV_1) and at the deeper trap region (ΔV_2). Second, a subsequent forward sweep hysteresis relative to the initial forward sweep curve is observed (ΔV_3). The first two can be explained by a shift in capacitance due to charge trapping, but they have a difference in magnitude, leading to the conclusion that during the reverse sweep they have different levels of charge. This leads to the conclusion that fast discharging traps may be at play. The subsequent forward sweep hysteresis (ΔV_3) indicates charges are trapped for a longer time, but some are re-emitted with an intermediate time constant (i.e. ΔV_3 is less than

$\Delta V_{1)}$. Finally, any residual major shift (ΔV_3) that is sustained in the C-V shift and in V_T has a long time constant. Thus, three general trap types are observed. We refer to them as short τ, intermediate τ, and long τ traps; they are mathematically defined in Table 2. Using these definitions, the quantity of each trap type can be calculated at each bias voltage (Figure 21A) as well as the total number of traps filled by a sweep to that voltage (Figure 21B). Due to the unknown band structure of the interfacial GaO_xN_y and the changing band structure with charge trapping, extraction of the exact trap locations in the band gap is complicated and outside the scope of this work.

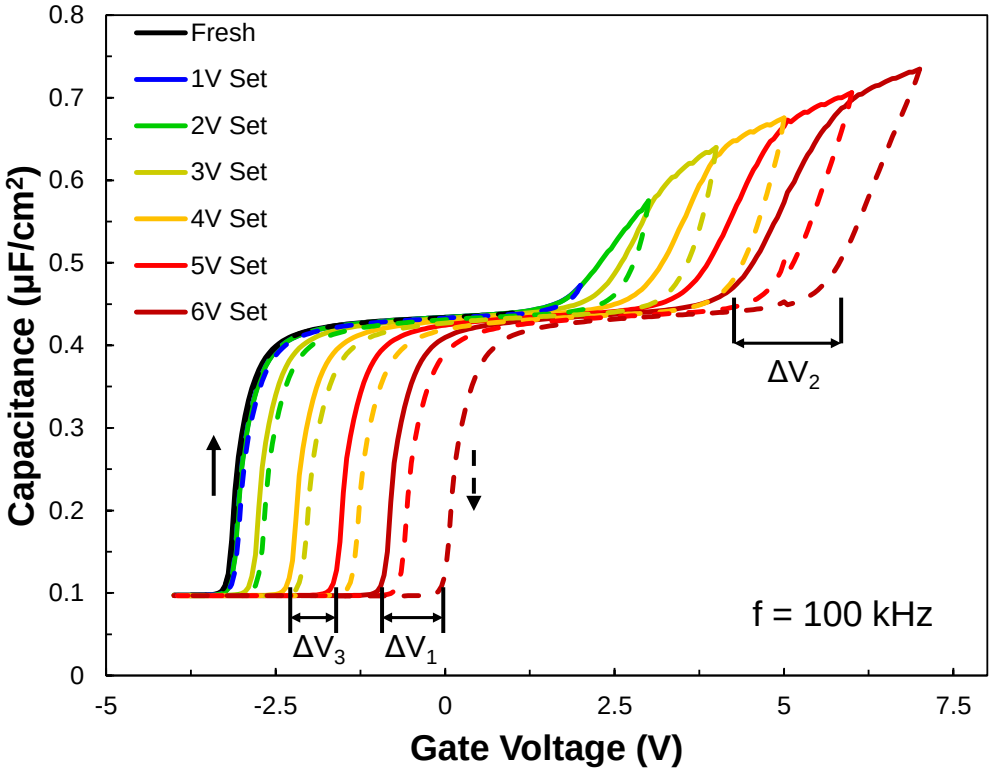

Figure 20: C-V measurements collected while sequentially increasing the maximum capacitor gate voltage. Both 2DEG and barrier accumulation threshold shift is observed. Hold time at maximum voltage is 90 ms.

After charge injection into the oxide/AlGaN interface, acceptor traps in the GaO_xN_y and HfO_2 capture electrons, neutralizing the interface charge and inducing positive threshold shift. Sweeping the voltage up to 6 V provides a ~3 V memory window (N_{it} = 8 x 10^{12} cm^{-2}). The traps are believed to be localized in or near the interface layer because the onset of gate leakage current does not shift as charge is trapped. At gate voltages above 2 V, the electric field across the gate dielectric is significant. Electrons trapped in the bulk HfO_2 would be emitted and swept away. Additionally, we believe the interlayer to be the primary source of long τ traps. Similar studies of Al_2O_3-gated GaN HEMTs have reported hysteresis due to trapping with shifts equivalent to ΔV_2 and ΔV_1 in Figure 20, but stable, lingering shift, ΔV_3, is not reported [45-47].

Table 2: Trap type definitions.

Short τ Traps	$N_T = \frac{C_{MIS}(\Delta V_2 - \Delta V_1)}{q}$	Traps that fill during charge injection to the oxide/AlGaN interface, but emit before 2DEG depletion (τ < 7s).
Intermediate τ Traps	$N_T = \frac{C_{MIS}(\Delta V_1 - \Delta V_3)}{q}$	Traps that emit between the end of one measurement and the beginning of the next (7 < τ < 30s).
Long τ Traps	$N_T = \frac{C_{MIS}(\Delta V_3)}{q}$	Traps that do not emit within the measurement window resulting in persisting V_T shift (τ > 30s).

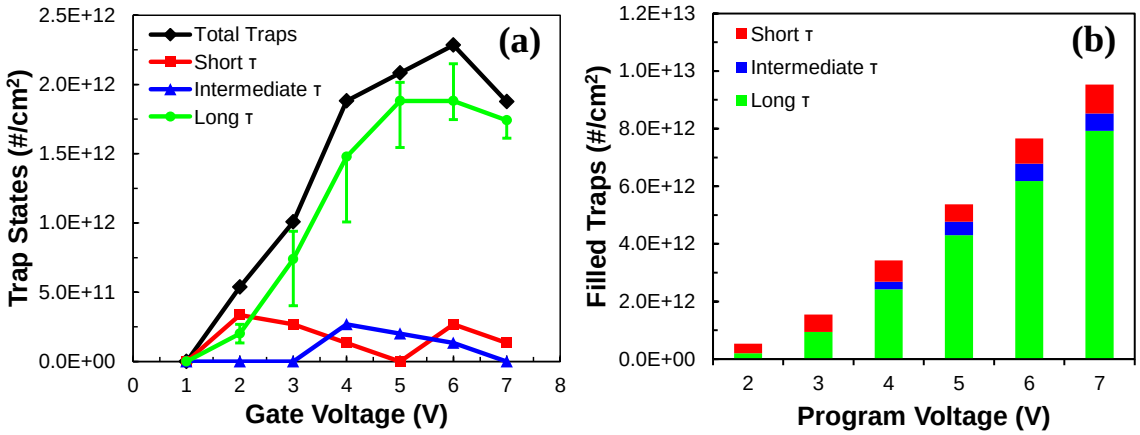

Figure 21: A) Approximate number of traps at each voltage level. Error bars are included for the long τ traps to give an indication of the reproducibility of the charging effect across the wafer. B) The total number of traps filled by a sweep to a given program voltage (integral of A).

Similar charge trapping behavior was observed in the MOSHEMTs, and intentional filling of the long time constant traps can be used to achieve enhancement mode operation. Figure 22 shows I_D-V_G and extracted threshold voltage before program, after 5 V program, and after 7 V program. Program consisted of holding the gate voltage at the program voltage for 1 s. Program at 7 V results in a threshold voltage of 0.45 V (as extracted using the $g_{m,max}$ method).

This shift comes with a surprisingly small cost. I_{DSAT} suffers a 10% decrease (212 mA/mm at V_G-V_T = 4.5 V, V_{DS} = 10 V), the sub-threshold slope increases by 15% (77 mV/dec), and R_{ON} increases by 13% (46.8 Ohm·mm). The increase in R_{ON} and SS is due to voltage stress degradation of the gate stack. Additional experimentation is required to determine the long term effects of the trapping on gate stack integrity. Transconductance of 55 mS/mm is maintained as well as I_{on} / I_{off} ratio greater than 10^8

(when measured at V_{GS} = +/- 5 V). Additionally, interface trapping did not noticeably increase the off-state drain current implying that the trapped charges are not laterally mobile at these drain biases (< 100 V). Gate recessing schemes commonly see drain current reductions of 75-85% (see trend line in Figure 24) due to the removal of the 2DEG. Since the interface charge acts effectively as a floating gate, the saturation current reduction is not nearly as severe.

A more significant cost arises from emission of the trapped charge. Figure 23 shows the charge retention time after a 7 V program. In order to maintain enhancement-mode performance, the interface charge would need to be refreshed every ~1000 seconds. This is especially problematic for power electronic applications; however the retention time is similar to previous reports of enhancement mode operation via a secondary floating gate [48], and this technology has the benefits of a lower program voltage and reduced processing cost. Use of a metal floating gate requires four additional steps: metal deposition, lithography, metal etch, and inter-gate isolation dielectric deposition.

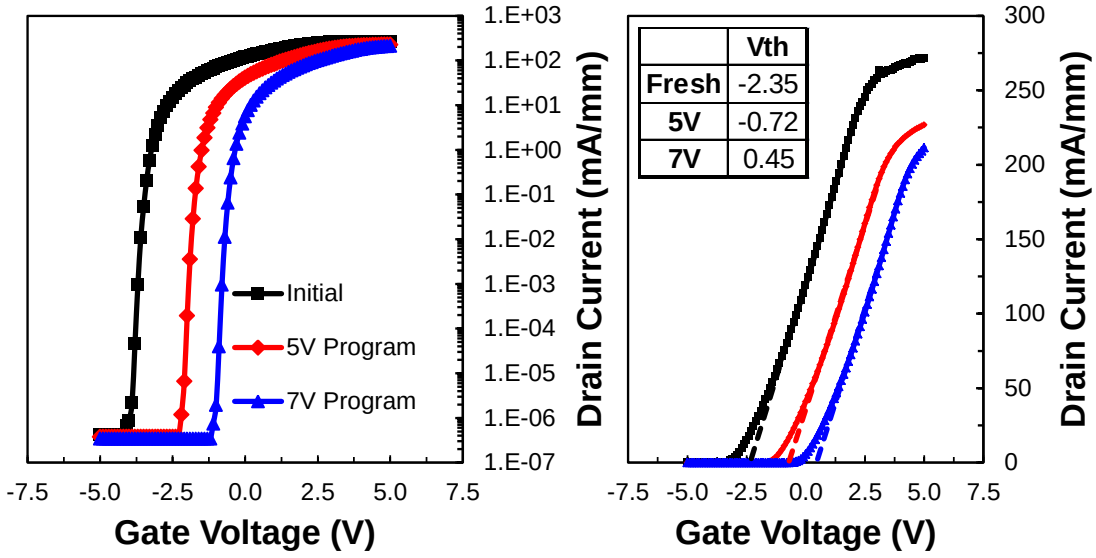

Figure 22: Both log scale and linear I_D-V_G plots after 0 V, 5 V, and 7 V programs showing threshold shift due to programming.

The performance achieved by the baseline technology (both depletion and enhancement mode operation) is compared to that of other reported CMOS-compatible technologies in Figure 24. The reduction of drain current accompanying a gate recessing scheme is highlighted by the dashed line connecting the two IMEC technologies.

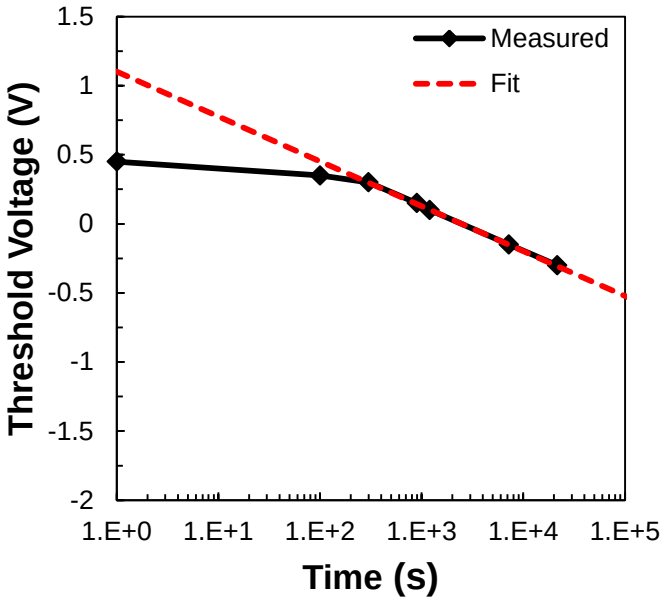

Figure 23: Threshold shift retention time measured after 7V program. Device was stored in the dark.

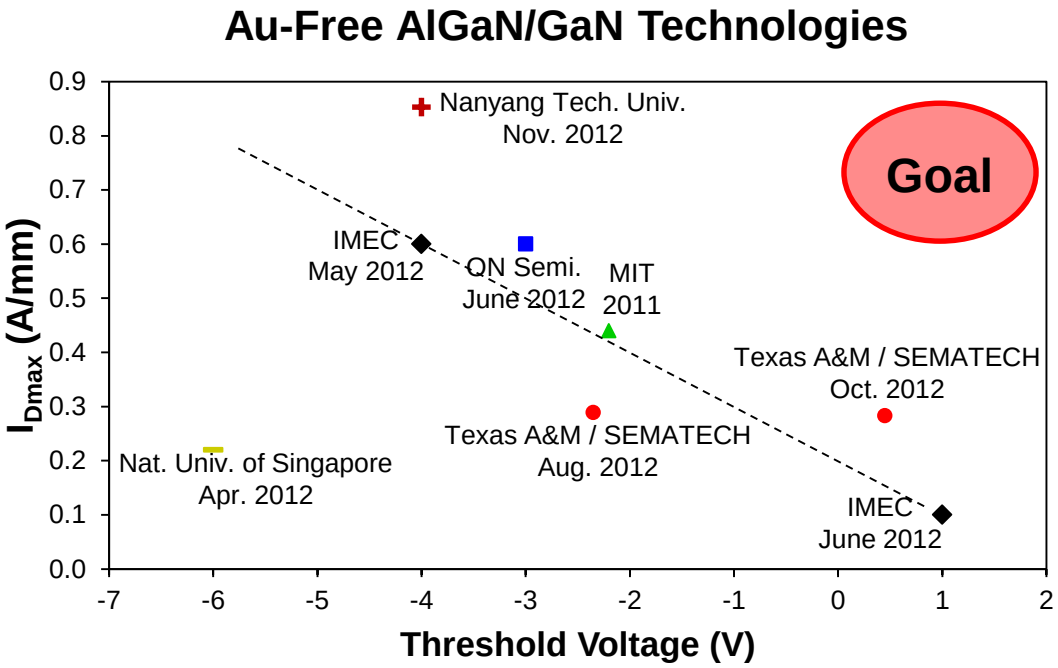

Figure 24: Comparison of reported Au-free technologies [8-10, 12, 13, 44, 49].

3.2 Integration Challenges of CMOS-compatible GaN Technology

Several key lessons were learned through the integration of the baseline technology. Some of them were briefly mentioned above, but they will be highlighted and summarized here. Figure 25 shows a waterfall chart recapping the baseline process.

The largest processing delay arose from the ion implantation process. The onsite implantation capabilities were insufficient to realize the high energy nitrogen implantation. As a result, the wafers had to be packaged and shipped to an external implantation vendor. Purchase of a dedicated implanter or implementation of a shallow trench isolation scheme would decrease the total wafer processing time.

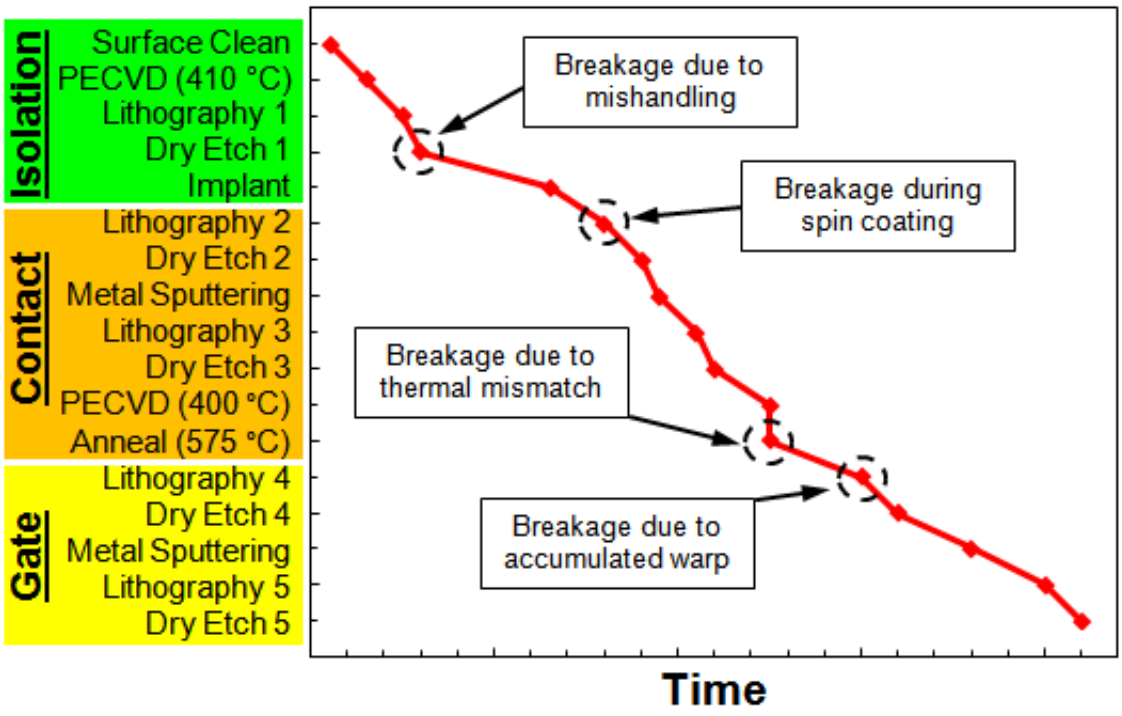

Figure 25: Waterfall chart showing processing time per step with wafer breakage risks highlighted.

Due to the lattice mismatch between GaN and Si, GaN-on-Si wafers are inherently strained making wafer breakage a major risk. While we observed breakage due to robot mishandling and accumulated wafer warp, the ohmic alloy anneal presented the biggest risk. Due to mismatch in the thermal expansion coefficients of GaN and Si, any temperature non-uniformities in the annealing furnace lead to breakage. Cylindrical rapid thermal processing systems are required, inhibiting flash anneals. To minimize wafer warp, thick substrates may be used [14], and wafer warp should be monitored throughout the process ($< \pm 70$ μm).

The ohmic anneal was also found to present the primary tool contamination hazard. At the beginning of process development, Au (commonly used in GaN contact metallizations) and Ga (a p-type dopant in Si) tool contamination risks were identified. Gold contamination was avoided by choosing Au-free metallizations, and Ga contamination was monitored by running TXRF analysis after processing of GaN epi-wafers. Analysis consisted of running a standard process for the respective tool on two Si wafers: one face-up and one face-down. TXRF was then performed on the Si wafers to check for trace concentrations of Ga and other contaminants. Concentrations below $5x10^{10}$ at/cm^2 were deemed a pass. Figure 26 summarizes the results of the TXRF analyses. Previous reports indicated that AlGaN etch steps led to tool contamination [8]; however, this work found Cl_2–based RIE plasmas to simultaneously clean Ga etch byproduct from the chamber walls. The only failure occurred during the ohmic anneal. After failure, the tool was recovered via solvent wipe down. Subsequent contamination was mitigated by employing a PECVD encapsulation layer prior to annealing.

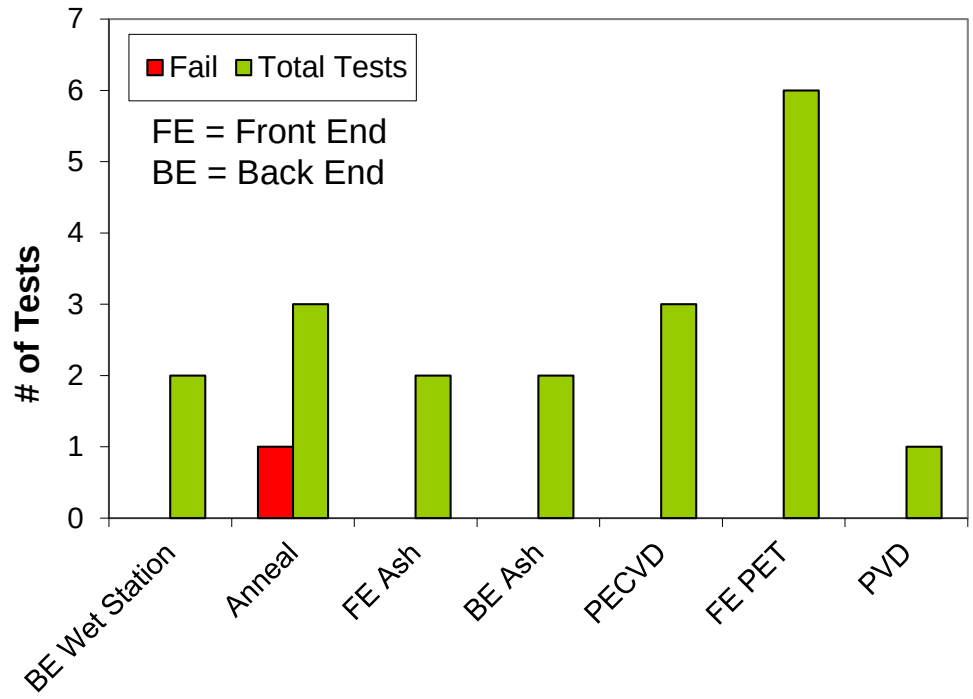

Figure 26: Bar chart presenting pass/fail TXRF results. Ga or Ta concentrations above $5x10^{10}$ at/cm^2 constituted a failure.

Another challenge encountered was CVD film compositional variations due to differences in nucleation surface composition, thermal conductivity, and plasma sheath. As discussed in Section 3.1.2, PECVD Si_xN_y behaved very differently when deposited on AlGaN/GaN compared to Si. The as-deposited density increased leading to unexpected Al diffusion. Additionally, the composition variation affected the etch rates of plasma etches that were initially developed on Si. As a result, all standard CVD processes must be requalified on GaN substrates.

Finally, dry etching of the ohmic contact metallization presents a challenge. Metallizations almost universally include a thick Al film with a high melting point metal

cap (Ta, W, TiN, TaN, etc.). Due to the difference in mechanical and chemical properties of the cap and interlayer, large undercut occurs. The effect can be addressed through careful optimization of the plasma chemistry.

4. SELF-ALIGNED OHMIC CONTACTS TO ALGAN/GAN HETEROSTRUCTURES

4.1 Overview of Si CMOS Salicide Process

Figure 27 shows an overview of a self-aligned silicide (salicide) contact process. The first step of the contact process is the deposition of the metal. Molybdenum, titanium, cobalt, and nickel have all been used in silicon's long history [50-53]. The wafers are then annealed and any metal in contact with silicon reacts to form a silicide (Figure 27C). After anneal, a wet etch is used to selectively remove the unreacted metal (Figure 27D). Thus, when combined with a dielectric spacer, the contacts are aligned to the gate without a lithography step. The contact process often concludes with a second anneal to set the desired phase (Figure 27E). For example, in a nickel silicide process, the dominant phase after the initial anneal is Ni_2Si. A second anneal is required to convert to the low resistance NiSi phase [54].

For adaption of the contact scheme to AlGaN/GaN heterostructures, three enabling process steps are required: a Si_3N_4, a metal that leaches nitrogen from the AlGaN to form a metal nitride and leaves behind *n*+ AlGaN, and a wet etch selective to the unreacted metal. The development of these processes will be discussed in detail in the following sections. Prior work from literature has focused primarily on selective area MBE for self-aligned processes which is not cost-effective [1, 6, 7]. This contact scheme will realize the cost-savings of a self-aligned module without the cost and throughput

limitations of MBE. This is a significant divergence from standard GaN HEMT technology.

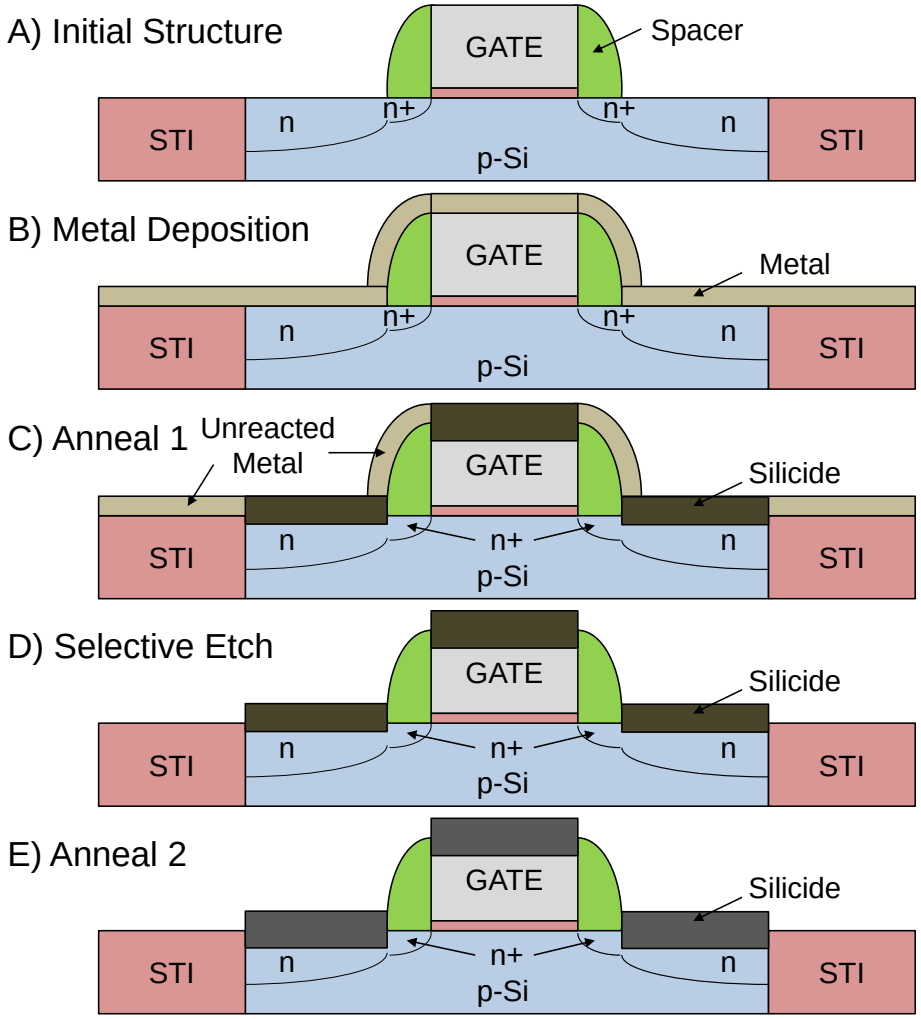

Figure 27: Overview of Si CMOS self-aligned contact process.

4.2 Sample Fabrication

All of the samples discussed in this section were prepared in the following manner. The starting wafer consisted of a 2/17.5/800 nm GaN/$Al_{0.25}Ga_{0.75}N$/GaN

heterostructure grown via MOCVD on Si (111). Including the strain relaxation layers, the total epitaxy thickness was ~2 µm. Hall measurements yielded an average sheet resistance of 415 Ω/sq. Processing began with a solvent clean and 10 minute native oxide strip in 1:10 HCl:DI-H_2O. Immediately after cleaning, samples were loaded into an Oxford Plasmalab 80 for PECVD deposition of 100 nm of Si_xN_y at 350 °C. 150 cycles of HfO_2 was then deposited by ALD to act as a protective etch stop layer (discussed in Section 4.5). Circular TLM structures were then patterned and windows were opened in the field dielectric stack. A wet and/or plasma surface clean (discussed in Section 4.7) was performed immediately prior to metal deposition. After metal deposition, the majority of samples were encapsulated with 50 nm of PECVD Si_xN_y and annealed at 865 °C in N_2 ambient for 1 minute. Encapsulation and unreacted metal were removed by etching in 1:50 HF:DI-H_2O. A second anneal was then employed with both temperature and time varied (discussed in Section 4.6). Finally, aluminum interconnects were deposited by a liftoff process and I-V measurements were collected. Figure 28 shows a cartoon of the completed test structure.

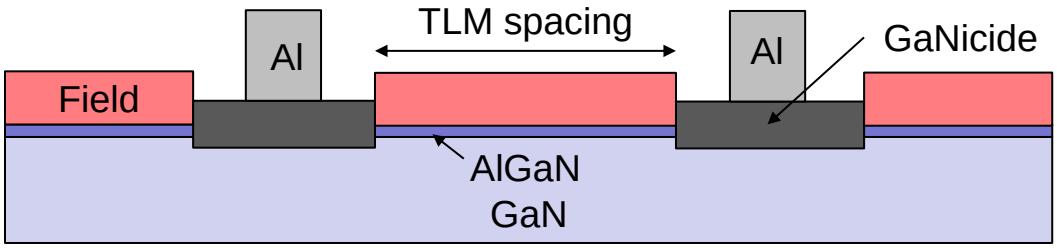

Figure 28: Cross-section cartoon of TLM test structure. Only one side of the circular structure is shown.

4.3 Metal Selection

Several metals have stable metal nitrides with enthalpy of formation lower than GaN: Al, Ta, Ti, Zr; however, Ta and Ti are most commonly used in literature due to the nearness of their work functions to the electron affinity of GaN (Table 3) [10, 55]. Ta was initially explored for use in the self-aligned contact process because low contact resistance can be realized using low temperature anneals. Unfortunately, the wet etch selectivity between Ta and TaN is poor [56]. The focus of development then shifted to Ti-based contacts because the selectivity of Ti over TiN is high in hydrofluoric acid based etchants (Figure 33). Ti-based ohmic contacts have been studied extensively in literature, so the details of the physics behind ohmic contact formation will not be repeated here [36-38, 57-60]. As a baseline, 100 nm of Ti was deposited using DC magnetron sputtering.

Table 3: Enthalpy of formation and work function for pertinent metal nitrides [61].

Material	Enthalpy of Formation (kcal/mole)	Φ_M / X_S (eV)
GaN	-25.0	4.05
VN	-51.9	5.1
TaN	-60.0	4.75
AlN	-76.5	0.6
TiN	-80.4	3.74
ZrN	-87.3	4.65

SIMS depth profiling in a contact window after metal deposition and PECVD encapsulation is shown in Figure 29. Very little nitrogen content (blue line) is observed

in the as-deposited titanium. The titanium signal continues into the AlGaN layer due to knock-on effects. The sample was then annealed, the encapsulation and unreacted titanium were removed using dilute HF, and the sample was again capped with Si_xN_y. SIMS depth profiling was performed once again, the results of which are shown in Figure 30. The metal thickness was reduced by ~40%. The nitrogen content in the titanium layer has increased to a level similar to that of the GaN layer, and titanium has diffused through the AlGaN layer to the AlGaN/GaN interface. This is expected to enable good ohmic contact to the 2DEG. Electrical measurement showed ohmic behavior with excellent uniformity across the sample (Figure 31A) confirming the viability of the self-aligned contact scheme for GaN-based devices. The remainder of this section describes numerous experiments aimed at further lowering the contact resistance while maintaining self-aligned behavior.

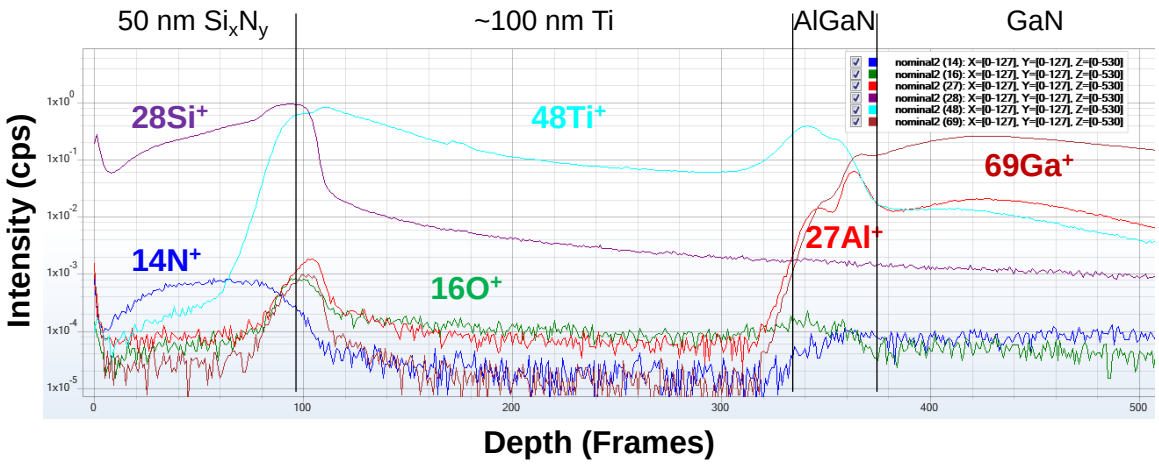

Figure 29: SIMS depth profile of as-deposited titanium, after PECVD Si_xN_y encapsulation, but before ohmic anneal.

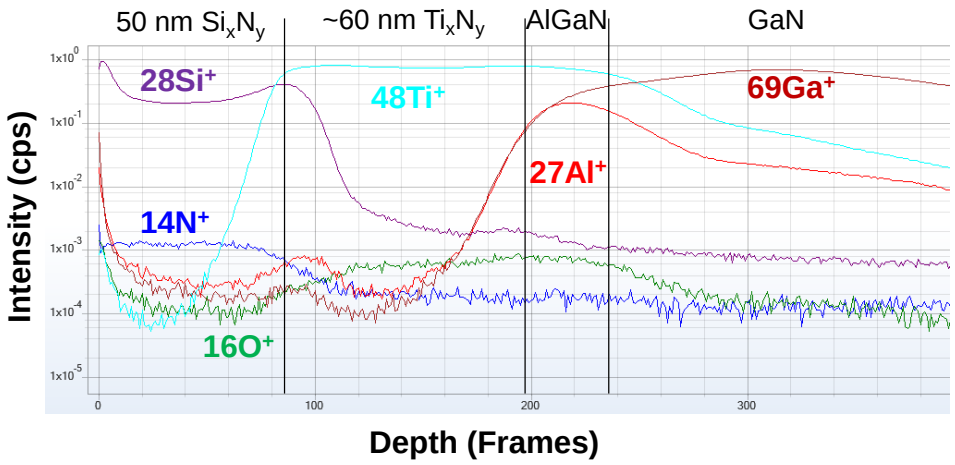

Figure 30: SIMS depth profile in contact window after anneal, selective etching, and capping with PECVD Si_xN_y.

We next explored the impact of an Al interlayer on the contact resistance. Most of the Ti-based alloyed contacts in literature include a thick Al layer which is believed to help decrease the contact resistance [37]. A typical bilayer (30 nm Ti / 180 nm Al) was deposited by sputtering and annealed. Widespread agglomeration was observed after anneal and was sufficiently severe to compromise the TLM structures so that the subsequent wet etch stripped everything off the wafer. To avoid this problem, thin Al interlayers were inserted into the titanium film. We ran experiments examining the impact of the thickness of the Al interlayer and the effect of its distance from the Ti / AlGaN interface. The results of the experiment are shown in Figure 31. Increasing the Al thickness increased the contact resistance. In all three cases, the addition of the thin Al layer increases the contact resistance and decreases the uniformity across the sample. As a result, the Al layer was not included in experiments described in later sections.

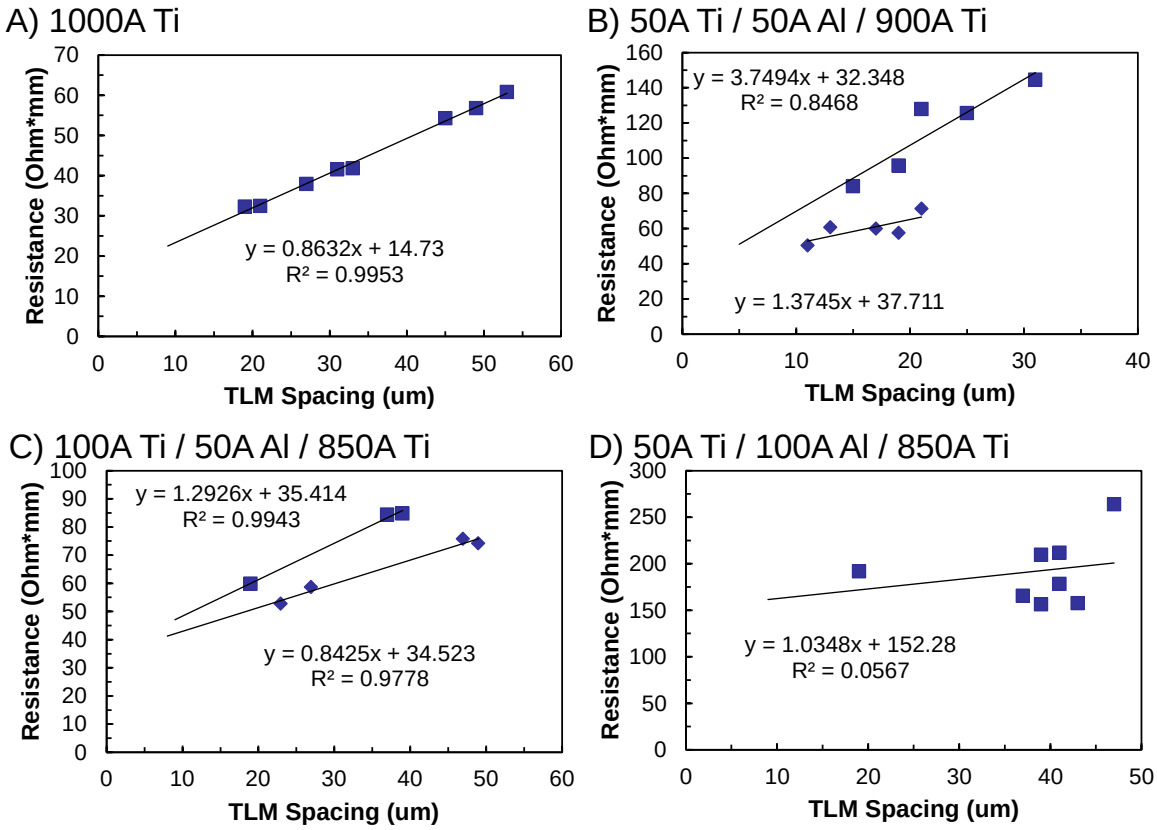

Figure 31: Resistance versus TLM spacing plots from an experiment examining the impact of a thin Al interlayer placed near the Ti / AlGaN interface.

The impact of deposition temperature was also explored. The sputtering conditions (bias power, Ar pressure, temperature) dictate the crystallographic orientation of the resulting Ti film [62]. Additionally, increasing the temperature may increase the interaction of the metal with the exposed AlGaN. Sputter depositions were carried out in a Kurt Lesker PVD 75 at room temperature, 100 °C, and 350 °C. The wafers were heated via tungsten filament lamps located behind the sample mounting plate. The temperature was slowly raised to the target temperature, then held for stabilization for 30

minutes prior to commencing the deposition. The resulting contact resistance and uniformity are shown in Figure 32. Uniformity decreases as the deposition temperature increases, without a significant improvement to the contact resistance. In light of this, the remainder of the metal depositions are performed at room temperature.

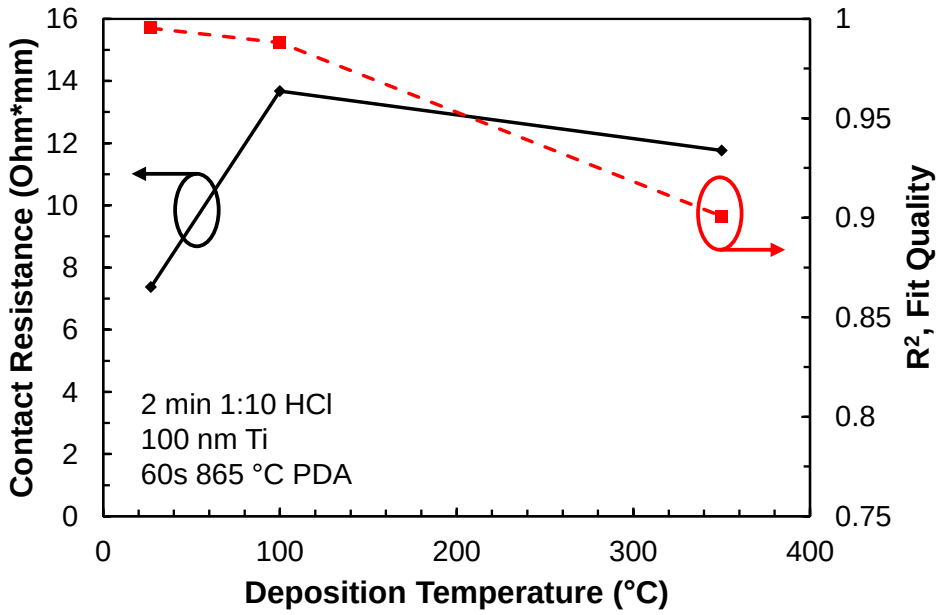

Figure 32: Extracted contact resistance and fit quality for Ti sputtered at various temperatures.

4.4 Selective Etch Development

Etch rate experiments were performed on blanket metal / Si samples to identify a controllable etch with high Ti over TiN selectivity. Both BOE and HF(49%) chemicals were explored at a variety of dilutions (Figure 33). TiN etched slower in HF leading to higher selectivities. In order to make sure that the etch transpired slowly enough to maintain adequate control, 1:50 HF:DI-H_2O was chosen for use as the selective etch.

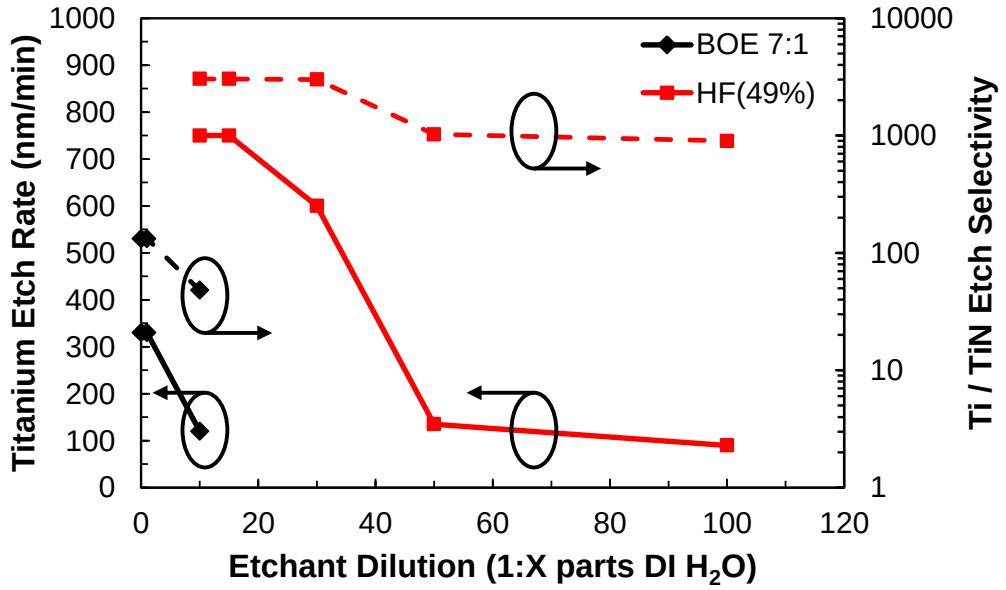

Figure 33: Etch rate and Ti/TiN selectivity as a function of dilution of BOE and HF-based etchants.

4.5 Field Stack Development

After selection of the wet etch chemistry, a protective field dielectric must also be engineered such that previously processed devices are not destroyed in the dilute HF. The Ti/field selectivity should be comparable or even better than the Ti/TiN selectivity. ALD HfO_2 was selected as the starting point for field dielectric engineering. From etch rate reports in literature, the etch rate of unannealed HfO_2 should be an order of magnitude lower than the TiN etch rate in 1:50 HF:DI-H_2O [56], and the etch rate is expected to be further decreased by densification due to the 865 °C ohmic anneal.

After a few experimental iterations, we began to suspect that the HfO_2 and Ti layers were interacting during the ohmic anneal. This resulted in conductive residues in the field region, as well as unexpectedly slow Ti removal, especially in small windows

(Figure 34A). To combat this issue, a 100 nm PECVD SiO_2 "delamination layer" was inserted between the HfO_2 and titanium. We reasoned that the SiO_2 would block interaction between HfO_2 and Ti, and its rapid etch rate in HF would help undercut hard-to-remove Ti residues. Clearing of Ti from small windows improved (Figure 34B), but some of the field residues persisted, and sample uniformity remained a challenge.

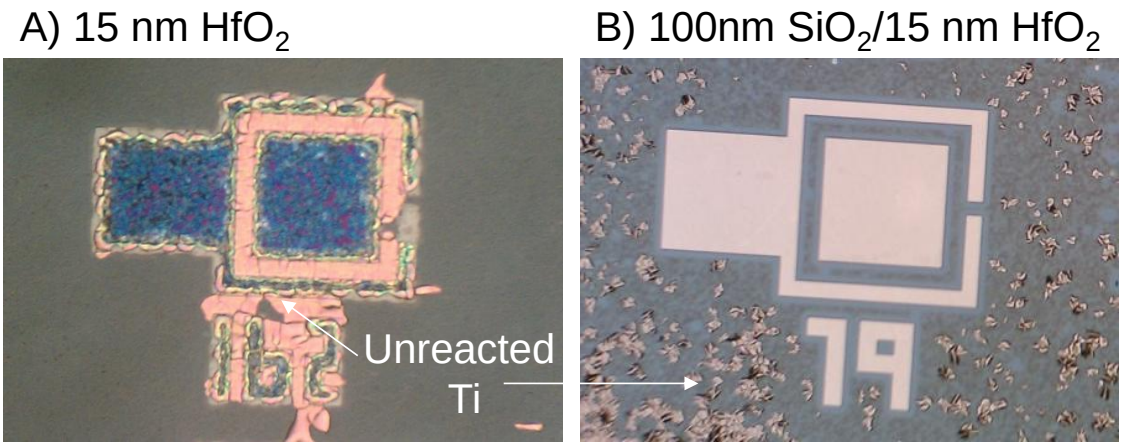

Figure 34: Top down micrographs taken after 10 minutes of etching in 1:50 HF:DI-H_2O of a sample without a SiO_2 delamination layer (A) and with a delamination layer (B).

In an effort to further improve uniformity and yield, a thin PECVD Si_xN_y diffusion barrier was added directly beneath the Ti film. This barrier inhibits oxygen diffusion from the SiO_2 into the titanium. Ti oxide is slow to etch in HF, especially after high temperature anneal [63]. Figure 36A shows an image of a sample processed using the $Si_xN_y/SiO_2/HfO_2$ field dielectric. The unreacted titanium cleared quickly and uniformly. The improved field dielectric also resulted in decreased contact resistance

(Figure 36B) by eliminating TiN over etching that previously occurred when trying to remove field residues.

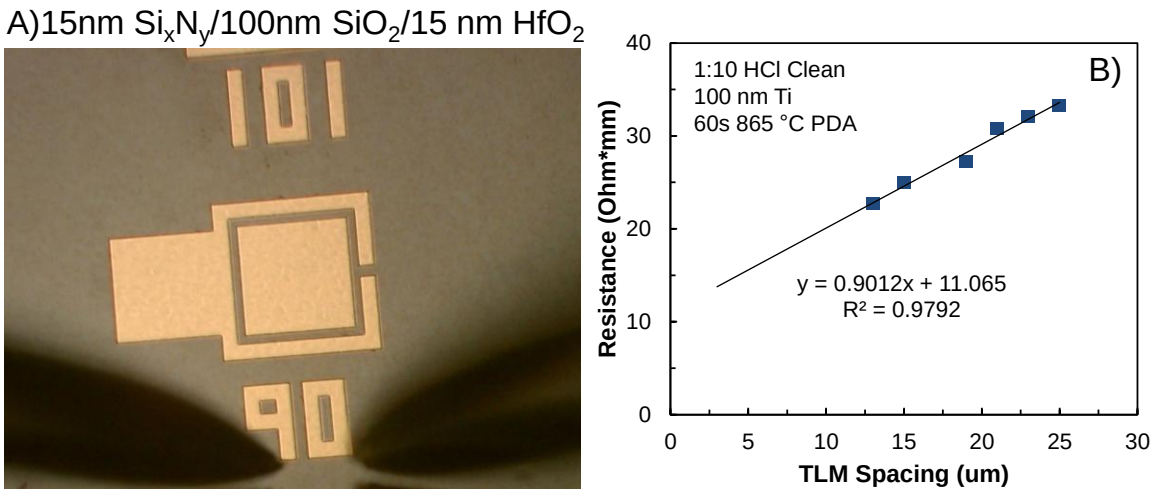

Figure 35: A) Optical microscope image taken after 8 minutes of etching in 1:50 HF:DI-H_2O. B) Resistance vs. TLM spacing plot showing decreased contact resistance relative to the baseline (Figure 31A).

The process of opening contact windows in the field dielectric progressed in three steps. First, the top silicon nitride and oxide were etched in BOE. Second, the HfO_2 film was etched in an Oxford Plasmalab 100 using a SF_6 / Ar plasma (described in detail in Section 3.1.3). Finally, the passivation nitride was etched using BOE. Figure 36 shows a cross-section SEM of the field stack captured after HfO_2 plasma etching.

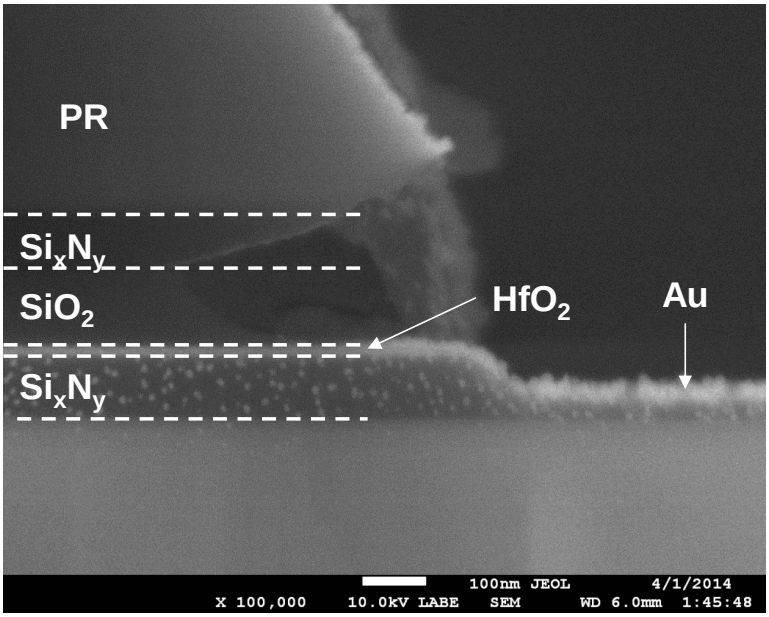

Figure 36: Cross-section SEM micrograph of the $Si_xN_y/SiO_2/HfO_2$ field dielectric stack captured after plasma etching the HfO_2.

4.6 Anneal Tuning

After development of the selective etch and improvement of the field dielectric, we began to optimize the thermal treatment. Two anneal steps were investigated: the ohmic alloy anneal (before selective etch), and the phase setting anneal (after selective etch). Figure 37 plots the contact resistance and fit quality versus anneal time for 100 nm of sputtered Ti annealed at 865 °C in ambient N_2. 865 °C has been previously demonstrated to be the optimum annealing temperature for Au-free, Ti-based ohmic contacts to AlGaN/GaN [10]. Increasing the anneal time decreases the contact resistance, but also decreases the uniformity across the sample. The longer anneal provides more time for Ti and Si_xN_y/SiO_2 to interact. Several samples were also generated using lower temperature anneals; however, nitrogen out-diffusion from the III-Nitride decreased as

the anneal temperature decreased resulting in degraded etch selectivity between the field and contact regions. Ohmic behavior was not observed.

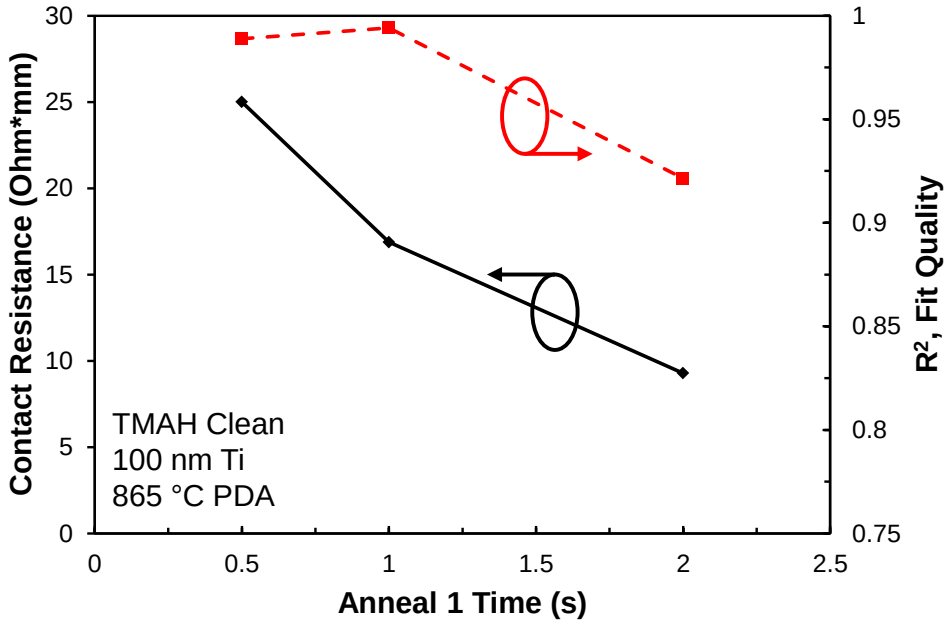

Figure 37: Contact resistance versus anneal time for the ohmic anneal.

The impact of a second anneal, after selective etching of unreacted Ti, was also investigated. Samples were annealed for 60 s at 865 °C, then etched in dilute HF. Following the etch, samples were annealed for an additional 60 s in ambient N_2 at temperatures varying from 350 °C to 750 °C. The resulting contact resistances are plotted in Figure 38. Anneal at any temperature degrades the contact resistance relative to the unannealed control sample. For this reason, only the initial ohmic anneal is incorporated into the final self-aligned contact process.

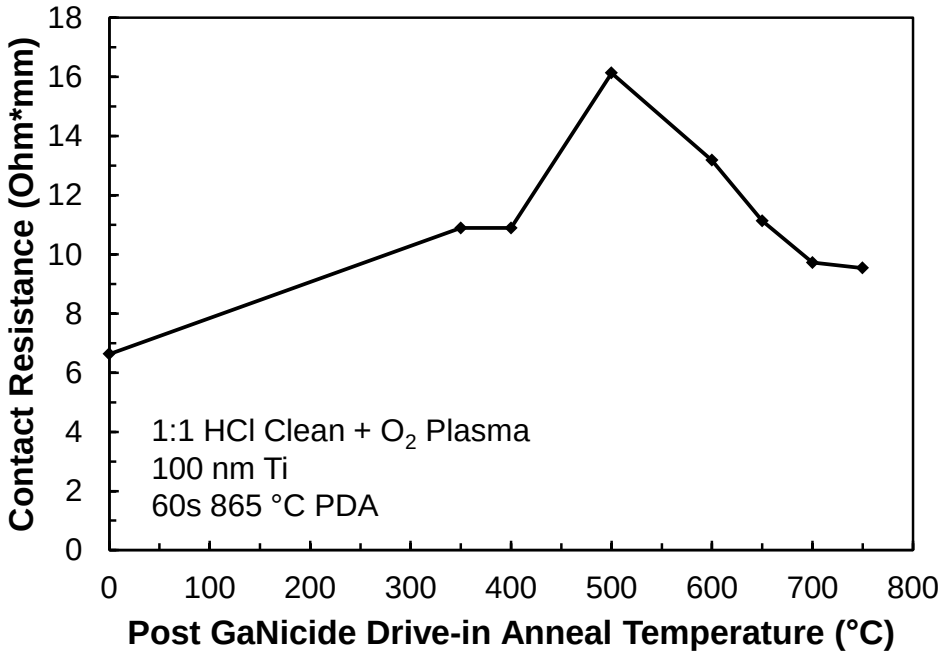

Figure 38: Contact resistance versus anneal temperature for the post-etch anneal. All anneals were performed in N_2 ambient and lasted for 60 s.

4.7 Pre-metallization Surface Treatment

Several factors must be considered when preparing AlGaN/GaN heterostructures for ohmic contact formation: native oxide removal, surface roughness, barrier recessing, and plasma doping. These factors are often interrelated further convoluting the optimization process. While an HCl surface clean will strip gallium oxides, it simultaneously increases surface roughness [64]. An oxygen plasma doping process will simultaneously increase native oxide thickness [65]. In the interest of experimental simplicity, we do not attempt to quantitatively monitor surface roughness, native oxide thickness, or substrate doping. Instead, we use the contact resistance to track the net impact of process variations.

Figure 39 summarizes the contact resistance as a function of barrier recess depth and surface clean acid dilution. Each of the surface cleans lasted for 2 minutes and was performed immediately prior to introduction of the sample to the sputtering chamber for titanium deposition. The "No HCl" sample was rinsed in a TMAH based photoresist stripper immediately prior to metal deposition. TMAH etches GaN anisotropically resulting in a smoothed surface [66-69]. Thus, the increasing etchant strength should also correlate to increasing surface roughness. We found 1:10 HCl:DI-H_2O to produce the lowest contact resistance. The fact that the contact resistance worsens after a stronger surface clean implies that the primary difference between the 1:10 and 1:1 cleaned samples is surface roughness. The decreasing resistance from no HCl to 1:10 (Figure 39, black dots) is likely due to native oxide removal.

The III-Nitride barrier was recessed using SF_6 / Ar plasma in an Oxford Plasmalab 100. The plasma conditions were 40 sccm SF_6, 10 sccm Ar, 200W bias, 400W ICP, 44 mtorr, and chuck temperature of 16 °C. This plasma etches $Al_{0.25}Ga_{0.75}N$ at a rate of 15 nm/min. Full barrier recessing produces the lowest contact resistance at the 1:1 HCl:DI-H_2O node (-18% relative to no recess); however, the SF_6 barrier recess plasma also aggressively etches Si_xN_y making it incompatible with a self-aligned spacer process. As a result, alternative surface treatments are pursued.

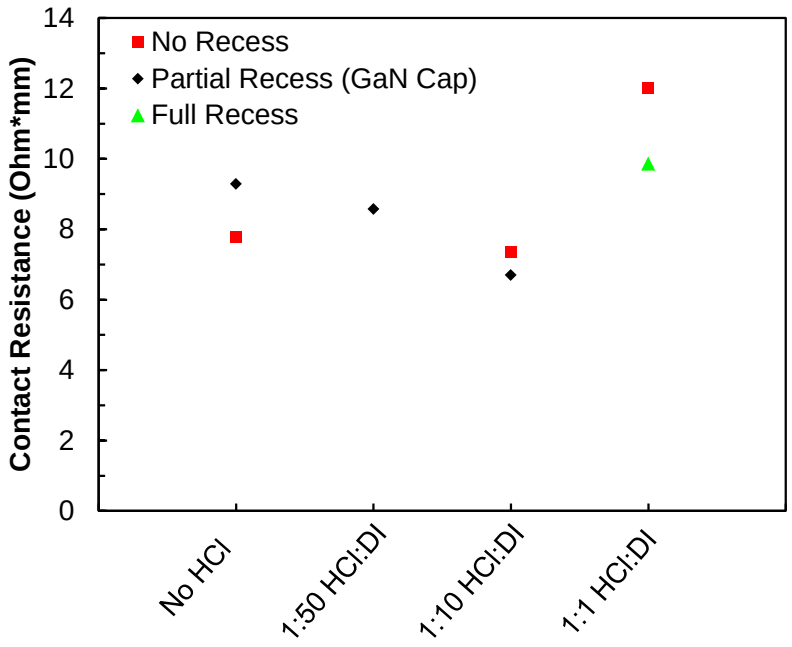

Figure 39: Contact resistance versus native oxide etchant dilution (impacts surface roughness) and barrier recess depth.

We next explored the impact of plasma treatments on the contact resistance. Oxygen acts as a *n*-type dopant in GaN, and oxygen plasma doping steps have recently been incorporated into non-alloyed ohmic contact schemes [65]. Samples were cleaned in 1:1 HCl:DI-H_2O to roughen the surface and maximize the exposed AlGaN surface area prior to introduction to an Oxford Plasmalab 80 plasma processing tool. Oxygen plasma treatment was carried out at 350 °C, with 25 sccm O_2 flowing and the pressure regulated at 80 mtorr. Plasma bias power was varied, and samples were generated with and without a post-plasma 1:10 HCl:DI-H_2O clean. A sample without plasma treatment was also processed as a control. Finally, a low power Ar plasma treatment was also performed in an effort to isolate the impact of surface doping from plasma cleaning. The

results are summarized in Figure 40. All of the samples resulted in good uniformity across the wafer. The post-plasma wet clean was found to be of little benefit. Increasing the oxygen plasma power negatively affected contact resistance. The Ar plasma treatment was found to enable the lowest contact resistance, and also improved the selectivity of the dilute HF etch. The Ar ion bombardment is believed to roughen up the field dielectric surface forming a crust that was more resistant to HF etching.

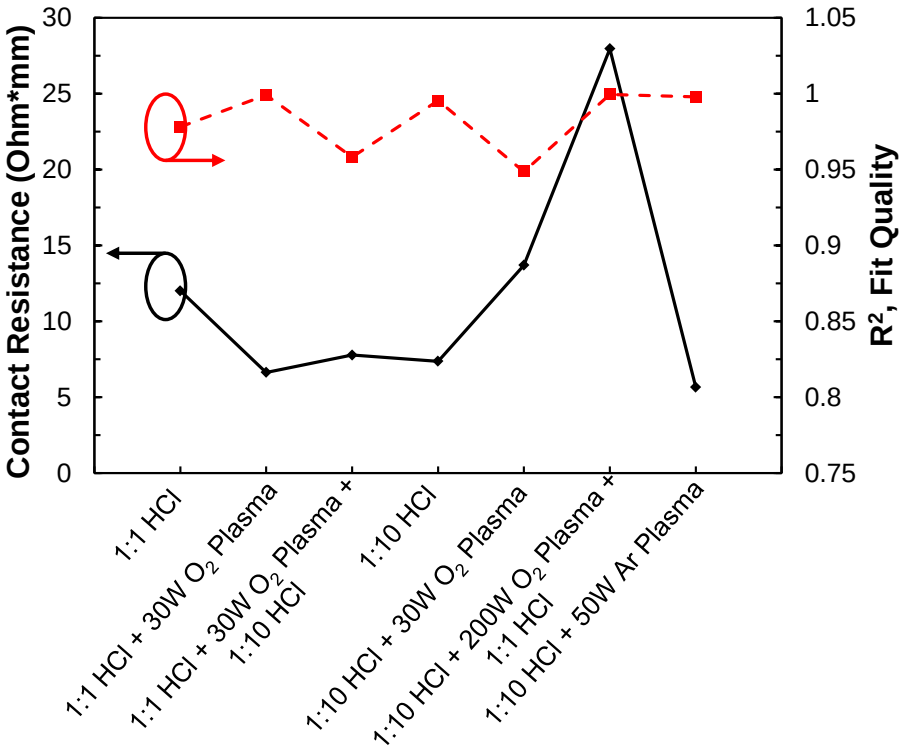

Figure 40: Contact resistance and fit quality versus plasma pre-treatment conditions.

4.8 Si_xN_y Spacer Development

In order to take advantage of the selective area contact formation and realize self-aligned contacts, a dielectric spacer process is required. Without a spacer, the contacts would short to the gate. For initial process development, 150 nm of evaporated Cr was lifted off on a silicon substrate. Then, 300 nm of Si_xN_y was deposited by PECVD. The conformal nature of the deposition results in smoothing at feature edges. Then, CHF_3 / O_2 (50 / 5 sccm) RIE at 150W bias and 50 mtorr is used to anisotropically etch the dielectric (etch rate = ~45 nm/min) leaving behind a triangular spacer adjacent to the gate metal. Cross-section SEMs before and after RIE are shown in Figure 41. The up-turned metal sidewall (an artifact of liftoff) causes a shift in the sidewall of the subsequent Si_xN_y (Figure 41A). The result is low yield of the spacer process. Most were fully removed. Only a few locations, as in (Figure 41B) had actual spacers remaining.

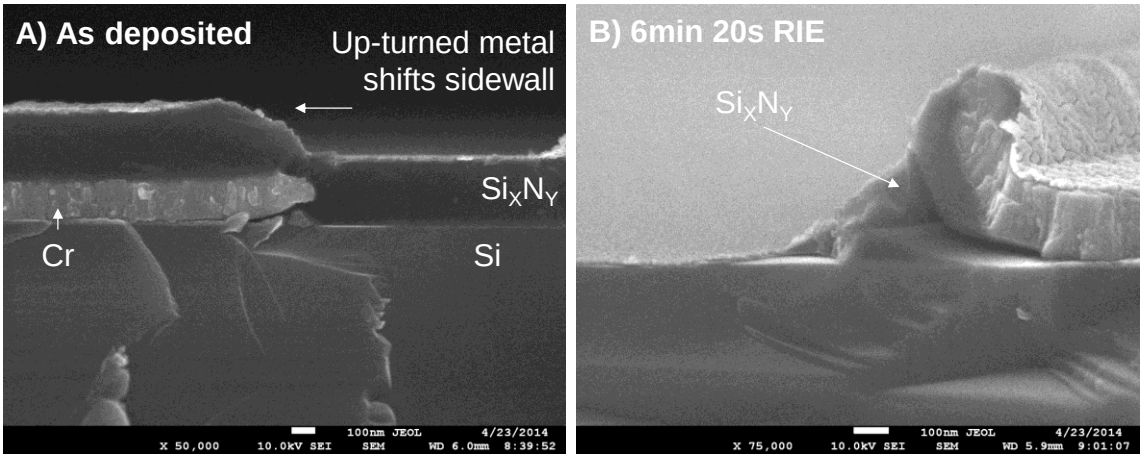

Figure 41: Cross-section SEMs of Si_xN_y spacer used in conjunction with gate metal liftoff. A) Immediately after PECVD deposition. B) After RIE of the Si_xN_y.

In order to remove the sidewall variability, additional samples were generated in which Cr was evaporated and patterned using commercially available Cr etchant (UEI CR-1A). The verticality and uniformity of the metal sidewall greatly improved (Figure 42A) leading to a drastic increase in spacer process yield. Cross section SEMs are shown before and after RIE in Figure 42. The etch was intentionally stopped ~5 seconds early to avoid damaging the substrate below. The RIE was followed by a 15 s rinse in BOE to clear remaining Si_xN_y residue. The process results in gate-to-drain and gate-to-source spacings of ~250 nm.

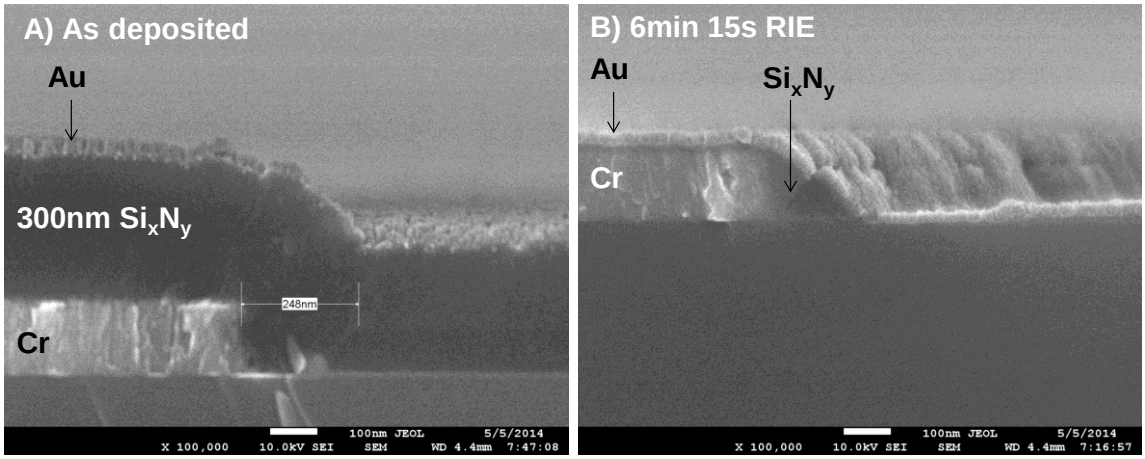

Figure 42: Cross-section SEMs of Si_xN_y spacer used in conjunction with positive gate pattern and etch. A) Immediately after PECVD deposition. B) After RIE of the Si_xN_y.

5. GATE STACK ENGINEERING FOR GATE-FIRST GAN-BASED HEMTS[*]

The gate stack engineering goals consist of enhancement mode operation, low-leakage performance (despite enduring the ohmic contact anneal), thermal stability, and low dielectric / III-Nitride interface trap density. The dielectric / III-nitride interface of interest will vary depending on the method for realizing enhancement mode operation. This section will describe our gate stack characterization methodology, analyze AlGaN/GaN Schottky diodes to provide baseline trapping information, and analyze several different dielectrics on AlGaN/GaN.

5.1 Techniques for Realizing Enhancement Mode Devices

Since the fundamental physics of AlGaN/GaN heterostructure devices lend themselves to depletion mode operation, methods for realizing enhancement mode operation have been intensively researched. Two general schemes have emerged, gate recessing and floating gate, along with several implementation variants. Each has unique advantages and disadvantages. The selection of enhancement mode scheme will dictate the primary dielectric/III-Nitride interface for optimization.

Gate recessing, as the name implies, involves removal of the AlGaN barrier in the gate region to remove the 2DEG. A channel is formed via the field effect to connect the source to drain. Because there is no longer a high density 2DEG for conduction, the

[*] Part of this section is reproduced from "Characterization of ALD Beryllium Oxide as a Potential High-κ Gate Dielectric for Low-Leakage AlGaN/GaN MOSHEMTs" by D.W. Johnson, J.W. Yum, T.W. Hudnall, R.M. Mushinski, C.H. Bielawski, W.E. Wang, S.K. Banerjee, H.R. Harris, 2014. *Journal of Electronic Materials*, 43, 151-154, Copyright 2014 by Springer Science + Business Media.

saturation current is drastically reduced relative to comparable depletion mode technologies [8]. Additionally, development of an etch selective to AlGaN over GaN has proven difficult. Variation in recess depth across a wafer will lead to large variation in threshold voltage. If using this scheme, dielectric/GaN interfaces are of primary importance. Improved etch control (and threshold voltage uniformity) has been achieved through insertion of a thin InGaN layer at the AlGaN/GaN interface to act as an etch stop layer [70]. The interlayer has the added benefit of increasing 2DEG carrier confinement [71]. This addition would change the interface of interest to dielectric/InGaN.

Enhancement mode operation through floating gate behavior can be realized in several different forms. First, a traditional floating metal can be fabricated and programed [72]. Second, as described in Section 3.1.4, dielectric/AlGaN interface traps can be intentionally charged. Both of these incarnations require programming and refresh due to charge dissipation. A third form involves implanting charged ions (through fluorine plasma treatment, for example) in the gate region [5, 73, 74]. No programming is required, but threshold stability remains a problem. The charges drift and diffuse with time and voltage stress. The threshold voltage slowly relaxes toward depletion mode. Finally, charge can be placed by using an InGaN capping layer above the AlGaN [75, 76]. The layer contributes piezoelectric charge at the InGaN/AlGaN interface that depletes away the 2DEG. Since the charge is due to material physics, stability is not an issue; however, the layer adds epitaxial and processing complexity.

Depending on which method is chosen, the dielectric/AlGaN or dielectric/InGaN interface must be optimized with respect to leakage and interface trapping.

For initial demonstration of gate-first, self-aligned HEMT technology, depletion-mode devices were used. Thus, the dielectric/AlGaN interface is the primary focus of this section. The results should translate well to a fluorine ion implantation scheme. Additionally, we have found that the behavior of dielectric/GaN and dielectric/AlGaN (low Al percent) interfaces are similar, so the results are also expected to apply for a gate-recessing scheme. The inclusion of In significantly changes the behavior of the dielectric/III-Nitride interface due to the relatively low thermal stability of In-N bonds [77]. Additionally, the impact of the InGaN layer on the ohmic contact module is not well understood. Therefore, dielectric/InGaN interfaces require separate optimization.

5.2 Gate Stack Characterization Methodology

Three different characterization methods are employed in this section, each providing unique information about the gate stack. XPS is useful for qualitative discussion of interface quality as it enables the detection of carbon contamination and sub-oxide formation and can also be used to determine the thermal stability of various binding states. *IV* measurements are used to compare gate leakage performance of various gate stacks. Finally, *CV* and *GV* measurements allow for determination of the bulk and interface trap density and trap position; however, the extraction of meaningful information from the CV and GV data is challenging, especially when dealing with semiconductor heterostructures.

One possible method for analysis of the trapping behavior of an AlGaN/GaN heterostructure is the conductance method [78]. Treatment of the AlGaN barrier as a dielectric like in a standard metal-oxide-semiconductor (MOS) structure was first proposed by Miller *et al.* [79]. However, since this initial proposal, the application of the conductance method to AlGaN/GaN MOS structures has not followed a clear and consistent procedure resulting in ambiguity in the interpretation of the results. Some groups apply the conductance method without mention of correcting the collected data for series resistance and barrier capacitance [80]. Others mention accounting for one parasitic but not the other [81]. Even when the data is prepared correctly, conversion of characteristic trap frequencies to energy level and position is nontrivial.

Another complicating factor is the determination of series resistance and effective oxide capacitance. These values can be determined using separate transfer length method (TLM) and terraced oxide test structures, respectively. While accurate, such structures require additional processing steps. The oxide capacitance can also be estimated using analytic calculation, but the barrier thickness and dielectric constant are not always accurately known. For these reasons, a self-contained method for parasitic extraction is desired. As part of this work, a self-contained procedure for extraction of series resistance and oxide capacitance, correction of measured capacitance and conductance data, and application of the conductance method for determining characteristic trapping information was developed.

5.2.1 Data Collection Methodology for Application of the Conductance Method

The Ni/AlGaN/GaN Schottky gate stack behaves similar to a metal-oxide-semiconductor (MOS) structure. Within the context of the conductance method, the AlGaN barrier acts effectively as a gate dielectric, making the conductance method valid for analyzing trapping at or near the AlGaN/GaN interface. This section provides a background description of the conductance method for interface trap analysis and highlights variations necessary for accurate application to III-nitride heterostructures. The electrical data from the diodes described in Section 5.3 is used to illustrate the method.

Figure 44 shows the measured capacitance (a) and normalized conductance (b) of the 20s etched Schottky diodes. Significant frequency dispersion (both lateral and vertical) is visible along with the onset of leakage current near 0.5V. While such dispersion may be due in part to frequency-dependent trapping behavior, it is typically also indicative of a parasitic series resistance.

The LCR meter assumes the circuit arrangement of Figure 44A when collecting the data, so some data manipulation is required to extract the conductance due to trapping. Nicollian and Brews proposed the model shown in Figure 44B [78]. Once the series resistance of the test structure, R_S, and the capacitance of the gate dielectric, C_{ox}, are known, the measured data can be analytically corrected to isolate the contribution due to carrier trapping. Nicollian and Brews proposed the following expressions for calculation of R_S and C_{ox}:

$$R_S = \frac{G_{m,a}}{G_{m,a}^2 + \omega^2 C_{m,a}^2} \quad (1)$$

$$C_{ox} = C_{m,a}\left[1 + \left(\frac{G_{m,a}}{\omega C_{m,a}}\right)^2\right] \quad (2)$$

where $C_{m,a}$ and $G_{m,a}$ are the saturation accumulation capacitance and conductance, respectively, and ω is the measurement frequency in rad/s. Then the corrected parallel conductance, G_p, is calculated by [79]

$$\frac{G_p}{\omega} = \frac{-\omega C_{ox}^2 (R_S C_m^2 \omega^2 + R_S G_m^2 - G_m)}{\omega^4 C_m^2 C_{ox}^2 R_S^2 + \omega^2 (C_{ox}^2 R_S^2 G_m^2 + C_m^2 + C_{ox}^2 - 2C_{ox}^2 R_S G_m - 2C_m C_{ox}) + G_m^2}. \quad (3)$$

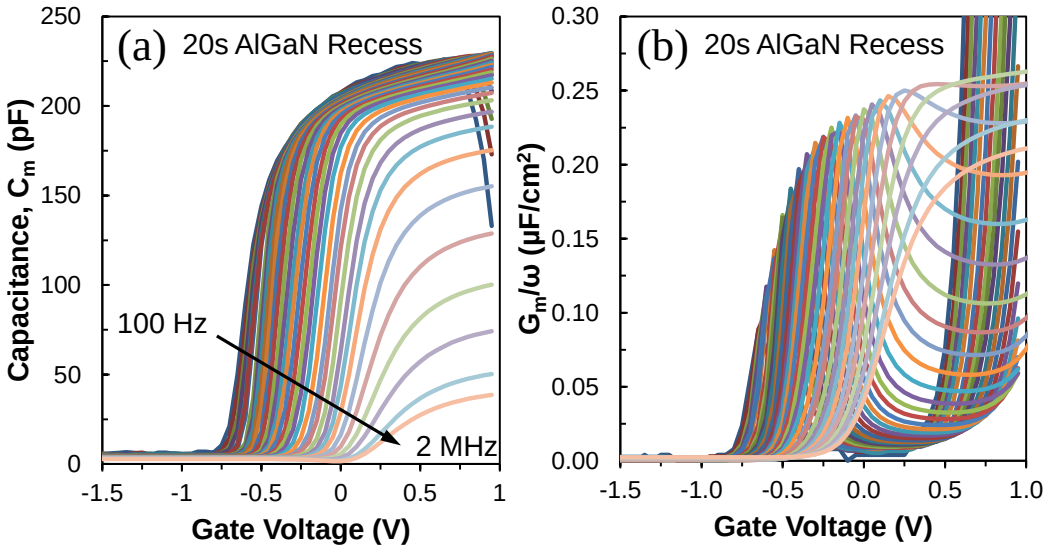

Figure 43: Measured capacitance (a) and normalized conductance (b) of the 20s recessed Schottky diode.

For thin, shallow dielectric barriers, leakage current due to tunneling can be large, and the separation between accumulation and the onset of leakage can be small (see Figure 43B). These factors make determination of the saturation accumulation capacitance difficult and lead to inaccurate estimates of R_S and C_{ox}. For example, the barrier capacitance calculated using (2) and the data of Figure 43 at 10 kHz and V_G = 0.5 V is 214 pF. Assuming a dielectric constant of 9.4 for $Al_{0.26}Ga_{0.74}N$ along with the diode area of 200µm x 200µm leads to a barrier thickness of 15.5 nm. This value is 25% greater than the thickness expected from the characterized etch rate, calling its accuracy into question. Error in the dielectric capacitance assumed strongly impacts the extracted density of traps; thus, alternative methods for quantifying R_S and C_{ox} must be identified.

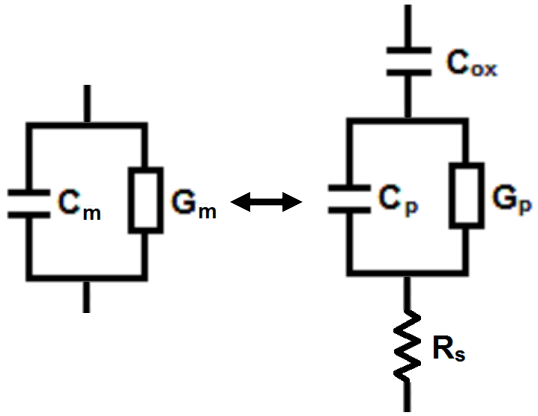

Figure 44: A.) Lumped circuit model used during data acquisition. B.) Equivalent circuit model used for extraction of trap density.

Significant research into methods of determining series resistance and oxide capacitance in the presence of a tunnel current was completed near the turn of the century for application to ultrathin gate dielectrics necessary for continued scaling of digital logic. One such method, proposed by Henson *et al.*, is adopted here for extracting series resistance [82]. Instead of calculating R_S directly for an arbitrary frequency and bias voltage, the accumulation capacitance is plotted as a function of frequency, and the resistance is extracted using a fitting equation.

Figure 45A and Figure 45B show the saturation capacitance – frequency plots for the 40s and 20s recessed diodes, respectively. The data was fit using the equation in Figure 45C and a least squares fitting algorithm with R_S and C_{ox} as free variables. In general, the left side of the plot (low frequency) is controlled by C_{ox} while R_S controls the roll-off frequency and slope (high-frequency behavior).

Three different criteria were used to select the bias voltage where the saturation capacitance occurs: fixed gate voltage, gate voltage corresponding to minimum conductance, and gate voltage at which *dC/dV* decreases to 10% of its maximum. All three are plotted in Figure 45B. From the variation at low frequency, we see that the method used to select the saturation capacitance directly affects the extracted C_{ox}. However, all three traces converge at high frequencies resulting in the extraction of the same series resistance despite the method. Thus, we conclude that this is a good method for determining R_S but a separate method is needed for C_{ox}. Resistances of 522 Ω and 1055 Ω are extracted for the 20 s and 40 s etched samples, respectively. The increase in

resistance is expected due to the decrease in channel carrier concentration resulting from additional thinning of the AlGaN barrier [83].

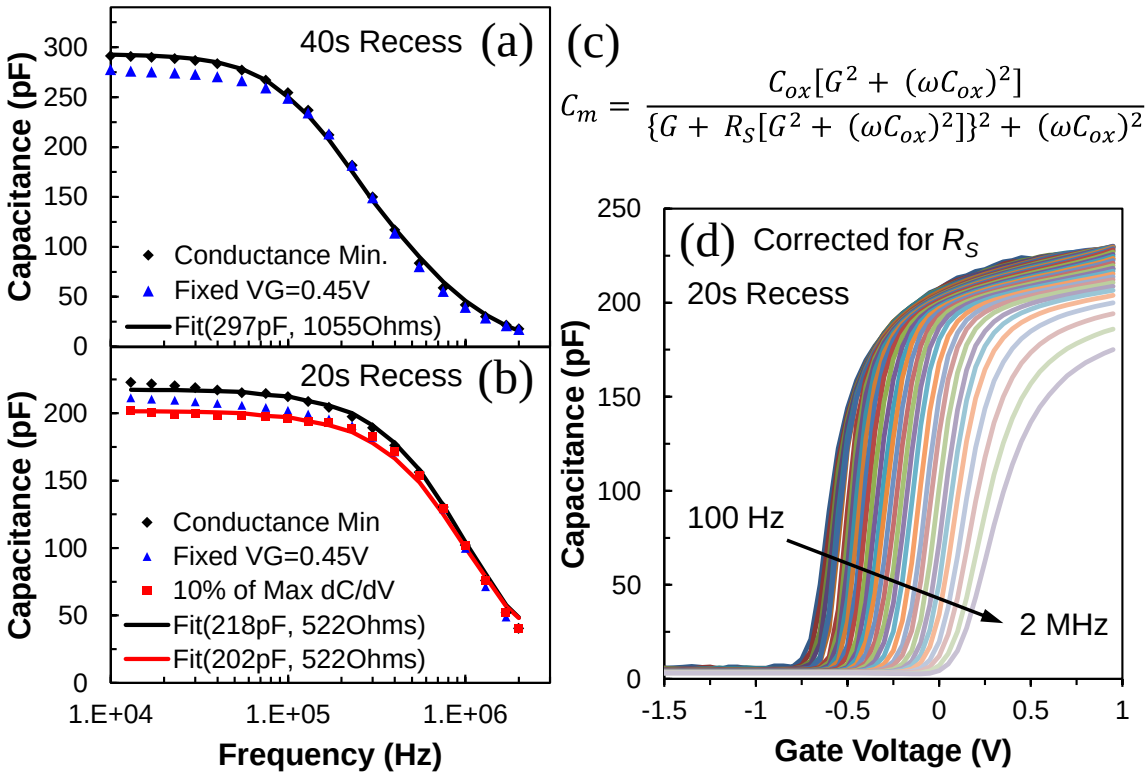

Figure 45: Accumulation capacitance versus AC signal frequency for the 40s (a) and 20s (b) recessed samples. Saturation capacitance is selected using three different criteria: fixed gate voltage, gate voltage corresponding to minimum conductance, and gate voltage at which *dC/dV* decreases to 10% of its maximum. R_S and C_{ox} are extracted through least-squares fitting of the equation shown in (c). The measured capacitance is corrected for R_S and plotted in (d).

Figure 45D shows the 20 s recessed capacitance data after R_S correction. Frequency dispersion is greatly reduced but is not fully removed. Use of (1) yields R_S of 764 Ω (+44%), and correction according to that value results in nearly complete removal

of the vertical frequency dispersion. In that case, the impact of interface traps is obscured by overestimation of R_S.

In the presence of leakage current, identifying the bias voltage corresponding to the accumulation capacitance is challenging. For this reason, we pursue an extraction method that fits across a range of bias voltages (opposed to the R_S case where we fit with respect to frequency).

Many methods for extracting oxide capacitance have been previously reported [84]. Several of them were applied to the data set above to determine their usefulness. First, the capacitance data was fit using a quantum-mechanical *CV* simulator [85]. However, modeling of the carrier concentration associated with the 2DEG proved challenging and led to large fit errors. Next, the analytic methods of Maserjian [86] and Kar [87] were applied. Both of these techniques rely on fitting of a tangential line to a plot of $1/C$ versus $[d(1/C^2)/dV]^{1/n}$ in the strong accumulation regime. However, this regime is where leakage effects are most pronounced. Instead, we adopt the method proposed by Islam and Haque [88]. In this technique, the measured capacitance is plotted versus $[dC/dV]^{1/3}$, and a tangent line is fit in the weak accumulation regime. Extrapolation of this tangent line to the *C* axis yields the dielectric capacitance.

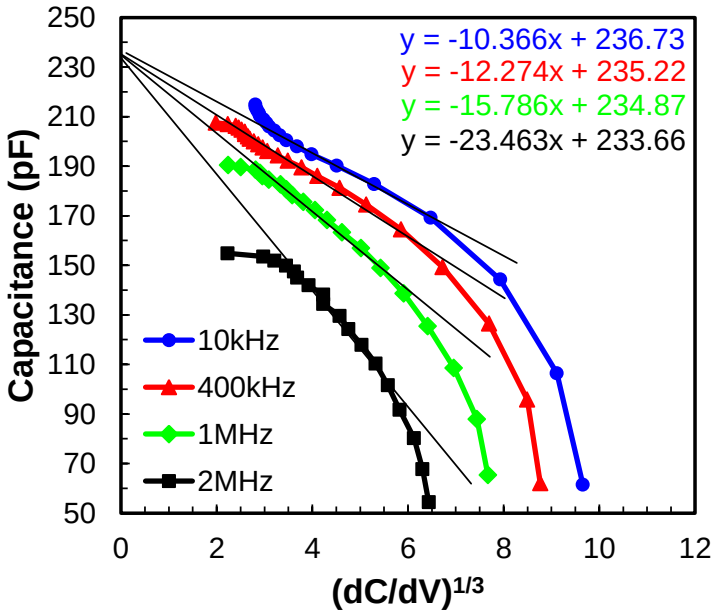

Figure 46: Haque plots of the 20 s recessed AlGaN/GaN diodes as a function of frequency for extraction of oxide capacitance. Capacitance data has been corrected for series resistance. Oxide capacitance is determined from the *y*-intercept of the linear fit line in the weak accumulation regime.

Figure 46 shows Haque plots as a function of frequency corresponding to the 20 s recessed diodes. Low frequency data was too noisy for reliable linear extrapolation. The highest frequency plot should provide the most accurate C_{ox} estimation as it will contain the smallest trapping component. It is important to note that the capacitance data was corrected for series resistance prior to generating the Haque plots. Similar plots were generated for the 40 s samples as well. Barrier capacitance was found to be 234 pF and 399 pF for the 20 s and 40 s samples, respectively. These values translate to barrier thicknesses near those expected from the etch rate.

Figure 47A shows the normalized parallel conductance after correction for R_S and C_{ox} using (3). The leakage at high bias has been accounted for, and now a second trapping artifact is visible. Figure 47B shows G_p/ω versus ω, again highlighting two distinct trapping regimes. Both regions can be fit using the single-trap state fitting expression,

$$\frac{G_p}{\omega} = \frac{qD_{it}\omega\tau}{1 + (\omega\tau)^2}. \qquad (4)$$

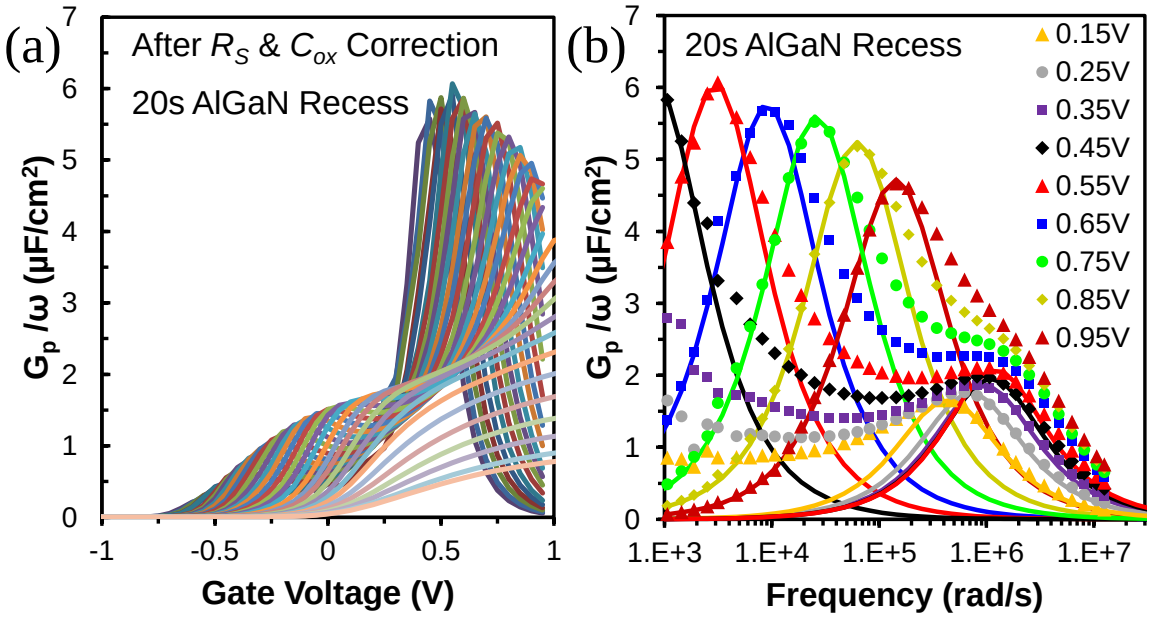

Figure 47: A.) Normalized conductance of the 20 s recessed samples after R_S and C_{ox} correction [see (3)]. B.) G_p/ω versus frequency showing two trapping regimes. Both regions can be fit with single-trap state fitting expressions (solid lines) [see (4)].

5.2.2 Trap Time Constant Estimation

Once corrected conductance data has been generated, it can be normalized and used to generate contour maps to aid in analysis of the trapping behavior (Figure 49). These plots highlight trapping density at a respective frequency (inverse of the trap time constant). For extraction of trap position and energy, an analytic method for calculating trap time constants is required.

Trap time constants (τ_{eff}) depend on two things: the depth in energy of the trap level and the distance from the primary source of free carriers (tunnel length). As the trap energy level moves deeper into the band gap, the time to capture and emit increases [see (6)]. Similarly, as the tunneling distance increases, the time required to capture a free carrier increases [89].

$$\tau_{\Delta E} = \frac{1}{\sigma v_{th} N_C} e^{\frac{E_C - E_T}{kT}} \tag{6}$$

$$\tau_{eff} = \tau_{\Delta E} e^{\frac{\Delta x}{\lambda}} \tag{7}$$

$$\lambda = \frac{\hbar}{\sqrt{8 * m_{eff} * q * (E_C - E_T)}} \tag{8}$$

Where $\tau_{\Delta E}$ is the capture time associated with the trap energy level, σ is the trap capture cross section, v_{th} is the average electron thermal velocity, N_C is the conduction band density of states, k is Boltzmann's constant, T is the temperature, Δx is the physical distance between the trap and the 2DEG, λ is the attenuation constant, $\hbar$ is the normalized Planck's constant, and m_{eff} is the effective electron mass. If we assume that, due to the low intrinsic carrier concentrations in undoped III-Nitrides, the 2DEG is the

primary source of free carriers, we can generate a map of the resonant frequency of a trap state as a function of the position and energy of the trap (Figure 50).

5.3 AlGaN/GaN Interface Characterization

Investigation of the trapping behavior of AlGaN/GaN gate stacks began with the fabrication and analysis of AlGaN/GaN Schottky diodes. The diodes allow qualification of the trapping behavior at the AlGaN/GaN interface and in the AlGaN barrier. This information will allow isolation of the trapping contributions of dielectric/AlGaN interfaces through differential comparison with AlGaN/GaN MOS capacitors.

5.3.1 AlGaN/GaN Diode Fabrication

Two sets of Schottky diodes were fabricated using $Al_{0.26}Ga_{0.74}N$/GaN on Si(111) substrates (4" diam.). The initial AlGaN barrier thickness was 17.5 nm and was capped with a thin GaN layer. The total thickness of nitride epitaxy, including the strain relaxation layers, was 2 μm. Hall measurements yielded a sheet resistance of 390 Ω/sq, and two-dimensional electron gas (2DEG) density of ~8 x 10^{12} cm^{-2}.

Device processing began with deposition of 140 nm of Si_xN_y by PECVD at 350 °C to serve as a surface state passivation layer. Then, 100 nm of Cr was evaporated and used as a hard-mask for subsequent dry etching of the AlGaN barrier. The Cr and Si_xN_y were wet etched at the Schottky contact region to create openings for the dry etch. Using an Oxford PlasmaLab 100 Plus Reactive Ion Etching (RIE) system, the AlGaN barrier was recessed for 20 s (Sample 1) or 40 s (Sample 2), leaving behind 12.8 nm and 8.1 nm of AlGaN, respectively. The Inductively Coupled Plasma (ICP) RIE was performed at SF_6 and Ar flow rates of 40 sccm and 10 sccm, respectively, with RF and ICP powers of

200W and 400W at a chuck temperature of 16 °C and a pressure of 44 mTorr. The Cr hard-mask was stripped and the Si_xN_y at the ohmic region was removed using Buffered Oxide Etch (BOE). The Ti(40 nm)/Al(100 nm)/Ni(40 nm)/Au(50 nm) metal stack was evaporated and patterned by a lift-off process prior to annealing at 865 °C for 30 s. Finally, the Ni(50 nm)/Au(50 nm) Schottky contact was evaporated and patterned by a lift-off process.

Capacitance and conductance as a function of gate voltage were measured using an Agilent E4890A precision LCR meter. Step size of 0.05 V, dwell time of 230 ms, and AC magnitude of 20 mV were used resulting in a sweep speed of 0.22 V/s. Measurements were collected at frequencies varying from 100 Hz to 2 MHz. At all frequencies, measurements were performed in the dark at room temperature, and gate voltage was swept from negative to positive with the 2DEG grounded.

5.3.2 Schottky Gate Leakage

Figure 48 shows the normalized absolute value of the gate leakage current for both diode sample sets. The large leakage currents under forward bias highlight the need for dielectric gating. The additional barrier recess time clearly shifts the onset of through barrier tunneling to the left and increases reverse bias leakage current, as well.

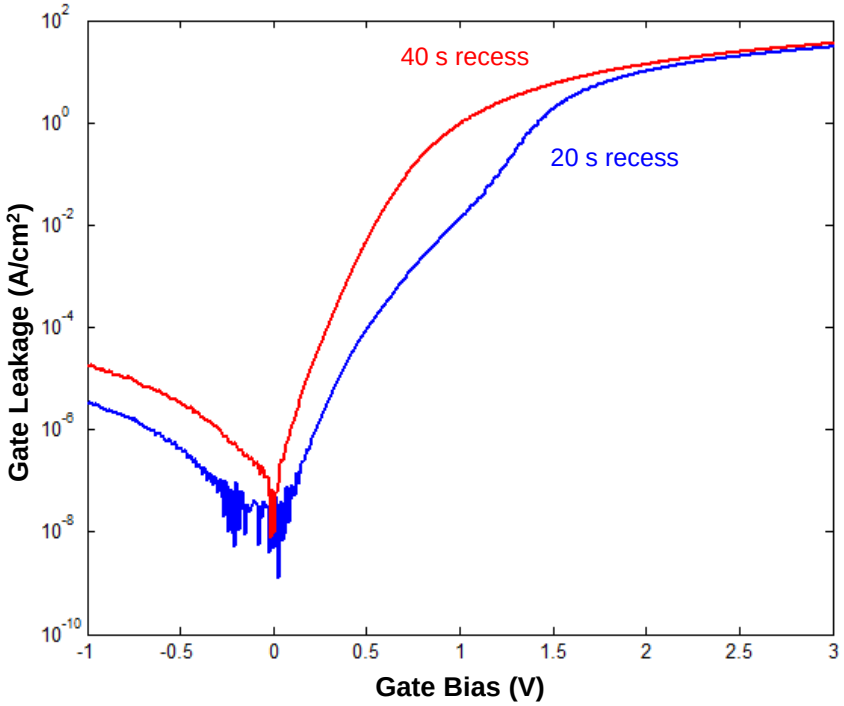

Figure 48: A logarithmic plot of the absolute value of gate leakage normalized by diode area for both the 40 s and 20 s recessed AlGaN/GaN Schottky diodes.

5.3.3 AlGaN/GaN Interface & Barrier Trapping

The procedure detailed in Section 5.2 was applied to both the 20 s and 40 s recessed samples. The corrected conductance data was then normalized and used to generate contour maps to aid in analysis of the trapping behavior of the Schottky diodes. When fitting conductance data using (4), D_{it} can be approximated by [78]:

$$D_{it} \approx \frac{2.5}{A * q} \left(\frac{G_p}{\omega}\right)_{max} \qquad (5)$$

A refers to the gated area, and q refers to the charge of an electron. Thus, D_{it} is directly estimated by plotting G_p normalized by $2.5/(A*q*\omega)$. Such plots are shown in Figure 49.

Two trapping regimes are visible. In Figure 49A, the onset of the first trapping regime occurs near V_G = -0.5 V, shortly after channel accumulation. We attribute this behavior to trapping at the AlGaN/GaN interface. The slope of the profile is roughly linear, indicating efficient movement of the Fermi level in response to applied bias [81], up until the onset of the second trapping regime near V_G = 0.5 V. At that point, charge due to trapping deeper in the AlGaN barrier (farther from 2DEG, nearer to surface) inhibits modulation of the band-bending at the interface. The Fermi level at the interface is effectively pinned until the second trapping regime fills to a similar energy level. Beyond this point, modulation is expected to resume albeit less efficiently because the incremental increase of applied bias voltage is split between the two trapping regimes.

It is important to note that the slope of the trapping profiles (i.e. higher frequency / shallower traps with increasing voltage) is not consistent with fixed energy bulk trap states. Such behavior indicates two discrete planes of traps with distributed trap energies. Potential physical explanations for the observed phenomenon will be discussed below.

In Figure 49B, the onset of trapping occurs near V_G = -0.2 V. The additional thinning of the AlGaN barrier pushes channel turn-on toward enhancement mode operation. Compared to the 20 s etched sample, a decrease in D_{it} is observed, especially at low bias. We believe this is simply due to the decrease in free carrier concentration in the 2DEG due to the reduced magnitude of piezoelectric polarization. Higher order conduction band energy states are empty allowing a smaller energetic cross-section of trap states to be in resonance at a given applied bias. The slope of the first trapping profile remains constant, indicating similar band modulation efficiency at the interface;

however, the slope of the second trapping profile steepens indicating improved modulation efficiency. This is expected due to the thinning of the barrier.

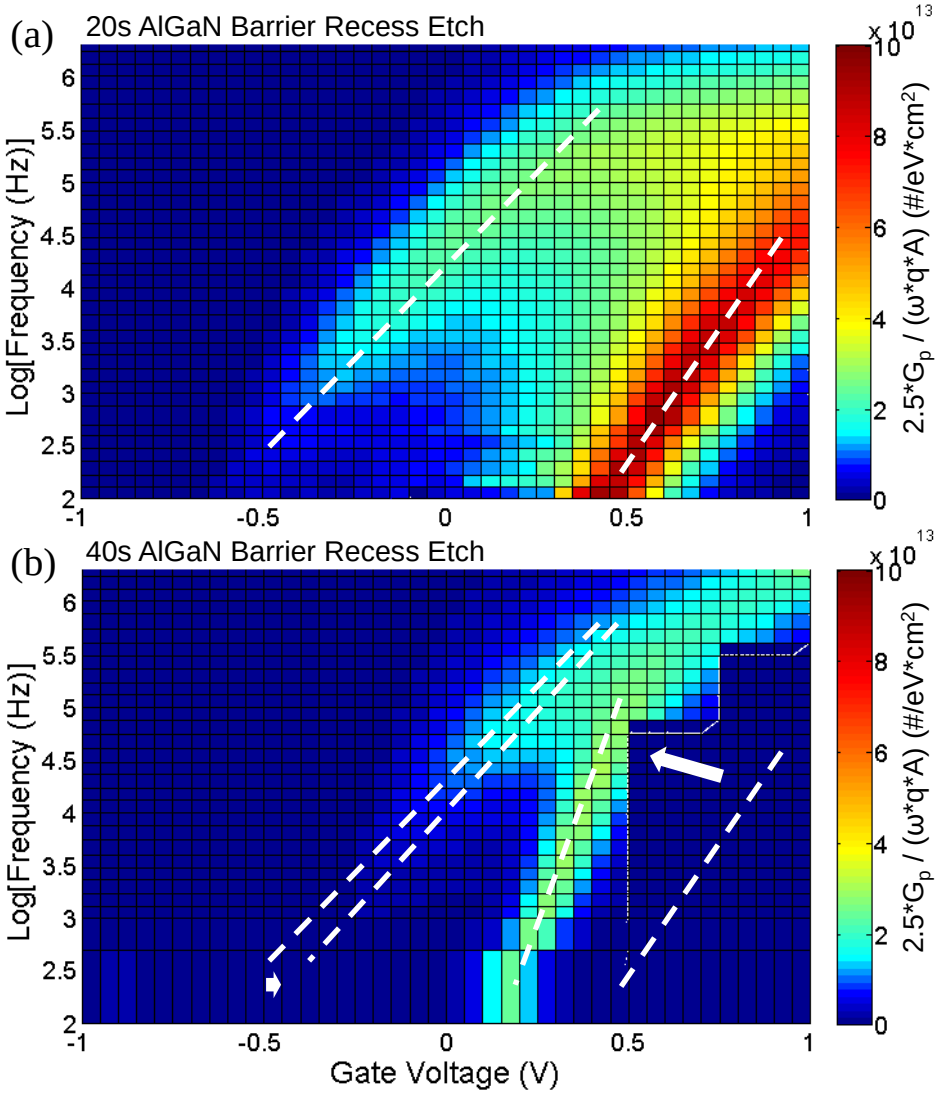

Figure 49: Contour maps of the normalized parallel conductance ($2.5G_p/\omega qA$) as a function of frequency and gate voltage measured at room temperature of 20s (a) and 40s (b) recessed AlGaN/GaN Schottky diodes. Intensity directly correlates to trap density, D_{it}, at that bias and resonant frequency.

In order to more accurately determine the location of the second trapping interface, we generate trapping maps to display characteristic resonant frequency as a function of trap energy and position (Figure 50). The frequency range is clipped to correspond to the frequency capabilities of the LCR meter, and the results are overlaid on band diagrams of the Schottky-gated region calculated by self-consistent numerical solution of Poisson's equation. Figure 50 shows trapping maps overlaid on band diagrams of the 20 s recessed gate stack for several bias conditions. A constant capture cross-section of $1x10^{-16}$ cm^{-2} was assumed along with an $Al_{0.26}Ga_{0.74}N$ density of states of $3.34x10^{18}$ cm^{-3} and a thermal velocity of $2.61x10^{7}$ cm/s. It is important to note that the majority of surface energy levels are inaccessible in the frequency range used. Thus, trapping artifacts observed near channel-accumulation-bias conditions should be localized near the AlGaN/GaN interface. Similar behavior was observed for the 40 s etched sample.

The positions of the two trapping planes in Figure 50 (~3Å and ~20Å from the AlGaN/GaN interface) were used to extract trap energy levels from the time constants enabling plotting of D_{it} as a function of trap energy in Figure 51. All traps are assumed to be located in the AlGaN layer and are referenced to the AlGaN conduction band edge.

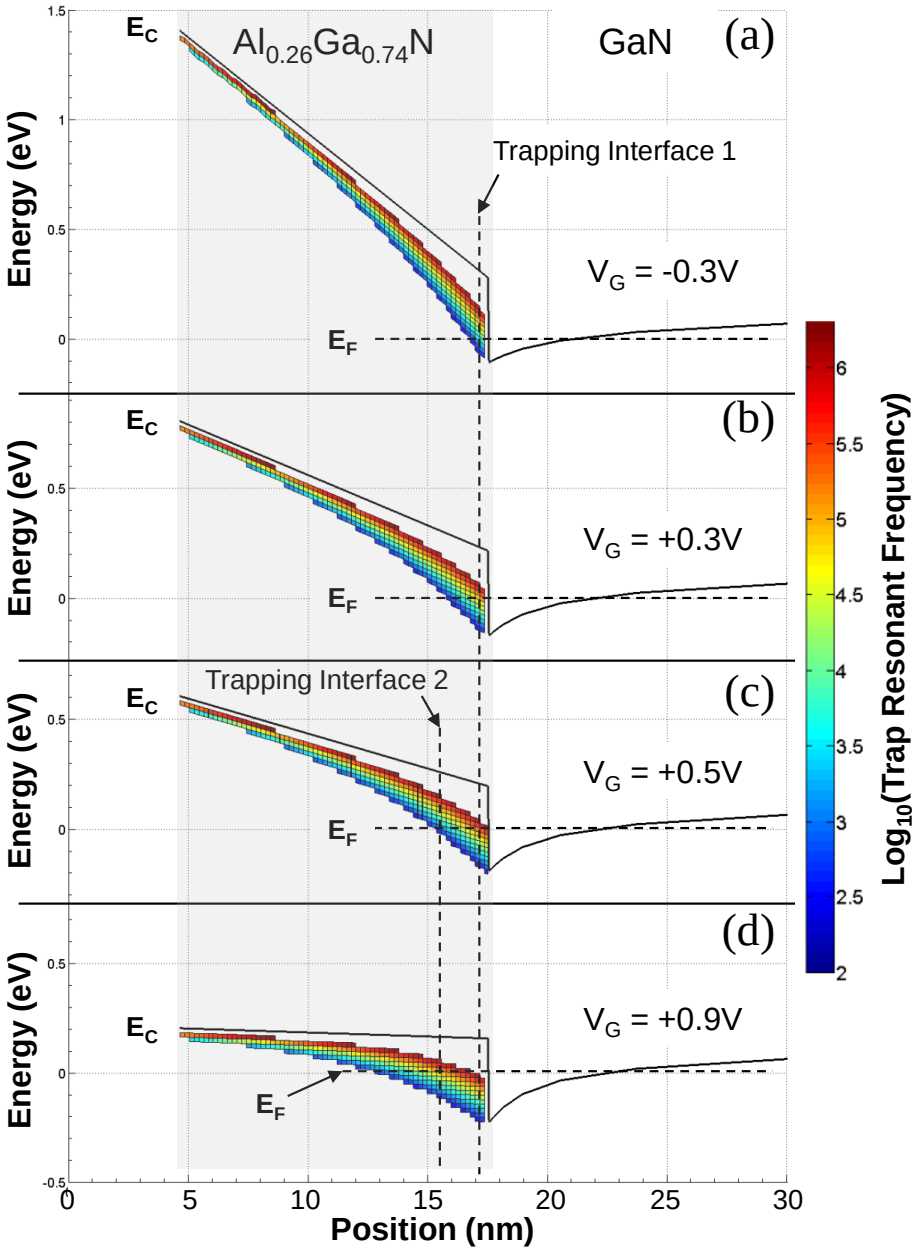

Figure 50: Potentially accessible trap locations are overlaid on band diagrams generated by numerical simulation at four bias conditions: -0.3V (a), +0.3V (b), +0.5V (c), and +0.9V (d). The boundaries of the trapping window are determined by the frequency limitations of the LCR meter. The color at each trapping location corresponds to the resonant frequency of the trap.

The physical origin of interface traps is well understood. Dangling bonds and lattice defects create mid-gap energy levels. Since observation of the trapping behavior is coincident with channel accumulation, the interface traps must be located just inside the AlGaN layer. Several researchers have also reported fixed energy AlGaN barrier traps [90]; however, the observation of a second plane of traps spatially removed from the channel has not been previously reported.

We believe the second trapping interface arises from the compositional pulling effect. Due to the strain caused by lattice mismatch, Al (or the low percentage column III material) diffuses away from the interface during MOCVD growth of the barrier film [91-93]. The result is a thin strain relaxation film at the interface with Al composition below the target composition.

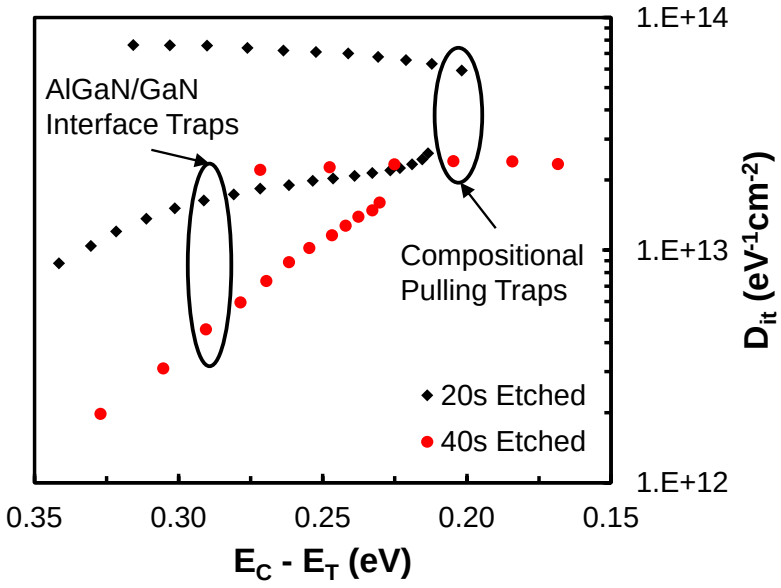

Figure 51: Trap density with respect to position in the AlGaN band gap at the two trapping planes identified in Figure 50. The density decreases after 40 s etch due to the decrease in resonant volume arising from faster surface potential modulation.

We profiled the composition of the AlGaN layer using secondary ion mass spectroscopy on a blanket sample (Figure 52). Analysis was performed without a standard, so direct extraction of percent composition is not possible. However, comparison of the Al and Ga signals in the AlGaN region qualitatively shows that the Al mole fraction is lowest at the AlGaN/GaN interface. The Al content increases toward the surface of the film. No clear composition step is visible, but that may be due to resolution limitations and knock-on effects.

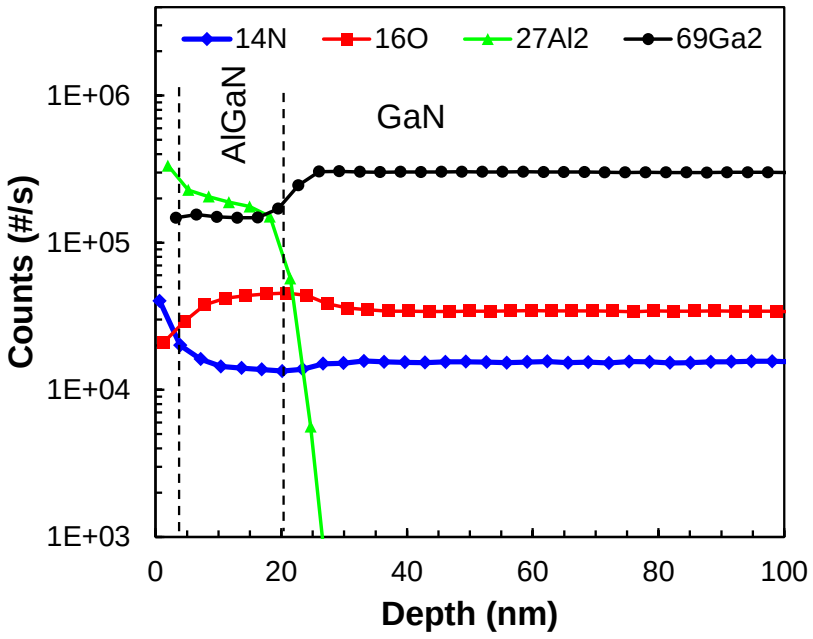

Figure 52: SIMS profile of AlGaN/GaN heterostructure showing Al percent composition gradient.

5.4 Dielectric/AlGaN Interface Characterization

Dielectric-gated GaN-based devices are receiving much attention due to their ability to simultaneously limit leakage currents while enabling high-voltage and/or high-frequency switching [94, 95]. Whether because of high blocking voltages, or aggressively scaled device dimensions (necessary for mm-wave operation) high internal electric fields develop and cause leakage currents. Minimization of these currents through optimization of the gate stack and the dielectric/GaN interface has been the focus of much research [12, 15, 18, 20, 21, 64]. *In situ* MOCVD Si_3N_4 has shown particular promise for enabling low interface trap densities [12, 22, 96], and when combined with a large bandgap dielectric such as Al_2O_3, has enabled low-leakage

performance. Beryllium oxide is another interesting dielectric that has received significant attention for Si and other III-V applications due to its large band gap (10.6 eV), thermal stability, and self-cleaning characteristics [97-100]. Additionally, the high thermal conductivity of BeO (300 W/m*K) makes it appealing for power applications.

In an attempt to perform a comprehensive study, several dielectrics were selected and deposited on AlGaN/GaN using CVD techniques: ALD H_2O-Al_2O_3, ALD O_3-Al_2O_3, ALD BeO, ALD H_2O-HfO_2, ALD O_3-HfO_2, and PECVD Si_xN_y. Thin blanket films (~30 Å) were deposited for XPS analysis, and thicker films (~200 Å) were deposited for MOS capacitor fabrication. The notable exception was the ALD BeO. The deposition was performed by a collaborator in Austin, so a single thickness (~30 Å) was used for both XPS and capacitor fabrication.

5.4.1 Dielectric/AlGaN/GaN Capacitor Fabrication

GaN/$Al_{0.26}Ga_{0.74}$N/GaN (2/17.5/800 nm) on silicon substrates were cleaned in 1:1 HCl:DI-H_2O for two minutes immediately prior to introduction to the deposition chamber (ALD or PECVD). Then six unique interface passivation layer and bulk gate dielectric combinations were deposited as detailed in Table 4. The beryllium precursor, $Be(C_2H_5)_2$ (DEBe), is not commercially available and had to be synthesized using Grignard metathesis as previously described by Yum, *et. al.* [99, 100]. TaN / Cr (20/100 nm) gate contacts were deposited by evaporation and patterned using Union Etchants CR1A chrome etchant followed by SF_6 / Ar ICP-RIE of the TaN. The plasma conditions were 30 sccm SF_6, 30 sccm Ar, 100W bias, 500W ICP, 10 mtorr, and 23 °C, leading to a removal rate of ~40 nm/min. Then 100 nm of Si_xN_y was deposited by PECVD to ensure

AlGaN surface state passivation and protect the gate during processing of the ohmic contacts.

Table 4: Deposition conditions and thicknesses of the six gate dielectrics evaluated in Section 5.

Wafer #	IPL	Method	Source Gases	Carrier	Temp.	Bulk	Method	Source Gas	Carrier	Temp.
1	3 nm Al_2O_3	ALD	H_2O, TMA	Ar	480 °C	17 nm HfO_2	ALD	H_2O, TMAH	N_2	200 °C
2	3 nm Al_2O_3	ALD	O_3, TMA	Ar	480 °C	17 nm HfO_2	ALD	H_2O, TMAH	N_2	200 °C
3	3 nm HfO_2	ALD	H_2O, TMAH	Ar	330 °C	17 nm HfO_2	ALD	H_2O, TMAH	N_2	200 °C
4	3 nm HfO_2	ALD	O_3, TMAH	Ar	330 °C	17 nm HfO_2	ALD	H_2O, TMAH	N_2	200 °C
5	3 nm BeO	ALD	H_2O, DEBe	N_2	250 °C	none				
6	10 nm Si_xN_y	PECVD	SiH_4, N_2	N/A	350 °C	none				

Contact windows were patterned and transferred into the Si_xN_y using BOE. Samples 1-4 were then processed through RIE to etch the HfO_2 (described in detail in Section 3.1.3) while the BeO and Si_xN_y gate dielectrics of Samples 5 and 6 were also etched in BOE. After opening contact windows, the photoresist was stripped. All samples were then cleaned in 1:10 HCl:DI-H_2O immediately prior to introduction to the DC magnetron sputter chamber for deposition of 7/200/20 nm of Ta/Al/Ta. The Ta was etched using RIE. The plasma conditions were 25 sccm SF_6, 10 sccm O_2, 100W bias, 20 mtorr, and 23 °C. This was followed by a wet aluminum etch in JT Baker Aluminum Etchant before removal of the final Ta layer using the same RIE conditions as above. The ohmic alloy anneal took place at 575 °C in ambient N_2 and lasted for four minutes. Due to the excellent thermal stability of TaN, it is not expected to interact with the gate dielectric at this temperature. TLM structures processed in parallel with the capacitors indicated a contact resistance of 0.79 Ohm*mm (Figure 53). Finally, windows were

opened in the SixNy using BOE to enable probing of the gate metal. A cross-section of the devices is shown in Figure 54.

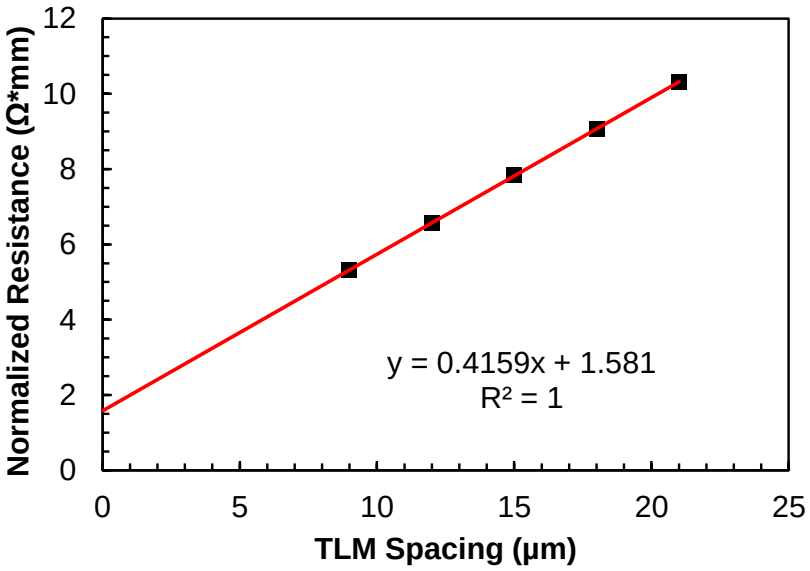

Figure 53: Resistance vs. spacing plot from TLM test structures processed in parallel with the gate-first capacitors.

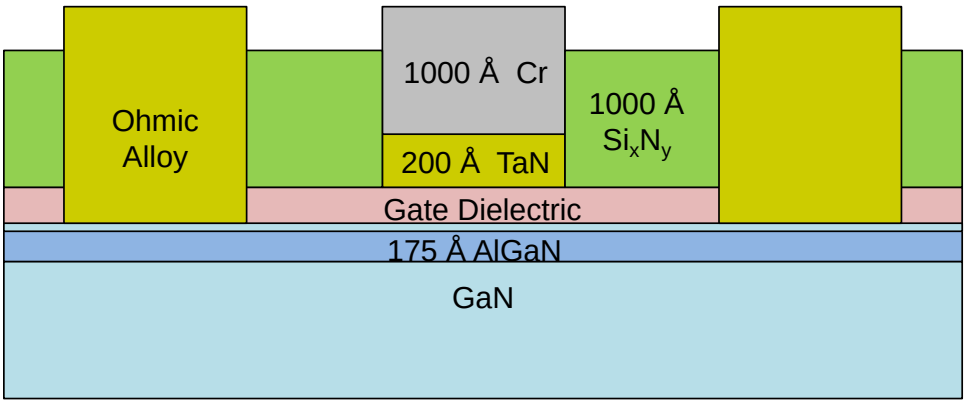

Figure 54: Cross-section cartoon of gate-first AlGaN/GaN capacitors.

Capacitance and conductance as a function of gate voltage were measured using an Agilent E4890A precision LCR meter. Step size of 0.05 V, dwell time of 230 ms, and AC magnitude of 20 mV were used resulting in a sweep speed of 0.22 V/s. Measurements were collected at frequencies varying from 100 Hz to 2 MHz. At all frequencies, measurements were performed in the dark at room temperature, and gate voltage was swept from negative to positive with the 2DEG grounded. A Hewlett-Packard 4145 parameter analyzer was used for I-V measurements. Again, the gate voltage was swept from negative to positive with the 2DEG grounded.

5.4.2 Dielectric/AlGaN/GaN Gate Leakage

The absolute gate leakage current of each of the gate-first capacitors is plotted in Figure 55 along with the leakage current observed in the gate-last baseline technology. Two things are obvious from the plot. First, the thick HfO_2 deposited on top of the thin interface passivation layers does not postpone the onset of through-gate leakage. All four of the IPL + HfO_2 samples break down at about the same time that the 3 nm BeO sample breaks down: around 1 V. The gate-last baseline also employed water-based ALD HfO_2, and the onset of dielectric break down does not occur until higher voltages. Thus, the ohmic contact anneal must be the cause of the increased leakage. Most likely, crystallization of the dielectric occurs. The second important observation from Figure 55 is that before the onset of tunneling, the forward bias gate leakage of the BeO capacitor is lower than the leakage of the baseline. This leakage is better than some of the best reports using HfO_2 [101] and SiO_2 [19] gate dielectrics, and is comparable to the leakage

obtained using Al_2O_3 [12]. Due to this improvement, BeO and the physics behind its low-leakage performance will be the primary focus of the remainder of this section.

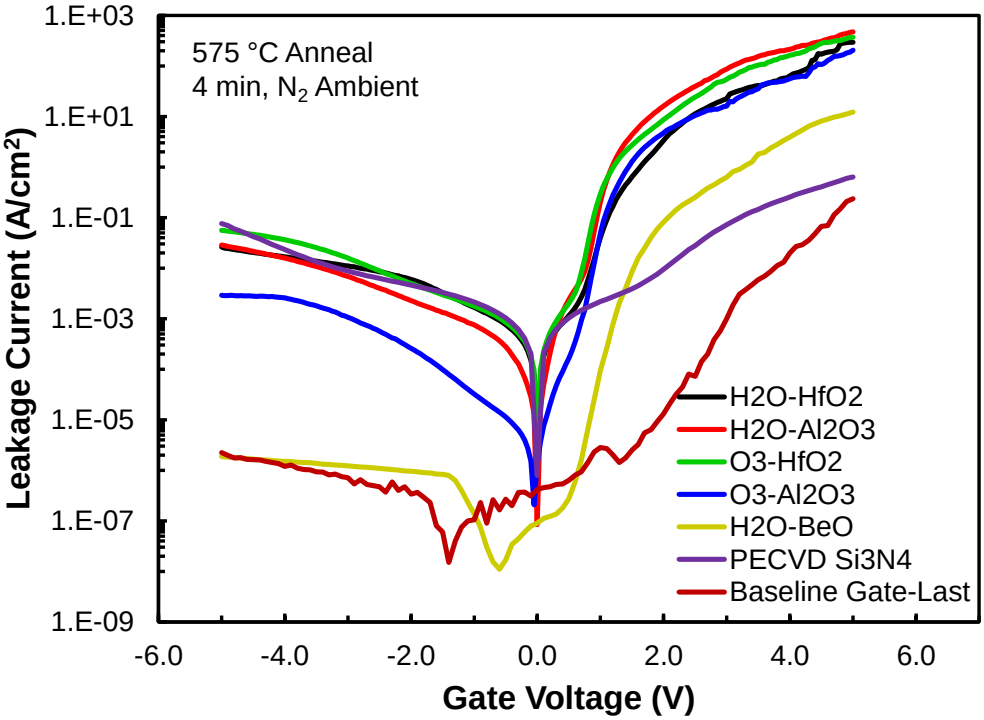

Figure 55: Gate leakage of MOS capacitors with several different gate dielectrics fabricated using a gate-first process flow.

XPS analysis was performed on as-deposited and annealed blanket BeO samples to determine the band alignment and analyze the thermal stability of the BeO/AlGaN/GaN gate stack. The samples were analyzed using an Al-Kα x-ray source (1486.6 eV) and hemisphere analyzer. The known N 1*s* binding energy of GaN (397.7 eV) was used for charge referencing of all spectra [102].

Figure 56 shows XPS scans of the Be 1*s* and O 1*s* regions. No change in the Be-O binding envelope is visible after anneal, confirming the strength of the BeO bond (asymmetry would be visible if decomposition occurred). This bond strength likely contributes to its ability to maintain low-leakage performance despite high temperature anneal. However, the O 1*s* envelope shifts toward a lower binding energy indicating increased gallium oxide content. This implies that a significant concentration of unincorporated oxygen exists in the as-deposited dielectric. BeO is known to be an excellent diffusion barrier, so the oxygen is not believed to have originated outside of the film [97].

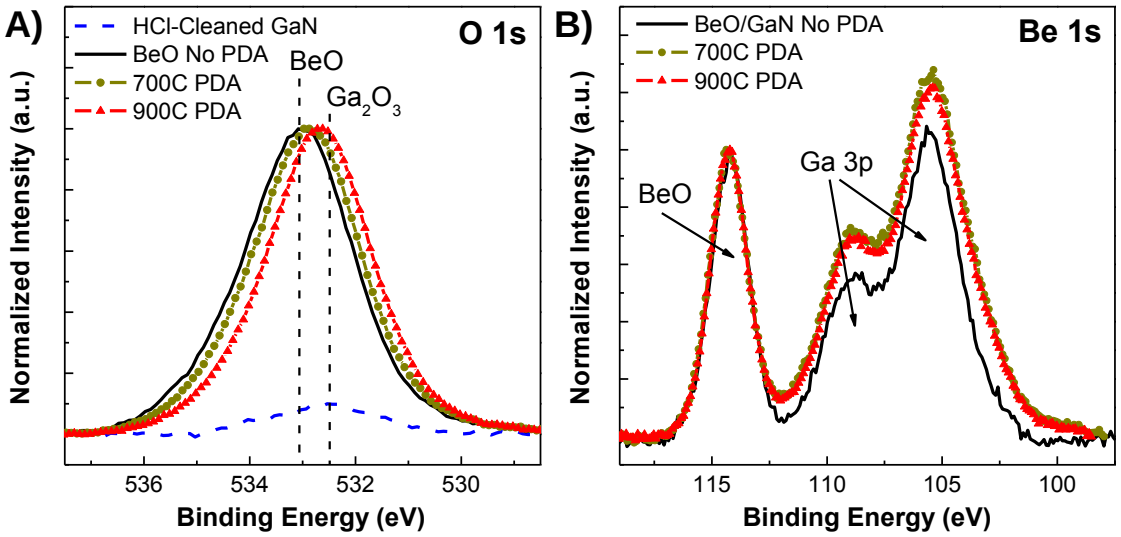

Figure 56: A) XPS spectra of O 1*s* energy region. B) XPS spectra of Be 1*s* energy region.

Figure 57 shows XPS scans of the Ga 2*p* and C 1*s* energy regions. Ga 2*p* spectra are used for qualification of the BeO/GaN interface due to the increased surface sensitivity of low kinetic energy electrons [103]. The Ga 2*p* reveals that an interfacial layer forms during deposition and anneal similar to that of ALD HfO_2 [15]. Significant GaO_x and GaO_xN_y exist as deposited, and high temperature anneal leads to additional interfacial contamination by hydrogen and carbon. Figure 57B shows that the BeO has higher carbon content compared to other ALD processes. This is due to the precursor synthesis process and has been previously reported [99]. Plasma enhanced ALD is recommended to help reduce carbon content and unincorporated oxygen content in the future; however, Texas A&M University does not have the capability at this time.

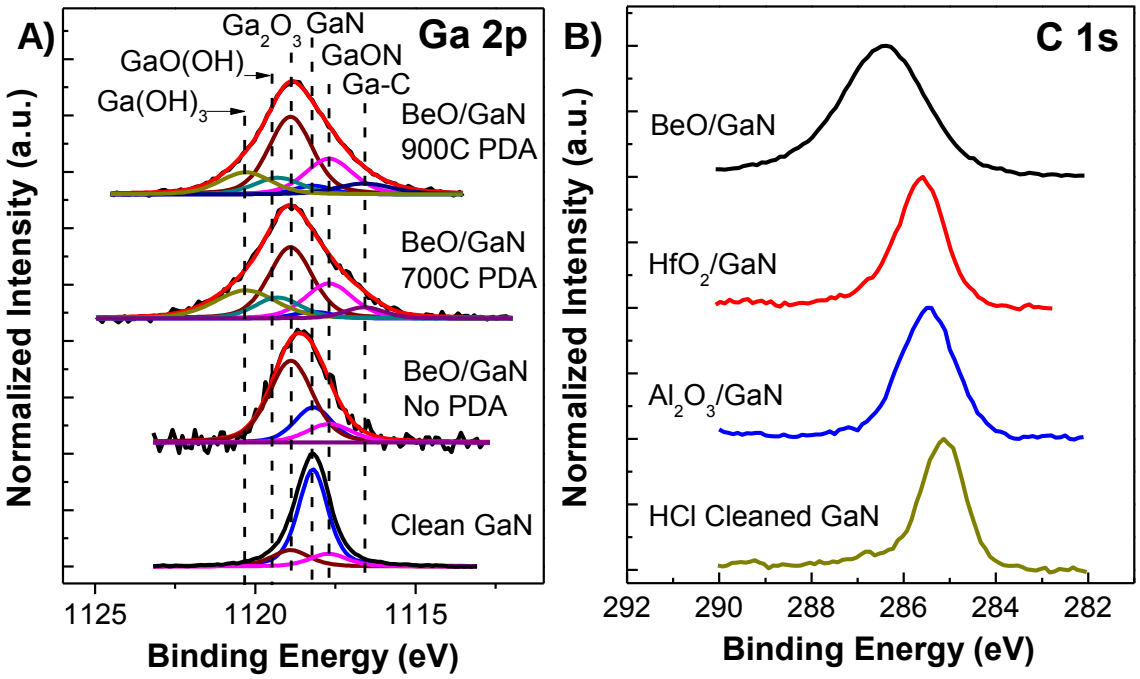

Figure 57: A) XPS spectra of Ga 2*p* energy region. B) XPS spectra of C 1*s* energy region.

Figure 58 shows TEM images of the annealed BeO sample (Figure 58A) and an as-deposited H_2O-HfO_2 sample (Figure 58B). From Figure 58A, we see that the BeO layer remains amorphous, even after anneal, and the presence of an interfacial layer (expected from XPS) is confirmed. Slight expansion of the film from 3 nm to ~5 nm is observed and attributed to diffusion of the carbon and unincorporated oxygen observed in XPS. By comparison, the HfO_2 appear polycrystalline, even before anneal. Large crystalline grains are visible in Figure 58B that nearly stretch across the entire film thickness. Leakage along these grain boundaries is believed to be the cause of the early onset of through gate leakage observed in Figure 55.

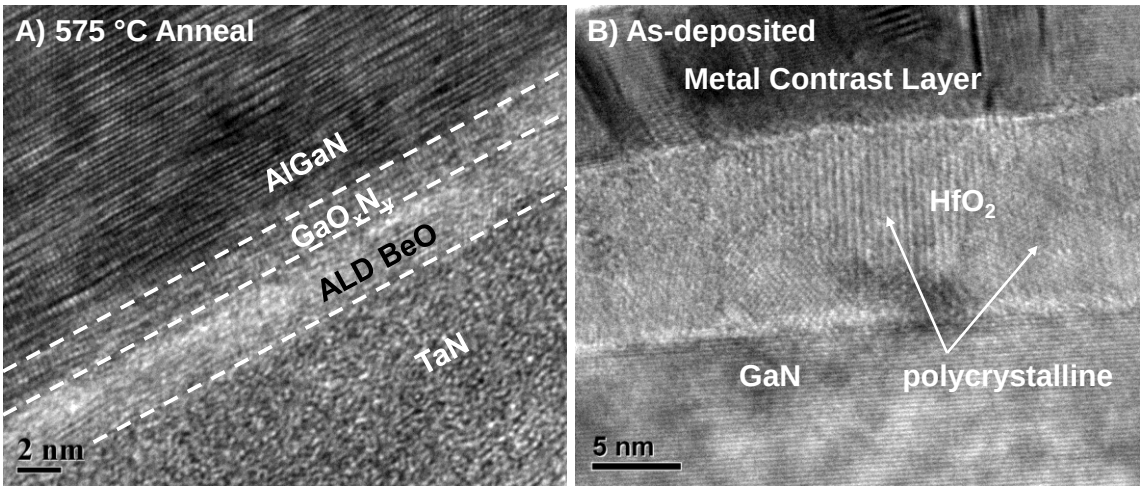

Figure 58: A) TEM of TaN/BeO/AlGaN gate region after 575 °C ohmic anneal. B) TEM of ALD HfO_2 as-deposited using H_2O and TEMAH precursors.

Figure 59 presents a comparison of the band structures of HfO_2/AlGaN and BeO/AlGaN as calculated using a numerical solver. The band alignment of BeO/AlGaN was established using the valence band offset (VBO) extracted from XPS spectra taken before and after dielectric deposition. The VBO is approximated as:

$$VBO = \left(E_{Ga\ 3d}^{AlGaN} - E_{VBM}^{AlGaN}\right) - \left(E_{Ga\ 3d}^{BeO/AlGaN} - E_{VBM}^{BeO/AlGaN}\right) = -1.9\ eV$$

The conduction band offset (CBO) of ~4.5 eV is nearly four times larger than that of HfO_2 on AlGaN. Large conduction band offset and the thermal stability of the Be-O bond are what enable the low-leakage performance observed in Figure 55.

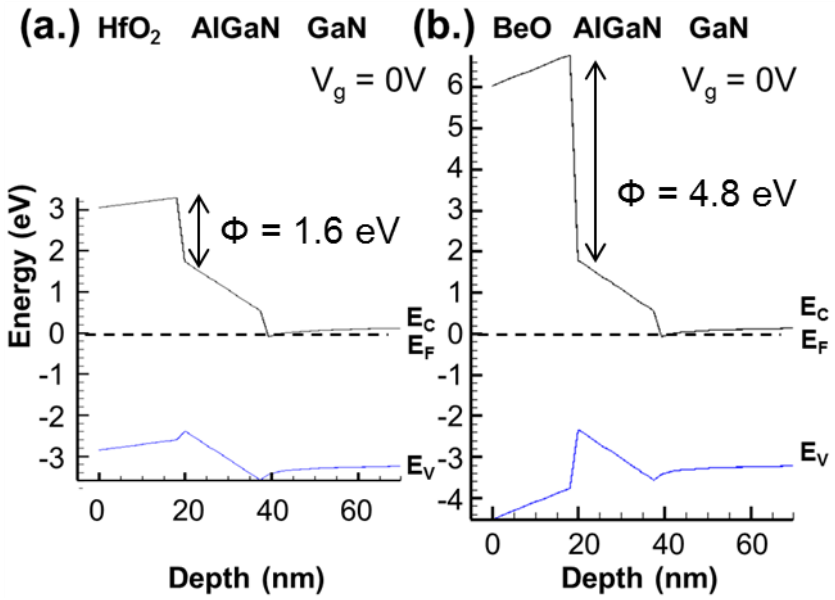

Figure 59: Numerically solved band diagrams for Ni/HfO_2/AlGaN/GaN (A) and TaN/BeO/AlGaN/GaN (B).

5.4.3 Dielectric/AlGaN/GaN Interface Trapping

The conductance method (as described in detail in Section 5.3) was used to determine the trapping behavior of the fabricated dielectric/AlGaN interfaces. In order to minimize current lag and frequency dispersion effects, the density of traps at the dielectric/AlGaN interface should be minimized [22-24]. Figure 60 shows capacitance as a function of gate voltage and frequency of the BeO capacitors. As in the baseline technology, two accumulation regions are observed: one corresponding to modulation of the AlGaN/GaN interface, and a second corresponding to accumulation of charge at the dielectric/AlGaN interface via tunneling. The second, higher bias voltage regime is the region of interest when comparing gate dielectrics. The self-contained method described above in Section 5.3 for determination of series resistance and effective oxide capacitance was also used here to correct the data collected from the capacitors. The corrected data resulted in well-behaved G_p/ω vs ω plots (Figure 61) which can be fit using the single-state trapping relation [Equation (4)] validating the use of Equation (5) for D_{it} estimation.

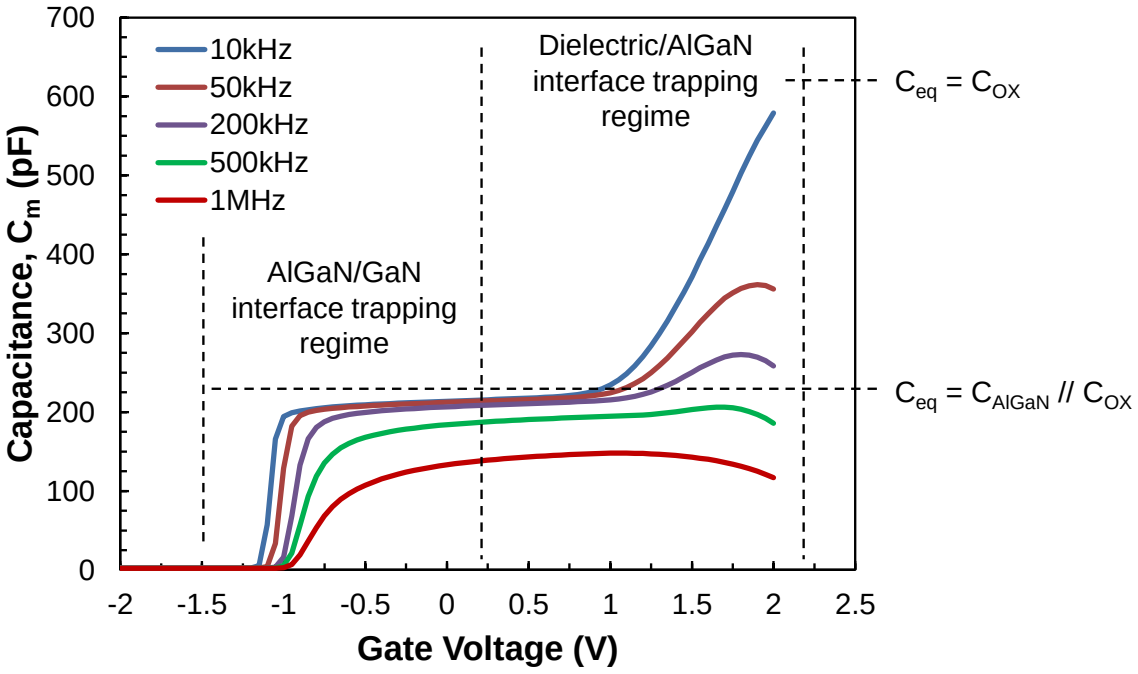

Figure 60: Capacitance as a function of gate voltage and frequency of the BeO MOS capacitors. The two trapping regimes of interest are highlighted.

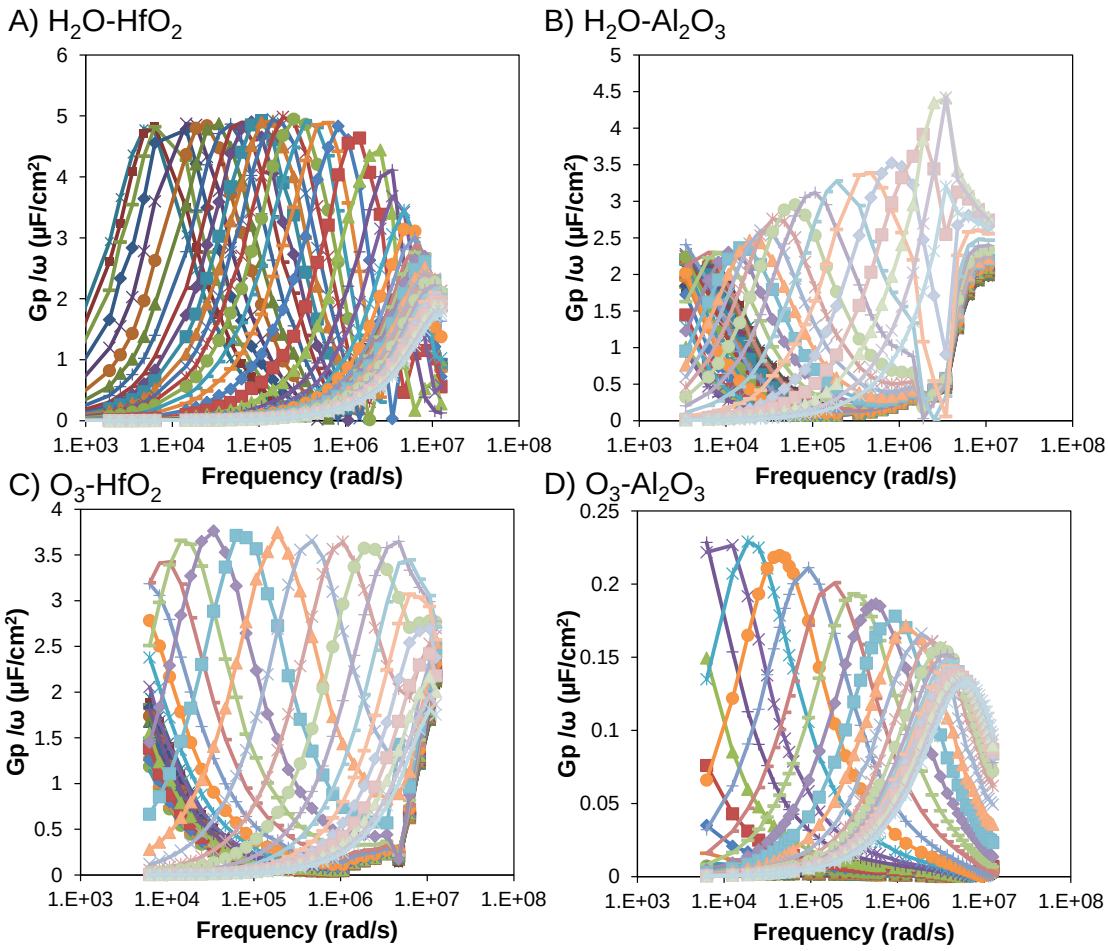

Figure 61: Normalized G_p/ω vs. ω plots for samples 1-4 as described in Table 4. Curves corresponding to gate biases in the range of 0 to 2 V are shown in each plot.

The corrected data was used to generate contour plots of the normalized parallel conductance [$2.5G_p/(\omega qA)$], which are shown in Figure 62. In the AlGaN/GaN trapping regime, a trap density of ~$3x10^{13}$ $eV^{-1}cm^{-2}$ was observed which is roughly equivalent to the AlGaN/GaN interface trapping density observed in the Schottky diodes. The slopes of the profiles are consistent with interface trapping and indicate good surface potential modulation. The O_3-Al_2O_3 manifests the lowest interface trap density (D_{it} ~$3 x10^{12}$ eV^{-}

$^{1}cm^{-2}$), with the PECVD Si_xN_y a close second. This value is similar to that previously reported using *in situ* plasma nitridation [104]. For optimum gate stack performance a bilayer dielectric is recommended: an *in situ* MOCVD Si_3N_4 or ozone-based ALD Al_2O_3 interface state passivation layer followed by ALD BeO for low gate leakage. Use of an ozone oxygen source and/or plasma enhanced ALD for BeO growth should result in decreased carbon and unincorporated oxygen content in the film, further improving performance. Additionally, for both ALD HfO_2 and Al_2O_3, the use of ozone as the oxygen source results in decreased trapping, so the use of an ozone precursor for BeO ALD is also expected to decrease interface trapping, potentially below the level of O_3-Al_2O_3 (D_{it} of H_2O-BeO is already lower than the D_{it} of H_2O-Al_2O_3).

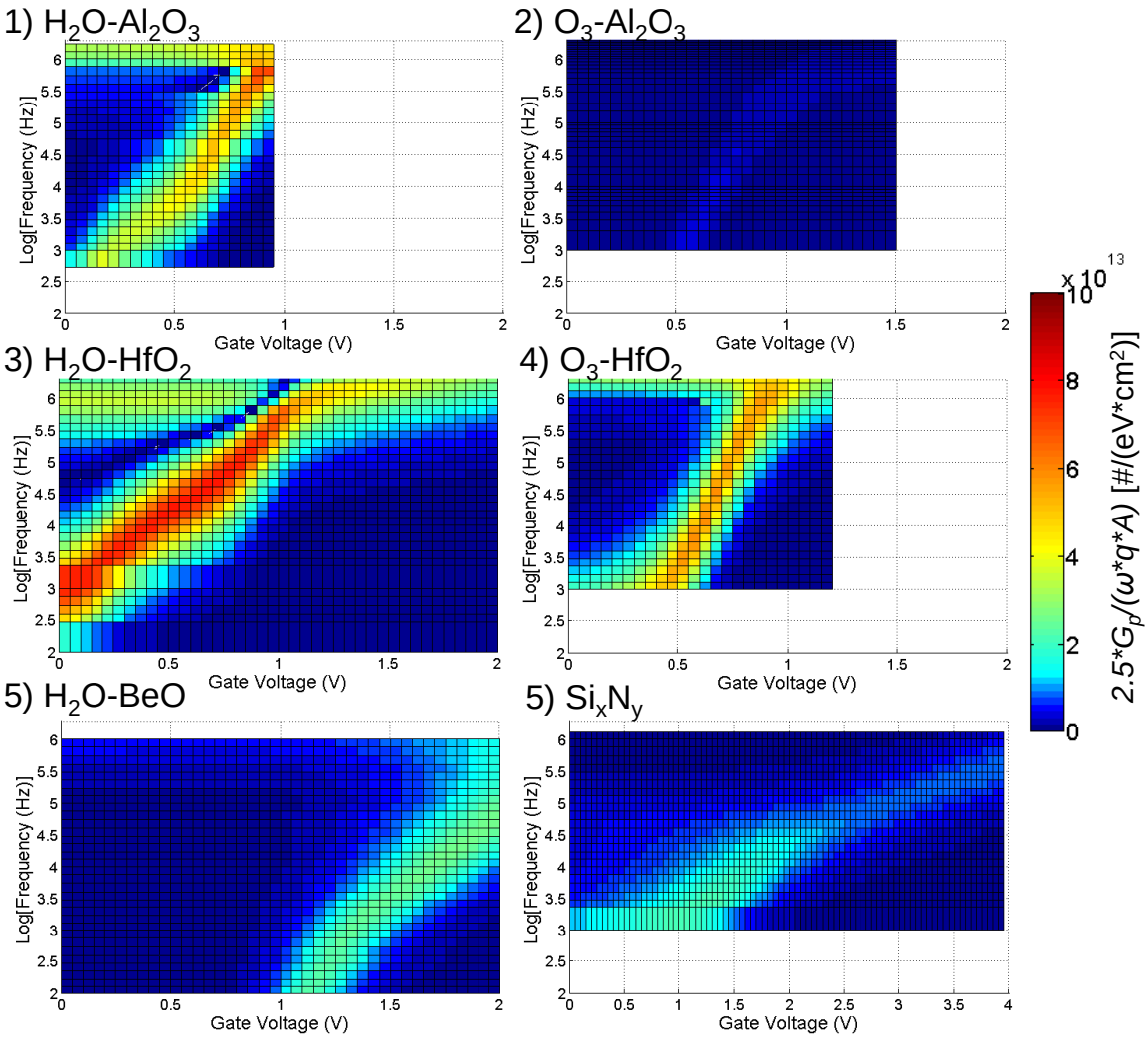

Figure 62: Contour plots of the normalized parallel conductance of the six capacitors described in Table 4. The bias region shown correlates to trapping at the dielectric/AlGaN interface.

6. SI-CMOS-LIKE ALGAN/GAN TRANSISTOR

To demonstrate the viability of the proposed self-aligned process flow and explore the challenges of its integration in CMOS-compatible AlGaN/GaN technology, three types of transistors were fabricated. First, a sample using the best surface treatment and metallization described in Section 4 was patterned using optical lithography to act as an experimental control (referred to as the "control sample"). Second, a sample was fabricated using the same process as the control sample with the sole addition of the Si_xN_y spacer process to isolate the performance impact of the spacer (referred to as the "spacer sample"). Third, a sample using the full spacer & self-aligned contact module was processed (referred to as the "self-aligned sample"). Cross-section depictions of each sample are shown in Figure 63. Due to limited access to BeO deposition, integration of the ALD BeO film into the transistor technology is left for future research. Similarly, the present transistor technology is limited to depletion mode operation. Integration of an enhancement mode scheme is not necessary to demonstrate the functionality of the self-aligned technology and is therefore deemed beyond the scope of this work.

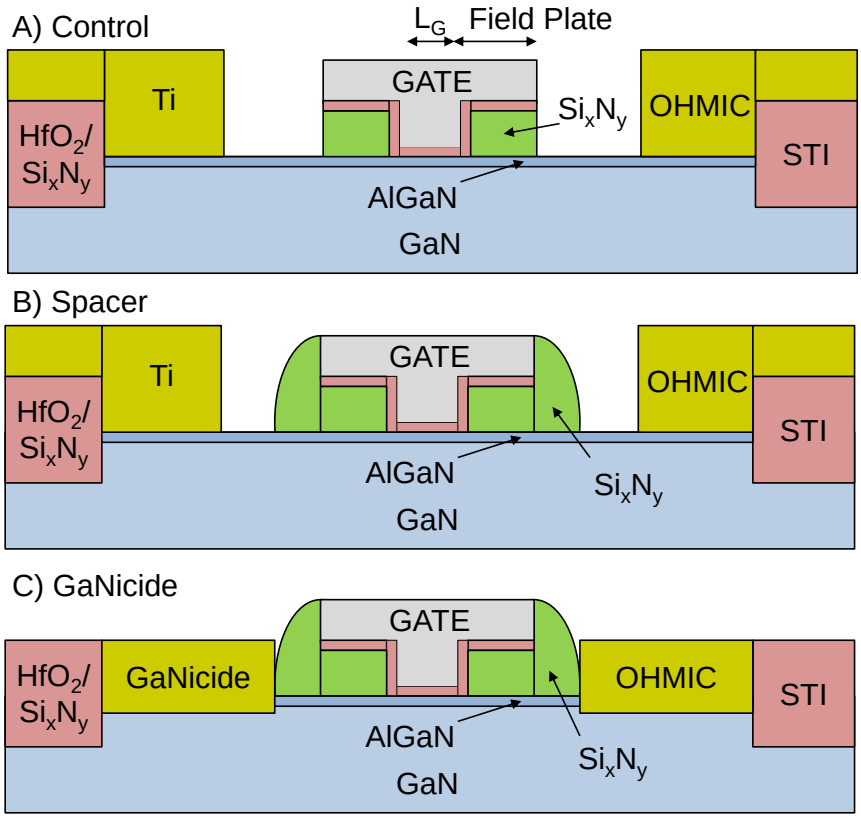

Figure 63: Cross-section cartoons detailing the three transistor samples that were fabricated.

6.1 Si-CMOS-Like Transistor Fabrication

Transistor fabrication began with processing of a shallow-trench-isolation module for inter-device isolation. Wafers were rinsed in solvent (Acetone / IPA) for hydrocarbon removal followed by a 10 minute native oxide strip in 1:10 HCl:DI-H_2O. Immediately after surface clean, the wafers were loaded into the PECVD system for passivation with 50 nm of Si_xN_y. 100 nm of Cr was deposited by electron beam evaporation, patterned, and used as a hard mask for dry etching the AlGaN/GaN trenches. As described previously, a SF_6 / Ar ICP-RIE process was used to etch the

AlGaN and GaN. After etching, the Cr hard mask was stripped using UEI CR-1A and the field isolation dielectric (100 nm Si_xN_y / 15 nm HfO_2 / 100 nm SiO_2 / 15 nm Si_xN_y) was deposited. The reverse image of the active area was then patterned, and openings were etched in the field dielectric, exposing the passivation Si_xN_y for processing of the gate module.

Processing of the gate module began by opening gate windows in the Si_xN_y passivation using BOE. 150 cycles of Al_2O_3 was deposited by ALD and annealed at 700 °C for 60 s in ambient N_2 for densification. 20 nm of TaN and 80 nm of Cr were deposited by electron beam evaporation for use as the gate metal. TaN is thermally stable and acts as a diffusion barrier. These properties should help minimize degradation of the gate dielectric during the ohmic anneal. Additionally, both TaN and Cr etch slowly in HF, so they should be able to withstand the etch of unreacted titanium. The Cr was patterned using CR-1A, then used as a hard mask to pattern the TaN and Al_2O_3. The same SF_6 TaN dry etch described in Section 5.4.1 was used for these samples. The gate stack was then used to pattern the Si_xN_y passivation layer completing the T-gate structure.

The ohmic contact module is where the processing of the three samples diverged. The spacer sample and the self-aligned sample were routed through the spacer process described in Section 4.8: 300 nm of PECVD Si_xN_y followed by a CHF_3-based plasma etch. The etch was followed by a 15 s dip in BOE to aid in cleaning up any plasma damage or Si_xN_y residue. The control and spacer samples were then patterned for metal liftoff. Immediately prior to introduction to the sputter chamber, all three samples were

rinsed in 1:10 HCl:DI-H_2O for 2 minutes and treated in Ar plasma for 30 s (as described in Section 4). 100 nm of Ti was sputtered at 250W RF power with 3 mtorr of Ar flow. The self-aligned sample was encapsulated in 50 nm of PECVD Si_xN_y, and then all samples were annealed in N_2 at 865 °C for 60 s. The Si_xN_y encapsulation and unreacted Ti were etched in 1:50 HF:DI-H_2O. Finally, Al(130 nm)/Ta(20 nm) interconnects were deposited by liftoff technique to enable device probing.

6.2 Transistor Performance

The transistor performance of the control sample is summarized in Figure 64. While large drain currents are achieved, the devices were extremely leaky leading to an I_{on}/I_{off} ratio of only ~100. From the I_D-V_G current profile in Figure 64A, we see that the 15 nm Al_2O_3 gate dielectric resulted in a threshold voltage of -3.75 V and a maximum transconductance of 149 mS/mm. The break down voltage of the self-aligned sample is expected to be poor, so low drain voltages of 5 V were used.

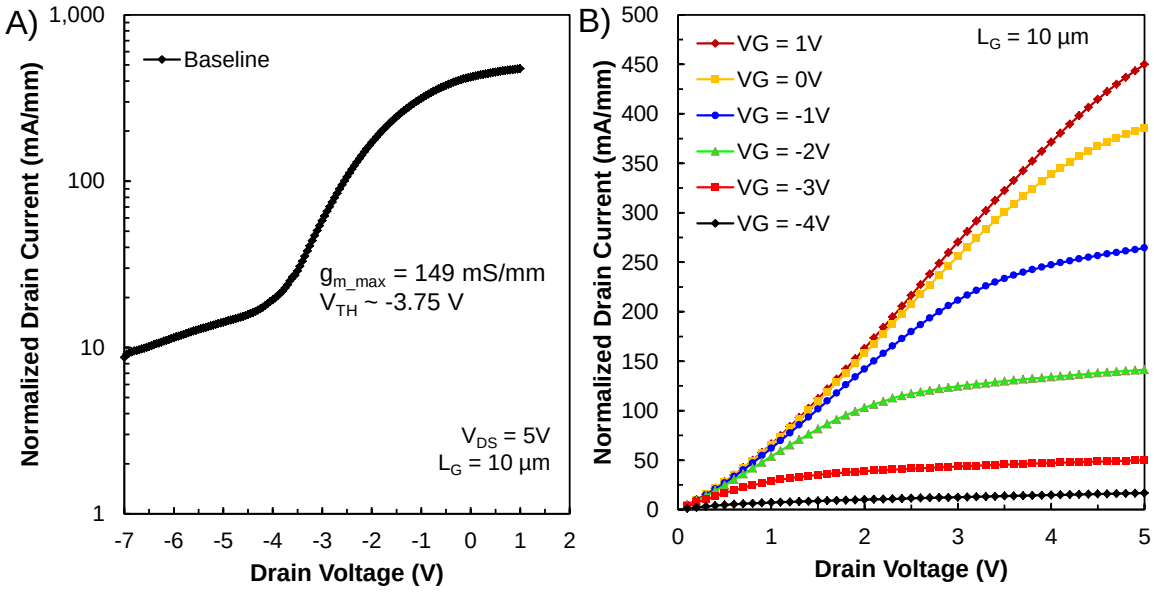

Figure 64: A) I_D-V_G current profile collected from the control sample. B) I_D-V_D current profile versus gate voltage collected from the same device as in (A).

The off-state drain leakage current shown on the right size of Figure 64A originates from two places. First, the gate dielectric provides a leakage path. Leakage current was collected by grounding the source and drain and sweeping the voltage on the transistor gate from negative to positive. As seen in Figure 65, the leakage current is comparable to the leakage observed in the Al_2O_3 capacitors of Section 5.4.2. A second leakage path is along the GaN mesa sidewalls. The delamination SiO_2 dielectric used to aid in removal of unreacted Ti was also found to lead to delamination of the gate metal at the mesa edges. Thus the gate did not overlap the active area, and the GaN sidewalls were not controlled by the gate.

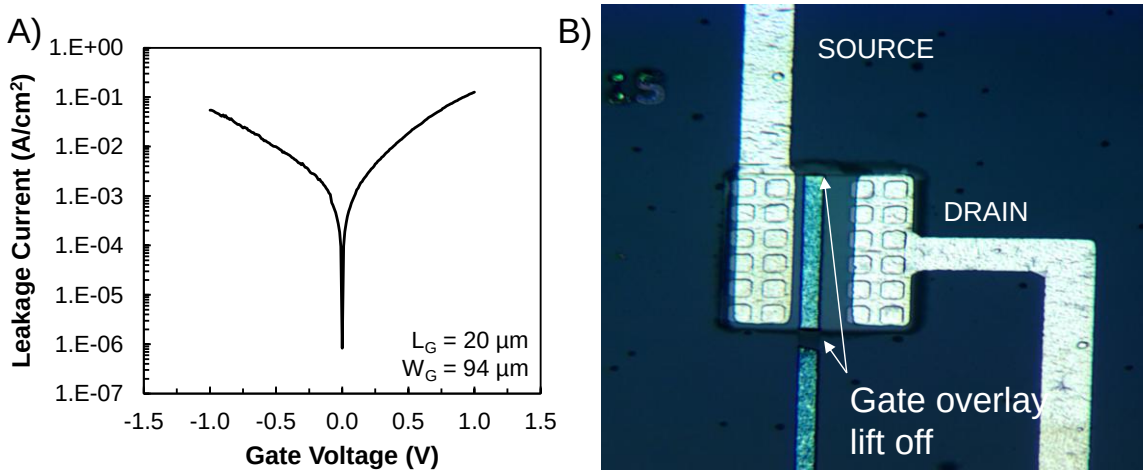

Figure 65: A) I_G-V_G current profile collected from the control sample. B) Top down optical microscope image showing gate liftoff at mesa edges.

The I_D-V_D behavior of the control and spacer samples was compared to determine the effect of the spacer process (Figure 66). Despite the post-etch BOE clean, the spacer plasma etch damages the AlGaN barrier layer leading to an increase in on resistance and a reduction in the maximum drain current at a given gate bias. However, the damage due to the CHF_3 plasma was found to aid ohmic contact formation.

Figure 67A and B show the resistance vs. TLM spacing for the self-aligned sample and a comparison of the on resistances across all three samples, respectively. The CHF_3 plasma etch resulted in reduction of the contact resistance to 0.36 Ohm*mm (an order of magnitude lower than the best resistance observed during GaNicide development in Section 4). This is an excellent value which confirms the effectiveness of the contact module for Au-free, self-aligned applications. Additionally, the self-

aligned component of the module enables extreme scaling of the source and drain access regions resulting in a 5x reduction in R_{ON} relative to the control sample (Figure 67B).

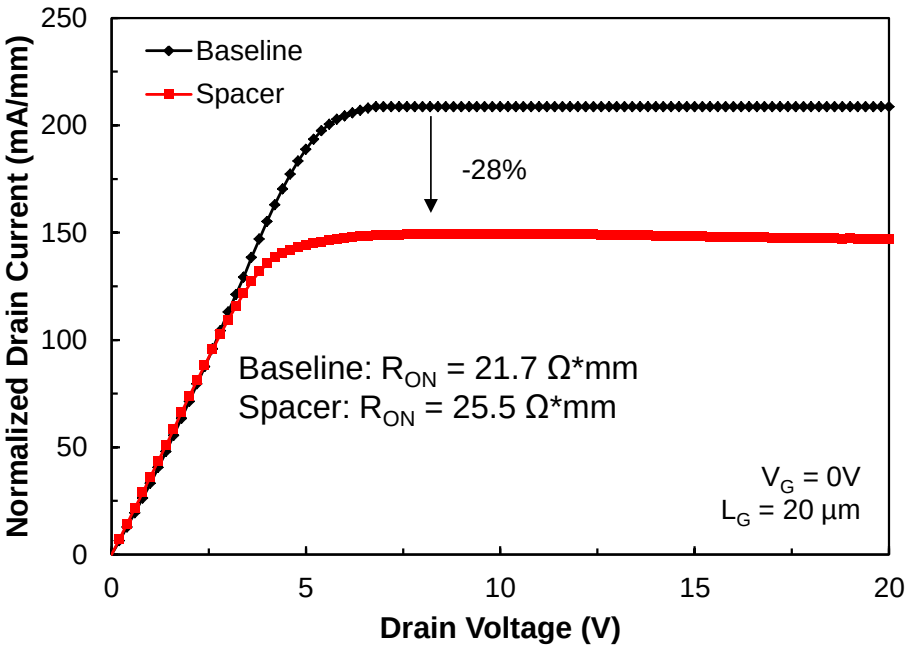

Figure 66: Comparison of I_D-V_D current profile at 0 V gate bias of control and spacer samples highlighting increased R_{ON} and reduced I_{Dmax}.

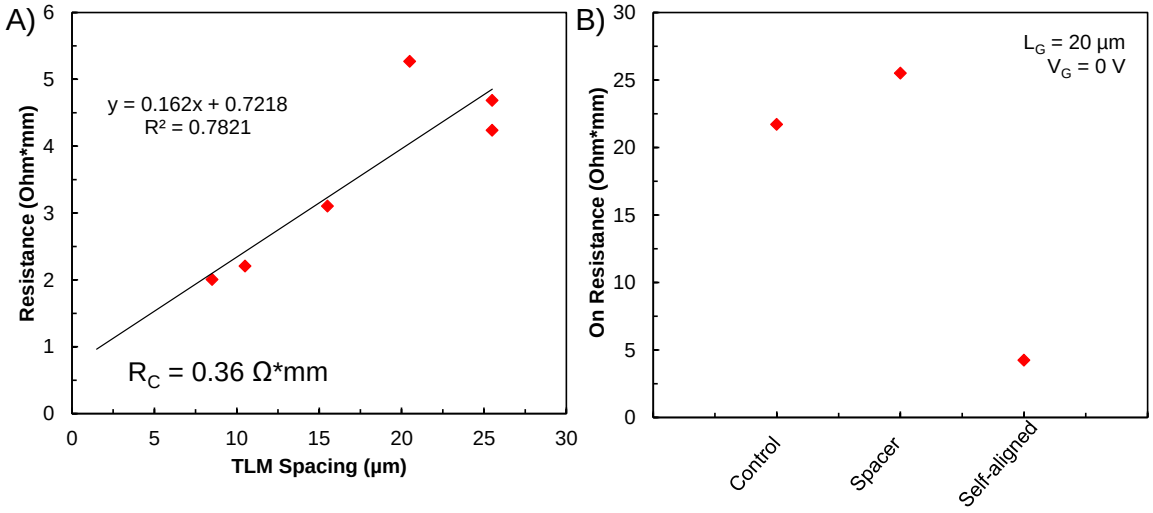

Figure 67: A) Normalized resistance vs. TLM spacing for the self-aligned transistors. B) Comparison of the on resistances of the three transistor samples.

Several problems were discovered relating to integration of the self-aligned process, which provide opportunity for future research. First, the breakdown voltage across the Si_xN_y spacers was only about 1.5 V. Since the threshold voltage was -3.75 V, this meant that the self-aligned transistors could not be turned off. The spacer needs improvement, and the gate dielectric thickness and gate-recess depth need to be optimized to tune the threshold voltage to enable switching performance. As mentioned above, a second problem was delamination of the gate stack near the edges of the active region. This issue could be addressed in the future by processing the gate module prior to deposition of the field dielectric. A third problem was intermixing of the Cr gate metal with Ti leading to removal of the gate metal in some areas during the dilute HF etch. Using thick TaN as the gate metal and removing the Cr hardmask after patterning the TaN should help limit Ti diffusion into the gate metal.

7. CONCLUSION & OUTLOOK

A self-aligned contact module has been developed and initial integration has been demonstrated. Titanium, combined with Ar and CHF_3 plasma treatments enabled a contact resistance of 0.36 Ohm*mm which is comparable to the best reported Au-free ohmic contact schemes. Additionally, the scaling of the source and drain access regions enabled by the self-aligned nature of the contact module led to a low R_{ON} of 4.24 Ohm*mm. This reduction of on resistance will lead to higher cutoff frequencies, especially when combined with extreme gate length scaling. The maximum drain current also exceeded the current achieved in the baseline technology by nearly an order of magnitude. Large on current and low on resistance were expected to be the primary benefits of a self-aligned technology, and those goals were realized with great success. In Figure 68, the performance of the self-aligned technology is compared to the baseline technology of Section 3 and a typical Au-free technology from literature.

	Goals	Baseline	Self-aligned	[12]
R_{ON} (Ohm*mm)	<5	41.3	**4.24**	9.1
R_C (Ohm*mm)	<1	**0.2**	0.36	0.65
$I_{D,max}$ (A/mm)	>0.2	0.3	**2**	0.6
V_{br} (V)	>10	>100	2	**850**
$I_{G,leak}$ (A/cm^2)	<1E-5	**1E-6**	1E-1	5E-6

Figure 68: Performance comparison of the self-aligned technology to that of the baseline technology and a typical Au-free technology from literature.

The cost-savings potential of the self-aligned process is tremendous. While the savings due to decreased R&D requirements and shallower learning curves are difficult to quantify, the processing savings are easy to estimate. The operating costs of the fab used for integration of the baseline technology (Section 3) were used to compare the baseline contact module to the self-aligned module. A minimum lot size of six wafers was assumed. Figure 69 details the cost estimates. The metal patterning lithography is removed and replaced with the additional field dielectric and spacer processes. The end result is a savings of $170 per wafer (about 1% of front end processing cost). While the spacer process enables low on resistance (leading to higher operating frequencies), many power electronics applications require large breakdown voltages. In these cases, the contact windows could still be defined by optical lithography rather than by a spacer process. The processing cost savings would increase due to removal of the spacer processing. If all of the projected GaN product incorporated this process (100,000 wafers per year by 2015 [3]) the annual savings would be ~$17 million.

Baseline Contact Module					Self-Aligned GaNicide Contact Module			
Step	**Moves ($39)**	**Engr. Time ($180)**	**Tool Time ($1000)**		**Step**	**Moves ($39)**	**Engr. Time ($180)**	**Tool Time ($1000)**
CVD - SiN Dep	6	0.5			ALD - ALD HfO2	6	0.5	
CTR - HMDS	6				CVD - SiO2/SiN Dep	6	0.5	
CTR - PR	6				CTR - HMDS	6		
ALN - Expose CON-Win	6		1		CTR - PR	6		
CTR - Develop	6				ALN - Expose Rev-Active	6		1
PET - SiN Etch	6	0.5			CTR - Develop	6		
ASH - PR Strip	6				PET - SiO2/HfO2 Etch	6	0.5	
WTS - HCl Clean	6	2			ASH - PR Strip	6		
PVD - M1 Dep	6	0.5			CVD - SiN Dep	6	0.5	
CTR - HMDS	6				PET - SiN Spacer Etch	6	0.5	
CTR - PR	6				WTS - HCl Clean	6	2	
ALN - Expose CONTACT	6		1		PVD - M1 Dep	6	0.5	
CTR - Develop	6				RTA - Ohmic Anneal	6	0.5	
PET - M1 Etch	6	1			WTS - HF Selective Etch	6	2	
ASH - PR Strip	6							
RTA - Ohmic Anneal	6	0.5						
Total	96	5	2		Total	84	7.5	1
Cost Sub-total	$3,744.00	$900.00	$2,000.00		Cost Sub-total	$3,276.00	$1,350.00	$1,000.00
Base Total Cost	**$6,644.00**				Base Total Cost	**$5,626.00**		
Cost per wafer:	$1,107.33				Cost per wafer:	$937.67	**-$169.67**	15.32%

Figure 69: Cost savings estimate due to incorporation of self-aligned contact module. Steps highlighted in red on the left are cut out of the process and replaced with the steps highlighted in green on the right.

The opportunities for future research into the proposed contact scheme consist primarily of integration optimization and yield enhancement. The breakdown voltage limitations of the narrow spacer necessitate optimization of the spacer and fine tuning and control of the threshold voltage. Additionally, over etch during spacer formation led to removal of some of the field dielectric which degraded the yield of the subsequent selective etching.

There is still room for improvement of the gate stack, as well. BeO shows great promise as a gate dielectric because the large band gap, conduction band offset to AlGaN, and thermal stability of the Be-O bond enable low-leakage performance even after high temperature anneal. However, ALD BeO is a relatively immature process.

Precursor synthesis has yet to be commercialized. Work toward decreasing the carbon and unincorporated oxygen content, either by optimization of deposition conditions or by transitioning to plasma-enhanced ALD, is required. Additionally, the use of ozone as an ALD precursor shows great promise for reducing interface trapping and should be explored in conjunction with BeO.

The future of GaN-based RF and power electronics is bright. As improvements to the manufacturing process continue, operating costs will decrease. The optimization of Si-CMOS compatible technologies will decrease the need for capital investment and enable GaN to seize additional market share from Si power electronics.

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APPENDIX A – RECIPE SUMMARY

Name	Tool	Plasma Chemistry	Pressure (mtorr)	Temp. (°C)	RF Power (W)	ICP Power (W)	Rate (nm/min)	HM?	HM Er (nm/min)
AlGaN/GaN SF_6 Etch	Oxford Plasmalab 100	40 sccm SF_6, 10 sccm Ar	44	16	200	400	15	Cr	6
Ta SF_6 Etch	Oxford Plasmalab 100	25 sccm SF_6, 10 sccm O_2	20	23	100	0	10	PR	
Si_xN_y CHF_3 Etch	Oxford Plasmalab 100	50 sccm CHF_3, 5 sccm O_2	50	20	150	0	45	PR	
TaN SF_6 Etch	Oxford Plasmalab 100	30 sccm SF_6, 30 sccm Ar	10	23	100	500	40	Cr	10
HFO_2 SF_6 Etch	Oxford Plasmalab 100	20 sccm SF_6, 10 sccm Ar	10	23	50	500	23	PR	
Si_xN_y PECVD	Oxford Plasmalab 80	125 sccm SiH_4/N_2, 700 sccm N_2	600	350	15	NA	7.5		
SiO_2 PECVD	Oxford Plasmalab 80	425 sccm SiH_4/N_2, 710 sccm N_2O	1000	350	20	NA	43		
Si_xN_y CF_4 Etch	Applied Materials Centura Super E	150 sccm CF_4	30	23	7	750	70	PR	
AlGaN Cl_2 Etch	Applied Materials Centura Super E	25 sccm Cl_2, 25 sccm Ar	20	23	50	300	80	PR	
Ta/Al/Ta Etch	Applied Materials Centura DPSII	1.) 50 sccm Cl_2, 50 sccm BCl_3 2.) 25 sccm Cl_2, 50 sccm BCl_3	10	23	75	200	240	PR	

APPENDIX B – SAMPLE CODE

B.1 DitContourGenerator.m

```
%Contour Generator
%Data file should be matrix of Dit magnitudes with measurement frequencies in row 1, and bias voltages in column 1.

RAW = importdata('SiN_Dit.txt','\t');

Y = RAW(1,:);
Y(1) = [];
Y = log10(Y);

X = RAW(:,1);
X(1) = [];
X = transpose(X);

dit = RAW;
dit(1,:) = [];
dit(:,1) = [];
dit = transpose(dit);

surf(X,Y,dit)
xlabel('Gate Voltage (V)','FontSize',18);
ylabel('Log[Frequency (Hz)]','FontSize',18);
set(gca,'FontSize',14);
%set(gca,'YScale','log');
view([0 0 1]);
caxis([0 3E13]);
xlim([0 4]);
%ylim([100 2000000]);
ylim([2 6.3]);
colorbar;
h = colorbar;
set(h, 'FontSize',14);
hFig = figure(1);
set(hFig, 'Position', [0 100 820 440]);
```