

**ANALOG FIR FILTER USED FOR RANGE-OPTIMAL PULSED RADAR
APPLICATIONS**

A Thesis

by

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ABSTRACT

Matched filter is one of the most critical block in radar applications. With different measured range and relative velocity of a target we will need different bandwidth of the matched filter to maximize the radar signal to noise ratio (SNR). Conventional matched filter designs incorporate surface acoustic wave (SAW) filters. However, it is not inherently tunable and will need multiple SAW filters with to change the bandwidth resulting in costly solutions.

In this work, a novel method of implementing the matched filter with an analog FIR filter is proposed. The FIR filter provides a linear phase response which is suitable for radar applications. Analog FIR filters can be implemented in the discrete domain, requiring operational amplifiers, switches and capacitors. In this work, the FIR filter is implemented using a highly programmable operational transconductance amplifier with tunable transconductance gain.

The operational amplifiers designed for the filter uses a fully differential source degeneration topology to increase the linearity; also capacitive degeneration was placed to compensate its high frequency response. An active continuous-time common mode feedback (CMFB) circuit is also presented. This circuit presents a much smaller load capacitance to the output of the amplifier, yielding a higher frequency response.

To satisfy system specifications a 128-tap FIR system is implemented, which require over 128 amplifiers, 136 unity capacitors of 1pF each and 4760 switches. The functionality of the proposed architecture has been verified through schematic and

behavior model simulations. In the simulation, the robustness of the FIR filter to process and temperature variation is also verified. The circuits were designed in the TowerJazz 180nm CMOS technology and fabricated on November 2013.

To my parents and sister

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1. INTRODUCTION

Nowadays wireless communication systems demand wireless receiver solutions that accommodate various standards. The advantages of digital signal processing coupled with improvements in the processing technology, encourage RF systems to be designed with more emphasis on digital processing. This is further catalyzed by the tremendous growth of semiconductor processing technology which keeps pushing the technology node down to few tens of nanometers, thereby decreasing the total area of integrated circuits and the power consumption.

Signal processing is usually performed in the digital domain due to programmability. For many purposes, one can more easily design, modify, and depend on filters using a digital signal processing (DSP) because the filter function on the DSP is software-based, flexible, and repeatable. Also, digital signal processing provide a more stable and tolerant output than analog domain [1].

However, analog implementations of signal processing functions are required owing to that many real world systems are analog in nature. Also, with proper analog signal processing before analog-to-digital converter (ADC) the performance requirements on ADC can be relaxed which is important for our application.

1.1. Radar system

Pulse-Doppler radars detect the transit time and Doppler shift of a reflected RF pulse in order to measure the range and relative velocity of a target. Typical pulsed radar designs use a superheterodyne architecture to provide frequency selectivity at an intermediate frequency (IF) before down conversion to baseband. An example receiver block diagram is shown in Figure 1 for a pulse-Doppler radar applications. Details on this application, including the sampling process are provided in [2] [3].

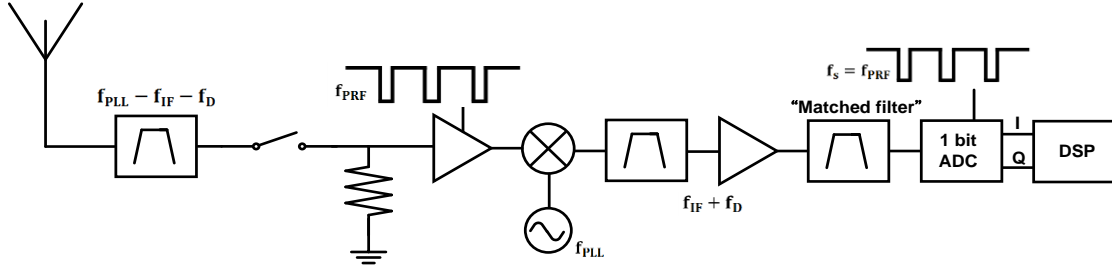


Figure 1 Block diagram illustrating a superheterodyne pulse-Doppler radar receiver

The pulsed RF signal is transmitted from the antenna to the target from which it receives a Doppler shift f_D , the return signal at $f_{PLL} - f_{IF} + f_d$ is bandpass filtered, gated through a receiver protection switch and downconverted by an image-reject mixer to $f_{IF} + f_d$. This IF signal is bandpass filtered through a radar matched filter and sampled once per pulse by a 1-bit analog-to-digital converter (ADC) clocked at the minimum possible rate $f_s = f_{PRF}$. The sampled signal passes finally to a digital signal processor (DSP) for analysis.

Consider the matched filter included in the block diagram from Figure 1. With different measured range and relative velocity of a target we will get different RF pulse width τ , the bandwidth of this filter must be equal to $1/\tau$ to maximize the SNR [2], Figure 2 illustrates this.

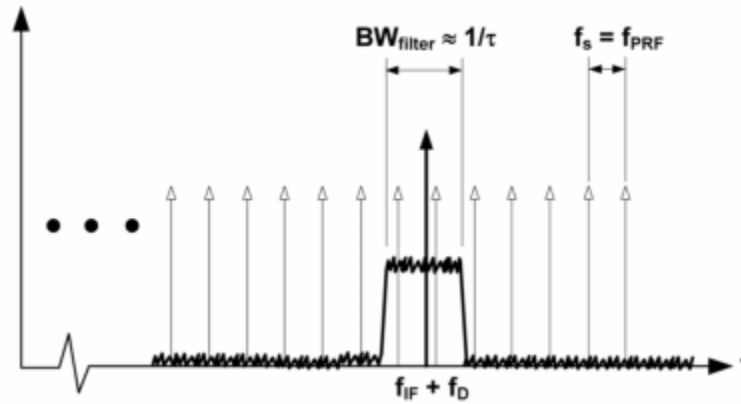


Figure 2 Subsampling the filtered IF signal

When the pulse width is very small (narrow-band pulses) most of the original signal energy is spread in broadband. To recover the signal we need to collect information well beyond signal bandwidth; for that reason we will need to use broadband filters.

To complicate this tradeoff, most pulsed radar systems have the capability to vary pulse parameters such as pulse repetition frequency (PRF) and duty cycle as the distance to the target changes. Although there are existing solutions implementing the matched filters with surface acoustic wave (SAW) filters, it also has several drawbacks of high insertion loss, not inherently tunable and high cost [4] [5]. We will need to

switch between multiple SAW filters to optimize bandwidth for a given receiver pulse width and doing so increases receiver size and complexity while only allowing for coarse tuning of the matched filter response.

1.2 Matched filter

A matched filter is a linear filter designed to detect the presence of a waveform or pulse buried in additive noise $v(t) = Ax(t - t_0) + n(t)$ where A and t_0 are unknown constants, and $n(t)$ is noise. The output of a matched filter will typically exhibit a sharp peak in response to the presence of the pulse at its input. From this peak we may determine the time location t_0 , and amplitude A of the pulse within the received waveform. The SNR of the received pulse is defined as the ratio of the peak signal power to the average noise power $SNR = \frac{\text{peak signal power}}{\text{average noise power}} = \frac{\max\{|Ax(t-t_0)|^2\}}{|n(t)|^2}$ [6] [7].

Matched filters are commonly used in radar applications. Radars transmit electromagnetic pulses which reflect off distance objects, the echoes are captured by a receiving antenna which may be very weak signals buried in additive noise, the noise can be picked up by the antenna and also created by the antenna itself and surrounding noise. Matched filters are used to process the received signal, and hence optimize the chance of detecting a target.

1.3 Analog FIR matched filters

For wireless communication receivers, more and more signal processing functions are being shifted from analog to digital domain since digital signal processing

(DSP) is more cheap, flexible and integratable. However, the lack of proper analog signal processing before analog-to-digital converter (ADC) imposes stringent performance requirements on ADC. Therefore, at least low-cost analog signal processing is necessary to reduce ADC performance requirements [8][11].

In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of finite duration. As shown in Figure 3, the output is a weighted sum of the current and a finite number of previous values of the input, the operation is described by the following equation, which defines the output sequence $y[n]$ in terms of its input sequence $x[n]$: $y[n] = b_0x[n] + b_1x[n-1] + \dots + b_Nx[n-N] = \sum_{i=0}^N b_i x[n-i]$, where b_i are the filter coefficients, N is the filter order with $N+1$ terms in the equation (N th order / $N+1$ -tap filter).

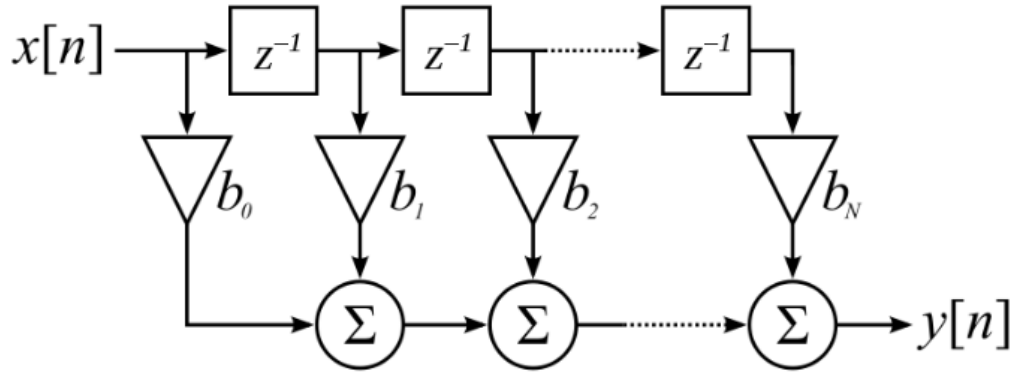


Figure 3 FIR filter in canonical realization

The main goal of the matched filter is to measure the range and relative velocity of a target, we want to keep the constant group delay of the filter small in order to

minimize the error of the detected range and velocity. A FIR filter has a number of properties that makes it attractive in modern design, requires no feedback, is inherently stable and the most important for radar applications is it can easily be designed to be linear phase/constant group delay by making the coefficient sequence symmetric [9]-[11].

1.4 Thesis organization

The main objective of this thesis is to design a single solution for the matched filter where we can change the needed bandwidth according to different detected target's range and velocity. Couple solutions of the tunable OTA was reviewed and proposed, after some analysis we chose one that was suitable, and implemented it on chip to meet the required specification for the system. The main challenge in designing the filter for this application is to design a reliable FIR filter in spite of different temperatures or process variation while having an effective tuning scheme to change the bandwidths accordingly.

Section 2 introduces FIR analog filters. The Section begins with some basic metrics such as properties, specification and operation. Macro model simulation was constructed in Matlab and Cadence to test the feasibility of the architecture. The Section concludes with a discussion on the needed coefficients for each bandwidth of the filter, an analysis for the system noise was also looked into.

Section 3 discusses some possible OTA candidates. The main parameters associated with the OTA such as output resistance, input output range, linearity and

noise etc.. are discussed along with the tradeoff in each parameter. For example, it is hard to design a low noise and high linearity OTA. There has not been many techniques discussed recently for the tunable FIR filter and we provide a possible solution to be used in radar applications. However, the proposed solution have some issues and the circuit will be adjusted in the next section.

Section 4 discusses some of the OTA issues mentioned in section 3 and came up with some circuit techniques to overcome the problem. The main parameters of the new OTA is once again analyzed and shows a large improvement for the application.

Section 5 shows the simulation result of the OTA step response. Some discussion were made to relate the step response and the FIR filter frequency response, we further improved the circuit while analyzing it's time domain response and also made a discussion for the design of the analog switches. Transistor level simulation were done in CADENCE to demonstrate the feasibility of the proposed solution.

Section 6 shows the layout of the work with a discussion on the complex clock routing, conclusions are made and the scope for future work in the thesis was discussed.

2. FUNDAMENTALS OF ANALOG FIR FILTERS

This section deals with some basic metrics such as specification, properties and operation along with some macro model simulation to test the feasibility due to process variation. A table for the needed coefficients for the filter is listed for each bandwidth and an analysis for the system noise was also discussed at the end.

2.1 FIR filter specifications

For this prototype, the main performance requirements of the filter that will be designed are:

1. IF Center Frequency – 40 MHz
2. Tunable IF bandwidth – {1, 2, 4, 6, 8, 12, 15, 20, 25, 30} MHz
3. 40-dB Rejection BW – No greater than 20 MHz more than the 3-dB BW
4. Out-of-Band Rejection – 45 dB minimum outside the 40-dB BW, over the 10 kHz to 1 GHz range
5. Group delay – Variation of no more than ± 10 ns over all bias, temperature, and bandwidth settings
6. Chip Area – 2mm x 3mm

2.2 System level architecture

Figure 4 shows the filter architecture chosen to meet the all of the bandwidth selections for the application [2]. An FIR filter approach has been chosen in order to meet the requirements of the constant group delay (linear phase response). As will be discussed later in the section, as long the total number of taps in the filter, as well as the sample rate, stay constant, the ideal group delay will remain a constant across all bandwidth selections. For the 150 MHz UWB mode, the 100 MHz notch filter and discrete time FIR filter will be bypassed and only the first stage filter will be used.

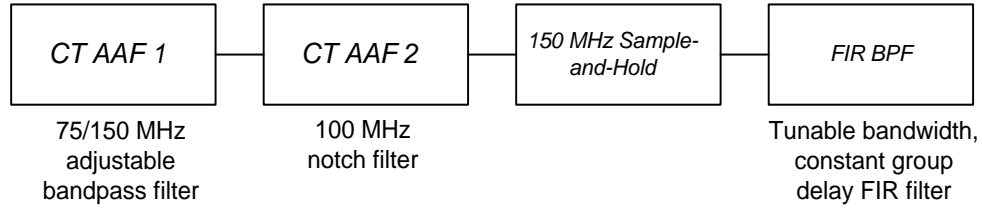


Figure 4 IF filter architecture

The overall architecture in Figure 5 is a discrete time analog FIR filter. Since we will have to convert the signal from continuous time to discrete time a sample and hold (S/H) circuit is placed before the FIR filter, with S/H circuit the input signal will have to be band limited otherwise alias issues will occur [9]. For a 150MHz S/H we will need an ideal 75MHz bandpass filter to limit the bandwidth of the incoming signals to $f_s/2$ to prevent aliasing, where f_s is the sampling frequency of the S/H.

The first block in Figure 5 is a 6th order OTA-C continuous-time anti-aliasing filter (CTAAF) with a bandwidth of 75MHz, it provides an attenuation of 50dB at

450MHz which is larger than the specification of 45dB attenuation for the out of band signals. However, the 40dB rejection bandwidth is around 240MHz and is too large for the specification (40-dB Rejection BW is no greater than 20 MHz more than the 3-dB BW). We can solve this issue by using a higher order filter but it is not desirable since the order will be too large resulting in a large area and high power solution. Instead, we cascade another 100MHz notch filter after CTAFF1 so the 40-dB rejection BW is less than 15MHz of the 3-dB BW. The first two blocks in cascade works as a continuous time anti-aliasing to meet the 40-dB rejection bandwidth and out of band rejection.

It was found that the higher the sampling rate of the filter (f_s of the S/H), the more difficult it is to obtain a small bandwidth in the bandpass filter without exponentially increasing the number of taps and therefore chip area and complexity. A sampling frequency of 150 MHz was chosen to implement the bandpass filter since it enables the designers to meet the smaller bandwidth requirements of the filter with a reasonable number of taps (32) in the FIR filter allowing the filter to meet the silicon area requirements.

One of the most important specification for the filter used in radar application is the group delay, for a variation of no more than ± 10 ns over all bias, temperature, and bandwidth settings FIR filter is a good candidate. The CTAFF group delay is around 4.5ns which leaves some margin for the FIR filter.

2.3 FIR filter characteristic

Following the sample-and-hold is the tunable FIR bandpass filter. FIR filters are discrete time in nature, thus the need for a sample-and-hold circuit at its input. An FIR filter was chosen because it can provide a linear phase response and therefore constant group delay across all frequencies. To achieve linear phase response in the FIR filter the coefficients need to be symmetric - $a_0 = a_N, a_1 = a_{N-1}, a_2 = a_{N-2} \dots$ etc. [13]. The group delay can be defined as $t_{grp} = \frac{N_{taps}}{2 \times f_s}$ [14], where t_{grp} is the group delay, N_{taps} is the number of taps for the FIR filter and f_s is the sampling frequency.

From this equation, as long as the sampling rate and number of taps remains constant, so will the group delay; however, by varying the gain of various stages in the filter, the shape of the magnitude response can be varied allowing a tunable bandwidth with constant group delay.

2.4 FIR filter operation

From [13] [14], the FIR filter we need to design for a fast roll off is a tap filter of 128 taps. There are several ways to implement this, a single 128-tap filter, 16 stages of 8-tap filter in cascade or 4 stages of 32-tap filter in cascade. We chose to implement a four 32-tap filter in cascade as shown in Figure 5, and the reasoning will be addressed in the end of the section.

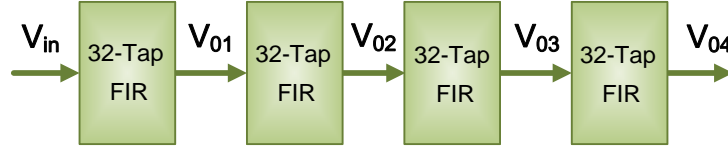


Figure 5 FIR filter architecture with four 32-tap blocks in cascade

To describe how the architecture of the analog FIR filter works, we will show an 8-tap realization to simplify the analysis, however the same concept applies to different taps of numbers. An 8-tap FIR filter equation can be expressed as

$$y[n] = a_1x[n-1] + a_2x[n-2] + \dots + a_8x[n-8] = \sum_{i=1}^8 a_i x[n-i] \quad (2.1)$$

taking the Z transform of the equation we end up with

$$Y[Z] = a_1X[Z]Z^{-1} + a_2X[Z]Z^{-2} + \dots + a_8X[Z]Z^{-8} = X[Z] \sum_{i=1}^8 a_i Z^{-i} \quad (2.2)$$

Figure 6 shows the implementation of an 8-tap FIR filter with Figure 7 showing the required clock phases needed to implement the proper operation of the filter. The S/H is running at a clock frequency of CLK=150 MHz with 50% duty cycle, each period of the clock determines the individual clock phase ϕ_i . The clock phase ϕ_i runs at a frequency of 15MHz with a 10% duty cycle. As shown in Figure 7, the period of the clock phase ϕ_i being high is 6.5ns so the clocks can be non-overlapping with a 160ps margin.

To describe the operation we look at Figure 6. The first capacitor stores the first 8 clock cycles of the current injected from $G_{mi}(OTA)$ and measured in phase 10 from

the multiplexer (MUX), the equation for the capacitor can be expressed as

$$i_{o1}(\varphi_{10}) = \sum_{i=1}^8 (g_{mi} v_{in}(\varphi_i)) \quad (2.3)$$

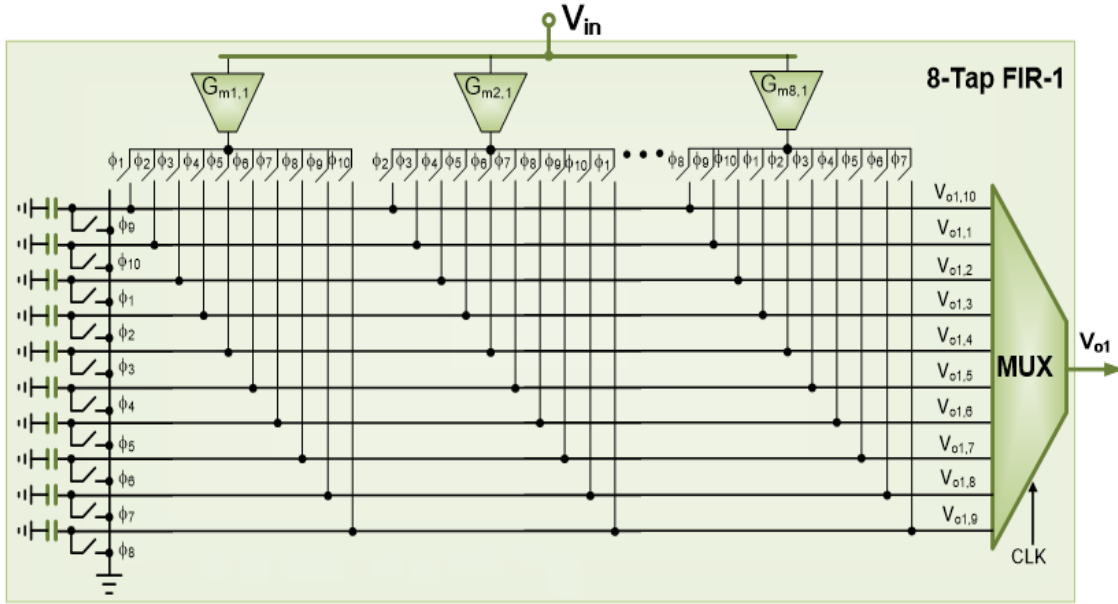


Figure 6 Conceptual block diagram of an 8-tap cell realization

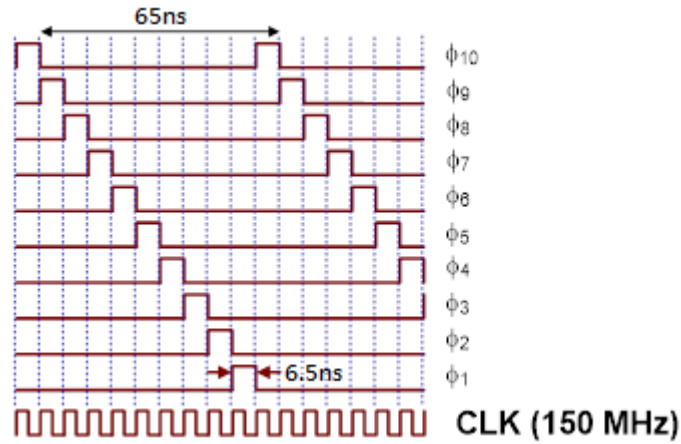


Figure 7 Clock phases required for the 8-tap filter

This current is integrated in a capacitor, since the signal is coming from a S/H, it remains constant during each clock phase, leading to the following expression for the capacitor output voltage

$$v_{o1,10}(\varphi_{10}) = \left\{ \frac{1}{C} \right\} \int_{\varphi_i=1}^8 (g_{mi} v_{in}(\varphi_i)) dt = \left\{ \frac{T_{ck}}{C} \right\} \sum_{i=1}^8 (g_{mi} v_{in}(\varphi_i)) \quad (2.4)$$

Employing the Z-transform of the discrete equation, leads to the following result

$$V_{01}(Z)|_{\varphi_{10}} = \left\{ \frac{T_{ck}}{C} \right\} \left\{ \sum_{i=1}^8 g_{mi} Z^{-i} \right\} V_{in}(Z) = \left\{ \frac{T_{ck}}{C} g_{m1} V_{in}(Z) \right\} \left\{ \sum_{i=1}^8 a_i Z^{-i} \right\} \quad (2.5)$$

Where $a_1 = 1$ and $a_2 = g_{m2-8}/g_{m1}$. The coefficients $a_i = g_{mi}/g_{m1}$ are independently adjusted by selecting the ratio of transconductances, which could be over 98% accurate. Although the first term in equation (2.5) is PVT sensitive, it affects only the filter gain, but the filter shape and group delay are insensitive to these variations. Notice that to complete the operation described in Figure 7, it is required to have 10 clock cycles; 8 clock cycles to accumulate the current components (one per clock cycle) plus an extra phase for reading and one for resetting.

Evidently, equation (2.5) resembles the typical equation of FIR architectures (2.2), with the tap coefficients being implemented using weighted transconductors. To map the equation (2.5) to (2.2) we selected $C=1p$, $T_{ck} = 150MHz$ so g_m can be within a range of tens to hundreds of uA. The coefficients and the transconductors values will be shown in tables in the next section.

By having a very high order filter, much faster roll-off in the stop band can be obtained as well as narrower bandwidths; however, implementing a single large number of taps (144) can be very difficult with the exponentially increasing number of switches, metal routing would be complex and parasitic loading would also be an issue. For 16

stages of 8 taps in cascade, it was found in Matlab that the sensitivity to PVT variations of each TAP coefficient increases with the number of cascade stages, and the transfer function is not reliable. For this design, four 32-tap filters were cascaded to provide the desired frequency response while maintaining a reasonable number of switches.

While Figure 6 shows the basic idea of how to implement an 8-tap analog FIR filter is illustrated, Figure 8 shows how the filter for this design (32-tap) is implemented. Instead of 8 transconductors there will be 32 with 34 non-overlapping clock phases used to control the switches. For this design, all four FIR filters from Figure 6 will be identical. This requires the design of 16 total transconductors due to the desired transfer function being symmetric – $G_{m1} = G_{m32}, G_{m2} = G_{m31}, G_{m3} = G_{m30} \dots$ etc. Each stage will use the same number of clock phases, so an 128 order filter is implemented with only 34 clock phases instead of the 130 that would be required if the FIR filter was designed as a single stage.

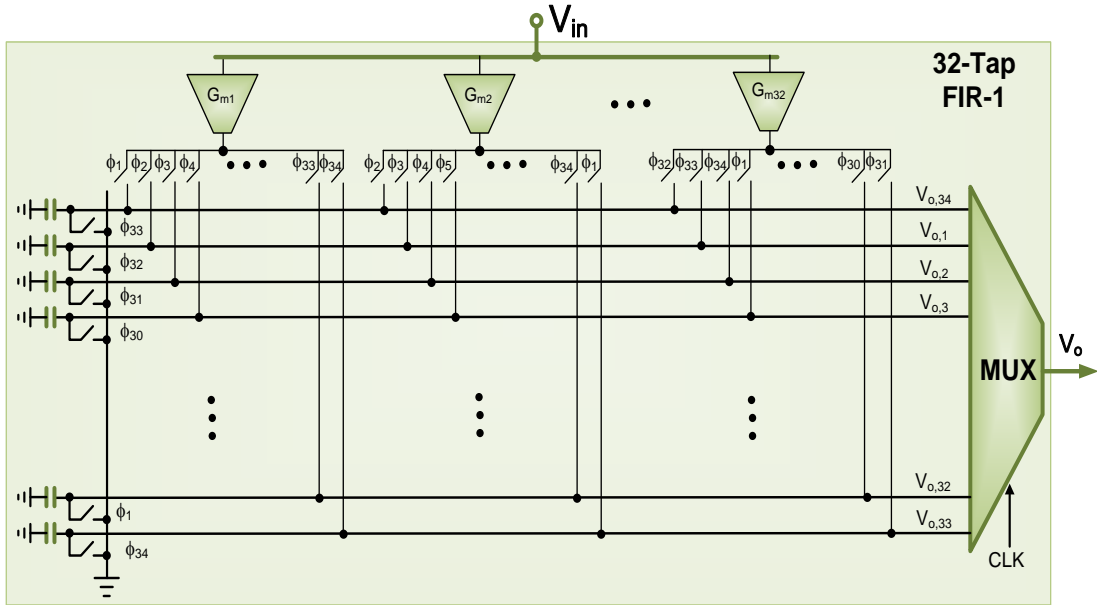


Figure 8 32-tap FIR filter implementation

2.5 FIR filter macro model simulation

Filter transfer functions were designed in MATLAB to meet the required bandwidth specifications. Figure 9 and Figure 10 are two of the transfer functions that were designed. Both transfer functions are implemented using the same clocks, only the filter coefficients are changed. Table 1 shows the coefficients needed and Table 2 shows the transconductances values that needed to be designed for the tunable transconductors in order to achieve the required bandwidth selections. Note that the smallest bandwidth column is listed as 3.5 MHz and not 1 MHz as required in the specifications. 3.5 MHz was the smallest -3 dB bandwidth that could be achieved with a 150 MHz clock. In order to decrease the bandwidth further, the number of taps in the filter must be greatly increased which will result in a large area and power increase which is not practical since the extra parasitic would be detrimental to the performance – or the clock rate

could be decreased which makes it more difficult to filter out the out-of-band interferers which become in-band signals due to aliasing.

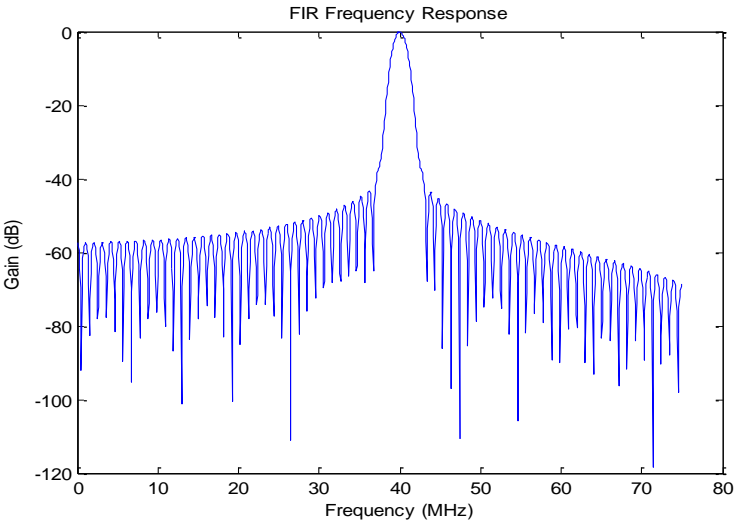


Figure 9 Frequency response for 3.5 MHz BW

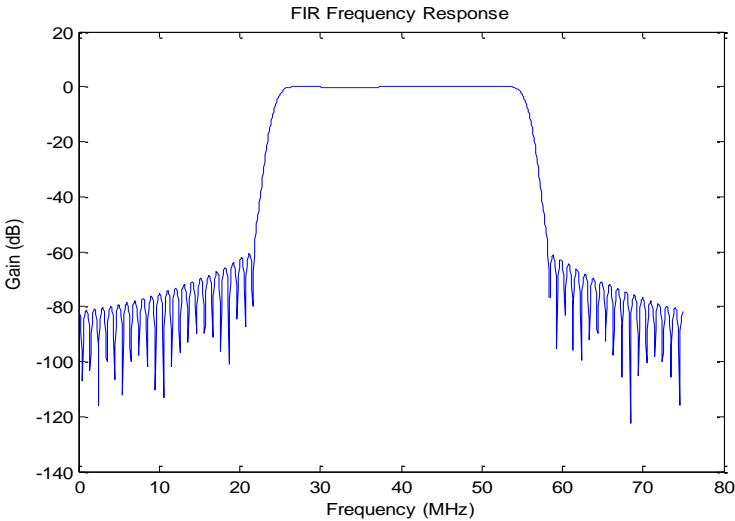


Figure 10 Frequency response for 30 MHz BW

Table 1 Coefficients values for each Gm cell and bandwidth selection

| Gm | 3.5 | 4 | 6 | 8 | 10 | 12 | 15 | 20 | 25 | 30 |
|-----------|------------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 1 | 0.64 | 0.644 | 0.623 | 0.56 | 0.68 | 0.599 | 0.62 | 0.642 | 0.61 | 0.587 |
| 2 | -0.097 | -0.226 | -0.093 | -0.130 | 0.5893 | -0.044 | -0.101 | 0.0755 | -0.092 | 0.0544 |
| 3 | -1.242 | -4.861 | -1.127 | -1.96 | 16.818 | 0.2385 | -1.040 | 3.123 | -0.527 | 2.272 |
| 4 | 0.5333 | 2.929 | 0.379 | 0.896 | -10.33 | -0.484 | 0.168 | -1.808 | -0.244 | -1.005 |
| 5 | 2.082 | 14.911 | 0.854 | 3.210 | -47.14 | -3.205 | -0.834 | -6.072 | -2.571 | -0.991 |
| 6 | -1.474 | -13.03 | 0.000 | -1.68 | 32.572 | 2.832 | 1.669 | 1.4954 | 2.101 | -2.235 |
| 7 | -3.005 | -31.48 | 1.1506 | -1.474 | 51.476 | 5.776 | 5.003 | -5.332 | 2.413 | -8.575 |
| 8 | 3.060 | 36.934 | -3.278 | -1.250 | -22.93 | -4.422 | -5.466 | 13.576 | 1.427 | 6.4806 |
| 9 | 3.673 | 49.906 | -6.196 | -5.506 | 23.46 | -1.724 | -4.971 | 21.208 | 6.649 | -2.080 |
| 10 | 5.203 | 77.938 | 12.042 | 14.130 | -12.27 | -4.956 | 1.6580 | -24.87 | -12.78 | 19.110 |
| 11 | -3.677 | -59.63 | 10.740 | 14.597 | -15.70 | -9.903 | -4.565 | -3.761 | -6.490 | 17.851 |
| 12 | 7.5037 | 129.50 | 26.038 | 38.733 | 46.455 | 34.220 | 23.494 | 38.542 | -3.527 | -16.98 |
| 13 | 2.7640 | 50.048 | -10.88 | -17.17 | 21.952 | 17.522 | 14.027 | -34.78 | -10.65 | 11.664 |
| 14 | 9.3031 | 174.13 | 39.897 | 46.685 | 86.876 | 72.590 | 62.861 | 18.317 | 69.651 | 117.53 |
| 15 | -1.029 | -19.68 | 4.650 | 7.784 | -105.6 | -9.039 | -8.146 | 25.57 | 10.590 | -20.33 |
| 16 | 9.984 | 191.96 | 45.789 | 77.09 | 105.3 | 90.908 | 82.929 | 26.62 | 112.97 | 224.55 |

Table 2 Transconductance values in $\mu\text{A/V}$ for each Gm cell and bandwidth selection

| Gm | 3.5 | 4 | 6 | 8 | 10 | 12 | 15 | 20 | 25 | 30 |
|-----------|------------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 1 | 1.380 | 0.091 | 0.484 | 0.300 | 0.030 | 0.339 | 0.442 | 0.170 | 0.442 | 0.248 |
| 2 | -0.210 | -0.032 | -0.073 | -0.070 | 0.026 | -0.025 | -0.072 | 0.020 | -0.067 | 0.023 |
| 3 | -2.680 | -0.687 | -0.876 | -1.050 | 0.742 | 0.135 | -0.742 | 0.827 | -0.382 | 0.960 |
| 4 | 1.150 | 0.414 | 0.295 | 0.480 | -0.456 | -0.274 | 0.120 | -0.479 | -0.177 | -0.425 |
| 5 | 4.490 | 2.107 | 0.663 | 1.720 | -2.080 | -1.814 | -0.595 | -1.608 | -1.863 | -0.419 |
| 6 | -3.180 | -1.837 | 0.000 | -0.900 | 1.437 | 1.603 | 1.190 | 0.396 | 1.523 | -0.993 |
| 7 | -6.480 | -4.449 | 1.170 | -0.790 | 2.271 | 3.269 | 3.567 | -1.412 | 1.749 | -3.623 |
| 8 | 6.600 | 5.219 | -2.548 | -0.670 | -1.012 | -2.503 | -3.897 | 3.595 | 1.034 | 2.738 |
| 9 | 7.920 | 7.052 | -4.814 | -2.950 | 1.035 | -0.976 | -3.544 | 5.616 | 4.818 | -0.879 |
| 10 | 11.220 | 11.013 | 9.356 | 7.570 | -5.417 | -2.805 | 1.182 | -6.586 | -9.266 | 8.074 |
| 11 | -7.930 | -8.426 | 8.344 | 7.820 | -6.928 | -5.605 | -3.255 | -0.996 | -4.703 | 7.542 |
| 12 | 16.180 | 18.299 | 20.229 | 20.750 | 20.495 | 19.367 | 16.749 | 10.206 | -2.556 | -7.176 |
| 13 | 5.960 | 7.072 | -8.453 | -9.200 | 9.685 | 9.917 | 10.000 | -9.210 | -7.720 | 4.928 |
| 14 | 20.060 | 24.606 | 30.996 | 25.010 | 38.328 | 41.082 | 44.814 | 48.505 | 50.469 | 49.657 |
| 15 | -2.220 | -2.782 | 3.613 | 4.170 | -4.659 | -5.116 | -5.808 | 6.772 | 7.674 | -8.592 |
| 16 | 21.530 | 27.125 | 35.569 | 41.300 | 46.498 | 51.449 | 59.121 | 70.491 | 81.860 | 94.870 |

In real implementation the FIR filter coefficients will have mismatches due to process or temperature variation that deviates with its ideal value, however the system architecture is reliable to coefficient mismatch less than 10% from the Matlab simulations.

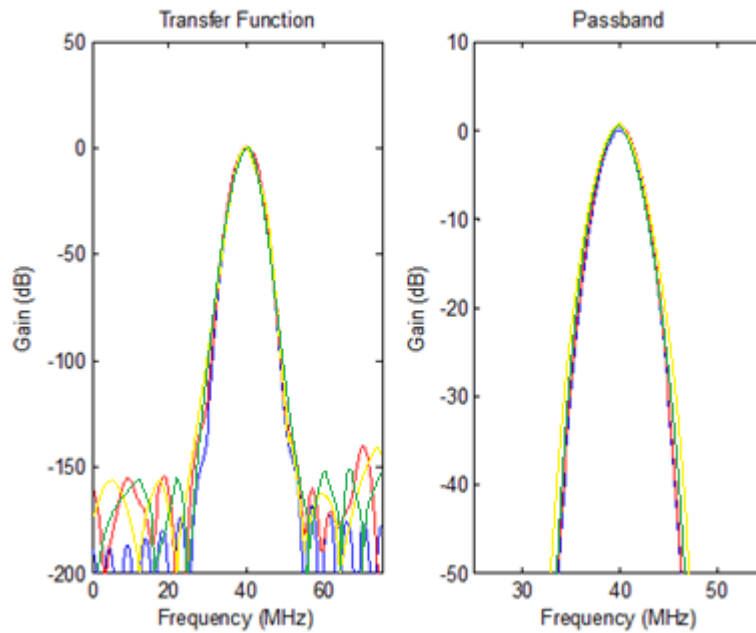


Figure 11 Frequency response due to coefficient mismatch

As shown in Figure 11, the left side shows the whole filter response centered at 40M HZ. The blue lines are the ideal coefficients from the previous table and the other lines are a random mismatch of 10% errors on the coefficients. There is a little difference in the transfer function and we will zoom into the pass band as shown in the right side figure. With several iterations, the coefficients error within 10% does not make much difference in the pass band (largest around 0.5dB to 1dB difference), this

architecture is quite robust for process or temperature variation that can cause mismatch for the coefficients.

2.6 Thermal noise issues

For the sake of noise analysis, let us consider the simplify version of the FIR filter as depicted in Figure 12. The output voltage can be expressed as

$$v_0(Z) = R_L v_{in}(Z) \sum_{k=0}^N g_{mk} Z^{-k} = R_L g_{m0} v_{in}(Z) \sum_{k=0}^N \frac{g_{mk}}{g_{m0}} Z^{-k} = R_L g_{m0} v_{in}(Z) \sum_{k=0}^N C_k Z^{-k} \quad (2.6)$$

Where C_k are the FIR filter's coefficients and g_{m0} is the transconductance of the first transconductor. For a unity passband gain filter, it is expected that all current components will have an overall effect such that

$$R_L g_{m0} \sum_{k=0}^N C_k Z^{-k} = 1 \quad (2.7)$$

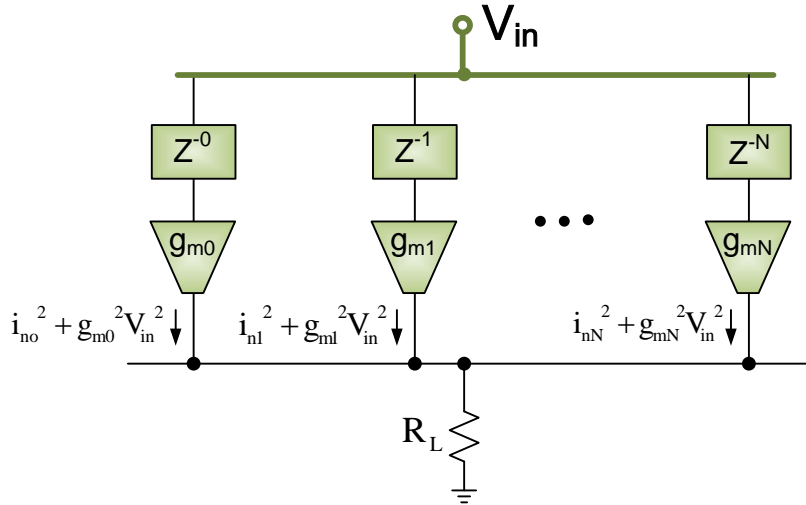


Figure 12 Small signal model for noise computation

Assuming that the noise contribution of the Z^{-i} delay element and the transconductance element are measured at the output, then it follows from Figure 12 that

$$i_{nT}^2 = 4kT\gamma g_{m0} \sum_{k=0}^N |C_k| \quad (2.8)$$

Where γ stands for the noise contributions of the additional transistors used for the realization of the transconductance and delay cells; its value is usually in the range of 1.5-3. The signal to noise ratio can be obtained

$$SNR = \frac{\{g_{m0} v_{in-RMS} \sum_{k=0}^N C_k Z^{-k}\}^2}{\int_{BW} 4kT\gamma g_{m0} \sum_{k=0}^N |C_k| df} = \left\{ \frac{\{\sum_{k=0}^N C_k Z^{-k}\}^2}{\sum_{k=0}^N |C_k|} \right\} \left\{ \frac{v_{in-RMS}^2}{\frac{4kT\gamma}{g_{m0}} BW} \right\} = \left\{ \frac{\{\sum_{k=0}^N C_k Z^{-k}\}^2}{\sum_{k=0}^N |C_k|} \right\} \{SNR_{g_{m0}}\} \quad (2.9)$$

The first factor in this expression is a result of the noise contribution due to all FIR coefficients normalized to the noise generated by the first g_m cell the last term is the SNR of the first transconductor; evidently g_{m0} must be set according to noise level considerations. Evidently, the SNR of the basic transconductance cell must be designed to satisfy our basic filter requirements.

For a classic continuous-time system, the integrated noise of a gm cell is determined by the value of the transconductance as well as the system bandwidth. The input referred noise density of the first transconductor can be computed as

$$v_{n0}^2 = \frac{4kT\gamma}{g_{m0}} = (80 \times 10^{-20}) \left(\frac{20 \gamma}{g_{m0} (mA/V)} \right) \quad (2.10)$$

Where 80×10^{-20} (V^2/Hz) corresponds to the noise density level of a 50 ohm resistor.

Therefore, the noise figure of the first g_m cell becomes

$$NF = 10 \log_{10} \left(\frac{20 \gamma}{g_{m0} (mA/V)} \right) \quad (2.11)$$

For $\gamma = 1$ and $g_{m0} = 0.1mA/V$, NF corresponds to approximately 23dB.

Therefore, in a first approximation, NF around 25dB should be expected for the entire FIR solution. Evidently thermal noise effects can be reduced at the expense of higher transconductance which results in more power consumption and a bulkier solution.

However, there is the switching effect that may increase noise level. Switching transients in digital MOS circuits can perturb analog circuits integrated on the same die by means of coupling through the substrate [15][16][17]. Various approaches to reducing substrate crosstalk are the use of physical separation of analog and digital circuits, guard rings, and a low-inductance substrate bias. In mixed-signal systems, fast switching transients produced in the digital circuits can couple into sensitive analog components, thereby limiting the analog precision that can be achieved. As a result of the demands for higher clock rates and greater analog precision that accompany progress in the underlying semiconductor technology, switching noise is an increasingly serious concern in the design of mixed-signal integrated circuits. Typical switching effect can increase noise level by 2-3dB.

3. OTA DESIGN ISSUES

In this section we discuss some possible OTA solutions. The main parameters associated with the OTA such as output resistance, input output range, linearity and noise are discussed along with the tradeoff for each parameter. For example, it is hard to design a low noise and high linearity OTA. There has not been many techniques discussed for the tunable FIR filter and we provide a possible solution to be used in radar applications. However, the proposed solution have some issues and the circuit will be adjusted in section 4.

3.1 Output resistance of the OTA

The main purpose of the OTA is to pump current into the fixed capacitor with the ability to tune the needed current to get the corresponding transconductance values for the FIR filter. Figure 13 illustrates the operation of the OTA.

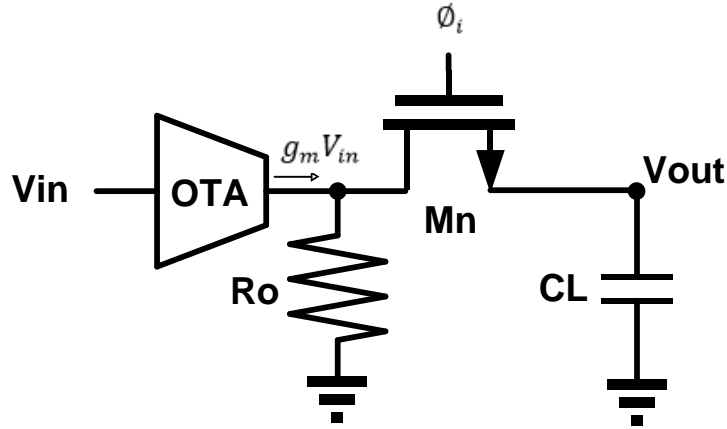


Figure 13 Model for output resistance calculation

Assuming M_N has negligible resistance when on, and assuming zero initial conditions in the capacitor. For an infinite R_o ,

$$V_{out}(t) = \frac{g_m}{C_L} t \quad (3.1)$$

If the output impedance is not large enough there will be current loss and the output voltage becomes

$$V_{out}(s) = g_m \frac{R_o}{1+sR_oC_L} V_{in}(s) \quad (3.2)$$

For an input voltage step $V_{in}(s) = \frac{1}{s}$, then

$$V_{out}(s) = g_m \frac{R_o}{s(1+sR_oC_L)} = g_m R_o \left(\frac{1}{s} - \frac{1}{s + \frac{1}{R_oC_L}} \right), \quad (3.3)$$

taking the inverse Fourier transform we get

$$V_{out}(t) = g_m R_o (1 - e^{-t/R_oC_L}) \quad (3.4)$$

For a 1% charging error in a 6.5ns time frame between equation 3.1 and 3.4, the time constant $R_o C_L$ needs to be larger than 650ns. With $C_L = 1\text{p}$, R_o needs to be larger than 650k Ohms. Figure 14 illustrates this effect.

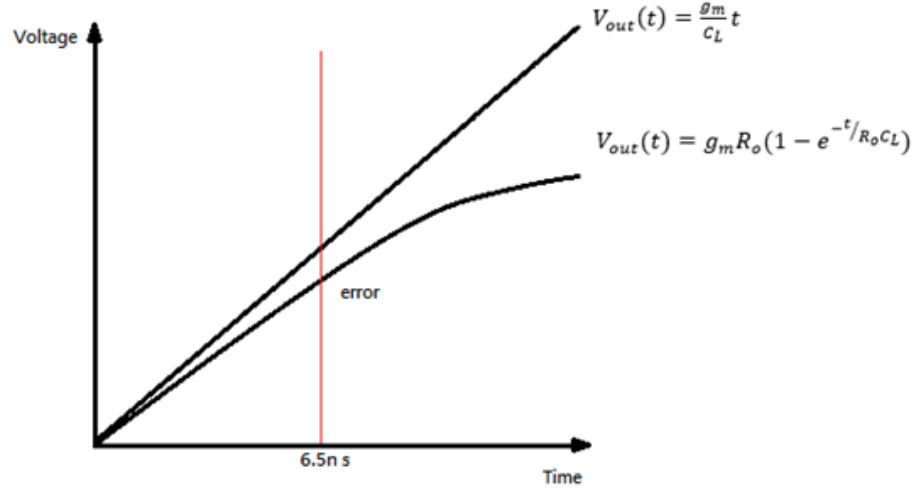


Figure 14 Transient response with finite output resistance

3.2 Specification of the OTA

The specification of the OTA is as shown in Table 3.

Table 3 Specification for the OTA

| Specification | Value |
|-----------------------------|---------|
| VDD | 1.8 V |
| Overall current consumption | <3 mA |
| IIP3 | >15 dBm |

Table 3 Continued

| Specification | Value |
|-------------------------|------------------------------|
| Noise density (NF<25db) | $< 12.8 \text{ nV/HZ}^{1/2}$ |
| Output resistance | $>650\text{k Ohms}$ |
| Overall Gm | $100\mu\text{A/V}$ |

The power was chosen to be less than 6mW per stage, hence we chosen the current consumption to be less than $6 \div 1.8 \approx 3\text{mA}$ per OTA. IIP3 was chosen to be larger than 15dBm according to the system implemented in [4], since the matched filter is in a relatively latter stage the linearity is important. The noise density was calculated in a first order approximation in equation (2.11) where only the input transconductor is calculated, which might be larger in real implementation.

3.3 Gilbert cell based OTA

Gilbert cell is usually known for its mixing properties, however it is not needed for our application. However, it is able to change the transconductance with varying an input voltage signal and we may find it applicable for our application. The realization of the gilbert cell based OTA is as shown in Figure 15.

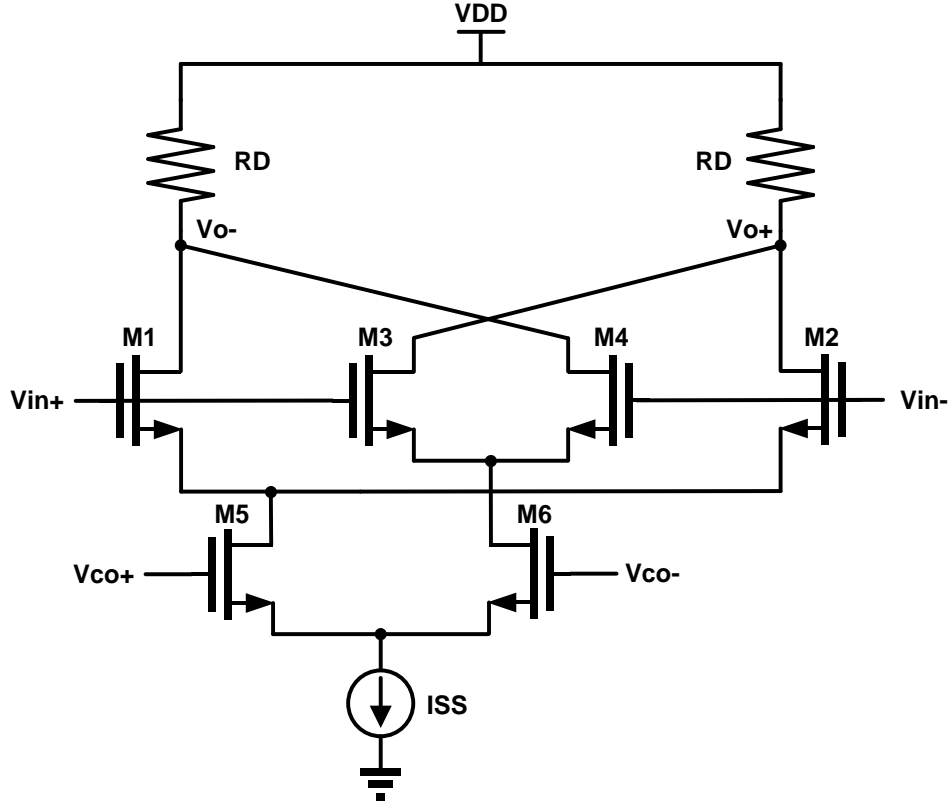


Figure 15 Gilbert cell based OTA

The circuit consists of two differential pair (M1:M2, M3:M4) with its tail current controlled by the gate voltage of M5, M6 (V_{co}). For $M1=M3$ and $M2=M4$, the transconductance of the structure can be calculated by shorting the outputs to ground while measuring the current, $G_m = g_{m1} - g_{m2}$. In order to tune the G_m we can vary V_{co} to tune the tail current for the differential pair $g_m = \sqrt{2u_n C_{ox} I_d \frac{W}{L}}$, where u_n is the mobility of electrons, C_{ox} is the gate oxide capacitance per unit area, I_d is the current flowing through M1, M3 and $\frac{W}{L}$ is the ratio size of M1, M3. The output resistance is resistive

termination R_D and will need to be modified to a current source load to provide high output impedance.

3.3.1 Sensitivity

Sensitivity is a measure of the change in system performance due to a change in the nominal value of a certain element.

$$S_x^y = \frac{x}{y} \frac{\partial y}{\partial x} \quad (3.5)$$

Normalized variations at the output are determined by the sensitivity function and the normalized variations of the parameter

$$S_x^y \approx \frac{x}{y} \frac{\Delta y}{\Delta x} \text{ or } \frac{\Delta y}{y} = S_x^y \frac{\Delta x}{x} \quad (3.6)$$

Usually, process variation and temperature changes can affect the transconductance, with sensitivity analysis we can identify most critical elements.

Calculating the sensitivity of G_m with respect to g_{m1}

$$S_{g_{m1}}^{G_m} = \frac{dG_m}{dg_{m1}} \times \frac{g_{m1}}{g_{m1} - g_{m2}} = \frac{g_{m1}}{g_{m1} - g_{m2}} = \frac{1}{1 - \frac{g_{m2}}{g_{m1}}} \quad (3.7)$$

For a low G_m , $g_{m1} \approx g_{m2}$ which will result in a large sensitivity. For example, for $G_m = 5u$, $g_{m1} = 100u$, $g_{m2} = 105u$, $S_{g_{m1}}^{G_m} = 20$, which is quite large. Figure 16 shows the sensitivity plot of the Gilbert cell

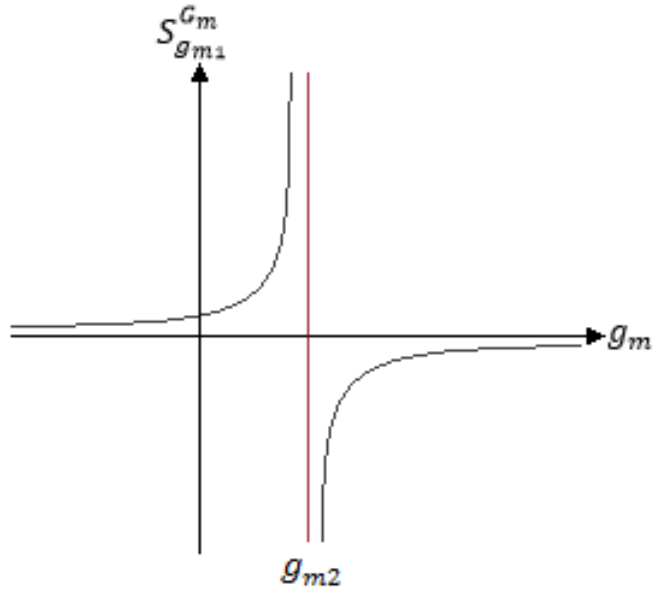


Figure 16 Sensitivity plot of the Gilbert cell

Although for $G_m = 0$, we can just omit the OTA, this characteristic is not good in our application since with temperature and process variation we may not be able to achieve the desirable low G_m due to its high sensitivity.

3.3.2 Voltage headroom

Another drawback of the topology is the need of a large voltage headroom which is not available with a low supply voltage (1V~1.8V). As with a cascade structure, the gilbert cell consumes a greater voltage headroom than a simple differential pair does. In order for the transistor to work in saturation region, it is necessary that $V_{CM,in} >$

$V_{CM,co} + V_{GS1} - V_{TH5} \approx V_{CM,co} + V_{OV}$, where $V_{CM,co}$ and $V_{CM,in}$ are the common mode

voltages of the two inputs of gilbert cell. This equation shows the difference between these common mode voltages, roughly should be larger than an overdrive voltage. [18]

3.3.3 Linearity

The analysis for the linearity of the OTA is in appendix A,

$$HD3 = \frac{A_{HD3}}{A_F} \approx \frac{V_m^2}{32(V_{GS} - V_{TH})^2} \quad (3.8)$$

The equation can conclude that by tuning the tail current we will also change the overdrive voltage which eventually changes the HD3 which is not desirable!

To overcome the sensitivity and linearity problems in the Gilbert cell, we need to change the operation of the OTA current from cancelation to splitting.

3.4 Existing solutions for source degeneration and current mirror tuning

Since most current communication systems are mixed-signal systems, digitally controllable variable gain amplifier (VGA) are preferred in order to simplify the interface to the digital core and take advantage of digital signal processing (DSP) circuitry [19]. A popular amplifier structure used in many digitally controlled VGA circuits is the fully differential source degenerated amplifier topology [20]. The source degeneration technique that presented in [21] provides a relatively constant bandwidth for the entire gain range.

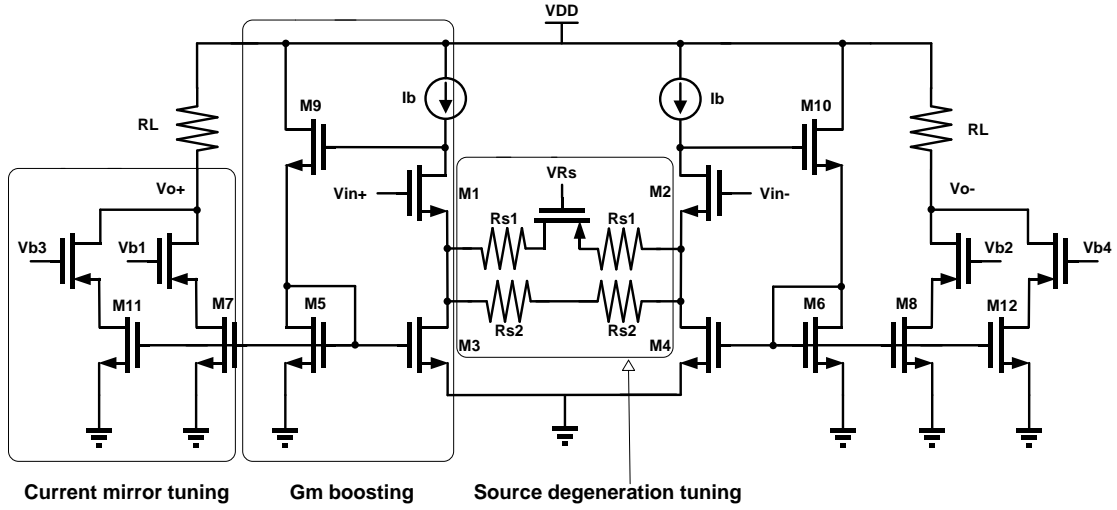


Figure 17 source degeneration and current mirror tuning

Figure 17 shows the circuit schematic of a differential gain block with source degeneration that is adopted for existing solutions for the VGA. In this configuration, gm-boosting circuitry is used to increase the gain and enhance the performance of the VGA [21]. The gm-boosting circuitry is used to minimize the dependence of the gain of the circuit on the gm of the input transistors. The use of this circuitry results in an increase in the effective transconductance of the differential pair and consequently provides higher gain while minimizing the gain error caused by variations in gm. This enhancement also makes the system more linear. Since the input transistors are biased using current sources I_b (Figure 17), the dc value of the gate-source voltage of the input transistors, along with their bias currents, is roughly independent of the input voltage. The gain of the overall circuit is given by [20]

$$A_v = N \frac{R_L}{\frac{R_s}{2}}$$

where N is the size ratio of transistors M3 to M7, R_s is the source degeneration resistor and R_L is the load resistor. The gain can be adjusted by changing N or the resistor values R_s and R_L . The method of gain tuning by changing the current mirror ratio is also presented in [20], where a differential amplifier with constant source-degeneration resistor utilizes an array of current mirrors. This technique provides a high gain range and a moderate gain accuracy.

However, for high-frequency applications, the large capacitance resulting from the array of current mirrors limits the bandwidth of the VGA. The gain can also be controlled by changing the value of resistors. To achieve a constant bandwidth for the entire gain range, only the source-degeneration resistor R_s should be changed. A digital realization of this topology is presented in [21], where a constant bandwidth of 15 MHz is reported. However, the gain range that results from changing this resistor is limited.

To sum up, this topology shows a possible candidate for the application, however the tradeoff for the tuning scheme is undesirable for our application. Tuning the source degeneration resistor for different transconductance will result in different linearity and tuning the current mirror with large ratios will result in a low speed application.

3.5 Tunable OTA

In this section, we came up with an OTA topology that will meet the specifications required for the radar application. Emphasis was put on the linearity since we do not want it to change while tuning different filter bandwidths. A lot of the analysis on linearity is based on [22][23].

3.5.1 Concept explanation of tunable transconductance OTA

The concept of the tunable OTA by current splitting is shown in Figure 18.

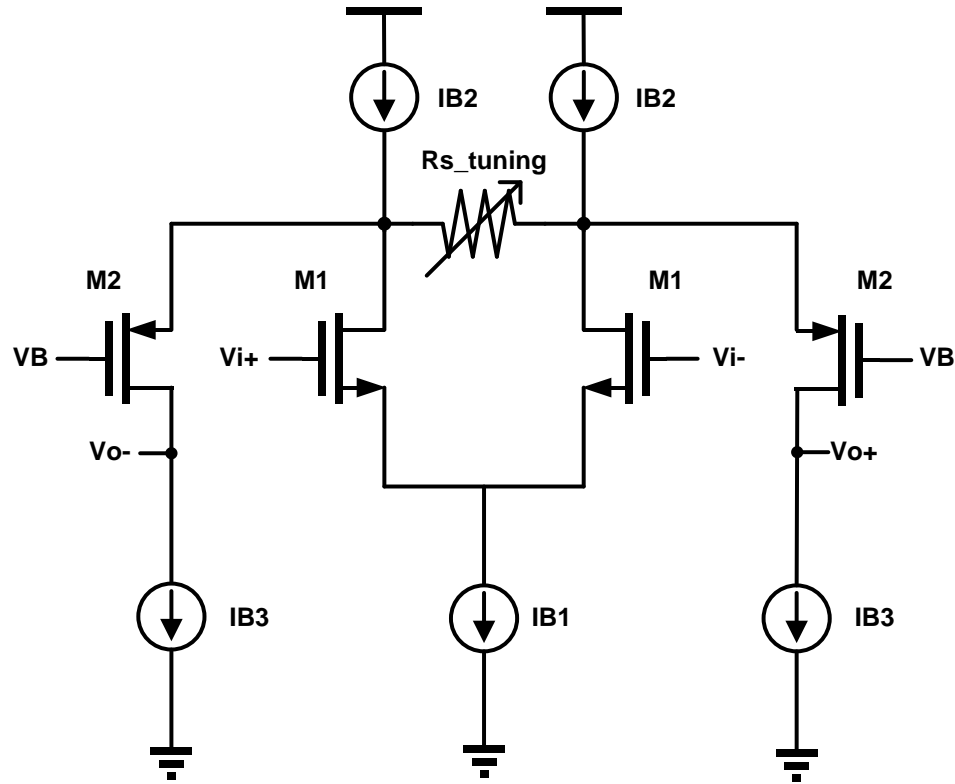


Figure 18 Concept of the tuning output current scheme

We have a basic differential pair input M1 to steer currents, a tunable resistor at the middle to adjust the current, and a folded cascode transistor M2 to steer the remaining currents and allow a larger output swing.

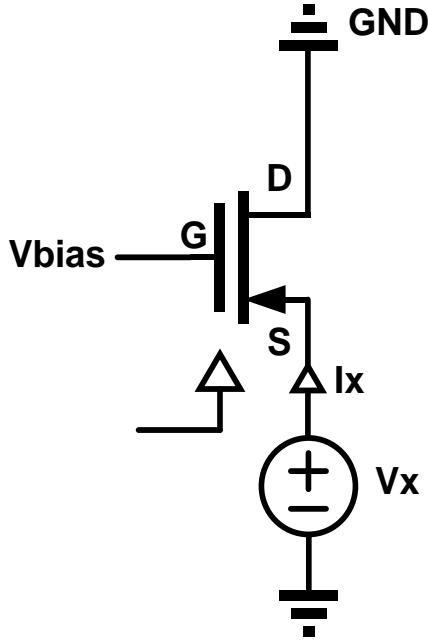


Figure 19 Resistance calculation when looking into the source

The resistance looking at the source of M2 is calculated by adding an external voltage source V_x , and a testing current signal I_x to see what the resistance is. This is shown in Figure 19. By using the small signal model of the NMOS we can calculate the resistance

$$I_x = g_m(V_x - 0) + \frac{V_x}{r_o}$$

$$r_x = \frac{V_x}{I_x} = \left(\frac{1}{r_o} + g_m\right)^{-1} = \left(\frac{1}{g_m} // r_o\right) \approx \frac{1}{g_m} \quad (3.9)$$

As shown in Figure 20, to analyze the whole system on how the output current flows, we replace the input transistors M1 with a current source and the cascode transistor M2 as an impedance of $\frac{1}{gm_2}$ looking at the source.

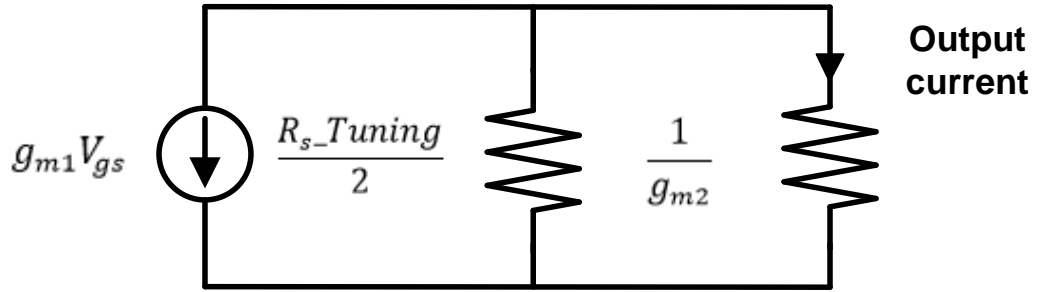


Figure 20 Small signal analysis

Assume the input AC voltage is 1V and for 1st order linear model on the transistor. The output current is simply $G_m = \frac{g_{m1} \times R_s_tuning / 2}{R_s_tuning / 2 + 1 / g_{m2}}$. By tuning R_s you can adjust the current steered to the output ranging from 0 to gm_1 . Note that the most current you can get is gm_1 from the input device and can decrease the output current according to R_s_tuning .

3.5.2 N multiplication factor tuning scheme

The tuning resistor can be replaced by MOSFET to change different multiplication factor to get different currents, this is shown in Figure 21. Note that a multiplication factor of three means there are three MOSFET in parallel, Figure 22 shows an example of an N multiplication factor transistor

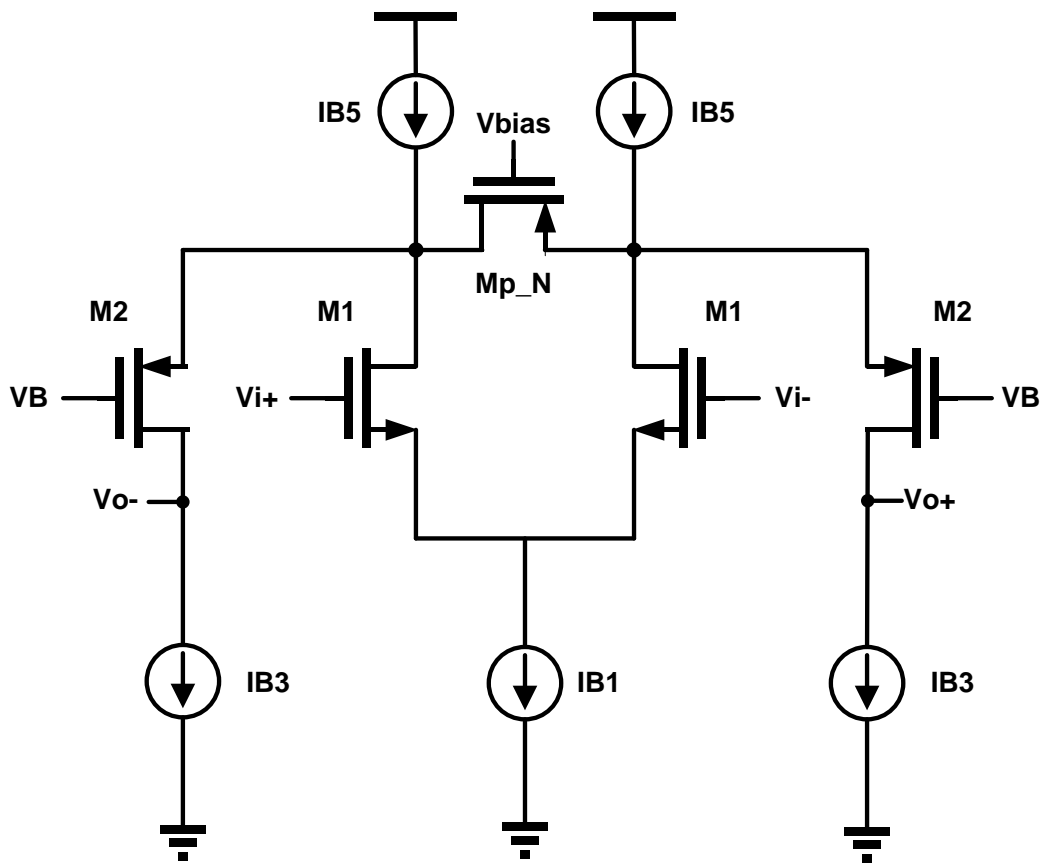


Figure 21 Tuning scheme with an N multiplication factor transistor

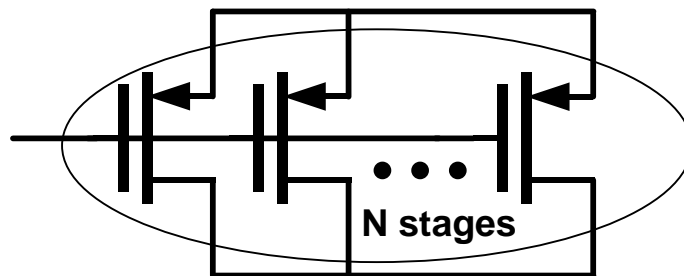


Figure 22 N multiplication factor transistor

The tuning resistor is simply implemented by a PMOS transistor M_{p_N} working in triode region, where N is the multiplication factor of the transistor. We can change the multiplication factor to tune the current flowing to the output. For a large multiplication factor the resulting resistance is the smaller and hence we can decrease the output current. For the tuning transistor M_{p_N} the resistance is

$$R_{on} = \frac{1}{u_p C_{ox} \frac{W}{L} (V_{GS} - V_T)} = g_{d_p} \quad (3.10)$$

The transconductance of the circuit can be calculated as,

$$G_m = g_{m1} \times \frac{u_p C_{ox} (\frac{W}{L})_p (V_{GS_p} - V_T)^{-1}}{u_p C_{ox} (\frac{W}{L})_p (V_{GS_p} - V_T)^{-1} + u_p C_{ox} (\frac{W}{L})_2 (V_{GS_2} - V_T)^{-1}} \quad (3.11)$$

By selecting a proper bias ($V_{bias} = V_B$), the overdrive voltage of both transistor can be designed to be the same and the equation can be reduced to

$$G_m = g_{m1} \times \frac{1}{1 + \frac{(W/L)_p}{(W/L)_2}} \quad (3.12)$$

As shown in equation 3.12 we can make the transconductance a function of the ratio of two PMOS sizes. By using a common centroid layout this ratio will be reliable with process variation or temperature variation. To sum up by making the bias voltage V_B and V_{bias} the same voltage with a common centroid layout technique for M_{p_n} and M_2 the transconductance is well defined with process variations.

Figure 23 shows the transconductance gain values that can be implemented when using different multiplication factors of N. The simulation was done in cadence with

parametric sweeping the multiplier number of M_{p_n} , the transconductance value was measured with putting an ideal voltage source at the output with proper bias with setting $V_{AC} = 1$, the values was imported into Matlab.

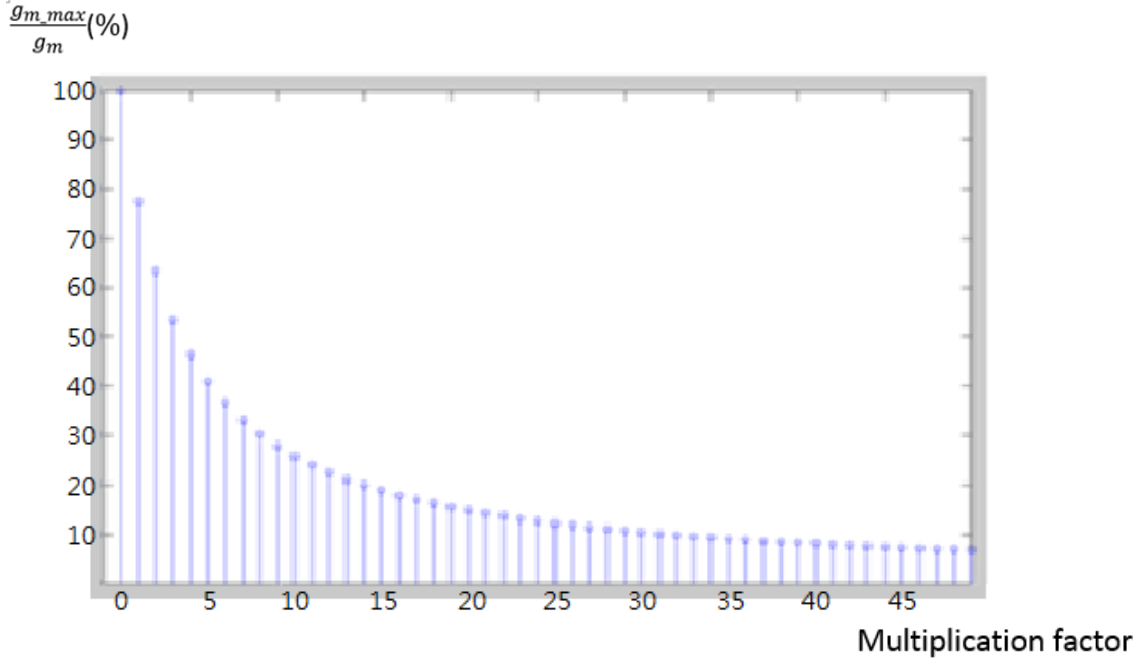


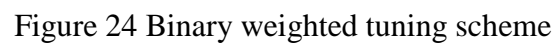
Figure 23 Transconductance tuning with changing the multiplication factor of M_{p_N}

Figure 23 shows the ratio percentage of the transconductance relative to its maximum value (100uA/V in this case) while changing different multiplier of M_p . This figure shows a $1/x$ shape which coincides with equation (3.12)

$$g_{m1} \propto \frac{1}{1+x}, \text{ where } x = \frac{(W/L)_n}{(W/L)_2}$$

In order to get the g_m values listed in Table 2, we will need to design five OTA's with different g_m 's to cover it.

3.5.3 Binary code tuning and biasing



As shown in Figure 24, the tunable transistor is implemented by putting MOSFETS M_N in parallel with different multiplication number. By turning on and off the switches we can get different equivalent multipliers for different resistance. To turn the switched resistor on it needs to be biased at the same voltage as V_B and for the switched resistor to be off it needs to be biased at V_{dd} . The biasing scheme of the switched resistor is shown in Figure 25.

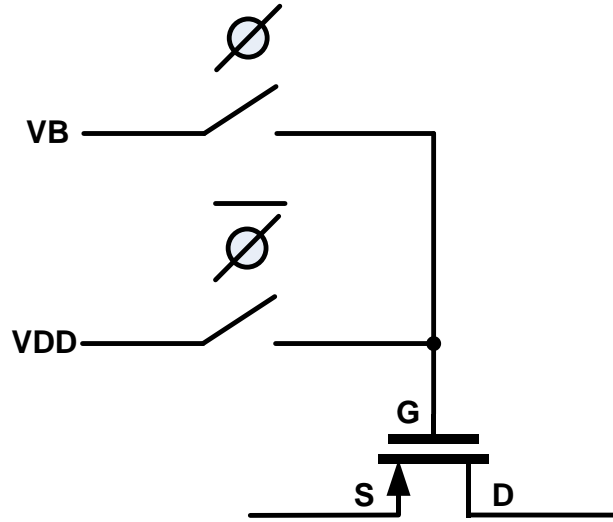


Figure 25 Biasing for the analog switches

The tuning scheme for the switched resistor is simply binary. For a digital code of $\phi = 0$, $\bar{\phi} = 1$ the PMOS gate is biased at V_{DD} and the transistor is off. On the other hand, for a digital code of $\phi = 1$, $\bar{\phi} = 0$ the PMOS gate is biased at V_B and the transistor is ON.

The more switched resistor you have the higher resolution you will have. There is a diminishing effectiveness of tuning the current to very low values since the equation is of the form $\frac{1}{1+x}$ as shown previously. Shown in Figure 26, we have decided to use a binary weighted code with a total of 5 switched resistor which can have a tunability of $2^5 - 1 = 31$ values of transconductance, the binary weighted switched resistor are implemented with putting different parallel numbers of the switched resistor together with sequence of 2 to the power of N, where $N = 1 \sim 5$. Table 4 shows the digital bits and code number for the corresponding M_N , code 1 is the most significant bit and code 5 is the least significant bit. According to the bandwidth needed we will need different transconductance to achieve the target bandwidth, the digital circuits will control which switches to be on and off for each different bandwidth. The length of the switched resistor was chosen with the smallest length available in the technology to maintain a small parasitic capacitance and the width was chosen to have enough resolution when tuning the transconductance, the switched resistor values will be listed at the end of this section.

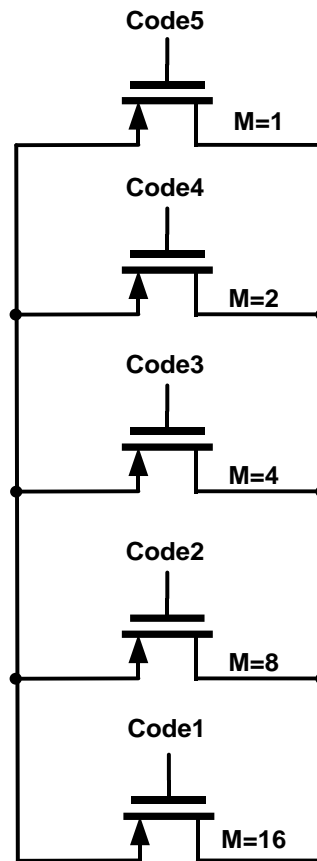


Figure 26 A binary code of 5 for the switches to achieve different tuning

Table 4 Digital codes and sizes for the corresponding switches

| Digital bits | X0000 | 0X000 | 00X00 | 000X0 | 0000X |
|-------------------|-------|-------|-------|-------|-------|
| Code number | Code1 | Code2 | Code3 | Code4 | Code5 |
| Multiplier number | 16 | 8 | 4 | 2 | 1 |

3.5.4 Simulation results for tunable current

The simulation was done in cadence using parametric to sweep different codes to get different output current. Table 5 shows all the tuning codes with the respective output current.

Table 5 Digital code for the corresponding output current

| | | | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Code | 00000 | 00001 | 00010 | 00011 | 00100 | 00101 | 00110 | 00111 | 01000 |
| Gm(uA) | 95.08 | 85.09 | 77.00 | 70.32 | 64.70 | 59.91 | 55.79 | 52.19 | 49.03 |
| Code | 01001 | 01010 | 01011 | 01100 | 01101 | 01110 | 01111 | 10000 | 10001 |
| Gm(uA) | 46.23 | 43.74 | 41.50 | 39.47 | 37.64 | 35.97 | 34.44 | 33.03 | 31.74 |
| Code | 10010 | 10011 | 10100 | 10101 | 10110 | 10111 | 11000 | 11001 | 11010 |
| Gm(uA) | 30.54 | 29.43 | 28.40 | 27.44 | 26.54 | 25.70 | 24.91 | 24.16 | 23.46 |
| Code | 11011 | 11100 | 11101 | 11110 | 11111 | | | | |
| Gm(uA) | 22.80 | 22.18 | 21.59 | 21.03 | 20.49 | | | | |

We took the needed value for Gm16 on Table 2 and compare the results to see how well it matches, this is shown in Table 6.

Table 6 Comparison of ideal G_m needed and the implemented G_m

| | | | | | | | |
|---------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Ideal G _m (uA) | 21.53 | 27.12 | 35.56 | 41.3 | 46.49 | 51.44 | 59.12 |
| Implemented G _m (uA) | 22.8 | 28.40 | 37.64 | 41.50 | 49.03 | 52.19 | 59.91 |
| Percentage difference | 5.2% | 4.7% | 5.4% | 0.48% | 5.3% | 1.4% | 1.3% |
| Code | 11011 | 10100 | 01101 | 01011 | 01000 | 00111 | 00101 |
| Ideal G _m (uA) | 70.49 | 81.86 | 94.87 | | | | |
| Implemented G _m (uA) | 70.32 | 85.09 | 95.08 | | | | |
| Percentage difference | 0.2% | 0.2% | 0.2% | | | | |
| Code | 00011 | 00001 | 00000 | | | | |

From Table 6 we notice the percentage difference is small on large G_m and can get up to 5% of difference while tuning it to lower values, this is because the need to get to very low G_m is limited by its $1/x$ property. However, this is not a problem. Due to the previous FIR system simulation we know that for small gm's as long as the percentage difference is not above 10% the result is almost the same. Also recall the FIR function is a ratio of two G_m and the percentage can cancel each other.

To sum up we implemented a tunability of 31 different transconductance with 5 codes as shown in Figure 27.

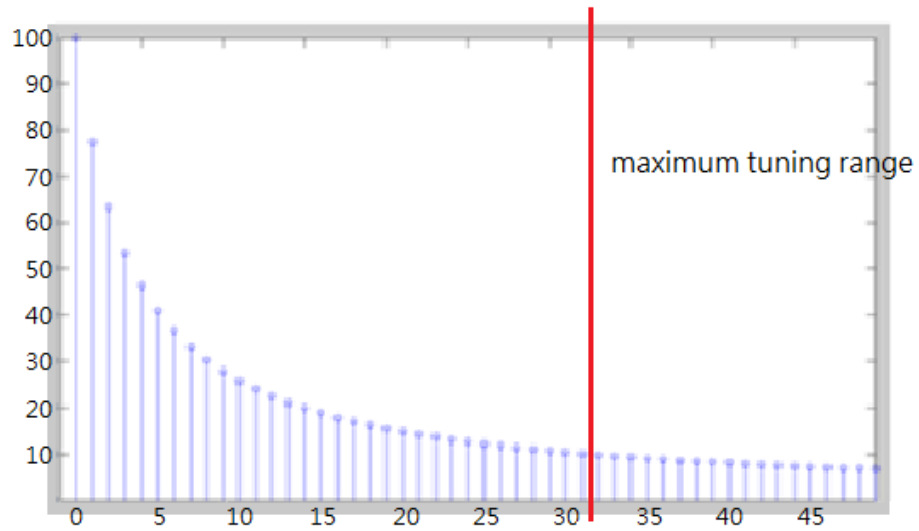


Figure 27 Achievable tunability for the OTA

3.5.5 MOSFET parasitic analysis

MOS transistor have Source and Drain terminal that can have different parasitic capacitance at both sides due to layout. For example, in Figure 28 and Figure 29 where we have a two finger transistor, the drain capacitance is roughly two times then the drain.

Since $C_d \approx 2C_s$, the impedance at both sides are unsymmetric (not same). Maintaining symmetry in differential circuits is important since you can cancel even order nonlinearities [24][25].

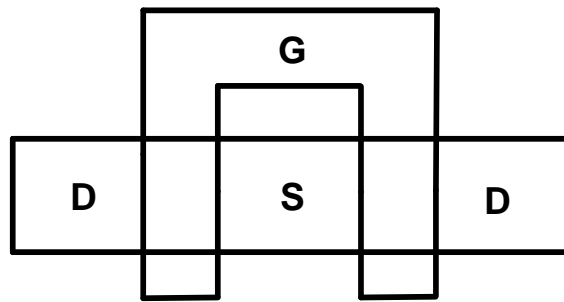


Figure 28 Different parasitic capacitance at source and drain

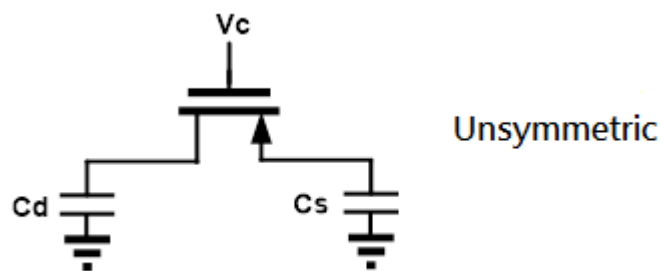


Figure 29 Unsymmetrical parasitic on MOSFET

If we put two transistors in cascade with proper placement of the source and drain, both sides will have the same capacitance at the left and right side to provide symmetric capacitance.

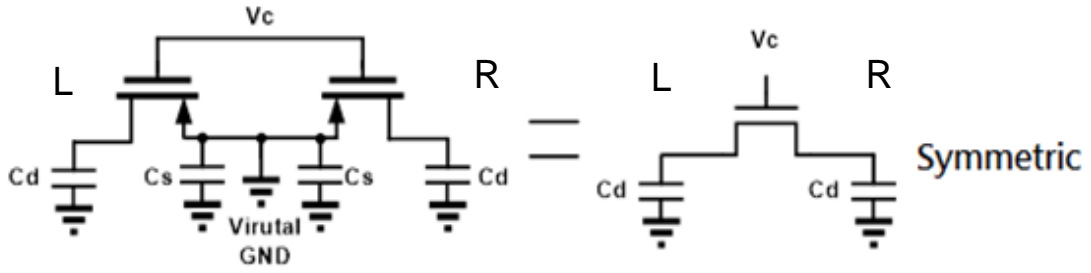


Figure 30 Symmetric impedance for the switched resistor

Placing the switched resistor into the main OTA, node L and R will have the same voltage if the OTA is designed properly. As shown in Figure 30, a virtual ground (AC ground) is located at the middle and C_s can be neglected since both sides of the terminal is shorted to AC ground. What we have left is C_d at both sides and can make effort on the layout to try to minimize the capacitance.

3.6 Operational transconductance amplifier design

This section contains analysis and simulations results for the designed OTA. Parameters like output resistance, transconductance frequency response, linearity and noise are the most critical ones. Figure 31 shows the schematic of a simplified OTA with N-Type input stage, the biasing and common mode feedback are omitted just for the sake of analysis.

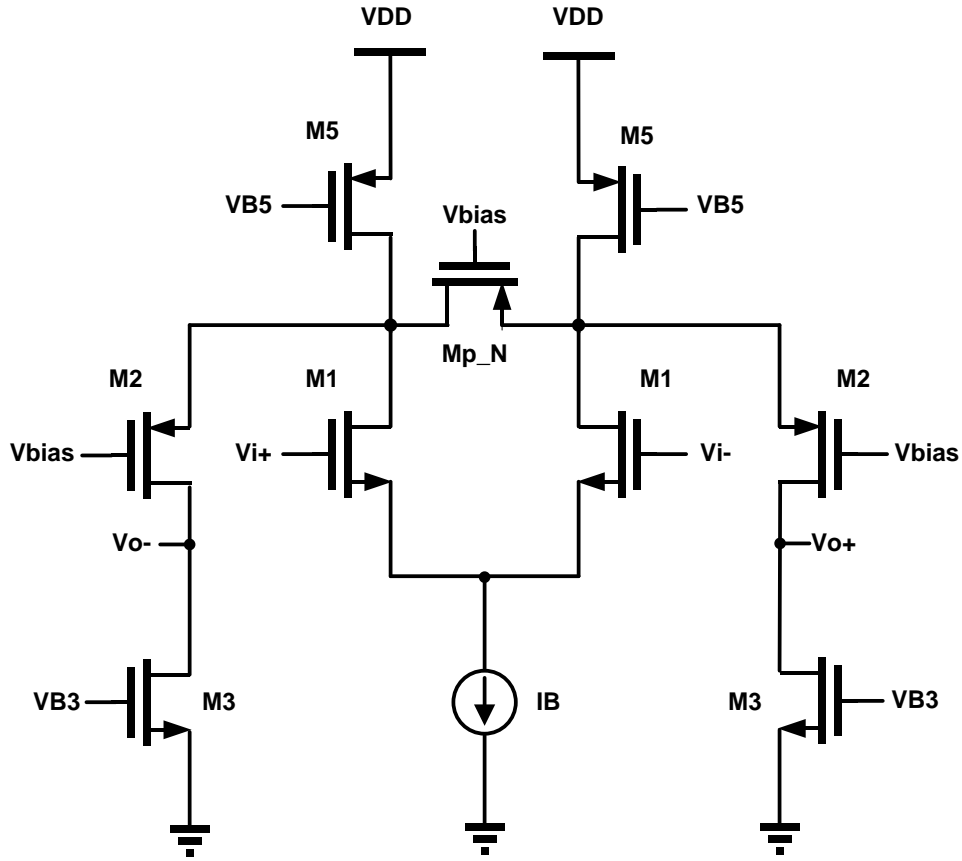


Figure 31 Simplified OTA for analysis purpose

3.6.1 Transconductance frequency response

By changing the multiplication factor of M_{P_N} (The number of parallel MOSFET devices), we can tune the transconductance of the OTA. Figure 32 shows the transconductance frequency response while changing the multiplication factor of M_{P_N} . The multiplication factor changes from 1 to 31 in respect to the lines from top to bot shown in Figure 32.

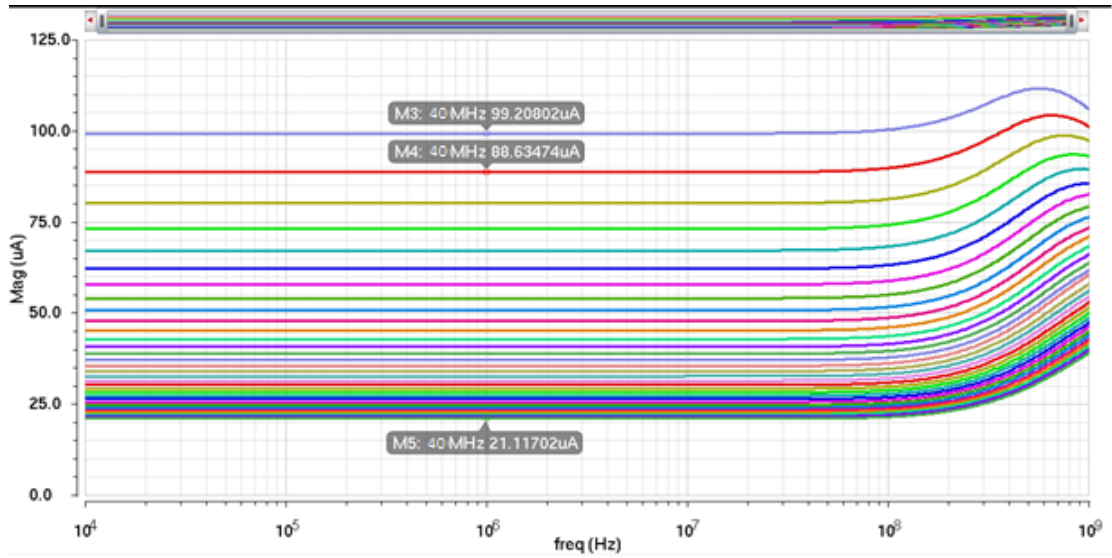


Figure 32 Transconductance frequency response while changing the multiplication number of M_{P_N}

Since we are only interested in the low frequency transconductance, we can simply look at the transconductance value at 40MHz (center frequency of the filter). With the help of CADENCE “value” function we can take the transconductance value and plot it in histogram as shown in Figure 33.

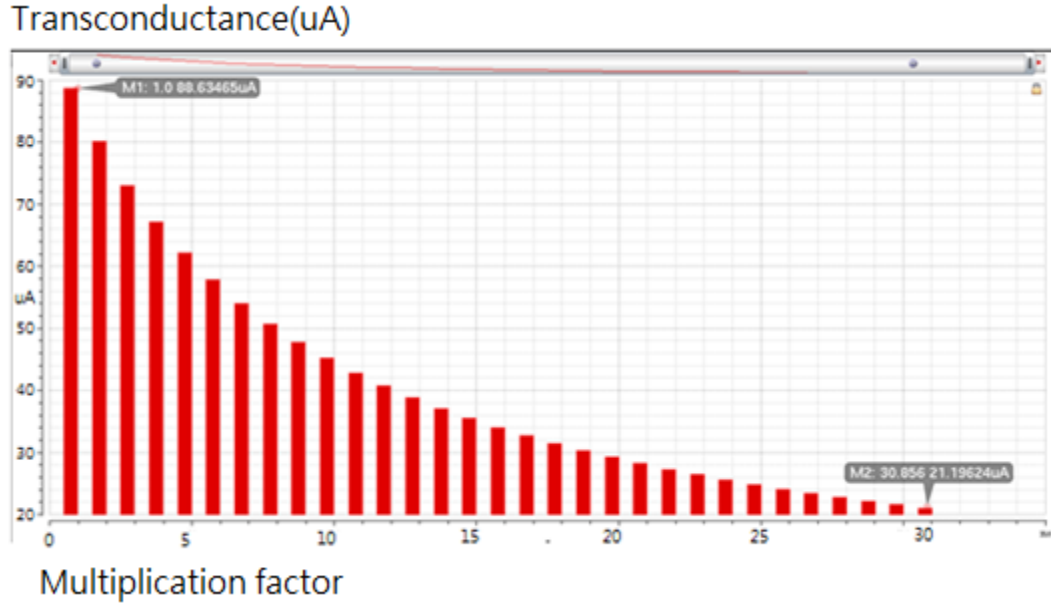


Figure 33 Transconductance value while changing the multiplication factor of M_{P_N}

Figure 33 shows the tunability of the transconductance with the shape of $\frac{1}{x}$ which was discussed in the previous section.

3.6.2 Output resistance

Assuming we have a multiplication factor of N on the tuning transistor M_{P_N} .

The output resistance is:

$$\begin{aligned}
 R_o &\approx r_{o3} // (g_{m2} r_{o2} (r_{o1} // r_{o5} // \frac{0.5}{g_{dsp_N}})) \\
 &= r_{o3} // (g_{m2} r_{o2} (r_{o1} // r_{o5} // (\frac{0.5}{u_p C_{ox} N (\frac{W}{L})_{p_N} V_{ov}})))
 \end{aligned}$$

which means when we try to change different multiplication factor for M_{p_N} the output resistance will also vary which is undesirable if the percentage difference is large and having a small output resistance in one case. To simulate the output resistance we put an ideal voltage source with 0.9V DC bias voltage and set AC voltage to 1, we then take the reciprocal of the small signal current.

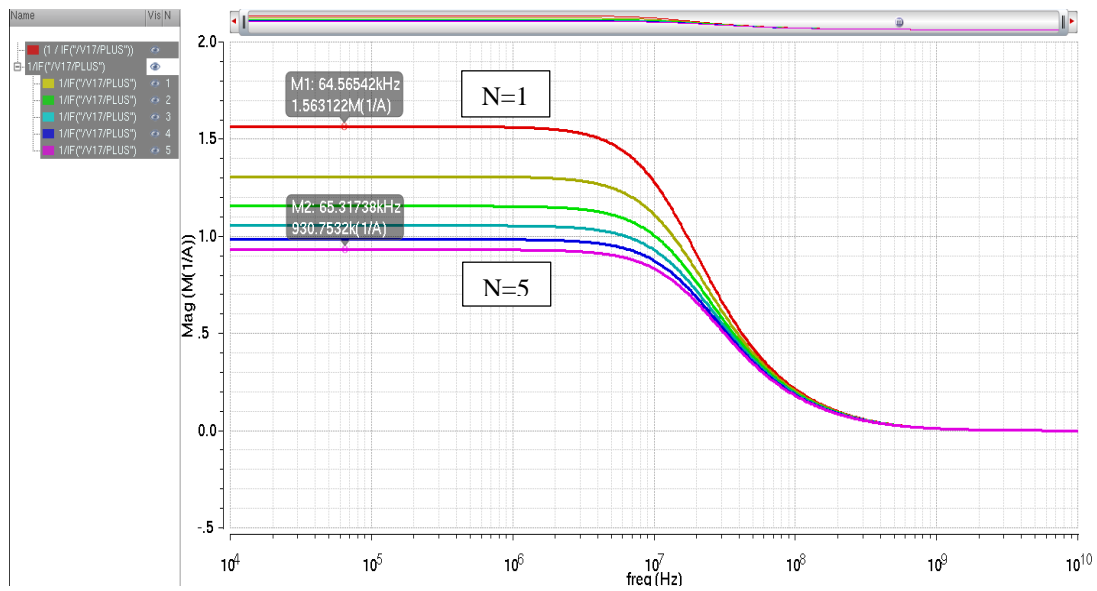


Figure 34 Output impedance when changing the multiplier of the switch

Figure 34 shows the output resistance decreases while having a larger multiplication factor. For multiplication factor changing from 1 to 5 the resistance can drop to 40%, although it is still higher than the specification of 650k Ohms this is undesirable as if you have unit step input voltage the rising and fall time of the output voltage will be different which might cause ISI problems [25].

3.6.3 Input/Output common mode voltage

The input and output common mode voltage was set to half the VDD (0.9V) to maximize the output swing. However, as seen in Figure 35 the OTA output will be connected to Mn and Mp working as an analog switch to charge the current to CL depending on the clocks ϕ_i .

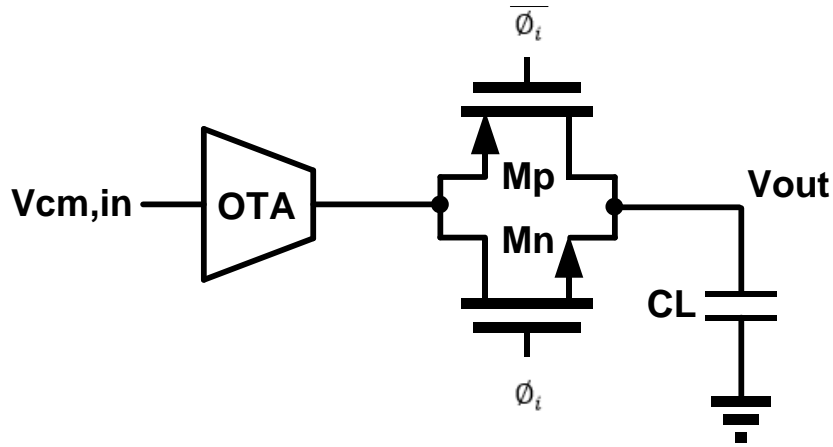


Figure 35 Simplified model for the FIR filter operation

Figure 36 shows the switch resistance with different common mode voltage. Line1 is with NMOS transistor, line2 is with PMOS transistor and line3 is NMOS and PMOS in parallel. If we chose to use NMOS and PMOS transmission gate the resistance is relatively low for all input common mode voltage, however the parasitic capacitance it provides is the largest of all three cases and is not desirable. In the next section we've chosen an input/output common mode voltage of 0.6V volts so we can use an NMOS analog switch for low resistance while keeping a relative small parasitic capacitance.

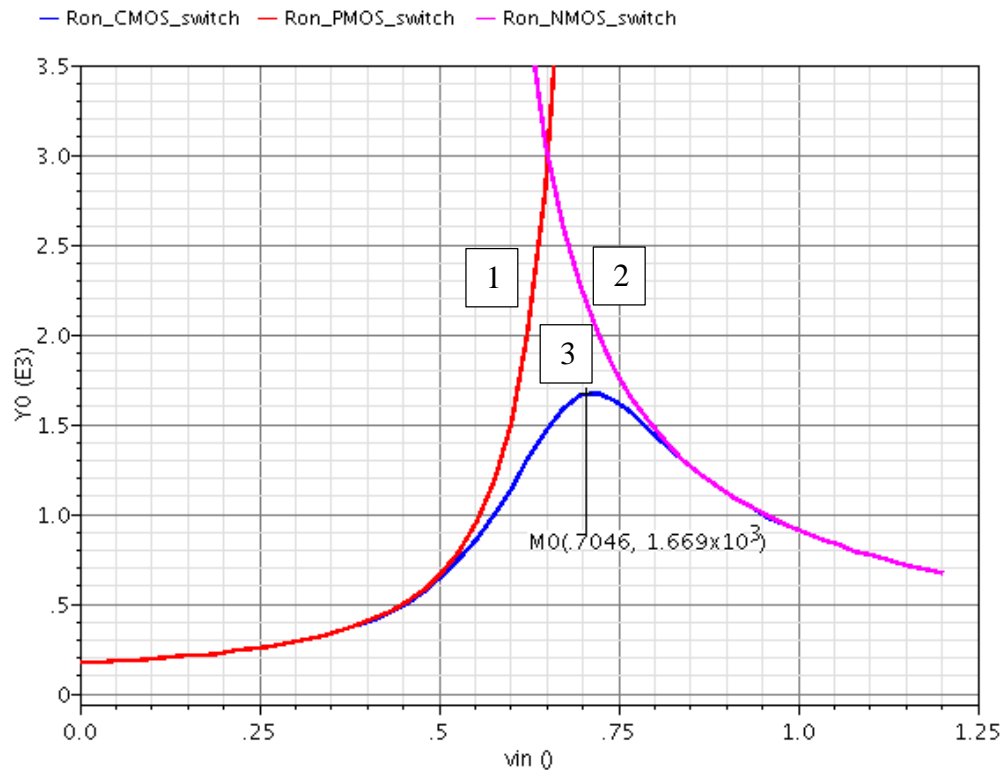


Figure 36 Switch resistance with different common mode voltage

3.6.4 Frequency response, DC gain, Power consumption

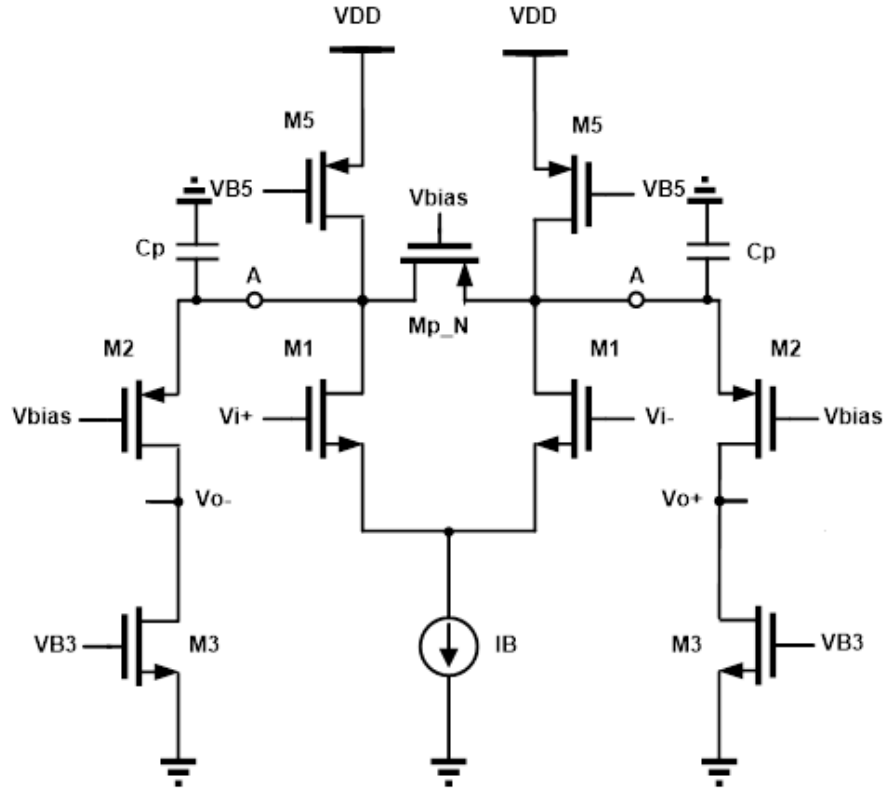


Figure 37 Schematic for transconductance frequency response

Figure 37 shows the schematic for frequency response analysis. Mostly we are interested in the transconductance of the OTA, to calculate it we can short the output to

ac ground (fixed DC bias). The transconductance can be calculated as $G_m = g_{m1} \frac{1}{1 + \frac{s}{\omega_p}}$,

where $\omega_p = RC_p$, R is the equivalent resistor seen at node A which is $(\frac{1}{g_{m2}} // r_{o1} // r_{o5} //$

$\frac{1}{g_{dsp_N}})$, C_P is the equivalent capacitor seen at node A, which is $\frac{C_{gs_M1}}{2} + C_{db_M1} +$

$$C_{db_M5} + C_{gd_M5} + C_{db_Mp_N} + C_{gd_Mp_N} + C_{gs_M2} + C_{sb_M2}.$$

To have a good frequency response we will need to push the pole to a high frequency, this can be done by minimizing the parasitic poles at node A which means smaller transistor sizes.

The simulation was done in cadence from AC simulation and plotting the gain and phase margin from V_i to V_o as shown in Figure 38.

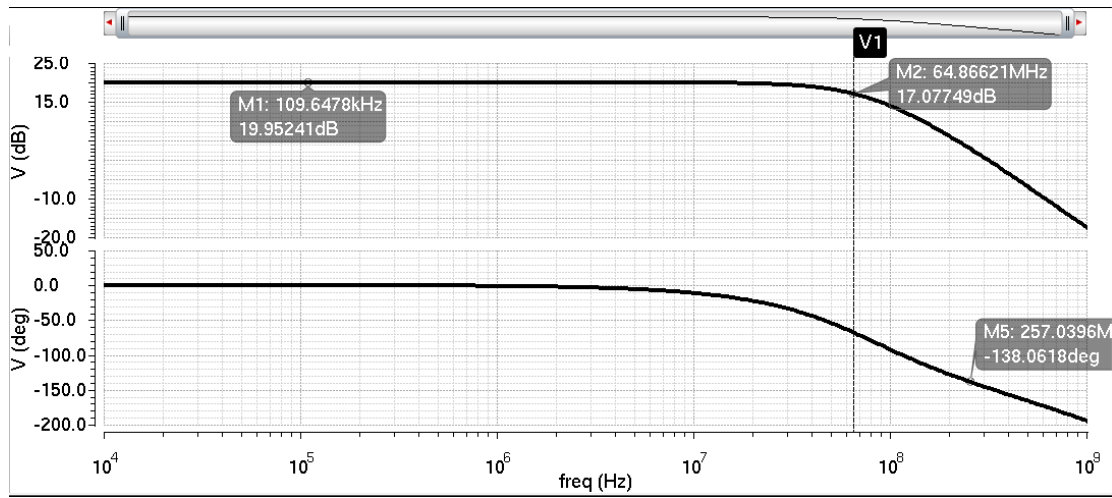


Figure 38 Frequency response of the OTA

The total power for a single OTA is

$$Power = V_{dd} \times 2I_{B5} = 1.8 \times 120\mu A = 216\mu W$$

Although power is not a main concern here, it is desirable to keep it as small as possible.

3.6.5 Noise analysis

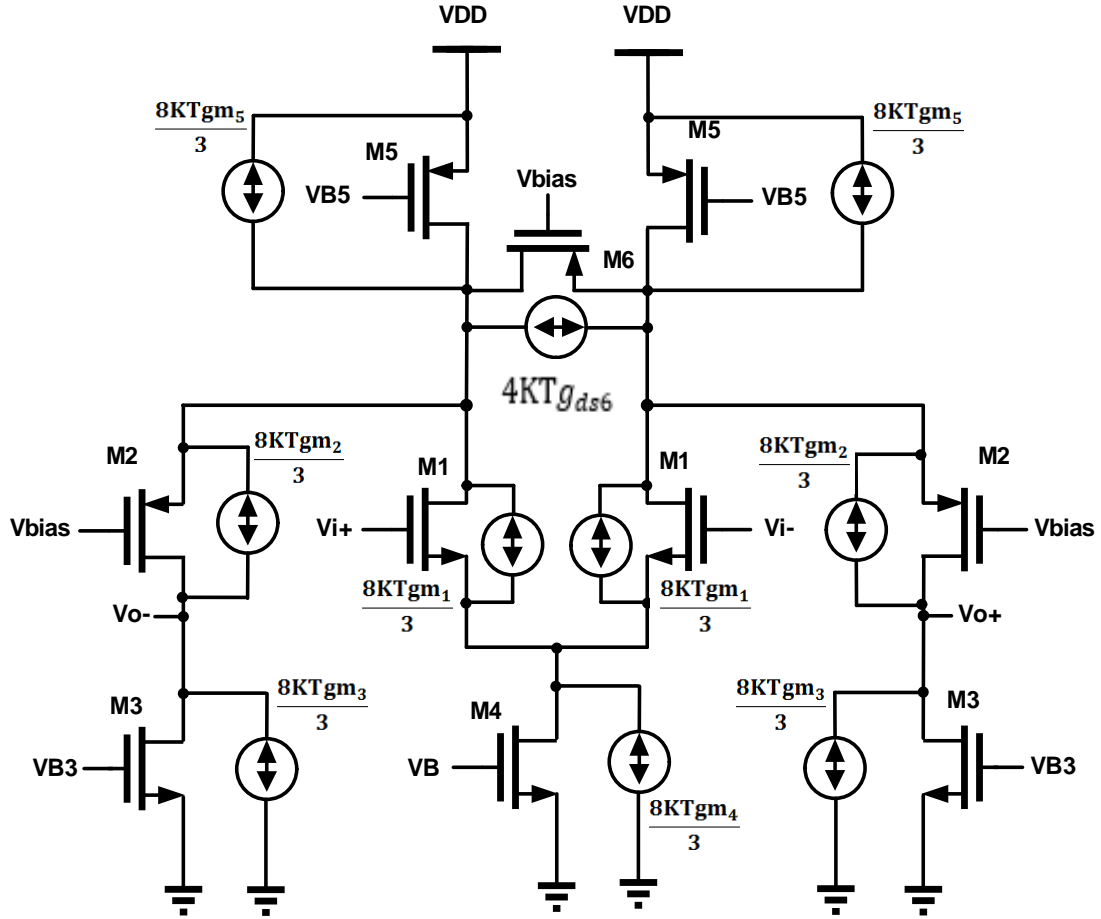


Figure 39 Noise analysis of the OTA

Since our specification operates at high frequency the flicker noise is negligible and will be omitted in the analysis. Also, $r_o \gg \frac{1}{g_m}$ since $g_m r_o > 10$ in typical modern technology.

The output current noise can be calculated from Figure 39.

$$\overline{I_o^2} = 2 \times \frac{8KT}{3} (g_{m3} + g_{m1}(\frac{g_{m2}}{g_{m2} + g_{ds6}})^2 + g_{m5}(\frac{g_{m2}}{g_{m2} + g_{ds6}})^2 + g_{m2}(\frac{g_{ds6}}{g_{m2} + g_{ds6}})^2 + \frac{3}{2} g_{ds6}(\frac{g_{m2}}{g_{m2} + g_{ds6}})^2)$$

The noise of the tail current source $\frac{8KTg_{m4}}{3}$ is evenly split half to the output

therefore contributes no noise. To find the equivalent input referred noise we divide it by

G_m^2 which is

$$G_m^2 = (g_{m1} \frac{g_{m2}}{g_{m2} + g_{ds6}})^2$$

$$\overline{V_{in}^2} = \frac{\overline{I_o^2}}{G_m^2} = \frac{16KT}{3} (g_{m3} (\frac{g_{m2} + g_{ds6}}{g_{m1}g_{m2}})^2 + \frac{1}{g_{m1}} + \frac{g_{m5}}{g_{m1}^2} + \frac{3}{2} \frac{g_{ds6}}{g_{m1}^2})$$

From this equation we know to have a low noise OTA, we must increase g_{m1} , decrease g_{m3} , g_{m5} . This can be done by proper transistor sizing with maximizing $(\frac{W}{L})_1$ while still maintaining the linearity needed and minimizing $(\frac{W}{L})_3$, $(\frac{W}{L})_5$ while keeping v_{dsat} small for the voltage headroom.

We will also want g_{ds6} to be small for low noise, however it is related to the tunability of the OTA resulting in a tradeoff between tunability and noise (A large size M_6 can tune the transconductance to a low value with a tradeoff of injecting more noise). It is desirable to have a low input noise and we will introduce a simple technique to reduce the noise from I_{B3} and I_{B5} with the tradeoff of reduced voltage headroom.

As shown in Figure 40, if we keep the same transistor size M3 and add a source degeneration resistor for the current source we can reduce the noise at the output with the tradeoff for less voltage headroom.

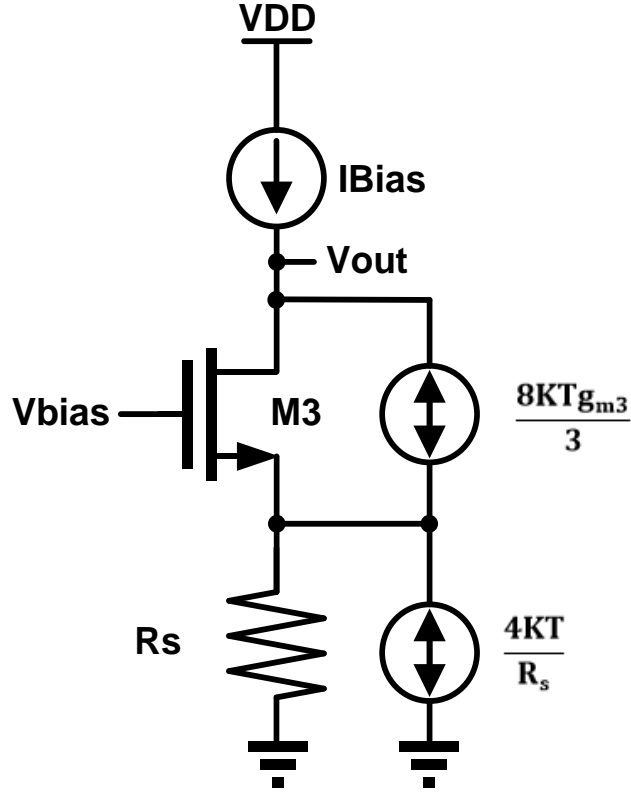


Figure 40 Adding source degeneration at current source for less noise

The total noise will then be

$$I_o^2 = \frac{8KTg_{m3}}{3} \left(\frac{1/g_{m3}}{1/g_{m3} + R_s} \right)^2 + \frac{4KT}{R_s} \left(\frac{R_s}{1/g_{m3} + R_s} \right)^2$$

to compare with the original noise without adding the source degeneration or $R_s = 0$, we take the ratio of both total noise

$$\frac{\text{Noise with source degeneration}}{\text{Noise without source degeneration}} = \frac{\frac{8KTg_{m3}}{3} \left(\frac{1}{1 + g_{m3}R_s}\right)^2 + \frac{4KT}{R_s} \left(\frac{g_{m3}R_s}{1 + g_{m3}R_s}\right)^2}{\frac{8KTg_{m3}}{3}}$$

$$= \frac{1}{1 + g_{m3}R_s} + \frac{1}{2} \frac{g_{m3}R_s}{(1 + g_{m3}R_s)^2}$$

If

$$\frac{1}{1 + g_{m3}R_s} + \frac{1}{2} \frac{g_{m3}R_s}{(1 + g_{m3}R_s)^2} < 1$$

then the source degeneration is an improvement in noise. As long as $g_{m3}R_s > 0$, the topology with source degeneration resistor will result in lower noise. However, this will have a lower voltage headroom of $I_{Bias}R_s$ as the resistor consumes extra voltage and also has a lower overall transconductance.

As discussed in appendix B, the noise of a single transistor is $\frac{4KT\gamma}{g_m}$, γ depends on process and therefore we need a test bench to extract the value. The test bench is shown in Figure 41 with an inductor as the load (noiseless) with the proper bias, Figure 42 shows the simulation result of the input referred noise.

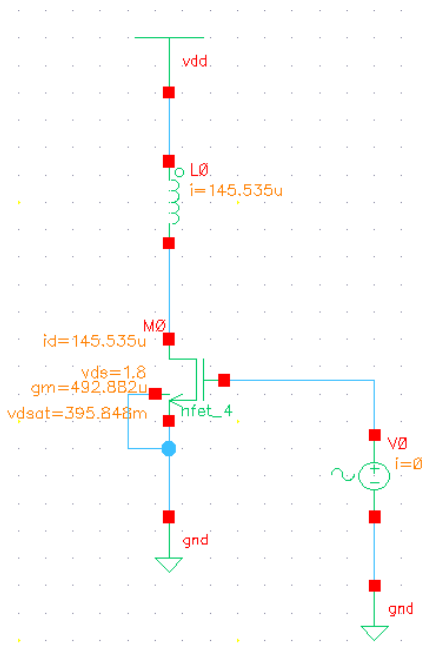


Figure 41 Test bench for extracting γ

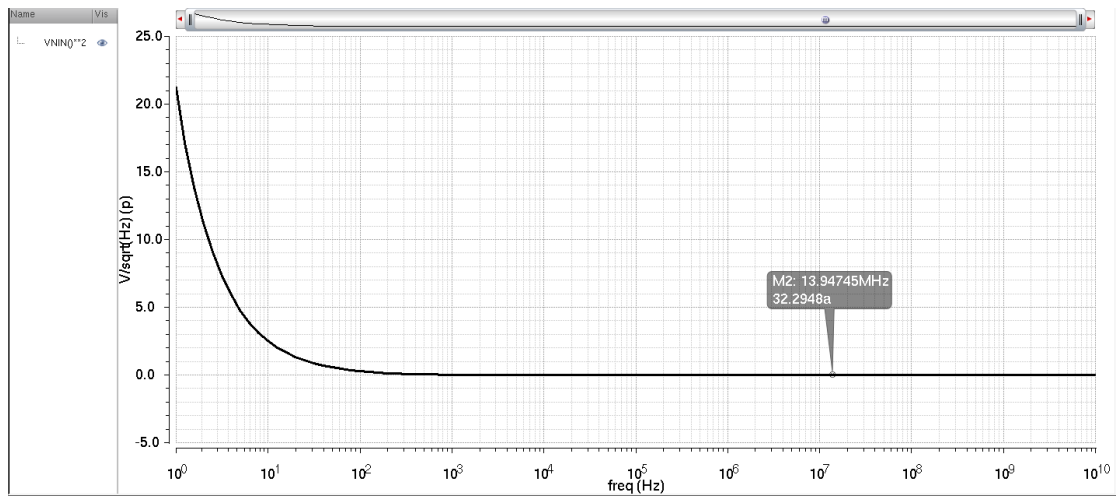


Figure 42 Input referred noise of a single transistor for extracting γ

The input referred noise simulation result is $32.3\text{aV}^2/\text{HZ}$ where it locates at a higher frequency so it's not affected by the flicker noise. Reversing the input referred voltage noise equation from $\overline{V_{in}^2} = \frac{4KT\gamma}{g_m}$ to $\gamma = \frac{g_m \overline{V_{in}^2}}{4KT}$ we can get

$$\gamma = \frac{32.3 \times 10^{-18}}{4 \times 1.38 \times 10^{-23} \times 300} \times 493 \times 10^{-6} = 0.96$$

With the γ extracted we can have 1st order comparison between the calculation and simulation results. Figure 43 shows the input referred noise with different degeneration resistor while M6 was turned off.

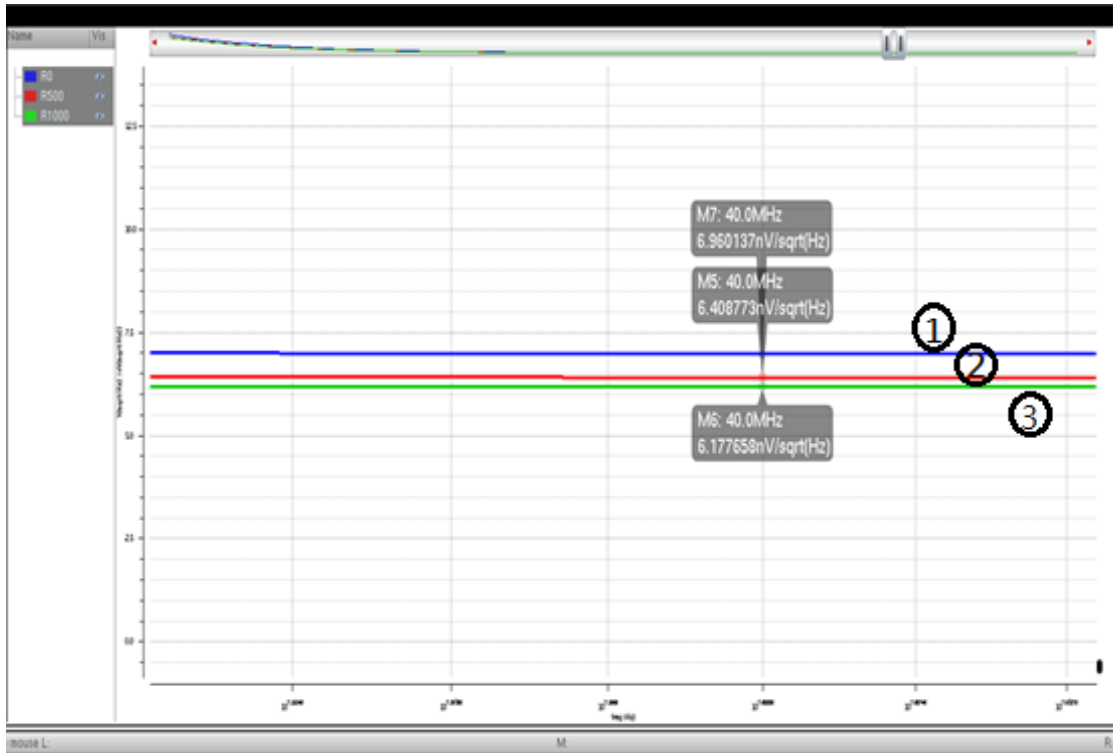


Figure 43 Input referred noise (zoned in thermal noise) of the OTA with different degeneration resistor values

The lines starting from top to bottom (1 to 3) correspond to the source degeneration resistor for the current source with value of 0 ($6.96\text{nV}/\sqrt{\text{Hz}}$), 500 ($6.4\text{nV}/\sqrt{\text{Hz}}$) and 1000 ($6.17\text{nV}/\sqrt{\text{Hz}}$) Ohm respectively, there is about 11 percent difference from the largest and smallest case which is not large, but still a small improvement with a tradeoff of 25mV drop of voltage headroom. To sum up, for higher degeneration resistor used for the current source the output noise is smaller, however the voltage headroom decreases by IR . We chose a resistor value of 1k Ohm for a reasonable tradeoff between the two.

Figure 44 shows the simulation of input referred noise with a source degeneration of 1k Ohms and different multiplication factor of M6.

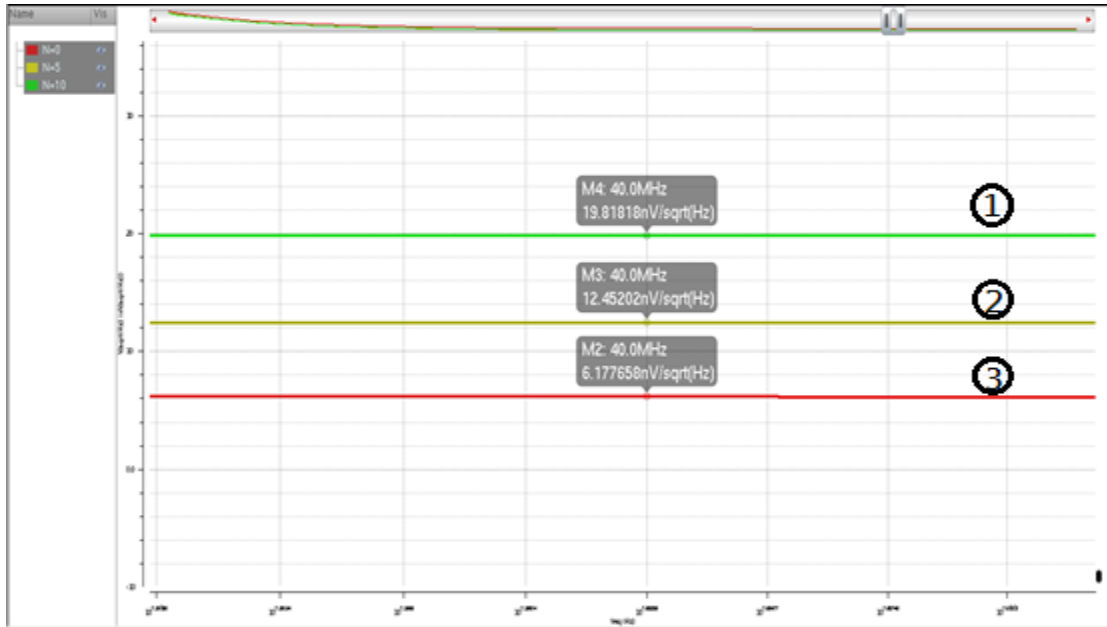


Figure 44 Input referred noise (zoned in thermal noise) of the OTA with different multiplication factor

In Figure 44, the lines starting from top to bottom (1 to 3) corresponds to multiplication factor of 10, 5 and 1 respectively, there is about 300% difference in noise between multiplication factor of 1 and 10. As a result, the more current we split into M6 to decrease the current, the more noise we get. This is inevitable and have to watch out not to over tune it for a large noise.

3.6.6 Linearity

Using the calculations in appendix B, we have $H_{D3} = \frac{1}{32} \frac{V_{in}^2}{(V_{GS} - V_T)^2}$ or $IP_3 = 3.3(V_{GS} - V_T)$, normally we want the overdrive voltage of the input device as large as possible to achieve good linearity. To simulate the linearity of IP_3 we use two tone simulation using periodic steady state in cadence, the result is shown in Figure 45. The details on the test bench are discussed in reference [28].

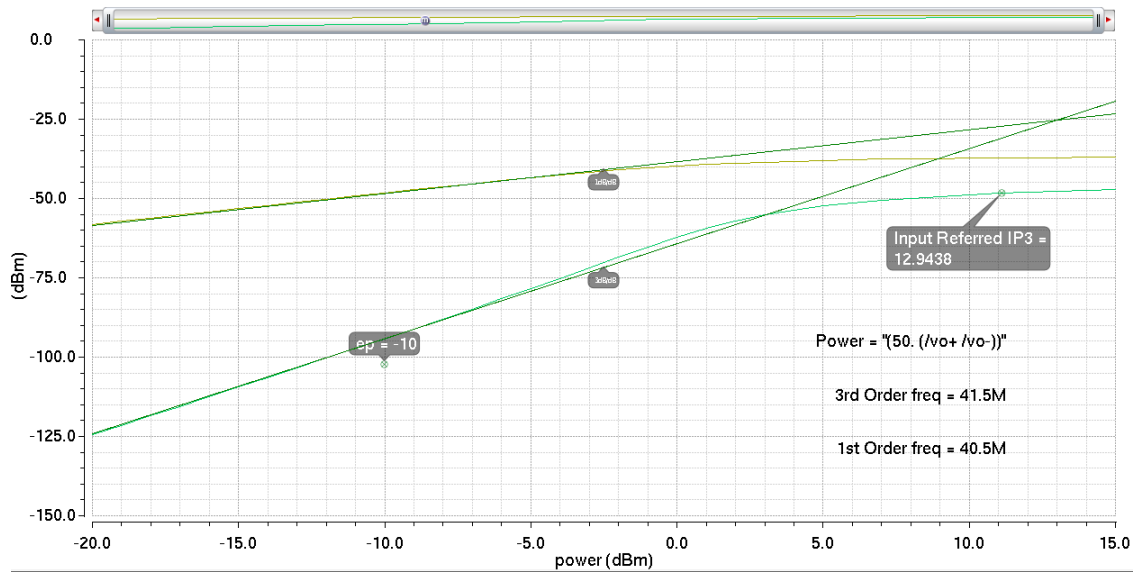


Figure 45 Linearity simulation result

The simulated IIP3 was 12.9dBm for an overdrive voltage of 260mV for the input transistor, the size of the input transistor was small to achieve a rather large overdrive voltage while pushing the voltage of drain to source of the tail current transistor barely on the edge of saturation. According to the equation $IP_3 = 3.3(V_{GS} - V_T)$ in Appendix A, for an IIP3 of 15dBm we need at least 380mV overdrive voltage, however since we are limited at a 1.8V voltage supply and having a 900mV bias at the input it is hard to achieve without the tail current transistor going into triode region with more voltage headroom.

To get more headroom for the tail current transistor we can have a higher input common mode voltage, however for maximum swing we will want the common mode voltage to be at half the VDD. There is a tradeoff between linearity and voltage swing. We will show a simple circuit technique which incorporates degenerated source resistance to improve the linearity in the section 4.

3.6.7 Design method and result

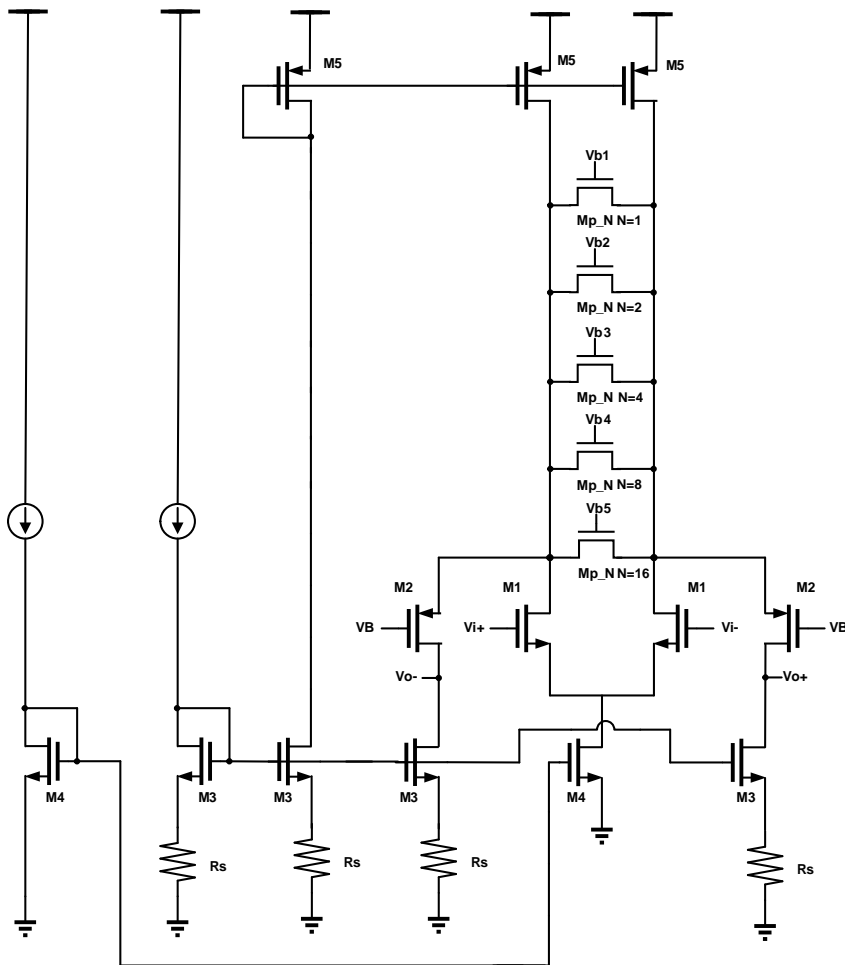


Figure 46 Schematic for the possible solution OTA

The final schematic we arrived in this section is shown in Figure 46. We start with sizing the input transistor with its smallest length provided in the technology for faster speed, the width is sized for the needed gm and linearity according to equation

$$HD3 = \frac{A_{HD3}}{A_F} \approx \frac{V_m^2}{32(V_{GS}-V_{TH})^2}. R_s \text{ was chosen so that the voltage headroom lost } (IR_s), \text{ is}$$

not too large with the improvement in noise. Once we find the size for the input transistor and the bias current we can move on sizing M2. M2 serves as a current buffer and it is better if we size it large but still maintaining $V_{DSAT} > 150mV$ to stay in strong inversion. M_{P_N} has the same length as M_2 and the width is sized to match the transconductance with table 2 . The length of the current mirrors was chosen as $180*4\mu m$ for better matching, and the length of the other transistor was 180n for maximum speed. Table 7 shows the transistor sizes for Figure 46 and Table 8 shows the simulated results for the circuit.

Table 7 Transistor sizes for the OTA

| IB1 | IB2 | Rs | M1 | M2 | M3 | M4 | M5 | Mp_N |
|-----|-----|----|---------|---------|-----------|---------|---------|-----------|
| 20u | 20u | 1k | 2u/900n | 3u/600n | 1.6u/900n | 3u/900n | 3u/900n | 600n/600n |
| | | | 2 | 4 | 1 | 2 | 2 | |

Table 8 Calculated and simulation result comparison

| | Calculated | Simulated |
|----------------------|------------------------------------|------------------------------------|
| Output resistance | 650k Ohm | 930k Ohm |
| Linearity (IIP3) | 12.2dBm ($V_{ov} = 280mV$) | 12.94dBm |
| Noise (spot noise) | $8.12 \text{ nV}/\sqrt{\text{Hz}}$ | $6.98 \text{ nV}/\sqrt{\text{Hz}}$ |
| In/Output CM voltage | 0.9V | 0.9V |
| Power | 216uW | 208.4uW |

The simulation result from Table 8 is when transistor M_{N_P} is off, when we change different codes for different transconductance the output resistance, linearity and noise will also change to some extent. To sum up, this topology has some weakness.

1: During different tuning phases the output resistance change. 2: Linearity does not meet the required specification and will need a larger V_{dsat} which will kill the voltage headroom. 3: The input/output common mode voltage is relatively high if we were connecting the OTA output to a NMOS analog switch for minimum parasitic capacitance.

4. IMPROVED OTA FOR FIR FILTER APPLICATION

One of the challenging aspect in designing tunable OTA is it's insensitivity to parameters for different tuning schemes. As shown in section 3, the output resistance changes a lot when changing the transconductance, also the linearity is not good enough for the application. In this section we used the main concept of the previous circuit but made some adjustment for it.

4.1 Improvements for the OTA

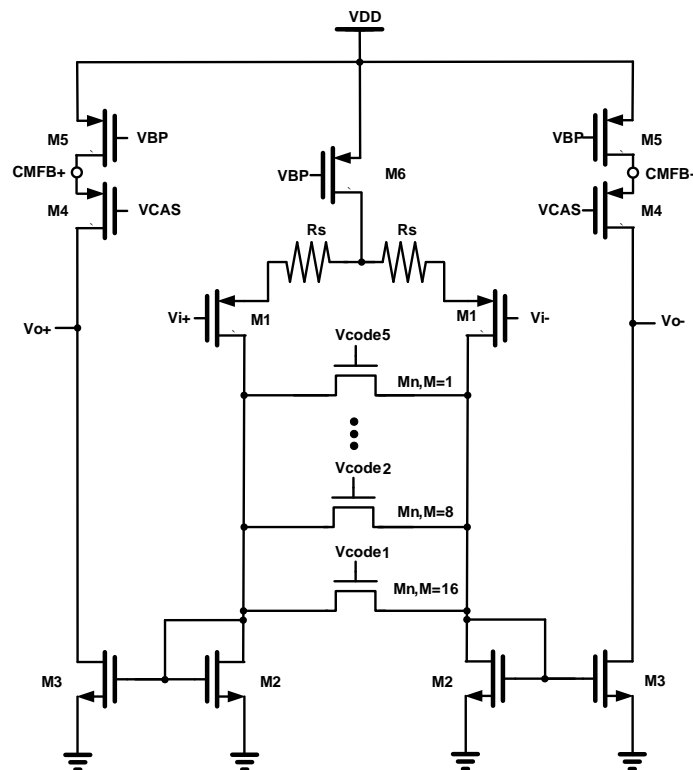


Figure 47 Schematic of the OTA

The improved schematic is shown in Figure 47, we've changed to PMOS input device to increase the voltage headroom since we desire a low common voltage. Current mirror that acts like a current buffer M2 and M3 were also added so that output resistance will be insensitive when the analog switches are turned on and off. Degeneration resistors R_s are added to increase the linearity with the tradeoff of voltage headroom. Also the node CMFB is where the CMFB circuit will return its adjusted signal to have a fixed output voltage. The details for the CMFB circuit will be mentioned in the section below.

4.2 Bias circuit

The bias circuit for the analog switches M_n is shown in Figure 48.

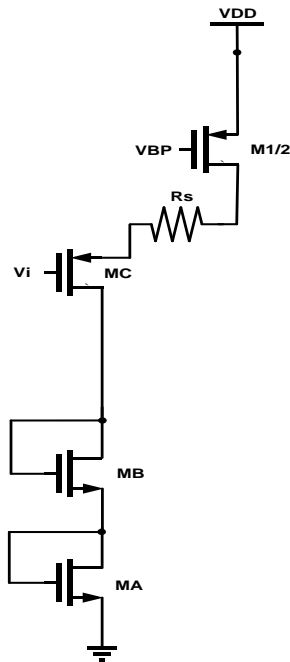


Figure 48 Bias circuit for the OTA

In order to make the current tuning a ratio of transistor sizes M2 and Mn (explained in section 2) needs to have the same overdrive. In order to bias the switched resistor Mn at the exact same V_{ov} we copy the same branch of the OTA and add a diode connected MB so that the overdrive voltage of M2 and Mn matches.

4.3 Common mode feedback circuit

There are many advantages for fully differential circuits over their single-ended counterparts such as greater output swings, better noise performance and avoiding mirror poles to achieve a faster speed. However for a high-gain differential circuit the output common mode voltage is quite sensitive to device properties and mismatches, thus we require common-mode feedback to have a properly defined output common mode voltage.

We can basically divide the task of the CMFB into three operations: sensing the output common mode level, comparison with a reference and returning the error to the amplifier's bias network.

A common mode feed-back circuit is a circuit sensing the common-mode voltage, comparing it with a proper reference, and feeding back the correcting common-mode signal (both nodes of the fully-differential circuit) with the purpose to cancel the output common-mode current component, and to fix the dc outputs to the desired level. The operation is as shown in Figure 49 and the circuit is shown in Figure 50.

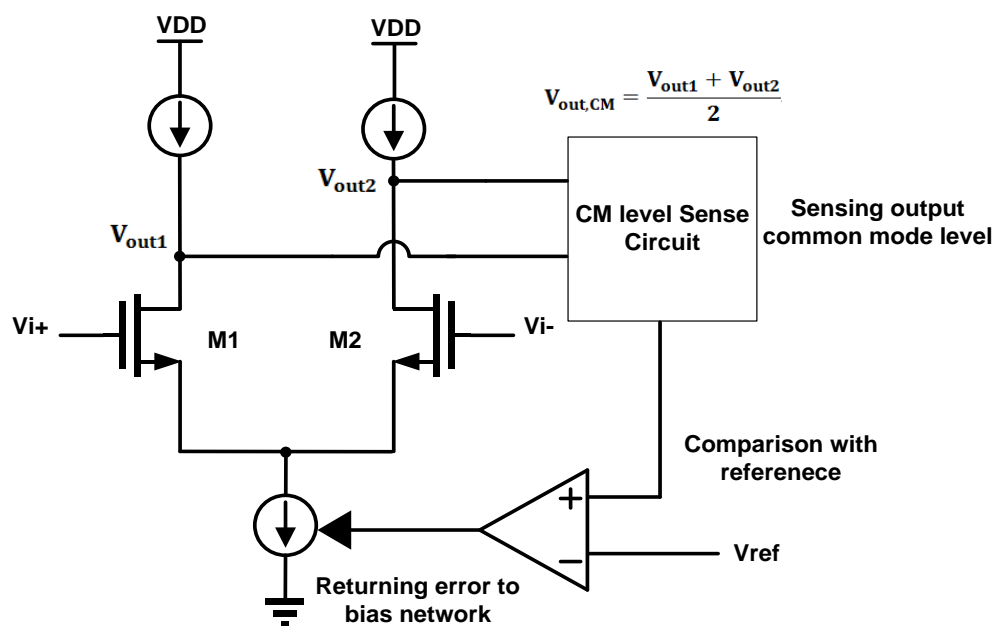


Figure 49 Common mode feedback concept for the OTA

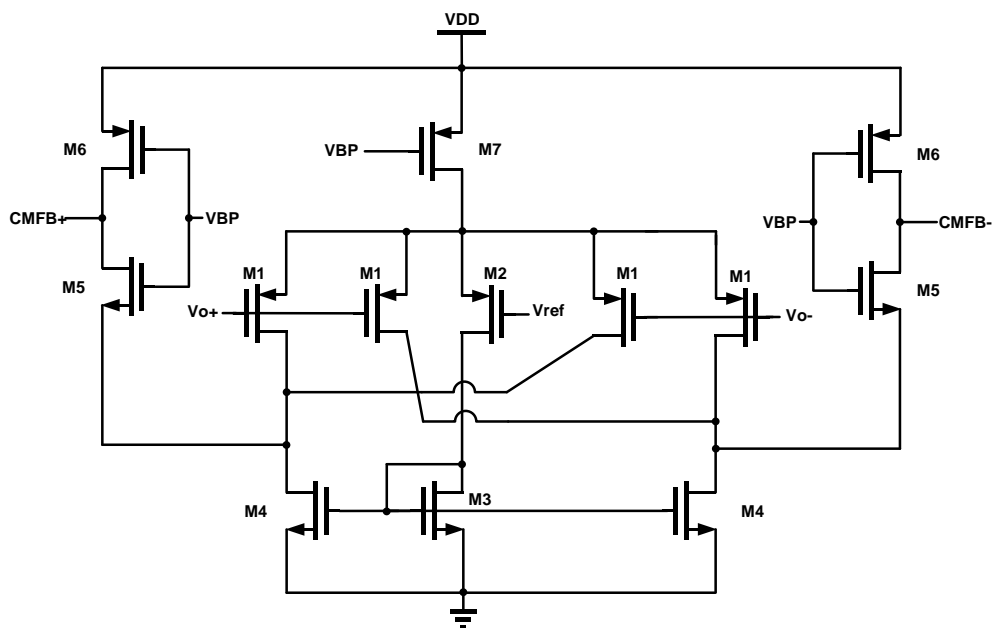


Figure 50 Common mode feedback circuit for the OTA

The main goal of the CMFB circuit is to adjust the common mode output voltage and let the differential mode stay the same, the circuit architecture was mostly adjusted from reference [26].

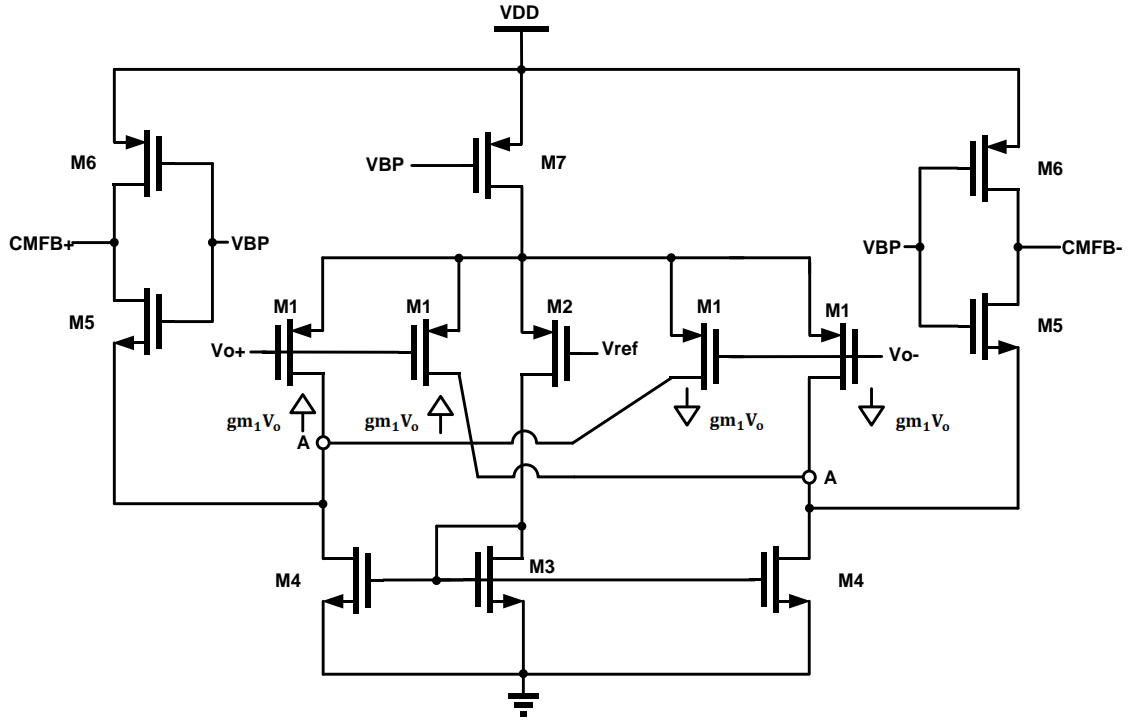
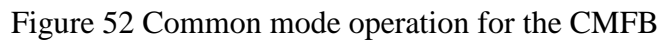


Figure 51 Differential operation for the CMFB

Figure 51 shows the differential operation, the detected output signal $g_{m1}V_o$ cancels each other at node A ($g_{m1}V_o - g_{m1}V_o = 0$), thus not generating additional differential signals to affect the operation of the OTA.



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Table 9 Transistor size for the CMFB circuit

| | M1 | M2 | M3 | M4 | M5 | M6 |
|------|-----------|-----------|---------|---------|-----------|-----------|
| W/L | 2.5u/400n | 2.5u/400n | 750n/1u | 750n/1u | 2.5u/400n | 2.5u/400n |
| N | 1 | 2 | 4 | 6 | 2 | 2 |
| Bias | 5u | 10u | 10u | 10u | 5u | 5u |

Table 9 shows the transistor size for Figure 50, the size of M2 is chosen to be 2 times M1 so that according to equation $g_m = \sqrt{2I_D u_n C_{ox} \frac{W}{L}}$ will result in $g_{m1} : g_{m2} = 1 : 2$. However, in the real implementation the current path that g_{m2} flows has more parasitic capacitance that will degrade the transconductance, therefore the current mirror M3 and M4 was made with a ratio 1:1.5 to boost up the lost transconductance. M5 and M6 size is chosen so that the current buffer resistance into the CMFB node is small enough.

4.3.1 Simulation setup and results

The simulation setup is as shown in Figure 53 and the simulation result is in Figure 54. A common mode current pulse of 15uA is injected into the output node (Figure 54.1). The output voltage node is plotted to see its respective common mode transient response $\frac{V_{o+} + V_{o-}}{2}$ (Figure 54.2), the differential mode transient response it also plotted $V_{o+} - V_{o-}$ (Figure 54.3)

The common mode transient resembles a phase margin larger than 60 which settles quite fast and the differential mode transient response is good which settles to zero. The CMFB circuit works properly with an input step voltage.

4.4 OTA characteristic

This section contains some analysis and simulations for the parameters of the OTA in Figure 47. With the circuit improvements we will see from the section that the linearity and output resistance will improve a lot which makes it a strong candidate for the application.

4.4.1 Output resistance

The output resistance is $R_o \approx r_{o3} / (g_{m4} r_{o4} r_{o5})$, from the equation the output resistance is independent of the switched resistor indicating it will remain the same output resistance for all tuning cases. This was done by putting additional current mirrors to act as a buffer. The simulation setup is same as described in section 3.5.2 and the simulation result is shown in Figure 55.

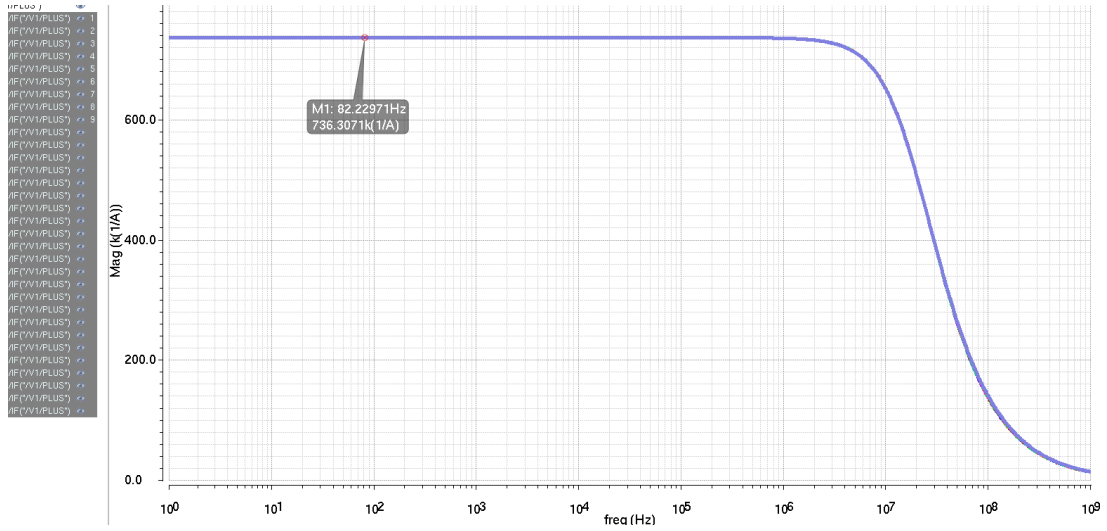


Figure 55 Output impedance with varying multiplication factor of switched resistor

As expected the output resistance remains the same with different multiplier factor of the switched resistor, the output resistance stays 736k Ohms which is suitable for our application.

4.4.2 Transconductance

The differential pair with source-degeneration for linearity improvement is used to produce the needed transconductance to obtain a particular coefficient in the filter. A bank of switched resistor working in triode region will be placed between the drains of the differential pair in order to tune the transconductance therefore changing the filter bandwidths. The switched resistor will have an effective resistance of R_{Triode} resulting in an effective transconductance of

$$G_m = \frac{g_m}{1 + g_m R_s} \times \frac{R_{Triode}}{R_{Triode} + \frac{1}{g_m}}$$

With proper bias of $V_{control}$, G_m will reduce to

$$G_m = \frac{\frac{W}{L}_{PMOS}}{\frac{W}{L}_{PMOS} + 2 \frac{W}{L}_{triode}}$$

which is a ratio of transistor sizes and can be matched greatly through proper layout techniques.

4.4.3 Linearity

By adding source degeneration resistance we can increase the linearity. Using the same calculations in appendix B, we get $H_{D3} = \frac{1}{32} \frac{1}{(1+g_m R)^2} \frac{V_{in}^2}{(V_{GS}-V_T)^2}$, normally $1 + g_m R$ is around 1.5-3 in practice since there is a tradeoff between linearity and voltage headroom. Figure 56 shows the simulation result of the linearity.

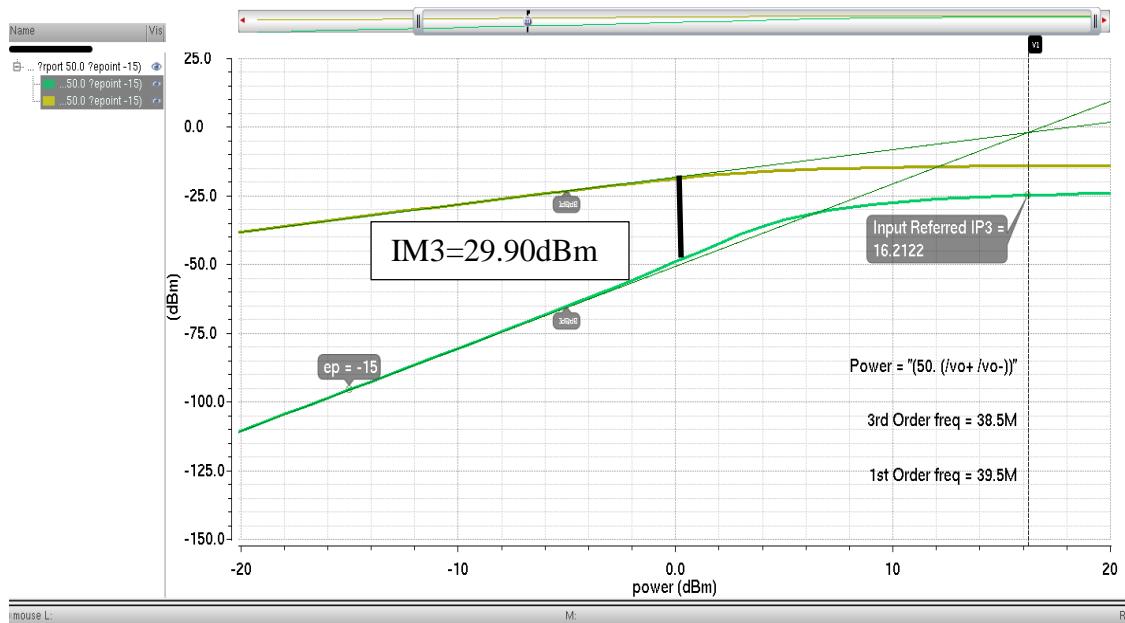


Figure 56 IIP3 simulation of the OTA

IIP3 is related to V_{dsat} of the input transistor, normally a large V_{dsat} results in better linearity. In Figure 56 for a power of 0dBm IM3=29.98dBm resulting in an IIP3 of 16.21dBm. For the simulation we've added a resistor of 100 Ohms in parallel with the output to make sure that the output swing does not saturates due to high gain.

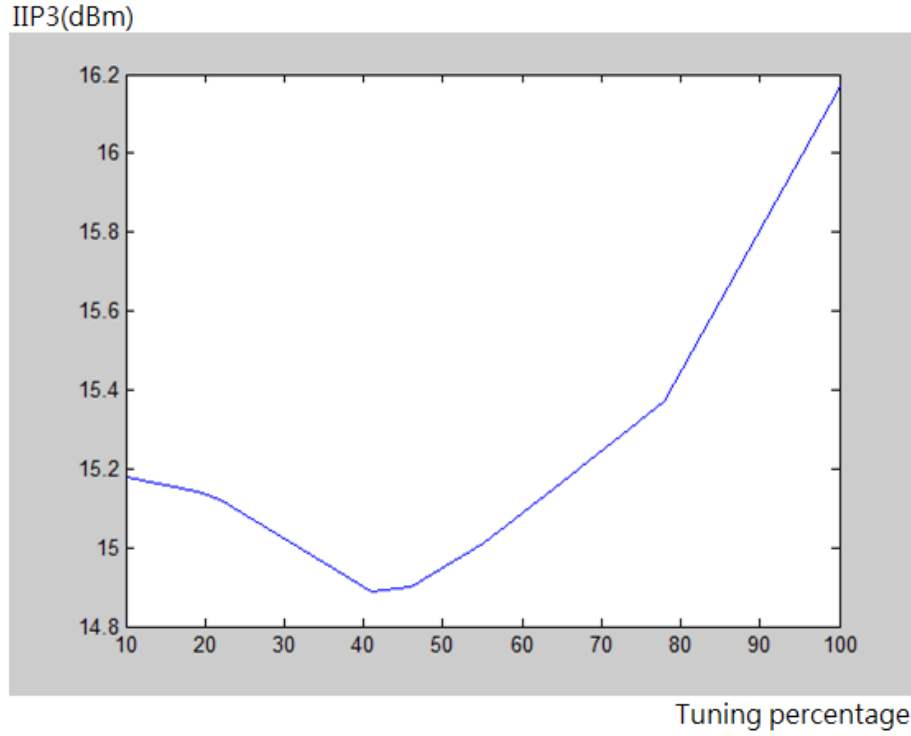


Figure 57 IIP3 simulation of the OTA with varying the tuning percentage of g_m to g_{max}

Figure 57 shows for different tuning percentage relative to the maximum transconductance, IIP3 is about the same for each cases. With different tuning there is only a minor difference in the parasitic capacitance at the mirroring node, the input overdrive voltage for all case is still the same resulting similar IM3 for different tunings. The largest difference is about 1dbm as shown in the simulation.

4.4.4 Changing the polarity of the OTA

In the FIR filter we need to have negative coefficients according to Table 2. This can be done by switching the output nodes, input nodes or at the current source. The best place to place it is at the low resistance node since it will not be a large pole and will not

current mirrors at the bot are used for coarse tuning and acting as an output buffer to keep the same output resistance while operating different bandwidths. Table 10 shows the summary of simulation results of the circuit in Figure 58.

Table 10 Calculated and simulation result comparison

| | Calculated | Simulated |
|----------------------|----------------------------------|------------------------------------|
| DC gain | 650k Ohm | 732k Ohm |
| Linearity (IIP3) | 18.6dBm | 16.212dBm |
| Noise(Spot noise) | $18 \text{ nV}/\sqrt{\text{Hz}}$ | $40.8 \text{ nV}/\sqrt{\text{Hz}}$ |
| In/Output CM voltage | 0.6V | 0.6V |
| Power | 300uW | 316uW |

5. CURRENT INTEGRATION OF THE OTA

The purpose of the OTA is to pump different currents into the capacitor depending on the bandwidth requirements. This section shows the simulation result of the OTA step response in time domain and frequency response of the FIR filter. During the analysis we made improvements on the circuit to improve its time domain response. A design consideration of the switches from OTA to the capacitor were also discussed to have a better frequency response of the filter. In the end, schematic simulation results in CADENCE are presented to demonstrate the feasibility of the proposed approach.

5.1 Step response in time domain

An important characteristic of the dominant pole frequency response vs time domain response for current integration is analyzed here. Assuming an OTA with an open loop gain of A_0 and a dominant pole of ω_p , the frequency response is $F(s) = \frac{A_0}{1+s/\omega_p}$, the output time domain response for a step input $V_{in} = au(t)$ can now be expressed as $V_{out}(t) = A_0(1 - \exp\frac{-t}{\tau})u(t)$ where $\tau = 1/\omega_p$ the time constant τ plays a huge role in current integration since a small τ means the capacitor will be charged fast to its ideal value.

A test for the step response is important as it indicates how fast the OTA responds from a sudden input voltage. The system cannot act until the output current settles down to the vicinity of its final state, delaying the overall system response.

Formally, knowing the step response of a dynamical system gives information on the stability of the system, and its ability to reach one stationary state when starting from another. Figure 59 shows the test bench and Figure 60 shows the comparison of the current integrated into the capacitor with an ideal current source.

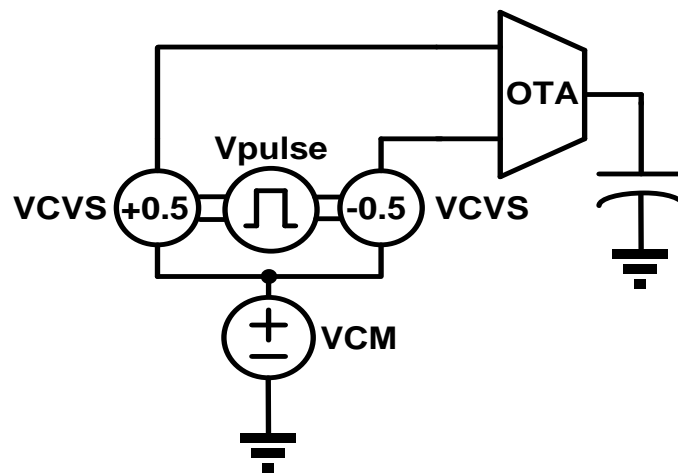


Figure 59 Test bench for the step response for the OTA

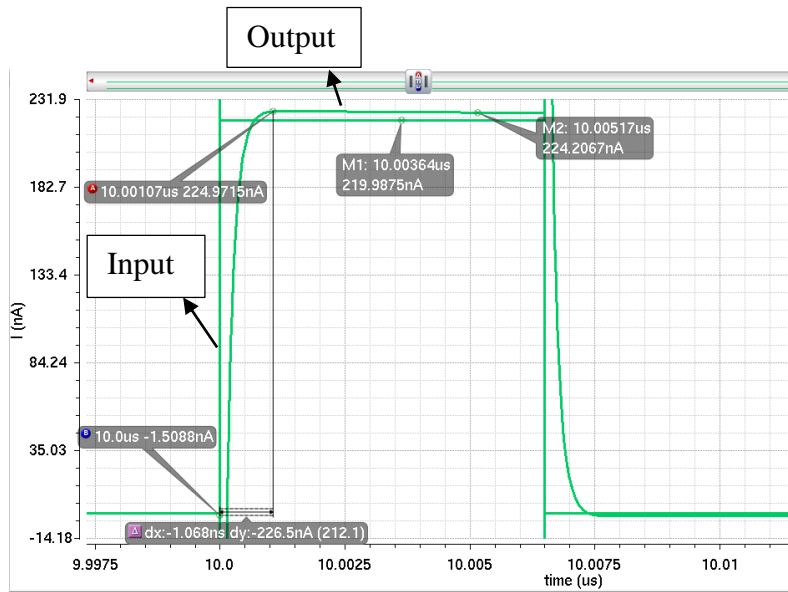


Figure 60 Output step response in time domain

Injecting a unit step voltage at the input we can see from Figure 61 that there is a rise time about 1ns which is caused by the node from mirroring the current to the output (Dominant pole location). To optimize this we need to minimize the capacitor at the mirroring node from Figure 58. Figure 61 shows the voltage when the current is being integrated into the capacitor.

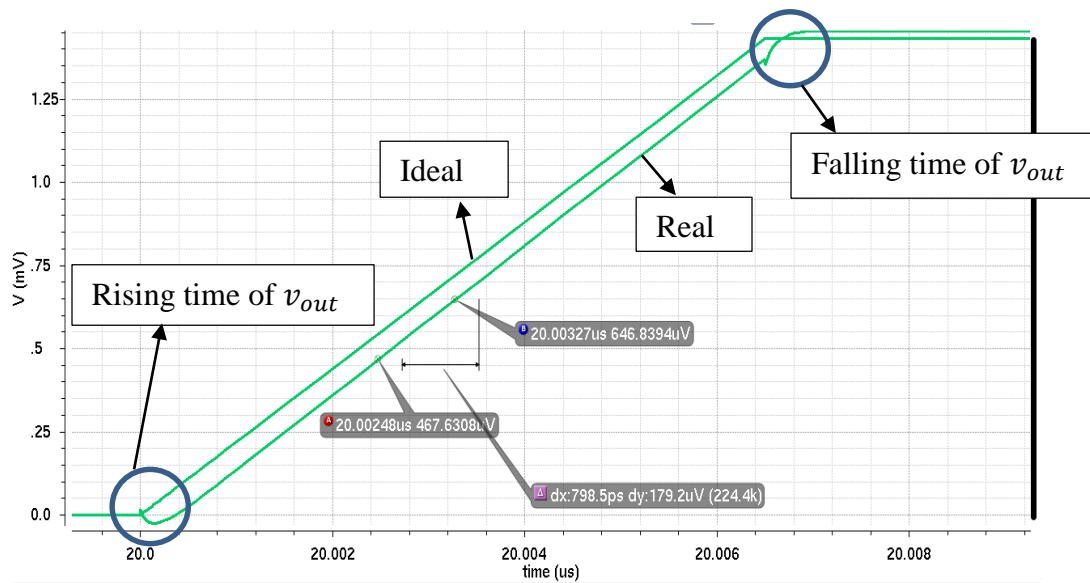


Figure 61 Voltage being integrated by the capacitor

Looking at the voltage being integrated by the capacitor, during the rising time and falling time the current integration is not perfectly linear since the current is changing every time. The two transition point cannot change abruptly indicating that the high frequency signals cannot pass through.

As we will see in the simulation results later in the section this pole will cause the integrated current to be less than expected and can cause a problem to the FIR frequency response.

5.2 128 tap FIR filter response in frequency domain

The application demands different bandwidth for different detected target locations, we simulated 3.5M, 15M and 30M Hz bandwidth to see how well we

designed. To simulate the FIR filter frequency response we inject sinusoid tones within the filter frequency range with 0dB in power, the spacing of the tones are around 1~3MHz depending on the resolution you want. The simulation results was on the schematic level with putting a spectrum of frequency tones at the input passing through the filter to see its shape. Figure 62,63 and 64 shows the FIR filter response with 3.5M, 15M, 30M bandwidth respectively.

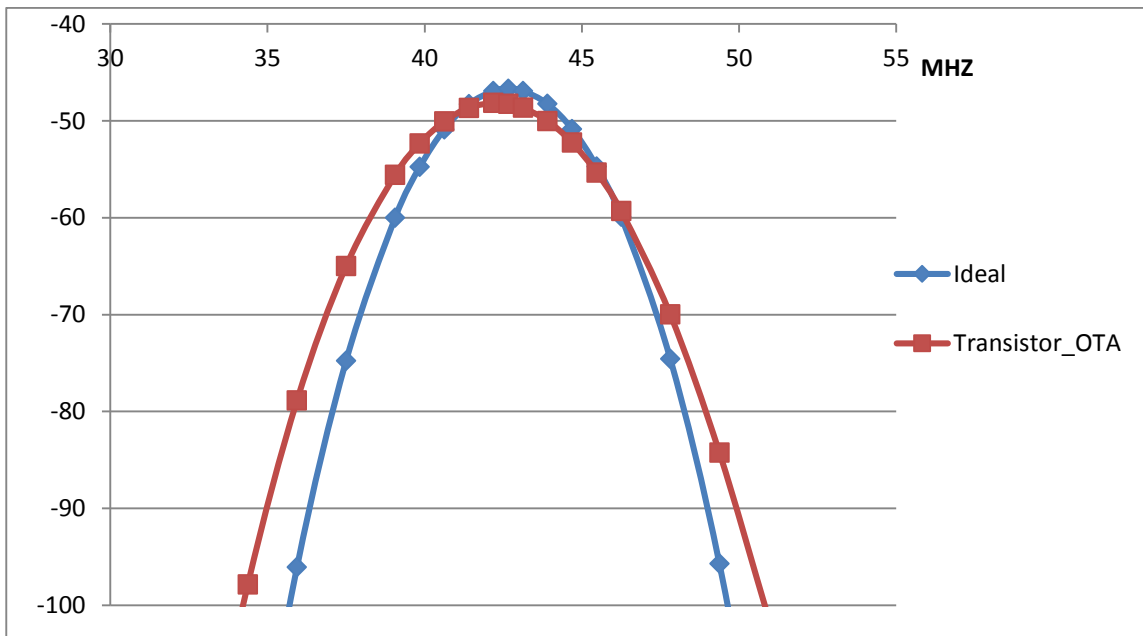


Figure 62 FIR filter response for 3.5MHz bandwidth

The 3dB BW is around 3.28MHz. There is about 2dB loss in the pass band due to the small errors in the implemented OTA, as for the stop band it provides enough attenuation for the specification.

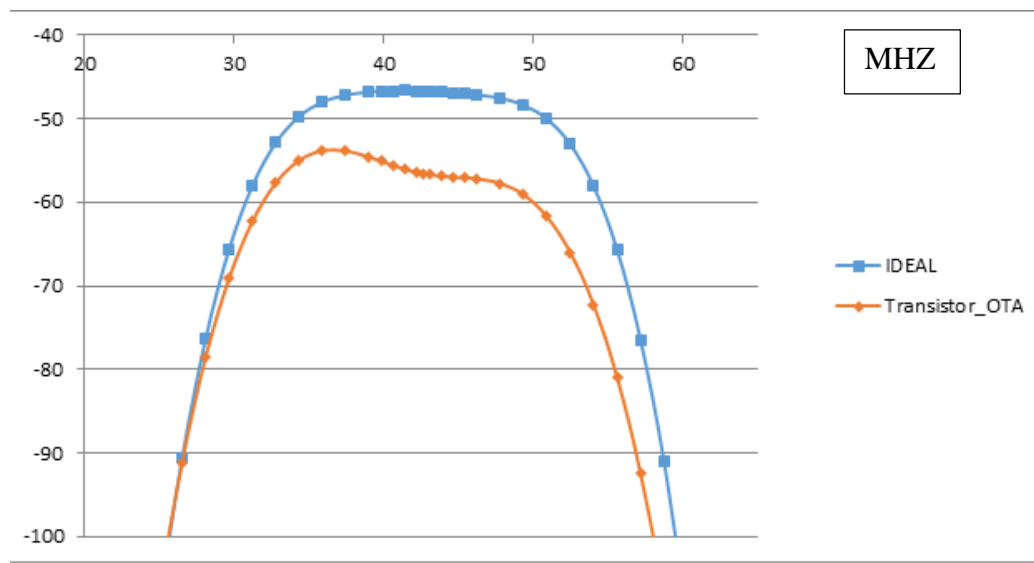


Figure 63 FIR filter response for 15MHz bandwidth

For the 15MHz bandwidth the filter response at the high frequency drops around 8db which is quite large.

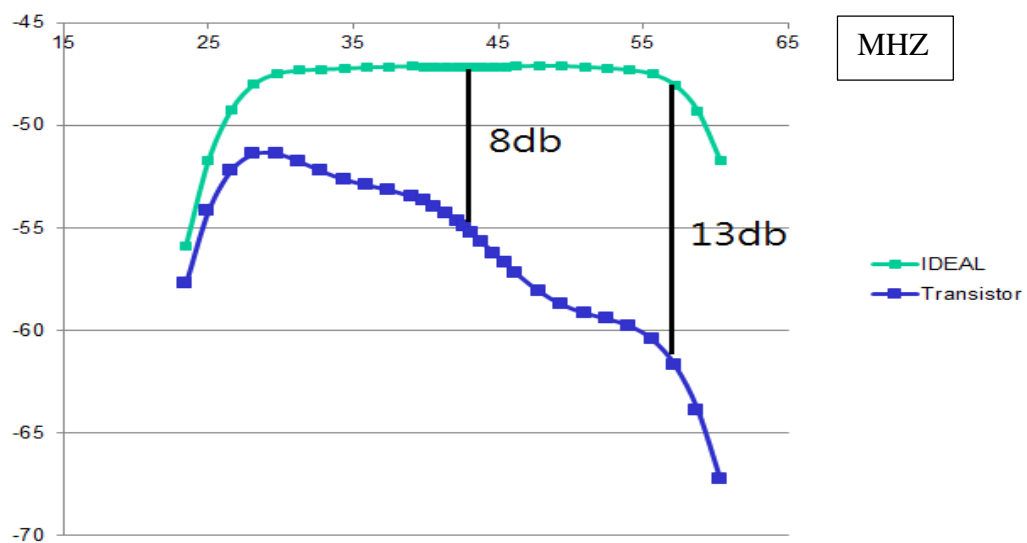


Figure 64 FIR filter response for 30MHz bandwidth

For the 30MHZ bandwidth the filter response at the high frequency drops from 8db to 13dB and increases for higher frequencies.

5.3 Conclusion and improvement

We can clearly see that the higher the bandwidth extend the higher the degradation at high frequency gets. The reason for the high frequency degradation is caused by the poles of the OTA, which does not allow the high frequency components to pass through. In a time domain perspective, the current integration is reduced during the rising and falling edges, so any small errors in it was cause a huge difference between the ideal current integration and the real integration.

To overcome this problem we have several possible solutions. First, we can simply push the dominant pole even farther to reduce the rising and falling time, however more advance technology will be needed to minimize the parasitic capacitance to operate at a faster speed. Second, we could increase the total time of the integration current so that the errors will be negligible, but due to the specification for the frequency center point we have the time is fixed. Lastly, we can somehow boost the current in the transition phase so that it can recover the loss of the current.

In the next section we will overcome this problem with a small change for the OTA.

5.4 High frequency compensation

As shown in Figure 65, a capacitor was added in parallel to the degeneration resistor to increase the high frequency response, this results in having a better current integration in a fixed time window time. Table 11 shows the transistor sizes implemented in Figure 65.

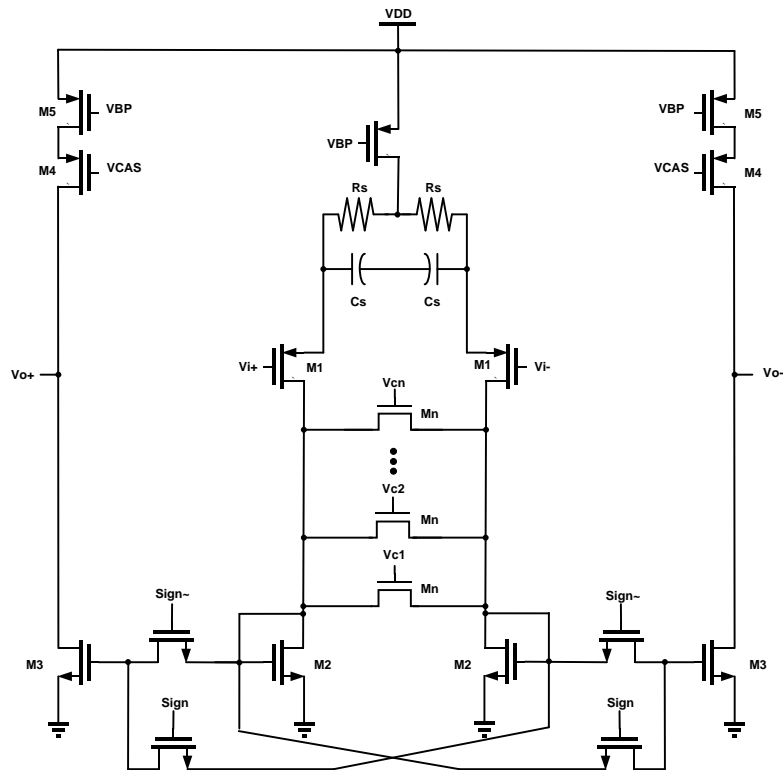


Figure 65 Complete schematic for the OTA with high frequency compensation

Table 11 Transistor size for the final OTA

| | M1 | M2 | M3 | M4 | M5 | MN | Msign |
|-------|-------|---------|---------|-----------|-----------|-----------|------------|
| W/L | 2u/1u | 750n/1u | 750n/1u | 2.5u/0.4u | 2.5u/0.4u | 220n/0.8u | 220n/0.18u |
| N | 8 | 4 | 4 | 4 | 4 | 1 | 1 |
| | Rs | | Cs | | | | |
| Value | 4kOhm | | 640f | | | | |

To see it intuitively, currents were originally being lost during the transition phases (high frequency components), by adding capacitor in parallel with the degeneration resistor the transition phases will short the capacitors which will act like an OTA without the source degeneration boosting the transconductance.

5.4.1 Compensation analysis and improvements

As shown in Figure 66, the new gm frequency response without the output pole is $\frac{g_m}{1+g_m(R_s//sC_s)} = \frac{g_m(1+sR_sC_s)}{(1+g_mR_s)+sR_sC_s}$. A left half plane pole at $\frac{1+g_mR_s}{R_sC_s}$, and a left half plane zero at $\frac{1}{R_sC_s}$, the left half plane zero can boost the high frequency response which is desirable for our application.

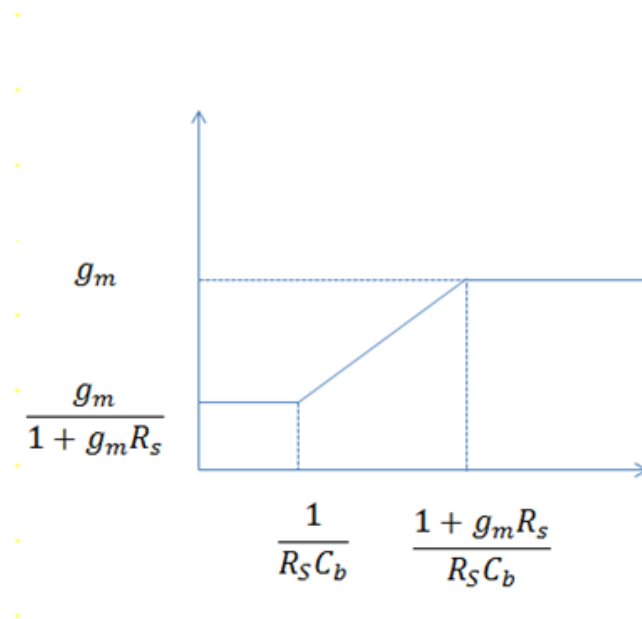


Figure 66 Theoretical frequency response with high frequency compensation

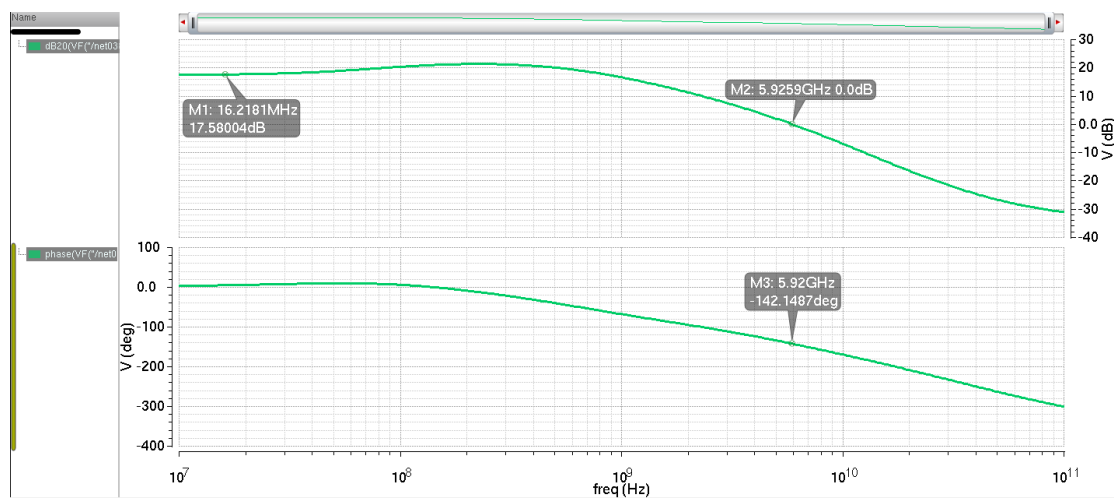


Figure 67 Simulated frequency response with high frequency compensation

We can see the left half plane zero in the simulation will boost the high frequency response. The pole at the output was omitted in the analysis but is shown in Figure 67.

Figure 68 shows the time domain response with adding degeneration capacitors, the added capacitor causes the current integration to be more effective having a small boost resulting for the compensation of the lost current.

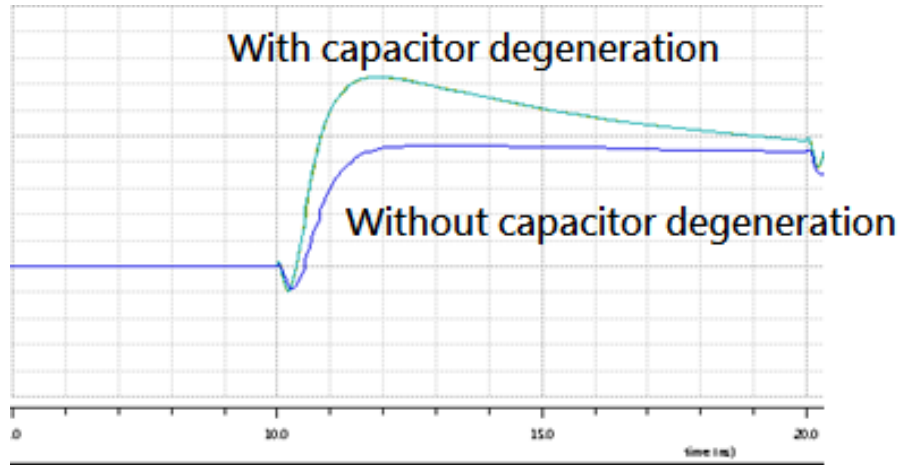


Figure 68 Current integration comparison in time domain

From Table 2, implementing one OTA for all the tuning range is nearly impossible. Taking a look at the row of the table we noticed there is around five possible ranges. Starting from largest to smallest we have 90uA to 20uA, 20uA to 4uA, 11uA to 1.2uA, 6.6uA to 0.7uA and 2.6uA to 0.2uA. Table 12 is a comparison of the G_m needed simulated in matlab labeled as I(Ideal) and the ones in transistor level design labeled as R(Real), the digital code are also listed for the needed current.

Table 12 Transconductance tuning implemented for the OTA

| Gm | 3.5 | 4 | 6 | 8 | 10 | 12 | 15 | 20 | 25 | 30 |
|-------------|------------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 1I | 1.380 | 0.091 | 0.484 | 0.300 | 0.030 | 0.339 | 0.442 | 0.170 | 0.442 | 0.248 |
| 1R | 1.472 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| code | 000011 | | | | | | | | | |
| 2I | -0.210 | -0.032 | -0.073 | -0.070 | 0.026 | -0.025 | -0.072 | 0.020 | -0.067 | 0.023 |
| 2R | -0.277 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| code | 111111 | | | | | | | | | |
| 3I | -2.680 | -0.687 | -0.876 | -1.050 | 0.742 | 0.135 | -0.742 | 0.827 | -0.382 | 0.960 |
| 3R | -2.6 | 0.7665 | -0.912 | -1.008 | 0.7665 | 0.2779 | 0.7665 | 0.833 | -0.375 | 1.008 |
| code | 100000 | 101001 | 100111 | 100110 | 001001 | 011111 | 101001 | 001000 | 110110 | 000110 |
| 4I | 1.150 | 0.414 | 0.295 | 0.480 | -0.456 | -0.274 | 0.120 | -0.479 | -0.177 | -0.425 |
| 4R | 1.126 | 0.407 | 0.304 | 0.491 | -0.467 | -0.277 | 0.277 | -0.467 | -0.277 | -0.426 |
| code | 000101 | 010100 | 011100 | 010000 | 110001 | 111111 | 011111 | 110001 | 111111 | 110011 |
| 5I | 4.490 | 2.107 | 0.663 | 1.720 | -2.080 | -1.814 | -0.595 | -1.608 | -1.863 | -0.419 |
| 5R | 4.353 | 2.148 | 0.730 | 1.713 | -2.148 | -1.837 | -0.730 | -1.605 | -1.837 | -0.730 |
| code | 000010 | 001000 | 011111 | 001011 | 101000 | 101010 | 111111 | 101100 | 101010 | 111111 |
| 6I | -3.180 | -1.837 | 0.000 | -0.900 | 1.437 | 1.603 | 1.190 | 0.396 | 1.523 | -0.993 |
| 6R | -3.243 | -1.837 | 0 | -0.913 | 1.425 | 1.605 | 1.220 | 0.730 | 1.510 | -0.984 |
| code | 100100 | 101010 | | 111000 | 001110 | 001100 | 010001 | 011111 | 001101 | 110110 |
| 7I | -6.480 | -4.449 | 1.170 | -0.790 | 2.271 | 3.269 | 3.567 | -1.412 | 1.749 | -3.623 |
| 7R | -6.620 | -4.353 | 1.164 | -0.798 | 2.346 | 3.243 | 3.717 | -1.425 | 1.713 | -3.243 |
| code | 10000 | 100010 | 010010 | 111100 | 000111 | 000100 | 000011 | 101110 | 001011 | 100100 |
| 8I | 6.600 | 5.219 | -2.548 | -0.670 | -1.012 | -2.503 | -3.897 | 3.595 | 1.034 | 2.738 |
| 8R | 6.620 | 5.253 | -2.584 | -0.730 | -1.024 | -2.584 | -3.717 | 3.717 | 1.024 | 2.876 |
| code | 000000 | 000001 | 100110 | 111111 | 110101 | 100110 | 100011 | 000011 | 010101 | 000101 |
| 9I | 7.920 | 7.052 | -4.814 | -2.950 | 1.035 | -0.976 | -3.544 | 5.616 | 4.818 | -0.879 |

Table 12 Continued

| Gm | 3.5 | 4 | 6 | 8 | 10 | 12 | 15 | 20 | 25 | 30 |
|-------------|------------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 9R | 7.339 | 7.339 | -4.839 | -3.087 | 1.224 | -1.224 | -3.610 | 5.459 | 4.839 | -1.224 |
| code | 000010 | 000010 | 100101 | 101010 | 011111 | 111111 | 001000 | 000100 | 000101 | 111111 |
| 10I | 11.220 | 11.013 | 9.356 | 7.570 | -5.417 | -2.805 | 1.182 | -6.586 | -9.266 | 8.074 |
| 10R | 11.200 | 11.200 | 8.865 | 7.339 | -5.459 | -2.879 | 1.224 | -6.261 | -8.865 | 7.339 |
| code | 100000 | 100000 | 000001 | 000010 | 100100 | 101011 | 011111 | 100011 | 100001 | 000010 |
| 11I | -7.930 | -8.426 | 8.344 | 7.820 | -6.928 | -5.605 | -3.255 | -0.996 | -4.703 | 7.542 |
| 11R | -7.339 | -8.865 | 8.865 | 7.339 | -7.339 | -5.459 | -3.328 | -1.224 | -4.839 | 7.339 |
| code | 100010 | 100001 | 000001 | 000010 | 100010 | 100100 | 101001 | 111111 | 100101 | 000010 |
| 12I | 16.180 | 18.299 | 20.229 | 20.750 | 20.495 | 19.367 | 16.749 | 10.206 | -2.556 | -7.176 |
| 12R | 16.587 | 18.327 | 20.451 | 20.451 | 20.451 | 20.451 | 16.587 | 10.434 | -4.070 | -7.167 |
| code | 000010 | 000001 | 100000 | 100000 | 000000 | 000000 | 000010 | 101000 | 111111 | 101111 |
| 13I | 5.960 | 7.072 | -8.453 | -9.200 | 9.685 | 9.917 | 10.000 | -9.210 | -7.720 | 4.928 |
| 13R | 6.047 | 7.167 | -8.296 | -9.251 | 9.809 | 9.809 | 9.809 | -9.251 | -7.995 | 4.878 |
| code | 010011 | 001111 | 101100 | 101010 | 001001 | 001001 | 001001 | 101010 | 101101 | 011001 |
| 14I | 20.060 | 24.606 | 30.996 | 25.010 | 38.328 | 41.082 | 44.814 | 48.505 | 50.469 | 49.657 |
| 14R | 20.523 | 24.498 | 30.381 | 25.315 | 37.983 | 42.207 | 44.693 | 50.659 | 50.659 | 50.659 |
| code | 111101 | 110111 | 010001 | 010110 | 101100 | 101010 | 101001 | 000111 | 000111 | 100111 |
| 15I | -2.220 | -2.782 | 3.613 | 4.170 | -4.659 | -5.116 | -5.808 | 6.772 | 7.674 | -8.592 |
| 15R | -2.266 | -2.879 | 3.610 | 3.944 | -4.839 | -4.839 | -5.459 | 6.261 | 7.339 | -8.865 |
| code | 101111 | 101011 | 001000 | 000111 | 100101 | 100101 | 100100 | 000011 | 000010 | 100001 |
| 16I | 21.530 | 27.125 | 35.569 | 41.300 | 46.498 | 51.449 | 59.121 | 70.491 | 81.860 | 94.870 |
| 16R | 21.697 | 27.124 | 36.173 | 39.984 | 47.489 | 50.659 | 58.462 | 69.108 | 84.495 | 95.081 |
| code | 011011 | 010100 | 101101 | 101011 | 001000 | 000111 | 000101 | 100011 | 100001 | 000000 |

5.5 Simulation results for different bandwidths

Figure 69,70 and 71 shows the frequency response of 3.5M, 15M, 30M bandwidth respectively, process corners for fast, normal and slow are also shown.

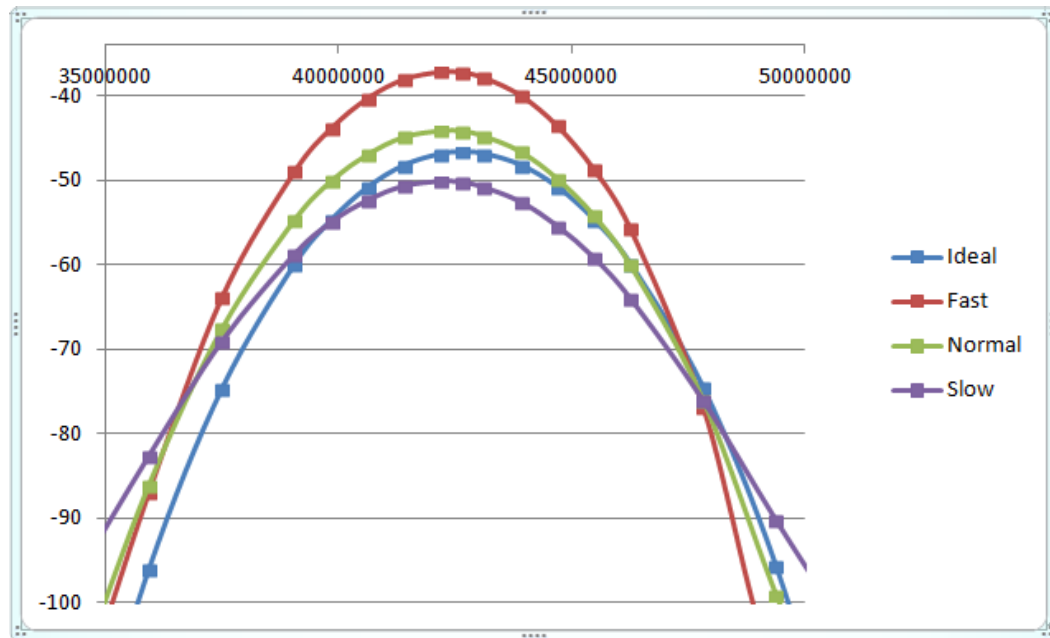


Figure 69 3.5MHZ bandwidth with different process corners

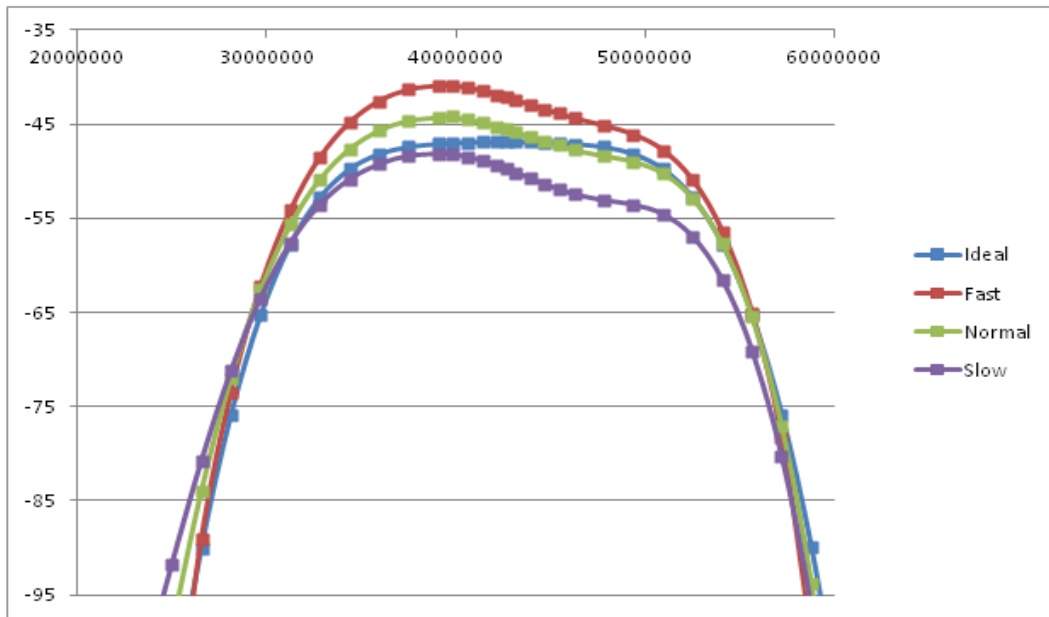


Figure 70 15MHZ bandwidth with different process corners

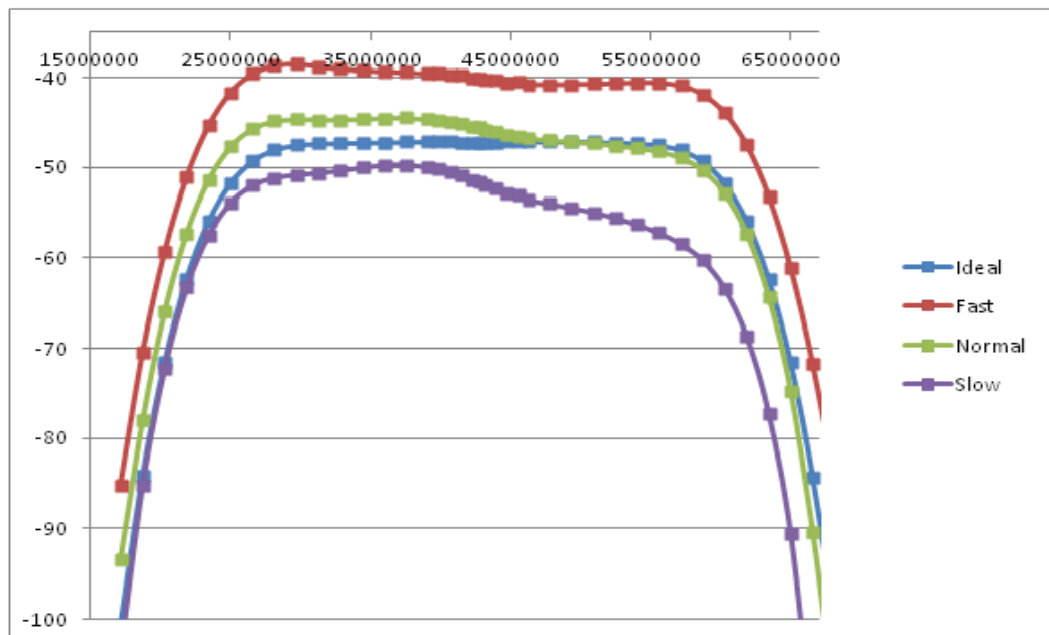


Figure 71 30MHZ bandwidth with different process corners

The frequency response is much better compared to section 5.2, especially at high frequency the degradation is not as severe. An important result of these figures is that with different process corners the shape remains almost the same with only shifting in the amplitude. In a slow process g_m is normally smaller and the FIR amplitude is determined by g_m/C this results in amplitude changes with different process. However, this is not a major problem since it's the shape that matters most. The shape of the transfer function is a ratio of g_m 's which makes it reliable even with temperature or process variation.

The simulation of the FIR filter time domain response is shown in Figure 72, bandwidths of 3.5M, 15M and 30M were simulated together for analysis. An important discover is the peaks of the three filters overlap each other during the simulation meaning the time delay (group delay) between them is small.

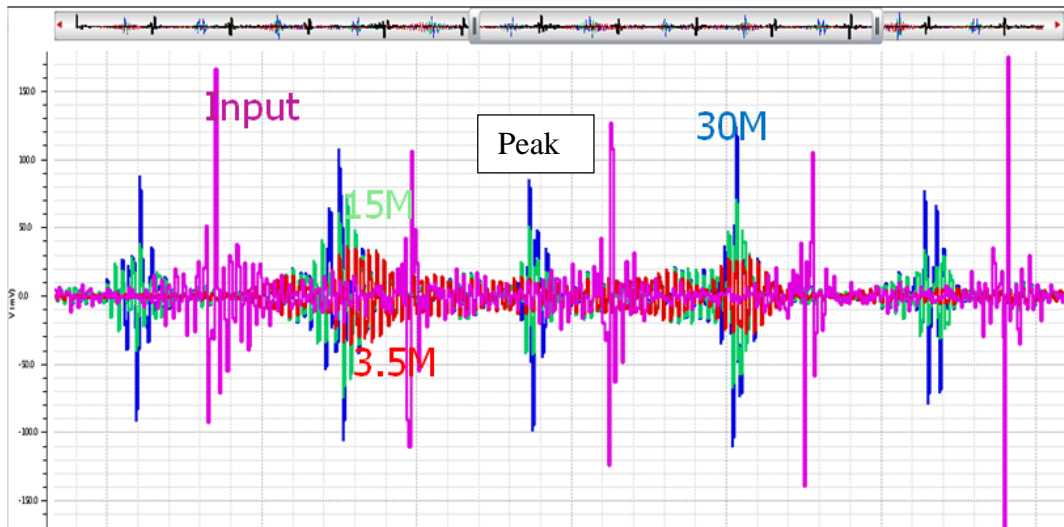


Figure 72 Time domain response of the FIR filter with different bandwidths

5.6 Non-ideality of the analog switch

Another important aspect is the non-ideality of the analog switches.

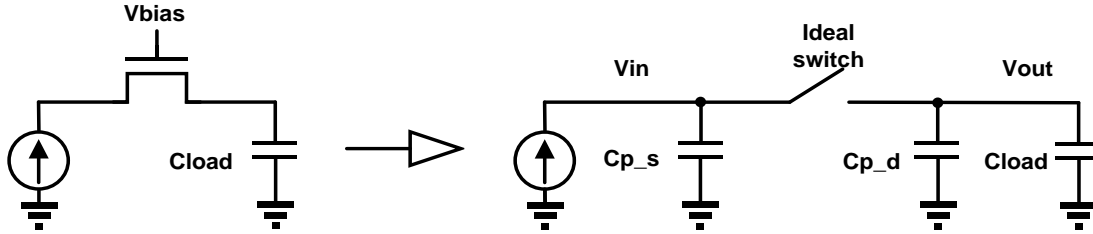


Figure 73 Conceptual view for the non-ideality of the switches

As Shown in the Figure 73, the OTA (simplified with a current source) will have to pump current to Cload at each clock cycle, in order to do this we need analog switches that corresponds to different clock cycles. Using charge conservative equation

$$V_{out} = \frac{C_{p_s}}{C_{p_s} + (C_{p_d} + C_{load})} V_{in} = \frac{1}{1 + \frac{(C_{p_d} + C_{load})}{C_{p_s}}} V_{in}$$

which corresponds to an error about $\frac{C_{p_s}}{(C_{p_d} + C_{load})}$, for $C_{p_d} + C_{load} = 2p$ and $C_{p_s} = 0.1p$

this corresponds to an error of 5%. Notice how C_{p_d} is actually good and what we need to do is minimizing C_{p_s} .

A simple layout technique can help which is shown in Figure 74.

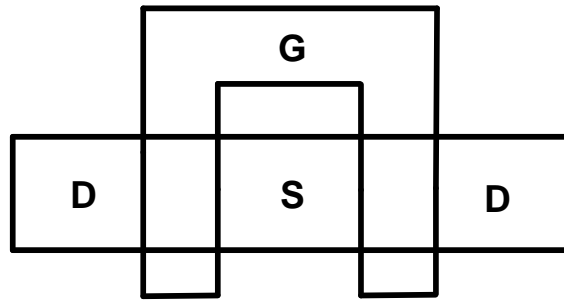


Figure 74 Proper layout technique for the switch design

By using even number of fingers and placing the source at the middle we can minimize the parasitic capacitance for the source. The NMOS switch was used which has a small capacitance to reduce the charge sharing effect. Figure 75 shows the filter frequency response when the NMOS switch was taken into account.

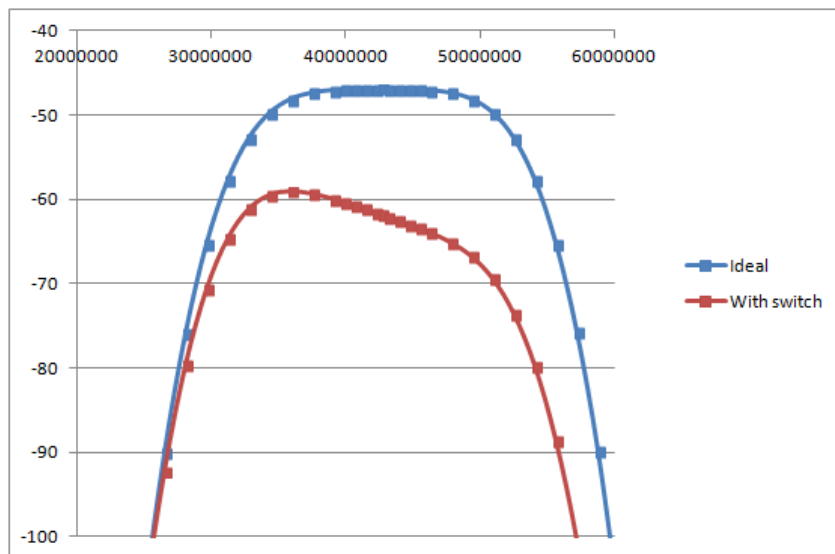


Figure 75 FIR filter response degradation due to charge sharing effect

Due to the charge sharing effects the frequency response at the high frequency drops quite a lot. There is a tradeoff between the switch resistance and the parasitic capacitance, for a reasonable switch resistance we want to make the capacitance at the left side as small as possible. We can also increase the load capacitance to minimize this effect but it is limited by the chip size. After some simulations we decided to have a load of 2pF and a switch size that corresponds to 1k ohm which corresponds to $W=10\mu$ and $L=180\text{nm}$.

6. LAYOUT OF THE OTA

For transistor layout, methods such as interdigitation, common centroid and dummy insertion layout techniques are used to reduce mismatch by ensuring that the two halves of the differential structure will be similarly affected by process variations. A common layout technique known as gate splitting is also used to reduce gate resistance. To ensure proper body contact and to minimize the substrate noise coupling, several body contacts are placed close to each transistor. Multiple via connections are used to ensure connectivity and to reduce the parasitic resistance of the via. Also, to reduce the IR drops, the pad connections are routed by wide traces on the top metal layer, which has lower sheet resistance [27]. Figure 76 shows the layout of a section of the 32-tap FIR filter.

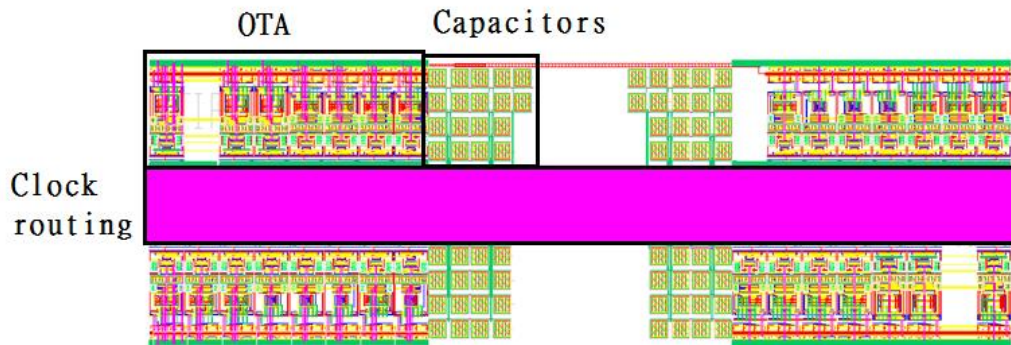


Figure 76 Layout of the 32-tap FIR filter

One of the most important part of the layout is the floor plan of clock routing and the output routing. The vertical and horizontal clock routing is done by metal 1,2 respectively. The vertical and horizontal of the output routing is done by metal 4,5 respectively. Metal 3 is added at the middle of both routing and connecting it to ground to act like a shield so the crosstalk is less severe, this effective solution can increase the signal impurity, the cross section of the layout can be seen in Figure 77.

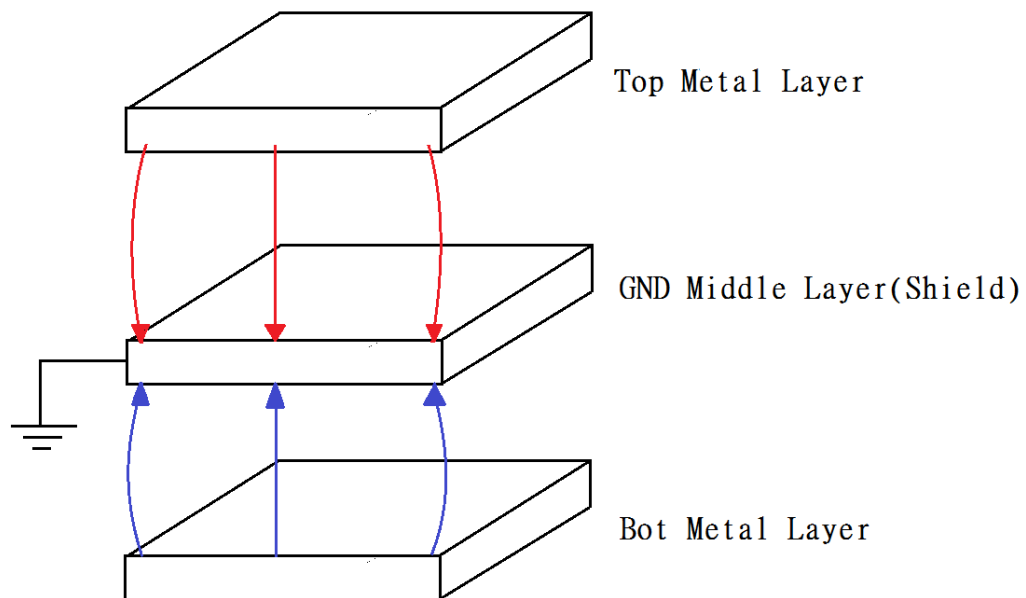


Figure 77 Layout for the metal layers

At last Figure 78 shows the complete layout for the entire chip, including the anti-aliasing filter, multiplexer and frequency synthesizer which are notated in the figure. The chip is size 3mm×2mm.

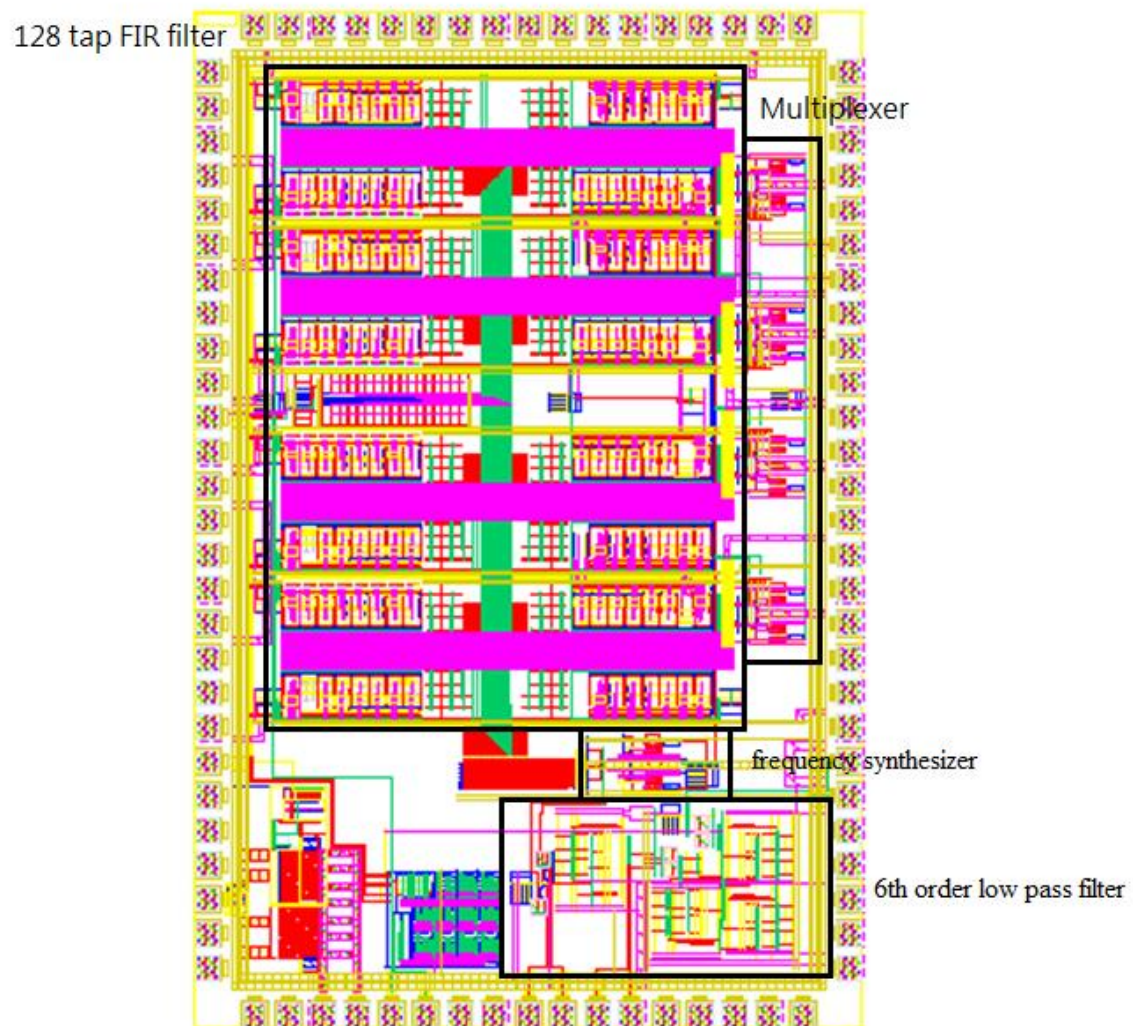


Figure 78 Layout of the entire chip

7. SUMMARY AND CONCLUSIONS

The analog FIR filter is a suitable architecture when a low resolution ADC is needed, as it processes the signals in analog domain before going to digital domain. In this radar application the ADC can be relaxed by 2~3 bits with the analog FIR filter. The design of tunable transconductance operational amplifier results in low speed when using current mirror tuning due to the extra capacitance created at the dominant pole. Gilbert based OTA is also not a suitable architecture for the application since linearity varies when tuning the transconductance and needs to work with a high VDD due to its large voltage headroom. To overcome the low speed and linearity issues, a novel method of a P-type input folded cascade OTA with switched resistor was proposed in this thesis. Also, a current mode CMFB circuit was used to achieve a fast settling response for the output. The design was then characterized to accommodate for temperature and process variation, simulations were also done to prove the design was reliable. Finally, the impact of the nonidealities of the switches can cause to the FIR filter frequency response was analyzed. The circuit design was done in TowerJazz 180nm CMOS technology.

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APPENDIX

Appendix A: Background for nonlinearity

Distortion is important in communication systems, in which many frequency channels have to be processed. Since it can affect the purity of the output signal, we need to know which distortion levels correspond with a certain signal level since distortion levels will always increase for increasing input amplitudes. Nonlinear distortion is generated by a nonlinear transfer curve as shown in Figure 79.

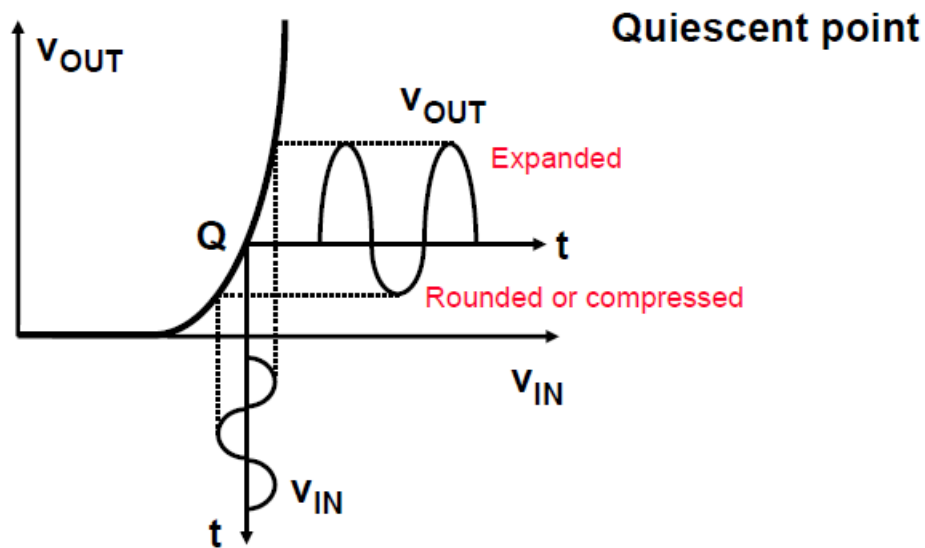


Figure 79 Non-linearity transfer function

The output voltage is biased at a quiescent point Q , an input sinewave will result in an output waveform which is distorted. Let's say the transfer function is $= a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + \dots$. Coefficient a_0 gives the DC output voltage in quiescent

point, coefficient a_1 gives the small signal gain. $a_{2,4,6...}$ represents the even-order nonlinearities and $a_{3,5,7...}$ represents the odd-order nonlinearities. Usually the odd-order is more important since we can cancel the even-order distortion by using a differential structure.

For any nonlinear transfer function, the coefficients can be easily found by taking derivatives. $a_0 = y @_{u=0}$, $a_1 = \frac{dy}{du} @u = 0$, $a_2 = \frac{1}{2} \frac{d^2y}{du^2} @u = 0$, $a_3 = \frac{1}{6} \frac{d^3y}{du^3} @u = 0$

Once the nonlinearity has been described by a power series, the harmonic distortion can easily be calculated with substituting $V_{in} = U \cos \omega t$, and taking the ratio of the component at $3\omega t$ over ωt .

$$HD_3 = \frac{1}{4} \frac{a_3}{a_1} U^2$$

A more important characteristic is the intermodulation distortion where it takes place when you have two adjacent channel frequencies, these two fundamental frequencies will generate all intermodulation products in a nonlinear system, and this is common in communication systems. With substituting $V_{in} = U(\cos \omega_1 t + \cos \omega_2 t)$ and finding $IM_2 @ \omega_1 \pm \omega_2$, $IM_3 @ 2\omega_1 \pm \omega_2$ and $\omega_1 \pm 2\omega_2$ with respect to the fundamental frequency. $IM_2 = 2HD_2 = \frac{a_2}{a_1} U$, $IM_3 = 3HD_3 = \frac{3}{4} \frac{a_3}{a_1} U$, Figure 80 illustrates the intermodulation distortion.

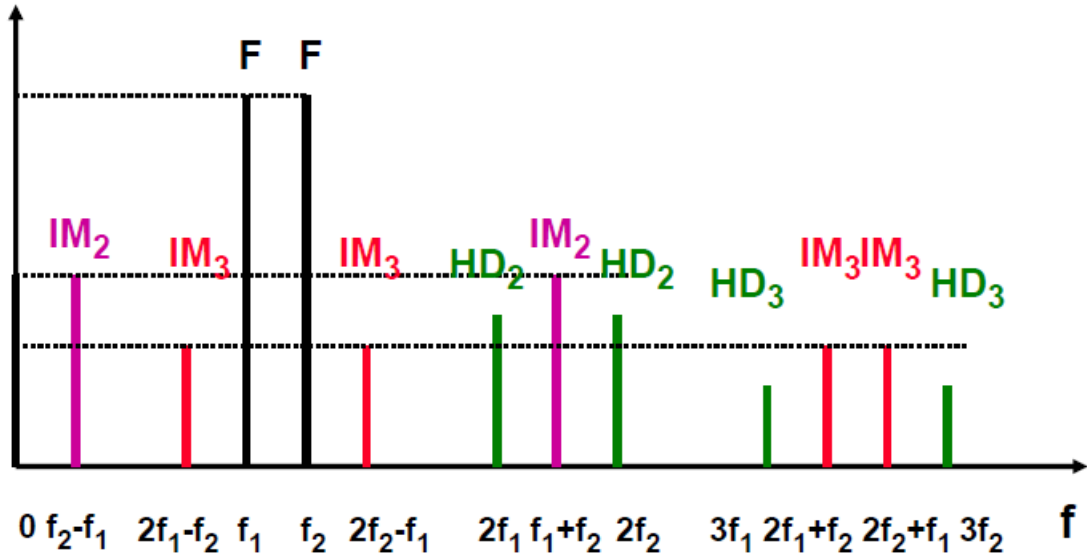


Figure 80 Impurity signal tones for two adjacent frequency

We can see that the second-order distortion generates components at low frequency, which can be filtered out using a bandpass filter or using a differential topology to cancel the even-order effects. The tones at $2f_1 - f_2$ and $2f_2 - f_1$ are the most important tones since they appear just near the fundamental tones and can be easily measured with a spectrum analyzer.

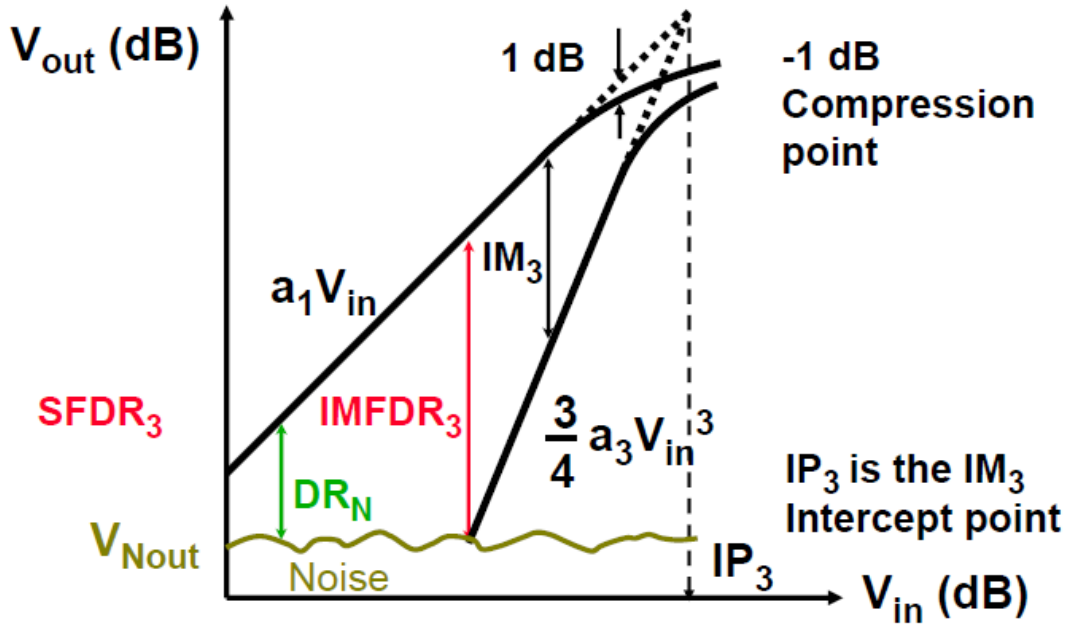


Figure 81 Amplitude IM_3 versus input signal

A differential amplifier is taken with input voltage V_{in} , which gives a nonlinear output voltage V_{out} , with coefficients a_1, a_3 since $a_2 = 0$ in a differential system. As shown in Figure 81, the components are plotted on a log scale basis, the fundamental itself has a slope of 1dB/dB, whereas the third-order IM_3 component have a slope of 3dB/dB. The ratio between the two is IM_3 , which is the distance between the slope in the vertical direction in the figure. It is important to find IM_3 at a specific voltage because distortion will become severe at high voltage levels, and noise will become an issue at low voltage levels. The maximum value is attained when the IM_3 level equals the noise level, which is the largest possible dynamic range that can be reached, this is the third-order Intermodulation Free Dynamic Range $IMFDR_3$.

By extrapolating the two slopes the point is called the IM_3 intercept point IP_3 .

The IP_3 is reached at the input voltage for which the amplitude of the fundamental $a_1 V_{in}$

equals IM_3 . It's value is easily calculated from the power series $IP_3 = \sqrt{\frac{4 a_1}{3 a_3}}$

Appendix B: Analysis of the non-linearity of differential pair

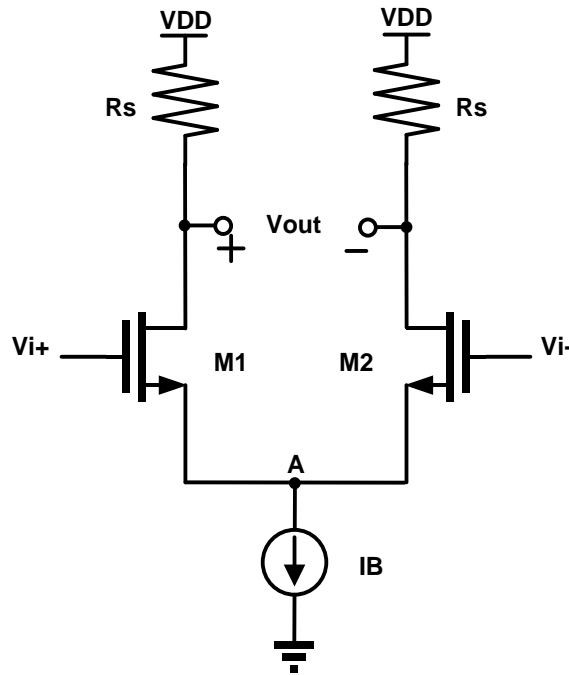


Figure 82 Simple differential pair

From Figure 82, assuming M1 is in saturation region and the circuit is symmetric. Doing a KVL at node A we have $V_{i+} - V_{i-} = V_{GS1} - V_{GS2}$ (A.1). The square-

law equation for MOS is $I_D = \frac{1}{2}u_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$ and, therefore, $V_{GS} = \sqrt{\frac{2I_D}{u_n C_{ox} \frac{W}{L}}} +$

V_{TH} (A.2).

Replacing (A.2) into (A.1) we have $V_{i+} - V_{i-} = \sqrt{\frac{2I_{D1}}{u_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{u_n C_{ox} \frac{W}{L}}}$. Squaring

both sides and noticing that $I_{D1} + I_{D2} = I_B$,

we obtain $\frac{1}{2}u_n C_{ox} \frac{W}{L} (V_{i+} - V_{i-})^2 - I_B = -2\sqrt{I_{D1}I_{D2}}$. Squaring both sides again,

we arrive at $(I_{D1} - I_{D2})^2 = -\frac{1}{4}(u_n C_{ox} \frac{W}{L})^2 (V_{i+} - V_{i-})^4 + I_B u_n C_{ox} \frac{W}{L} (V_{i+} - V_{i-})^2$.

Rearranging the equation with relations between $(I_{D1} - I_{D2})$ and $(V_{i+} - V_{i-})$ we thus get

$$I_{D1} - I_{D2} = \frac{1}{2}u_n C_{ox} \frac{W}{L} (V_{i+} - V_{i-}) \sqrt{\frac{4I_B}{u_n C_{ox} \frac{W}{L}} - (V_{i+} - V_{i-})^2} =$$

$$\frac{1}{2}u_n C_{ox} \frac{W}{L} V_{in} \sqrt{4(V_{GS} - V_{TH})^2 - V_{in}^2} = u_n C_{ox} \frac{W}{L} V_{in} (V_{GS} - V_{TH}) \sqrt{1 - \frac{V_{in}^2}{4(V_{GS} - V_{TH})^2}}$$

For approximating the small signal nonlinearity we assume $|V_{in}| \ll V_{GS} - V_{TH}$,

then using Taylor expansion series we can get

$$I_{D1} - I_{D2} \approx u_n C_{ox} \frac{W}{L} V_{in} (V_{GS} - V_{TH}) \left[1 - \frac{V_{in}^2}{8(V_{GS} - V_{TH})^2} \right], \text{ replacing } V_{in} = V_m \cos \omega t$$

for sinusoid analysis. We obtain, $I_{D1} - I_{D2} = u_n C_{ox} \frac{W}{L} V_{in} (V_{GS} - V_{TH}) \left[V_m \cos \omega t - \right.$

$\left. \frac{V_m^3 \cos^3(\omega t)}{8(V_{GS} - V_{TH})^2} \right]$. Expanding $\cos^3(\omega t)$ we get $I_{out} = I_{D1} - I_{D2} = g_m \left[V_m - \right.$

$\left. \frac{3V_m^3}{32(V_{GS} - V_{TH})^2} \right] \cos \omega t - g_m \frac{V_m^3 \cos(3\omega t)}{32(V_{GS} - V_{TH})^2}$, for small signals linearity analysis $V_m \gg$

$\frac{V_m^3 \cos(3\omega t)}{32(V_{GS} - V_{TH})^2}$ and we have $HD3 = \frac{A_{HD3}}{A_F} \approx \frac{V_m^2}{32(V_{GS} - V_{TH})^2}$ or $IM_3 = 3HD_3$, $IP_3 =$

$3.3(V_{GS} - V_T)$

With a simple expression left, in order to increase the linearity the overdrive voltage of the input transistor must be increased

Appendix C: Analysis of noise on MOSFETS

Noise is an arbitrary signal, we will never know what to expect next. The signal amplitude is unpredictable and as a result there is a Gaussian spreading around zero and the average value is zero. In order to grab the concept of noises or describe them into equations we have to take the power of the noise which is done by squaring the voltage.

Noise is a quantity that comes as a power, not a voltage or current. Figure 83 illustrates the behavior of white noise.

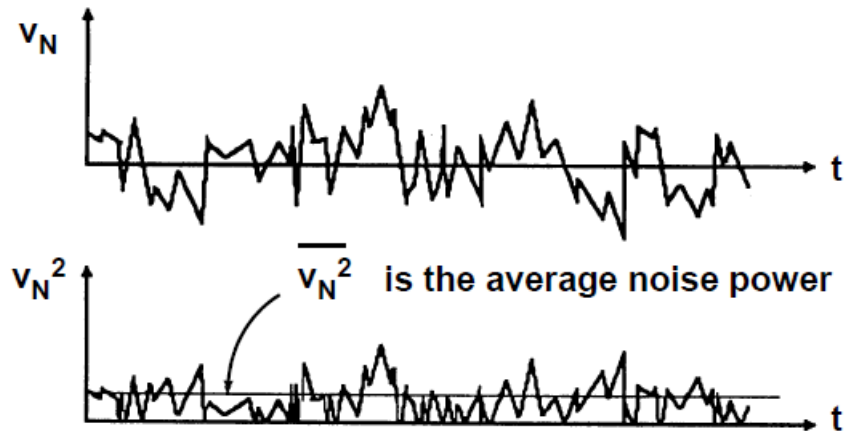


Figure 83 White noise

Normally the noise consists of two regions. One is white noise which is a flat region and extends to very high frequencies. The other is called the flicker noise ($1/f$) exists in the low frequency area and is inversely proportional to the frequency.

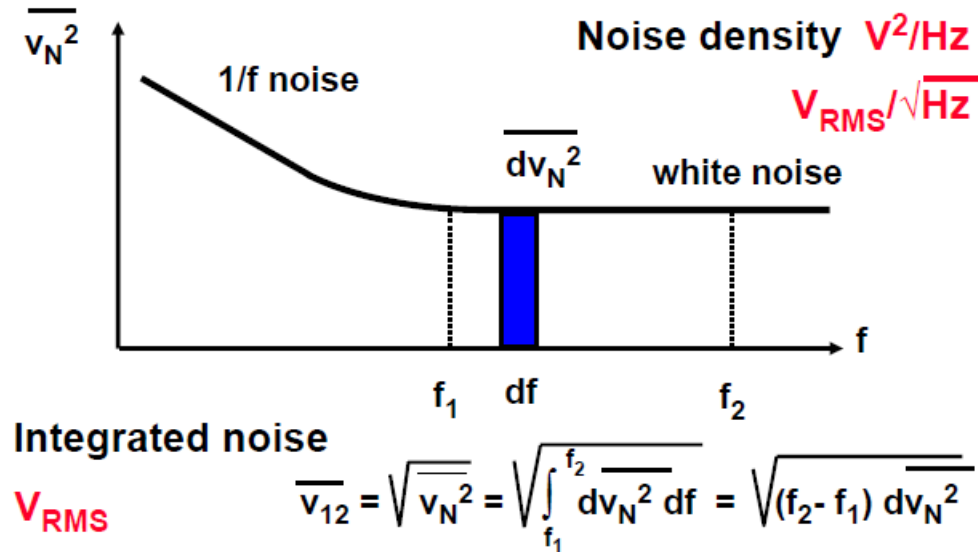


Figure 84 Noise density

The noise density is the noise power in an elementary small frequency band as shown in Figure 84. Its units is V^2/Hz , or by taking the square root V_{RMS}/\sqrt{Hz} . In order to calculate the total noise power in certain frequencies we need to integrate the noise density from f_1 to f_2 .

For our schematic we need to focus on the analysis of the noise of resistor's and MOSFETS.

A resistor gives thermal noise, it is modeled by a voltage source in series with the resistor or a current source in parallel as shown in Figure 85.

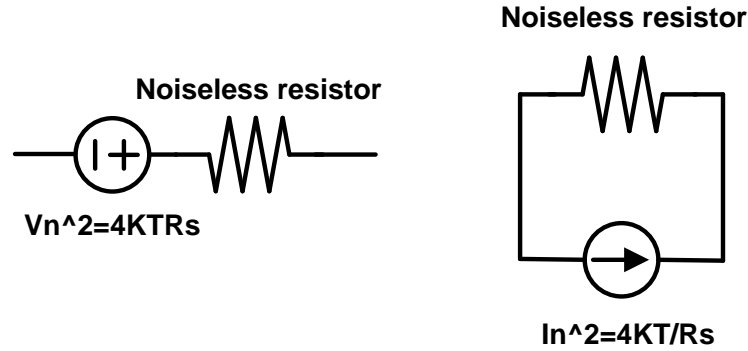


Figure 85 Noise model for resistor

The noise density is $\overline{V_n^2} = 4kTR$ (V^2/HZ) or $\overline{I_n^2} = 4kT/R$, where $k = 1.38 \times 10^{-23} J/K$. For a resistor of 1kOhm and 23 degrees room temperature the noise density is about $4nV_{RMS}/\sqrt{HZ}$

A MOSFET has a resistive channel while operating in saturation region. As a result, it exhibits thermal noise which is the most significant source noise generated in the channel. It is shown that for a long-channel MOS device operating in saturation, the channel noise can be modeled by a current source connected between source and drain with a noise density of $\overline{I_n^2} = 4KT\gamma g_m$ or $\overline{V_n^2} = 4KT\gamma/g_m$, where $\gamma = \frac{2}{3}$ for long channel devices and can go even larger for submicron MOSFET's, the model is shown in Figure 86. It is about 50% larger for 0.18um CMOS and doubles for 0.13um CMOS.

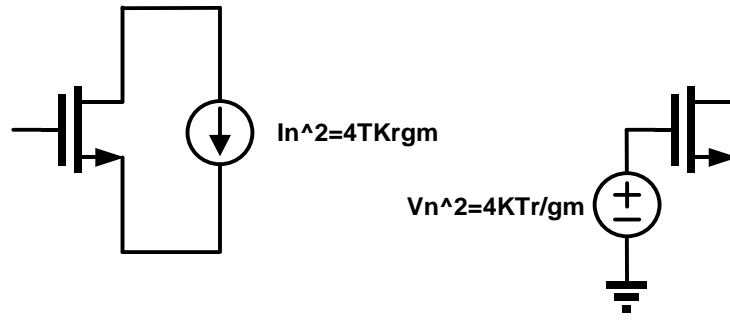


Figure 86 Noise model for MOSFET

The silicon has a crystal structure, which is cut off at the surface, where gate oxide is grown on top. Many dangling bonds appear at the end of this surface and gives rise to extra energy states. This causes surface states which contribute to the $1/f$ noise.

As shown in Figure 87, the flicker noise is modeled as a voltage source in series with the gate $\overline{V_n^2} = \frac{K}{C_{ox}WL} \frac{1}{f}$, where K is a process-dependent constant on the order of $10^{-25} V^2 F$

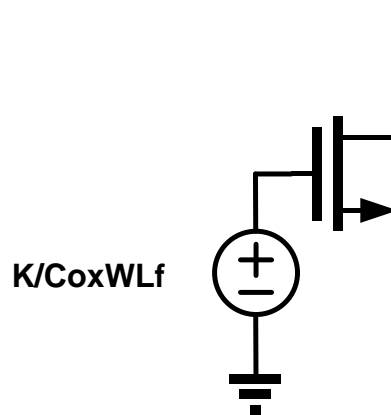


Figure 87 Flicker noise model for MOSFET

Since we may have MOSFET working in triode region, it is also imperative to make the noise model for the linear region MOSFET. A MOSFET working in a linear region has an equivalent resistance of $\frac{1}{g_m}$ and can replace the R of the thermal noise model of a resistor $\overline{V_n^2} = 4KTR \rightarrow \frac{4KT}{g_m}$, or $\overline{I_n^2} = 4kT/R \rightarrow 4kTg_m$

Since $g_m = u_n C_{ox} \frac{W}{L} (V_{GS} - V_T) = \sqrt{2I_D u_n C_{ox} \frac{W}{L}} = \frac{2I_D}{V_{GS} - V_T}$, from our OTA used for the application, we can tell that for a fixed $\frac{W}{L}$ for determine the current tuning, and fixed $V_{GS} - V_T$ so that the tuning scheme is stable with process and temperature variation