

PATTERNING ORGANIC ELECTRONICS BASED ON NANOIMPRINT
LITHOGRAPHY

A Dissertation

by

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ABSTRACT

The objective of this work is to investigate a high-resolution patterning method based on nanoimprint lithography (NIL) for the fabrication of organic electronics. First, a high-resolution, nondestructive method was developed to pattern organic semiconductors. In this approach, a sacrificial template made of amorphous fluorinated polymer (Teflon-AF) was first patterned by NIL. Poly(3-hexylthiophene) (P3HT), a organic semiconductor, was then spin-coated on the Teflon-AF template. Removing the sacrificial template by a fluorinated solvent achieved high-resolution P3HT patterns. P3HT lines and squares of various sizes (0.35 micron to tens of microns) were obtained by this method. This process of removing the sacrificial template is fully compatible with organic semiconductors. This technique was then used to fabricate passive-matrix organic light-emitting diode (PMOLED) arrays for flat-panel display applications.

Fabrication of a self-aligned bottom gate electrode for organic metal semiconductor field effect transistor (OMESFET) was also developed. This self-aligned gate allows the transistor to have a potential to operate in the high frequency. Owing to the lack of an insulating layer, OMESFET can also work in a relatively low voltage range compared to other organic field effect transistors with an insulating layer. This work also demonstrates its capability of patterning alternating self-aligned metals at the nanoscale.

This research also developed a low-cost and time-saving technique to create nanostructures by transferring nanoscale polymeric sidewalls into a substrate. This

polymer sidewall transfer lithographic technique can be used for generating nanostructures without advanced electron-beam lithography. Potential applications include the fabrication of nanoimprint molds with high-resolution patterns for applications in nanofluidics and nanophotonics. The polymeric sidewall is a vertically spreading layer deposited by spin-coating a polymer solution on a vertical template. Varying processing parameters such as the solution concentration or the spin-coating speed, changes the sidewall dimension, which, after pattern transfer, also changes the structure dimension on the substrate. High-resolution trenches of about 15 nm have been achieved after transferring straight-line sidewalls into the substrate. Other than straight-line sidewall patterns, this method also fabricated ring-shaped patterns including circles, squares, and concentric squares.

Finally, a new structure of organic solar cells (OSCs) was investigated for increasing the solar power conversion efficiency. Although the experimental result did not meet the theoretical expectation, reasonable modifications of the device structure will be tested to achieve the goal in the future.

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NOMENCLATURE

AFM	Atomic force microscope
Al	Aluminum
Al ₂ O ₃	Aluminum oxide
Ar	Argon
Au	Gold
BHJ	Bulk heterojunction
Cr	Chromium
CVD	Chemical vapor deposition
DCB	1,2-Dichlorobenzene
DPI	Dots per inch
DSSCs	Dye-sensitized solar cells
DUV	Deep ultraviolet lithography
EUV	Extreme ultraviolet lithography
FDTS	Perfluorodecyltrichlorosilane
g_m	Transconductance
HCL	Hydrochloric acid
HFES	Hydrofluoroethers
HfO ₂	Hafnium oxide
HMDS	Hexamethyldisilazane
HOMO	Highest occupied molecular orbital

ICP	Inductively coupled plasma
ITO	Indium tin oxide
N ₂	Nitrogen
NIL	Nanoimprint lithography
OFESC	Organic field effect solar cell
OFETs	Organic field effect transistors
OLEDs	Organic light emitting diodes
OMISFET	Organic metal insulator semiconductor field effect transistor
OMESFET	Organic metal semiconductor field effect transistor
OSCs	Organic solar cells
PCBM	[6,6]-Phenyl- C61 butyric acid methyl ester
PECVD	Plasma enhanced chemical vapor deposition
PEDOT:PSS	poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)
PMOLED	Passive matrix organic light emitting diode
P3HT	poly(3-hexylthiophene)
RIE	Reactive ion etching
SAM	Self-assembled monolayer
SEM	Scanning electron microscope
SFIL	Step and flash imprint lithography
SF ₆	Sulfur hexafluoride
Si ₃ N ₄	Silicon nitride
SiO ₂	Silicon dioxide

T_g

Glass transition temperature

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CHAPTER I

INTRODUCTION AND LITERATURE REVIEW

1.1 Introduction

Since the organic semiconductor was first reported in 1948[1], successful demonstrations of electronics made of organic semiconductors have attracted more and more research interests due to several advantages: low-cost fabrication, ease of processing, and the capability of building flexible electronics. Organic semiconductors are conjugated molecules that include conjugated small molecules and conjugated polymers depending on their molecular size. These conjugated molecules contain alternating single bond and double bonds. This bonding arrangement results in delocalization of electrons in organic molecules, providing them very attractive electrical and optical properties[2, 3]. With these novel properties, organic semiconductors can be used for many electronic applications including organic light-emitting diodes (OLEDs)[4, 5], organic solar cells (OSCs)[6], and organic field-effect transistors (OFETs)[7].

In recent years, the continuous improvement of organic electronics has enabled the realization of their practical application, which requires them to be integrated into circuits. Therefore, patterning organic electronics becomes an important topic in device applications. Currently, there are many technologies used for patterning polymer materials, such as photolithography, ink-jet printing, screen printing, flexo printing, gravure printing, laser writing, electron-beam lithography, and nanoimprint lithography

(NIL). Among these techniques, laser writing and electron-beam lithography cannot be used for patterning organic semiconductors because their high energy damages the material. NIL is the most suitable technique for electronics application due to its high-resolution and high-throughput capability. Other patterning techniques either lack of high-resolution capability or have low fabrication throughput. Since this work is primarily based on NIL, in this literature review, only NIL will be introduced in more detail while other patterning methods will be briefly discussed.

1.2 Nanoimprint lithography (NIL)

NIL is an emerging technique toward high-resolution and high-throughput patterning. It is a mechanical molding lithography, so the working principle of NIL is fundamentally different from the conventional photolithography. The principle of this technique is to transfer patterns from the imprinting mold to the resist coated on a substrate. Figure 1.1 schematically illustrates the process of NIL. This technique has already demonstrated a capability of fabricating high-resolution patterns. As illustrated in Figure 1.2, patterns of about 10 nm can be obtained by NIL[8]. There are mainly two types of nanoimprint approaches, thermal imprint and UV imprint. Because of their different principles, their mold and imprint resist are different and will be discussed in the following sections.

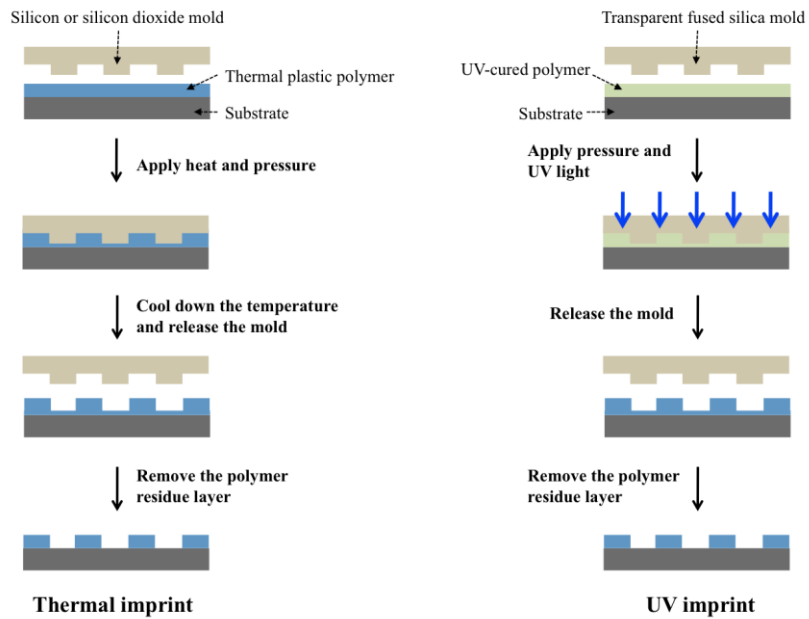


Figure 1. 1. Fundamental principles of thermal nanoimprint lithography and UV nanoimprint lithography.

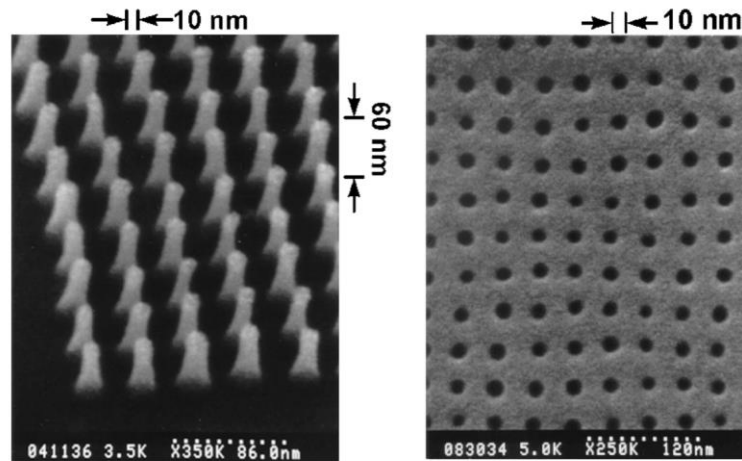


Figure 1. 2. The sub-10 nm patterns fabricated by NIL. The figure on the left is the nanoimprint mold of 10 nm protrusions in dimension and the one on the right is the imprinted patterns on the imprint resist[8].

1.2.1 Nanoimprint mold

In thermal NIL, the selection of mold material is based on the considerations of material hardness, thermal expansion coefficient, and compatibility with traditional nanofabrication processing. The material hardness strongly affects the durability of the nanoimprint mold. The thermal expansion coefficient plays a critical role in the thermal NIL because a thermal mismatch between the mold and the substrate causes pattern distortions during the processing and affects the pattern fidelity. Therefore, using the same material for both the mold and the substrate forms a good pair for a highly precise NIL[9]. Currently, fabricating silicon and silicon dioxide molds can be easily achieved with semiconductor manufacturing technology. As shown in Figure 1.3, the required processes of building structures on Si and SiO₂ are patterning polymer resist on the substrate, depositing metal as an etching mask, and etching the substrate using reactive ion etching (RIE) technique. Concluding all of the discussions mentioned above, Si and SiO₂ are the most suitable material for the imprint mold[9]. The fabrication of a UV-imprint mold is the same as that of a thermal imprint mold. The only requirement is to use a transparent substrate for UV light to pass through. Fused silica, therefore, is usually the most used material for UV-imprint.

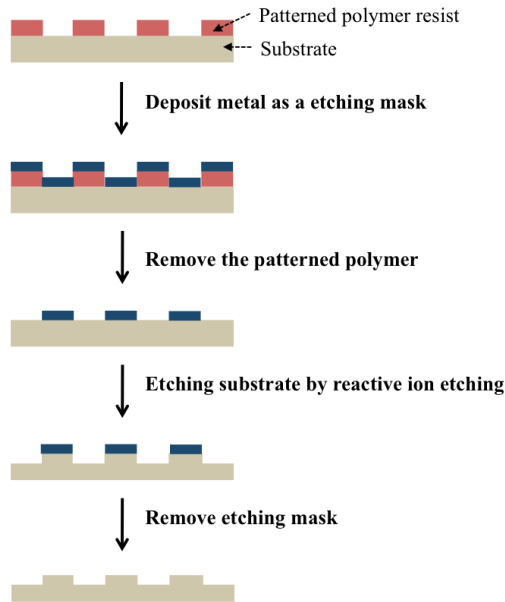


Figure 1. 3. The process of fabricating an imprinting mold.

High density of nanostructures on the surface of the mold increases its surface area, resulting in a large contact interface between the mold and the imprinted resist compared to that between the substrate and the imprinted resist. Such large contact interface causes a strong adhesion of the imprinted resist to the mold and becomes difficult to separate the mold and the imprinted resist after molding the resist. This phenomenon leads to large defected patterns. In this regard, the surface of the mold is usually treated to reduce the adhesion. The most used method is to coat the mold surface with a self-assembled monolayer (SAM) of a fluorosilane, such as tridecafluoro-1,1,2,2-tetrahydrooctyltrichlorosilane ($\text{CF}_3\text{-(CF}_2\text{)}_5\text{(CH}_2\text{)}_2\text{SiCl}_3$). This method can be processed by either a solution-phase or a vapor-phase coating[10, 11]. This coating has a low

surface energy which reduces the adhesion of the resist to the mold and it has been proven to be repeatedly used for thousands of UV nanoimprints[9].

1.2.2 Nanoimprint resist

Polymers used as the imprinting resist need to meet two requirements during the imprinting processing: low young's modulus and low viscosity. In thermal imprint, these requirements can be simultaneously achieved by heating the polymer above their glass transition temperature (T_g). Empirically, the imprint temperature is chosen about 70°C – 90°C above the T_g in order to have a good imprint result[9, 12]. Poly(methyl methacrylate) (PMMA) is the most commonly used imprint resist due to its low volume change under large temperature and pressure variations[13]. In the case of UV-imprint, the imprint resist is originally a liquid phase precursor that can be cured by UV-light exposure. This liquid phase resist has automatically satisfied two requirements of NIL, low young's modulus and low viscosity, without exposure to high temperature and high pressure that could limit the throughput of NIL processing[9]. A derivative technique, step and flash imprint lithography (SFIL), was then developed based on UV-imprint, allowing this technique potentially be used for integrated circuit manufacturing[14].

1.3 Other patterning methods for organic semiconductors

1.3.1 Photolithography

Photolithography is a widely used technique for patterning electronics in current semiconductor manufacturing. It is an optical lithography that utilizes a light source to

resolve patterns pre-designed on a photo-mask. Recently, it has been adapted to pattern organic semiconducting molecules by employing a special fluorinated photoresist that can be processed in fluorinated solvents which, for example hydrofluoroethers (HFEs), have been proven to be inert to organic semiconducting molecules[15]. The fabrication processing is the same as traditional photolithography. Figure 1.4 shows an example of the processing method and a patterned result of an organic semiconducting material. Due to the limitation of light wavelength, the reported minimum dimension by using UV-lithography is $0.4\ \mu\text{m}$ [16].

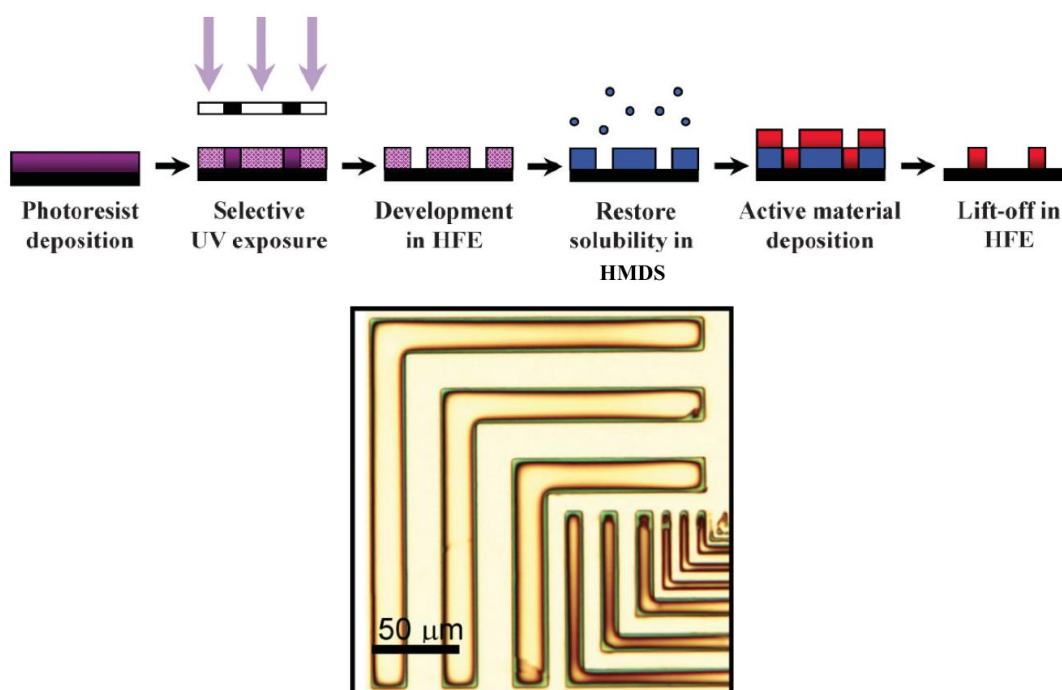


Figure 1. 4. The photolithography patterning method for organic semiconducting materials and the organic semiconducting material patterned by photolithography[15].

1.3.2 Ink-jet printing

Processing organic semiconductors in solution phase enables them to be patterned by ink-jet printing[17]. Like the conventional ink-jet printer, this approach directly prints patterns by continuously ejecting droplets from a piezoelectric nozzle to a desired location. The technique of ejecting a fixed volume of droplets attributes to a change of pressure generated by a piezoelectric tubular actuator attached to the nozzle. Figure 1.5 shows a general structure of the piezoelectric ink-jet printing nozzle. Printable devices, such as OLEDs, OFETs and OSCs, have been demonstrated based on this technique. Currently, this approach can provide patterns with dimensions greater than 20 μm [17].

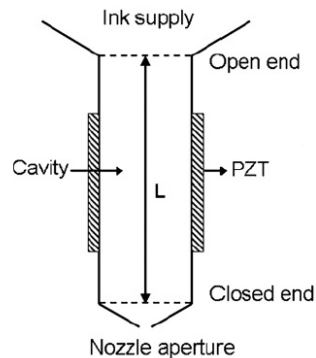


Figure 1. 5. The piezoelectric ink-jet printing nozzle with piezoelectric tubular actuator attached on the side in order to eject a fixed volume of solutions[18].

1.3.3 Screen printing

Screen printing is a printing technique that is commonly used in printing images on soft substrates such as clothes and papers. This technique was then adapted for electronic applications because of its high throughput. The principle of the method is

illustrated in Figure 1.6. The screen stencil is held above the substrate with a paste applied on top of it. The squeegee presses the paste across the screen stencil, pushing the paste through the screen stencil and depositing the paste on the substrate. The patterning resolution of this technique is able to reach $10\ \mu\text{m}$ [19].

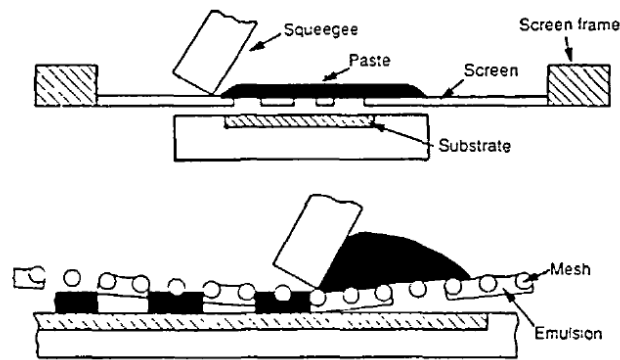


Figure 1. 6. The schematic diagram of the screen printing principle[20].

1.3.4 Gravure printing and flexo printing

Both gravure printing and flexo printing are roll-to-roll printing techniques potentially offering low cost and high throughput manufacturing. The difference between these two methods is that gravure printing uses a concave cylinder while flexo printing uses a convex cylinder. Figure 1.7 shows a schematic diagram of gravure printing and flexo printing. In gravure printing, the concave cylinder is immersed in the ink that covers the entire concave structures. A doctor blade scrapes the ink on the cylinder surface, leaving the grooves full of ink, which is then transferred to the flexible substrate with a pressure induced by an impression cylinder. In flexo printing, an anilox cylinder is immersed in the ink like the gravure printing. The doctor blade does not

directly contact with the anilox cylinder instead it keeps a small gap between the blade and the cylinder. The plate cylinder with convex structures is coated with ink by contacting with the anilox cylinder. Then, the ink can be transferred to the flexible substrate with a pressure induced by the impression cylinder[21].

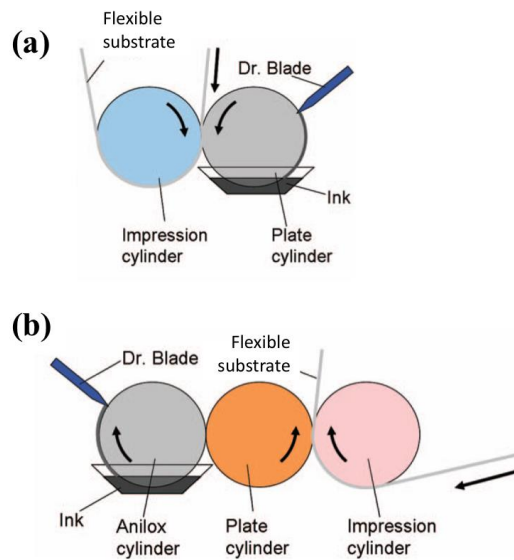


Figure 1. 7. Schematic diagram of (a) gravure printing and (b) flexo printing[21].

The resolution of the printed patterns directly depends on the dimension of the structure fabricated on the cylinders. Currently, gravure printing provides a pattern resolution of 9 μm [22] and flexo printing offers a resolution of 50 μm [23].

1.4 Proposed method for patterning organic electronics

In this work, several patterning and fabrication methods for organic electronics are proposed. All these techniques are primarily based on NIL due to its potential

advantages of high-resolution and high-throughput. Patterning organic semiconductors and metal electrodes is the main investigation of those proposed techniques because both organic semiconductors and metal electrodes are major parts of organic electronics. These patterning methods along with experimental details, novelties, and results will be discussed respectively in different chapters.

In Chapter II, the technique for high-resolution and non-destructive patterning of isolated organic semiconductors for device applications is described in detail. Sub-micron isolated organic semiconductor patterns are successfully achieved, with a potential to further reduce the pattern resolution into deep sub-micron region. The technique has the capability of achieving the highest organic semiconductor patterning resolution, thus providing a practical route towards the fabrication of organic integrated circuits based on high-performance nanoscale organic electronic devices.

For organic electronics to enter commercial applications, the device and circuit performance must be further enhanced. Current OFET device structure is not optimized for this purpose, resulting in organic circuits with low performance. In Chapter III, a technique to fabricate self-aligned organic MESFET device is presented. This technique eliminates parasitic capacitance and resistance in organic transistors, thus has the potential to achieve low operational power and high-frequency applications for organic circuits.

During the course of this research, a new technique is devised to fabricate sub-20 nm structures without advanced lithographic techniques. The technique is called polymer sidewall transfer lithography, and its process and capabilities are described in Chapter IV

in detail. This technique opens a facile route towards the fabrication of nanostructures with simple lab equipment. Potential applications include the fabrication of nanoimprint molds, nanofluidic devices and nanostructures for photonic applications.

At the end of this work, a novel organic electronic device, entitled organic field-effect solar cells, is fabricated by NIL. The device principles, fabrication schemes and preliminary results are discussed in Chapter V.

CHAPTER II

HIGH-RESOLUTION NON-DESTRUCTIVE PATTERNING OF ISOLATED ORGANIC SEMICONDUCTORS FOR DEVICE APPLICATIONS*

2.1 Introduction

Today, electronic devices made of organic semiconductors have exhibited many potential advantages over traditional electronics, including low-cost fabrication, flexible devices, and large-area integration. With these advantages, many researches have been investigated to explore more practical applications for these novel electronics. In order to have advanced applications, organic electronics such as OFETs and OLEDs, need to be patterned into isolated units, such that organic integrated circuits[24-26] and OLED displays[27] can be implemented. For integrated circuit applications, isolating electronics reduces device crosstalk within circuits. For display applications, red, green, and blue organic light-emitting pixels integrated into the display need to be separated and operated individually in order to generate images. To achieve organic semiconductor patterning, many advanced techniques were developed such as photolithography[15], ink-jet printing[28], screen printing[29], and nanoimprint lithography (NIL)[30]. Among them, NIL is the most suitable technique to patterning organic semiconductors due to its capability of patterning nanoscale structure, high throughput, and low-cost fabrication[8]. However, the residual layer after conventional nanoimprint connects all

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units and becomes a major issue in achieving isolated organic semiconductor structures. The conventional method to eliminate the residual layer is to use oxygen reactive ion etching (RIE)[30], but the highly reactive oxygen plasma can damage organic semiconductors, resulting in severe device degradation.

A nondestructive patterning method for organic semiconductors by employing a fluorinated sacrificial template that can be wet processed by fluorinated solvents was reported before[15]. Its process contains a sequence of photolithography patterning, deposition of organic semiconductor, and liftoff processing. The photolithography step is to pattern a fluorinated polymer template. After depositing the organic semiconductor on the patterned template, the liftoff process used to dissolve the template by a fluorinated solvent forms isolated organic semiconductor structures on the substrate. The fluorinated solvents are inert to non-fluorinated materials, including most of the organic semiconducting materials. In order to pattern even higher resolution patterns, I propose to combine NIL and the fluorinated template processing for the purpose of nondestructively patterning sub-micron isolated organic semiconductor structures.

2.2 Experimental method

In this experiment, Teflon-AF 1600 purchased from Dupont was used as the nanoimprint resist and the template material. FC-40, a perfluorinated solvent purchased from Sigma Aldrich, was selected to dissolve Teflon-AF[31]. The organic semiconductor to be patterned is poly(3-hexylthiophene) (P3HT, from Rieke Metals). P3HT was selected in this experiment because it is a widely used conjugated polymer in

various applications, including OFETs and organic solar cells (OSCs). The solvent to dissolve the P3HT polymer was 1,2-dichlorobenzene (DCB) purchased from Sigma Aldrich. A Teflon-AF solution of 2 wt% was made by dissolving Teflon-AF in FC-40. The solution was heated to 40°C for at least 24 hours to completely dissolve Teflon-AF. A P3HT solution was obtained by dissolving P3HT in DCB (15 mg/ml) and the P3HT solution was also heated to 40°C and stirred for 24 hours. Nanoimprint molds of various dimensions were made of thermally grown silicon dioxide and coated with perfluorodecyltrichlorosilane (FDTS) in order to easily separate the mold from the resist after imprinting. To coat FDTS on the mold, a small amount of FDTS was mixed with heptane and the mold was immersed into the solution for 10 minutes. After coating FDTS, the mold surface became highly hydrophobic.

The patterning technique is schematically illustrated in Figure 2.1. The steps from (a) to (f) are explained as following: (a) The 2 wt% Teflon-AF solution was spin-coated on the silicon dioxide substrate at 800 rpm, forming a 210 nm–230 nm thick Teflon-AF film serving as the nanoimprint resist; (b) The mold thermally imprinted the Teflon-AF film at 230°C and 900 psi; (c) The mold pattern was transferred into the resist after releasing the mold. The patterned resist served as a sacrificial template to pattern organic semiconductors; (d) Oxygen RIE was used to anisotropically etch the Teflon-AF template in order to eliminate the residual layer; (e) The organic semiconductor P3HT was spin-coated on the Teflon-AF sacrificial template; and (f) After removing the Teflon-AF template by the FC-40 solvent, isolated P3HT structures were formed on the substrate.

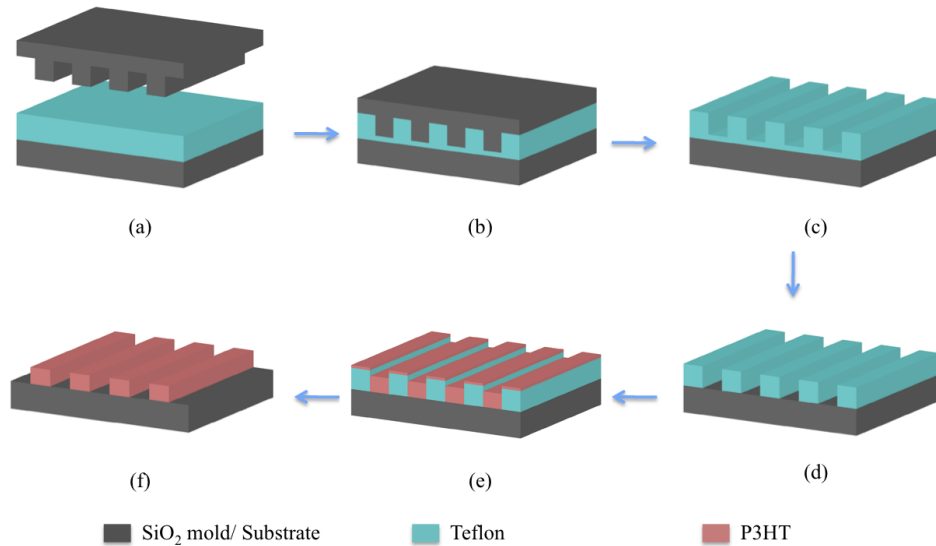


Figure 2. 1. Schematics of nondestructive patterning of isolated P3HT by nanoimprint. (a) Spin-coat the Tefflon-AF solution to form a thin Tefflon-AF film. (b) Thermally imprint the Tefflon-AF film by a nanoimprint mold. (c) After releasing the mold, patterns are generated in the Tefflon-AF film. (d) Remove the residual layer by oxygen RIE. (e) Spin-coat P3HT on the Tefflon-AF sacrificial template. (f) Dissolve the Tefflon-AF template in FC-40 solvent to obtain P3HT patterns.

2.3 Results and discussion

2.3.1 Patterning polymer sacrificial template

To nondestructively pattern P3HT, a fluorinated sacrificial template that can be processed by fluorinated solvents is needed[15, 32]. The main reason to use fluorinated material as the sacrificial template is that the wet process with fluorinated solvents is fully compatible with organic semiconductors. Fluorinated solvents are classified as orthogonal to both polar and non-polar solvents; in other words, fluorinated solvents are inert to organic materials that can be processed in polar and non-polar solvents[32].

Teflon-AF 1600 has a glass transition temperature of 160°C. Experiments show that the imprinting temperature needs to be at least 220°C to completely transfer patterns from the mold to Teflon-AF 1600. Therefore, the imprinting temperature was set to be 230°C to mold the Teflon-AF layer. For the imprinting pressure, the range of 300 psi to 900 psi successfully transfers patterns above 220°C. Higher pressures out of this range have a risk to break the mold and lower pressures cannot fully transfer patterns.

Although the surface of Teflon-AF is highly hydrophobic, oxygen RIE removal of the residual layer after nanoimprint increases its surface energy and renders the surface hydrophilic property. In general, a hydrophobic template surface is desired in the process of spin-coating the P3HT solution in order to aggregate P3HT mostly in the template cavities and repel the P3HT solution from the template surface. Fortunately, the hydrophobic surface of Teflon-AF after oxygen RIE can be restored by thermal treatment above its glass transition temperature (160°C). Figure 2.2 illustrates contact angles of water droplet on the Teflon-AF surface before and after RIE treatment. The flat pristine Teflon-AF had a contact angle of around 112° (Figure 2.2(a)). After oxygen RIE treatment, the surface turned from hydrophobic to hydrophilic, and the contact angle was generally below 90° (Figure 2.2(b)). After thermal treatment at 160°C on a hotplate for 1 minute, the contact angle increased to 93.4°. Figure 2.2(e) shows a continuous increase in the contact angles of water droplet on the Teflon-AF surface as the annealing temperature increases. After 240°C annealing for 1 minute, the contact angle was restored to 107.1°, which is close to that of the pristine Teflon-AF surface. In this work,

the annealing temperature of 170°C was used to ensure hydrophobic Teflon-AF surface while maintaining pattern fidelity.

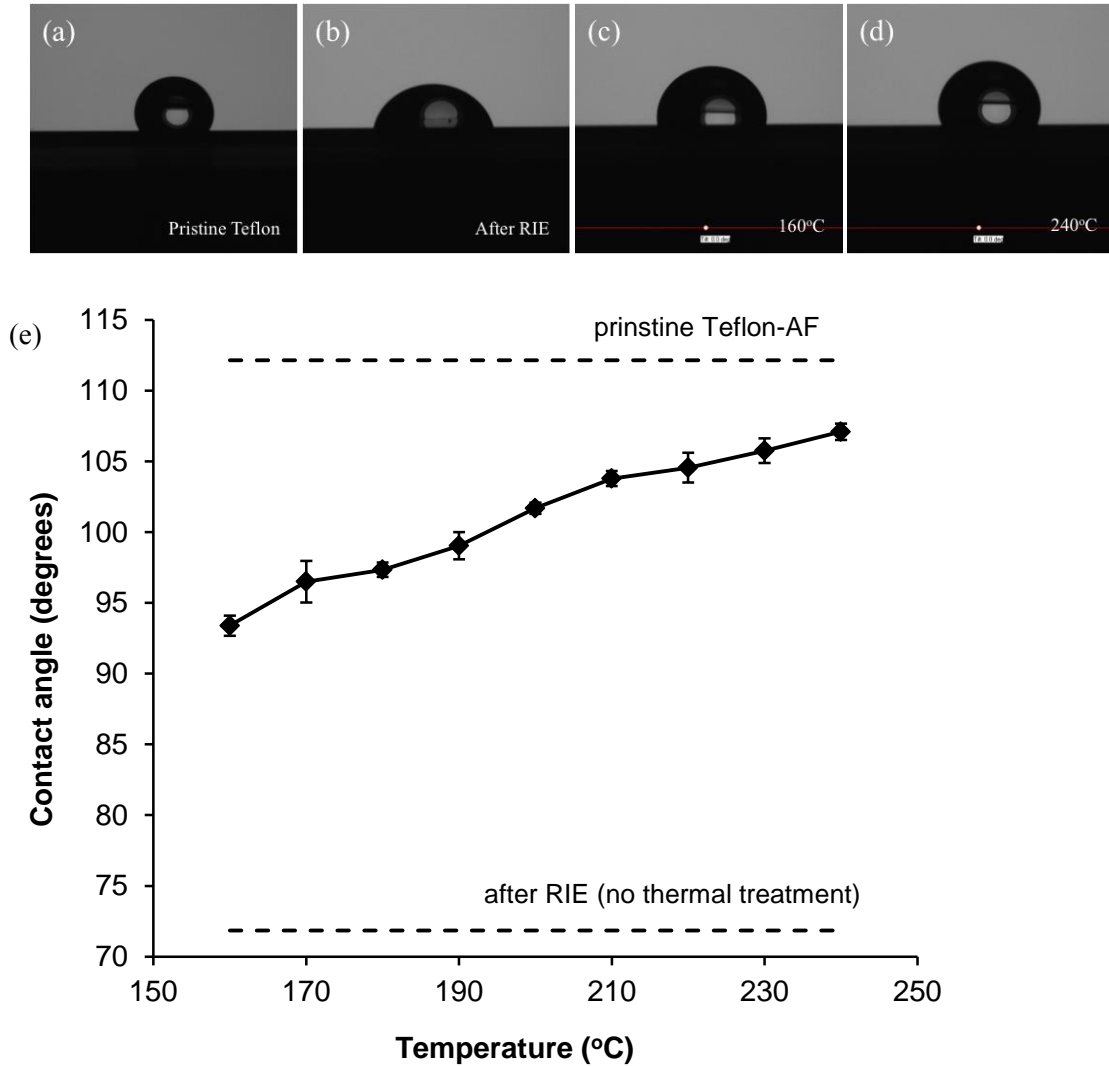


Figure 2. 2. Contact angles of water droplet on different Teflon-AF surface conditions. (a) Pristine Teflon-AF after spin-coating. (b) Teflon-AF after oxygen RIE. (c) RIE-treated Teflon-AF after 1 minute annealing at 160°C. (d) RIE-treated Teflon-AF after 1 minute annealing at 240°C. (e) Water contact angle variation after 1 minute annealing at different temperatures.

2.3.2 Patterning isolated organic semiconductor structures

Organic semiconductor structures ranging from tens of microns to sub-micron can be easily achieved by the technique described in Figure 2.1. The patterning results of P3HT structures are shown in Figure 2.3. Figure 2.3 (a) and (b) show the optical microscope image and the fluorescent microscope image of 50 μm P3HT lines, respectively. Figure 2.3 (c) and (d) show 5 μm P3HT gratings in optical and fluorescent microscope images, respectively. In the fluorescent images, the dark background clearly indicates that P3HT patterns are completely isolated. All P3HT gratings exhibit smooth line edges. Since nanoimprint lithography has the potential to produce high-resolution patterns, sub-micron P3HT structures are also obtained by the same approach. Figure 2.4 shows P3HT square patterns in the dimension of 1 μm and 0.5 μm . Figure 2.4 (a) and (c) are optical microscope images and Figure 2.4 (b) and (d) are fluorescent microscope images.

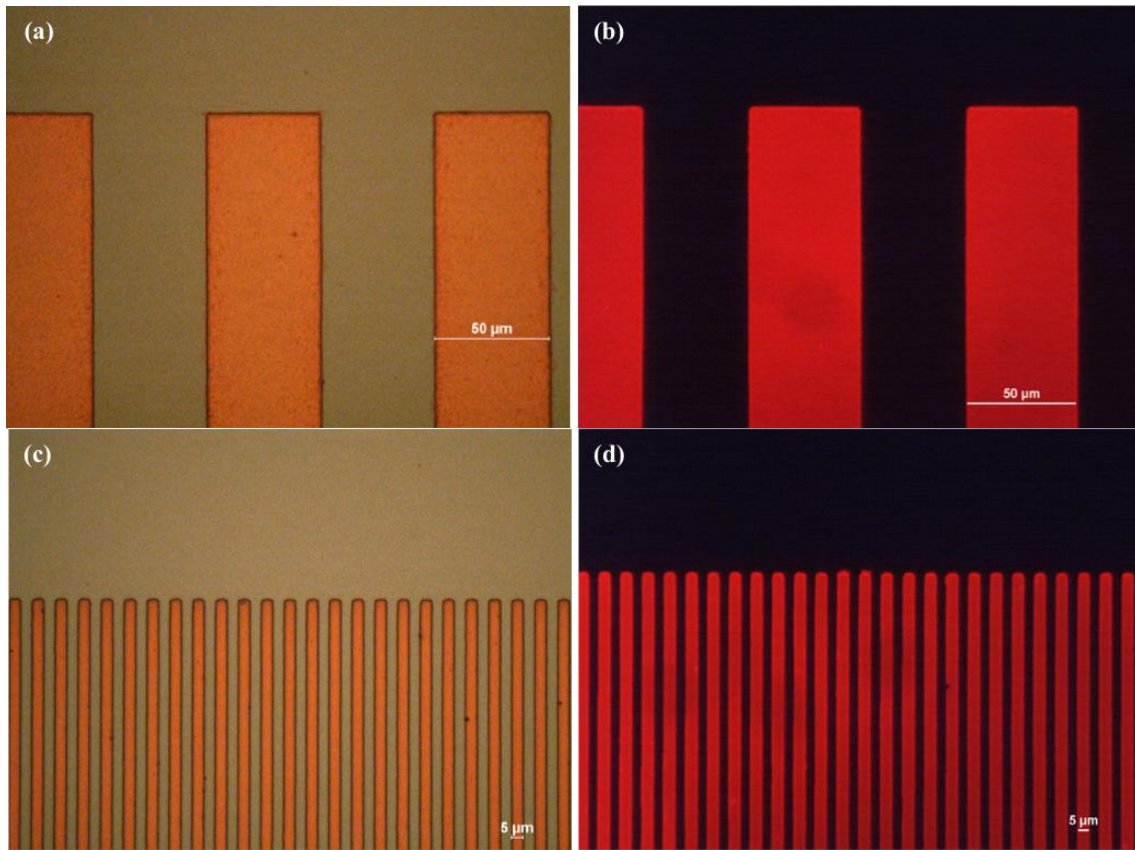


Figure 2. 3. Images of isolated P3HT grating patterns achieved by nanoimprint and sacrificial template. (a) and (b) show the optical image and the fluorescent image of 50 μm P3HT gratings, respectively. (c) and (d) show the optical image and the fluorescent image of 5 μm P3HT gratings, respectively.

In Figure 2.4, some defects, especially in the 0.5 μm patterns, were observed after patterning. This issue was caused by the poor adhesion between the P3HT pattern and the substrate. After spin-coating the P3HT solution on the Teflon-AF template, it was found that a small amount of P3HT can still stay on the Teflon-AF surface despite the surface hydrophobicity after thermal treatment. Therefore, to efficiently dissolve the Teflon-AF template and liftoff P3HT on the template, an ultrasonic bath was used. Poor adhesion between the P3HT squares and the substrate resulted in a few missing

structures during the ultrasonic agitation. Comparing Figure 2.4 (a) and (c), smaller structures with smaller contact area to the substrate yield more defects.

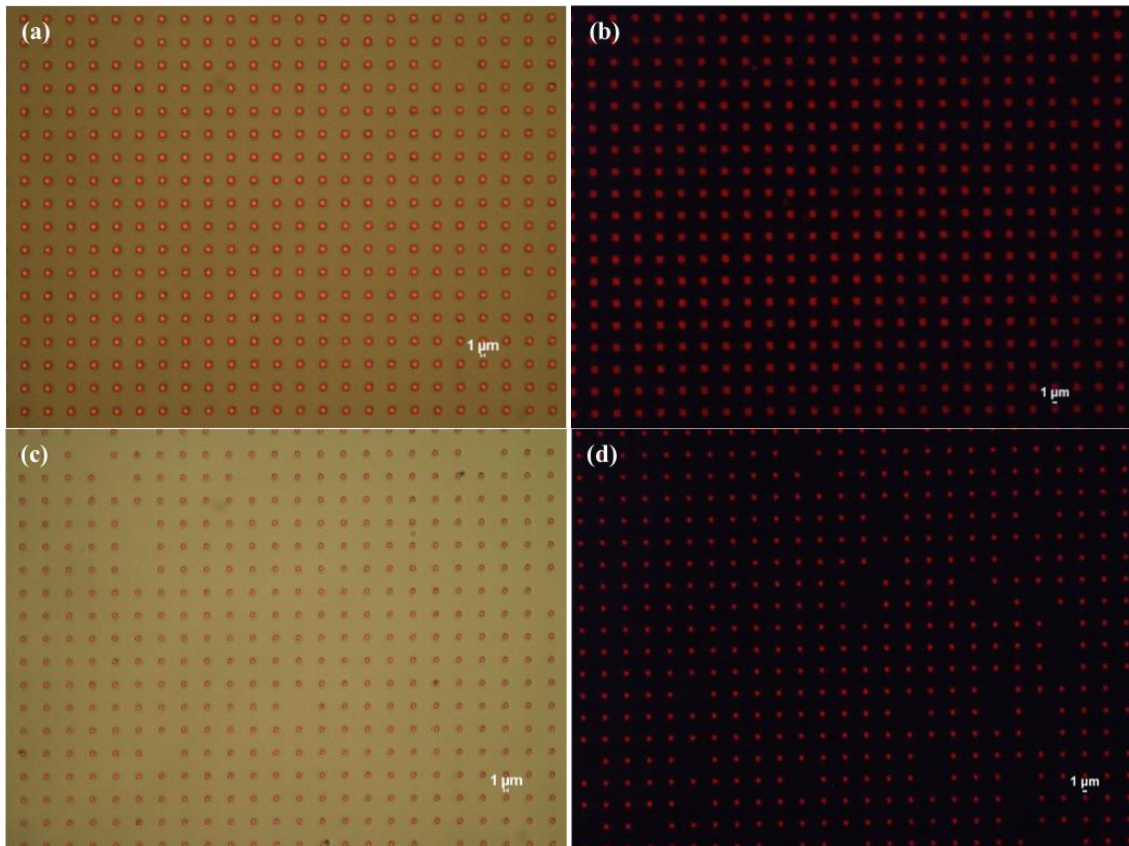


Figure 2. 4. Images of P3HT square patterns achieved by nanoimprint and sacrificial template. (a) and (b) show the optical microscope image and the fluorescent microscope image of 1 μm P3HT squares, respectively. (c) and (d) show the optical microscope image and the fluorescent microscope image of 0.5 μm P3HT squares, respectively.

The 350 nm P3HT grating patterns are also obtained as shown in Figure 2.5. Figure 2.5 (a) shows both the P3HT pattern and the Teflon-AF template. Two peeled-off Teflon-AF lines clearly show that P3HT filled in the trenches of the Teflon-AF template. Figure 2.5 (b) is the cross-sectional view of the P3HT grating after removing the Teflon-

AF Template. The sub-micron isolated P3HT lines are well defined. It also shows that the edges of the P3HT lines are taller than the middle of the P3HT lines. This is caused by the drying process of the P3HT solution in the trenches of the Teflon-AF template.

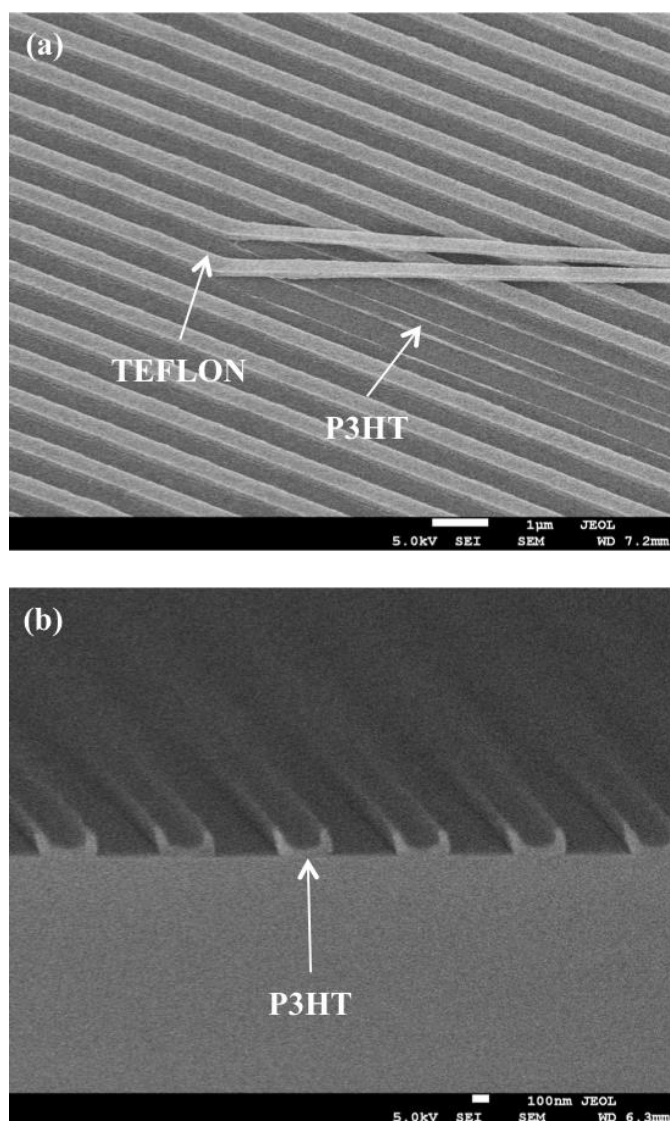


Figure 2. 5. Scanning electron microscopy (SEM) monographs of 350 nm P3HT grating patterns. (a) Teflon-AF and the P3HT patterns before removing the Teflon-AF template. (b) Cross-sectional view of 350 nm P3HT patterns after dissolving the Teflon-AF template.

2.3.3 Patterning OLED arrays

The proposed patterning technique can be used to not only pattern isolated organic semiconductor structures, but also fabricate organic electronic device arrays. Based on the method developed in this work, a passive-matrix organic light-emitting diode (PMOLED) array was demonstrated. Figure 2.6 shows the processing steps. First, indium tin oxide (ITO) stripes of 50 μm were patterned on a glass substrate by photolithography (Figure 2.6(a)). To pattern the ITO, S1805 photoresist purchased from Rohm and Haas was spin-coated (4000 rpm) on the 40 nm thick ITO layer deposited on the glass substrate. After UV exposure (20 mJ/cm^2) with a photo-mask of 50 μm stripe patterns, the sample was developed in the MF-319 developer to reveal photoresist stripes on the ITO layer. The photoresist stripes served as the mask in the processing of the ITO etching. The ITO was wet etched in the 37% hydrochloric acid (HCl). Finally, the patterned photoresist stripes, after etching the ITO, were removed by acetone. By this mean, ITO stripes can be achieved. Then 2 wt% Teflon-AF solution was spin-coated on top of the ITO stripes to form a 230 nm thick Teflon-AF film (Figure 2.6(b)). After thermally imprinting the Teflon-AF film at 230°C and 900 psi with a grating mold of 400 nm in depth and 100 μm wide, 50% duty cycle (Figure 2.6(c)), the mold was released and oxygen RIE was used to remove the residual layer (Figure 2.6(d)). A very thin poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) layer was spin-coated as the hole transport layer and a 100 nm thick P3HT film was spin-coated as the light emitting layer. After that, a 100 nm thick aluminum (Al) layer was thermally evaporated on top of the P3HT layer (Figure 2.6(e)). Finally, dissolving the Teflon-AF

template and lifting off the PEDOT:PSS/P3HT/Al stack completed the device fabrication. Figure 2.7(a) shows the PMOLED pattern imaged from the backside of the glass. The vertical white stripes are ITO patterns and the horizontal stripes are stacks of PEDOT:PSS/P3HT/Al. The intersections of the vertical and the horizontal lines are individual OLED pixels. Each pixel is addressable by applying a turn-on voltage to its corresponding row and column electrodes. Figure 2.7(b) shows an array of electrically biased OLED pixels. Each pixel is a 50 μm square. Since the pitch is 100 μm and the duty cycle is 50%, this method easily demonstrated a PMOLED display of 254 dots per inch (DPI) resolution.

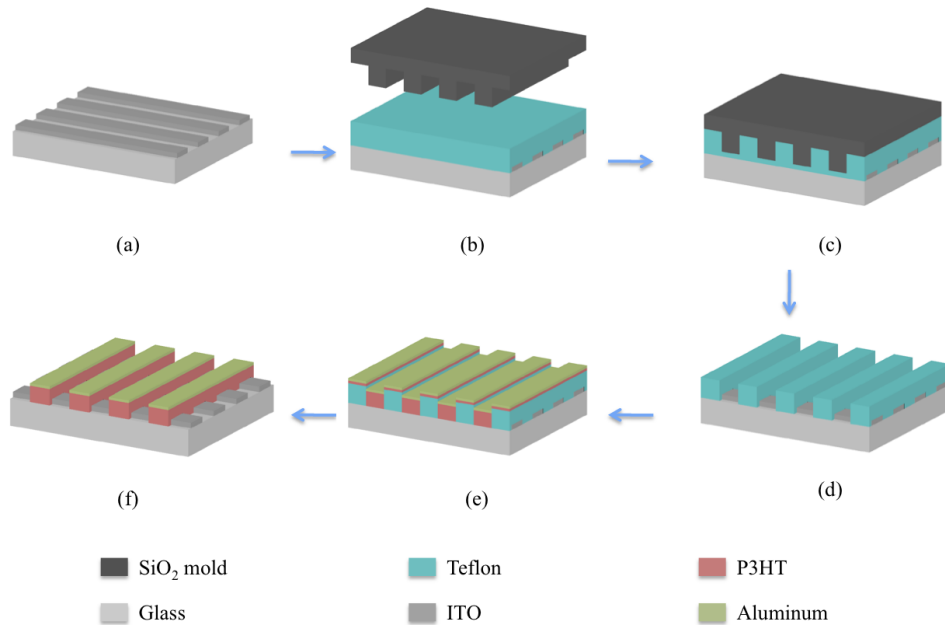


Figure 2. 6. Schematics of the fabrication process for the passive-matrix organic light-emitting diode (PMOLED) array. (a) Pattern ITO on a glass substrate. (b) Spin-coat Teflon-AF on the substrate. (c) Thermally imprint Teflon-AF with a nanoimprint mold. (d) Remove the residual layer by oxygen RIE. (e) Deposit a stack of PEDOT:PSS, P3HT and Al. (f) Dissolve the Teflon-AF template to liftoff the PEDOT:PSS/P3HT/Al stack on the template.

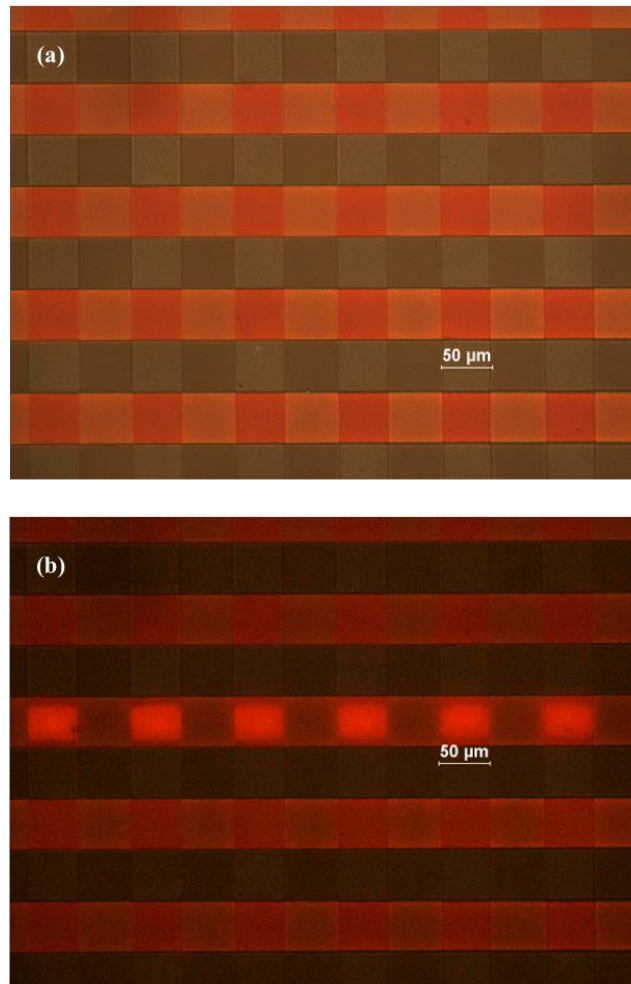


Figure 2. 7. PMOLED array patterned by nanoimprint and sacrificial template. (a) The vertical stripes are 50 μm ITO patterns and the horizontal stripes are stacks of PEDOT:PSS/P3HT/Al. The intersections of the vertical and the horizontal patterns are OLED pixels. (b) Optical image of the electrically biased PMOLED array.

2.3.4 Advantages and future development

By using the fluorinated template patterned by nanoimprint as the intermediate step, I have successfully achieved non-destructive patterning of organic semiconductor structures. Patterning isolated organic semiconductor structures with nanoimprint has several advantages over other printing or photolithography-based techniques. First,

nanoimprint technique has high-resolution capability and this characteristic easily enables high-resolution organic semiconductor structures. Although the smallest structure we demonstrated here is 350 nm, there is no fundamental limitation on smaller patterns. Potentially sub-100 nm structures can be attained. Second, nanoimprint ensures well-defined patterns with very low line edge roughness. The pattern size, shape and line edge roughness are determined by mold patterns, which can be precisely controlled with mature microelectronic processing of thermally grown SiO₂. In printing-based techniques, the spreading of organic semiconductor ink can smear the pattern shape and change the pattern size. Third, nanoimprint has extended its application to roll-to-roll processing to achieve a fast and low-cost patterning[33], and 3-D nanoimprint to realize self-aligned lithography that overcomes the difficulty of layer-to-layer alignment in fabricating electronic devices[34, 35]. The proposed technique has no limitation to be adapted to both roll-to-roll processing and 3-D nanoimprint. Fourth, the technique presented here can be applied to all organic semiconductors, including organic small molecules. It is expected that thermally evaporating small molecules and lifting off in fluorinated solvents can achieve isolated structures of small molecules. Finally, the overall process is still simple and low cost, and it can be easily extended to fabricate integrated organic electronics in large scale.

It is also noticed that the presented technique needs further tailoring and optimization. First, poor adhesion between P3HT and the substrate resulted in the missing of a few structures after lifting off in the ultrasonic bath. This can be addressed by using coupling agents, such as amine silanes[36], to improve the adhesion between

organic semiconductors and the silicon or silicon oxide surfaces. Second, the tall edges in P3HT patterns may become an issue in some device fabrications. This issue can be easily addressed by pressing the patterned structures with a flat mold to smooth out the tall edges.

High-resolution patterning of isolated organic semiconductor structures is expected to have many applications in organic electronics. It can be used to directly pattern OLED arrays for flat-panel display and solid-state lighting applications. The sub-micron and deep sub-micron organic semiconductor patterns can also be used to fabricate high performance OFETs with high cut-off frequencies. Also, the isolated patterns enable the possibility of fabricating organic integrated circuits because devices are isolated from each other to prevent cross interference.

2.4 Conclusion

The proposed method combining NIL and fluorinated template processing has successfully demonstrated the capability of patterning isolated P3HT structures from $0.35\mu\text{m}$ to tens of microns. Inherited from traditional NIL, this technique is capable of generating high-resolution structures. Additionally, this technique achieves nondestructive patterning of organic semiconductors because oxygen RIE is not directly applied to the P3HT thin film and the FC-40 solvent is compatible with organic semiconductors. The patterning technique demonstrated here is not limited to P3HT. It is applicable to all organic semiconductors, both solution-processed and vapor-deposited materials. Moreover, the technique can be extended to directly fabricate organic

electronic device arrays. In the case of PMOLED fabrication, this technique provides a proof-of-concept demonstration. Although P3HT is not the optimized material for OLED application, other materials suitable for OLEDs can be used in the future for flat-panel display and solid-state lighting applications.

CHAPTER III
FABRICATING ORGANIC METAL-SEMICONDUCTOR FIELD EFFECT
TRANSISTOR (OMESFET) OF SELF-ALIGNED BOTTOM GATE

3.1 Introduction

Organic electronics have become a potential research topic due to their attractive advantage of low-cost fabrication, and the possibility of making flexible electronic devices. Today, continuous evolutions of organic semiconductors and modifications of the device structure have gradually improved the device performance[37, 38]. Even though the device performance has been greatly improved in the past few years, organic field effect transistors (OFETs) still need a lot of effort to be used in practical applications due to its high operational voltage and low operational frequency.

Organic field effect transistors are mainly classified as organic metal-insulator-semiconductor field effect transistors (OMISFETs) and organic metal-semiconductor field effect transistors (OMESFETs) according to the device structure[39]. The structure of OMISFETs contains an insulating layer between the gate electrode and the semiconducting material. The insulating layer is an important part that influences the operational voltage and the device performance. To build flexible electronics, the insulating layer also needs to be flexible and usually dielectric polymers are preferred[40]. Typically, polymer insulators have low breakdown potentials and low dielectric constants. To prevent the device breakdown, the transistor needs to use a thick polymeric insulating layer, which requires a large gate voltage to induce field effect

charges in the transistor channel. This is the main reason that OMISFETs usually need a large operational voltage. Moreover, the interface between the insulating layer and the organic semiconductor also influences the device performance[41-43]. In MESFETs structure, the gate electrode directly contacts with the organic semiconductor and forms a depletion region in the semiconducting bulk[44, 45]. Such depletion region due to the lack of electric carriers is a nonconductive layer. In the forward bias or without bias at the gate electrode, only a thin depletion layer is formed and the semiconducting bulk mainly occupies the channel region of the transistor. This condition is considered as turn-on status because the channel is able to conduct current through the semiconducting bulk. In the condition of reverse bias, the depletion layer expands and eventually occupies the entire organic semiconductor, turning off the conducting channel[46]. This on/off mechanism only requires a relatively low voltage compare to OMISFETs. Therefore, OMESFETs is actually a potential device to be used for low voltage circuit applications[47, 48].

OMESFETs in current literature are built as top gate and bottom source/drain configuration with organic semiconductors sandwiched between the gate and the source/drain because of its simple fabrication process. However, the top gate configuration is difficult to restrict the gate electrode to the channel region and therefore the gate has a large overlap area with source and drain. Such large overlap causes a large parasitic capacitor between electrodes and greatly lowers the device cut-off frequency[49]. Therefore, a bottom gate, bottom source/drain configuration becomes a better device structure for high-speed circuit applications because the overlap area can

be reduced. Figure 3.1 shows schematic diagrams of OMESFET in both top gate configuration and bottom gate configuration. The minimized electrode overlap in the bottom gate structure can reduce the capacitance and provides the device a higher cut-off frequency. However, when the device dimension is greatly shrunk, it becomes more and more difficult to pattern the bottom gate by an optical alignment system. In this research, I propose a method to fabricate a self-aligned gate electrode for OMESFET by employing nanoimprint lithography (NIL). This approach does not require a highly accurate alignment system and is able to align the gate electrode easily in the channel region without contacting with source/drain electrodes.

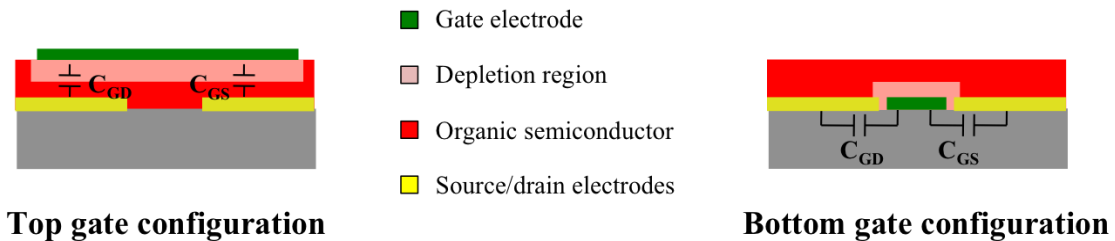


Figure 3. 1. Schematic diagrams of OMESFET in both top gate configuration and bottom gate configuration. The overlap area between the gate and the source/drain in the bottom gate structure is smaller than that in top gate structure.

3.2 Experimental method

Figure 3.2 illustrates the cross-section of the fabrication process. (a) A layer of 40 nm gold (Au) was first deposited on a SiO₂ substrate with 4 nm Chromium (Cr) as an adhesion layer and then 400 nm poly(methyl methacrylate) (PMMA) was spin-coated on the top of the Au as an imprinting resist. (b) The PMMA layer was thermally imprinted by a mold with a protrusive stripe of 270 nm tall and 10 μm wide. (c) The mold was

released from the PMMA film, leaving a thin PMMA residue layer on the Au surface. (d) Oxygen RIE was used to remove the PMMA residue layer and expose the Au/Cr. (e) The exposed Au/Cr layer was etched by the diluted Au etchant and Cr etchant sequentially. A small area of the Au/Cr underneath the PMMA layer was also over etched, forming an undercut profile. (f) Deposit 25 nm aluminum (Al) as the gate electrode with 3 nm Cr as an adhesion layer. (g) Dissolve the PMMA layer in acetone to liftoff the Al/Cr deposited on the PMMA layer. The separated metals serve as transistor electrodes: source, drain and gate. (h) Spin-coat 40 nm P3HT on the electrodes as the semiconducting layer.

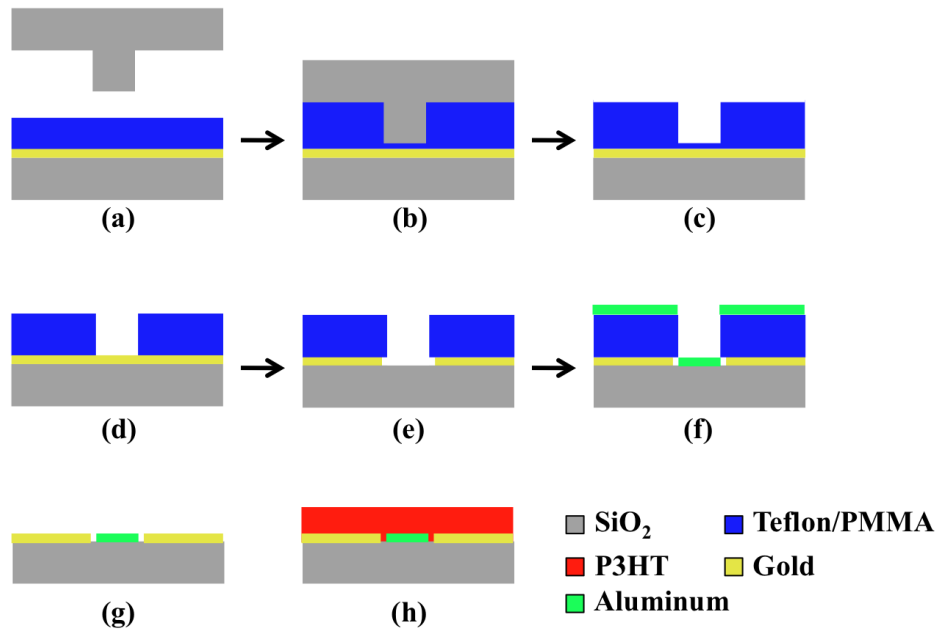


Figure 3. 2. The fabrication process of OMESFETs with a self-aligned gate electrode. (a) Spin-coat an imprinting resist (PMMA or Teflon) on the Au/Cr surface. (b) Thermally imprint the resist. (c) Remove the imprinting mold. (d) Use RIE to remove the residue layer of the resist. (e) Over etch the Au/Cr. (f) Deposit Al/Cr as the gate electrode. (g) Dissolve the resist to liftoff the Al/Cr (h) Spin-coat P3HT.

3.3 Results and discussion

The imprinting process in this experiment was to create a channel region to deposit a gate electrode for the field effect transistor. Here, PMMA was used as the imprinting resist and the imprinting mold made of SiO₂ was coated with perfluorodecyltrichlorosilane (FDTS) in order to easily separate the mold from PMMA. The adhesion between PMMA and Au surface is very poor. In the process of separating mold and imprinting resist, in Figure 3.2(c), most of the PMMA will be peeled off even though the mold has been coated with FDTS. To overcome this issue, the PMMA film was deposited thicker than its standard thickness for the imprinting process. In this experiment, the mold has a protrusive stripe of 270 nm tall and 10 μm wide without repeated pattern. The standard process is to deposit a 300 nm PMMA for the mold to imprint down 270 nm, leaving about 30 nm residue layer. Nevertheless, the PMMA film in this case needs to be deposited at least 400 nm to prevent itself from peeling off. Another solution to solve the adhesion issue is to utilize Teflon-AF as the imprinting resist. The imprinting condition for Teflon-AF has been reported in the previous article[50]. The better adhesion between Teflon-AF and Au allows imprinting a 300 nm Teflon-AF film without peeled off defects. Imprinting a thin resist, e.g. 300 nm film, yields a thin residue layer that requires less RIE etching time to remove residue layer and, therefore, maintains better pattern fidelity.

Etching the Au and Cr metal in the channel region creates two separated metals serving as source/drain electrodes. The channel length, distance between the source and drain electrodes, was 10 μm determined by the protrusive pattern on the imprinting

mold. The channel width was 600 μm determined by the dimension of the Au/Cr metal pattern deposited on the substrate. In order to well control the etching process, a slow etching rate is preferred. Here, both Au etchant and Cr etchant were diluted in DI water in the ratio of 1:2 (etchant: DI water). The wet etching process creates an undercut profile, indicating that small portion of the Au/Cr covered by the PMMA film was also etched because the chemical etchant isotropically etches the metal. This undercut profile ensures the isolation of the gate electrode from source/drain electrodes while depositing the gate metal. The gate electrode in this experiment used Al/Cr (25 nm/3 nm) because Al has a relatively low work function compared with the highest occupied molecular orbital (HOMO) level of the P3HT. The large energy level difference forms Schottky barrier at the interface of Al and P3HT and causes a rectifying response, which exhibits a diode current at the forward bias and does not have a current at the reverse bias. Moreover, the contact of P3HT and Al metal has been proven to form a depletion region in partial of the P3HT bulk[51]. Applying a reverse bias expands the depletion region and eventually turns off the channel because the depletion region occupies the entire P3HT bulk.

The detail of the depletion region in the P3HT film is shown in Figure 3.3. Figure 3.3 (a) shows the expansion of the depletion region when increasing the reverse gate bias. Figure 3.3 (b) illustrates the energy band diagram perpendicular to the gate electrode, explaining the cause of the depletion region and the expansion of the depletion region. The depletion region is caused from the bending of the HOMO level. In the bending region, electric carriers, holes in this case, drift away. Therefore, the depletion

region in the P3HT layer does not conduct current due to the lack of holes. Increasing the reverse gate bias extends the bending area, resulting in the expansion of the depletion region. Figure 3.3 (c) shows the energy band diagram along the source and drain electrodes at equilibrium and under the reverse gate bias. At equilibrium, the barrier between the electrode and P3HT is low, allowing electric carriers to enter the P3HT channel from the Au electrode. When the reverse gate bias increases and turns off the channel, the barrier height increases and blocks electric carriers from entering the P3HT channel.

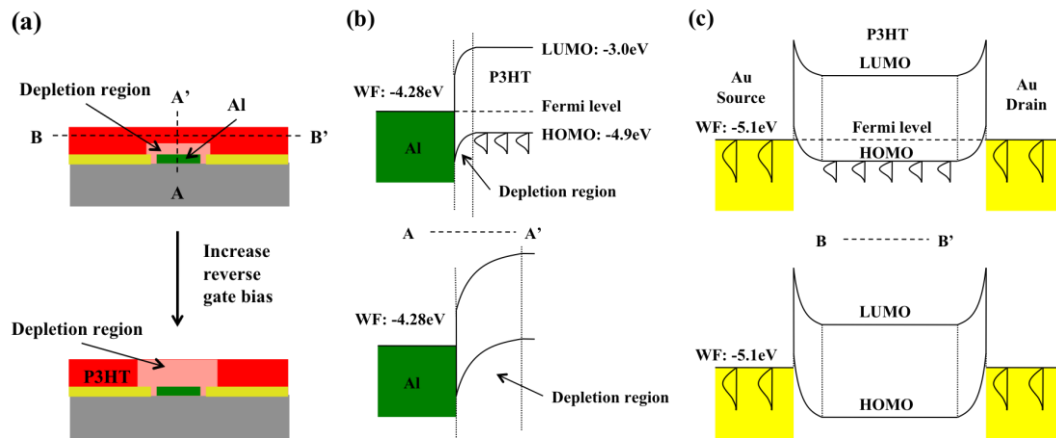


Figure 3. 3. The detail of forming the depletion region. (a) The depletion region expands and turns of the conducting channel when increasing the reverse gate bias. (b) The energy band diagrams perpendicular to the gate electrode show the cause of the depletion region in P3HT and the expansion of the depletion region. (c) The energy band diagrams along the source and drain electrodes show the condition at equilibrium and at the reverse gate bias.

3.3.1 OMESFET of self-aligned gate electrode

The patterning result of the OMESFET electrode is illustrated in Figure 3.4(a). Electrodes are separated by small gaps created by over etching Au/Cr electrodes. As

mentioned previously, this method allows the deposition of Al/Cr metal without contacting with the previous Au/Cr metal, forming a self-aligned gate electrode. Figure 3.4(b) is an atomic force microscope (AFM) image of the device cross-section clearly showing that Au/Cr electrodes are about 45 nm tall and the Al/Cr is about 28 nm tall with small gaps of less than 1 μm separating all the metal electrodes. The dimension of the gap can be modified by controlling the etchant concentration and the etching time. As mentioned above, OMESFET of top gate configuration in most literatures has a large overlap area between the gate and source/drain. Such large overlap area induces a large parasitic capacitor that lowers the cutoff frequency and limits the transistor working in the high frequency region. With this self-aligned structure, the transistor minimizes the electrode overlap area and has a potential to be used for high frequency applications.

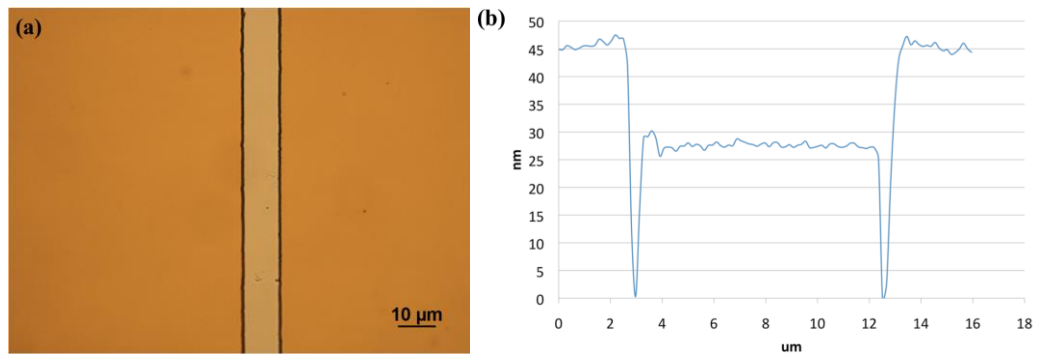


Figure 3. 4. (a) The optical microscope image of the OMESFETs electrodes. The Au source/drain electrodes are separated by the Al gate electrode. (b) The AFM image of the device cross-section.

The transistor of 10 μm channel length and 600 μm channel width was completed by spin-coating 40 nm P3HT on patterned electrodes. The P3HT based OMESFET is considered a normally on transistor, indicating that it is on when no bias is

applied to the gate, and turns off when the gate reverse bias reaches to a certain value. Figure 3.5 illustrates the rectifying response, which measures the gate current while applying a gate bias, suggesting that this OMESFET can be operated in the gate voltage between -1V and at least 3V without having a large gate current flowing to the transistor.

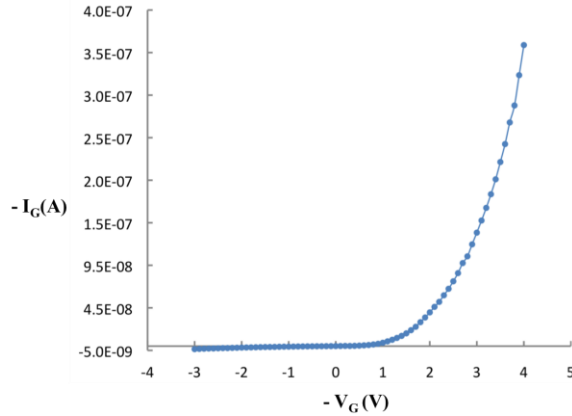


Figure 3. 5. Rectifying response of the MESFET measuring from the Al electrode.

The general form of the rectifying current density can be expressed as the following equation[49].

$$J = J_0(e^{qV_a / \eta kT} - 1)$$

where J_0 is the saturation current density, q is the electric charge, V_a is the applied voltage, η is the ideality factor, k is the Boltzmann's constant, and T is the temperature.

Figure 3.6 shows the width normalized I-V curve of the OMESFET, and the transfer characteristics at V_D of -10V. From the transfer characteristic, the value of transconductance g_m and on/off ratio can be extracted[49]. The value of g_m extracted

from this OMESFET is $5.69\text{E-}7$ (Ω^{-1}). The on/off ratio in this case is about 1.63 in the gate operational voltage between 0V and 2.4V.

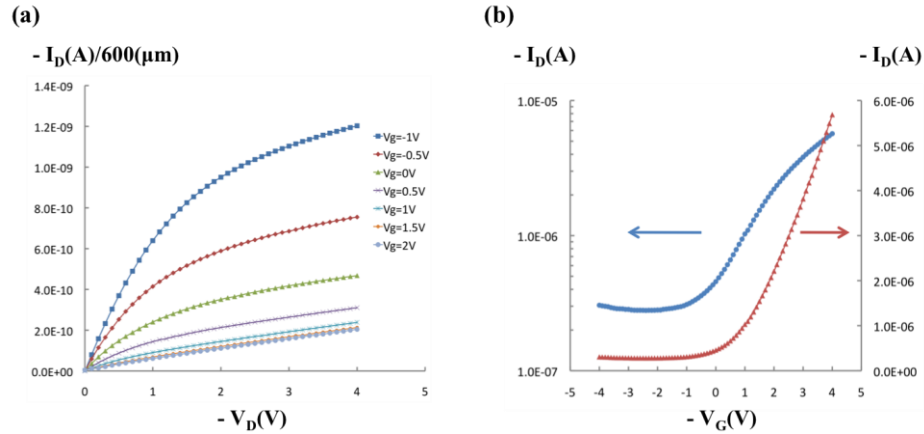


Figure 3. 6. Electric responses of the P3HT based OMESFETs of 10 μm channel length and 600 μm channel width. (a) Width normalized I-V response. (b) Transfer characteristics.

The working principle of how the OMESFET conducts currents between the source and the drain electrodes is illustrated in Figure 3.7. When the drain electrode is negatively biased, the energy band along the source and drain electrode will be bended and an electric field will be generated in the P3HT channel. This electric field drives carriers flowing from the source electrode to the drain electrode through the channel opening, resulting in a drain current.

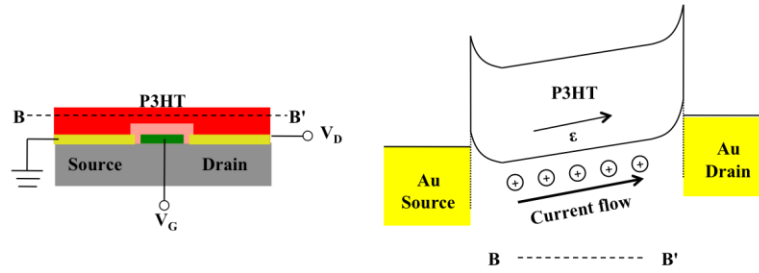


Figure 3. 7. The electric field in the P3HT film drives the current flowing from the source electrode to the drain electrode.

The OMESFET can operate in either the linear region or the saturation region depending on the magnitude of the drain voltage. Figure 3.8 shows the P3HT channel diagrams in both the linear region and the saturation region. The notation t is the channel depth, r is the channel opening, W_D is the depletion layer width, W_{Ds} is the depletion layer width at the source end, and W_{Dd} is the depletion layer width at the drain end. In the linear region as shown in Figure 3.8 (a), carriers entering from the source electrode can flow through the large channel opening r as described in Figure 3.7 because the depletion region width W_D is thinner than the channel depth t . Thus, the drain current increases linearly with the increasing of the drain voltage. When the drain voltage continuously increases, the depletion layer width at the drain end can reach to the same thickness as the channel depth ($W_{Dd} = t$) as shown in Figure 3.8 (b). Here, the depletion layer width at the source end (W_{Ds}) does not change because the voltage difference between the source and gate is not changed. In this condition, the channel pinch-off and the current goes into the saturation region.

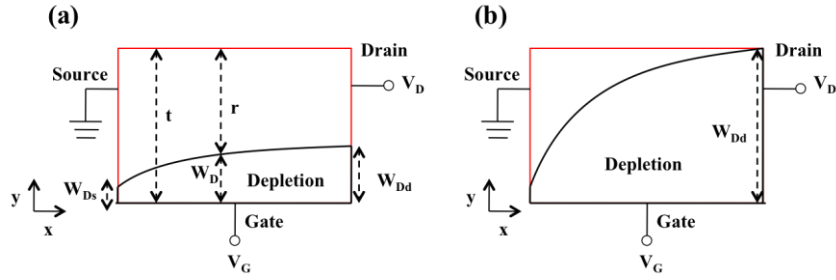


Figure 3. 8. The P3HT channel diagram in (a) the linear region and (b) the saturation region.

The general form of the drain current can be expressed as the following equation[49].

$$I_D = \frac{Zq\mu N_A t}{L} \left\{ V_D - \frac{2}{3\sqrt{\psi_p}} [(\psi_{bi} + V_D - V_G)^{3/2} - (\psi_{bi} - V_G)^{3/2}] \right\}$$

where Z is the channel width, q is the electric charge, μ is the carrier mobility, N_A is the carrier concentration, t is the P3HT channel depth, L is the channel length, ψ_p is the pinch-off potential, and ψ_{bi} is the built-in potential at the source end.

In the linear region ($V_D \ll V_G$ and $V_D \ll \psi_{bi}$), the drain current can be reduced to the following equation[49].

$$I_{Dlin} = \frac{Zq\mu N_A t}{L} \left(1 - \sqrt{\frac{\psi_{bi} - V_G}{\psi_p}} \right) V_D$$

In the saturation region, the drain current can be expressed as the following equation[49].

$$I_{Dsat} = \frac{Zq\mu N_A t}{L} \left[\frac{\psi_p}{3} - (\psi_{bi} - V_G) \left(1 - \frac{2}{3} \sqrt{\frac{\psi_{bi} - V_G}{\psi_p}} \right) \right]$$

□

From the drain saturation current, the transconductance can be expressed as the following equation[49].

$$g_m \equiv \frac{dI_{Dsat}}{dV_G} = \frac{Zq\mu N_A t}{L} \left(1 - \sqrt{\frac{\psi_{bi} - V_G}{\psi_p}}\right)$$

In this experiment, however, the OMESFET hardly reaches flat saturation currents and it is difficult to completely turn off the drain current at a reverse gate bias, resulting in a low on/off ratio. The possible reason is that the entire fabrication was processed in the atmosphere that causes oxygen doping to P3HT, and thus increases the conductivity of the P3HT film, resulting in a high off current.

3.3.2 Self-aligned metal in nanoscale

This approach also demonstrates patterning self-aligned metal gratings in nanoscale. Figure 3.9(a) shows the AFM images of alternating Au and Al lines. Al lines were deposited on the area on which Au had been removed by wet etching. One duty cycle of the Au line and the Al line is about 700 nm. The Au line is about 20 nm tall and the Al line is about 30 nm tall as shown in Figure 3.9(b). They are separated by a small gap created by wet etching the Au metal. This result shows that this approach can also be used in nanoscale electronics. However, the wet etching process is a non-uniform etching. As shown in Figure 3.9(a), the edge of the Au metal appears rough in shape. To resolve this issue in the future, the Au metal can be etched by using reactive ion etching (RIE) that provides an uniform and more controllable etching processing.

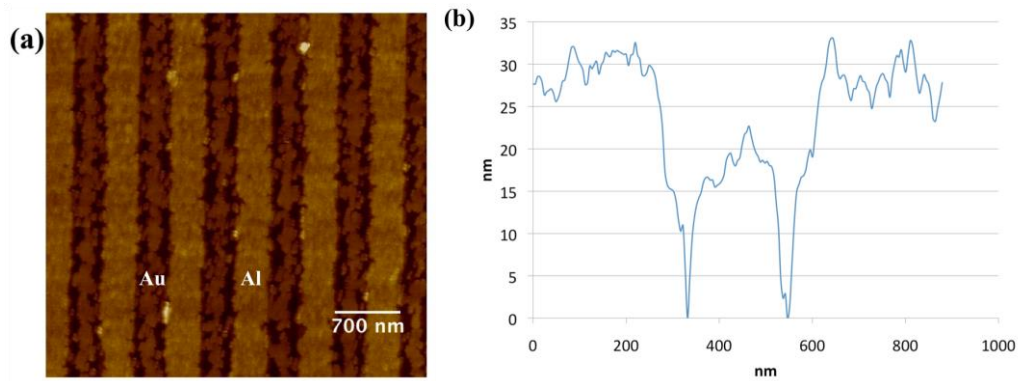


Figure 3. 9. Alternating Au and Al metal lines in nanoscale. (a) AFM image. (b) Cross-section.

3.4 Conclusion and future work

This work has successfully fabricated a gate self-aligned OMESFET of 10 μm channel length and 600 μm channel width by using NIL. The transistor in this work has the potential to be operated in the high-frequency region due to the reduction of overlap area between the gate and source/drain electrodes that causes a high parasitic capacitor. The transistor is also expected to be operated in a lower operational voltage region compared to OMISFET. These two advantages make the OMESFET a better candidate to be used in the practical circuit applications. However, the OMESFET hardly reaches flat saturation currents and it is difficult to turn off the drain current at the large gate reverse bias, resulting in a low on/off ratio. The possible reason is that the fabrication is processed in the atmosphere that induces oxygen doping to the P3HT and increases the conductivity of P3HT. In the future, processing P3HT and the device measurement need to be handled in a glove box with an inert gas environment, such as N_2 or Ar. This work also demonstrated self-aligned metal lines in nanoscale. Alternating Au and Al lines in

nanoscale were achieved. This approach shows the capability of patterning nanoscale self-aligned electrode. However, removing Au by chemical wet etching causes rough edge. This issue is expected to be resolved by using RIE etching in the future.

Moreover, parameters such as the pinch-off potential, the carrier concentration and the carrier mobility can be extracted for future work. To obtain those values, a C-V curve measured from Au-P3HT-Al stacking structure is needed. The C-V relation of the structure can be expressed as the following equation.

$$C = \sqrt{\frac{q\epsilon N_A}{2(\psi_{bi} - V)}}$$

where ϵ is the permittivity of P3HT. By inversely squaring the capacitance, a C^{-2} -V curve can be obtained. The C^{-2} -V equation can be expressed as the following equation.

$$C^{-2} = \frac{2(\psi_{bi} - V)}{q\epsilon N_A}$$

The built-in potential is the intersection of the curve extrapolation and the voltage axis. The drain voltage of the OMESFET in the saturation condition has the following relation.

$$V_{Dsat} = \psi_p - \psi_{bi} + V_G$$

As the built-in potential and the drain voltage have been known, the pinch-off potential can be obtained by setting V_G to 0 V. The pinch-off potential can be expressed as the following equation. From this equation, the carrier concentration can be extracted.

$$\psi_p = \frac{qN_A t^2}{2\epsilon}$$

□

The saturated drain current expressed in the previous section can be used to find the carrier mobility of the OMESFET because, except for the carrier mobility, all the parameters have been known.

CHAPTER IV
HIGH-RESOLUTION PATTERNING BY POLYMERIC SIDEWALL
TRANSFERRED LITHOGRAPHY

4.1 Introduction

The fabrication of nanoscale patterns has become an important topic due to the increasing need to shrink devices in integrated circuits in order to improve device performance and reduce power consumption. To achieve this goal, many advanced techniques have been employed such as deep ultraviolet lithography (DUV)[52], extreme ultraviolet lithography (EUV)[53], and electron beam lithography[54]. Although these novel techniques are able to create ultra-small structures, their high-cost process makes these techniques not commonly accessible. Especially for E-beam lithography, its time-consuming process is not practical for large volume manufacturing. Currently, an emerging technique, nanoimprint lithography (NIL), has demonstrated a low-cost, high-resolution, and high-throughput capability for nanostructure fabrication[8, 14, 33]. With these merits, it has been widely used in many device applications[50, 55-57]. However, a master mold of pre-defined patterns is required to perform NIL. Although the mold can be used for many times, a new mold always needs to be fabricated when launching a new design. To pattern nanoscale structures, the mold is traditionally made by E-beam lithography, a relatively high-cost and time-consuming processing. Therefore, in order to reduce the fabrication cost and time from above techniques, an alternative method capable of fabricating nanostructures needs to be

considered. The purpose of this work is to develop a low-cost and time-saving technique to generate nanostructures without expensive and sophisticated equipment.

The proposed method is realized by transferring polymeric sidewall layers into substrate. The sidewall layer is created by spin-coating a polymer solution on a pre-patterned template, which can be generated by either photolithography or NIL with existing molds. The template has a vertical wall for the polymer solution to spread vertically and form a polymeric sidewall layer. The dimension of the sidewall layer is very easy to reach nanoscale and is controllable by changing processing parameters. A similar method has been reported by using chemical vapor deposition (CVD) to deposit a silicon nitride (Si_3N_4) as a sidewall layer[58, 59]. Comparing the proposed technique with the CVD based sidewall transfer lithography, the proposed method is easier and faster, and does not require a vacuum and high temperature environment. Therefore, this technique can be used not only in the silicon-based substrate but also potentially in soft polymeric substrates.

4.2 Experimental method

In this experiment, 1 wt% PMMA and 2 wt% Teflon-AF solutions were prepared in advance. PMMA was dissolved in toluene solvent and Teflon-AF was dissolved in FC-40 fluorinated solvent. The PMMA solution was then filtered before using. Figure 4.1(a) to 4.1(k) illustrates the experimental process. (a) First, the Teflon-AF solution was spin-coated on the silicon substrate to form a uniform Teflon-AF film, and (b) the film was imprinted with an existing NIL grating mold, (c) forming a Teflon-AF template. (d)

After removing the Teflon-AF residue layer by oxygen reactive ion etching (RIE), the PMMA solution was then spin-coated on the Teflon-AF template so that (e) a PMMA layer can cover the whole template. (f) The PMMA residue layer was also removed by oxygen RIE, leaving only PMMA sidewall layers attached to the template. (g) After dissolving the Teflon-AF template in the FC-72 solvent, PMMA nanoscale sidewalls were formed. In order to transfer sidewall patterns into the substrate, (h) a thin chromium (Cr) layer was then deposited on the substrate and sidewall patterns. (i) The Cr layer was used as an etching mask after removing PMMA sidewalls. (j) After etching the silicon substrate and (k) removing the Cr layer, PMMA sidewall patterns were transferred into the silicon substrate.

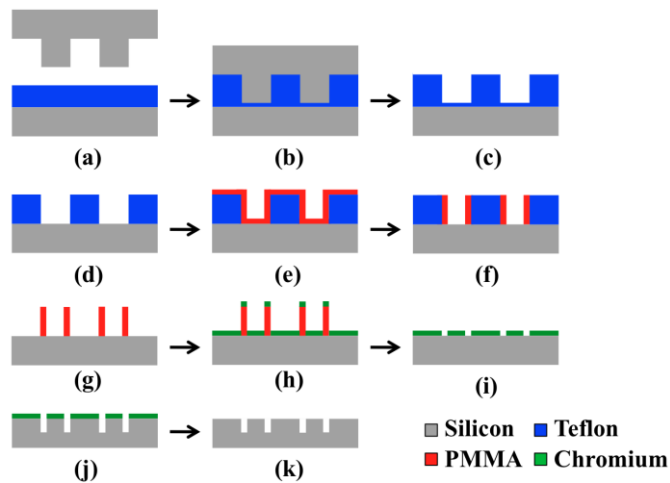


Figure 4. 1. Schematics of the experimental processing. (a) Spin-coat the Teflon-AF solution to form a thin film. (b) Thermally imprint the film with a grating mold. (c) The pattern of the mold is transferred into the Teflon-AF film. (d) Remove the Teflon-AF residue layer by oxygen RIE. (e) Spin-coat the PMMA solution on Teflon-AF. (f) Remove the PMMA residue layer by oxygen RIE. (g) Dissolve Teflon-AF by FC-72 solvent. (h) Deposit a thin Cr layer. (i) Remove the PMMA sidewalls and liftoff the Cr on the PMMA. (j) Use Cr as a mask and etch the silicon substrate. (k) Remove the Cr layer.

4.3 Results and discussion

4.3.1 Sidewall fabrication and pattern transfer

To create polymeric sidewall layers, a template of vertical walls is needed for the polymer solution to spread vertically and to form a thin layer. In this work, the template was created by NIL with an existing mold. The mold used in this experiment was a 700 nm periodic grating of 300 nm trenches, 400 nm protrusions and 350 nm depth as shown in Figure 4.2. The template material to be patterned uses Teflon-AF, because it is a fluorinated polymer dissolved only in fluorinated solvents, which enables another solution process on top of it; for example, spin-coating the PMMA solution on the Teflon-AF template is completely feasible because toluene cannot dissolve the Teflon-AF template during spin-coating. Regarding creating the template by photolithography, a fluorinated photoresist is required[15]. Although this type of photoresist has been reported for practical applications such as fabricating organic light emitting diodes and organic thin film transistors, it is still not commercially available. In this experiment, FC-40 was selected as the solvent used for dissolving Teflon-AF and making the Teflon-AF solution[31], because it is a relatively thick solvent and has a high boiling point of 158°C–173°C making it an ideal solvent to create a very uniform Teflon-AF film on the substrate. Here the Teflon-AF solution was spin-coated on the silicon substrate at 800 rpm, forming a 230 nm Teflon-AF film. The film was then baked on a hot plate at 100°C to completely dry the FC-40 solvent.

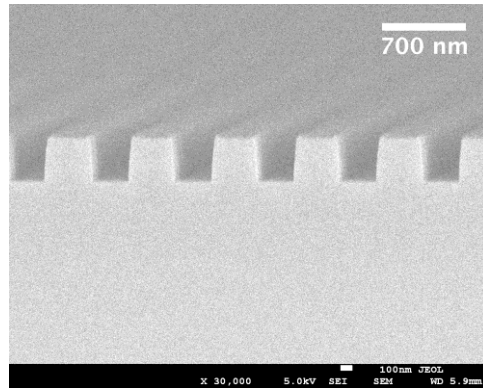


Figure 4. 2. The nanoimprint mold of 700 nm periodic grating with 300 nm trenches, 400 nm protrusions and 350 nm depth.

In this experiment, the Teflon-AF film was thermally imprinting at 230°C and 900 psi[50]. To prevent the Teflon-AF film from peeling off from the substrate, the silicon substrate was primed with hexamethyldisilazane (HMDS), which improves the adhesion between the substrate and the film. To prime the substrate, HMDS was spin-coated on the silicon substrate at 4000 rpm and the substrate was then soft-baked at 120°C for 3 minutes before coating with Teflon-AF. The mold was also coated with perfluorodecyltrichlorosilane (FDTS) in order to easily separate the mold and the imprinted Teflon-AF template. To coat the mold with FDTS, a small amount of FDTS was dropped into heptane, and the mold was immersed into the heptane for 10 minutes. Afterward, the mold was baked at 110°C for 1 minute. With an HMDS primed substrate and a FDTS treated mold, the Teflon-AF template can strongly attach to the substrate while releasing the mold.

NIL always needs to eliminate the residue layer after mold releasing, as described in Figure 4.1(d). This task is usually processed by oxygen RIE because its

anisotropic etching can maintain the pattern fidelity. The oxygen RIE, in this experiment, used the following conditions: oxygen flow rate 20sccm, chamber temperature 24°C, chamber pressure 10 mtorr, forward power 50 W, and inductively coupled plasma (ICP) 0 W. Under these conditions, the etching rate for eliminating the Teflon-AF residue layer is about 2.3 nm/second. Teflon-AF originally has a highly hydrophobic surface. After removing the Teflon-AF residue layer by oxygen RIE, its surface becomes hydrophilic. The hydrophilic surface benefits the process of spin-coating the PMMA solution on the Teflon-AF template[50]. Here, the PMMA solution was spin-coated at 3000 rpm to form the PMMA layer covering the Teflon-AF template. In this process, 30 nm PMMA residue was also formed in the template trenches. The same RIE conditions to eliminate the Teflon-AF residue was used to remove the PMMA residue layer, as described in Figure 4.1(f). The rate for etching the PMMA residue layer is about 1.4nm/second.

In this experiment, FC-72 was used to remove the Teflon-AF template because, after washing away the Teflon-AF template, it leaves less residue than using FC-40 and it dries faster than FC-40 due to its low boiling point of 50°C–60°C. Dissolving the Teflon-AF template usually forms a very thin residue layer during the drying of FC-72 solution. Hence, 10 seconds oxygen RIE was usually applied to ensure complete removal of the Teflon-AF, leaving only PMMA sidewall layers on the substrate. Figure 4.3 shows the scanning electron microscope (SEM) image of PMMA sidewalls and the sidewall profile when the Teflon-AF template is completely removed. These PMMA sidewalls can easily achieve a dimension of around 30 nm in width.

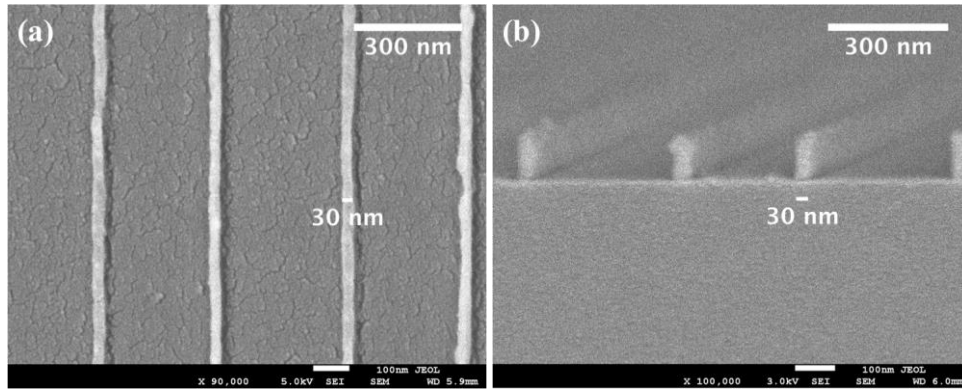


Figure 4. 3. PMMA sidewalls after completely removing the Teflon-AF template. (a) Top view of PMMA sidewalls. (b) The profile of PMMA sidewalls.

Transferring these PMMA sidewalls into the substrate can further achieve nanotrenches as proposed in Figure 4.1(h) to 4.1(k). To do this, 5 nm Cr was deposited as a mask for etching 50 nm in the silicon substrate. The RIE process for the silicon etching used the following parameters: sulfur hexafluoride (SF_6) flow rate 10 sccm, oxygen flow rate 5 sccm, chamber temperature 10°C , chamber pressure 10 mtorr, forward power 50 W and ICP 0 W. Under these conditions, the rate for the silicon etching is about 2.4 nm/second. This method successfully created trenches of about 30 nm in width after etching the silicon and removing the Cr mask. Figure 4.4(a) shows the top-view of the nanotrenches and Figure 4.4(b) shows the profile of the trench patterns. The width of trenches is almost the same as that of PMMA sidewalls, which suggests that the trench dimension is determined by the sidewall dimension. The original mold only determines the repeating cycle of the trench pattern. The result also demonstrates that this technique is able to produce 30nm trenches without employing DUV, EUV, or E-beam lithography. Most importantly, the entire process is relatively low-cost, time-

saving and does not require sophisticated equipment. Compared with the conventional method to deposit Si_3N_4 sidewalls, this method does not need a vacuum and high temperature environment.

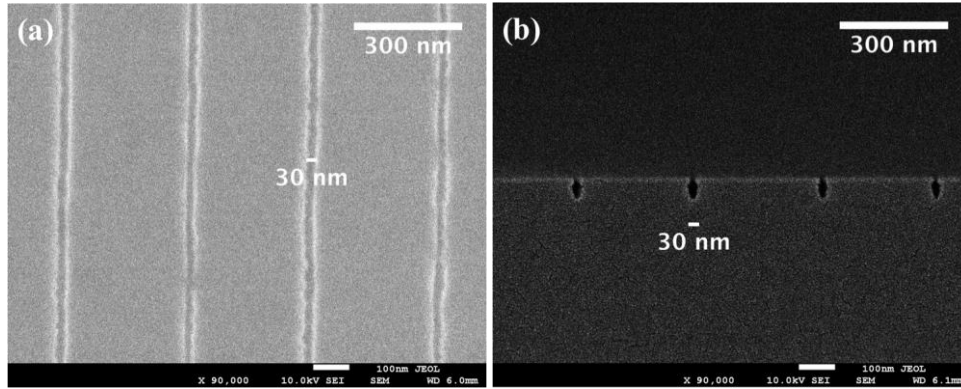


Figure 4. (a) The top-view of the trench patterns after transferring sidewalls into the substrate. (b) The cross-section of the trench patterns.

4.3.2 Change of trench dimension

Since the width of the PMMA sidewall determines how wide the trench is, adjusting the width of the sidewall is a practical way to change the trench dimension. The PMMA sidewall changes its size with processing parameters, the concentration of the PMMA solution or the spin-coating speed. Hence, the trench dimension also can be adjusted by controlling those parameters. In order to investigate how these parameters influence the pattern size, trench patterns created from different solution concentrations and spinning speeds were discussed in the following two cases.

The first case was to examine the influence of the solution concentration on the trench width. In the experiment, 0.5 wt%, 1 wt%, 1.5 wt% and 2 wt% PMMA solutions

were spin-coated on the Teflon-AF template with a randomly selected spinning speed, 3000 rpm. Different solution concentrations produce different sidewall dimensions as well as residue thicknesses. In order to estimate the proper RIE etching time for eliminating the PMMA residue, it is essential to know the residue thickness of each condition. Figure 4.5(a) lists the PMMA residue thickness in the template with respect to its corresponding solution concentrations. With the same process illustrated in Figure 4.1, trench patterns of different widths can be achieved. Figure 4.5(b) shows the trench width with respect to its solution concentrations. This result clearly depicts that the solution concentration is a factor that alters the width of the PMMA sidewall and influences the trench width after transferring sidewall patterns into the substrate. However, the trench dimension does not increase exponentially like the PMMA residue thickness when the solution concentration increases. Instead, its increasing curve tends to slow down. The reason is probably that removing a thicker PMMA residue needs longer RIE time, which causes more side etching on PMMA sidewalls and results in the slow increase of the trench dimension. In this demonstration, we have successfully achieved high-resolution trenches of about 15 nm as shown in Figure 4.5(c) by processing the 0.5 wt% PMMA solution. Although this case has already reached 15 nm structures, achieving an even smaller pattern size is still possible. Similar to spin-coating a polymer solution on a flat surface, forming the sidewall layer is caused by spreading of the polymer solution. The only difference is that sidewalls spread on a vertical wall instead of a flat surface. Therefore, further reducing the solution concentration is still possible to diminish the sidewall thickness so that smaller structures can be fabricated.

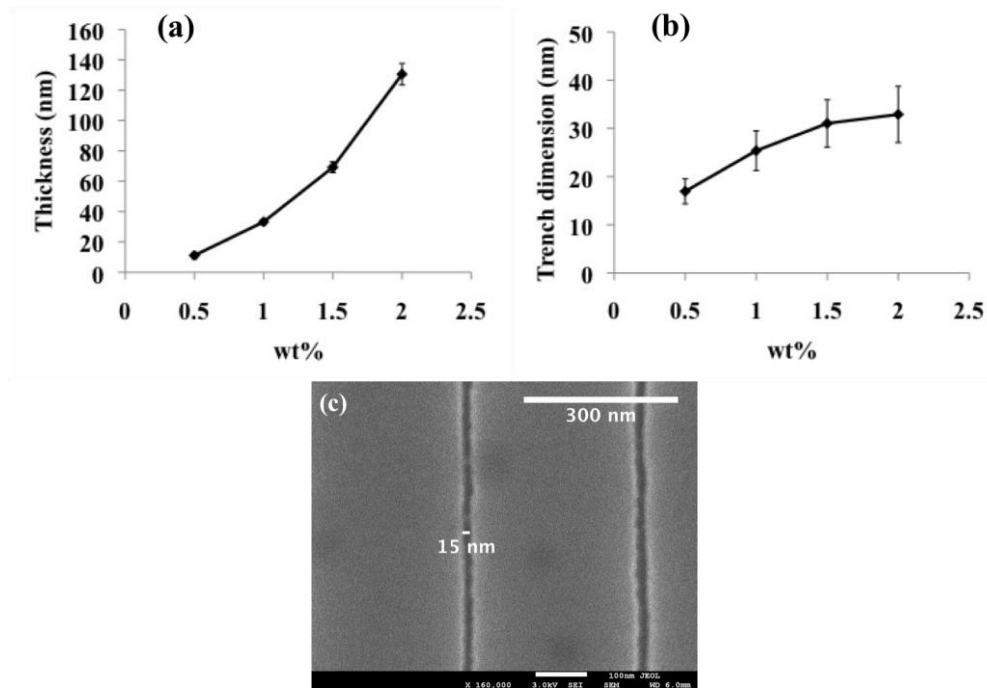


Figure 4. 5. (a) PMMA residue thicknesses in the Teflon-AF template with respect to PMMA solution concentrations. (b) Trench dimensions with respect to PMMA solution concentrations. (c) Trenches of about 15 nm were achieved by processing the 0.5 wt% PMMA solution at 3000 rpm.

For the second case, the influence of the spin-coating speed on the trench width was examined. In this experiment, 1 wt% PMMA solution was selected to coat the template with spin-coating speeds of 1000 rpm, 1500 rpm, 2000 rpm, 2500 rpm, and 3000 rpm. The thickness of the PMMA residue and the trench width generated by different spin-coating speeds are shown in Figure 4.6(a) and 4.6(b). The result shows a tendency of decreasing trench width as the spin-coating speed becomes higher. However, the trench width does not have an obvious change as that in case 1, which indicates that the width of the PMMA sidewall in case 2 does not change significantly when the spin-coating speed changes.

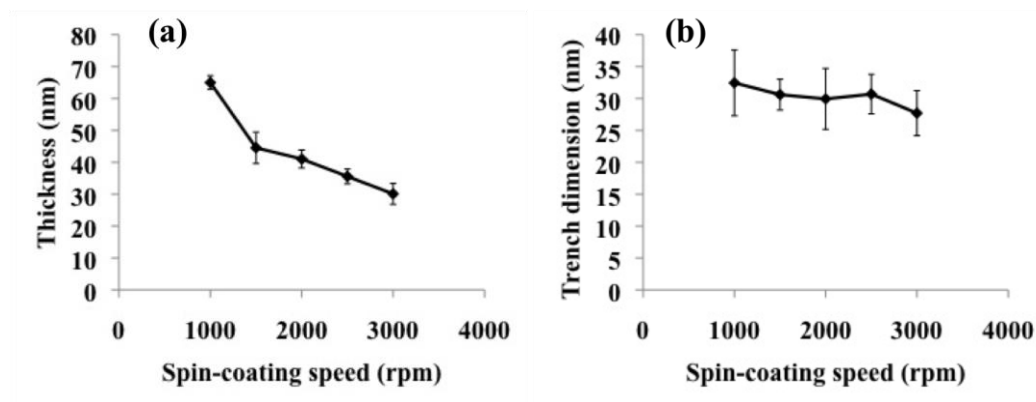


Figure 4. 6. (a) PMMA residue thicknesses in the Teflon-AF template with respect to spin-coating speeds. (b) Trench dimensions with respect to spin-coating speeds.

These two cases demonstrate that the trench dimension can be controlled by adjusting processing parameters. Although both cases show a trend of changing dimension, their changing degrees are not the same. Comparing results of the two cases, the trench (or sidewall) dimension is more sensitive to the concentration of the PMMA solution, especially to the low concentration solution, 0.5 wt% in this case. This suggests that a small variation in the solution concentration can cause a significant difference in the pattern size. Therefore, it is very important to prevent the solvent from evaporating during the storing and processing. As for the spin-coating speed, it is a relatively insensitive parameter to the trench (or polymer sidewall) dimension because the pattern dimension only has a small change over a wide spinning speed range. This indicates that using different spin coaters of a slightly different spin speed does not cause an obvious change in the pattern dimension.

4.3.3 Ring-shaped sidewall contours

This technique has successfully demonstrated nanotrenches, which attributes to its ability to create the nanoscale PMMA sidewall layer. Technically, it is not just limited to the straight-line sidewall. By modifying the NIL mold patterns, sidewalls of various ring-shaped contours were also achieved. Figure 4.7(a), 4.7(b) and 4.7(c) show SEM images of ring-shaped sidewalls of circles, squares, and concentric squares; the inset images are their corresponding molds. Figure 4.7(d), 4.7(e), and 4.7(f) are three-dimensional AFM images of these ring-shaped sidewalls. These PMMA sidewalls repeat the same outline of mold features including the arc and the angle, which potentially enable this technique to extend its applications to create NIL molds, metal line connections in integrated circuits, nanofluidics and nanophotonics.

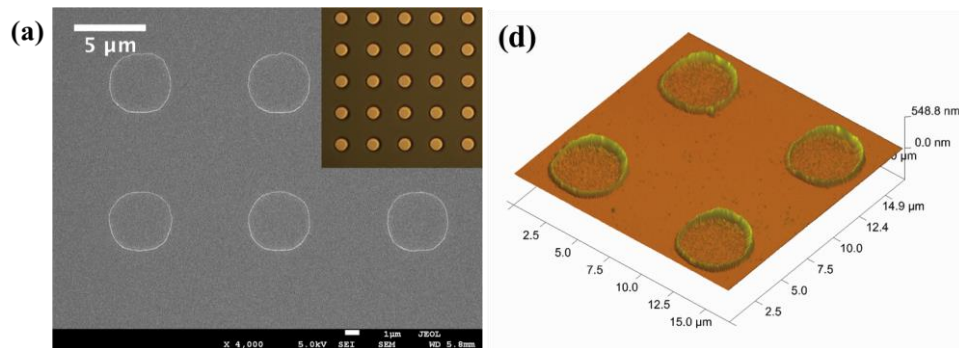


Figure 4. 7. SEM images of PMMA sidewall contours: (a) circles, (b) squares, and (c) concentric squares. The inset images are their corresponding molds for creating the sidewalls. Three-dimensional AMF images of the sidewall contours: (d) circles, (e) squares, and (f) concentric squares.

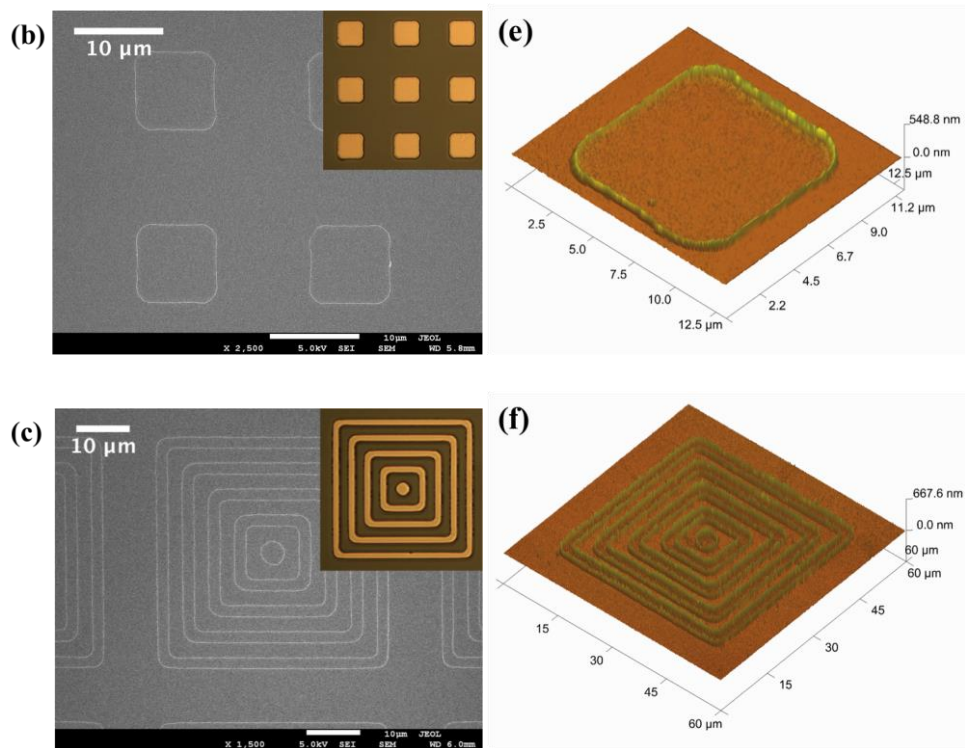


Figure 4. 7 continued.

4.4 Conclusion

This technique is a low-cost and time-saving method to fabricate nanostructures. It has successfully achieved nanotrenches after transferring PMMA sidewalls into the substrate. By changing processing parameters, such as the concentration of the PMMA solution or the spin-coating speed, the width of the trench can also be changed, which is caused by the change of the PMMA sidewall dimension. In this work, 15 nm high-resolution trenches have been achieved. Although this work demonstrated 15 nm structures, a smaller pattern size can possibly be fabricated. The achievement of nanotrenches attributes to the success of fabricating straight-line PMMA sidewalls. By modifying the mold pattern, ring-shaped contours of circles, squares, and concentric

squares were also achieved. These sidewalls of various contours enable this technique to find practical applications not only in fabricating high-resolution NIL molds but also in device applications such as nanoscale metal lines for device connections, nanofluidic devices and nanophotonics. Instead of generating trench structures, this method theoretically can fabricate protrusive structures by using the PMMA sidewall as the mask to anisotropically etch the substrate. Due to its versatility, this technique will be able to explore more applications in the future.

CHAPTER V

FIELD EFFECT SOLAR CELLS

5.1 Introduction

Increasing the efficiency of organic solar cells has been a critical challenge in developing low-cost solar energy harvesting devices. Currently, the maximum power conversion efficiency of the P3HT/PCBM based solar cell, a common organic solar cell, is around 5%[60, 61]. The main issue of this low efficiency is that most of the electron-hole pairs generated by incident photon energy recombine in a very short time[62]. Due to the recombination issue, only a small fraction of photo-generated electrons and holes can be separated and contribute to the output current. Although many techniques have been developed to improve power conversion efficiency, for example, bulk heterojunction (BHJ) solar cells[63, 64] and dye-sensitized solar cells (DSSCs)[65], they still cannot solve the recombination issue because they are designed only to increase the junction interface of the p-type and n-type semiconducting materials, to increase light absorption, and to generate more electron-hole pairs. To efficiently separate electron-hole pairs, a strong electric field is needed. In organic solar cells, the electric field is primarily generated from the work function difference of the anode and cathode electrodes[66]. Such an electric field is too weak to provide a high power conversion efficiency. This issue can be overcome by intentionally introducing an extra electric field into organic solar cells. Recently, a reported research achieved this concept by using a permanent electric field from a poled ferroelectric polymer layer. This research group

added a ferroelectric layer in the organic solar cell to induce an internal electric field, and their results showed that the efficiency was increased from 1–2% to 4–5%[67]. Nevertheless, the strength of the internal electric field is not high enough. In this work, I plan to modify the solar cell structure by introducing an extra electrode in order to generate a large external electric field to assist the separation of electrons and holes, and eventually achieve a higher efficiency.

5.2 Fabrication method

The method to fabricate the proposed solar cell is shown in Figure 5.1. (a) Deposit a 200 nm Si_3N_4 film on 100 nm thermally grown SiO_2 by plasma enhanced chemical vapor deposition (PECVD). (b) Pattern a 30 nm thick Au grating as anode electrodes on Si_3N_4 with a 3 nm Cr as adhesion layer. The patterning method can use either photolithography or nanoimprint lithography (NIL) according to the Au electrode dimension. As an electrode, all the Au grating lines were connecting together. The anode was a 100 μm periodic grating with a 50% duty cycle. (c) Deposit a thin layer of Teflon-AF on the Au grating as a patterning template. (d) A square opening was then created on the Teflon-AF film to expose the Au contact. (e) Deposit 70 nm poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) as the hole transport layer and then deposit a mixture of poly(3-hexylthiophene) (P3HT) and [6,6]-Phenyl-C61 butyric acid methyl ester (PCBM) as the active layer. (f) Deposit an ITO cathode electrode on the P3HT/PCBM film by sputtering coating.

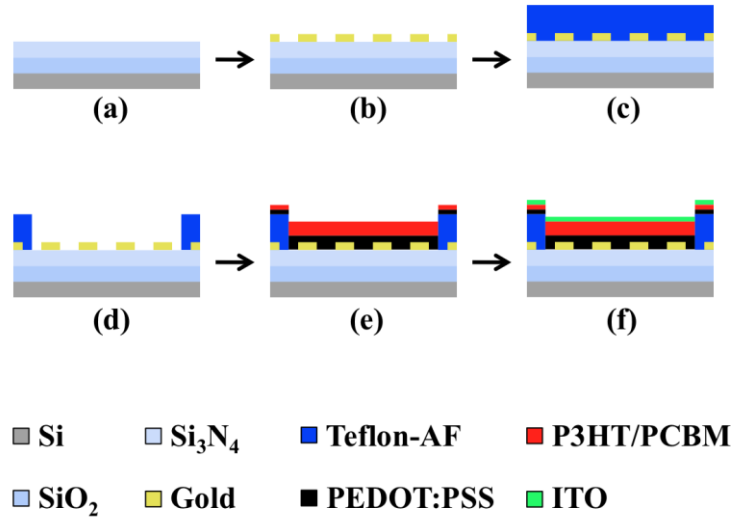


Figure 5. 1. The process of fabricating a field effect solar cell. (a) Deposit Si₃N₄ on thermally grown SiO₂. (b) Pattern Au grating as the anode electrode. (c) Deposit Teflon-AF as a patterning template. (d) Expose Au electrode by patterning the Teflon-AF layer. (e) Deposit PEDOT:PSS as the hole transport layer and mixture of P3HT and PCBM as the active layer. (f) Deposit ITO as a cathode electrode.

5.3 Discussion and measurement results

The principle of the proposed solar cell is to introduce a strong electric field generated by an external electrode to efficiently separate the electron-hole pairs. It is similar to the function of the gate electrode in metal oxide field effect transistors (MOSFETs) that provides an electric field to attract or repel electric charges. Therefore, we name the proposed solar cell “the organic field effect solar cell” (OFESC) and the external electrode “the gate electrode.” To introduce the electric field, an insulating layer needs to isolate the active layer and the gate electrode. In this experiment, the 100 nm thermally grown SiO₂ was used as the insulating layer and the silicon substrate was then used as the gate electrode. To minimize the gate leakage current flowing through the

SiO₂ while not sacrificing too much electric field entering the active layer, a 200 nm Si₃N₄ was deposited on top of the SiO₂ by PECVD instead of continuously growing 200nm SiO₂ because Si₃N₄ has a higher permittivity than SiO₂. The anode electrode was fabricated as the metal grating that allows the electric field to enter the active layer through the grating area not covered by the metal electrode. Figure 5.2 shows the 100 μm patterned Au grating of 50% duty cycle that was used in this experiment.

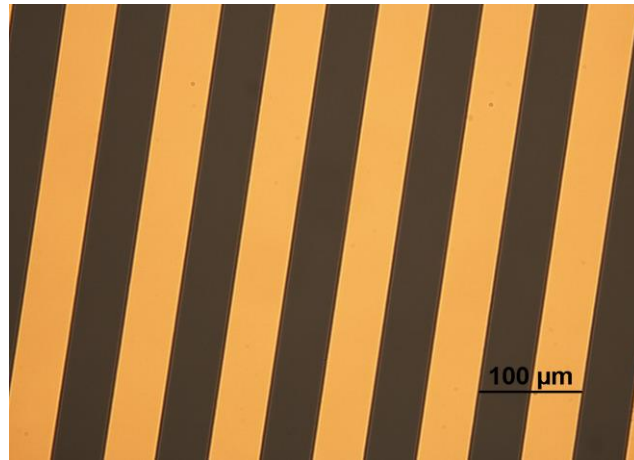


Figure 5. 2. The 100 nm Au grating of a 50% duty cycle patterned on the Si₃N₄ serving as the organic solar cell anode.

In Figure 5.1(c) and 5.1(d), a layer of Teflon-AF was coated on the entire structure and then a square opening of 0.225 cm² was created to expose the electrode. The patterning approach can be either photolithography or NIL. The purpose of exposing a small area of anode was to confine the active layer within the small square area in order to prevent a large leakage current occurring between two large conductive layers, one is the gate electrode and the other one is the large area of active layer. If the active

layer were coated on the entire structure instead of confining it in a small area, a large leakage would occur even if the structure had a thick insulating layer. In this study, the active layer was the mixture of P3HT (p-type) and PCBM (n-type) because it has been widely used for organic solar cells[68, 69]. The 70 nm PETDOT:PSS, a hole transport layer, was first coated on the electrode before depositing the P3HT/PCBM active layer because it helps to increase the solar cell efficiency. The P3HT/PCBM film was baked in the vacuum oven for 1 hour at 150°C. The baking process causes phase separation of P3HT and PCBM. The phase separation creates numerous junction interfaces between P3HT and PCBM and increases the efficiency of the device[70, 71]. The reason to use ITO as the cathode electrode is because it is a transparent material that allows the incident light to penetrate itself and to be absorbed by the active layer. Here, the ITO was deposited on the active layer by sputtering coating.

The experimental setup for testing the OFESC is illustrated in Figure 5.3. This setup uses two sourcemeters (Keithley 2400) to implement three terminals: anode, cathode, and gate. The only difference between the OFESC and the conventional solar cell is the additional gate terminal in the OFESC structure; the bias applied to the anode and cathode is the same as the conventional solar cell. The measurement for the conventional solar cell is described in Appendix A. As shown in Figure 5.3, the extra gate bias induces an electric field to separate electron-hole pairs. Ideally, the power conversion efficiency increases when applying a negative gate bias and decreases when applying a positive gate bias.

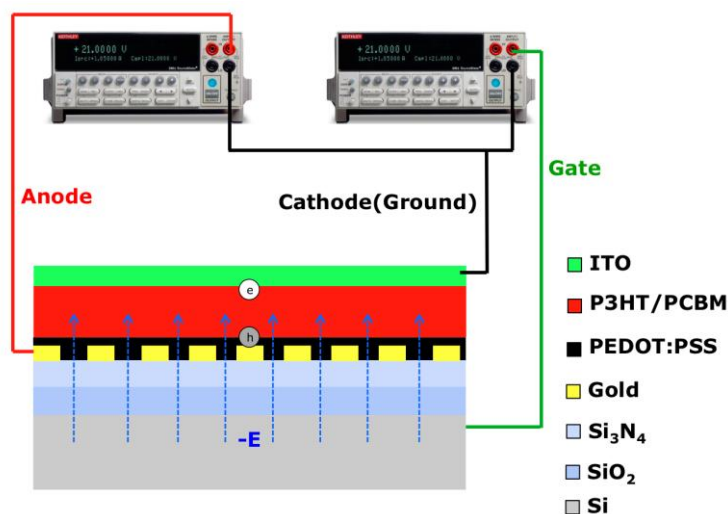


Figure 5. 3. The experimental setup for testing the organic field effect organic solar cell (OFESC) and the OFESC device structure.

The measurement results are shown in Figure 5.4. The x-axis represents the applied voltage (measured in volt) between anode and cathode electrode and the y-axis represents the current density (measured in ampere/cm²) flowing through the anode. The light source is a Xenon lamp calibrated by a standard light source and an integrating sphere. In this experiment, the power output of the light source was around 150 mW/cm². Figure 5.4(a) presents J-V curve of the OFESC in both dark and light conditions without any gate bias. The current density was measured from the anode electrode at various electric biases. From the curve in the light condition, the output power of the solar cell can be extracted as 93.795 μ W/cm². Hence, the power conversion efficiency without gate bias was 0.0625%. The detail of obtaining the power conversion efficiency is described in Appendix A. Figure 5.4(b) to 5.4(g) are OFESC responses to various gate biases in the light condition. In each figure, the green line represents the response of 0 V gate bias, the red cross represents the positive gate bias, and the blue

circle represents the negative gate bias. Theoretically, the negative gate bias increases the solar cell efficiency (the blue circle response shifts down from the green line response) while the positive gate voltage decreases the solar cell efficiency (the red cross response shifts up from the green line response). However, according to those J-V responses, the external gate bias inducing the electric field did not contribute to the device efficiency even at a high voltage of 80 V. In Figure 5.4(g), the J-V responses at the gate bias of +80 V and -80 V show the same response as that of 0 V gate bias. Such phenomenon suggests that the external electric field does not influence the solar cell response in this device. In Figure 5.4(h), high voltages of ± 100 V were applied to the gate electrode and changed the output curve. The reason that causes this change is that the large leakage current flows through the insulating layer and dominates the output curve. Figure 5.4(i) shows the leakage current measuring from the gate terminal.

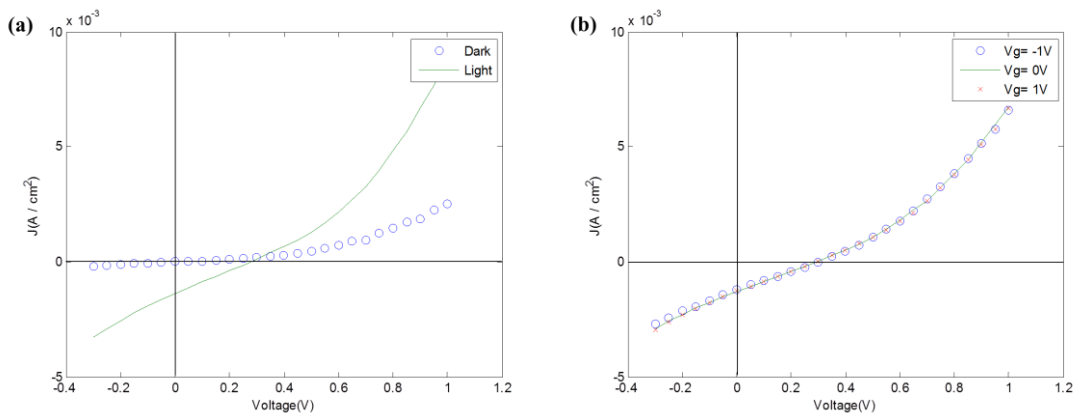


Figure 5. 4. (a) The electric responses of the OFESC in both dark and light environments. (b) – (g) Electric responses of the OFESC in various gate biasing conditions without large gate leakage currents. (h) The electric responses of the OFESC at a large gate biases of ± 100 V. (i) Large gate leakage currents occur measuring from the gate terminal at ± 100 V gate bias.

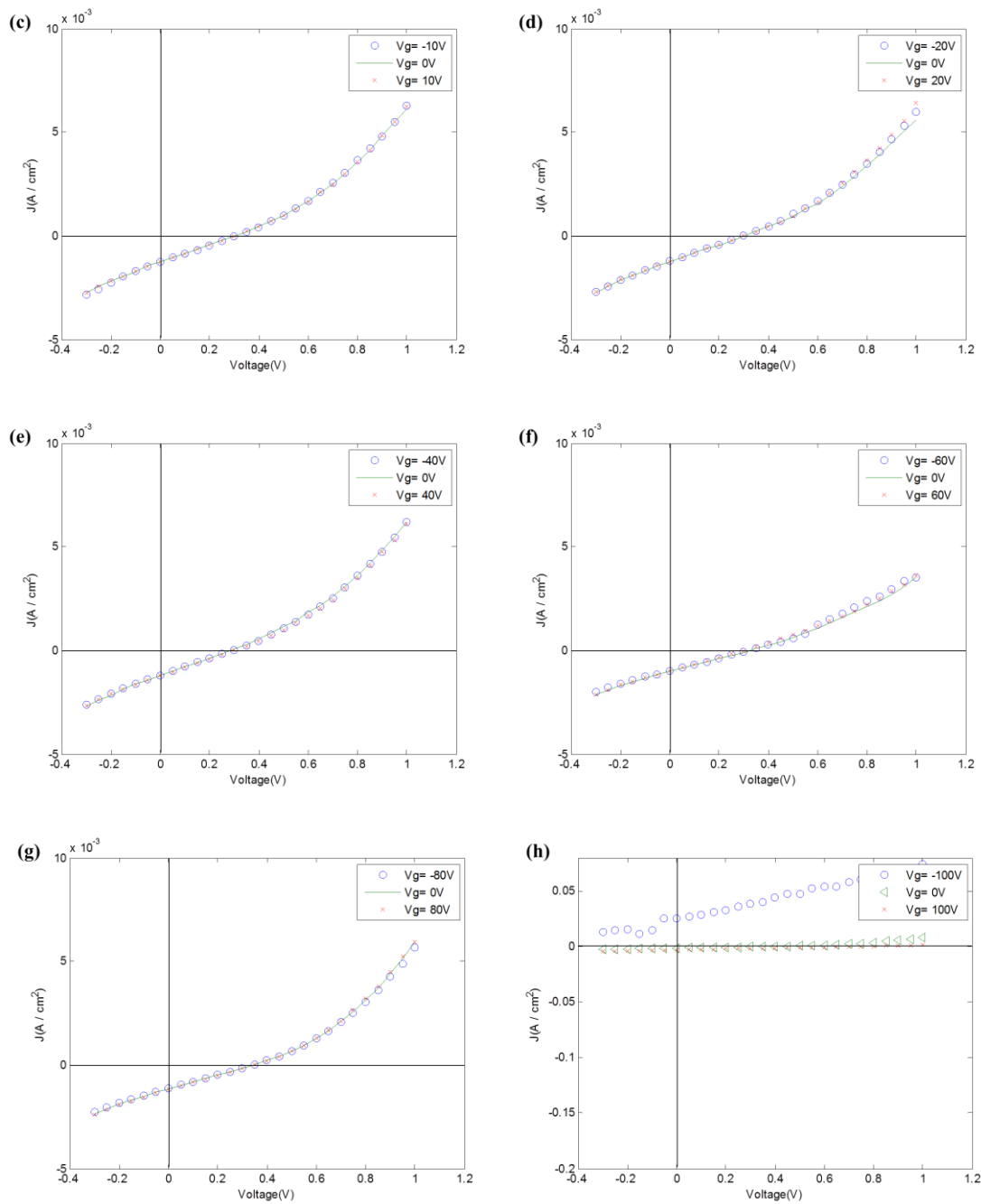


Figure 5. 4 continued.

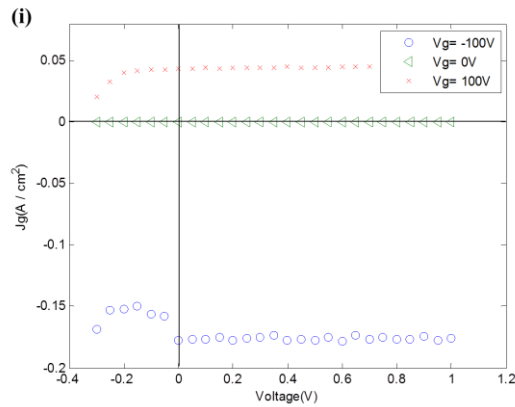


Figure 5. 4 continued.

5.4 Conclusion and future work

The prototype of OFESC has been fabricated and measured in this experiment. Based on its J-V responses at various gate biases, the external electric field did not influence the solar cell performance. Continuously increasing the gate bias eventually results in a large leakage current flowing through the insulating layer. The possible reason for not showing the field effect could be that the electric field entering the active layer was too weak to separate electron-hole pairs due to the thick insulating layer. For future work, I plan to use a dielectric layer that has a higher permittivity than that of Si_3N_4 and deposit it on the SiO_2 , for example Al_2O_3 or HfO_2 , in order to induce a stronger electric field in the active layer and efficiently separate electron-hole pairs. Moreover, other parameters such as different dimensions of Au grating and the thickness of active layers will be examined.

CHAPTER VI

CONCLUSIONS AND FUTURE WORKS

Patterning high-resolution organic electronics has been an important topic toward advanced device applications, such as integrated circuits and flat-panel displays. In this study, patterning methods for organics electronics were investigated primarily based on NIL due to its potential advantages of high-resolution and high-throughput. Fabricating organic electronics includes patterning organic semiconductors and metal electrodes. In the first work, NIL was used to pattern organic semiconductors and isolated P3HT structures from 0.35 micron to tens of microns were achieved. This technique is a nondestructive patterning for organic semiconductors because oxygen RIE that is used for eliminating the residue layer is not directly applied to the P3HT film. The fluorinated solvent for removing the sacrificial template is also fully compatible with organic semiconductors. This method is applicable to all organic semiconductors, both solution-processed and vapor-deposited materials. Based on this approach, PMOLED was also fabricated for the flat panel display application. Although P3HT is not an optimized material for OLED application, other materials suitable for OLED can be used in the future.

In the second work, NIL was also used to fabricate a self-aligned metal gate electrode for OMESFET of 10 μm channel length and 600 μm channel width. The transistor was expected to operate in the low voltage, high-frequency region due to the lack of the dielectric layer and the minimized overlap area between gate and source/drain

electrodes. However, in this experiment it is difficult for the transistor to reach saturation current and to turn off the drain current at the large gate reverse bias, resulting in a low on/off ratio. The possible reason for these two phenomena is that the fabrication is processed in the atmosphere that induces oxygen doping to P3HT, making it more conductive. This issue can be resolved by processing the fabrication in an inert gas environment, such as N₂ or Ar. Self-aligned and alternating Au and Al lines in nanoscale were also demonstrated. Each duty cycle of the Au and the Al line is about 700 nm. This approach shows the capability of patterning nanoscale self-aligned electrodes, but removing Au by chemical wet etching causes a rough edge. This issue can be resolved by using reactive ion etching in the future. Other researches for organic field effect transistors are discussed in Appendix. In Appendix B, an encapsulation method for organic devices is demonstrated, and in Appendix C, a method is investigated to improve the performance of OFETs by reducing the contact resistance.

Considering that the fabrication of a high-resolution NIL mold requires sophisticated equipment as well as an expensive and time-consuming processing, a low-cost and time-saving method to fabricate nanostructures was developed in the third work. This work has successfully achieved nanotrenches by transferring PMMA sidewalls into the substrate. The dimension of PMMA sidewalls can be changed by varying processing parameters, such as the concentration of the PMMA solution or the spin-coating speed, which also change the pattern dimension on the substrate after transferring PMMA sidewalls. By transferring PMMA straight-line sidewalls, 15nm high-resolution trenches were achieved. PMMA sidewall contours of circles, squares,

and concentric squares were also achieved. These sidewalls of various contours enable this technique to find practical applications in fabricating not only high-resolution NIL molds but also nanoscale metal lines for device connections, nanofluidic devices and nanophotonics.

Finally, the prototype of an organic field effect solar cell (OFESC) structure has been proposed in this study. Both the anode electrode and the P3HT/PCBM organic semiconductors can be patterned by NIL. Based on its J-V responses, the experimental result did not meet the theoretical expectation. The possible reason could be that the electric field was too weak to separate electron-hole pairs due to the thick insulating layer. For future work, in order to induce a stronger electric field in active layer and efficiently separate electron-hole pairs, a dielectric layer that has a higher permittivity than that of Si_3N_4 , such as Al_2O_3 or HfO_2 , needs to be used. Other parameters such as different dimensions of the Au grating and the thickness of the active layer will also be examined.

In summary, these proposed methods of the first three studies, patterning organic semiconductors, patterning metal electrodes and fabricating nanoimprint molds, have been proven to match with theoretical concepts. Although some of the results are not perfect, they can be improved in the future with further modifications of experimental design, which include using a better organic semiconductor for the OLEDs application (chapter II); processing organic semiconductors in an inert gas environment, and using RIE to etch metal contact in order to achieve smooth edges (chapter III). These prove-of-concept approaches have achieved the expected NIL merits, high-resolution patterning

capability. This merit enables a facile route towards nanoscale organic electronics. The other advantage, high-throughput capability, is expected to be achieved in future work by replacing the thermal NIL with roll-to-roll imprinting lithography or step and flash imprinting lithography (SFIL). For the OFESC project, the device structure was fabricated according to the proposed method. However, the electrical measurement did not meet the expected response. The unexpected result doesn't mean that the proposed structure cannot achieve the goal because a similar theory has successfully been demonstrated in organic field effect transistors. With proper modifications on the device structure described in chapter V, the expected field effect response could be achieved in future work. During the course of this research, these proposed methods have achieved most of their expectations and show the versatility of NIL. NIL is indeed a promising technique to develop organic electronics. In the future, other device applications can be explored based on NIL or those novel approaches proposed in this study.

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APPENDIX A

P3HT/PCBM BILAYER ORGANIC SOLAR CELL

In this experiment, a conventional bilayer solar cell made of P3HT (P-type) and PCBM (N-type) organic semiconductors was fabricated and measured in order to investigate the fabrication process and its power conversion efficiency. The fabrication process started with depositing a thin PEDOT:PSS as a hole transport layer on indium tin oxide (ITO) glass substrate by spin-coating (2000 rpm) the PEDOT:PSS solution, followed by P3HT and then PCBM deposition. To deposit the P3HT/PCBM bilayer by the solution processing, P3HT was dissolved in dichlorobenzene to obtain a P3HT solution (15 mg/mL) and PCBM was dissolved in dichloromethane to obtain a PCBM solution (10 mg/mL). The P3HT solution was first spin-coated (400 rpm) on the PEDOT:PSS to form the P3HT layer and the PCBM solution was then spin-coated on the P3HT layer to form the PCBM layer. Here, depositing the PCBM layer doesn't dissolve the P3HT layer because P3HT is insoluble in dichloromethane. Finally, Al was deposited on top of the PCBM layer by thermal evaporation.

The solar cell structure and the measurement setup are shown in Figure A. 1. In the device structure, the ITO serves as an anode electrode and Al serves as a cathode electrode. The measuring system used a Keithley sourcemeter 2400 to acquire electric output from the solar cell. The connection of the sourcemeter to the device is that the positive port to the anode and the negative port to the cathode. The light source used in the solar cell characterization was a Xenon lamp that can simulate sunlight and was

calibrated by a standard light source and an integrating sphere. Here, the light power was measured 250 mW/cm^2 . When the organic solar cell is exposed in this light environment, an electrical potential will be built between the anode and cathode, resulting in a photo current in the external connection.

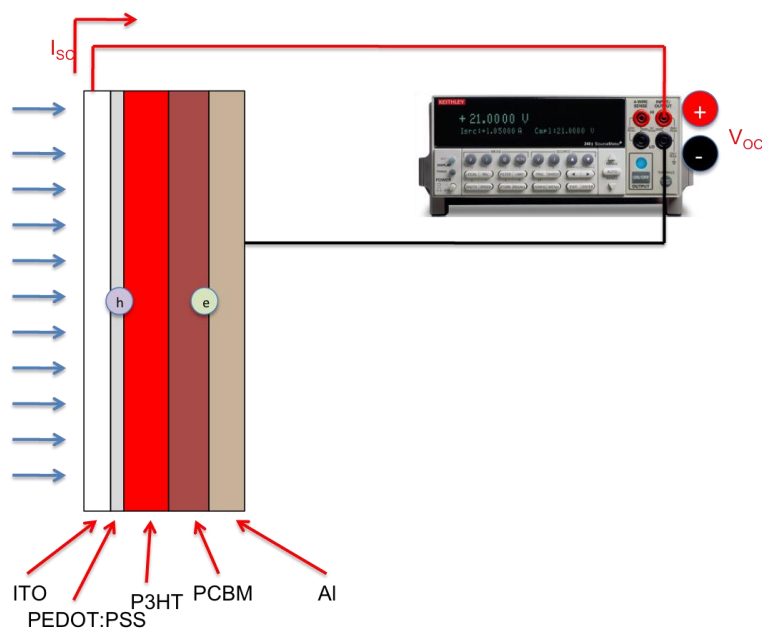


Figure A. 1. The device structure of the P3HT/PCBM organic bilayer solar cell and the experimental setup for the solar cell measurement.

Figure A. 2 is the energy diagram of the bilayer organic solar cell explaining the solar cell working principal. With an incident light entering the solar cell, electron-hole pairs known as Frenkel excitons will be generated in the P3HT layer. The electron-hole pairs diffuse to the interface between P3HT and PCBM, and dissociate into electrons and holes. Via an electric field between the anode and the cathode, electrons move to the

cathode electrode, while holes move to the anode electrodes. Thus, the device can output a current.

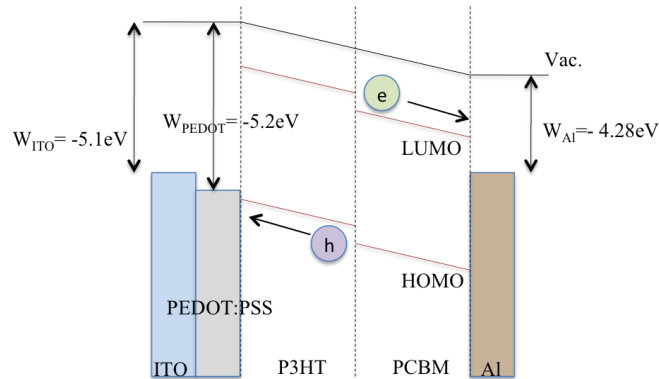


Figure A. 2. The energy diagram of the P3HT/ PCBM bilayer solar cell.

To evaluate the performance of an organic solar cell, the power conversion efficiency is usually an important factor. The power conversion efficiency can be calculated from the electric output (current density-voltage characteristics) of the solar cell. Figure A. 3 is the solar cell output characteristics in both dark and light environment. The output in the dark condition is basically a diode response. In the light condition, the diode response shifts down, intersecting with the X-axis, the open-circuit voltage (V_{OC}), and the Y-axis, the short-circuit current density (J_{SC}). The maximum output power of the solar cell is the maximum rectangular area within the region of the output curve and X-Y coordinates. The power conversion efficiency is therefore the ratio of the maximum output power to the incident light power.

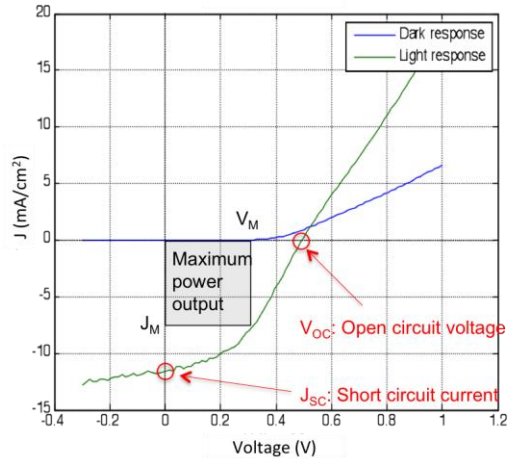


Figure A. 3. The electric output of the organic solar cell. The blue line is the output in the dark environment and the green line is the output in the light environment. The maximum power output of the solar cell is the maximum rectangular area within the region of the green line and X-Y coordinates.

The power conversion efficiency of the organic solar cell can be expressed by the following equations.

$$\eta = \frac{P_{out,max}}{P_{in}} = \frac{J_M \times V_M}{P_{in}} = \frac{V_{OC} \times J_{SC} \times FF}{P_{in}}$$

where $P_{out,max}$ is the maximum output power, P_{in} is the incident light power, J_M and V_M are the current density and the voltage of the maximum power output respectively, V_{oc} is the open circuit voltage, J_{sc} is the short circuit current density, and FF is the fill factor.

Fill factor is the other factor that can be used for evaluating the performance of the solar cell[72, 73] and it is given by the following equation.

$$FF = \frac{J_M \times V_M}{V_{OC} \times J_{SC}}$$

□

Here, the input optical power was 250 mW/cm^2 . From the light response, we measured the maximum output power to be 2.43 mW/cm^2 . Therefore, the device has a power conversion efficiency of 0.97%, and a fill factor of 41.5%.

APPENDIX B

ENCAPSULATION FOR ORGANIC TRANSISTORS

This experiment was to investigate an encapsulating approach for the P3HT-based organic field effect transistors (OFETs). P3HT is a fragile organic semiconductor and can be deteriorated in the moisture and light[74]. Therefore, organic electronics made of P3HT organic semiconductor need to be isolated from the moisture and light. In this experiment, Teflon-AF and Al were used to encapsulate P3HT because Teflon-AF can repel the moisture and Al can block light. Moreover, Al_2O_3 forming on the Al layer can prevent oxygen doping to the P3HT layer. Here, two identical P3HT based OFETs were fabricated in a bottom gate and bottom contact configuration. After fabrication, one device was encapsulated by Teflon-AF and Al, and the other one did not have any encapsulation. The device structures of these two OFETs are shown in Figure B. 1.

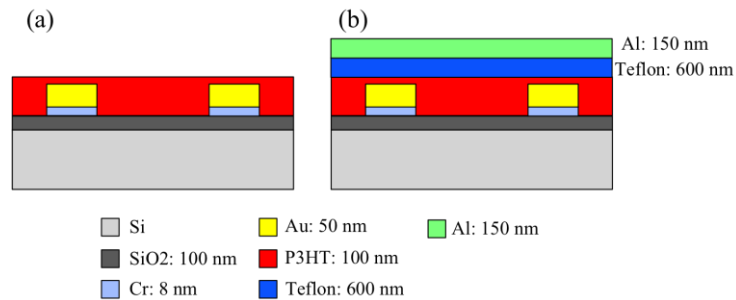


Figure B. 1. The device structures of the P3HT based OFETs. (a) without encapsulation. (b) with encapsulation.

These OFETs were fabricated on the 100 nm thermal SiO_2 . The Si substrate serves as the gate electrode and the SiO_2 serves as the dielectric layer. The source and

the drain electrodes were 50 nm Au with 8 nm Cr as the adhesion layer patterned by the conventional photolithography. The P3HT active layer (100 nm) was deposited by spin-coating the P3HT/dichlorobenzene solution. To encapsulate the device, Teflon-AF and Al were additionally deposited on the P3HT layer. The Teflon-AF layer (600 nm) was deposited by spin-coating a Teflon-AF/FC-40 solution. The Al layer (150 nm) was deposited by thermal evaporation.

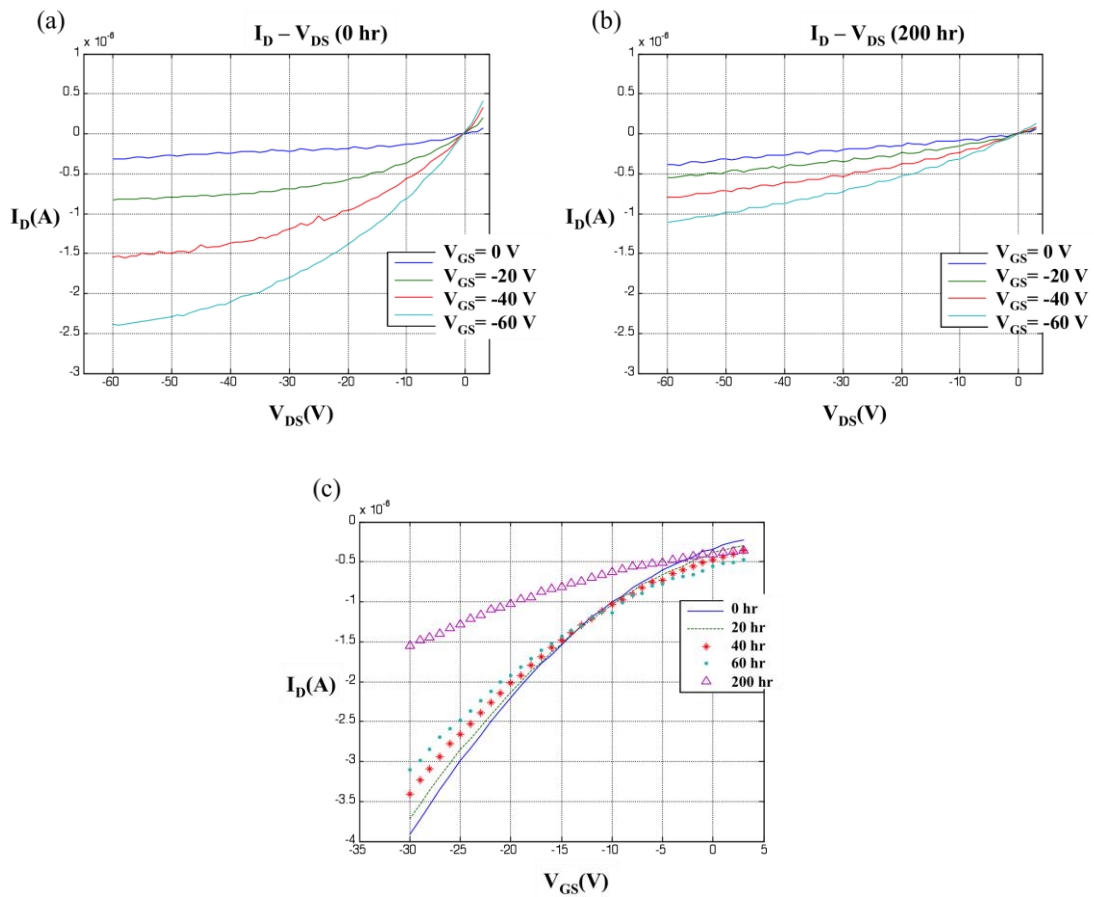


Figure B. 2. Device measurements of the P3HT OFETs without encapsulation. (a) The $I_D - V_{DS}$ curve measured as the device was just fabricated. (b) The $I_D - V_{DS}$ curve after exposing the device 200 hours to the air. (c) Transfer characteristic measured at different time.

These two devices were exposed to the atmosphere for more than 200 hours. Measurements were taken after devices were just fabricated and after devices were exposed to the air for 20 hours, 40 hours, 60 hours and 200 hours. Figure B. 2 show device measurements of the P3HT OFETs without encapsulation. Figure B. 2 (a) and (b) are drain current - drain voltage (I_D - V_{DS}) measurements after the device fabrication, and after 200 hours. Figure B. 2 (c) is the transfer characteristic at different exposing times.

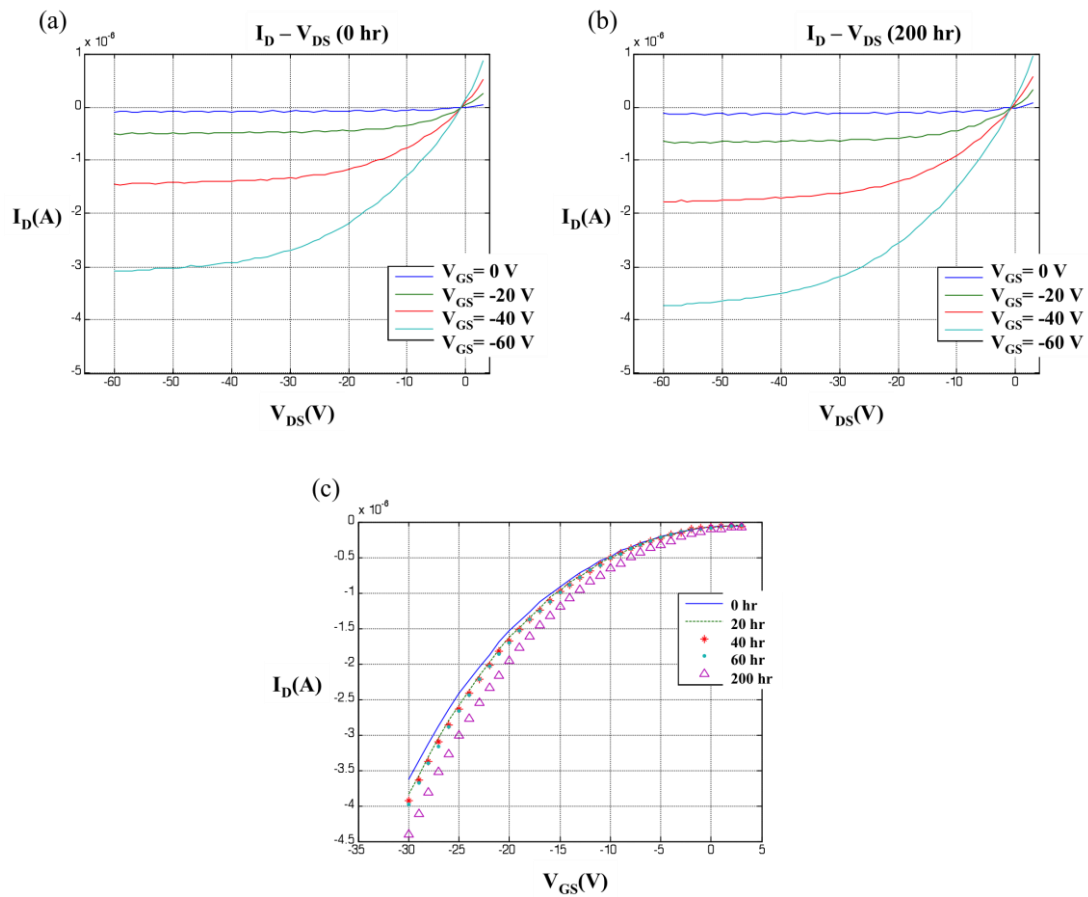


Figure B. 3. Device measurements of the encapsulated P3HT OFETs. (a) The I_D - V_{DS} curve measured as the device was just fabricated. (b) The I_D - V_{DS} curve after exposing the device 200 hours to the air. (c) Transfer characteristic measured at different time.

Figure B. 3 show measurements of the encapsulated OFETs. Figure B. 3 (a) is the I_D - V_{DS} measurement right after the device fabrication, and Figure B. 3 (b) is the I_D - V_{DS} measurement after exposing the device 200 hours to the atmosphere. Figure B. 3 (c) is the transfer characteristic measured at different exposing times. According to these measurements, the device without encapsulation encounters a severe deterioration after 200 hours. For the device encapsulated by Teflon-AF and Al, although the device after 200 hours becomes more conductive which might be the effect of the oxygen doping, it can still function as an OFET and maintain the original device property.

In summary, using both Teflon-AF and Al is a practical method to encapsulate P3HT based OFETs because Teflon-AF repels the moisture and Al can efficiently block light. Comparing the two devices in this experiment, the encapsulated device exhibits longer lifetime than that without encapsulation. Therefore, this encapsulating method can be used as a reference approach for the development of P3HT based organic electronics in the future.

APPENDIX C

REDUCTION OF CONTACT RESISTANCE IN P3HT BASED ORGANIC FIELD EFFECT TRANSISTORS

Today, organic field effect transistors (OFETs) have exhibited many attractive advantages, such as low cost and low temperature processing, flexible electronics, and large area electronic application. However, their low performance is still an issue for circuit applications. One of the important factors that can impact the performance is the contact resistance. OFETs usually experience a high contact resistance due to a high carrier injection barrier between the electrode and the organic semiconductor. For p-type OFETs, gold (Au) is usually selected as electrodes because Au has a high work function to easily inject holes into the HOMO level (similar to the valence band in silicon based semiconductors) of p-type organic semiconductors. In this experiment, P3HT (p-type) was selected as the organic semiconductor for fabricating OFETs. To reduce the contact resistance, 1.3 nm selenium (Se) was coated on the Au electrodes because, for P3HT, Se has a lower injection barrier than Au. This experiment compared contact resistances of two different electrode contacts in P3HT based OFETs. One was the conventional Au contact and the other one was the Au contact coated with 1.3 nm Se. Both of them were bottom gate and bottom source/drain contact. In this experiment, the channel resistance of these two cases was also compared.

OFETs in this experiment were built on the 100 nm thermal grown SiO₂, which also serves as a gate dielectric layer. The source and the drain electrodes were patterned

by photolithography, thermal evaporation and liftoff processing. In the thermal evaporation, 8 nm Cr was first deposited as an adhesion layer before depositing 50 nm Au. Other samples were additionally deposited 1.3 nm Se on the Au. After completing the source and the drain electrodes, P3HT/dichlorobenzene solution (15 mg/mL) was spin-coated on the electrodes with 800 rpm to form a P3HT film. Without an encapsulation, P3HT can be deteriorated in the moisture and light[74]. In order to prevent the device from degradation, Teflon-AF 1600 and Al were used for encapsulating the devices. Teflon-AF is a highly moisture repellent, and Al reflects light and forms a dense Al_2O_3 to prevent the moisture and oxygen from entering the P3HT active layer. In this experiment, 2 wt% Teflon-AF solution (dissolved in FC-40) was spin-coated on the P3HT layer with 800 rpm to form a 230 nm Teflon-AF layer and 100 nm Al was deposited on the Teflon-AF layer. The schematic diagram of the OFETs structure is shown in Figure C. 1.

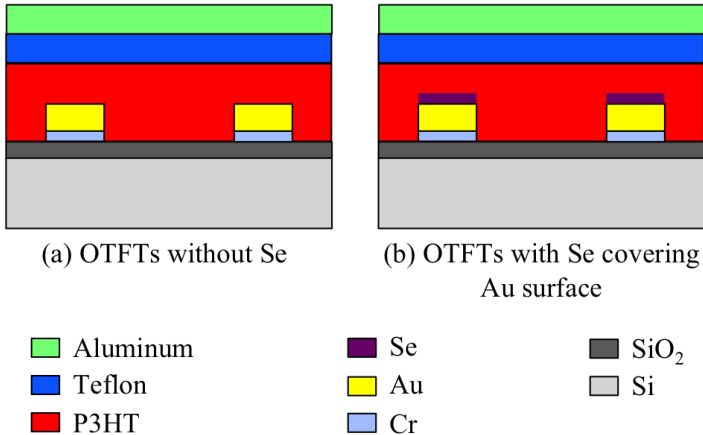


Figure C. 1. The encapsulated OFETs (a) without Se coating and (b) with Se coating on the Au electrode surface.

Each structure has 8 groups of sample. Each group contains 10 devices with the channel length ranging from 5 μm to 50 μm in 5 μm interval. The channel width is 500 μm for all the devices. Each device was taken 33 measurements at different times. These measurements were then averaged into one single resistance value.

To extract the contact resistance and the channel resistance, the total resistances (R) from the source to the drain in different gate voltages were plotted in the coordinate of the resistance (R) versus the channel length (L). The contact resistances can be obtained by extrapolating the total resistances (R) to the value where the channel length is zero[75]. On the coordinate, the slope of the total resistance (R) represents the channel resistance per unit length[76]. The derivation of the channel resistance is shown below.

$$S = \frac{R_{(n+1)} - R_{(n)}}{(n+1) - n} = \frac{[R_c + R_{ch(n+1)}] - [R_c + R_{ch(n)}]}{(n+1) - n} = R_{ch(n+1)} - R_{ch(n)} = R_{ch(1)}$$

where S is the slope of the total resistance, n is the channel length, $R_{(n)}$ is the total resistance with length of n, R_c is the contact resistance and $R_{ch(n)}$ is the channel resistance with length of n.

Since the contact resistance and the channel resistance are functions of the gate voltage, the value of them changes at different gate voltages. The measurements were conducting only in the saturation region ($V_D=30\text{ V}$) because, in these devices, the linear region near the origin has a large leakage gate current while the saturation region doesn't have the leakage current.

Due to the device defect and some data that were not able to extract contact resistances, only 6 groups of data were used for extracting the Au contact resistance. For the Au/Se contact resistance, only 1 group of data can extract the contact resistance. The

other 7 groups cannot extract the contact resistance because the total resistance (R) lines intersect before meeting zero channel length. Figure C. 2 shows an example that can extract contact resistance and Figure C. 3 shows an example that cannot extract contact resistance.

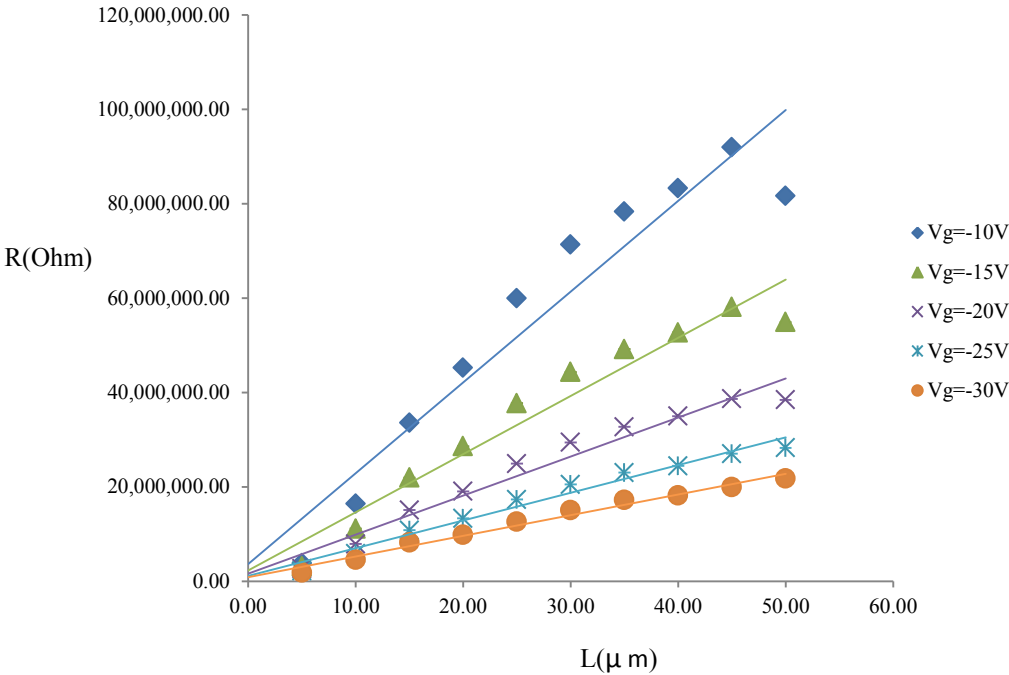


Figure C. 2. Data group that can extract the contact resistance.

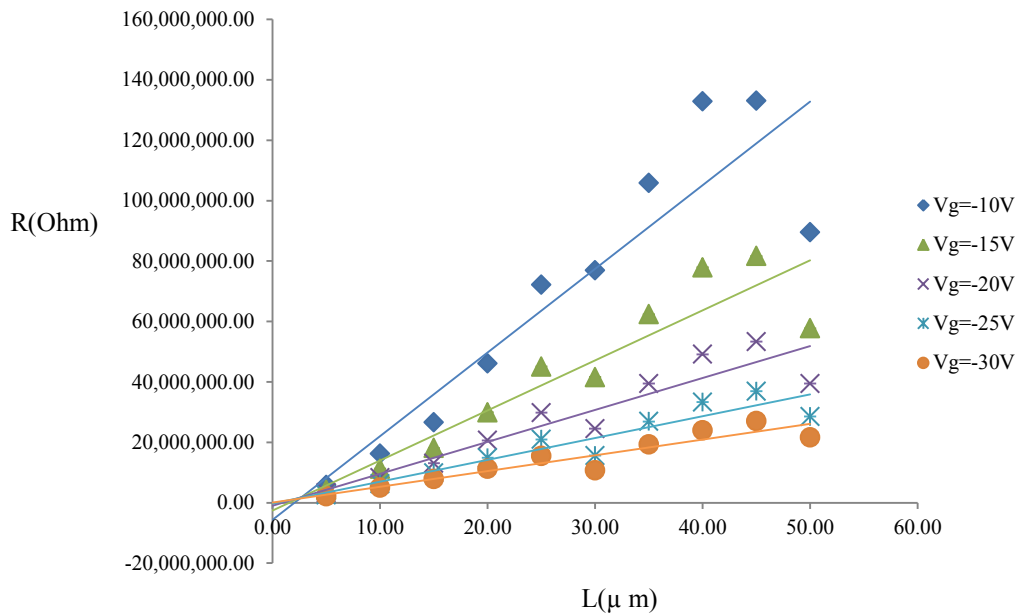


Figure C. 3. Data group that cannot extract the contact resistance.

Contact resistances in different gate voltage are shown in Figure C. 4. For the Au contact, the data was summarized from 6 data groups. For the Au/Se contact, only one group can be used so that there is no standard deviation for the Au/Se case. From this result, it is obvious that the contact resistance with additional Se deposited on the gold does not have significantly improvement and it is within the standard deviation range of that Au contact resistances. Therefore, from this data, I assume that the Au/Se contact performs like the Au contact.

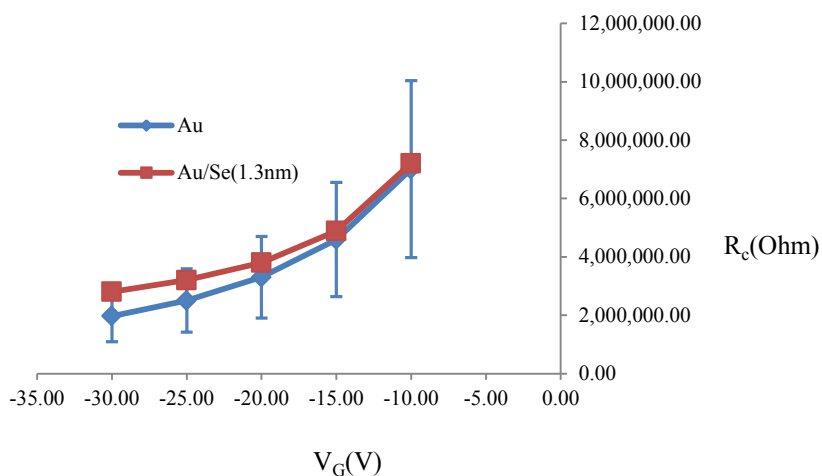


Figure C. 4. Contact resistances of both the Au contact and the Au/Se contact in different gate voltages.

Channel resistances in different gate voltage were also compared. The result is shown in Figure C. 5. This is an expected result because the channel material was P3HT for both cases so that the channel resistance should have a similar value.

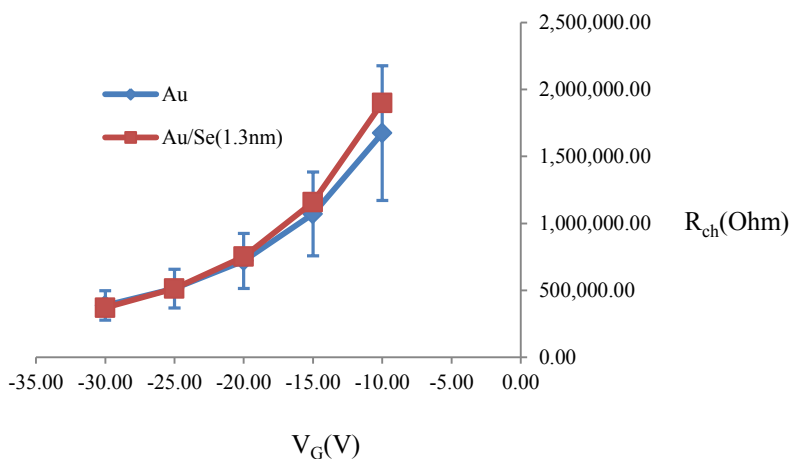


Figure C. 5. Channel resistances of both the Au case and the Au/Se case in different gate voltages.

Since the channel resistance only uses the slope of the total resistance (not like the contact resistance needs to extrapolate R to the y axis), we can easily obtain channel resistances from all the 8 groups of the Au/Se case and compare it with the channel resistance of the Au case. The result is shown in Figure C. 6. The Au/Se case shows a higher average of the channel resistance, which also indicates the steep slope of the resistance group that cannot extract the contact resistance as described in Figure C. 3. Although the resistance of Au/Se is a little higher at low gate voltage, the standard deviations of these two cases still have a large overlap. Moreover, at high voltage, they are almost identical. Therefore, the channel resistance of these two contacts should be the same.

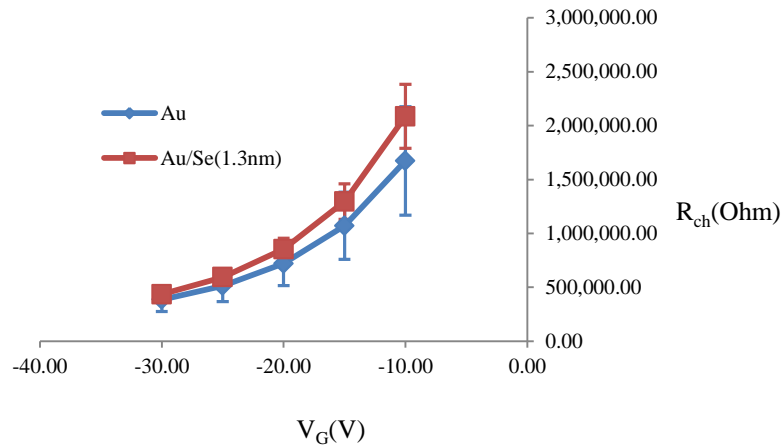


Figure C. 6. Channel resistances of both the Au case and the Au/Se case in different gate voltages. In this case, all the 8 groups of Au/Se case were used.

In summary, the result illustrated in Figure C. 4 shows that coating a thin layer of Se on the Au electrode has no significant improvement in the contact resistance. The

reason is probably that Se was only coated on the top of Au, which means the channel might not be able to contact with the Se coating because the channel is formed in between the source and the drain contacts. However, the conclusion summarized from the data that only uses one group of the Au/Se contact might not be correct, but this procedure can be used as a reference for future research. Therefore, to improve the experiment in the future, more data groups need to be included, and top source/drain contacts might be a better choice to use because it ensures that the Se coating can directly touch the channel.