MULTILEVEL CONVERTER TOPOLOGIES FOR UTILITY SCALE SOLAR PHOTOVOLTAIC POWER SYSTEMS

A Dissertation

by

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ABSTRACT

Renewable energy technologies have been growing in their installed capacity rapidly over the past few years. This growth in solar, wind and other technologies is fueled by state incentives, renewable energy mandates, increased fossil fuel prices and environmental consciousness. Utility scale systems form a substantial portion of electricity capacity addition in modern times. This sets the stage for research activity to explore new efficient, compact and alternative power electronic topologies to integrate sources like photovoltaics (PV) to the utility grid, some of which are multilevel topologies.

Multilevel topologies allow for use of lower voltage semiconductor devices than two-level converters. They also produce lower distortion output voltage waveforms. This dissertation proposes a cascaded multilevel converter with medium frequency AC link which reduces the size of DC bus capacitor and also eliminates power imbalance between the three phases. A control strategy which modulates the output voltage magnitude and phase angle of the inverter cells is proposed. This improves differential power processing amongst cells while keeping the voltage and current ratings of the devices low.

A battery energy storage system for the multilevel PV converter has also been proposed. Renewable technologies such as PV and wind suffer from varying degrees of intermittency, depending on the geographical location. With increased installation of these sources, management of intermittency is critical to the stability of the grid. The

proposed battery system is rated at 10% of the plant it is designed to support. Energy is stored and extracted by means of a bidirectional DC-DC converter connected to the PV DC bus. Different battery chemistries available for this application are also discussed.

In this dissertation, the analyses of common mode voltages and currents in various PV topologies are detailed. The grid integration of PV power employs a combination of pulse width modulation (PWM) DC-DC converters and inverters. Due to their fast switching nature a common mode voltage is generated with respect to the ground, inducing a circulating current through the ground capacitance. Common mode voltages lead to increased voltage stress, electromagnetic interference and malfunctioning of ground fault protection systems. Common mode voltages and currents present in high and low power PV systems are analyzed and mitigation strategies such as common mode filter and transformer shielding are proposed to minimize them.

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1. INTRODUCTION

1.1. Growth of Renewable Power and Photovoltaic Power Installations

The growth in demand for electricity has always been increasing but in recent years the rate of growth has slowed down. Recent figures indicate that the growth has dropped to 0.7% per year [1]. Capacity addition to the grid has kept up with the demand but the sources of generation have varied over decades. Recent capacity additions have come mainly from natural gas power stations and renewable energy sources. Fig 1.1 shows the growth in electricity generation by energy source, which gives the predictions for robust growth in renewable energy installations.

Amongst renewable energy sources, solar and wind power provide most of the growth, as can be seen from fig. 1.2. The steady and rapid growth in solar photovoltaic installation across the United States has been driven by many factors including renewable portfolio standards, decreasing costs of installations and incentives such as feed-in-tariffs or net-metering mandated by governments.

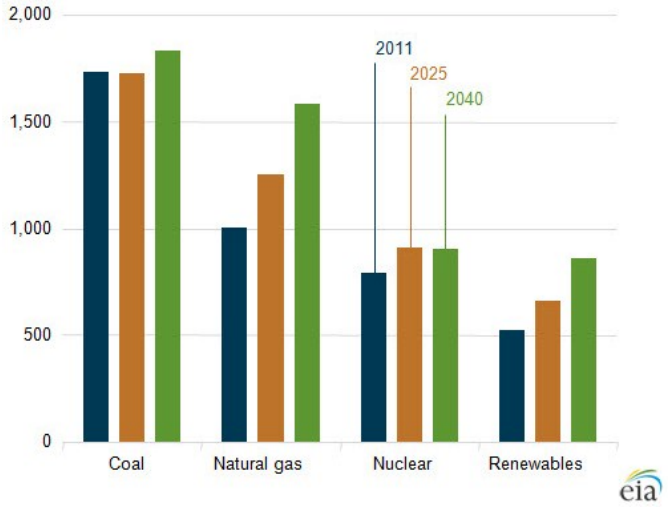

Fig. 1.1: Electricity generation by fuel, 2011, 2025 and 2040 (billion kWh) Source: EIA (May 2013) [1] *

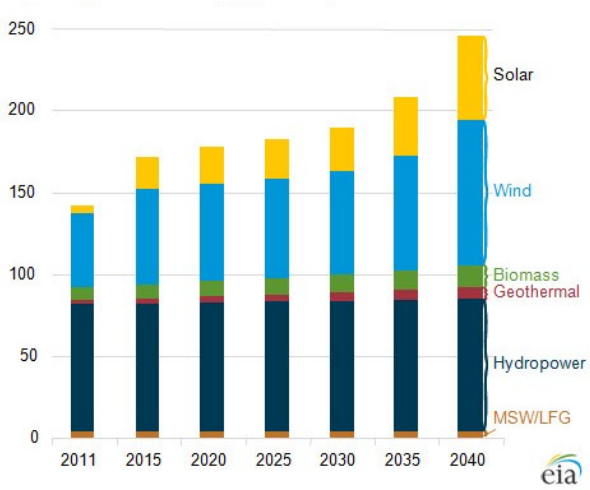

Fig. 1.2: Renewable energy sources by installed capacity, 2011-2040 (GW) Source: EIA (May 2013) [1] *

As of 2013 the total capacity of PV installations in the USA stands at 8 GW [2]. Of the 3.3 GW of capacity addition in PV in the year 2012, more than half – 1.7 GW –

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was in the utility sector [2]. With incentives and subsidies from governments and feed-in-tariffs from utilities, grid parity in solar PV sector is said to have been achieved [3]. Also, the cost of installations is projected to reduce by 35% by 2025, adjusted to inflation.

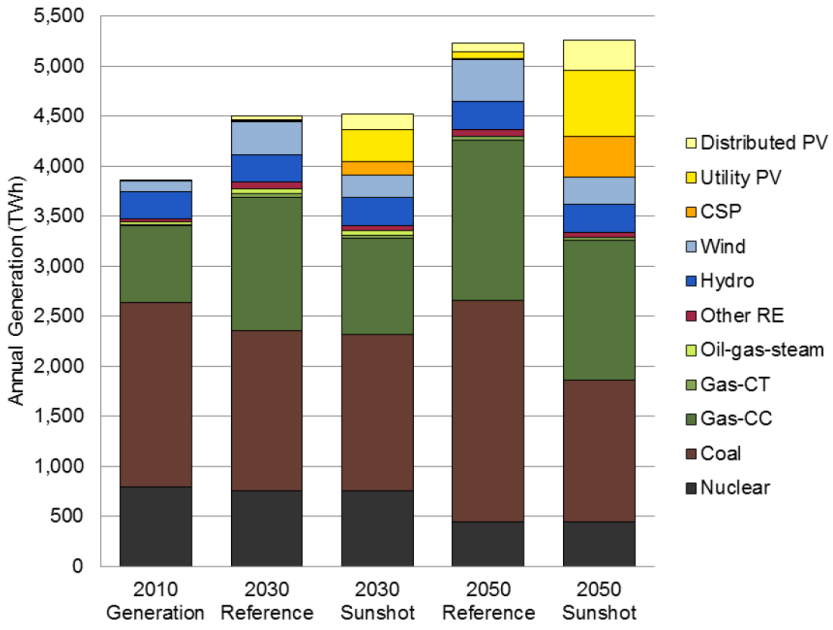

Fig. 1.3: U.S. PV installations by market segment, 2030 & 2050 forecasts. Source: NREL [4] *

All the aforementioned factors are predicted to contribute to tremendous growth in utility sector PV installations, as seen from fig. 1.3 [4]. The increasing capacity addition of solar PV and installation of larger power stations has led to research and development in high power converter topologies for PV applications, which will be further discussed later in this chapter.

* Used with permission from US National Renewable Energy Laboratory

1.2. Characteristics of Solar PV Cells and Arrays

Solar photovoltaic modules are constructed by connecting numerous PV cells in series. There are different types of cell chemistries, the most important of which are Crystalline silicon, Polycrystalline thin film (e.g.: Cadmium telluride), Mono-crystalline thin film (e.g.: Gallium arsenide). A typical commercial solar PV module is rated 250 – 300 W. When light is incident on the surface of the PV cell, some of the light energy is absorbed by the cell to produce electricity. In addition to producing a current the PV cells also generate a small electric field across them which results in output voltage which is typically 0.6 V per cell for a commercial PV module. The voltage-current characteristics of a PV cell and by extension, a PV module are given in fig. 1.4. It can be seen from the figure that PV cells may be characterized as weak current sources since they exhibit the properties of a current source under low voltage and as the voltage increases, the current collapses beyond a "knee point". Also, these properties are dependent on the temperature of the cells and incident solar radiation (insolation), or the amount of solar power incident on a unit area of the module. As the insolation decreases, the current generated by the module decreases and as the temperature increases the voltage generated decreases. These two phenomena are fairly independent.

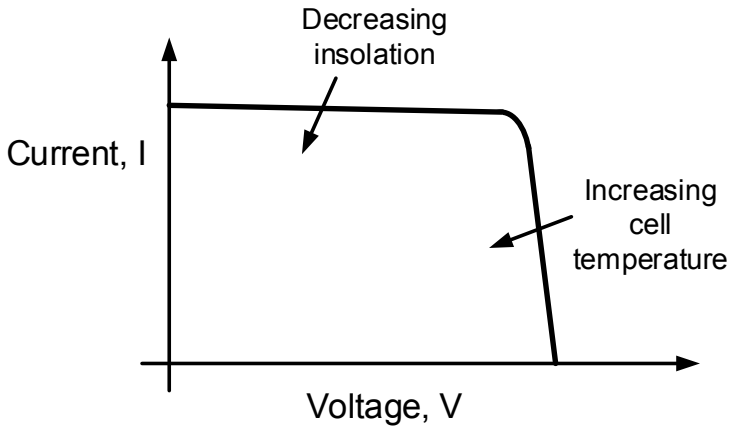

Fig. 1.4: The voltage-current characteristics of solar photovoltaic cell

In fig. 1.4 it may be seen that beyond a voltage level, the current generated by the PV cell starts to reduce. It is easy to deduce that at this point, both the voltage and the current generated by the cell are at their maximum, which means that the power generated by the cell at this point is the maximum possible for those operating conditions of insolation and temperature. Using power electronic circuits, it is possible to apply this voltage to the PV cell, ensuring that the power generated by the cell is at a maximum. This operation is called Maximum Power Point Tracking (MPPT).

PV modules can be connected in series and parallel combinations to produce desired DC voltage and current ratings. Such combinations are termed PV arrays. The PV arrays have V-I characteristics similar to the cell, appropriately scaled. PV arrays can be connected to power electronic converters so that the PV power may be processed and supplied to the load or the utility grid.

1.3. Commercial and Utility Scale Solar PV Integration

Solar PV installations vary in their installed capacity from domestic applications which are in the multi kW range and utility scale plant which are as high as hundreds of MW. This categorization is done mainly based on the size of the installation. Installations on residential rooftops which are below 10 kW are generally grouped into Residential systems. Installations on business buildings and warehouses are usually larger than 10 kW and may be up to megawatts and these installations are known as Commercial systems. Utility systems are much larger, ground-mounted systems which are often greater than 100 MW [5].

The operation of large scale plants has a significant impact on the utility grid. As the capacity of PV installations grows they constitute a growing part of the grid capacity itself. This presents unique challenges, because until few years ago almost all of the grid capacity was conventional synchronous generator based plants, powered by sources such as gas or nuclear power. Problems such as intermittency of solar power pose power electronic design challenges since the stability of the utility grid depends on the regulation of the PV plant as well. The impacts of photovoltaic installations and other distributed sources on the grid, and the design challenges and requirements are reflected upon, in documents such as IEEE 1547 Standards [6] for distributed energy resources. Some examples of the impacts which PV plants could have on the grid and design requirements to minimize the impact are given here (from IEEE 1547).

- *Impact on Utility Grid:* Power injected into the grid from the distributed resource could completely offset the local load demand of the power system, causing an

increase in bus voltage. If the distributed resource supplies (capacitive operation) or consumes (inductive operation) reactive power, the bus voltage is significantly affected in the local electric power grid. This, in addition to the previous effect, contributes to an increase in bus voltage at the local power system.

- *Power Quality – DC injection:* The distributed resource and its interconnection system shall not inject dc current greater than 0.5% of the full rated output current at the point of common coupling. Any injection of DC current could begin to saturate the cores of distribution transformers, which causes higher values of current spikes in the system.
- *Power Quality – THD:* While supplying balanced linear loads, the THD of line current supplied by the inverters should not exceed 5%. Standards such as IEEE 519 also dictate the permissible amounts of harmonic content for individual harmonic numbers.
- *Islanding Protection:* When the grid voltage collapses and results in an outage, an island of locally energized voltage buses is formed within the grid power system, leading to safety concerns. The interconnection system should detect the formation of this island and cease to energize the local power grid within two seconds.

1.4. Literature Review

The integration of photovoltaic power plants to utility grids has been a topic of research interest for many years. The commonly used topology for utility and commercial power plants is the centralized inverter topology. However, alternative

topologies to maximize power quality and energy harvest have been and continue to be proposed. Research in multilevel topologies has yielded different control strategies to maximize power harvest under partial shading conditions. Also, a lot of research literature has been published on the practical issues in PV integration such as parasitic capacitances, common mode voltages and currents. Another area of recent research interest is energy storage for utility grids, with hybrid power stations gaining attention.

1.4.1. PV Topologies: Two-level Inverter

Conventional utility scale PV plants first convert the generated DC voltage to a regulated bus using a DC-DC converter as seen in fig. 1.5, which also performs MPPT. This voltage is fed to an inverter to produce 480 V, 3-phase, V_{ac}, which is then stepped up to 13.2 kV medium voltage AC using a line frequency transformer.

This system suffers from some disadvantages such as the DC bus voltage being limited due to safety regulations (1000 V in EU and 600 V in USA). This means that the increased current causes higher losses, increased cable sizes and costs. Also, the line frequency transformer used for grid interconnect is bulky in size.

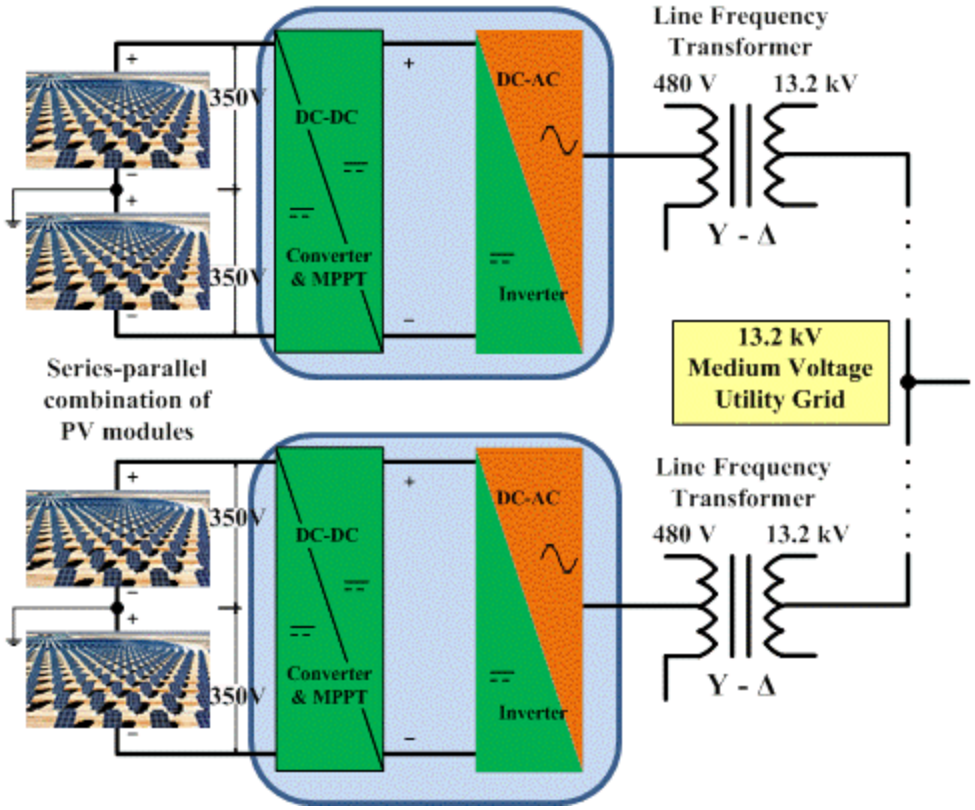

Fig. 1.5: Conventional utility scale PV plant interfaced to medium voltage electric grid

When such a PV inverter system is connected to the PV arrays, maximum power point tracking (MPPT) could be performed by the inverter or the DC-DC converter stage. Since the arrays are connected in series-parallel configuration, the currents carried by the array is limited by the modules which are least illuminated. This in turn reduces the overall power production. The effects of such shading may be mitigated by moving the MPPT DC-DC converter to the string level, as shown in fig. 1.6 or the module level so that each module can produce maximum possible power independently. This leads to an increase in overall energy yield of the PV power system [7].

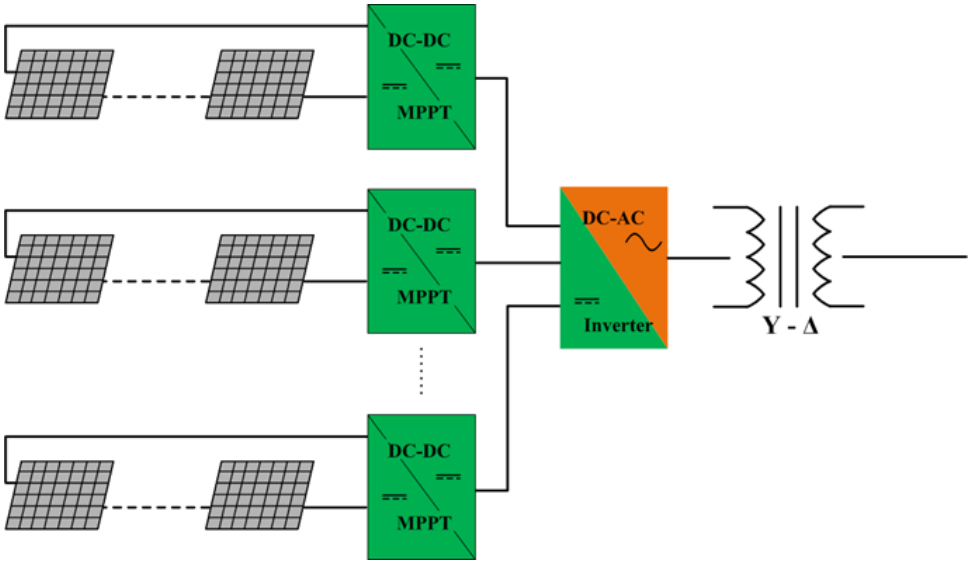

Fig. 1.6: String level MPPT converters reduce effects of partial shading and increase energy yield

The two-level inverter will need high voltage semiconductor devices for high DC bus applications. Multilevel inverters on the other hand, have better performance than the two-level topology since they produce much better output voltage waveforms and they can operate at a lower switching frequency than two-level inverters. They also can utilize low voltage semiconductor devices which are less expensive and faster in operation.

1.4.2. PV Multilevel Topologies: Diode-clamped

Many multilevel topologies have been proposed to improve operational performance and efficiency. Diode clamped topologies were proposed in [8] and [9] which enable individual array MPPT control and provide a better quality output voltage waveform than a full-bridge inverter. Multilevel NPC topologies [10-13] and cascaded

multilevel topologies [14-20] have also been proposed which process power from individual arrays rather than a large field. These topologies can also process unbalanced power amongst phases or the cascaded cells [15, 16, 18]. These proposed topologies still require line frequency transformer isolation and in the case of cascaded multilevel converters, suffer from double frequency power ripple on the DC bus capacitor.

In the diode clamped topology, as shown in fig. 1.7, PV arrays (*n-1* in number) are connected in series and the inverter is an *n*-level inverter with individual array MPPT control [8]. Since this is a multilevel inverter the output current has low distortion and the grid power factor is high. Any DC power imbalances which occur between the arrays are resolved by independent array MPPT control.

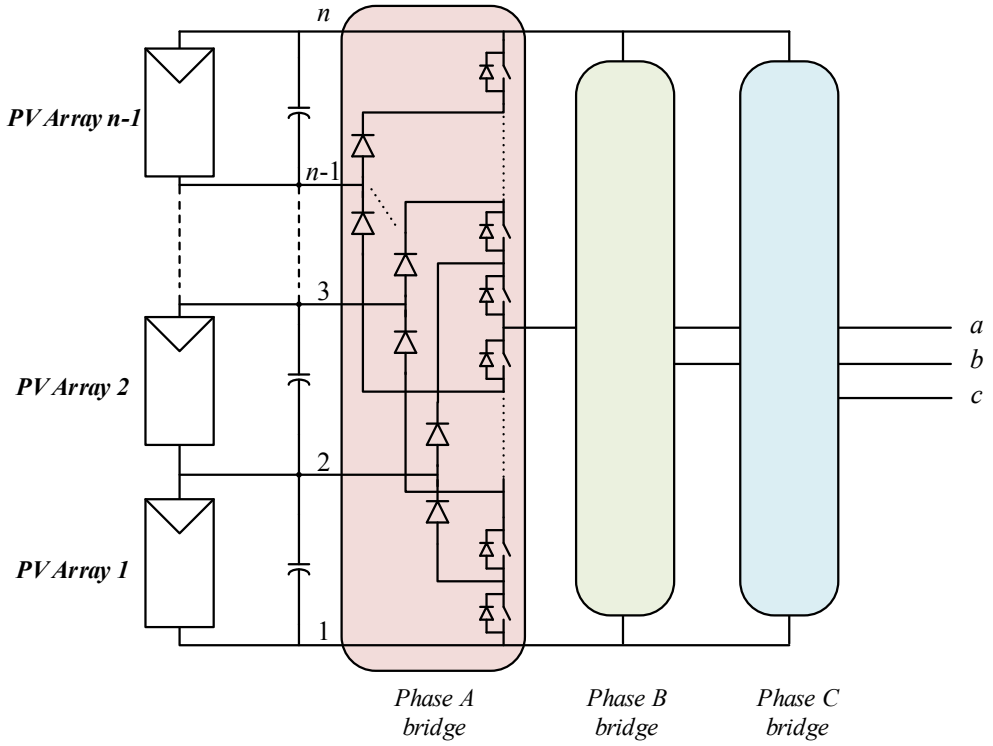

Fig. 1.7: Diode clamped *n* level inverter with individual array MPPT control

This system, despite delivering a much superior performance to that of a two-level inverter, suffers from certain deficiencies. The DC bus voltage effectively limits the number of arrays *n* that can be connected in series. Also the system is non-modular and the control is complex. The system still needs a line-frequency transformer to interface with the grid.

1.4.3. PV Multilevel Topologies: Modular Multilevel

A modular multilevel topology has cascaded H-bridges as shown in fig. 1.8 to produce a multilevel output waveform [18]. Each H-bridge is connected to a PV array or string. MPPT operation is performed by each H-bridge converter so any power

imbalance between the cells in the multilevel inverter could be resolved. These power imbalances among phases or cells require modulation compensation schemes (zero sequence injection) to produce balanced, equal line-line voltages.

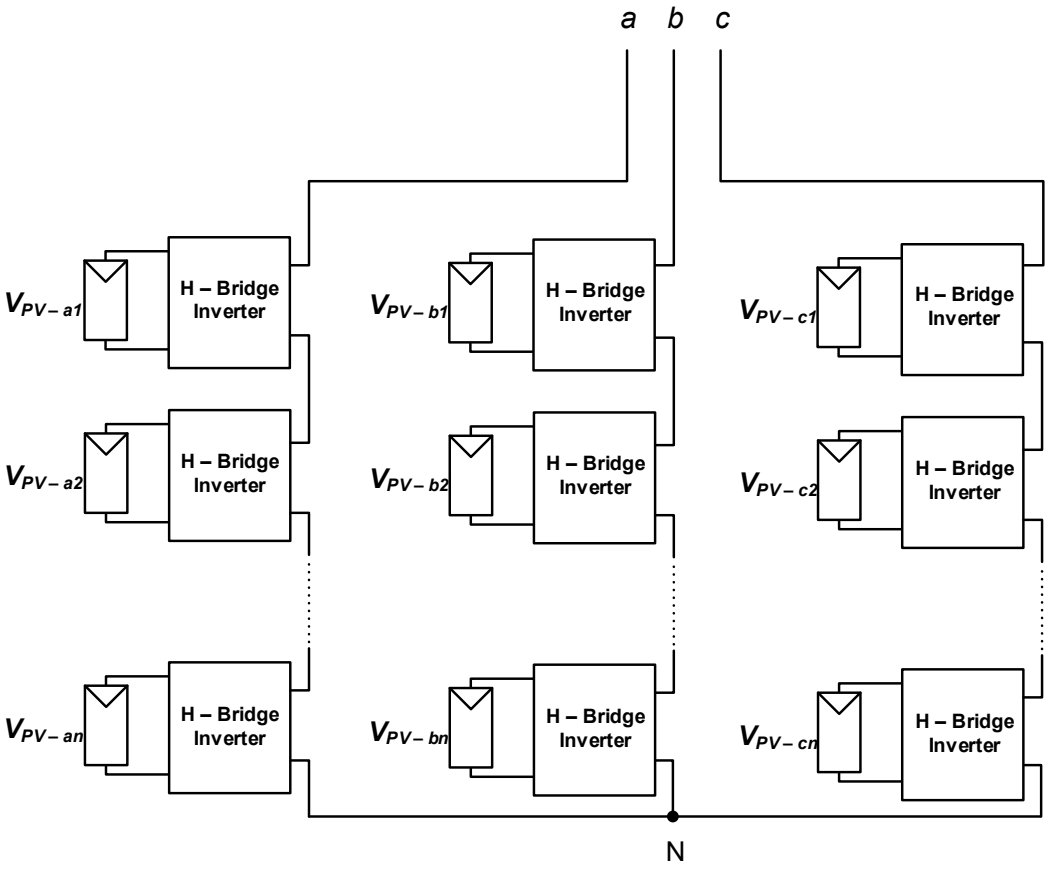

Fig. 1.8: Modular cascaded multilevel H-bridge topology for three phase grid integration

This approach too, has some disadvantages. The DC bus experiences a double frequency power ripple. Even though this is a three phase inverter, the H-bridges operate as if they were single phase, leading to the double frequency ripple. This requires large capacitors on the DC bus. Also, since there is no high frequency transformer isolation,

the maximum possible gain of the inverter is 1. Since modulation compensation schemes could further reduce the magnitude of output voltage, the DC bus voltage needs to be higher than necessary to produce the rated output voltage. Further, the PV modules in this system experience increased common mode voltage problems because of high voltage operation.

These disadvantages notwithstanding, multilevel topologies have been found to be more efficient and have a better performance than two-level inverters [21]. They offer better efficiencies since they enable high voltage operation. They have superior output distortion properties and also reduce common mode voltages and electromagnetic interference problems. Further, the individual switches may be operated at a lower switching frequency to produce a higher switching frequency voltage waveform at the output. These reasons have made high voltage operation and multilevel inverters an attractive option for PV integration. Table 1.1 shows a comparison of PV topologies, two-level and multilevel, to better illustrate the differences between these architectures. In comparing the topologies a DC bus voltage of 800 V is assumed. The inverters are rated 1 MW and the transformer turns ratio is limited to 1:6 for both the line and medium frequency devices. The IGBTs for the 2-level, NPC and diode clamped topologies are 500 A rated and the cascaded topologies have 200 A rated devices.

Table 1.1: Comparison of PV Grid Integration Topologies for 1 MW, Medium Voltage 13.2 kV Grid Integration

Topology:	**2-level**	**Neutral point clamped**	**Diode clamped *n* – level**	**Cascaded without MF transformer**	**Cascaded with MF transformer**
No. of IGBTs	12 – 18	36	$3 \cdot 2^n$	36 (3 levels)	72
Device voltage rating	1.2 kV	600 V	$\frac{1200}{n}$	1.2 kV	4.16 kV
Output quality	Poor	Good	Good, function of *n*	Good	Good
Line frequency transformer	Yes	Yes	Yes	Yes	No
Control	Simple	Moderate	Complex	Complex	Complex
Notes	High filter requirements, transformer ratio 1:6	Fault tolerance poor	Greater MPPT accuracy possible	Transformer ratio 1:6	Low current rating, reduced cost of cabling

1.4.4. PV Multilevel Control Techniques

Control techniques for multilevel inverter topologies have been studied extensively. Some of the techniques studied for multilevel control are [22]

a. Voltage oriented control

b. Voltage – direct power control

c. Virtual flux based control

d. Virtual flux direct power control

These techniques have also been used and adapted for multilevel inverter based PV systems. Many publications deal with control of PV multilevel for power imbalance amongst the cascaded multilevel cells and amongst the three phases. They consider a single phase inverter cell to be connected exclusively to a PV array. Control techniques proposed often involve a centralized controller which corrects for the phase and cell power imbalance. The output voltages of the individual inverters are controlled by modulation angle correction, thereby introducing a neutral point shift [23]. Feedforward techniques have been proposed to take into account the drift in DC bus voltage while calculating the modulation index [16]. More advanced techniques such as model predictive control have been proposed to predict the switching states as cost functions to control the DC bus voltages [24].

1.4.5. PV Battery Energy Storage

Battery energy storage devices are becoming more prevalent and they provide advantages such as mitigating intermittency effects of renewable energy sources. PV battery systems have been proposed for grid frequency and voltage support using real and reactive power support [25]. Bidirectional isolated DC-DC converters have been proposed for generalized battery energy storage systems using lithium ion batteries [26] and bidirectional DC-DC converters for exclusively DC distribution grids have also been studied [27]. Cascaded multilevel converters for battery charging have also been proposed [28] with battery state-of-charge estimation techniques. However, this

topology is transformerless, which means that some of the batteries operate at an elevated potential on both their terminals.

1.5. Research Objective

The objective of this dissertation is to analyze, propose, and design multilevel inverter topologies for utility scale solar photovoltaic applications. Multilevel topologies have been found to be more efficient than two level inverters and provide improved power quality. The proposed multilevel topology will interface MW scale utility photovoltaic power stations with a medium voltage utility grid. The problems discussed in the previous section associated with multilevel topologies such as double frequency power, requirement of line frequency isolation transformer will be addressed. The proposed topology will utilize a medium frequency isolation transformer which increases power density and provides galvanic isolation to the PV modules. The multi output transformer design will eliminate double frequency pulsations on the DC bus capacitor, leading to a reduction of its size. The design and rating analysis of the medium frequency transformer will be done. The multilevel inverter will use a cycloconverter to produce the desired AC output voltage which provides bidirectional capability.

Multilevel inverters employed in photovoltaic power processing face an important issue, viz partial shading or unbalanced insolation amongst the cascaded inverter cells. A control methodology is to be developed which enables different cells of the multilevel inverter to process varying powers. In developing the control method, the well-known and established concepts of real and reactive power flows will be used. The individual cell output voltages magnitude and phase angle will be calculated such that

the powers processed by an individual cell corresponds to the available power from the respective PV array. The analysis behind the control method will be first derived assuming that there is a centralized controller which performs the necessary calculations and generates the modulation indices for the inverter. A design example of a 10 MW PV system interfacing to a medium voltage grid and simulations results will be discussed. A laboratory scaled down prototype inverter will be developed.

The control methodology once derived, will form the basis of developing an independent controller for an individual cell in a multilevel inverter. The control technique will be inspired by droop control techniques employed in the operation of parallel inverters connected to a common voltage bus. Similar to the droop control technique, each inverter will be individually programmed and equipped to control power flow, independent of feedback from other inverters in the system. However, grid voltage zero crossing data will be made available to the individual inverters. The closed loop controller will control modulation index for an inverter cell such that any amount of real power can be processed from the PV arrays, provided the grid voltage has not collapsed.

Photovoltaics and other renewable energy sources are often associated with intermittency, which affects the utility grid in ways that could destabilize it. This issue is resolved by a combination of accurate forecasting of renewable availability and reactive power support from inverters using power electronics. However, energy storage systems are becoming more popular in providing support to the grid during intermittency. A battery energy storage system for utility scale PV will be developed in this work. The battery system will be designed to support up to 10% reduction of the PV system. The

design and operation of the bidirectional converter which charges and discharges the battery will be discussed. A study of the design of the battery system and various battery chemistry choices available will also be performed. A design example for the battery energy storage device and simulation results will also be discussed.

Common mode (CM) voltages and currents are an important issue faced by power electronics and electric machine designers. These phenomena lead to problems such as nuisance tripping, deterioration of components and electromagnetic interference (EMI). This work will perform an analysis of PV modules with respect to parasitic capacitances, which influence CM currents in PV modules. CM voltages in various PV inverter topologies including the proposed topology will be characterized and analyzed, along with simulation and experimental results. Techniques to mitigate CM voltages and currents will also be discussed.

1.6. Outline of Dissertation

This dissertation is organized into six chapters. Chapter 1 introduces photovoltaic technology and their growth into an important player in the modern utility grid. The operational characteristics of PV power plants and their impact on the grid are discussed. A literature review of state-of-the-art and research publications on new topologies is done and the research objective is described.

Chapter 2 provides the description of the proposed medium frequency AC link inverter and explains its operation. The design of the inverter and the medium frequency transformer are discussed. The operation of the inverter along with simulation results and prototype experimental results are provided. Chapter 3 develops a control technique

to independently control individual cascaded inverter cells. The chapter first describes the operation of droop control and describes the derivation of cascaded inverter control. Simulation and experimental prototype results are also provided.

Chapter 4 discussed common mode voltages and currents in various PV inverter topologies. Analysis and measurement of parasitic capacitances in a commercial PV system are described. The development of CM voltage and currents and techniques to mitigate them are explained with simulation results.

Chapter 5 is concerned with the development of a battery energy storage system for multilevel PV inverters. Various battery technologies available for this application are discussed. The DC-DC converter used to interface the battery with the grid is explained and analyzed. Simulation results for a 0.1 p.u. battery system are provided for a 5 MW rated PV multilevel system.

Chapter 6 provides a summary of the research work and concludes with recommendations for future research topics.

2. MEDIUM FREQUENCY AC LINK CASCADED MULTILEVEL INVERTER AND ZONAL POWER BALANCER*

2.1. Introduction

A commercial large utility solar photovoltaic power station consists of a number of PV arrays, which are large number of PV modules connected in series-parallel configuration. PV modules are connected in series to form a string, specified by the desired PV voltage and a number of strings are connected in parallel, determined by the PV current rating. Each of the PV arrays in the power station is interfaced to a central three phase inverter. As discussed in the previous chapter, multilevel inverter topologies have several advantages such as better power quality, utilization of lower voltage rating devices, etc. The proposed topology is a multi-level DC-AC converter for MW scale applications which has the aforementioned advantages and also improves partial shading operation [29]. The plant is divided into a number of zones as shown in fig. 2.1; the DC voltage from each zone is converted to medium frequency (MF) AC using an IGBT-based full bridge inverter. It is then fed to an MF transformer with 3 secondary windings (one for each phase), stepped-up and then fed to a full bridge AC-AC converter to generate 3-phase AC. The proposed system has the following advantages:

- PV field is configured as a center-point grounded system to realize higher voltage DC while preserving the insulation level of individual panels. High DC

* This chapter is adapted from [29] H. S. Krishnamoorthy, S. Essakiappan, P. N. Enjeti, R. S. Balog, and S. Ahmed, "A new multilevel converter for megawatt scale solar photovoltaic utility integration," in *Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 1431-1438. Digital Object Identifier: 10.1109/APEC.2012.6166008

voltage operation reduces the current rating requirement of cables and also improves efficiency.

- A unique current sharing scheme is introduced such that zonal MPPT is achieved.
- Use of medium frequency transformer isolation reduces the size and cost and at the same time, provides galvanic isolation between PV modules of different zones of the plant.
- Multilevel operation allows use of SiC MOSFET devices in the AC-AC converter leading to higher efficiency. Further, the semiconductor devices are utilized more effectively. The reduction in current decreases the cable size and cost [30].
- Due to the modular nature of the approach, it is possible to bypass one zone at a time for maintenance without disconnecting the entire system.
- Harmonic current is reduced on the DC link, which allows the usage of thin film capacitors with smaller sizes and longer life-times. Switching frequency harmonics are also reduced by phase shifted carrier pulse width modulation (PSC-PWM).
- A new control method is proposed for the series connected inverter modules under partial shading. The approach controls each inverter voltage/phase-angle to continuously adjust the power delivered.

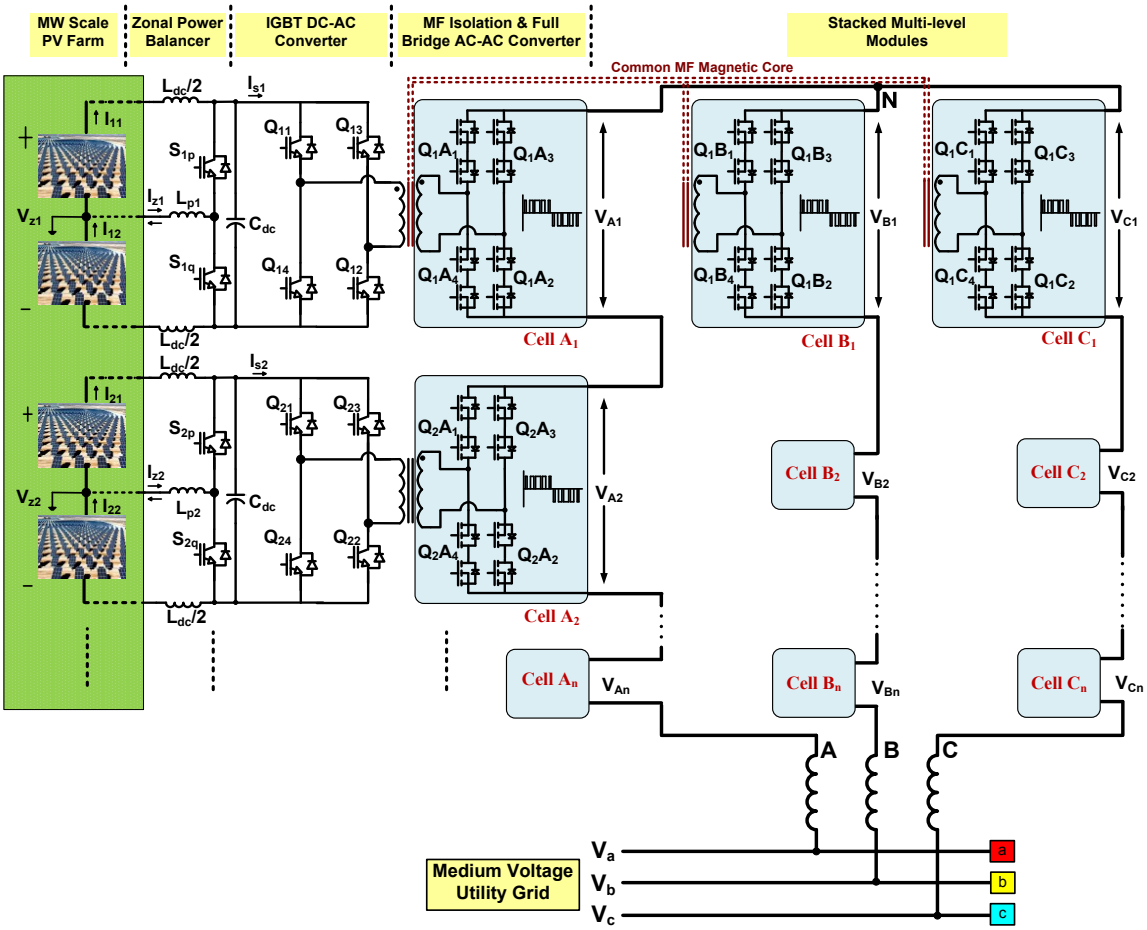

Fig. 2.1: Proposed Multi-level DC-AC-AC Converter with MF isolation and Zonal MPPT

2.2. Description and Working of Proposed Multilevel Converter

Fig. 2.1 shows the proposed multilevel converter. Inductors- L_{p1}, L_{p2} ... L_{pn}, along with the switches S_{1p}, S_{1q}, S_{2p}, ... S_{nq} are controlled to function as current choppers which regulate the currents (I_{11}, I_{12} …, I_{n2}) in order that the current through the PV arrays can be different/adjusted to achieve MPPT. The full bridge inverter with switches- Q_{11}, Q_{12}, Q_{13}, Q_{14}, Q_{21}, … Q_{n4} are switched at MF and this voltage is applied to the primary of the

MF transformer. The SiC MOSFET based AC-AC converter with bidirectional switches- Q_1A_1, Q_1A_2, Q_1A_3, Q_1A_4, Q_1B_1 … Q_nC_4 convert the MF AC to get line frequency AC. The line inductors can induce circulating currents in the transformer secondary at large loads, which can be used to attain ZVS on switches on primary side [31]. When the number of levels is large, the grid-side L-C filters which have to be used in conventional topologies can be eliminated due to the PSC-PWM on AC-AC side [32-35]. Alternatively, the same functionality may be achieved by constructing the AC-AC converter as an indirect matrix converter, which would consist of a controlled rectifier followed immediately by a full bridge inverter without a DC bus capacitor. Another alternative topology would be to use a triple active bridge on the PV side to produce three square wave voltages, which would be applied to three medium frequency single phase transformers. This approach would reduce the device current ratings but increase the number of devices used on the transformer primary side.

Considering a 10 MW solar PV plant divided into n zones of 1 per unit (p.u) power, each generating a maximum V_{dc} = 1 p.u voltage (around 0.5 p.u/array). Assuming that the secondary side SiC MOSFETs are rated for 3.3 kV, the peak voltage that each MOSFET can block after a derating of 50%, is around 1.7 kV. So, the maximum peak-to-peak secondary voltage of transformer can be V_{sec} = 1.7∗2 = 3.4 kV, which can be used to generate a maximum sinusoidal output voltage of 1.2 kV rms. In order to interface with a 13.2 kV rms medium voltage utility grid and to allow flexibility in the modulation index (m_a) to 0.8, number of zones can be calculated as:

$$n = \frac{(13200/\sqrt{3})}{(m_a * 1200)} \cong 8 \tag{1}$$

So, the base power (1 p.u) is taken as 1.25 MW (10 MW/8) and base voltage (1 p.u) is taken as 1.0 kV. This makes base current as 1250 A and base impedance as 0.8 Ω.

2.2.1. Zonal Power Balancer under Partial Shading

At times of unequal shading within a zone, the current in series connected arrays is limited to that of the least illuminated array. The zonal power balancer eliminates this problem. The currents in the power balancing inductors (L_{p1}, L_{p2}, etc.) are controlled to be equal to the difference in array currents in a zone.

For the design of the power balancer, steady state duty cycle for switching of the IGBT S_{np} can be written as $D = V_2/(V_1 + V_2)$ and that for S_{nq} as, $D' = 1 - D$. With this, the inductor value can be calculated as:

$$L_p = \frac{D \cdot V_1}{f_{sw} \cdot \Delta I_L} \tag{2}$$

where V_1 and V_2 are the voltages of the two stacks in zone-1 ($V_1 + V_2 = V_{z1}$). f_{sw} is the MPPT switching frequency and ΔI_L is the maximum allowable ripple current in the inductor.

Same equations apply for other zones as well. In the present context, it is assumed that the voltages V_1 and V_2 can vary from 0.5 p.u to 0.4 p.u each, at the worst condition and the power delivered by each array may vary independently from 0% to 100% capacity during the day. For a switching frequency of 20 kHz and ΔI_L of 50 A, L

can be calculated as 240 μH. Fig. 2.2 shows the simulated waveforms of current through power balancing inductor (L_{p1}) and voltage across the inductor in zone-1 under the condition that the array with voltage V_2 = 500 V delivers 100% power, while the array with voltage V_1 = 450 V delivers only 50% power due to partial shading. It can be seen that the average current through the inductor is -560A, which enables power balancing between the arrays.

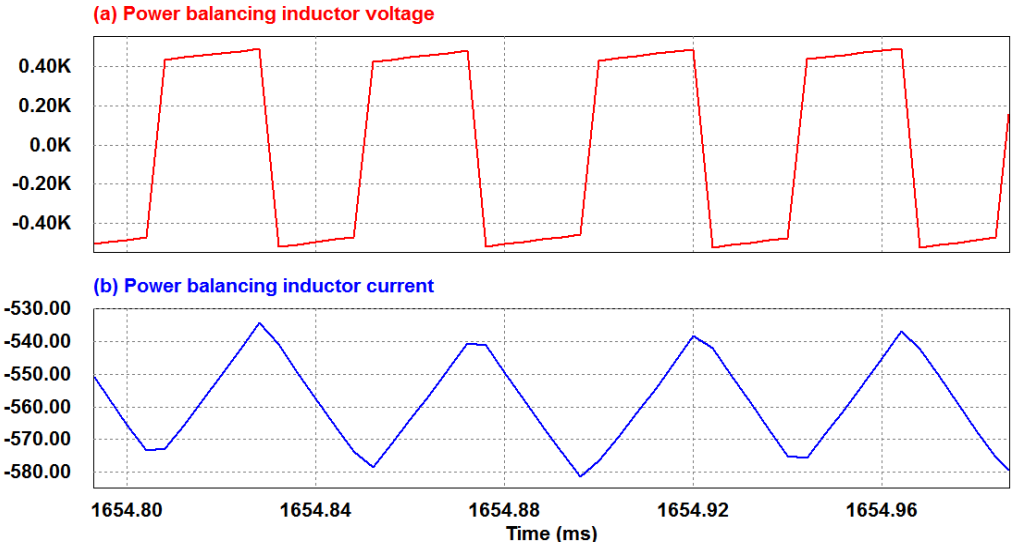

Fig. 2.2: (a) Voltage and (b) Current of power balancing inductor

2.2.2. DC-AC-AC Converter

The inversion of PV side DC voltage to line frequency AC is accomplished by the DC-AC-AC medium frequency AC link converter. The primary side voltage is generated by the full bridge inverter and the square wave voltage produced is applied to the AC-AC converter, which produces a sinusoidal PWM voltage on the output side.

The Fourier series expansion of voltage at transformer primary, V_{pri} can be written as:

$$V_{pri}(t)=\frac{4V_{dc}}{\pi}\cdot\left[\frac{\sin 1\omega_1 t}{1}+\frac{\sin 3\omega_1 t}{3}+\frac{\sin 5\omega_1 t}{5}+\frac{\sin 7\omega_1 t}{7}+\ldots\right] \tag{3}$$

With PSC-PWM at the secondary side AC-AC converter, switching function can be split into two components (one with a rectifier switch function and another with a sine PWM inverter switch function) and can be written as:

$$S_{acac}(t)=S_{rect}(t)\cdot S_{inv}(t) \tag{4}$$

where

$$S_{rect}(t)=\frac{4}{\pi}\left[\frac{\sin 1\omega_1 t}{1}+\frac{\sin 3\omega_1 t}{3}+\frac{\sin 5\omega_1 t}{5}+\frac{\sin 7\omega_1 t}{7}+\ldots\right] \tag{5}$$

$$S_{inv}(t)=m_a\left(\sin(2\pi\cdot 60\cdot t)+\sin(\omega_2 t)+\ldots\right) \tag{6}$$

m_a is the voltage modulation index, ω_1 is the IGBT bridge square wave switching frequency and ω_2 is the AC-AC converter carrier frequency. The carrier frequency can be chosen as $\omega_2 \approx 4*\omega_1$ to reduce the size of input as well as AC side filters (ω_1 may be chosen as $2\pi*1.44$ k rad/s as per MF transformer design). After evaluating the switching functions, the effective output phase voltage can be calculated as:

$$V_{out}(t)=V_{pri}(t)\cdot S_{acac}(t)=\frac{n_2}{n_1}\cdot V_{dc}\cdot S_{inv}(t) \tag{7}$$

While the MPPT and zonal power balancer take care of shadowing effects between the two arrays in a single zone, power variation between the zones are taken care by regulating the zone output voltages depending on their power transfer

capabilities, so that output current of all zones is the same. AC output voltages of the 'n' zones are subject to the condition:

$$\sum_{k=1}^{n} V_k = V_{grid} \tag{8}$$

where V_{grid} is the phase to neutral grid voltage and V_1, V_2… V_n are the AC-AC converter output voltage vectors of 'n' zones. Here, $V_{grid} = 13200/\sqrt{3} = 7{,}621$V rms. If it is assumed that the phase angle of all zonal voltage vectors are equal under all conditions, the voltage magnitudes have to be varied in order to achieve the current same. But under shading conditions, the voltages will have to vary by large values to compensate for the power from PV arrays. This may lead to overrating of devices, reducing the device utilization. In order to facilitate better device utilization, the phase angles of the voltage vectors also need to be varied along with magnitude.

2.2.3. Switching Function Generation in Medium Frequency AC Link Converter

The medium frequency AC link converter may also be called a 1ϕ - 1ϕ matrix converter or a cycloconverter, since the high frequency voltage of the transformer secondary is converted into line frequency voltage. The switching function of the AC-AC converter is generated similar to a regular single phase inverter but a square wave forms the input to the converter, instead of a constant DC voltage as in the case of an inverter. Hence the switching function includes a rectifying component and a sinusoidal modulation component. The PWM gating signals generated may be through bipolar or unipolar modulation techniques. The carrier waveforms used are triangular since the

symmetrical nature of the pulses generated produces switching frequency harmonics at higher frequencies than sawtooth carriers. The carrier signals used in each of the cascaded cells in a multilevel inverter are phase shifted with respect to a reference cell, known as phase shifted carrier based PWM (PSC-PWM). The amount of phase shift applied to each carrier is dependent on the index of the inverter cell and the total number of cascaded cells. If N inverter cells are cascaded, the phase shift of the i^{th} cell with respect to the reference cell is $\frac{2\pi}{N}(i-1)$ if N is odd (symmetrical PWM) and $\frac{\pi}{N}(i-1)$ if N is even (asymmetrical PWM) [36].

PWM Bipolar Modulation

The PWM bipolar modulation technique produces output voltage which has two possible states: positive output voltage and negative output voltage, i.e. $+V_{dc}$ and $-V_{dc}$. This technique is simple but the output voltage waveform contains harmonics around m_f, where $m_f = \frac{f_{sw}}{f_{line}}$ (f_{sw} is the carrier frequency). The generation of switching functions for devices in the transformer primary side inverter and the cycloconverter, discussed in the previous section, is discussed below.

Devices Q_1A_1 through Q_1A_4 can be imagined to be the four switches of a single phase inverter. To generate a bipolar output voltage, the modulating signal is compared with the triangular carrier and when the modulating signal is greater, Q_1A_1 and Q_1A_2 are switched on. This is shown in fig. 2.3 and the operation when the modulating signal is less than the carrier can be illustrated similarly. Since the input to the cycloconverter is a square wave and not a constant DC, the sine PWM operation is reversed when the input

voltage is negative. This is pictorially illustrated in fig. 2.4 and the switching functions of all the devices are listed in table 2.1. It is seen that there are four possible switching states for the inverter-cycloconverter combination.

If N inverter cells are cascaded, the output voltage of the cascaded multilevel inverter has switching frequency harmonics around $f_{sw} \cdot N$.

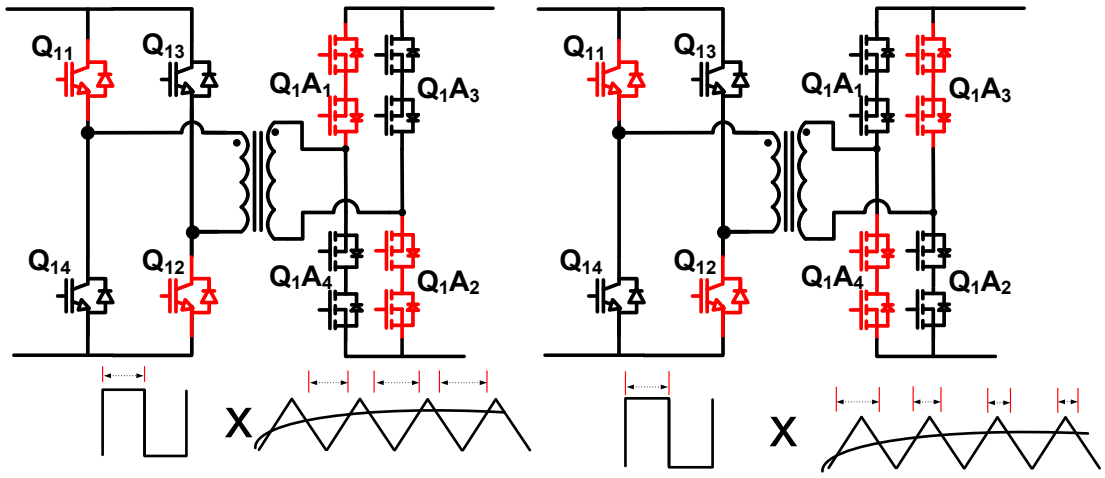

Fig. 2.3: PWM switching function generation using bipolar PWM technique for positive square wave voltage

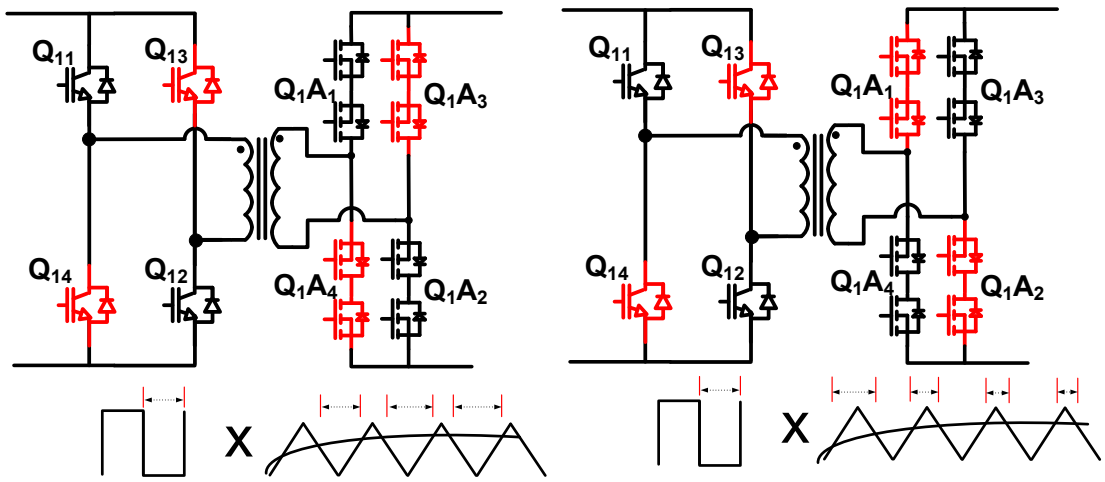

Fig. 2.4: PWM switching function generation using bipolar PWM technique for negative square wave voltage

Table 2.1: Switching Functions for Devices in Primary Side Inverter and Cycloconverter for Bipolar Modulation

Transformer Voltage	**Primary-side Inverter**		**Cycloconverter**			
	Q_{11}, Q_{12}	Q_{13}, Q_{14}	Q_1A_1	Q_1A_2	Q_1A_3	Q_1A_4
			$V_{mod} > V_{tri}$			
Positive	1	0	1	1	0	0
Negative	0	1	0	0	1	1
			$V_{mod} < V_{tri}$			
Positive	1	0	0	0	1	1
Negative	0	1	1	1	0	0

PWM Unipolar Modulation

The output voltage of a PWM inverter which uses unipolar modulation has three states: $+V_{dc}$, 0 and $-V_{dc}$. The modulating signals of the two bridges in a single phase inverter are phase shifted by 180° and the switching function for each bridge is independently generated. The switching frequency harmonics of a unipolar modulated inverter are present around $2m_f$, where $m_f = \frac{f_{sw}}{f_{line}}$. If N inverter cells are cascaded in the multilevel inverter, the output voltage contains switching frequency harmonics around $f_{sw} \cdot 2N$. The generation of switching functions is illustrated in fig. 2.5 and fig. 2.6. To generate a unipolar PWM for the cycloconverter, devices Q_1A_1 and Q_1A_3 are imagined to be part of one half-bridge; similar assignment is made to Q_1A_2 and Q_1A_4. The modulating sinusoidal waveform for the second half bridge is 180° phase shifted from that of the first half bridge. All possible switching states in the primary side inverter and cycloconverter are given in table 2.2. There are eight switching states possible for the inverter-cycloconverter combination.

During the switching operation of the cycloconverter, it is possible that voltage spikes may be introduced, since more than one transition are involved in moving from one switching state to another and the current through the leakage inductance of the transformer is interrupted. To prevent this, an appropriate commutation scheme such as the one discussed in [37] may be used.

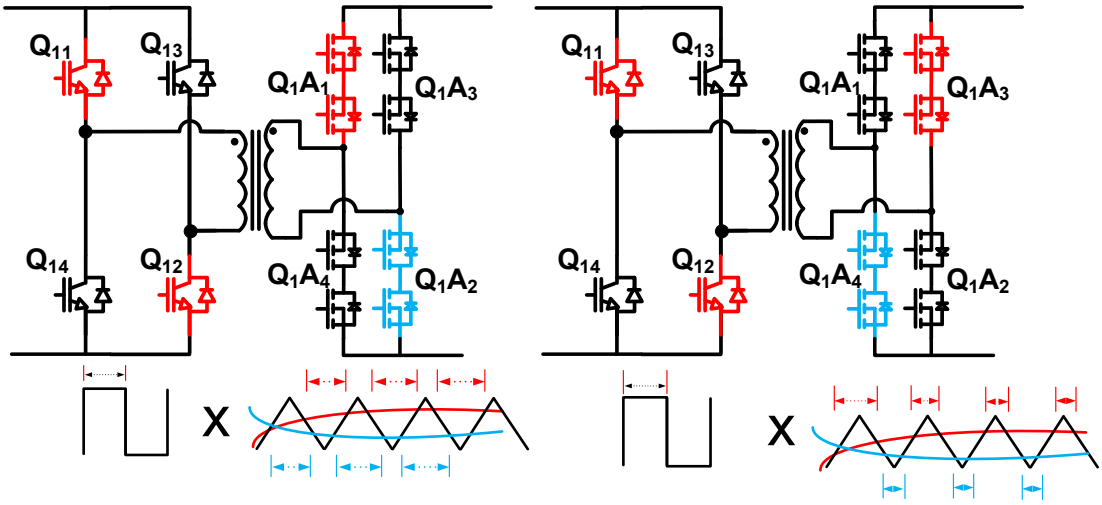

Fig. 2.5: PWM switching function generation using unipolar PWM technique for positive square wave voltage

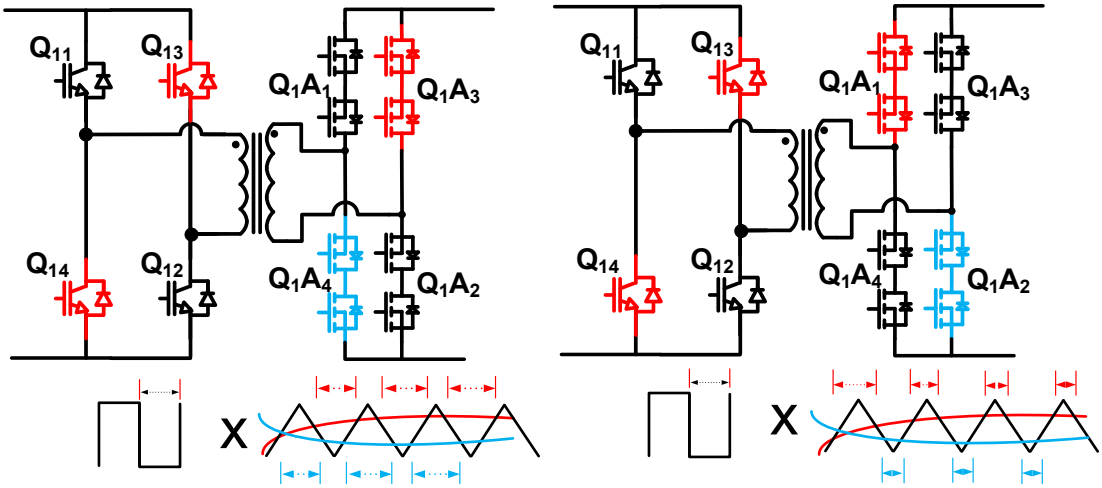

Fig. 2.6: PWM switching function generation using unipolar PWM technique for negative square wave voltage

Table 2.2: Switching Functions for Devices in Primary Side Inverter and Cycloconverter for Unipolar Modulation

Transformer Voltage	**Primary-side Inverter**		**Cycloconverter**			
	Q_{11}, Q_{12}	Q_{13}, Q_{14}	Q_1A_1	Q_1A_3	Q_1A_4	Q_1A_2
			$V_{mod1} > V_{tri}$		$V_{mod2} > V_{tri}$	
Positive	1	0	1	0	1	0
Negative	0	1	0	1	0	1
			$V_{mod1} < V_{tri}$		$V_{mod2} > V_{tri}$	
Positive	1	0	0	1	1	0
Negative	0	1	1	0	0	1
			$V_{mod1} > V_{tri}$		$V_{mod2} < V_{tri}$	
Positive	1	0	1	0	0	1
Negative	0	1	0	1	1	0
			$V_{mod1} < V_{tri}$		$V_{mod2} < V_{tri}$	
Positive	1	0	0	1	0	1
Negative	0	1	1	0	1	0

2.2.4. Transformer Design

As discussed in the previous section, the medium frequency transformer is constructed with four windings on a common core, with three of them forming the secondary outputs. Each of the three secondary windings in the transformers carry the $\omega_l \pm 2\pi*120$ rad/s current components due to single-phase operation; whereas the primary windings mainly contain ω_l frequency components; they do not have the $\omega_l \pm 2\pi*120$ rad/s harmonic current components. These components get cancelled magnetically due to the flux interaction in the 3-phase transformer under balanced load conditions. Fig. 2.7 and 2.8 show the waveforms and FFT, respectively, of zone-1 transformer primary current, transformer phase-A secondary current and 3-phase load currents. It can be seen that the $\omega_l \pm 2\pi*120$ rad/s harmonics are cancelled in the transformer primary. This results in having only PWM carrier frequency and higher order harmonics (of the AC-AC converter) at the DC bus apart from the DC component. Thus, the input LC filter can be small.

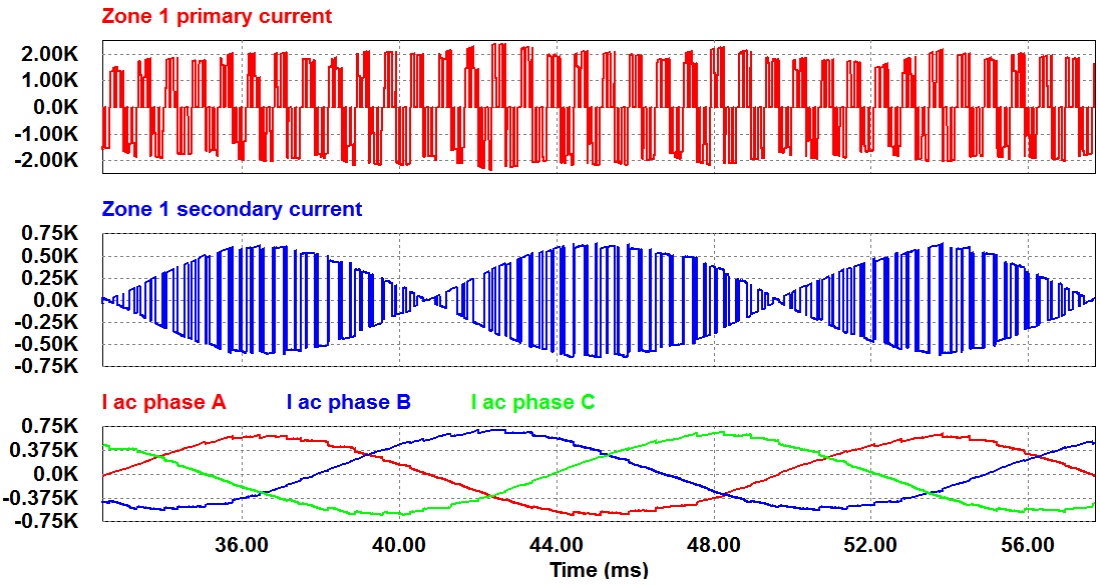

Fig. 2.7: Zone 1 transformer primary current, phase-A secondary current and balanced 3-phase load current – waveforms

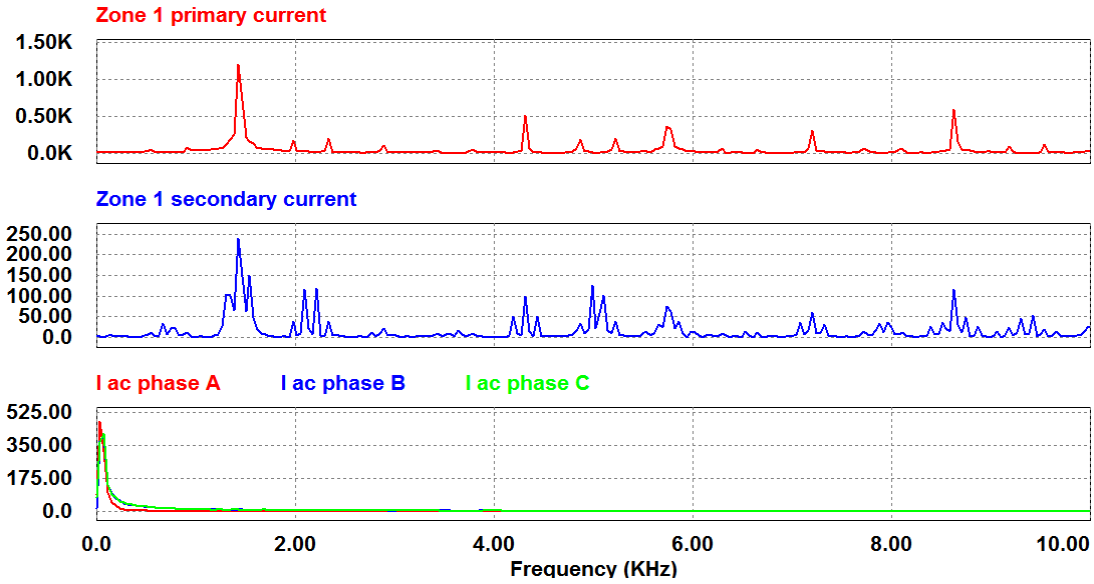

Fig. 2.8: Zone 1 transformer primary current, phase-A secondary current and balanced 3-phase load current - frequency spectrum

The transformer in every zone has to be designed with a turns-ratio considering the worst case voltage and current conditions. Recalling the design problem statement, the DC bus voltage may vary between 1.0 p.u and 0.8 p.u. The transformer secondary voltages have to be such that the rated AC voltage is produced for a modulation index of 0.8. This is done to accommodate power balancing among the zones under partial shading conditions. The control strategy is discussed in section-III. In order to produce rated voltages under different combinations of DC bus voltages and zonal power, the transformer turns-ratio can be calculated as:

$$\frac{n_2}{n_1} = \frac{\left(13200/\sqrt{3}\right) * \sqrt{2}}{n * m_a * V_{dc}} \cong 1.7 \tag{9}$$

The primary winding of the transformers has to be rated at 1.0 p.u voltage and the secondary windings have to be rated at $(n_2/n_1)*1.0$ p.u voltage. To calculate the current ratings, the per-phase secondary winding rms current is the same as output current. Assuming pure sinusoidal load current,

$$I_{sec(rms)} = \frac{Zone\,Power * \sqrt{2}}{3 * V_{\sec(rms)}} = \frac{\sqrt{2} \cdot n_1}{3 \cdot n_2}\, p.u \tag{10}$$

The transformer primary current on the other hand, does not contain the $\omega_1 \pm 2\pi*120$ rad/s and some higher order harmonics and subsequently have lesser proportion of rms current. After the ω_2 component, the next most significant harmonic contents that the current will be having are around $\omega_1+\omega_2$ rad/s. The rms current at the transformer

primary can now be approximated as $I_{pri(rms)} \cong 1.2 p.u$ [38]. The overall transformer rating can be expressed as:

$$VA_{tfrmr} = \frac{V_{pri} * I_{pri} + 3 * V_{sec} * I_{sec}}{2} \cong 1.31\, p.u \tag{11}$$

2.2.5. Input Filter Design

As discussed earlier, the operation of the four winding transformer ensures that there is no 120 Hz component in the input DC bus current, which allows the DC input filter to be small. Current components at $\omega_2 \pm 2\pi*60$ rad/s are the predominant harmonics present in the DC bus [38]. The first significant line frequency harmonics encountered are comparatively small in magnitude at 360 Hz, as in a three phase diode rectifier or a sinusoidal three phase inverter. The input filter is designed such that these harmonics are attenuated by 90%. The designed LC filter has the following values: L_{dc} = 200 μH; C_{dc} = 100 μF. The high frequency current harmonics in the PV arrays caused by zonal power balancer operation are also attenuated by this filter by more than 99%.

2.3. Simulation Results

The multilevel utility scale system design example rated at 10 MW was simulated, with the operating specifications in table 2.3. The photovoltaic arrays are emulated by a mathematical model. The voltage vector solutions derived previously were shown to produce expected values of individual inverter powers and total system power. Fig. 2.9 shows the converter three phase output voltages and line currents under

uniform full insolation throughout the system. The powers processed by all cascaded cells are equal in this operating condition. The multilevel converter produces a smooth near-sinusoid output voltage which makes it a low distortion system. The line current THD was measured to be 2.8%.

Table 2.3: Cascaded Multilevel PV Inverter System – Specifications

System rating	10 MW, 8 cascaded cells
Medium voltage grid	13.2 kV, 60 Hz, 5% line inductance
Medium frequency transformer	600 Hz
PWM switching frequency	1800 Hz
Modulation	Phase shifted carrier – sinusoidal PWM
PV emulation	Mathematical modeling of PV V-I characteristics

The output voltage vectors of individual inverter modules are in phase and equal in magnitude, as seen in fig. 2.10. The DC bus voltages of inverter cells are all equal to 1000 V.

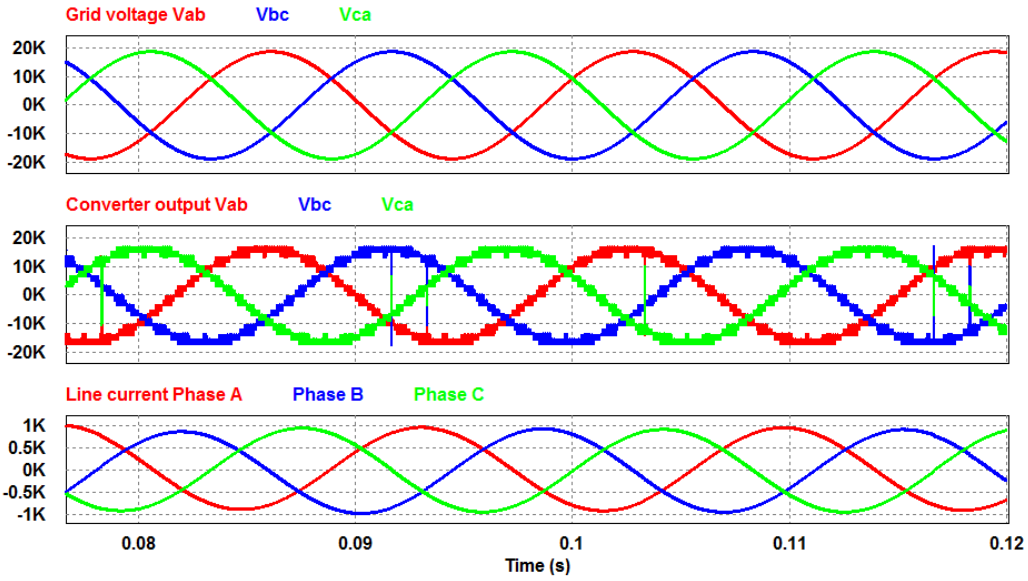

Fig. 2.9: Line currents, converter output voltages and the grid voltage in a multilevel PV system under uniform full insolation

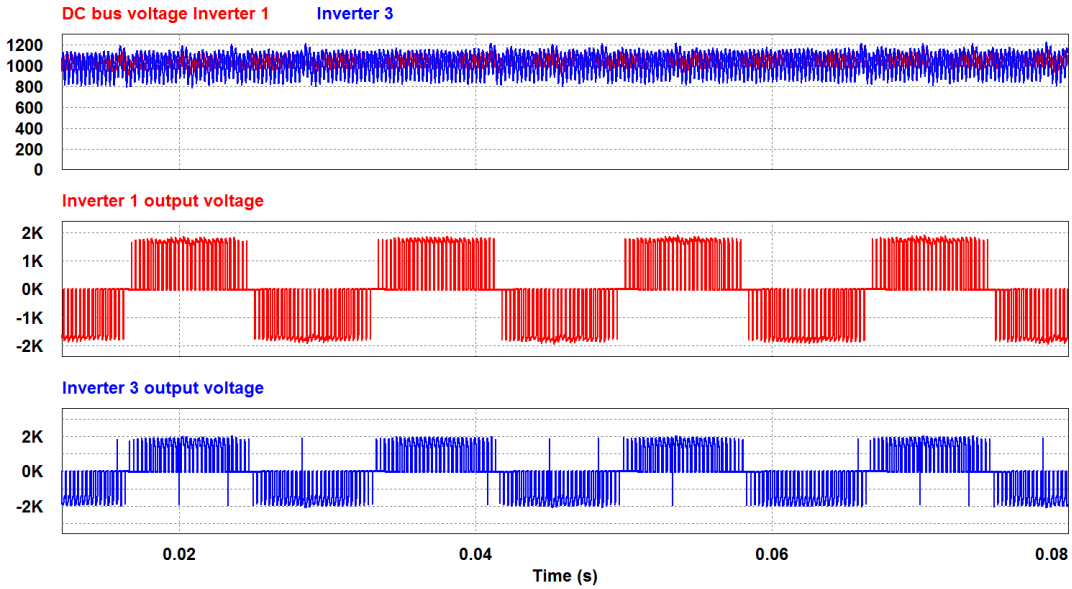

Fig. 2.10: DC bus capacitor voltages in inverter cells 1 and 3 and output voltage of inverter cells 1 and 3, phase A

2.4. Experimental Results

A laboratory prototype was built to validate the design and control of the zonal power balancer. Two bench-top power supplies were used in place of the PV arrays within a zone. The control algorithm was implemented using Texas Instruments TMS320F28035 microcontroller. The voltage and current waveforms of the power balancing inductor with the two voltage sources at 14.4 V and 21.6 V are given in fig. 2.11. The two voltage sources were observed to carry different currents (4.2 A and 0.7 A, average values) and the difference in currents was carried by the power balancing inductor (1 mH). Therefore, source 1 contributes 80% of the total power and source 2 contributes 20% of the power. The inductor current ripple can be varied as per equation (2). The power balancer's reference tracking capability was also tested by quickly varying the current reference signal. Fig. 2.12 gives the current reference (Ch 2) and the actual filtered current through the inductor (Ch 1), when the current reference is time-varying. Current limiting for the power balancing inductor was also provided in the control scheme to ensure safe operation.

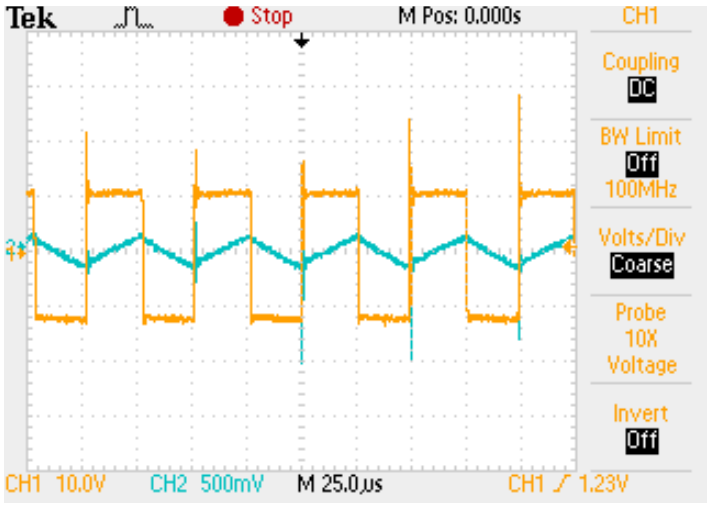

Fig. 2.11: Power balancing inductor voltage (Ch 1: 1 div = 10V) and current (Ch 2: 1div = 5A) waveforms under steady state operation. Inductor carries the difference between currents through the two sources.

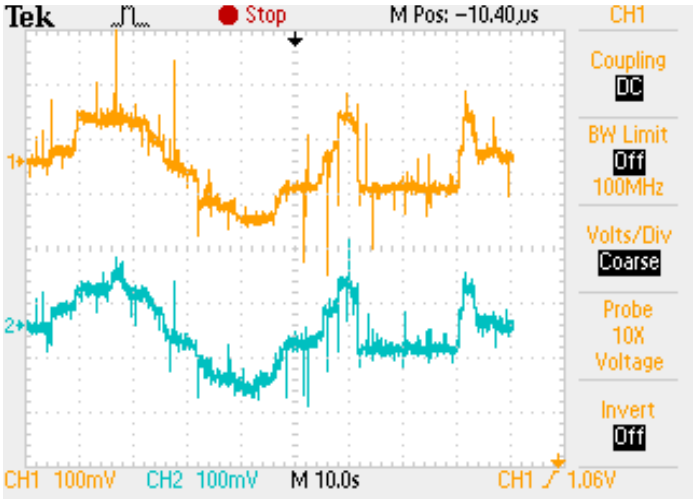

Fig. 2.12: Reference tracking performance of the power balancer circuit. Ch 2 is the current reference, the difference in source currents and Ch 1 shows the actual inductor current (1 div = 5A)

A 135 V, 12 A, 600 Hz medium frequency transformer with four windings, with a peak flux density of 0.62 T was designed, the specification of which are given in table 2.4. The efficiency of the transformer was calculated by experiment to be 97.5%.

Table 2.4: MF Transformer Design Specifications

Parameter	Value	Unit	Parameter	Value	Unit	Parameter	Value	Unit
A_e	2.00	ADJ. ST.	K_3	0.749		W_w	0.203	m
A_eA_c	12.48	REQ'D	K_2*K_3	0.235		*CoilW*	0.19	m
A_eA_c	8.00	SQ. ST.	*VA_tot*	6648	VA	*MLT*	0.232	m
A_eA_c	16.00	ADJ. ST.	B_m	0.623	T	*volt/t*	1.92	V/t
W_{wt}	2.5129	kg	B_{ac}	0.623	T	*Skin depth*	0.003	m
C_{wt}	5.289	kg	C_{loss}	34.98	W			
W_{vol}	0.0012	cu. m	W_{loss}	40.01	W			
C_{vol}	0.0008	cu. m	T_{rise}	79	°C			

One level of the multilevel inverter was built using four single phase inverters, one for square wave generation connected to one winding of the transformer and the rest of the three windings function as secondaries, connected to three, single phase indirect matrix converters. The secondaries were connected to diode rectifiers and followed by single phase inverters. The switching frequency of the inverters was 2880 Hz, providing for 48 PWM pulses per cycle. The AC output of the three inverters is connected to a three phase inductive load. Fig. 2.13 shows the output line-line voltages V_{AB} and V_{BC} in the three phase inverter operating at about 230 W.

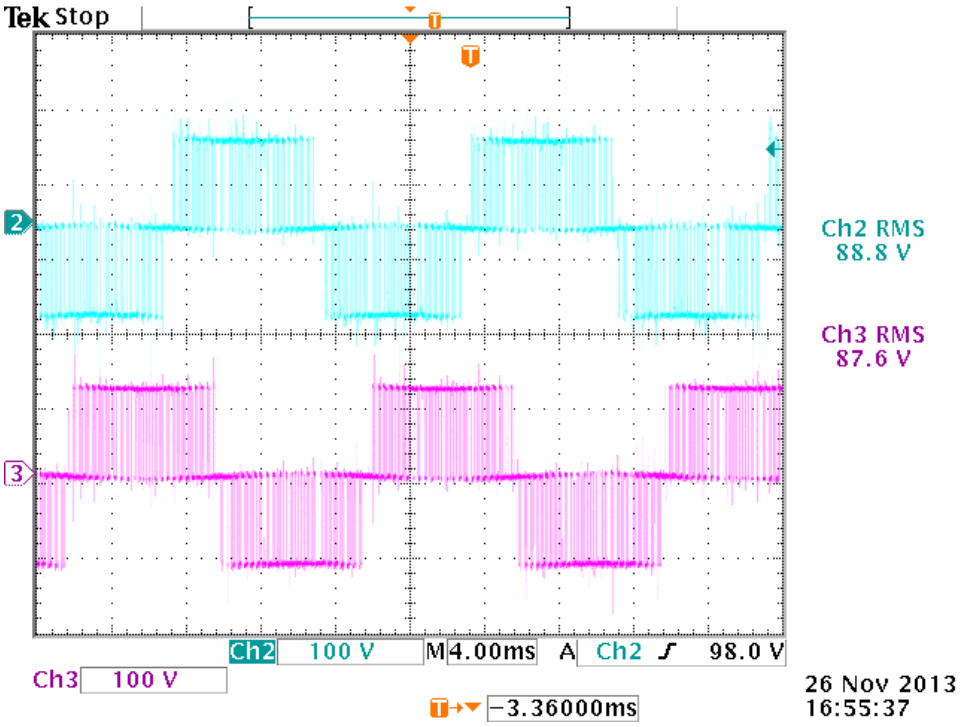

Fig. 2.13: Line-line output voltages in one cell of multilevel inverter – V_{AB} (channel 2) and V_{BC} (channel 3)

The line currents I_A, I_B and I_C are in fig. 2.14, showing balanced three phase operation. The currents in the medium frequency transformer primary and two of the secondaries are shown in fig. 2.15. It can be seen the secondary currents are medium frequency square wave pulses containing the inverter switching frequency component and a 120 Hz component superimposed. The 120° phase shift between the 120 Hz components in the three phases leads to their cancellation on the primary side. It may be recalled that in existing cascaded multilevel topologies in which each phase is supplied by an isolated PV array, a 120 Hz component exists on the PV side.

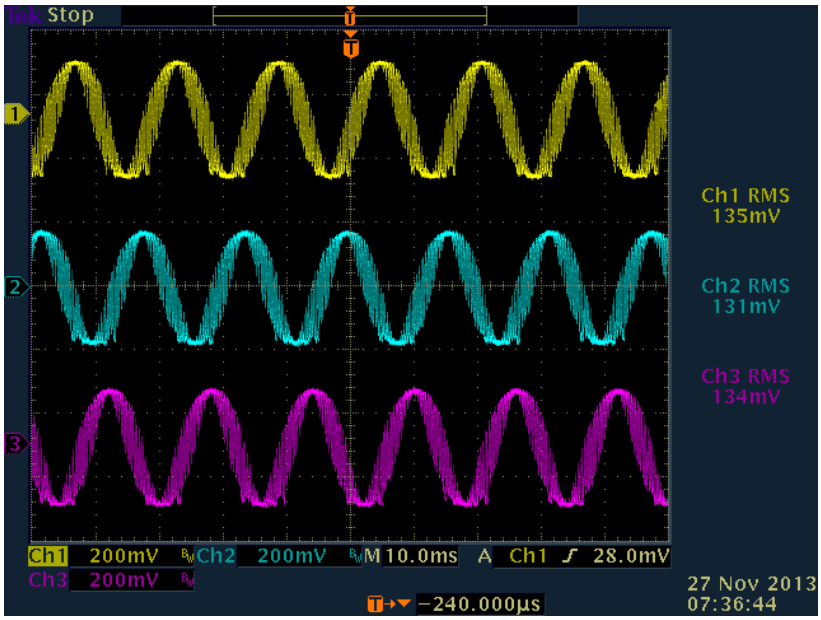

Fig. 2.14: Three phase balanced line currents I_A (channel 1), I_B (channel 2) and I_C (channel 3) in one cell of multilevel inverter operation

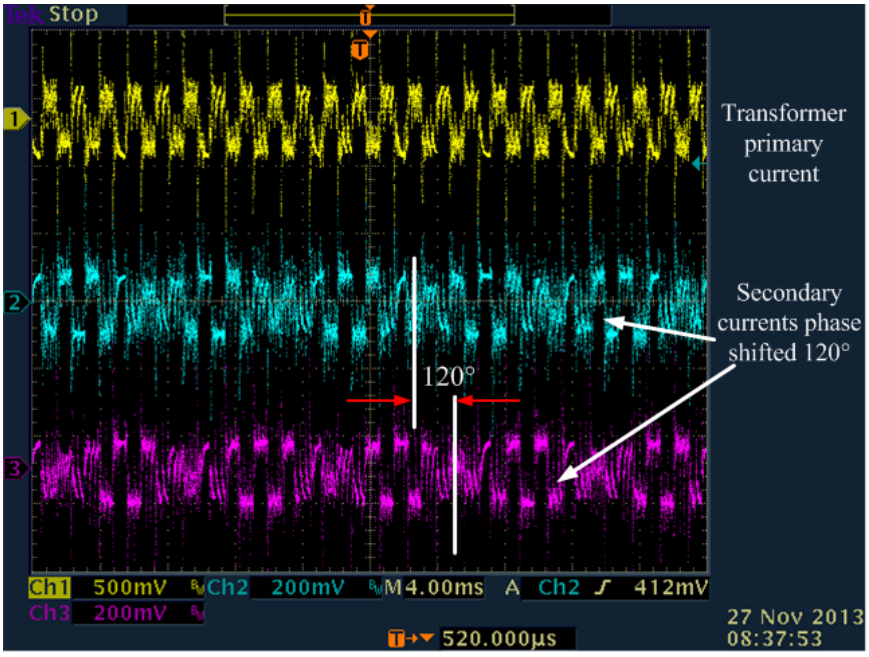

Fig. 2.15: Medium frequency transformer primary current (Channel 1), secondary current phase B (Channel 2), phase C (Channel 3). The 120° phase shift in the 120 Hz components in the three phases leads to cancellation of these currents in the primary

2.5. Conclusion

In this chapter, the proposed topology for a multilevel medium frequency AC link inverter for PV integration to the medium voltage grid was introduced. A unique current sharing approach has been introduced to achieve zonal MPPT. The multi output transformer provides a 120° phase shift in the DC side currents for the three phases, ensuring that the 120 Hz components are cancelled. Amplitude and phase modulation of individual inverter cell output voltages enables the cells to process different values of powers without increasing the device ratings or introducing any additional common mode voltages on the grid side.

3. CONTROL STRATEGY FOR CASCADED MULTILEVEL INVERTERS UNDER ASYMMETRIC INSOLATION*

3.1. Introduction

The control objective under partial shading aims to identify the appropriate modulation index m_a and phase angle δ_i for each series-connected inverter. The control of output voltage magnitude and power angle in the case of parallel–connected generators and inverters has been studied thoroughly [40-44]. Parallel connected inverters share the load based on their VA rating, with larger rated inverters processing a larger share of the load. This feature known as "droop control" is inherently present in synchronous generators and built into the controller of power electronic converters. A similar control strategy is proposed for cascaded multilevel inverters in this chapter for unequal insolation amongst the inverter cells.

3.2. Control Theory

In the proposed multi-level medium voltage PV topology, single phase inverters are cascaded to produce the system AC voltage. When unbalanced insolation happens i.e., modules connected to some of the inverters are shaded, the power available to those inverters is substantially less than power available to fully illuminated module inverters. Since the cascaded inverters are required to produce a specified resultant voltage, the line current reduces as an effect. The inverters receiving reduced DC power limit the

* This chapter is adapted from [39] S. Essakiappan, H. S. Krishnamoorthy, P. Enjeti, R. S. Balog, and S. Ahmed, "A new control strategy for megawatt scale multilevel photovoltaic inverters under partial shading," in *3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2012, pp. 336-343. Digital Object Identifier: 10.1109/PEDG.2012.6254023

current through the multilevel converter. Various techniques have been proposed to eliminate phase and cell imbalances and process different powers [15, 16, 18] [45-49]. But techniques involving voltage magnitude modulation or zero sequence injection may require use of higher voltage semiconductor devices and increased reactive power flow. A control theory is developed in this section to enable individual inverters to process different amounts of power while carrying the same current, by voltage amplitude and phase modulation. The real and reactive power flows between two AC sources are given by the following expressions in (12) and (13).

$$P = \frac{|\mathbf{V_1}||\mathbf{V_2}|}{X_S}\sin(\delta_1 - \delta_2) \tag{12}$$

$$Q = \frac{|\mathbf{V_1}|^2}{X_S} - \frac{|\mathbf{V_1}||\mathbf{V_2}|}{X_S}\cos(\delta_1 - \delta_2) \tag{13}$$

where $V_1\angle\delta_1$ and $V_2\angle\delta_2$ are the sending and receiving end ac voltages, X_S is the line impedance, P and Q are the real and reactive powers transferred. The real power available to the inverters from the PV modules is provided by the individual MPPT algorithm. In an n inverter system, the real power available to each inverter is represented as P_i and the sum of all powers gives the total system real power.

$$P_{total} = \sum_{i=1}^{n} P_i \tag{14}$$

Now P_i can be written as follows.

$$P_i = \frac{|\mathbf{V}_i|\left|\mathbf{V_S} - \sum_{\substack{j=1 \\ j \neq i}} \mathbf{V}_j\right|}{X_S}\sin(\delta_i - \overline{\delta_i}) \tag{15}$$

where $\overline{\delta_i}$ is the angular coordinate of the receiving resultant voltage $\mathbf{V_S} - \sum \mathbf{V}_j$. For an n inverter topology, the voltage output of each inverter can be represented as $V_i \angle \delta_i$, and the vector addition of all the inverter output voltages gives the string voltage of one phase, represented as $V_{AO} \angle \delta$.

$$\mathbf{V_{AO}} = \sum_{i=1}^{n} \mathbf{V}_i \tag{16}$$

The total real power transferred can now be represented as in (17).

$$P_{total} = \frac{|\mathbf{V_{AO}}||\mathbf{V_S}|}{X_S} \sin \delta \tag{17}$$

Using the equations above, the power processed by individual inverters P_i can be controlled by adjusting V_i and δ_i while satisfying the above conditions for P_i and P_{total} [50, 51]. The voltages and angles of individual inverters are controlled in such a way that the overall system power factor is maintained at unity. It is to be noted that the power output from one cell is not only dependent on the output voltage magnitude and phase of the respective inverter, but also on all the other inverters.

When all the photovoltaic modules are uniformly illuminated, the voltage vectors produced by cascaded inverters are all of equal magnitude and in phase, as seen in Fig. 3.1. The total power production for an n inverter system is simply, n times the power from one inverter. This balance is disrupted when partial shading occurs, reducing the power available to one or more inverters.

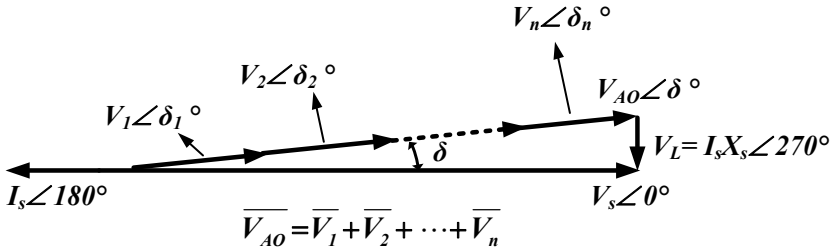

Fig. 3.1: Voltage vectors in a multilevel series connected inverters with fully illuminated PV arrays. The vectors are in phase and of equal magnitude. V_L is voltage across line impedance.

When *m* inverters out of *n* receive reduced power due to shading, the output voltage vectors of those inverters are reduced in magnitude and the remaining (*n-m)* inverters have higher output voltage magnitudes than the ideal case. There are multiple solution sets possible for the voltages and angles. One solution is to maintain unity power factor for the healthy inverters and set the voltage vectors of the shaded inverters in such a way that the addition of all voltage vectors produces the required multilevel phase voltage, while the overall system power factor remains close to unity. When total PV power decreases further, the voltage output of the healthy inverters has to increase to a maximum level, for a fixed DC voltage bus. Under such circumstances, the system power factor starts to decrease with available DC power. Fig. 3.2 provides the general solution for voltage vectors in the case of *m* shaded inverters.

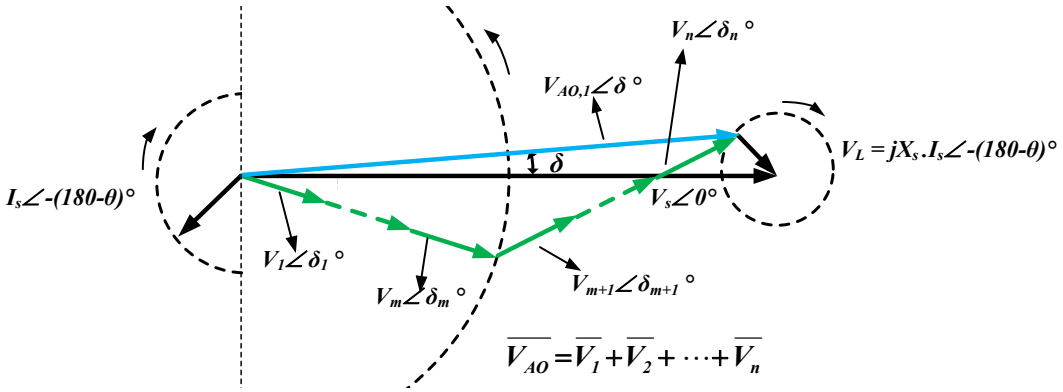

Fig. 3.2: General solution for voltage vectors in a multilevel series connected inverters with *m* shaded inverters.

In the medium voltage multi-level 10 MW PV system example, there are eight cascaded inverter modules. In order to demonstrate the control theory for operation under unbalanced insolation, the shading conditions in fig. 3.3 were assumed.

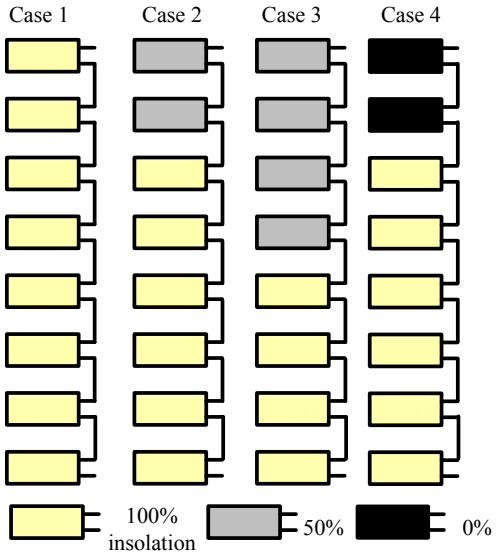

Fig. 3.3: Four cases of insolation pattern for the eight zones in 10 MW design example

Table 3.1: Solutions of Multilevel Inverters Voltage Vectors for Power Sharing – Four Different Cases

Note - $P_1 – P_8$: Fraction of power available from the eight PV zones; $V_1 – V_8$: per-unit voltage vectors; V_{ao}: Multilevel converter output voltage; PF: Displacement power factor

$P_{1,2}$	$P_{3,4}$	$P_{5,6}$	$P_{7,8}$	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_{AO}	PF
1	1	1	1	0.9538 ∠2.86°	0.9538 ∠2.86°	0.9538 ∠2.86°	0.9538 ∠2.86°	0.9538 ∠2.86°	0.9538 ∠2.86°	0.9538 ∠2.86°	0.9538 ∠2.86°	7.6305 ∠2.86°	1
0.5	0.5	1	1	0.5692 ∠17°	0.5692 ∠17°	1.0887 ∠0°	1.0887 ∠0°	1.0887 ∠0°	1.0887 ∠0°	1.0887 ∠0°	1.0887 ∠0°	7.6283 ∠2.5°	1
0.5	0.5	0.5	0.5	0.7958 ∠-22.58°	0.7958 ∠-22.58°	0.7958 ∠-22.58°	0.7958 ∠-22.58°	1.2073 ∠18.19°	1.2073 ∠18.19°	1.2073 ∠18.19°	1.2073 ∠18.19°	7.5325 ∠2.17°	0.95
0	0	1	1	0.8953 ∠-71.74°	0.8953 ∠-71.74°	1.2073 ∠15.91°	1.2073 ∠15.91°	1.2073 ∠15.91°	1.2073 ∠15.91°	1.2073 ∠15.91°	1.2073 ∠15.91°	7.5325 ∠2.17°	0.95

The inverter output voltages and angles are calculated such that the individual inverter cells process their respective available DC power, and the overall plant power factor is as close to unity as possible. Table 3.1 gives the solutions as calculated as per this control objective. From the table it becomes clear that for this design, if 0.95 is taken to be the minimum system power factor, cases 3 and 4 represent the limits of unbalanced insolation. If the design needs to accommodate further shading, the voltage ratings of the switches and the medium frequency transformer will have to be increased.

3.2.1. Effect of Modulation Index Control on Output Voltage THD

Multilevel inverters are designed to produce high quality (low THD) output voltage waveforms. This is made possible by different modulation techniques such as space vector modulation and phase shifted carrier sinusoidal modulation. In the phase

shifted carrier method, the carrier signals for each cell of the cascaded inverter are phase shifted from each other, producing output voltage pulses which are themselves phase shifted. This leads to the output voltage containing many levels, as defined by the number of cascaded cells. However, this property is true only when the modulation indices of all the cascaded cells are equal. The proposed control theory calls for modulation index and phase angle control, which could lead to the cells having different modulation indices. This leads to higher output voltage THD, as seen from fig. 3.4. The THD is the least if all the modulation indices are equal. As the difference between the highest index and the lowest increases, the THD begins to increase. Hence the output voltage THD performance may deteriorate upon partial shading.

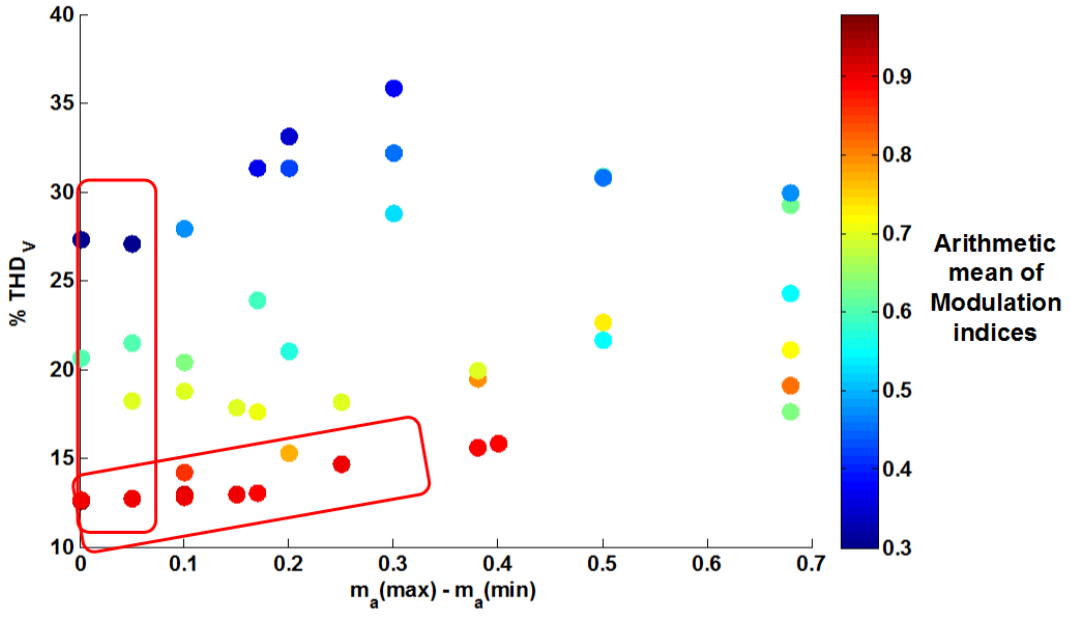

Fig. 3.4: Multilevel inverter output voltage THD for unequal modulation indices amongst cascaded cells

The red rectangles in the figure represent the likely regions of operation since extreme disparities in output voltage are not expected to occur in a significant number of cells. If there is a reduction in the modulation index of one cell it is accompanied by a change in modulation indices of other cells, as seen from the solution table.

3.3. Parallel and Cascaded Inverters Control

Conventional generating stations connected in parallel to the utility grid employ droop control methods to accomplish real power sharing. Fig 3.5 shows a system with two generators connected in parallel to the infinite bus at node G. When the system load increases, the frequency is reduced momentarily changing the power angles of the inverters δ_1 and δ_2 and the powers P_1, P_2, Q_1 and Q_2 are supplied, depending on the droop coefficient values of the generators m_1 and m_2, as shown in fig. 3.6. For parallel connected inverters, the droop characteristics for voltage and frequency are introduced in the controller. In this configuration, the inverters are connected to the same grid voltage and frequency.

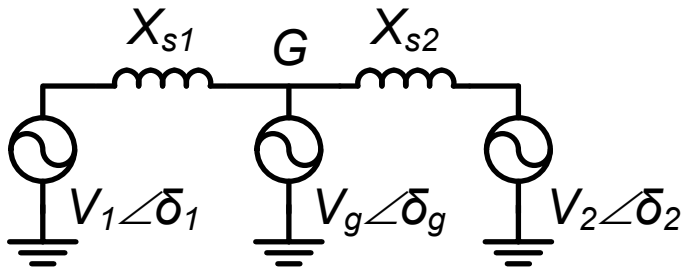

Fig. 3.5: One-line diagram of a parallel-connected two inverter system interfaced with infinite bus G. The phase angle δ_g of bus G is usually taken as the reference bus, 0°

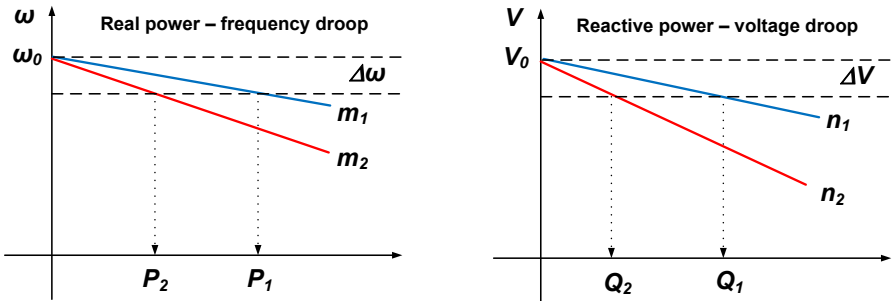

Fig. 3.6: Frequency and voltage droops used in parallel connected inverters for effective power sharing, based on the ratings of the inverters [41, 42]

When the inverters are cascaded, the control becomes complex because the sum of individual voltage vectors gives the multilevel inverter voltage. Also, as can be seen from (8) and (9), the real and reactive powers from every inverter are dependent on the voltage magnitudes and phase angles of *all* the inverters. The proposed control algorithm calls for continuous monitoring of the real and reactive powers at the output of every inverter. The control is in-house for each inverter and there is no communication amongst the inverters. It is however assumed that information is available about the reference phase angle from the grid side for synchronization purposes.

3.4. Proposed Control Strategy by Continuous Monitoring

The proposed control strategy is a direct power control method and is described in Fig. 3.7 [39]. The real power from each inverter is continuously calculated from the measured voltages and currents. It is then compared with the result of the MPPT algorithm, which is the available power from that zone of PV arrays. If the inverter real

power output is less than the available power, the phase angle δ_i of the sinusoidal reference signal is adjusted in transient mode.

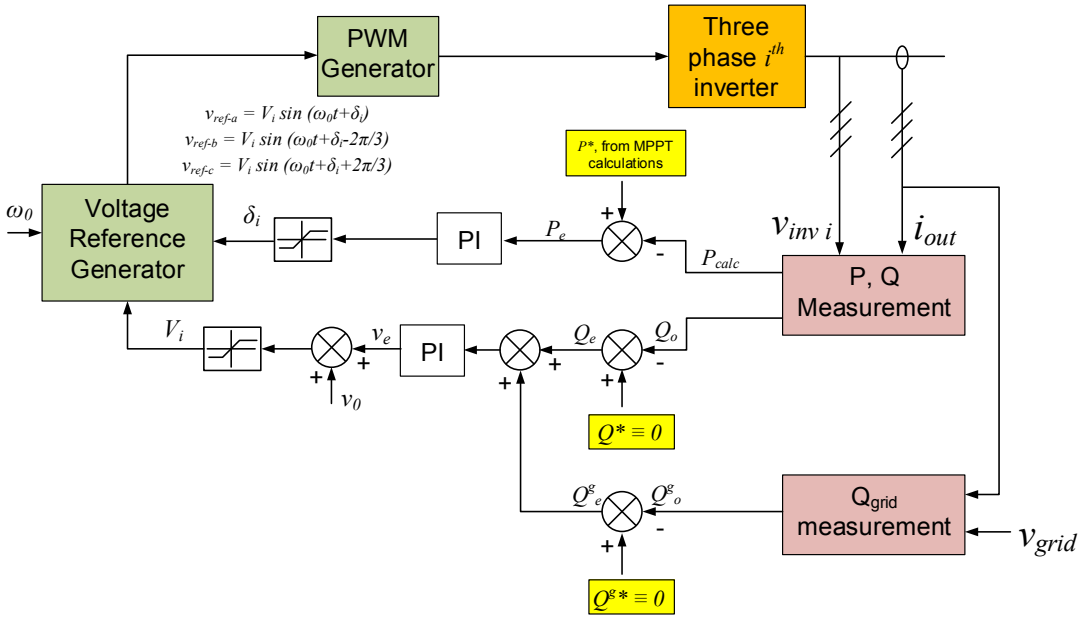

Fig. 3.7: Control algorithm for the operation of one inverter. Phase angle δ_i and modulation index ma of sinusoidal modulating signals are varied based on real power P_o and reactive power Q_o

The voltage loop has two parts: the first part calculates the reactive power production / consumption from the inverter and compares it with a desired value; the second part calculates the reactive power flowing to / from the grid and compares it with a desired value, to generate the voltage magnitude of the PWM modulating signal, i.e. the modulation index. Since an individual inverter cell does not have the reference angle information for the other inverter cells, it is possible for them to settle at different power angles with respect to the grid. If excessive reactive power is supplied, it is indicative of

the inverter output voltage being higher than optimal; so the modulation index has to be reduced. On the other hand, if excessive reactive power is consumed, the voltage magnitude is lower than the optimal value and this requires an increase in the modulation index. Any unfavorable mismatch between the overall converter voltage and the grid voltage causes an increased reactive power flow and hence it is detectable.

3.5. Multilevel Inverter Modeling and Analysis

The deduction of a small signal model for the multilevel inverter begins with formulating the average switch model of the inverter. As discussed in chapter 3, the triangular carriers are phase shifted by $\frac{360°}{N}(i-1)$ for the i^{th} inverter in an N inverter system (N odd). For simplicity in analysis a three cell cascaded system is considered, shown in fig. 3.8.

3.5.1. Average Model of Cascaded Multilevel Inverter

The output of the multilevel inverter is the sum of individual inverter cells' output voltages. This may be expressed as $v_{inv} = \sum_{i=1,2,3} v_{ac-i}$. To develop the average model, the inductor voltage v_L for when the switches are on, and when they are off are to be determined and their average is equal to zero, within that switching period [52]. This is possible because it is assumed that the modulating signal is constant within a switching period. Positive half-cycle of the output voltage is assumed.

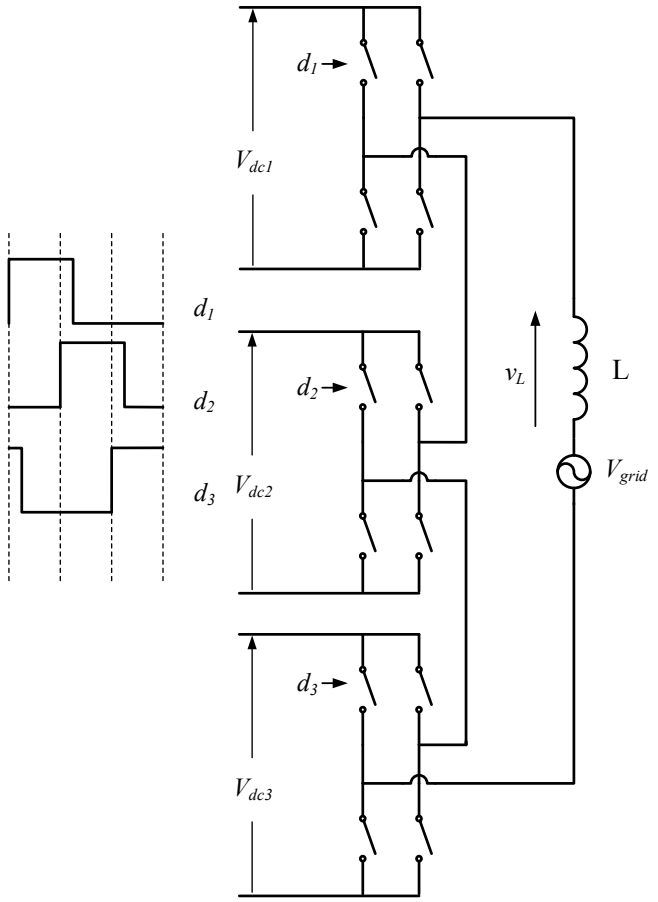

Fig. 3.8: Three cell cascaded multilevel inverter for analyzing average and small signal model

The duty cycles are (or, output voltages of inverters are positive during) d_1, d_2 and d_3. The average model is found as below.

$$s\ ON:\ v_L = V_{dc1} + V_{dc2} + V_{dc3} - V_{grid}$$

$$s\ OFF:\ v_L = -V_{grid}$$

$$\langle v_L \rangle = \left\langle L\frac{di}{dt} \right\rangle = d_1 V_{dc1} + d_2 V_{dc2} + d_3 V_{dc3} - (d_1 + d_2 + d_3) V_{grid} + (1 - d_1 - d_2 - d_3)(-V_{grid})$$

$$\langle v_L \rangle = d_1 V_{dc1} + d_2 V_{dc2} + d_3 V_{dc3} - V_{grid}$$

If the DC bus voltages are assumed to be equal (which is true in most cases of multilevel inverters) the switched average model equation for inverter current becomes

$$\langle v_L \rangle = \left\langle L \frac{di}{dt} \right\rangle = (d_1 + d_2 + d_3) V_{dc} - V_{grid} \text{ or}$$

$$\overset{\circ}{i} = \frac{(d_1 + d_2 + d_3) V_{dc} - V_{grid}}{sL} \tag{18}$$

where $\overset{\circ}{i}$ represents the average of the inductor current. From the average model the small signal model equation is developed by perturbing the duty cycles and the response in the inductor current is determined. The grid voltage and the DC bus voltage are not perturbed since they are taken to be constants.

$$\overset{\circ}{i} + \tilde{i} = \frac{1}{sL}\left[\left(d_1 + \tilde{d_1}\right) + \left(d_2 + \tilde{d_2}\right) + \left(d_3 + \tilde{d_3}\right)\right] V_{dc} - V_{grid}$$

This yields the expression given by (19) for output current to duty cycle transfer function as below.

$$\tilde{i} = \frac{(\tilde{d_1} + \tilde{d_2} + \tilde{d_3}) V_{dc}}{sL} \tag{19}$$

It can be seen that the current perturbation response due to one of the duty cycles is dependent on the perturbations in the other duty cycles as well. This expression may be extended to an *N* inverter cascaded multilevel inverter giving the expression (20).

$$\tilde{i} = \sum_{i=1}^{N} \frac{\tilde{d_i} V_{dc}}{sL} \tag{20}$$

3.5.2. Output Power – Phase Angle Control Stability Analysis

The output power of the cascaded multilevel inverter is controlled by adjusting the phase angle of the output voltage of the individual inverters, as described in the control strategy discussed in the previous section. The power (real) flow equation of a single cell of the cascaded inverter is reproduced below.

$$P_i = \frac{|\mathbf{V}_i|\left|\mathbf{V}_\mathbf{S} - \sum_{\substack{j=1 \\ j \neq i}} \mathbf{V}_j\right|}{X_S} \sin\left(\delta_i - \overline{\delta_i}\right)$$

For analysis purposes consider i = 1, the voltage vector $\mathbf{V}_S - \Sigma\ \mathbf{V}_j$ to be V_2 and the phase angle to be simply δ. This changes the above equation to (21)

$$P_1 = \frac{|V_1||V_2|}{X_s} \sin\delta = \frac{|V_1||V_2|}{X_s}\delta \tag{21}$$

Applying the small angle approximation removes the sine function. Also, δ the power angle is the time integral of error in angular frequency, $\Delta\omega$. Equating X_S to sL, the s-domain transfer function of phase angle to output real power is obtained to be

$$P_1 = \frac{|V_1||V_2|}{X_s}\ \delta \xrightarrow{Laplace} P_1(s) = \frac{|V_1||V_2|}{sL}\delta(s) \tag{22}$$

Assigning constant magnitudes of V_1, V_2 and L to 'q', (23) is the plant transfer function

$$G(s) = \frac{P_1(s)}{\delta(s)} = \frac{q}{s} \tag{23}$$

It can be seen that the transfer function is open loop stable. In order to design the closed loop controller, a PI controller was chosen. The transfer function of a PI controller with gains K_P, and K_I (proportional and integral respectively) is given by (24).

$$C(s)=\frac{K_P s+K_I}{s} \tag{24}$$

It is noted that the loop transfer function *G(s)C(s)* contains two poles at origin and the phase is 180° at DC, eliminating any possible gain margin. So alternatively a pole is introduced in the controller away from the origin, with the controller having the following structure given by (25).

$$C(s)=\frac{K_P(s+\alpha)+K_I}{s+\alpha} \tag{25}$$

Now the loop transfer function becomes (26)

$$G(s)C(s)=\frac{(q K_P)s+q(K_P \alpha+K_I)}{s^2+\alpha s} \tag{26}$$

The location of the introduced pole is close to the origin, which contributes to integral action and also, the phase of the loop transfer function is 90° at DC. The zero of the transfer function may now be placed arbitrarily. In order to determine the controller parameters a series of bode plots are drawn with a range of values for K_P and K_I. In fig. 3.9 the curves show the progression of the bode plots with changing K_P and K_I values. The values for K_P and K_I are chosen such that the phase margin is sufficiently large while also providing satisfactory steady state and transient performance. It may also be seen that the system has high gain margin. The location of the assigned zero affects the

dynamic performance of the system; as it moves towards the origin the response becomes faster.

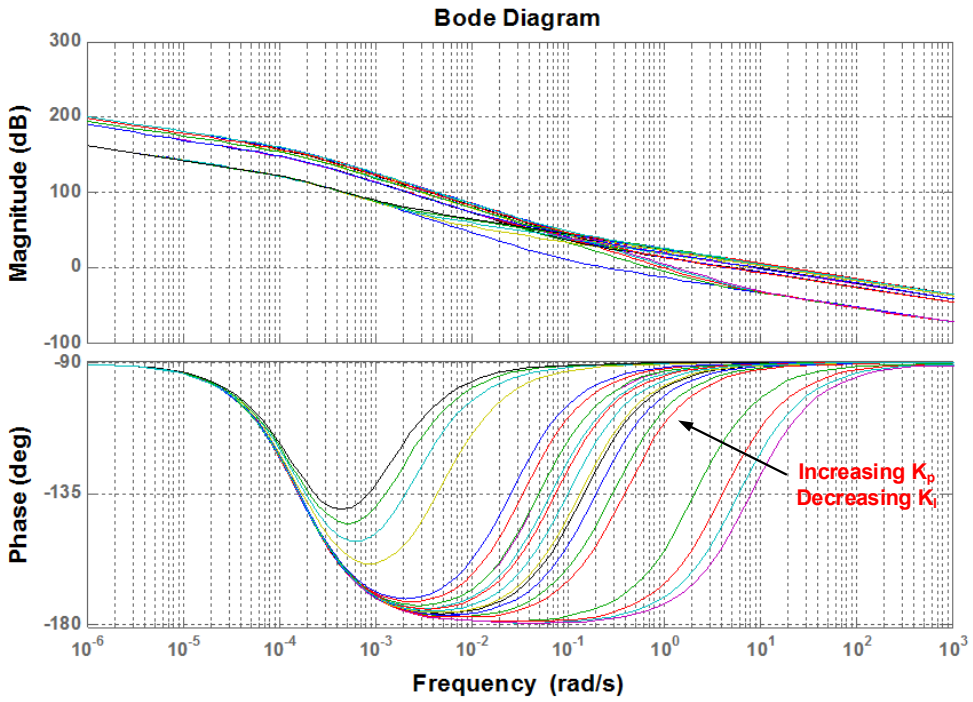

Fig. 3.9: Bode plot of system loop gain for a range of K_P and K_I values

This analysis provides the design procedure for one cell of the cascaded inverter. Once the cells are cascaded, changes in the output of one cell affects the feedback signals of the other cells as well. The controller of a cell in such a circumstance responds to this "disturbance" by adjusting its own output. Multiple cascaded inverters operating simultaneously in this manner could increase oscillations in the output of the system. With the available design, in order to ensure that fast dynamic responses to such changes do not affect the overall system output power, the zero and pole of the controller are

appropriately moved away from the origin, while the bode plot progression is as shown in fig. 3.10. This slows down the dynamic response of the individual inverters but improves overall system performance.

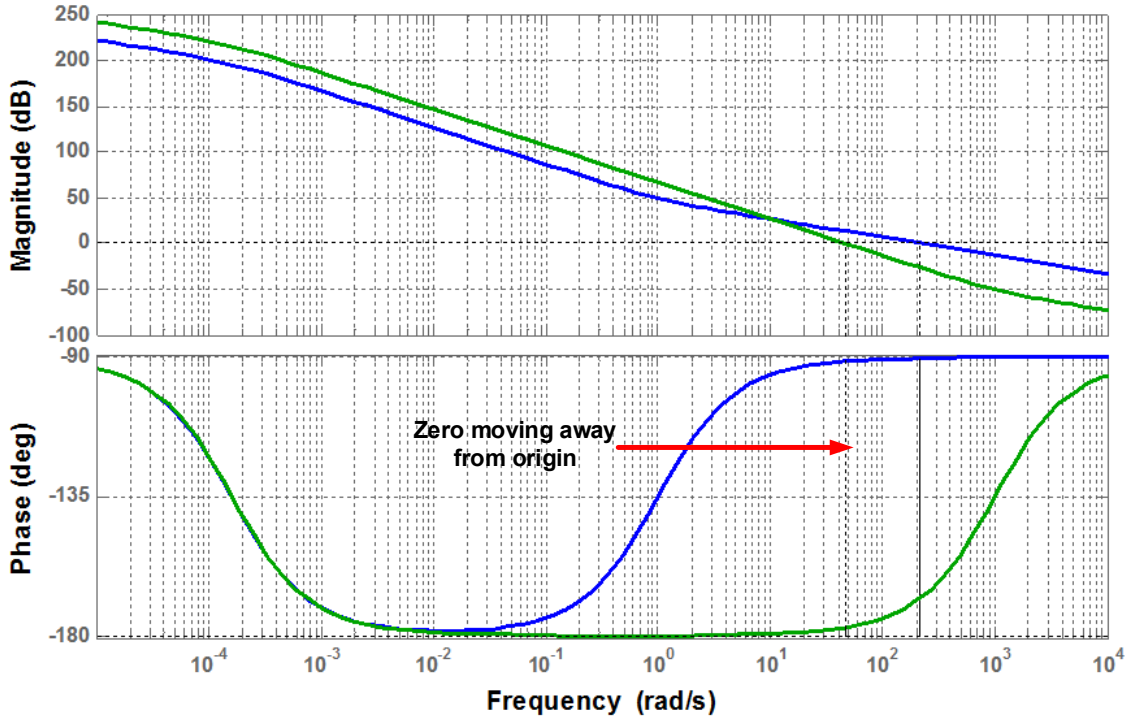

Fig. 3.10: The controller zero is moved away from origin to improve dynamic performance of the cascaded system

The values of α, K_P and K_I are calculated for the new position of the zero and the pole. The operation of the converter with the designed controller will be designed for rejection of disturbance at the power reference input.

3.6. Operation of Control Algorithm under Changing Insolation Conditions

The operation of the multilevel inverter assumes that the transition from one insolation level to another occurs slowly, when compared to the speed of operation of the controller, or the duration of one cycle of the grid voltage. It is also assumed that the MPPT controller operates at a much higher speed, compared to one cycle of the grid voltage.

When the insolation changes for one zone the phase angle and modulation index for that zonal inverter change, prompting an adjustment in the other inverters' voltage vectors as well. Ultimately, this process repeats and all the voltage reference signals converge to a steady state, as long as the new insolation persists. The controller parameters have to be carefully chosen as described in previous section, so as to prevent the power angle and voltage adjustment from rendering the whole system unstable. Also, the settling times during step changes in insolation have to be short, considering the fact that the real power load demand during this transient has to be met by the DC bus capacitors. A long settling time would mean that the capacitors have to be large in size to enable the plant to sustain the energy transfer to the grid during transients, without leading to output voltage sags or swells.

The grid power factor of the system is dependent the number of zones which are shaded and also, the depth of shading. Large number of shaded zones or some zones receiving too little insolation might affect the power factor. But extreme disparities in insolation such as some zones receiving near-zero while some receive full insolation are very unlikely to occur.

3.7. Simulation Results

The multilevel inverter system discussed in chapter 2 was simulated in PSIM with the specifications in table 3.2.

Table 3.2: Multilevel Inverter for Closed Loop Analysis - Specifications

Number of cascaded inverters cells	4
System power rating	5 MW
System voltage	6.6 kV
Medium frequency transformer	600 Hz
PWM switching	1800 Hz Unipolar modulation
Grid line impedance	10%
Controller parameter K_P	1×10^{-8}
Controller parameter K_I	1×10^{-5}
Reactive power loop gain K_P	1×10^{-10}

It is to be noted that all three phases of one level of the multilevel inverter are connected to the same zone of photovoltaic arrays and produce the same amount of power. The system is first simulated for consistent, 100% insolation in all PV zones. In this scenario, the real powers produced by all the three phase inverters are equal and the power factor is near-unity.

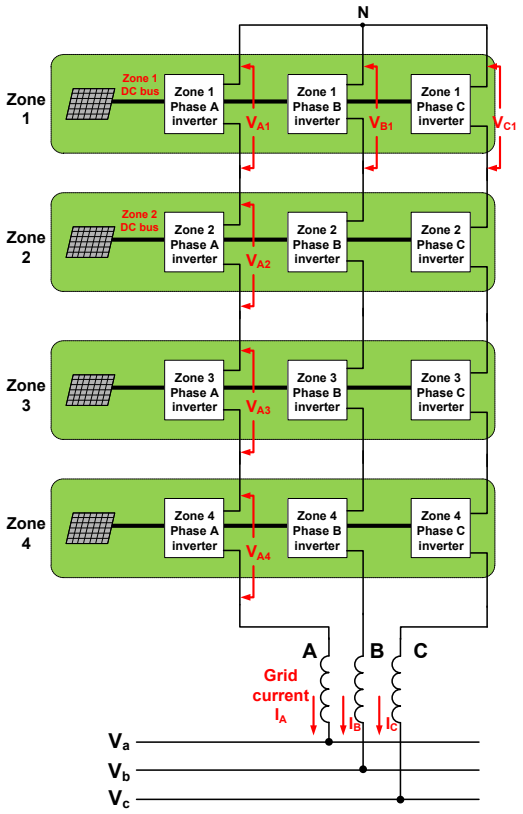

Fig. 3.11: Four cascaded three phase inverters with medium frequency transformer isolation interfaced with medium voltage utility grid

The output voltage of once cell of the cascaded multilevel inverter is shown in fig. 3.12. The converter operates using unipolar modulation and from the cascaded line-line voltage waveform the high quality of the output voltage waveform is evident. The sum of individual inverter output voltages such as in fig. 3.11 are vectorially added to produce the overall output voltage of the cascaded inverter.

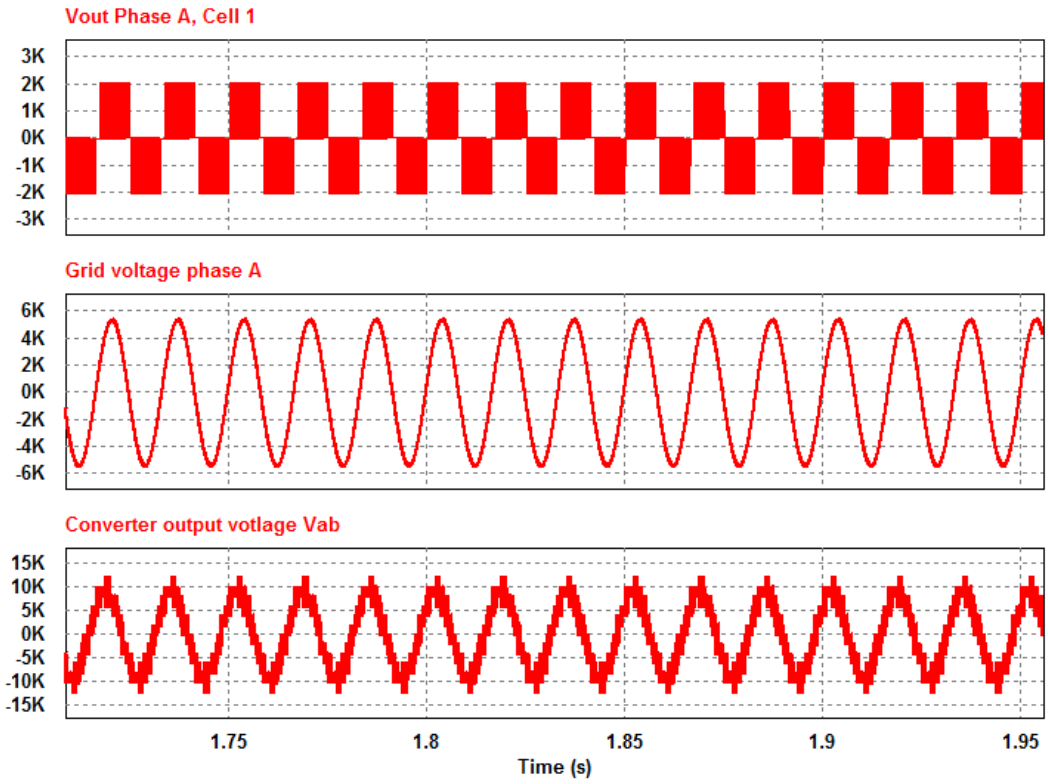

Fig. 3.12: Output voltage of one cell of the cascaded inverters, the grid voltage and multilevel inverter overall output voltage and in a PV system under uniform full insolation.

When all the PV zones receive equal power at 100%, the phase angles of the individual inverter cells settle at any steady state value, required to produce the reference power. It is seen from fig. 3.13 that the real powers produced by all the inverters are equal. The modulation indices of all the inverters are equal to 0.7. Fig. 3.14 shows the grid side phase-to-neutral voltage and line current with system power factor calculated to be 98%.

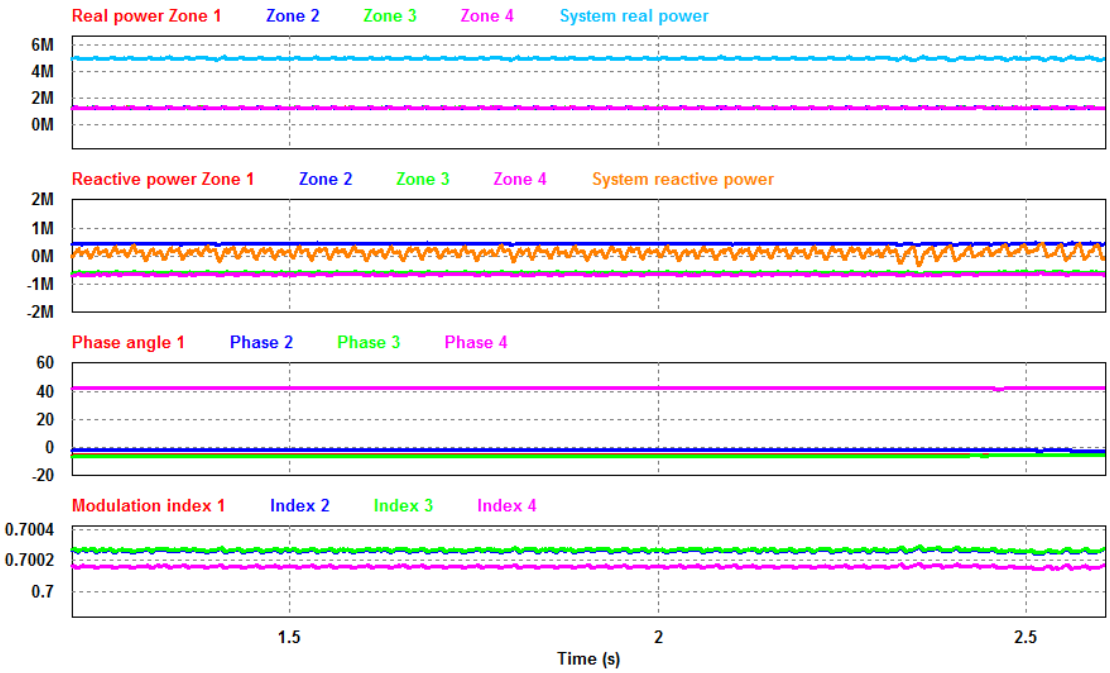

Fig. 3.13: Steady state operation of cascaded inverters with equal insolation at 100%

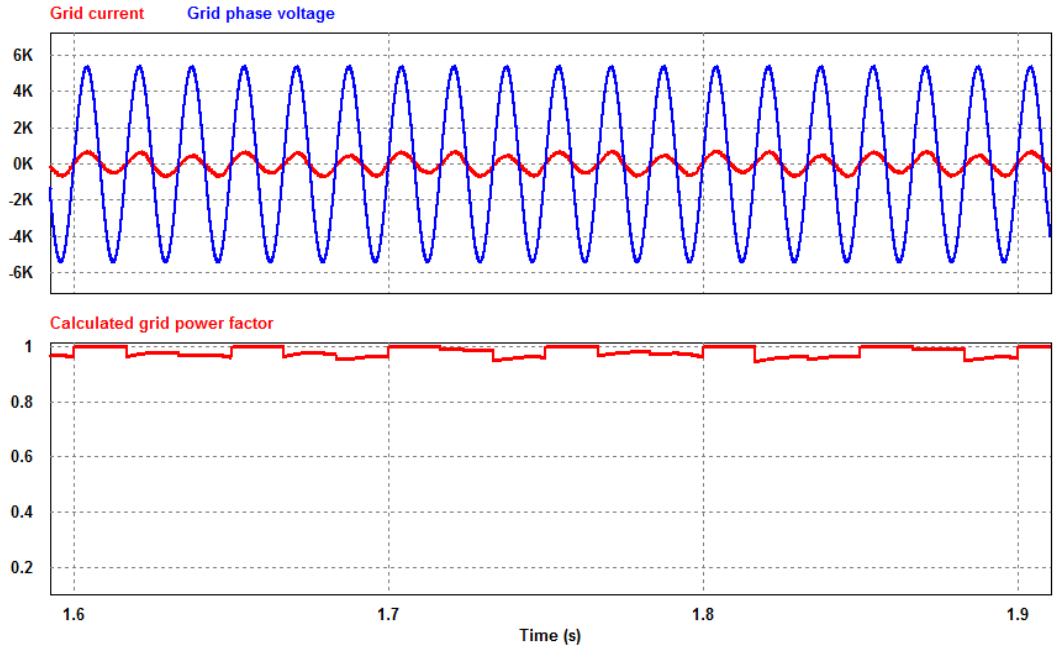

Fig. 3.14: Grid phase-neutral voltage and current showing unity power factor operation

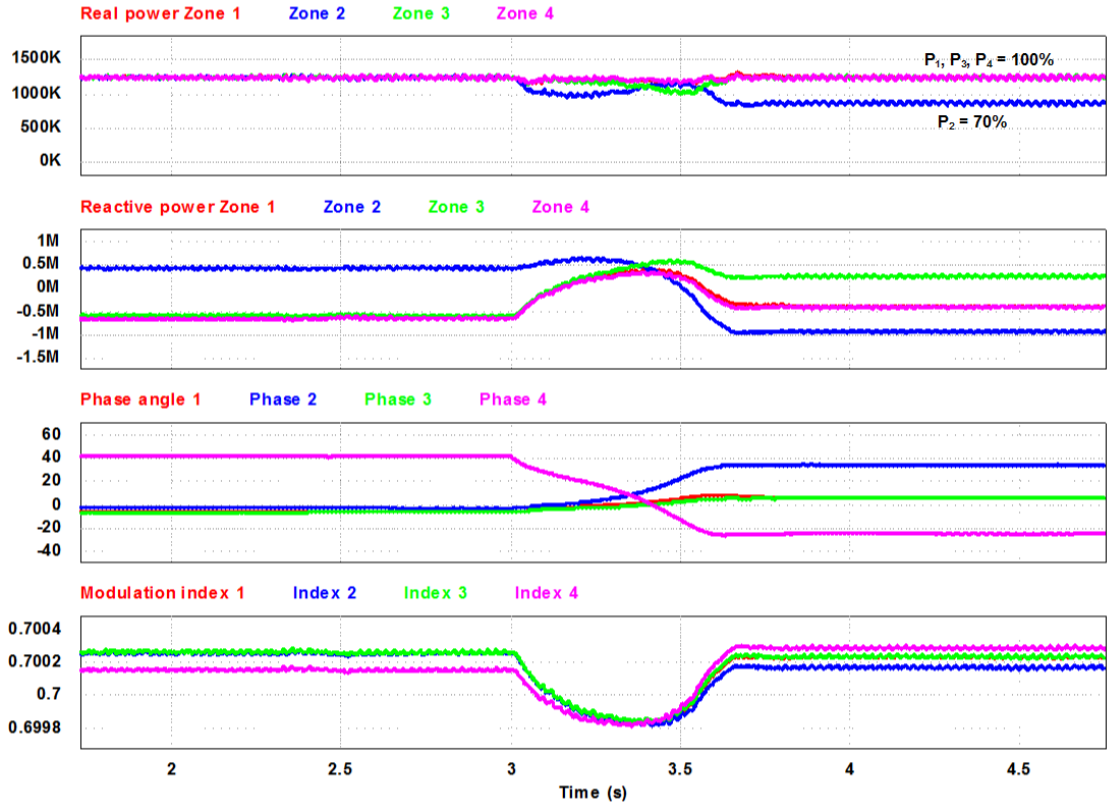

Fig. 3.15: Step change in reference power for inverter 2, at t = 3 s

In order to test the controller performance the reference real power to the controller of inverter 2 is changed to 70% of full power. It can be seen in fig. 3.15 that the phase angle of inverter 2 (and the other inverters in reaction to it) change and settle at a new value. The modulation indices also vary accordingly to produce the appropriate powers. It may also be seen from fig. 3.16 that the system continues to operate at near-unity power factor after a brief perturbation.

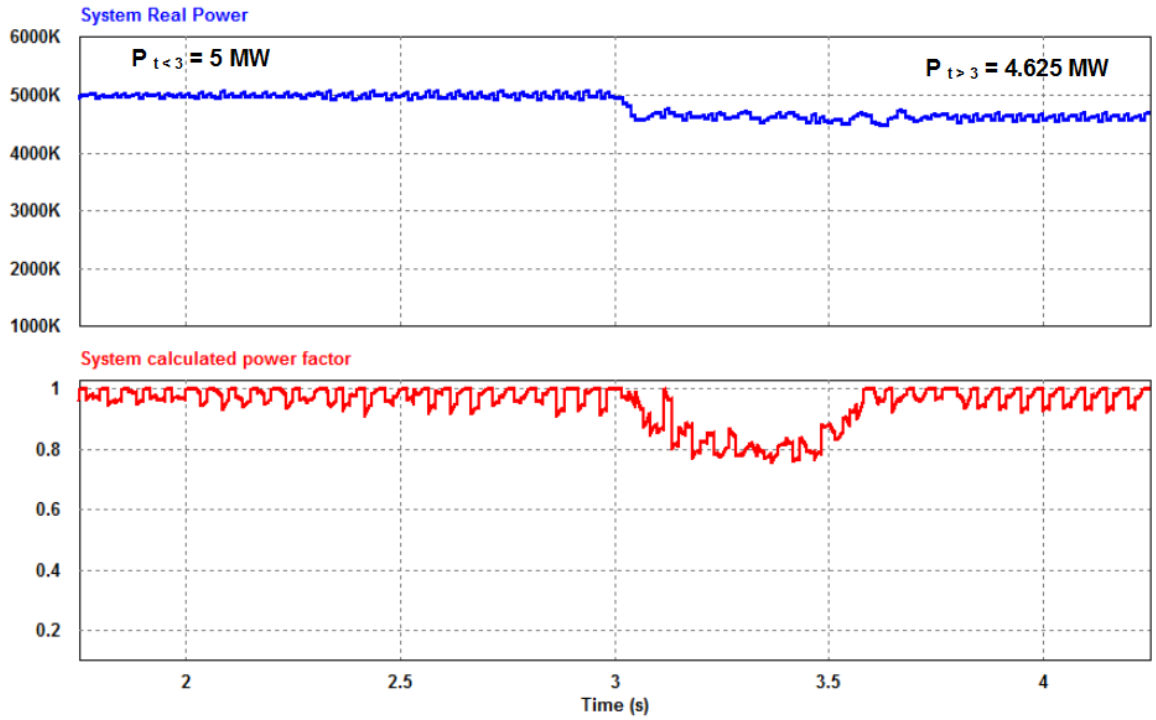

Fig. 3.16: System grid real power step response and system power factor

Fig. 3.17 demonstrates the tracking capability of the controller, with the real power reference for individual inverters changing at t = 6 s and t = 8 s. The phase angles and modulation indices are adjusted, to track the real power reference input. The real power reference of inverter 3 is reduced to 60% at t = 6 s and that of inverter 2 is returned to 100% at t = 8 s.

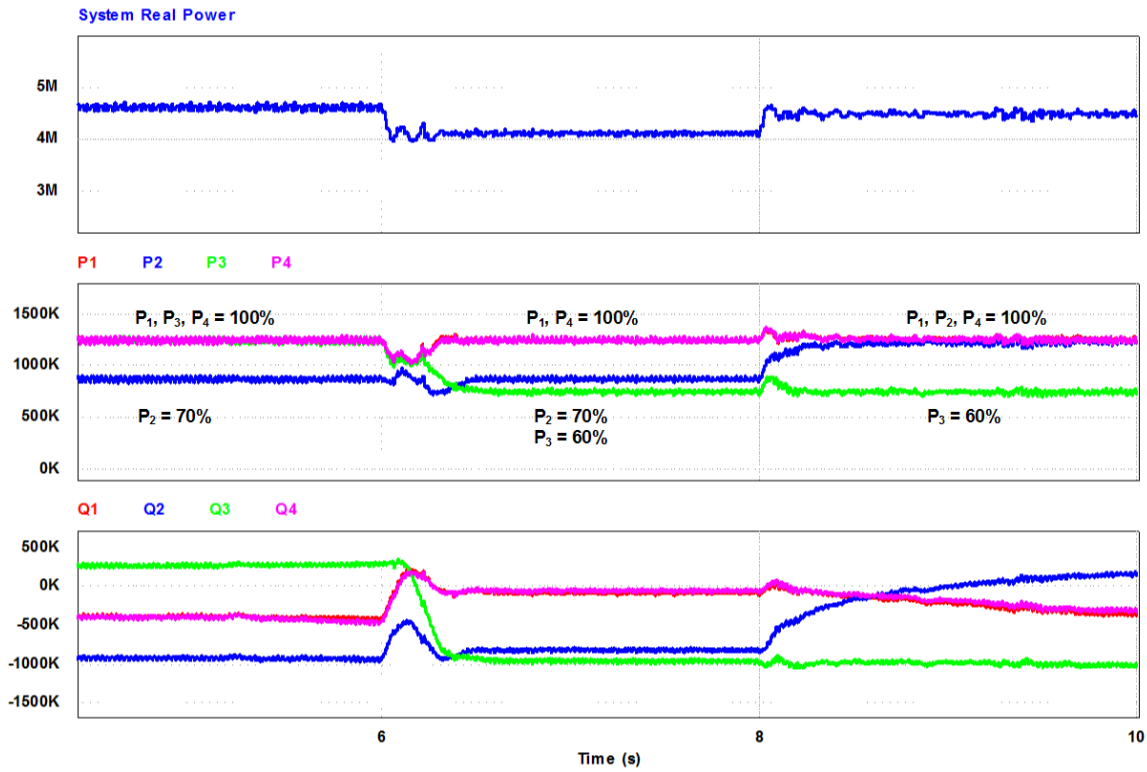

Fig. 3.17: Cascaded inverter controller tracking reference power control input

3.8. Conclusion

In this chapter, the controller for the proposed multilevel PV inverter was introduced. Under uniform insolation the output voltage vectors of the inverter cells are equal in magnitude and phase. However under partial shading conditions the voltage vectors are adjusted to produce the required real and reactive powers. The controller continuously measures the real and reactive powers from each inverter and the voltage vectors are continuously adjusted. It was shown that this method does not require a central controller and makes the system more modular and configurable. The control

algorithm has been shown to be effective in changing the voltage vectors to process the available powers.

4. UTILITY SCALE BATTERY ENERGY STORAGE SYSTEM FOR MULTILEVEL AC LINK PV INVERTER

4.1. Introduction

Modern electric power grids operate by accurately forecasting the load demand for numerous time intervals at least 24 hours ahead of time, called day-ahead forecasting. This prediction is then used to create a generation schedule for conventional and renewable energy power stations; and the load demand is met by dispatching the generated power to load centers. Accurate forecasting is critical to the operation of a power grid since large imbalances between generation and load leads to increased penalty costs [53]. With increased installation capacity of renewable energy sources such as solar thermal, photovoltaic, and wind power systems, there is increased research interest in accurate forecasting of these resources which are intermittent in nature [53-55]. This intermittency needs to be mitigated by other generating stations, failing which the grid could become unstable. Since renewable power plants based on power electronic converters have faster transient performance than conventional prime mover - synchronous generator based stations, any reduction in real power (say ΔP) may be better compensated by using power electronics - energy storage systems rated for ΔP and the power output of the PV plant could be smoothened. With this view, energy storage mandates have been proposed in terms of watts and not watt-hours [56] and grid-supporting energy storage devices are a topic of interest to many researchers [25, 57-59].

These mandates do not require a minimum amount of energy storage, which gives designers the flexibility to optimize performance and cost.

This chapter proposes a utility scale battery energy storage system (BESS) for PV plants to provide real and reactive power grid support during intermittencies in PV insolation. The battery system and associated power electronics are not rated at the same power levels as the PV station, but to compensate for up to 10% reduction in real power from the PV modules, for the duration of 30 minutes. The analysis of BESS power rating is given in the following section. The system uses a three-level bidirectional DC-DC converter to charge and discharge the batteries. The basic operation of the system, design, simulation and experimental results are discussed in this chapter.

4.2. Battery Energy Storage System – Analysis of System Rating

Battery energy storage systems for intermittency mitigation and capacity firming are sized in terms of power; and the energy storage capacity is chosen by the designers considering factors such as price of battery system, expected intermittency patterns, etc., [60]. PV forecast analysis predicts the real power availability from the PV system ahead of time. Any deviation in power generation from this forecast could result in grid-side power fluctuations and ought to be compensated for, by the battery system [61]. For analysis purposes, the recorded insolation data for Boulder, Colorado is sourced from [62]. It is assumed that accurate prediction data for insolation is available, averaged over 15-minute time intervals; intermittencies and variations within a 15-minute period are to be mitigated to provide a smoother plant output [63, 64]. Insolation data for a representative day (May 17, 2013) and 15-minute averages (assumed to be the forecast

values) are given in fig. 4.1. The average predicted values are to be produced by the PV plant, at the specified time of the day. The curve is time shifted since it begins at midnight, UTC.

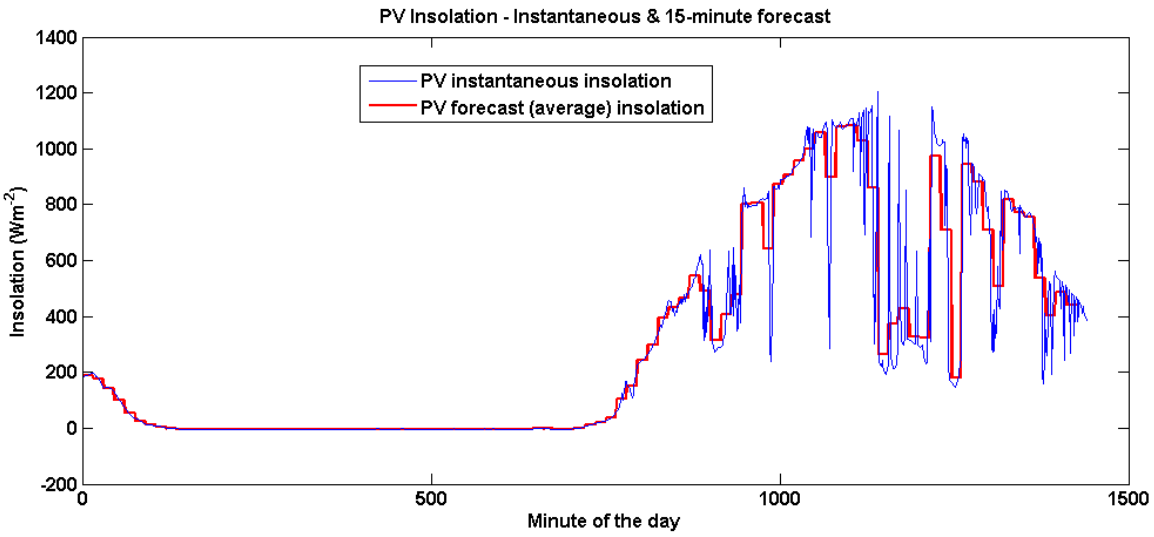

Fig. 4.1: Instantaneous and 15-minute average (forecast) PV insolation data for Boulder, CO on May 17, 2013

As fig. 4.1 shows, deviations in PV insolation from the average forecasted values will result in PV output power fluctuations. In the scenario described in fig. 4.1, the error between output power and previously forecasted power is shown in fig. 4.2.

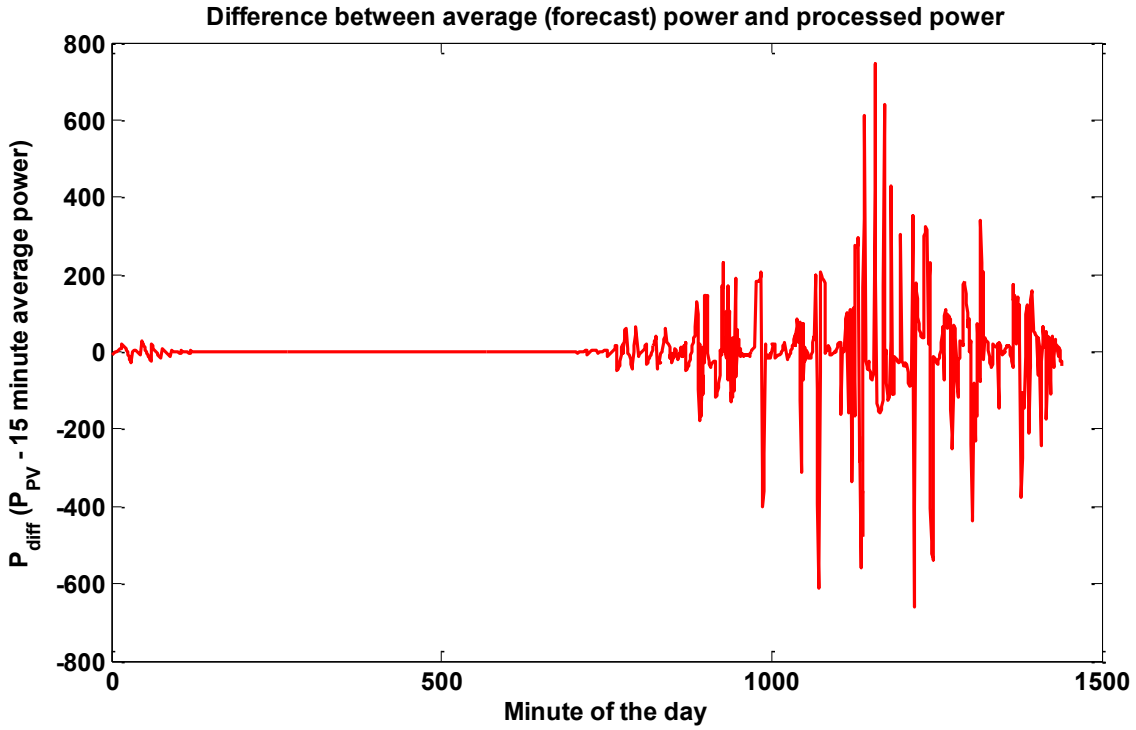

Fig. 4.2: Variations in PV insolation leads to deviation of processed power from average (forecast) power

The error data, when processed again with a BESS rated at 10% of plant power rating, the fluctuation in processed real power decreases. Any excess power from PV above the forecast power (up to 10% of plant power rating) is used to charge the battery system and any deficiency (up to 10%) is filled in by power from the battery system. This reduces the intermittency in output power of the plant, as seen in fig. 4.3 and the difference in power (between forecast and produced) decreases with a 10% battery storage system, as seen in fig. 4.4. The absolute value of the error, averaged over a day, reduces from 38 Wm^{-2} to 11 Wm^{-2}.

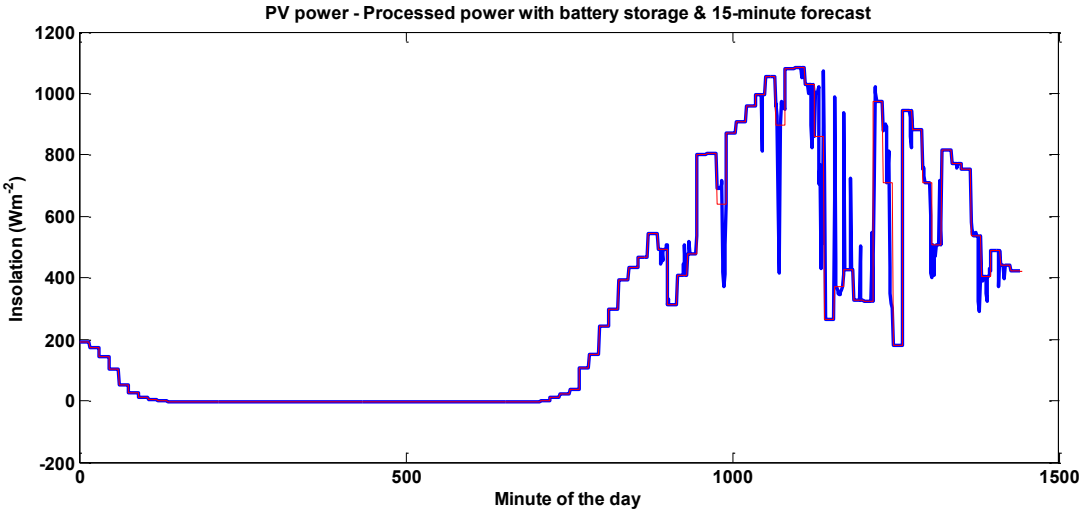

Fig. 4.3: PV processed power with battery storage (blue curve) compared to 15-minute forecast power (red curve)

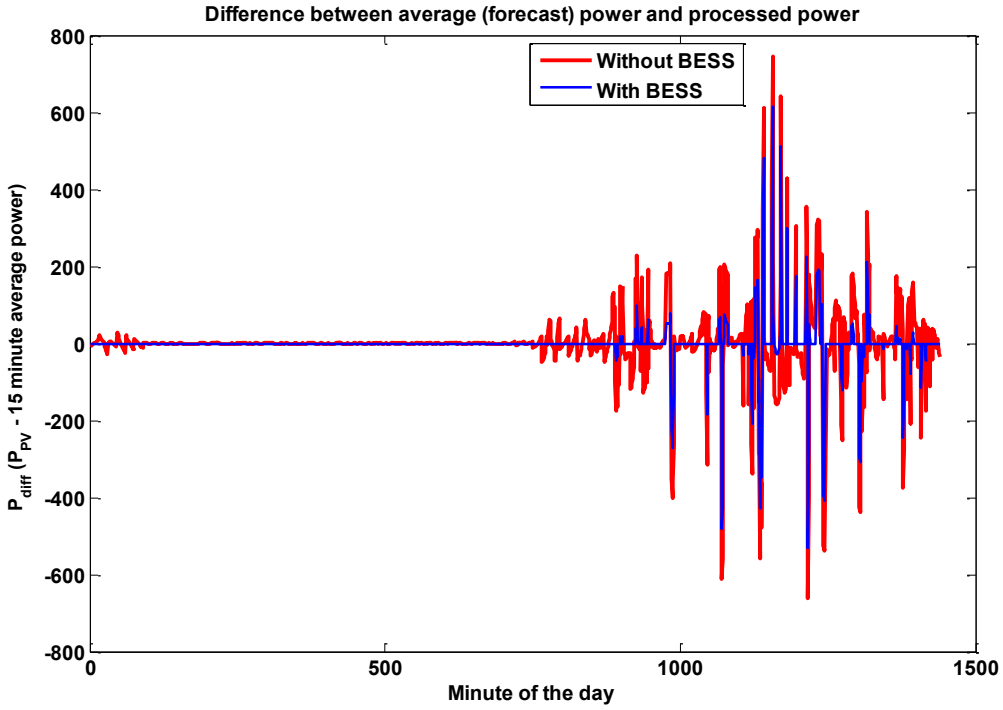

Fig. 4.4: Comparison of error between forecast power and processed power, without BESS and with BESS rated 10%

This analysis is repeated for four representative days from different seasons and also for various BESS power ratings ranging between 0% and 100%. It can be seen that as the power rating of the BESS is increased, the error between forecast power and the processed plant power decreases rapidly as seen from fig. 4.5. From table 4.1 it may be seen that the error approaches zero in all cases, as the BESS rating is increased. It is noted that the BESS power rating requirement is dependent on the PV insolation profile for the specific geographical location, local weather pattern, and the time of the year.

Table 4.1: Error between PV Forecast Power and Processed Real Power for Various BESS Ratings

BESS Power Rating (% of PV plant rating)	Deviation in processed power from forecast power (absolute value) in Wm^{-2}			
	Oct 31, 2013 (Day 304)	Aug 16, 2012 (Day 228)	May 13, 2013 (Day 136)	Jan 02, 2012 (Day 2)
0%	15.4	36.05	37.48	5.4
5%	6.29	19.14	19.54	0.05
10%	3.16	9.96	11.59	0
20%	0.67	1.13	4.62	0
30%	0.01	0	1.71	0
40%	0	0	0.54	0
50%	0	0	0.07	0
60%	0	0	0	0

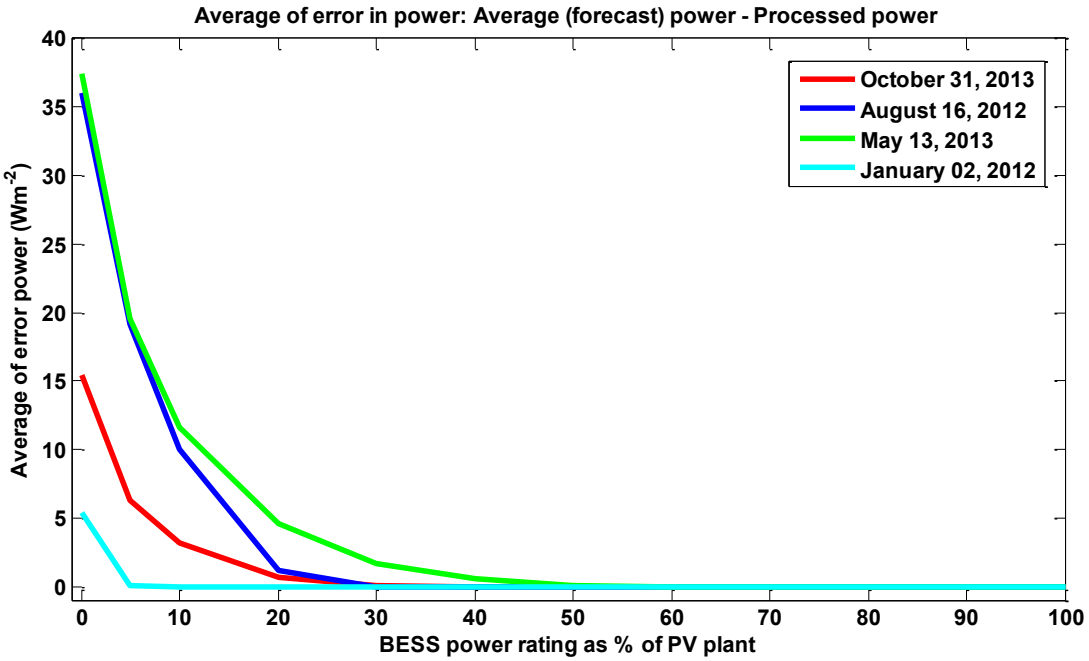

Fig. 4.5: Day-average of deviation in processed power from forecast power, as a function of BESS power rating

4.3. Proposed Battery Energy Storage System Architecture

Utility scale battery energy storage systems have been explored for various applications in [26-28, 65]. These systems propose a centralized approach to BESS. The proposed BESS consists of the multilevel PV AC link converter discussed in chapter 2, with the addition of a distributed bidirectional DC-DC converter and batteries, as shown in fig. 4.6. The battery system is midpoint grounded similar to the PV system itself, reducing the battery bus voltage. The output of the bidirectional converter is connected in parallel to the DC bus of PV high frequency inverter. Fig. 4.7 shows a more detailed view of the bidirectional converter which operates in buck mode while charging and

three-level boost mode while discharging the battery system. This may be reversed, depending on the DC bus voltage and battery design.

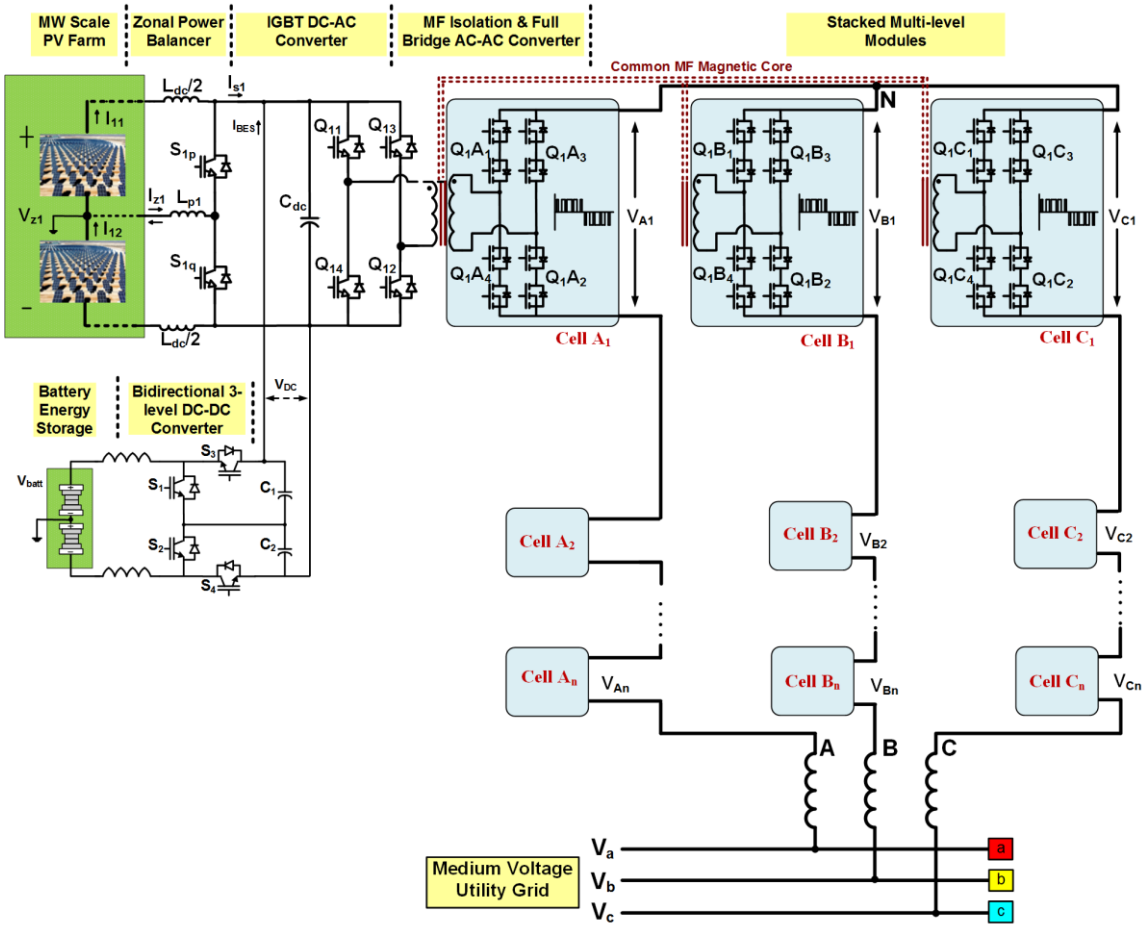

Fig. 4.6: Overall system diagram of battery energy storage system for utility scale PV plant

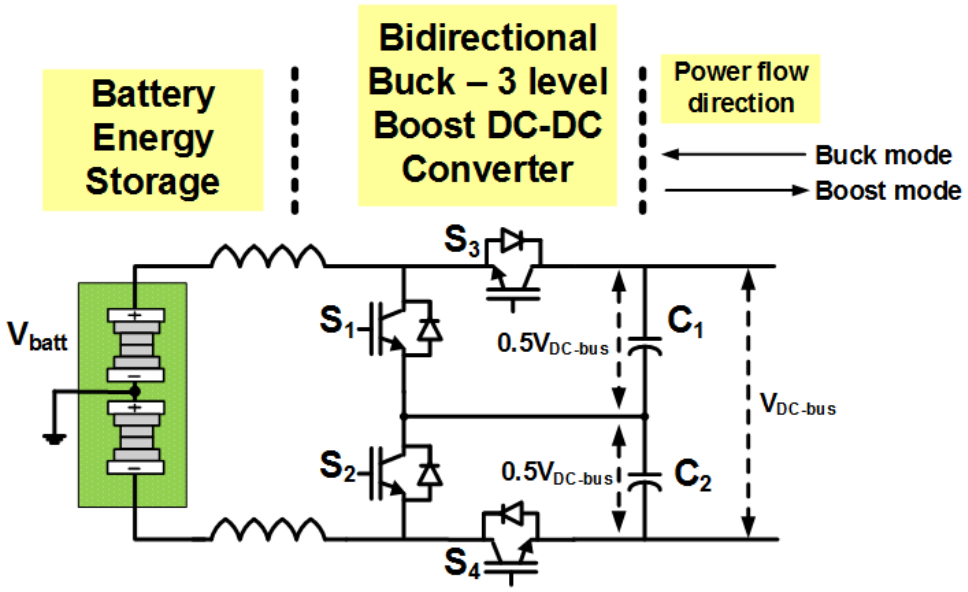

Fig. 4.7: Bidirectional DC-DC converter operating in buck mode for battery charging and 3-level boost mode for battery discharging

In the charging mode, devices S_3 and S_4 are applied the same switching function, to regulate the charging current of the battery. During battery discharge, S_1 and S_2 are operated in 3-level boost converter mode and the antiparallel diodes of S_3 and S_4 provide a path for the output current. These operating modes will be discussed in detail in the later sections.

4.3.1. Battery System

In order to design the battery for the PV-BESS system, various battery chemistries are available to the designer. The requirements for a utility BESS are high power / energy density, charge-discharge cycles rating, high reliability, low cost and good transient response [66-69]. Table 4.2 provides a comparison of common battery

chemistries. It can be seen that for utility BESS applications the sodium battery technology is the most appropriate since it has high energy density and large cycle rating, making it cost effective. It has also been shown to have excellent transient response [70]. However NaS batteries require a high operating temperature of 350 °C.

In the proposed system the battery open circuit voltage is designed to be smaller than the DC bus voltage. This means that the bidirectional DC-DC converter operates in boost mode for discharging and buck mode for charging. Such a design reduces the battery current ripple without requiring large passive filters. The battery system is designed to be discharged up to 60% DoD (depth of discharge).

Table 4.2: Comparison of Battery Chemistries

	Lead Acid	Sodium (NaS) Battery	Flow Battery (V Redox)	NiMH	Li-ion
Energy density (W.h/kg)	35	400	25	135	200
Charge-Discharge cycles	1000, 30% DoD	4500, 90% DoD	2000	2000	3000, 80% DoD
Cost ($/kWh)	200	400	400	350	1000
Self-discharge	5% /month	No	No	30% /month	7% /month
Memory effect	No	No	No	Little	No

4.3.2. Bidirectional DC-DC Converter: Charging Mode Operation

The bidirectional converter operates as a buck converter while charging the battery. Fig. 4.8 illustrates the operation of the buck converter. The voltage gain of the converter is given by $\frac{V_{batt}}{V_{dc-Bus}} = D$, where D is the duty cycle of devices S_3 and S_4. A small filter capacitor is connected to the battery to reduce high frequency ripple. The control policy of the buck converter regulates the average inductor current, ensuring it is below the maximum charge rate of the battery system. The real power available from the photovoltaic arrays is calculated by the MPPT controller. When the available real power is more than the power dispatched to the grid, a control input of reference power is applied to the buck converter, which regulates IGBTs S_3 and S_4 such that the excess available power is used to charge the battery. The current reference is continuously adjusted by the controller by sensing the open circuit voltage (OCV) of the battery. Estimating the battery state of charge (SoC) by sensing OCV is a widely researched topic [71, 72] beyond the scope of this work. As the OCV of the battery increases the current reference is decreased linearly and it is always maintained below the maximum charge rate of the battery, irrespective of battery OCV.

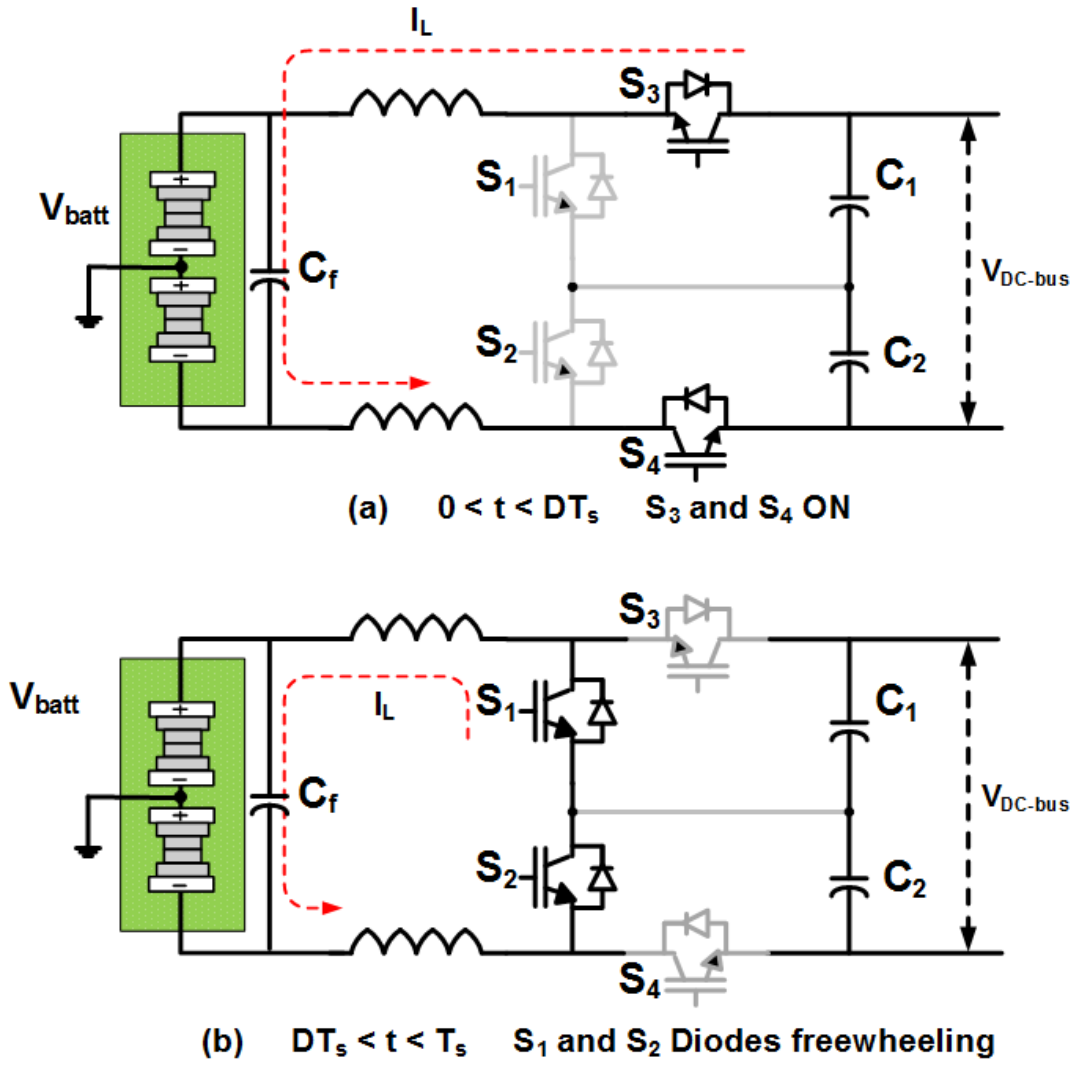

Fig. 4.8: (a) Switches S_3 and S_4 are ON for DT_s and the inductor current ramps up, supplying current to the battery (b) Switches are turned OFF and the inductor current freewheels through the antiparallel diodes of switches S_1 and S_2

Fig. 4.9 shows the logic of the DC-DC converter controller for the battery charging operation.

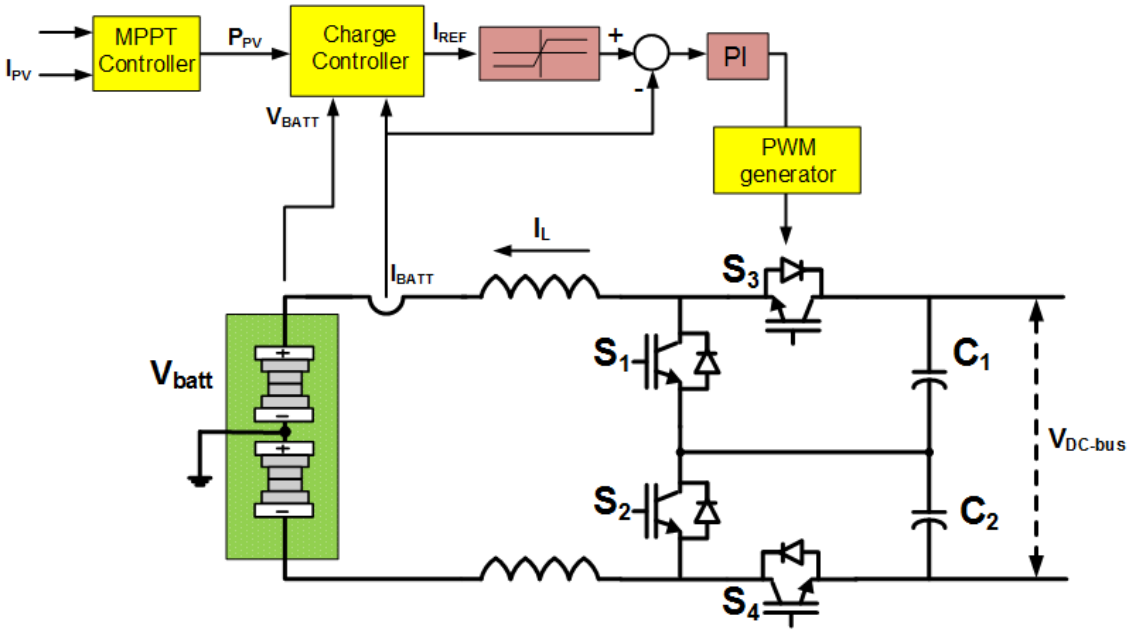

Fig. 4.9: Controller for DC-DC converter buck operation during charging mode of the bidirectional converter. The current reference generator senses the open circuit voltage of the battery

4.3.3. Bidirectional DC-DC Converter: Discharging Mode Operation

The bidirectional converter operates as a 3-level boost converter during the battery discharge periods. The circuit diagram of a 3-level boost DC-DC converter is given in fig. 4.10 [73, 74]. The voltage transformation ratio is given by the boost converter voltage gain expression $\frac{V_{DC}}{V_{FCS}} = \frac{1}{(1-D)}$, where D is the duty cycle of the IGBTs S_1 and S_2. The 3-level DC-DC converter has two modes of operation. When the input voltage of the converter is less than 50% of the output voltage, the converter operates in mode 1 and when the input voltage is greater than 50% of the output voltage, it operates

in mode 2. The switching functions of S_1 and S_2 are similar but phase shifted by 180°. The two modes of operation are discussed in detail below.

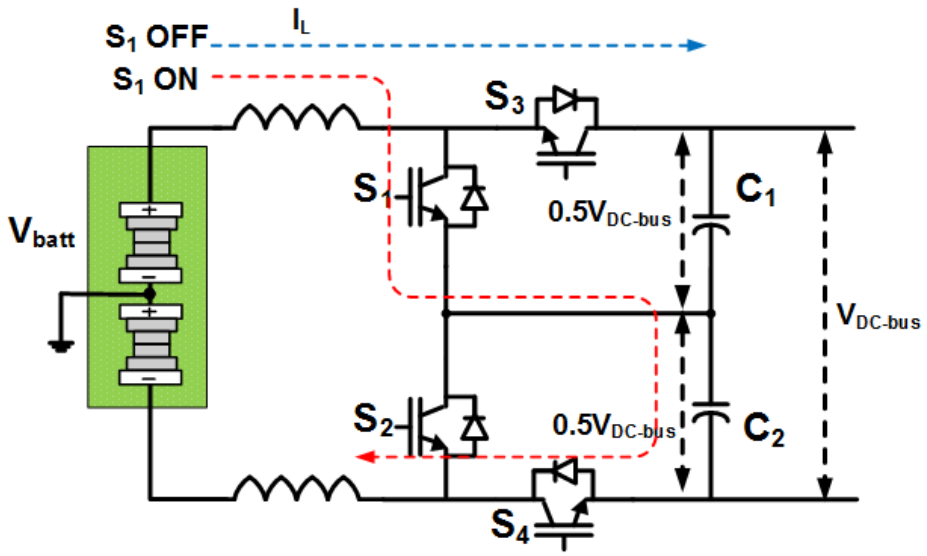

Fig. 4.10: Bidirectional DC-DC Converter in battery discharging mode operating as a 3-level boost converter (illustrated for the case that $V_{batt} > 0.5V_{DC\text{-}bus}$)

Operation Mode 1: V_{Batt} (V_{in}) < 0.5V_o

When the input voltage is less than half of the output voltage, it can be easily seen from the voltage gain expression that the duty cycle is more than 0.5. The waveforms for the switch gating signals and inductor current are given below in fig. 4.11. When both S_1 and S_2 are ON, the full input voltage V_{in} is applied to the inductor, ramping up the inductor current and the load current is supplied by the output capacitors C_1 and C_2. When one of the switches (say S_1, the top switch) is OFF the inductor current supplies the load and also charges the top output capacitor C_1. Similarly, when the

bottom switch S_2 is OFF and the top switch is ON, the bottom capacitor C_2 gets charged. The capacitor charging current profiles and load current are given in the fig. 4.12. The duty cycle of the converter remains above 0.5, as long as the converter input voltage is less than half of the output voltage and the operation remains in mode 1.

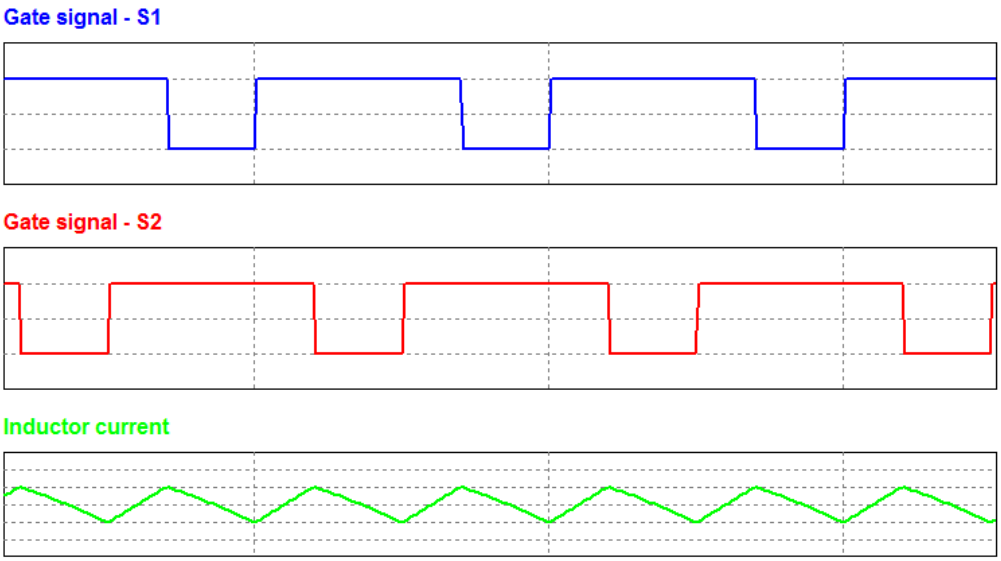

Fig. 4.11: Gating signals for top (S_1) and bottom (S_2) IGBTs in the three level DC-DC converter and the inductor current, operation mode 1 ($V_{Batt} < 0.5V_o$)

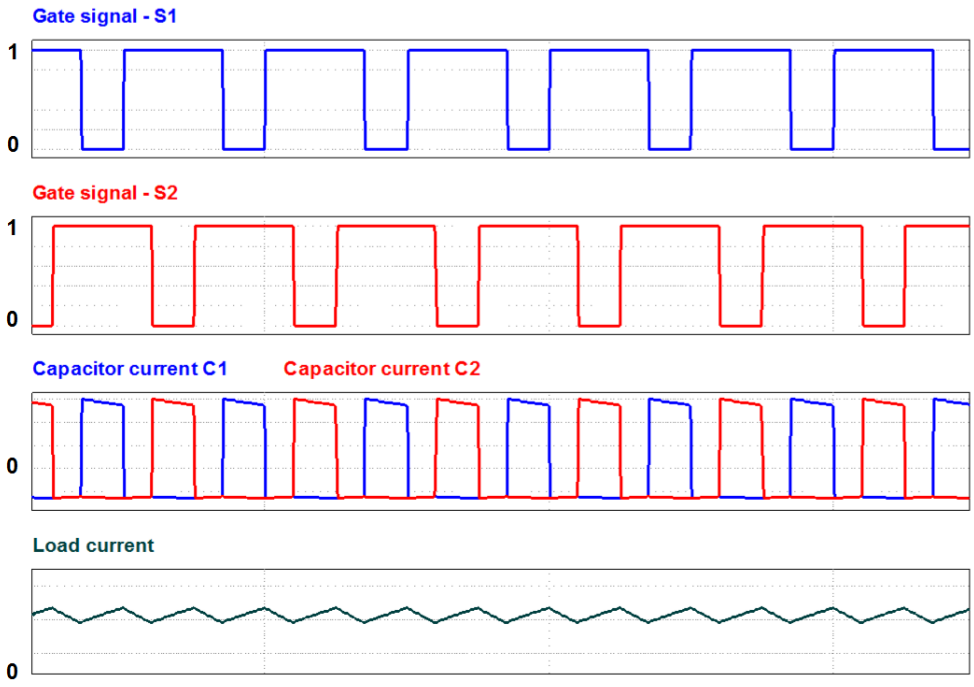

Fig. 4.12: Gating signals for top (S_1) and bottom (S_2) IGBTs, the currents through the top capacitor C_1 and the bottom capacitor C_2 and the load current in the three level DC-DC converter operating in mode 1 ($V_{Batt} < 0.5V_o$)

Operation Mode 2: $V_{Batt} > 0.5V_o$

In this mode of operation, since the input voltage is greater than half of the output voltage, the duty cycle of the converter in this mode is less than 0.5. This means that there are zero states, in which none of the both switches in the converter are ON. The switching patterns of the top and bottom devices are as given in the fig. 4.13. When one of the switches (say, S_1, top device) is ON, V_{in}-$0.5V_o$ is applied to the inductor and the inductor current ramps up, at the same time, charging the bottom capacitor, C_2. During this time the load current is supplied by the top capacitor C_1. Similar operation occurs when the bottom device S_2 is ON. The operating waveforms of the capacitor currents and

the load currents are given in fig. 4.14. The converter operation switches from mode 1 to mode 2 and vice versa, depending on the input voltage, without any action on the part of the controller.

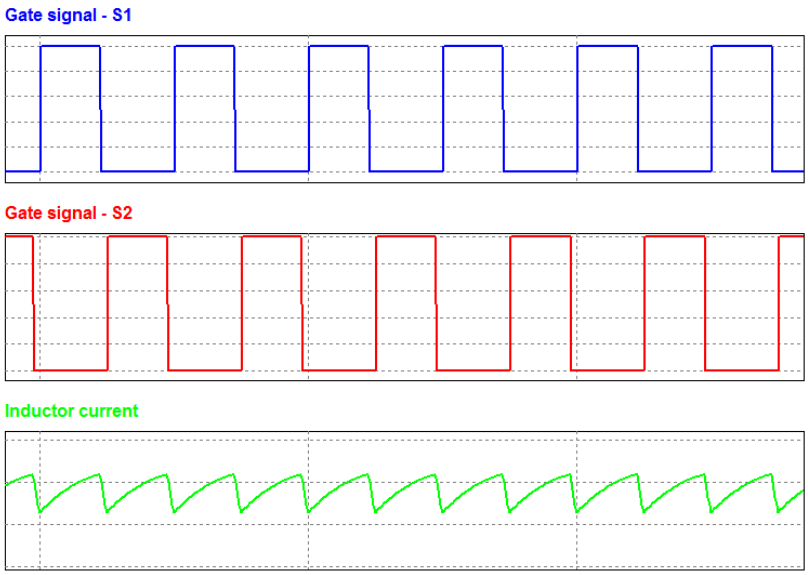

Fig. 4.13: Gating signals for top (S_1) and bottom (S_2) IGBTs in the three level DC-DC converter and the inductor current, operation mode 2 ($V_{Batt} > 0.5V_o$)

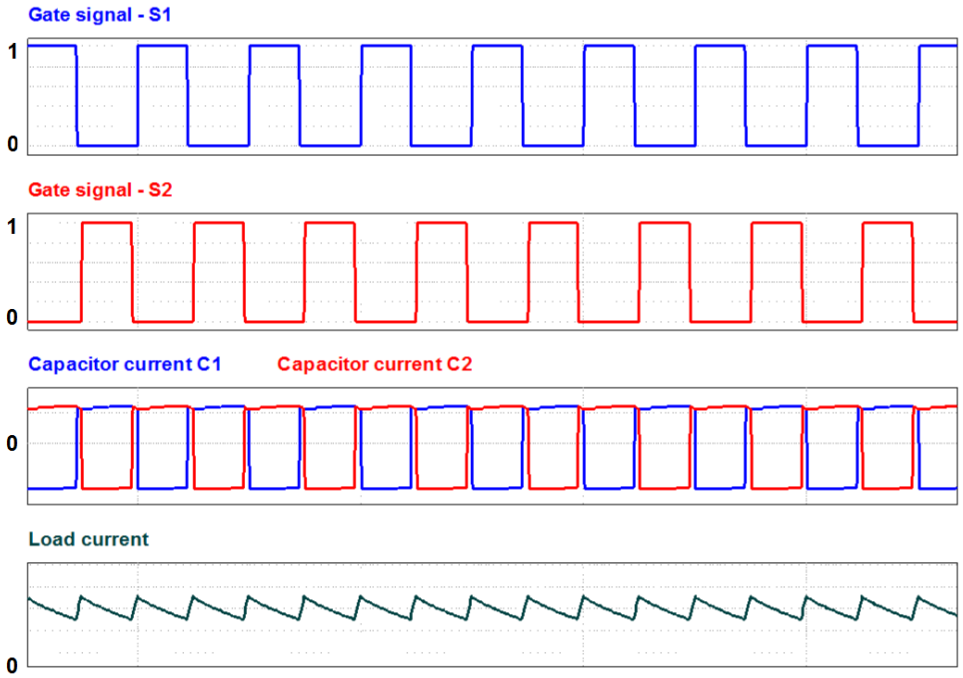

Fig. 4.14: Gating signals for top (S_1) and bottom (S_2) IGBTs, the currents through the top capacitor C_1 and the bottom capacitor C_2 and the load current in the three level DC-DC converter operating in mode 2 ($V_{Batt} > 0.5V_o$)

Closed loop operation of the three level boost converter is similar to the buck converter discussed in fig. 4.9. The battery voltage is continuously monitored to prevent deep-discharge while regulating the inductor current thereby, the average battery current.

4.3.4. DC-DC Converter Modeling

The PWM switch model for the 3-level converter is useful for controller modeling and efficiency estimation purposes and can be derived using the equivalent model in fig. 4.15. This model can estimate the efficiency reduction due to conduction losses; though switching losses have to be evaluated separately.

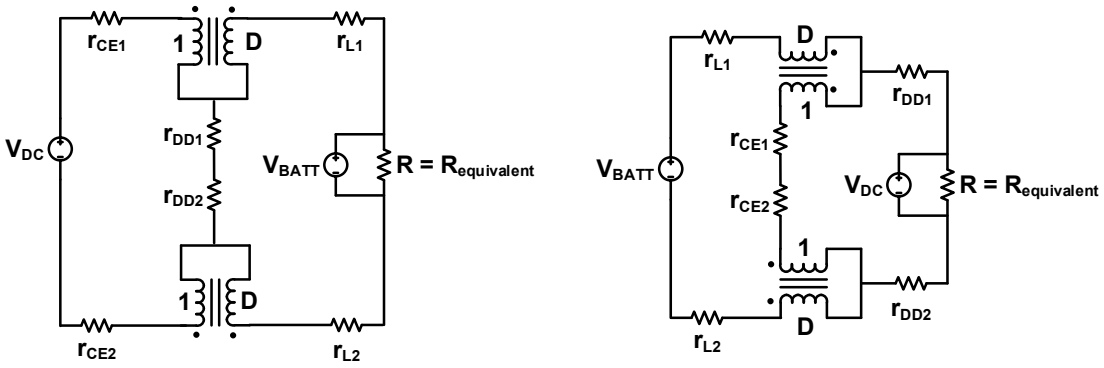

Fig. 4.15: PWM switch model equivalent diagram of (a) Bidirectional converter in charging mode – buck operation (b) Discharging mode – boost operation

The PWM switch models are derived using three port switching cell method described in [75] and [76]. The voltage gains of the bidirectional converter for these non-ideal cases are also determined. Analyzing the circuit in fig. 4.15 (a), the transfer function (voltage gain) of the non-ideal buck converter $\frac{V_{Batt}}{V_{dc}}$ could be evaluated as given in (27).

$$\frac{V_{Batt}}{V_{dc}} = D \cdot \left\{ \frac{1}{1 + \frac{2\left(D \cdot r_{ce} + r_L + r_{DD} \cdot (1 - D)\right)}{R}} \right\} \tag{27}$$

where V_{dc} is the inverter DC bus voltage, V_{Batt} is the battery voltage, D is the operating duty cycle at steady state, r_L is the inductor equivalent series resistance, r_{CE} is the equivalent IGBT on-state resistance and r_{DD} is the equivalent diode on-state resistance. The resistance R is the equivalent load resistance which is a function of the power transferred. The voltage gain expression for the non-ideal boost converter in fig. 4.15 (b) is also derived using the same technique and it is given in (28).

$$\frac{V_{dc}}{V_{Batt}}=\left(\frac{1}{1-D}\right)\cdot\left\{\frac{1}{1+\frac{\left(2r_L+2D\cdot r_{CE}+2\cdot(1-D)\cdot r_{DD}\right)}{R\cdot(1-D)^2}}\right\} \tag{28}$$

The duty cycle-to-output voltage transfer functions are also derived for the bidirectional converter. State-space averaging techniques are used to derive the transfer functions, which are shown in (29) and (30) for the buck and boost operations, respectively.

$$\frac{\hat{v}_{Batt}(s)}{\hat{d}(s)}=V_{dc}\frac{1}{\left(1+s\frac{LC}{R}+s^2LC\right)} \tag{29}$$

$$\frac{\hat{v}_{dc}(s)}{\hat{d}(s)}=\left(\frac{V_{Batt}}{(1-D)^2}\right)\frac{\left(1-s\frac{LI_L}{V_{Batt}}\right)}{\left(1+s\frac{L}{(1-D)^2R}+s^2\frac{LC}{(1-D)^2}\right)} \tag{30}$$

The transfer function (30) shows the presence of the right half zero in the boost converter which plays an important role in developing the closed loop controller.

4.4. Design Example for Utility Scale BESS

A design example for a utility scale BESS integrated PV system rated at 5 MW is discussed in this section. The specifications of the system are given in table 4.3.

Table 4.3: Specifications for Design Example for Utility Scale Bess Integrated PV

PV System & Multilevel Inverter	
Power rating	5 MW
Number of PV Zones, number of cascaded multilevel inverter cells	4
Grid voltage	13.2 kV three phase, 60 Hz
PV characteristics	Mathematically modeled
Isolation transformer frequency f_{sq}	600 Hz
PWM inverter switching frequency f_{sw}	1800 Hz
Battery System & Bidirectional DC-DC Converter	
Battery voltage	630 V at full charge; 590 V at full discharge; 300 NaS cells in series
Battery capacity	62500 kWh / 100 Ah, (212 A for 30 minutes)
Maximum charge rate	$\frac{C}{4}$; 53 A at 590 V OCV
Battery depth of discharge	60%
DC-DC converter rating	125 kW
Bidirectional converter switching frequency f_{dc}	2000 Hz
Inductor design	Critical inductance at 10% current
Capacitor design	10% voltage ripple at full load

The power ratings of the DC-DC converters and the batteries are fixed at 10% of the rating of the PV inverters. The battery, for simulation purposes, is modeled as a large capacitor with equivalent series resistance and inductance. Using the energy capacity rating, depth of discharge and specific energy density rating of the NaS battery, it can be determined that the designed battery will have a weight of 250 kg.

4.5. DC-DC Bidirectional Converter Design and Efficiency Analysis

4.5.1. Inductor Design

From table 4.3, the inductor is to be designed for a maximum rms current rating of 200 A. The inductor design is done for critical conduction operation at 25 A. Since maximum charge rate of the battery is 53 A and the charge rate is dependent on OCV, charging operation (buck converter) happens both in continuous and discontinuous conduction modes. The inductor value required is calculated in (31) and (32). At 25 A charging current, the battery voltage is 612 V.

$$L\frac{dI}{dt} = V_{Batt} = 612 \tag{31}$$

$$L\frac{2\Delta I_L \cdot f_{sw}}{D} = L\frac{50 \times 2000}{0.5} = 612 \tag{32}$$

The calculated inductance is 3.06 mH.

4.5.2. Capacitor Design

The capacitor is designed to provide 10% output voltage ripple at full load. The load current a full load is 104 A and the PV DC bus voltage is 1.2 kV. This leads to the design equations (33) and (34).

$$C\frac{dV}{dt} = I_{load} = 104 \tag{33}$$

$$C\frac{0.1 \times V_{dc} \times f_{sw}}{D} = C\frac{0.1 \times 1200 \times 2000}{0.5} = 104 \tag{34}$$

The calculated capacitor value is 217 μF. Since two capacitors are connected in series at the output, the value becomes 434 μF. Two capacitors of 500 μF are used in the design.

4.5.3. Device Ratings

The IGBTs in the bidirectional converter are rated to block the DC bus voltage, 1.2 kV. During the charging operation (buck converter) when IGBTs S_3 and S_4 are on the other two devices S_1 and S_2 would need to block 1.2 kV collectively. During discharging operation (boost converter) when S_1 and S_2 are on the DC bus voltage is to be forward-blocked by S_3 and S_4. So the IGBTs are rated to block 1.2 kV individually, derating the devices 50%. The devices would also need to have a current rating of 300 A. One identified candidate device is the Microsemi APTGT200DA120D3G [77].

4.5.4. Loss Estimation and Efficiency Analysis

Using manufacturers' datasheets for the IGBTs, the switching loss can be estimated at 125 kW operating power level. The switching loss characteristics show the per-cycle switching loss to be 57 mJ/cycle for one IGBT and reverse recovery losses of 20 mJ/cycle for one diode. At a switching frequency of 2 kHz, this corresponds to a switching power loss of 310 W. The conduction power loss can be readily calculated using a duty cycle of 0.5 and the published forward drop voltages of semiconductor devices and the estimated losses are 680 W. Assuming that the passive components contribute to a further 2% losses, the full load efficiency of the DC-DC stage is estimated to be 97%. The switching frequency of the converter may be changed to improve the efficiency, but the size of passive components will have to be increased to ensure satisfactory voltage and current ripple performance.

4.6. Simulation Results

The battery energy storage system designed for 5 MW is simulated and the results are discussed in this section. The converter produces a line-line voltage of 6.6 kV as seen in fig. 4.16. The line currents are also shown, which exhibit low distortion with a THD of 3%.

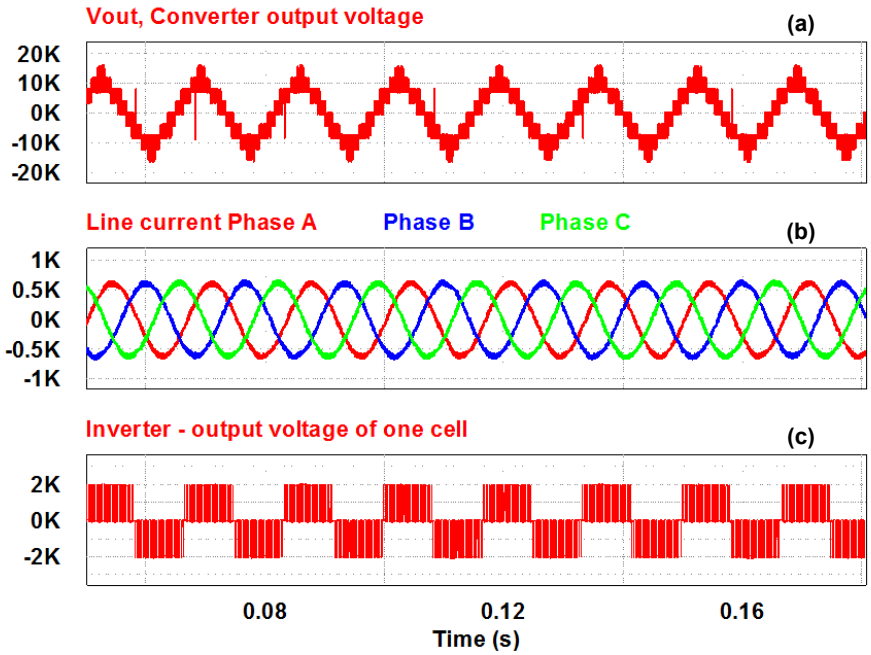

Fig. 4.16: (a) Line-line converter output voltage of multilevel inverter producing 6.6 kV, (b) line currents in the three phase system, and (c) the output voltage of one cell showing unipolar operation

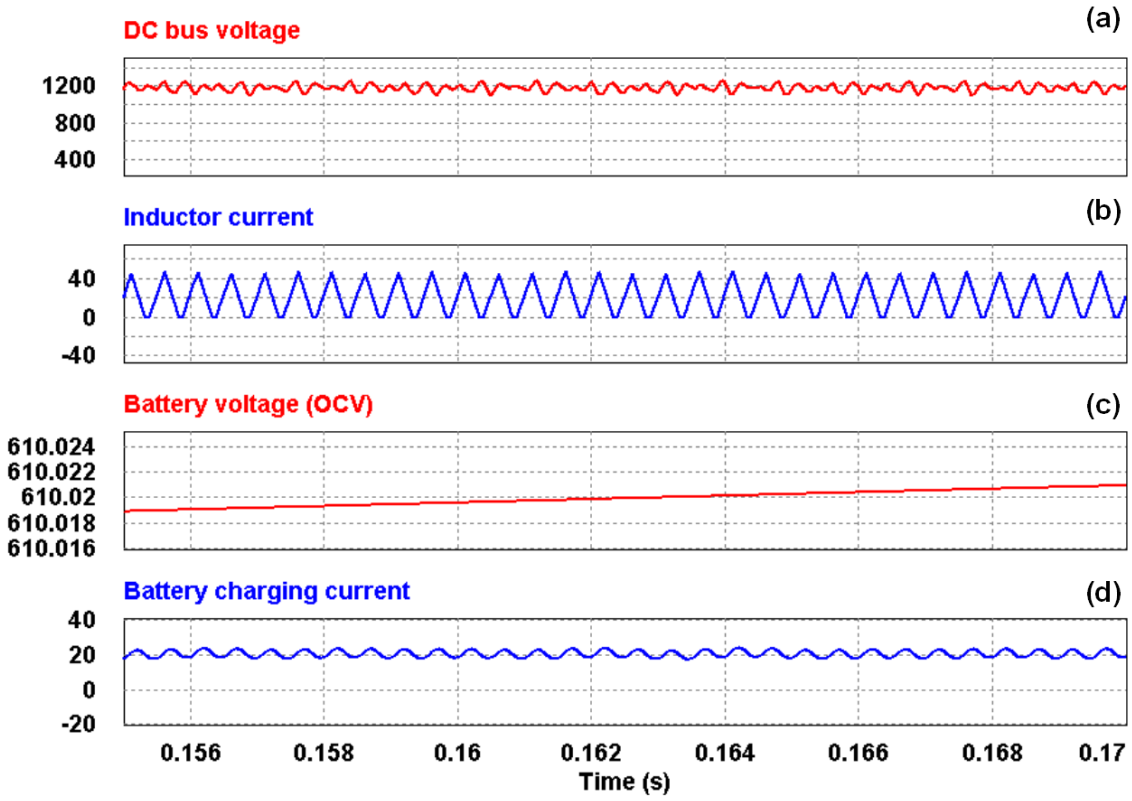

Fig. 4.17: (a) The DC bus voltage in a Utility BESS (b) DC-DC converter inductor current showing discontinuous conduction (c) battery system open circuit voltage (d) Battery charging current

The operation of the BESS in charging mode is shown in fig. 4.17. The bidirectional converter operates in buck mode processing 12 kW. The converter operates in discontinuous conduction mode as seen from the inductor current waveform with an average value of 20 A. The increase in battery OCV due to charging can be seen. In order to demonstrate the increase in battery OCV the equivalent capacitance in the battery model is deliberately reduced to a value smaller than the real value. The battery charging current is also shown in fig. 4.17. High values of ripple current through the

battery increase the cell temperature and reduce lifetime. There is a tradeoff between the permissible ripple current through the battery and the size of the passive components.

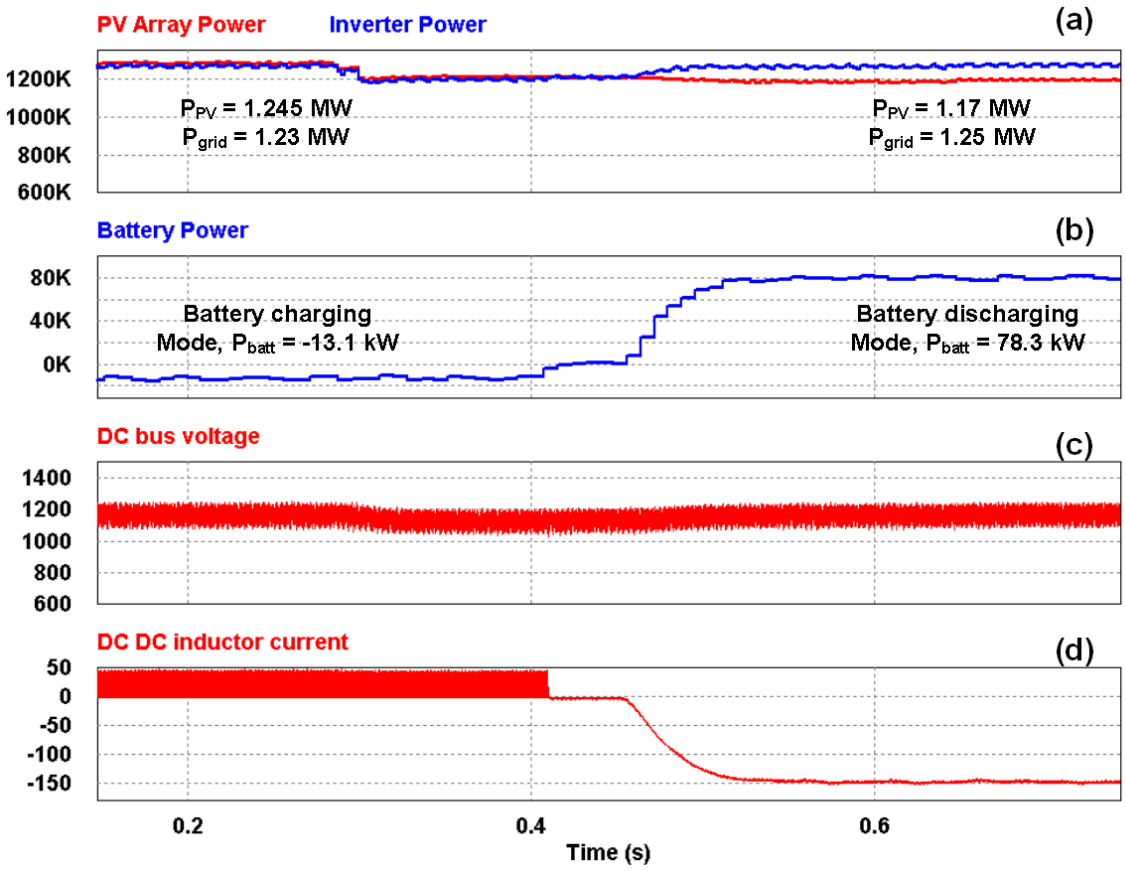

Fig. 4.18: Measured average power from (a) the photovoltaic modules and the overall output power, (b) power processed by the battery, (c) DC bus voltage regulated with minor reduction during loss of PV (d) the DC-DC inductor current during charge and discharge mode operations

When the DC power available from the PV modules suffers a reduction of about 7%, as seen in fig. 4.18, the DC-DC converter switches from charging operation (buck) to discharging (3-level boost) operation. Fig. 4.18 shows that until the reduction in PV

power, 13 kW of available power was used to charge the battery and the remaining power was being fed to the output of the inverter, i.e. grid. The reduction in power is sensed from the DC bus voltage and the inductor current ramps up in the opposite direction. The power being fed into the grid is now the sum of all available power from PV modules and the power being supplied by the battery system.

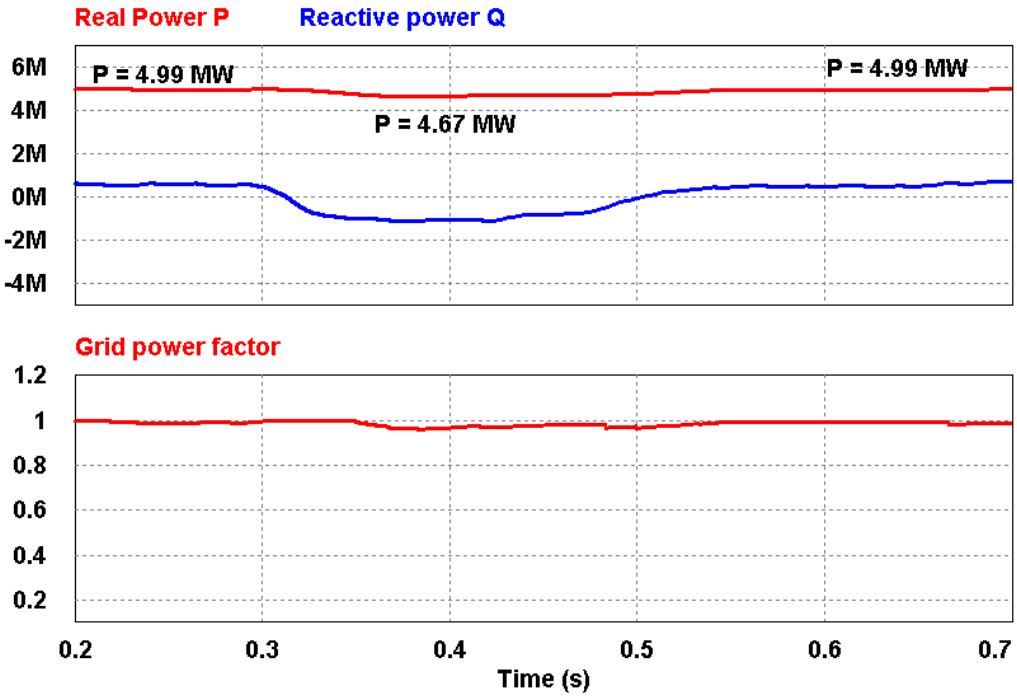

Fig. 4.19: The real and reactive powers fed into the grid by the utility scale PV – BESS and the grid power factor

The real and reactive power transfers by the utility scale PV – BESS are shown in fig. 4.19 along with the grid power factor. Until the reduction in PV power input, the system supplies both real and reactive powers to the grid. When PV power is reduced,

reactive power is consumed from the grid to supply the DC bus capacitor, without which the DC bus voltage would collapse. Upon the commencement of battery discharge operation, the DC bus capacitor is supplied by both PV and battery systems, reducing the reactive power consumption and ultimately starting to supply reactive power to the grid. From fig. 4.19 it may also be noted that the grid power factor is maintained close to unity, above the required 0.95 value.

4.7. Experimental Results

An experimental prototype BESS rated 200 W was built using a 48 V battery bank, seen in fig. 4.20 and the operation of bi-directional DC-DC buck – 3-level boost converter was verified.

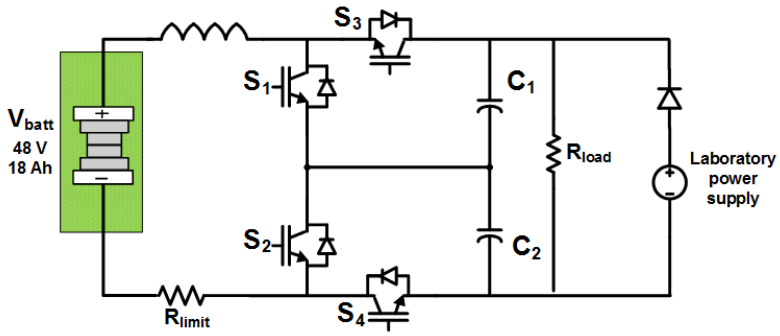

Fig. 4.20: Experimental setup for 48 V BESS with bidirectional converter

The battery bank was constructed using commercially available lead acid batteries to produce an open circuit voltage of 48 V. The bidirectional converter is then operated at a switching frequency of 2 kHz in 3-level boost mode (switches S_1 and S_2) to discharge the battery. A resistor bank acts as the power sink. The value of DC-DC

inductor is 3 mH. In the discharging mode the battery voltage is boosted to 80 V, producing 200 W of power and the discharging current is $\frac{C}{4}$. The device voltages and battery current in this operational mode are shown in fig. 4.21. It may be seen that the device voltage stresses ought to be made equal by balancing the capacitor voltages.

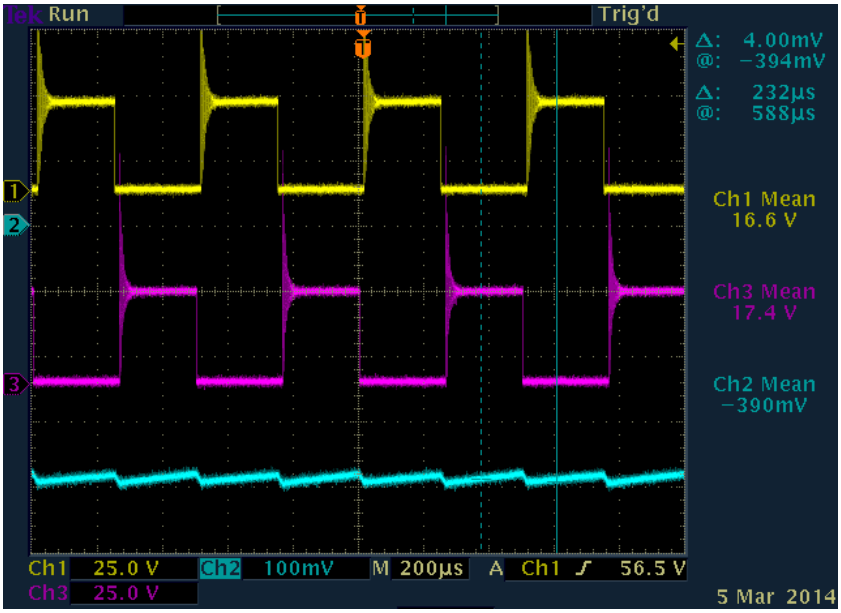

Fig. 4.21: Discharging operation (3-level boost) device voltages (S_1 – Ch 1, S_2 – Ch 3) and battery current (Ch 2) for 200 W operation

The bidirectional converter is also operated in the charging mode, which is a buck converter, with devices S_3 and S_4 having the same switching function. The antiparallel diodes in S_1 and S_2 provide freewheeling path for the inductor current. The device voltages, as seen in fig. 4.22 have identical switching functions. The charging current in this case is 110 mA.

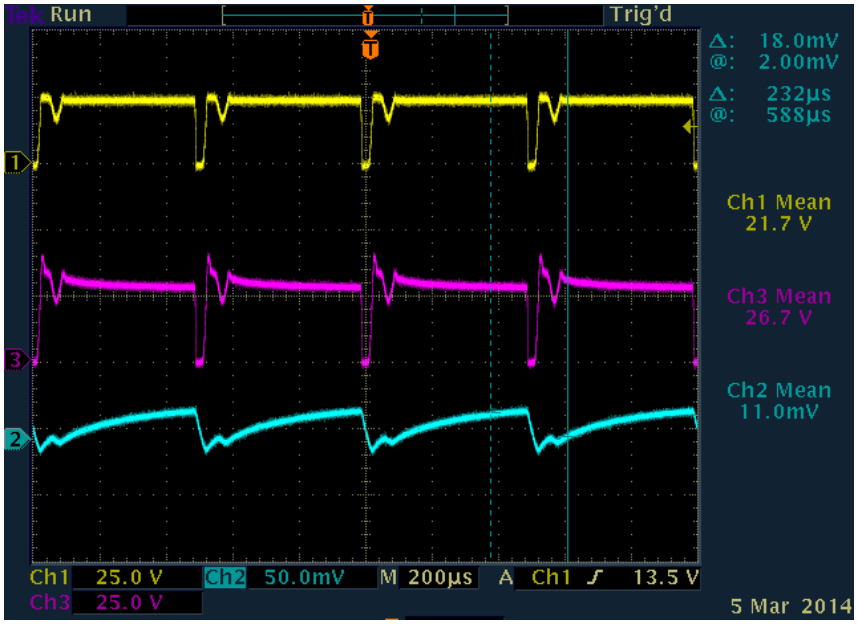

Fig. 4.22: Charging operation (buck) device voltages S_3 (Ch 1) and S_4 (Ch 3), and battery charging current (Ch 2)

The operation of the converter is also verified for transition between charging and discharging modes of operation. It may be seen from fig 4.23 and 4.24 that the bidirectional converter is capable of fast transient performance which is critical in the proposed BESS system. The battery voltage (yellow trace) is also shown which, on transition from discharging at 3.5 A to charging at 150 mA, exhibits a subtle increase.

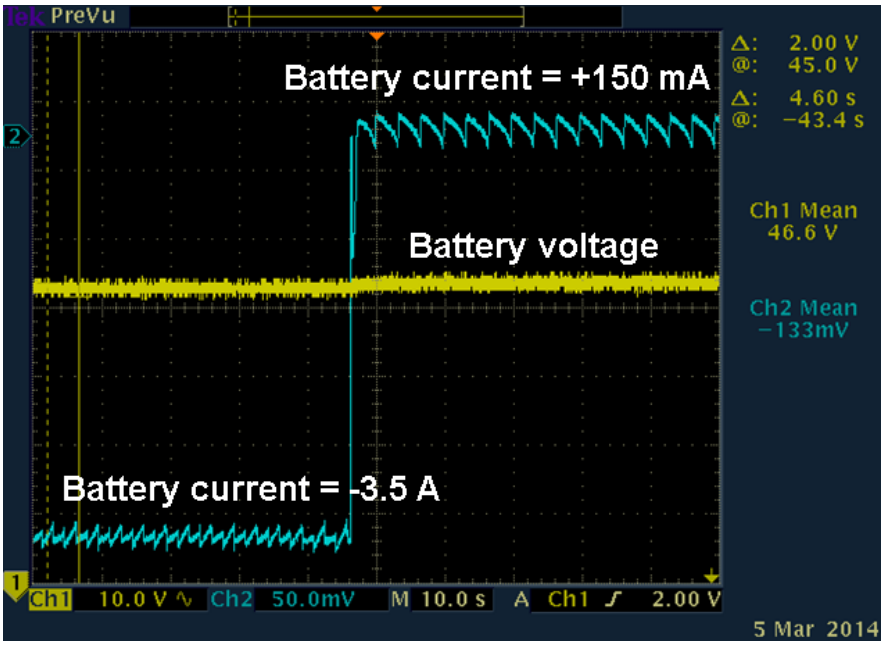

Fig. 4.23: Transient performance from discharging operation (boost) to charging operation (buck): Battery voltage (Ch 1) and battery current (Ch 2)

4.8. Summary and Conclusion

This chapter discussed a utility scale battery energy storage system for a photovoltaic power plant. The BESS uses a bidirectional DC-DC converter to interface the battery system with the DC bus capacitor of a PV array. The battery system suitable for such an application is the sodium sulphur (NaS) battery for its high specific energy and low cost, compared to other chemistries. The bidirectional converter operates as a buck converter while charging the battery and as a 3-level boost converter during the discharging of the battery. The converter and battery are rated at 10% power rating of the PV array. A design example rated at 5 MW consisting of four cascaded inverters was shown and simulation results were discussed. When the PV array loses power the battery

is discharged appropriately to compensate for the loss. This proposed approach remedies certain issues faced by PV power such as intermittency and improves stability of the grid over short periods of time, in the order of seconds or minutes.

5. ANALYSIS AND MITIGATION OF COMMON MODE VOLTAGES IN PHOTOVOLTAIC POWER SYSTEMS*

5.1. Introduction

In this chapter, the analyses of common mode voltages and currents in the afore-mentioned PV topologies are detailed [78]. The grid integration of PV power employs a combination of PWM DC-DC converters and inverters. Due to their fast switching nature a common mode voltage is generated with respect to the ground, inducing a circulating current through the ground capacitance. Common mode voltages lead to increased voltage stress, electromagnetic interference and malfunctioning of ground fault protection systems.

5.2. Common Mode Capacitances in Photovoltaic Systems

In a typical photovoltaic generation system, the PV module frames are grounded for safety. The planar structure of the cells and module glass results in capacitance to ground, which could be, depending on conditions such as weather and dust, as high as 150 nF/kW [79]. Power converters operating at high switching frequencies produce common mode voltages at the output in addition to the differential mode voltage. The high frequency transitions in the common mode voltage induce currents in the capacitances to ground. The occurrence of common mode currents and voltages introduce a number of problems including:

* This chapter is adapted from [78] S. Essakiappan, P. Enjeti, R. S. Balog, and S. Ahmed, "Analysis and mitigation of common mode voltages in photovoltaic power systems," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2011, pp. 28-35.
 Digital Object Identifier: 10.1109/ECCE.2011.6063745

- Common mode voltages increase the voltage stress on the lines and switches potentially leading to reduction in lifetime.
- High amplitudes of common mode current through the ground circuit pose an operational electrical hazard and also contribute to electro-magnetic interference (EMI) [80].
- Common mode currents increase the chance of malfunctioning of ground fault protection systems resulting in nuisance tripping [81].

Thus it is important to minimize the effects of common mode voltages and currents in PV power generation systems. This chapter analyzes common mode voltages in the PV topologies discussed above and proposes solutions such as common mode filter and high frequency transformer shielding.

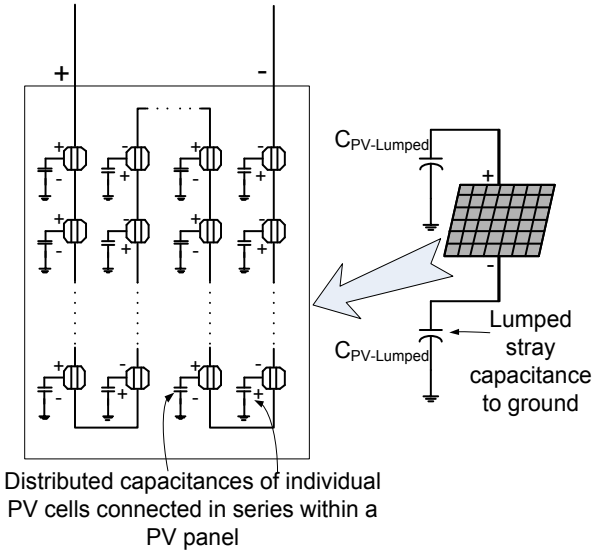

Fig. 5.1: Distributed and lumped capacitance models of a single PV module comprised of a plurality of series and parallel-connected cells

5.3. Distributed Ground Capacitances in a Photovoltaic Power System

In a typical PV system comprised of metal-framed PV modules, each PV module frame is bonded to earth ground. This introduces distributed stray capacitances between the photovoltaic cells and the ground-plane of the PV module. The distributed capacitances throughout the module are characterized by an equivalent lumped capacitance $C_{PV\text{-}Lumped}$ for this analysis, as shown in fig. 5.1.

In order to study the distributed, module-to-ground capacitances in a practical PV system, an equivalent capacitance model is developed. fig. 5.2 shows a 2.76 kW-per string rooftop system at Texas A&M University, College Station, Texas. The overall system contains ten strings with a total capacity of 27.6 kW. Each string is comprised of 12 series connected 230 W modules manufactured by Sharp (Model: ND230UCJ). As fig. 5.2 illustrates, the ground conductor is electrically bonded to the frame of every module. In order to derive the equivalent circuit shown in fig. 5.2, the lumped capacitance model is used.

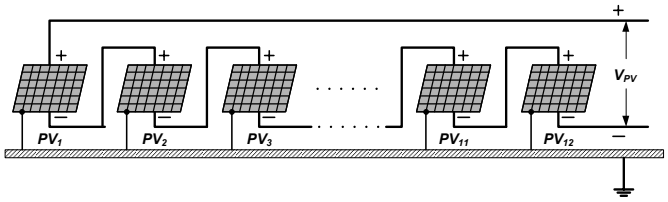

Fig. 5.2: Practical rooftop system of 2.76 kW-per string rating with 12 series modules. Note: Module frame is grounded, per NEC requirements

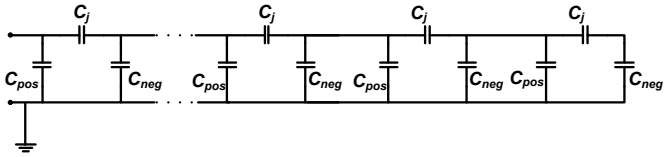

Fig. 5.3: Equivalent circuit of a 12 module PV system with C_j, p-n junction capacitance, C_{pos}, module-to-ground capacitance (positive terminal) and C_{neg}, module-to-ground capacitance (negative terminal)

The capacitances in the PV string system are represented by the equivalent circuit in fig. 5.3 where C_j is the p-n junction capacitance of the PV module, C_{pos} is the capacitance measured from the positive terminal of module to ground and C_{neg} is the capacitance measured from the negative terminal of module to ground. The stray capacitances on the two terminals may not necessarily be symmetric.

The equivalent capacitance of the entire string is measured between the positive terminal of module 1 and the frame-bonded ground. The experiment was performed under dark conditions so that the voltages in the common mode capacitances are zero and the junction capacitances are non-zero [82]. The number of modules in the string was progressively reduced and the capacitance to ground was measured. From the equivalent circuit in fig. 5.3 the capacitance to ground from the positive terminal of module 1 is C_n as given in (35), where n is the number of modules present in the circuit.

$$C_n = \begin{cases} \dfrac{(C_{n-1}+C_{neg})\cdot C_j}{C_{n-1}+C_{neg}+C_j}+C_{pos} & ;n \neq 1 \\ \dfrac{C_{neg}\cdot C_j}{C_{neg}+C_j}+C_{pos} & ;n = 1 \end{cases} \tag{35}$$

The experiment is repeated by shorting the negative terminal of the string to the ground. The equivalent circuit of the PV string with the negative terminal grounded is given in fig. 5.4. The capacitance to ground from the positive terminal of module 1 in the system in fig. 5.4 is given by (36).

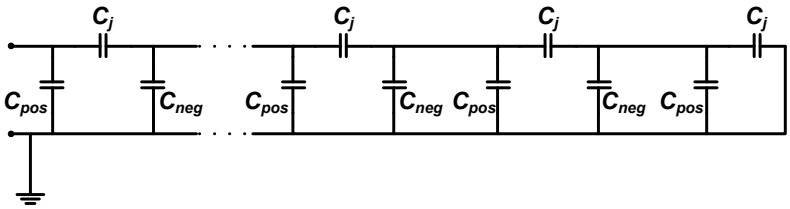

Fig. 5.4: Equivalent circuit of a 12 module PV system where the negative terminal is shorted to the ground, C_j is the p-n junction capacitance C_{pos}, module-to-ground capacitance (positive terminal) and C_{neg}, module-to-ground capacitance (negative terminal)

$$C_n = \begin{cases} \dfrac{(C_{n-1} + C_{neg}) \cdot C_j}{C_{n-1} + C_{neg} + C_j} + C_{pos} & ; n \neq 1 \\ C_{pos} + C_j & ; n = 1 \end{cases} \qquad (36)$$

The capacitances to ground from module 1 are measured for different values of n. Measured typical values of C_{pos}, C_{neg} and $C_{j,}$ as measured in individual modules, are 270 pF, 270 pF and 161,500 pF respectively. These values are used to calculate C_n from (35) and (36). The calculated and measured values are listed in table 5.1.

Table 5.1: Calculated and Measured Values of Module 1 Capacitance to Ground

No. of modules in circuit	**Capacitance with negative terminal floating (calc – calculated, meas – measured)**			**Capacitance with negative terminal shorted to ground**		
	Calc. (pF)	***Meas. (pF)***	***% Error***	***Calc. (pF)***	***Meas. (pF)***	***% Error***
12	5609	9180	63.7	15560	14100	-9.4
11	5252	3960	-24.6	16619	15200	-8.5
10	4870	3700	-24.0	17920	16530	-7.8
9	4465	3350	-25.0	19546	18220	-6.8
8	4037	3020	-25.2	21619	20070	-7.2
7	3587	2675	-25.4	24331	22600	-7.1
6	3117	2330	-25.2	28003	26120	-6.7
5	2628	1979	-24.7	33213	31312	-5.7
4	2123	1603	-24.5	41115	38530	-6.3
3	1604	1243	-22.5	54402	51125	-6.0
2	1075	854	-20.6	81155	78043	-3.8
1	539.5	470	-12.9	161770	158000	-2.3

The error between the calculated and measured values of capacitances to ground is up to 25.4% for the negative terminal floating method and 9.4% for the shorted negative terminal method occurring in the case of 12 modules in the circuit. An abrupt increase in the capacitance happens with floating negative terminal when the 12th module is added to the string along with the long power cables connecting to the inverter. The values of panel-ground capacitances as functions of the module index are shown in fig. 5.5 and fig. 5.6.

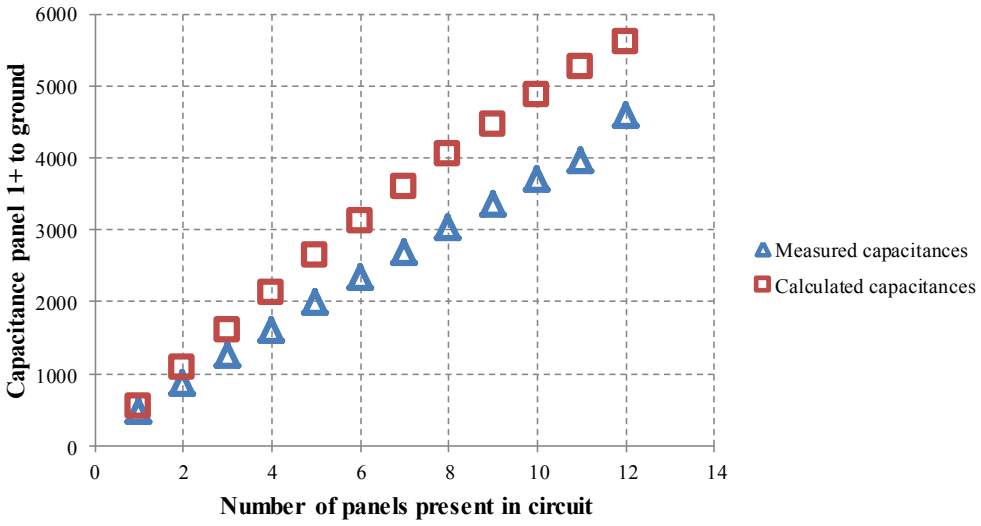

Fig. 5.5: Capacitance to ground at positive terminal of module 1 vs. module index, with the negative terminal floating

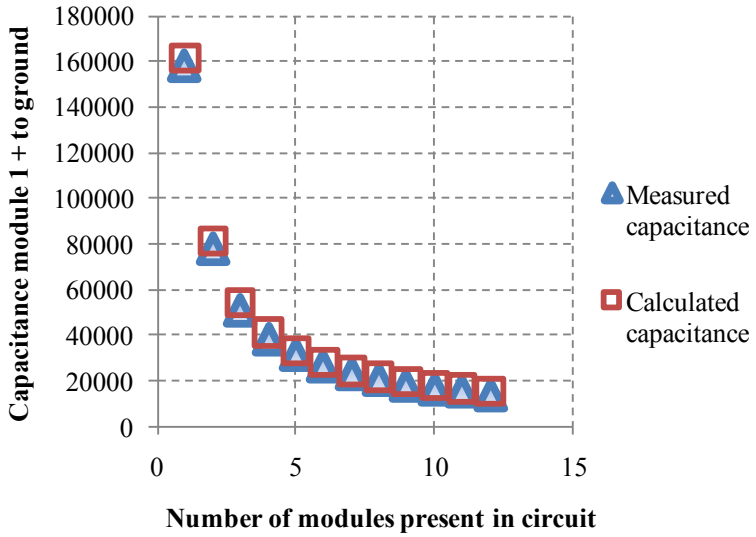

Fig. 5.6: Capacitance to ground at positive terminal of module 1 vs. module index, with the negative terminal shorted to the ground

The increase in the capacitance to ground, with increasing number of modules added to the string, as shown in fig. 5.5, demonstrates that the module at the highest voltage in a series connected string experiences the highest common mode equivalent capacitance and hence the highest voltage PV module will see the highest levels of common mode voltage elevation in the system [79]. The study of these distributed capacitances may also be employed in fault identification in photovoltaic systems [82]. In addition to the distributed capacitances in the photovoltaic modules, common mode capacitances are also present between the primary and secondary windings of isolation transformers, and to the ground from these windings.

5.4. Common Mode Equivalent Circuits of PV System Topologies

A photovoltaic power system is connected to the utility by means of high frequency PWM power converters. The operation of the DC-DC converters and DC-AC inverters produces, in addition to the differential mode voltage between the output terminals, a common mode voltage between either of the output terminals and the ground. This voltage elevates the potential of the output lines in the converter with respect to system ground and has high frequency PWM components [81]. To study the effects of common mode voltages and currents, the various topologies considered are given below, from fig. 5.7 to fig. 5.11.

1. In fig. 5.7 PV modules in series-parallel combinations to achieve utility scale voltages, which are then connected to the utility through a central DC-AC inverter followed by line frequency isolation transformer. The inverter also performs maximum power point tracking (MPPT).

2. In fig. 5.8 PV modules in series-parallel combinations with each module having its own DC-DC converter which are then connected to a central inverter In this approach the power extracted from each module is maximized because each module has its own MPPT converter.

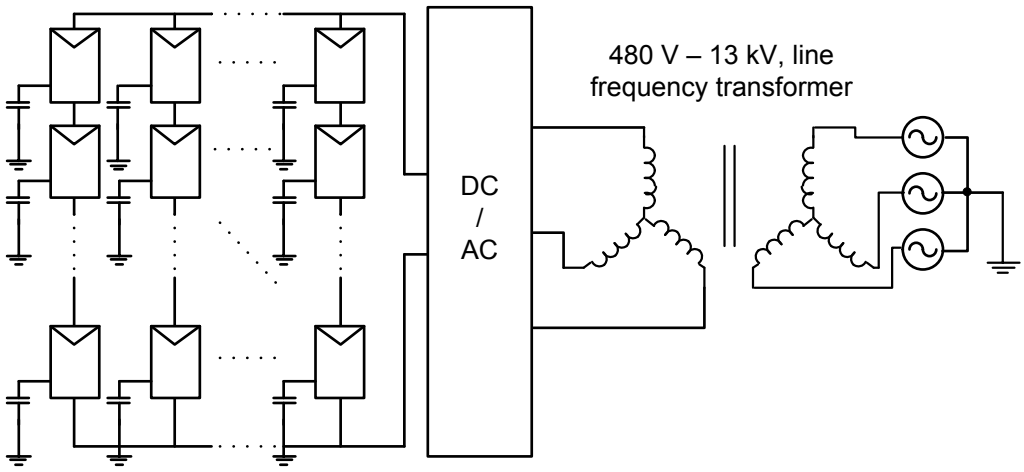

Fig. 5.7: Centralized approach with an array of PV modules connected in series-parallel as shown, with a central inverter and 60 Hz isolation transformer

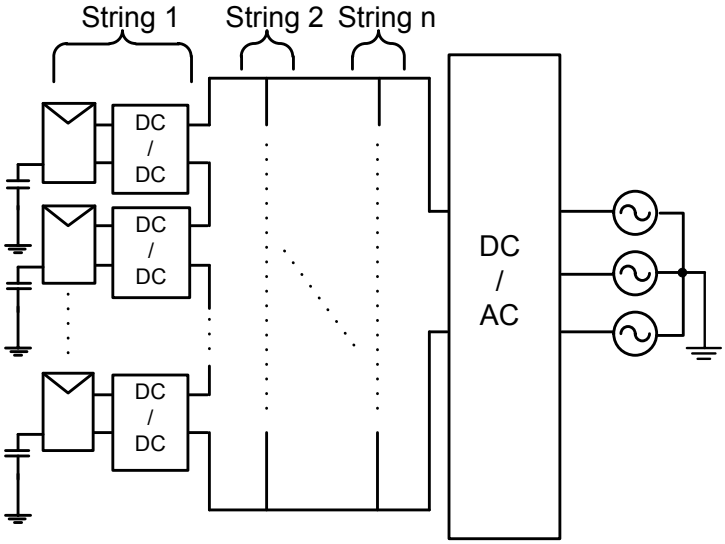

Fig. 5.8: An array of per-module DC-DC connected in series-parallel configuration with central inverter

3. In fig. 5.9 a medium voltage multilevel inverter topology is described. The system has “blocks” in which PV modules in series combinations are connected to

high frequency transformer isolated DC-DC converters, followed by single phase inverters. Multiple blocks in series form a three phase utility system. The medium voltage multilevel topology will be analyzed in detail in section IV.

4. In fig. 5.10 PV modules with their individual MPPT DC-DC converters are in parallel which are then connected to a central DC-AC inverter, in a plug-and-play fashion.

5. In fig. 5.11 the micro-inverter approach where each module is connected to its own DC-AC inverter is shown. The inverter is normally housed within the PV module.

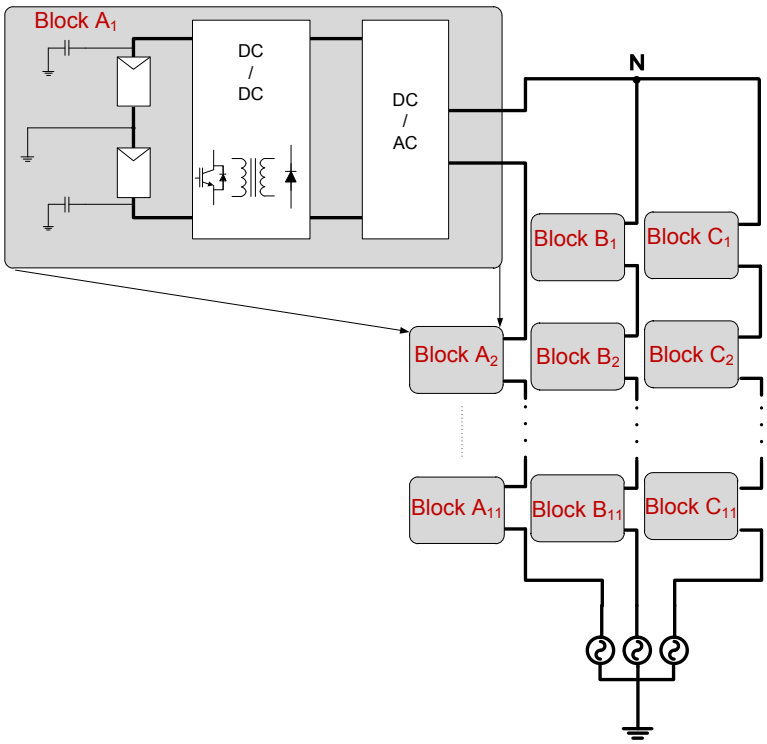

Fig. 5.9: Medium-voltage, multilevel topology built from modular blocks comprised of PV modules connected to a DC-DC converter followed by a single phase inverter.

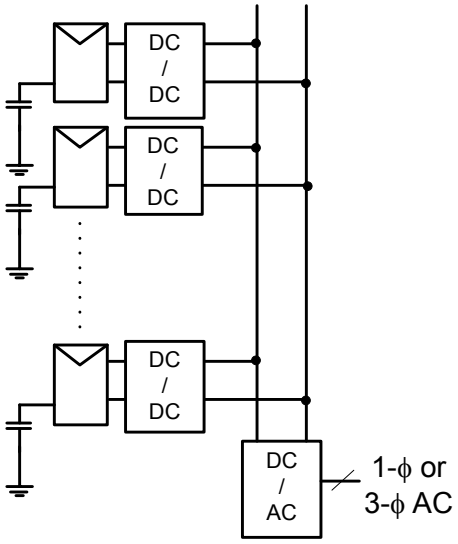

Fig. 5.10: Per-module DC-DC converters arranged in a plug-and-play fashion with one central inverter interfacing to utility

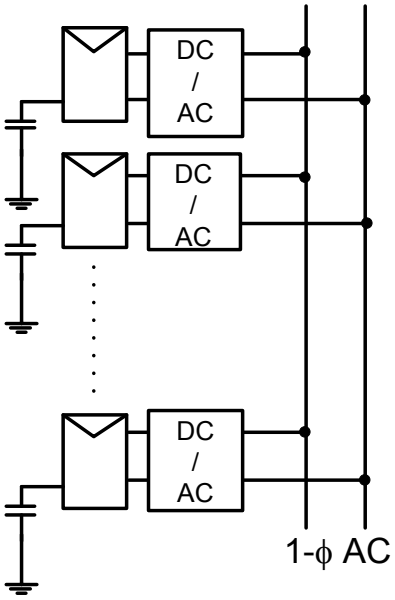

Fig. 5.11: Per-module DC-AC micro-inverters connected in parallel to the AC bus, supporting a plug-and-play design and operation of the system.

As the common mode voltages appear across the distributed capacitances in the PV system, current spikes are induced in them due to the high $\frac{dV}{dt}$ transitions in the common mode voltage [83]. The RMS value of common-mode current in the PV system is dependent on the value of the stray capacitance, switching frequency of the converter and the rise and fall times of the common mode voltage. This is similar to the problem faced in printed circuit board (PCB) design, caused by unintended coupling paths through parasitic capacitances [84].

The common mode equivalent circuits for the topologies discussed in fig.5.7 and 5.8 are presented in fig. 5.12 and 5.13. The high frequency transitions in common mode voltage in the inverter legs and DC-DC converter are modeled as switched mode voltage sources. For instance, the common mode voltage in the system depicted in fig. 5.12 is due to the inverter operation and can be derived as in (37).

$$V_{NG} = \frac{V_{aN} + V_{bN} + V_{cN}}{3} + V_{oG} \tag{37}$$

As illustrated in fig. 5.13 there are two possible common mode current paths: (a) common mode current component due to the DC-DC converter operation and (b) component due to the high frequency inverter operation.

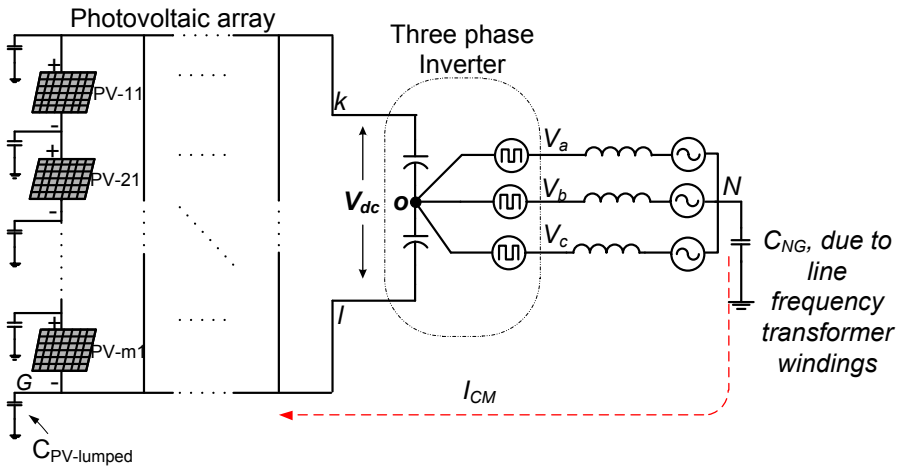

Fig. 5.12: Common mode equivalent circuit of an array shown in fig. 5.7 with *m* columns and *n* rows of PV modules with central inverter interfacing to utility

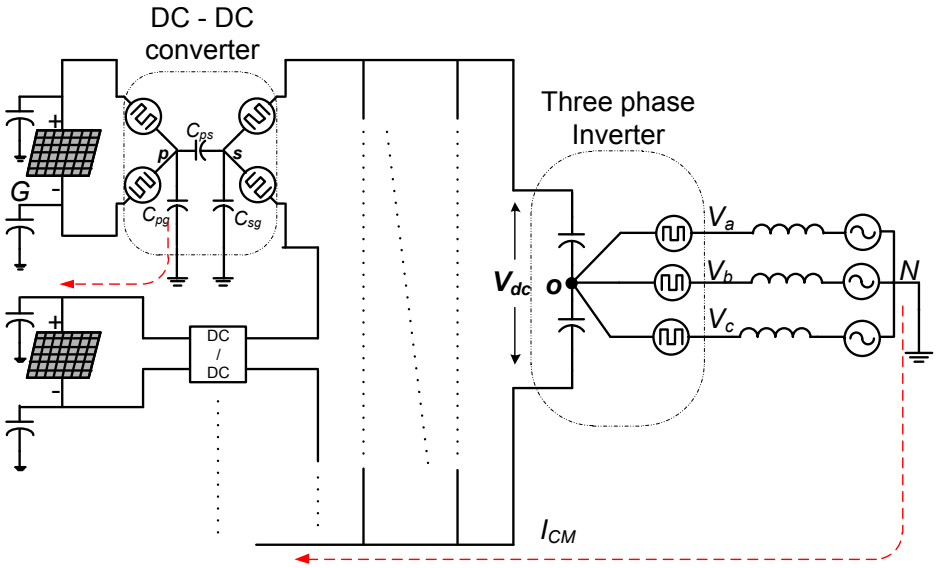

Fig. 5.13: Common mode equivalent circuit of an array shown in fig. 5.8 with *m* columns and *n* rows of per-panel DC-DC converters followed by central inverter

Fig. 5.14 and 5.15 show the common mode equivalent circuits for the topologies discussed in fig. 5.10 and fig. 5.11 respectively.

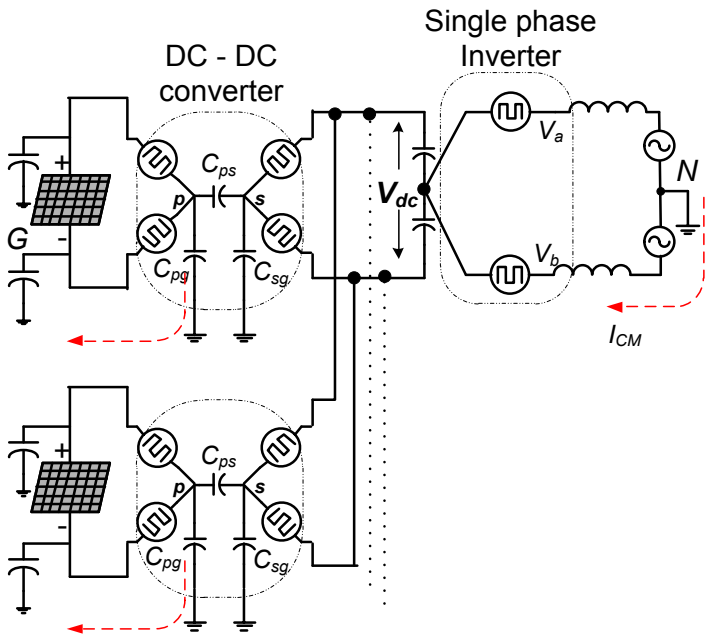

Fig. 5.14: Common mode equivalent circuit of string shown in fig. 5.10 with per-panel DC-DC converters in plug-and-play configuration

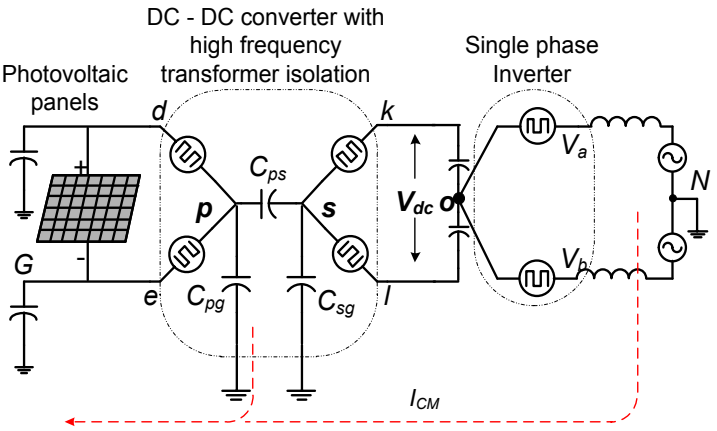

Fig. 5.15: Common mode equivalent circuit of per-panel micro-inverter configuration shown in fig. 5.11.

By simplifying the equivalent circuits, the value of common mode currents induced in the stray capacitances could be calculated. The common-mode currents, I_{CM}

in the topologies in fig. 5.12, 5.13, 5.14, and 5.15 are expressed in (38), (39), (40), and (41).

$$I_{CM} = \left[\frac{(2m-1)n\, C_{PV-lumped}\, C_{NG}}{(2m-1)n\, C_{PV-lumped} + C_{NG}} \right] \frac{d}{dt} \left(\frac{V_{aN} + V_{bN} + V_{cN}}{3} + V_{oG} \right) \tag{38}$$

$$I_{CM} = mn \frac{C_{pg} C_{PV-lumped}}{C_{pg} + C_{PV-lumped}} \frac{dV_{pG}}{dt} + mn\, C_{ps} \frac{d}{dt} \left[V_{pG} - \left(V_{so} + \frac{V_{aN} + V_{bN} + V_{cN}}{3} + V_{NG} \right) \right] \tag{39}$$

$$I_{CM} = m \frac{C_{pg} C_{PV-lumped}}{C_{pg} + C_{PV-lumped}} \frac{dV_{pG}}{dt} + mC_{ps} \frac{d}{dt} \left[V_{pG} - \left(V_{so} + \frac{V_{aN} + V_{bN}}{2} + V_{NG} \right) \right] \tag{40}$$

$$I_{CM} = mn \frac{C_{pg} C_{PV-lumped}}{C_{pg} + C_{PV-lumped}} \frac{dV_{pG}}{dt} + mn\, C_{ps} \frac{d}{dt} \left[V_{pG} - \left(V_{so} + \frac{V_{aN} + V_{bN} + V_{cN}}{3} + V_{NG} \right) \right] \tag{41}$$

Topology 1 shown in fig. 5.7 is simulated using PSIM with the system specifications given below in table 5.2.

Table 5.2: Specifications for Centralized Inverter Analysis

System voltage	Three phase AC 1100 V line-line RMS
Number of modules in string, m	40
Number of strings in system, n	10
System power rating	92 kW DC
AC side line frequency transformer, winding-ground capacitance	50,000 pF
PV Module-to-ground capacitance, C_{pos} / C_{neg}	270 pF
Inverter switching frequency	2500 Hz

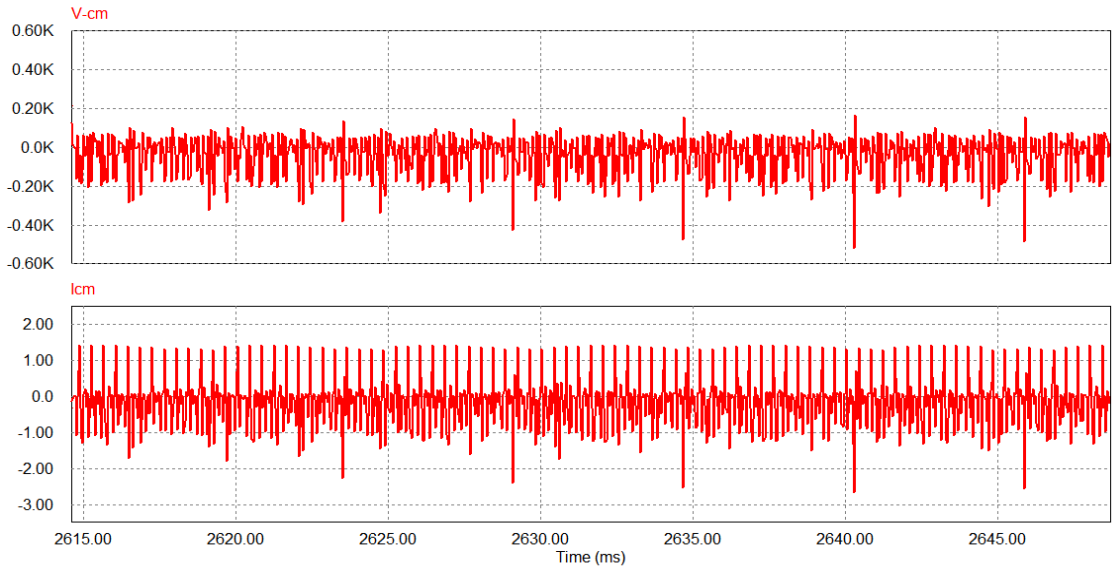

Fig. 5.16: Common-mode voltage and current on AC side transformer ground capacitance, C_{NG}

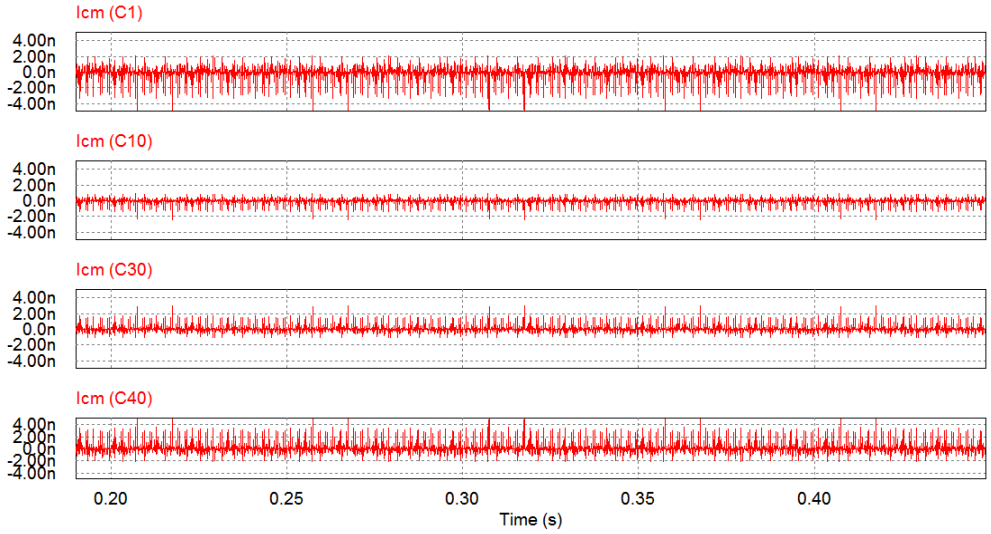

Fig. 5.17: Common mode currents in module-to-ground capacitance of modules 1,10,30 and 40 in a string

The waveforms of common-mode voltage and common-mode current on the AC side are given in fig. 5.16. In fig. 5.17, an analysis of the common mode currents in different module-to-ground capacitances shows that the PV modules with the lowest DC voltage exhibit the lowest common mode currents. As it can be seen the common mode currents increase in the modules that are further closer to the positive and negative dc bus rails.

5.5. Analysis of a Medium Voltage Multi-level Utility Photovoltaic System

A multi-level medium voltage utility photovoltaic system was studied for common mode voltage and current effects. The system specifications are as below in table 5.3.

Table 5.3: System Specifications for Medium Voltage Utility PV System

System voltage	Three phase AC 13 kV line-line RMS
Power rating	1.062 MW DC
Number of blocks in series, per phase	11
DC bus voltage per block	1056 V
Number of modules per block	140 (35 per string, 4 strings in parallel)
Control strategy	Multi-level Carrier Phase Shifted Sinusoidal PWM
Inverter switching frequency	2500 Hz

Each phase in the 13 kV system is comprised of 11 blocks in series, with each one producing a 690 V single phase AC output.

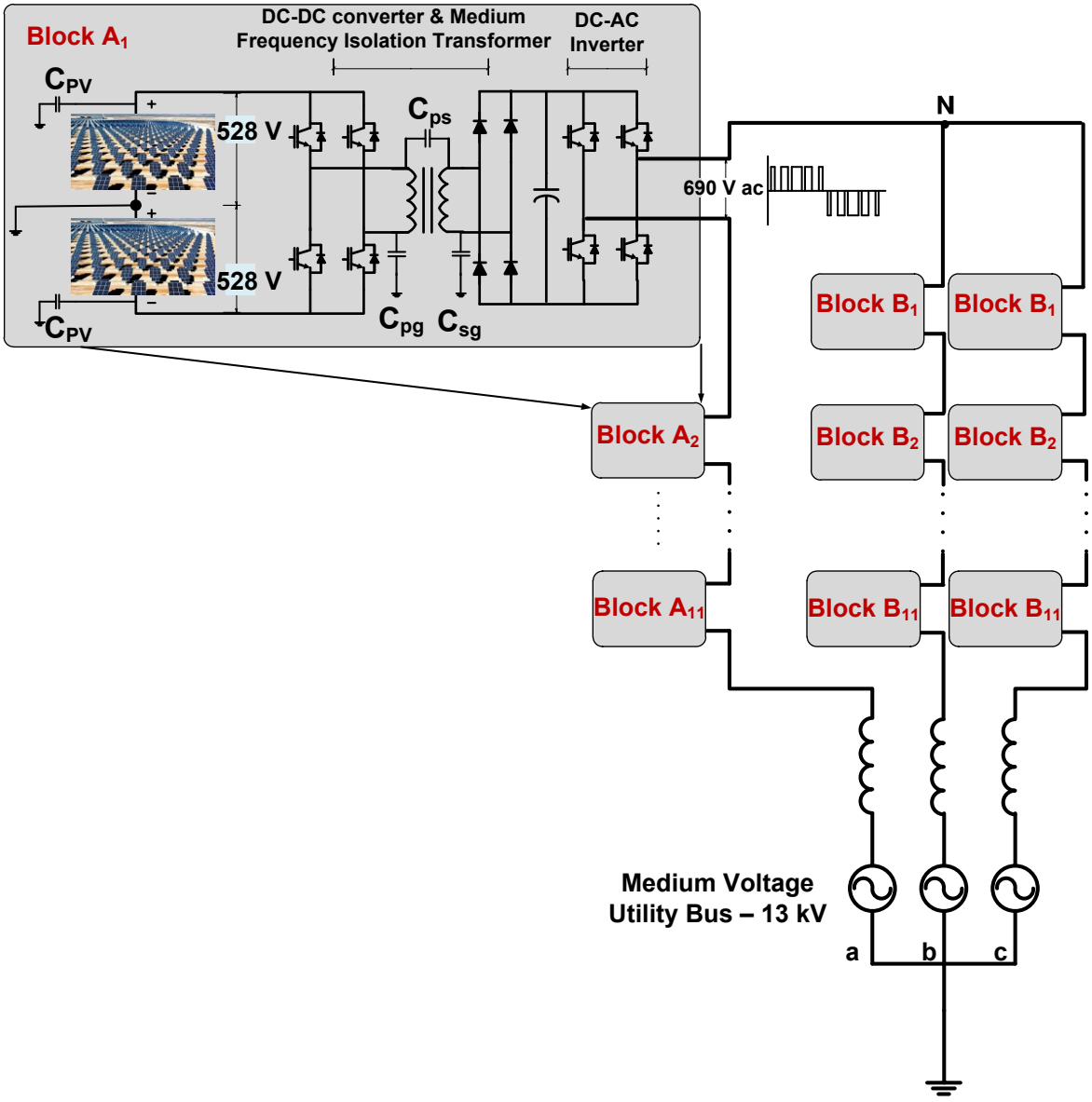

Fig. 5.18: Medium voltage 13 kV multilevel three phase system topology with 11 blocks per phase, each block producing 690 V single phase ac

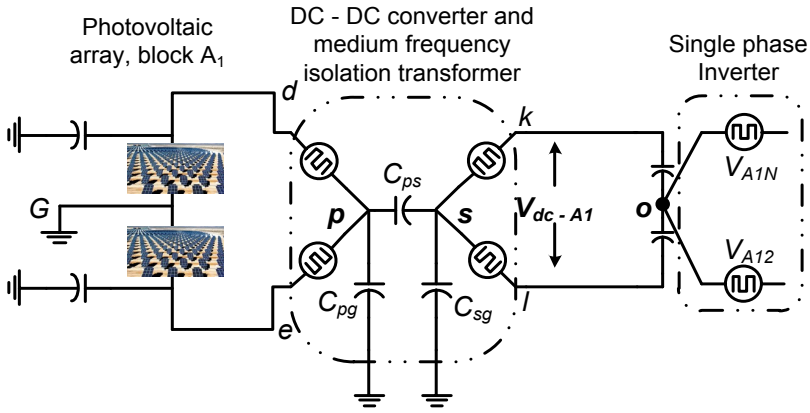

Fig. 5.19: Common mode equivalent circuit of one block (Block A_1) in 13 kV multilevel topology

The DC bus is formed by DC-DC MPPT converters with medium frequency transformer isolation fed by photovoltaic arrays. A schematic of the system is given in fig. 5.18. Since in commercial PV systems, entire arrays are connected to the earth individually, the lumped ground capacitances of blocks are used, C_{PV} calculated to be 65,000 pF, based on the values from table 5.1. The values of transformer winding to ground capacitances C_{pg}, C_{sg} and C_{ps} are chosen as 100 pF, 200 pF and 50 pF respectively. The equivalent circuit of a multilevel PV system block with common mode voltages modeled as switched mode voltage sources is shown in fig. 5.19.

The PWM carrier waveforms for the single phase inverter in each block are phase shifted with respect to the previous block by $\frac{360}{11}$ degrees. The output multilevel voltages are shown in fig. 5.20.

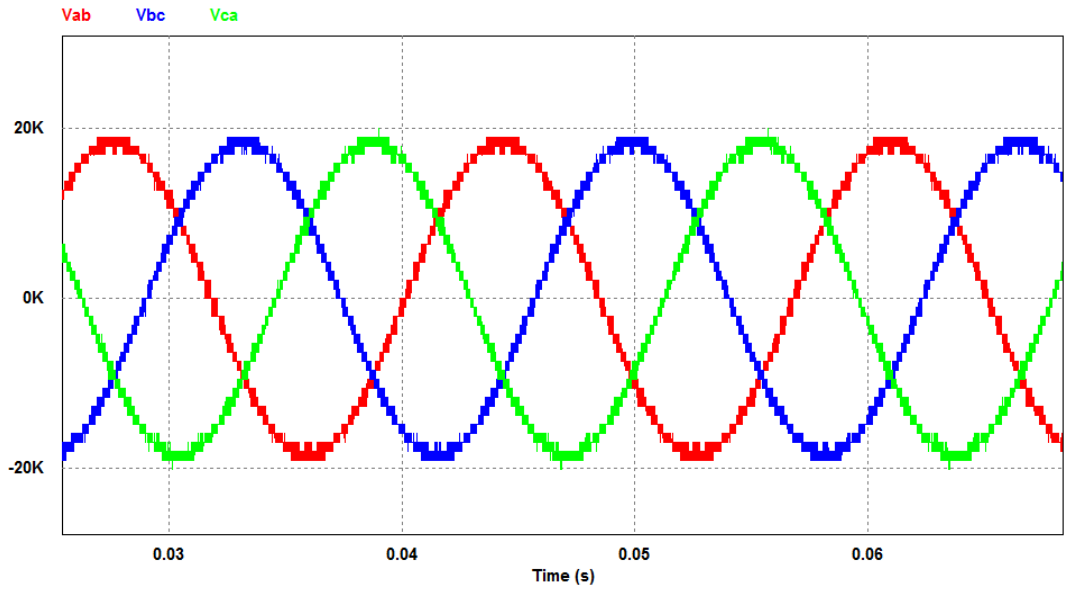

Fig. 5.20: Three phase line-line output voltages in a medium voltage level PV system

As it can be observed from simulation results in fig. 5.21, the blocks which are closer to the neutral point exhibit lower values of common mode voltages and currents in the ground capacitances. In the blocks that are progressively closer to the utility the common mode voltages and currents in the ground capacitances increase. The voltage stress on the medium frequency transformer primary-secondary capacitance also increases for blocks closer to the utility voltage. Fig. 5.22 shows the voltage stresses on the transformer winding capacitances in blocks 1, 6 and 11.The greater RMS voltage stress on blocks closer to the utility requires the transformers in those blocks to have greater insulation requirements.

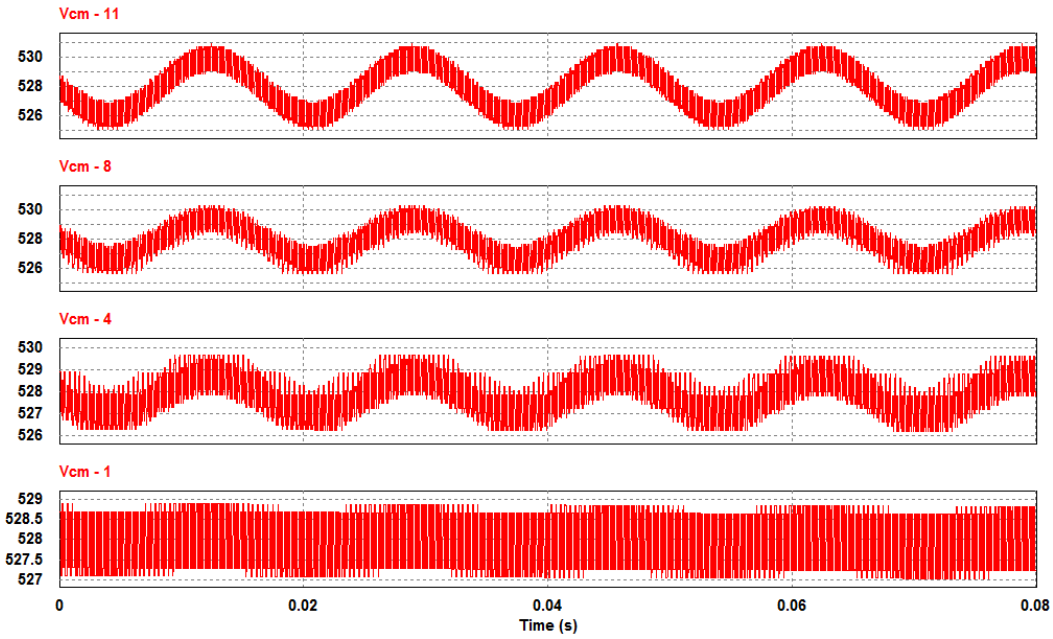

Fig. 5.21: Voltages across module to ground common mode capacitances in blocks 1, 4, 8 and 11

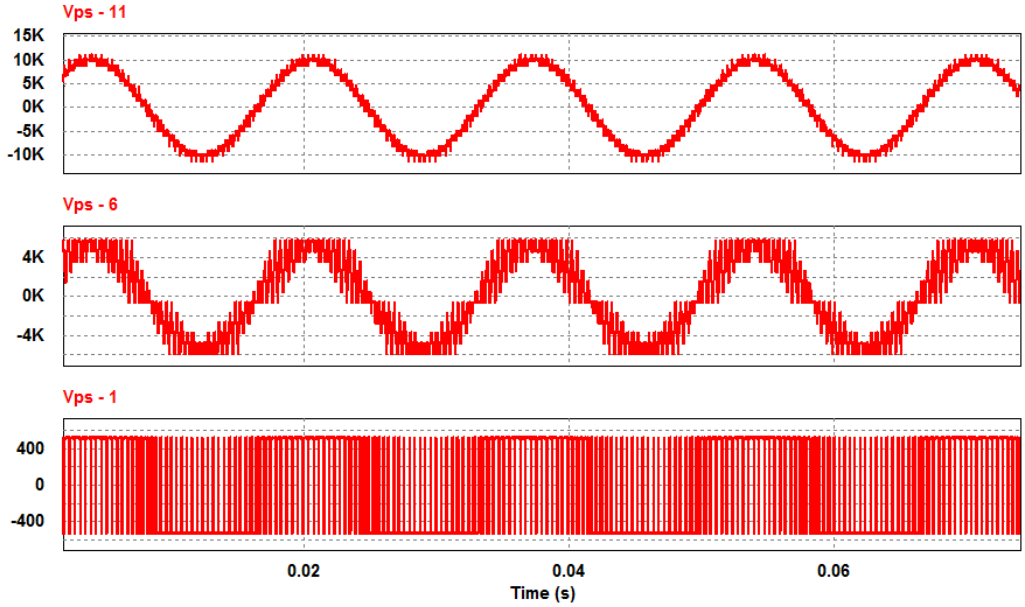

Fig. 5.22: Voltage stresses across primary-secondary winding capacitances in medium frequency transformer for blocks 1, 6 and 11

5.6. Mitigation of Common Mode Voltages in Multi-level Utility PV System

Common mode currents in stray ground capacitances are caused by high frequency $\frac{dV}{dt}$ transitions. In order to mitigate these currents the transitions in voltage need to be slower, i.e., the rise time and fall time of such transitions need to be increased. This can be achieved by introducing a common mode low-pass filter between the inverter output terminals and the DC bus. The L-C-R filter, as shown in fig. 5.23, is designed such that the filter time constant is larger than a critical rise time, which is a function of all the stray capacitances present in the system [6].

$$\text{Filtertimeconstant } \sqrt{L_f C_f} \geq t_{critical} \tag{42}$$

$$R_f = \sqrt{\frac{4L_f}{C_f}} \tag{43}$$

The filter component values are chosen using (42) and (43) such that the response to the filter is over-damped to reduce $\frac{dV}{dt}$ [85]. The design values of common mode filter component for the multi-level topology analyzed are: L_f = 250 μH, C_f = 16 μF and R_f = 15.4 Ω. Another technique to mitigate common mode currents is to use a shielded transformer in the DC-DC converter as seen in fig. 5.24. By using a transformer shielding and grounding it to their respective grounds, the transformer primary-secondary capacitance is split into two. This also breaks the path of the common mode circulating current by separating it into the common mode current loops in the DC-DC

converter side and the inverter side. The topology of one block of the medium voltage system with the common mode filter and transformer shielding is illustrated in fig. 5.25. The 13 kV multi-level PV system is analyzed with the common mode filter and the transformer shielding included.

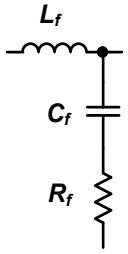

Fig. 5.23: L-C-R common mode low pass filter

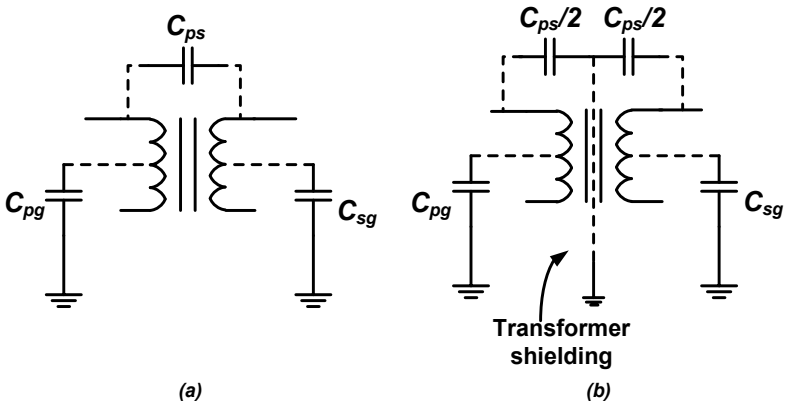

Fig. 5.24: Winding capacitances in transformer (a) without any shielding and (b) with transformer shielding

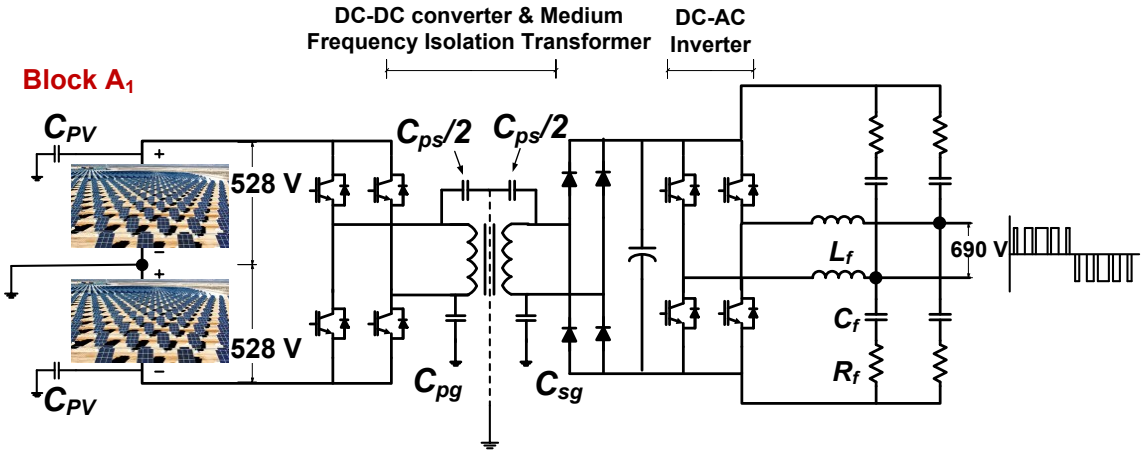

Fig. 5.25: One block in the phase A of multilevel medium voltage (13 kV) photovoltaic system with common mode filter and transformer shielding

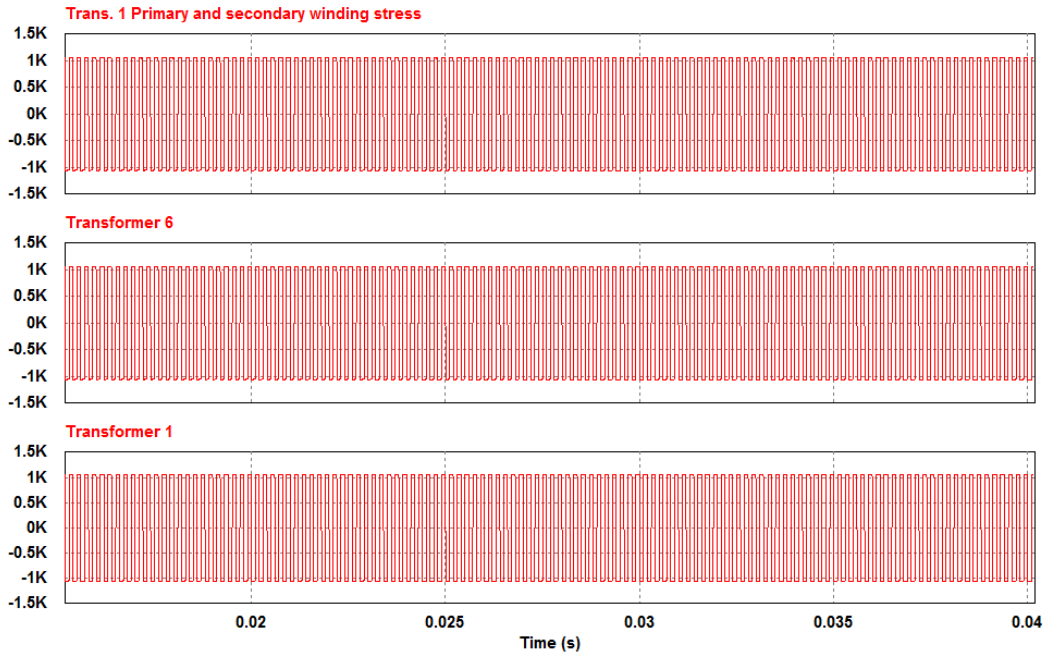

Fig. 5.26: Voltage stresses across primary-to-secondary winding capacitances in medium frequency transformer for blocks 1, 6 and 11, with common mode filters and transformer shielding

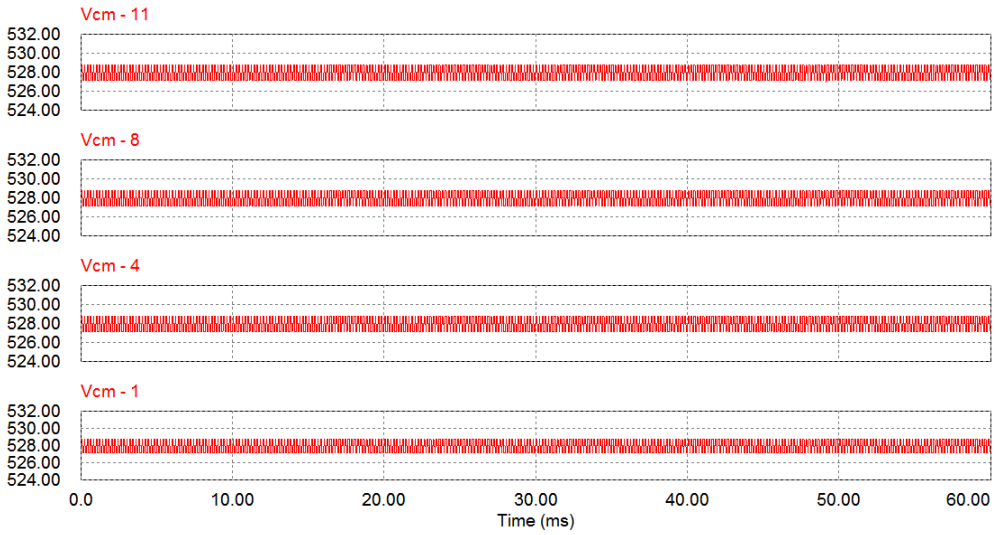

Fig. 5.27: Voltages across module-to-ground common mode capacitances in blocks 1, 4, 8 and 11, with common mode filter and transformer shielding

Upon using a common mode filter and transformer shielding, there is a significant reduction in the voltage stresses on high frequency transformer winding capacitances, as seen from fig. 5.26. The RMS values of voltage stresses for the transformers in blocks 1, 6 and 11 are listed in table 5.4.

Table 5.4: RMS Voltage Stress on Transformer Primary & Secondary Windings

RMS voltage stress on	**Without filter and shielding**	**With filter and shielding**
Transformer 11	7223.94 V	1054 V
Transformer 6	3963.62 V	1053 V
Transformer 1	527.39 V	1054 V

The use of transformer shielding ensures that the common mode voltages due the DC-DC converter and inverter operations are decoupled, reducing the voltage stresses on the PV modules, as seen from fig. 5.27.

5.7. Conclusion

In this chapter, the analysis of common mode voltages and currents in utility and commercial scale photovoltaic power generation schemes has been presented. The distribution of common mode capacitances along a series string of 12 modules was investigated using a 2.76 kW-per string rooftop PV system. The common mode equivalent circuits of various PV system topologies were derived. Mitigation strategies such as common mode low pass filter and isolation transformer shielding were also presented to reduce the effects of common mode voltages and currents. Simulation results of a PV module array rated at 92 kW connected to a central inverter show that the PV modules closer to the positive and negative dc bus rails exhibit the highest magnitudes of common mode currents. An example system of 1.06 MW rating was chosen for the analysis of medium voltage utility scale photovoltaic system. The magnitudes of voltage stresses on common mode capacitances for different blocks in a medium voltage system were found to increase on converter blocks closer to the utility grid. The transformer shielding was used to reduce the voltage stress on PV modules by isolating the common mode circulating current path. It has been shown that the common mode low pass filter, in conjunction with the shielding, significantly reduces the common mode voltage stress on the transformer winding capacitance, up to 50%. The other topologies studied such as per-module DC-DC converter array, parallel-connected

per-module DC-DC converter and microinverter topology have reduced common mode voltages at the PV modules and reduced voltage stress on the isolation transformer, reducing the insulation requirements for those transformers.

6. CONCLUSION AND FUTURE WORK

6.1. Summary

This dissertation discussed multilevel inverter topologies for utility scale PV applications. State-of-the-art topologies for grid integration of PV plants were discussed. It was seen that multilevel inverters had better performance than two level inverters. The proposed topology in chapter 2 had a medium frequency AC link transformer with three outputs, which were connected to three phases and this approach eliminated the double frequency ripple on the DC bus capacitor, reducing its rating. The proposed power balancing circuit reduced the effects of unequal insolation within a PV array. Simulation and experimental results demonstrated the operational performance of the proposed inverter.

A localized control strategy for the multilevel inverter was also proposed, in chapter 3 without the requirement for a centralized controller. This approach increased the modularity of the multilevel inverter by having individual inverter cells operate their own control loops for real and reactive power flows. An experimental design with four cascaded cells demonstrated the working of the control strategy. Chapter 4 discussed the phenomena of common mode voltage and common mode currents and the effects of parasitic capacitance on a large scale PV system. Measurements of parasitic capacitances on a practical system were shown. The analysis of CM voltages and currents was performed for different topologies of PV grid integration and techniques to mitigate the effects were discussed.

In chapter 5, a BESS for a utility scale PV system was proposed. The battery system was rated at 10% of the PV inverter and was designed to support the grid during PV intermittencies. The design and simulation results for a 5 MW PV system and scaled down laboratory prototype experimental results were discussed. The battery energy storage system was shown to improve grid stability in the short-run.

6.2. Future Work

Multilevel inverters are becoming more popular methods to directly integrate PV and other distributed energy sources to the utility grid. Research activity in this area has increasing interest and various opportunities for future research exist.

The efficiency advantages which the multilevel topologies possess over two level inverters may be compromised if the semiconductor switches are not highly efficient, since multilevel topologies use more of them. New semiconductor technologies such as SiC and GaN promise high efficiency and high power operation. These devices, combined with soft switching strategies, may improve efficiencies of multilevel converters tremendously. Soft switching techniques such as resonant and quasi resonant switching techniques for the proposed medium frequency transformer based multilevel inverter will be studied. Alternative magnetic materials for the medium frequency transformer such as nanocrystalline materials (e.g. FINEMET) might provide better efficiencies because of their high saturation flux densities.

The medium frequency transformer link may be employed to integrate different types of distributed sources such as wind, PV and fuel cell systems into the same utility grid or a microgrid. The transformer provides isolation between the various power

sources and the control strategy described in this work may be used to harvest different amounts of real and reactive powers from these sources.

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