FAULT-TOLERANT PARTIAL-RESONANT HIGH-FREQUENCY AC-LINK CONVERTERS AND THEIR APPLICATIONS

A Dissertation

by

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ABSTRACT

Recently, the demand for high-power-density converters with high efficiency and enhanced reliability has increased considerably. To address this demand, this dissertation introduces several low, medium, and high power converter topologies with high-frequency ac links and soft-switching operation, both with and without galvanic isolation. These converters can be in ac-ac, dc-ac, ac-dc, or dc-dc configurations to transfer power from the utility, energy storage systems, or renewable/alternative energy sources (e.g., photovoltaics, wind, and fuel cells) to stand-alone loads or the utility. The advantages of these topologies include soft switching at turn-on and turn-off of all the semiconductor devices, exclusion of short-life electrolytic capacitors in the link, step-up/down capability, and the use of a small-sized high-frequency transformer for galvanic isolation. The proposed converters are also able to generate output waveforms with arbitrary amplitude and frequency as well as achieving a high input power factor in the ac-ac and ac-dc configurations. Moreover, some of the introduced topologies have fault-tolerance capability, which may allow the converter to run even with one or more faulty switches. In this case, a partial failure will not result in the converter shutdown, and thus system availability is improved.

The high-frequency ac link of the introduced converters is composed of an ac inductor and small ac capacitor. The link inductor is responsible for transferring power, while the link capacitor realizes soft-switching operation. As the link components have low reactive ratings, the converters exhibit fast dynamic responses. The inductor can be replaced by an air-gapped high-frequency transformer to achieve galvanic isolation without the need for any snubber circuits. Due to operation at a high frequency, the link transformer is

substantially smaller in size and lower in weight compared to conventional line-frequency isolation transformers. In this work, the proposed power topologies are explained in detail, and their comprehensive analyses are given to reveal their functioning behavior in various working conditions. Simulation and experimental results at different operating points are also presented to verify the effectiveness of the introduced power converters.

To my beloved wife, Ghazal,

my devoted parents, Nasser and Shokouh,

and my dear siblings, Nazi, Alireza, and Amirreza.

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1. INTRODUCTION

With the recent advances in the solid-state semiconductors, as well as magnetic and capacitive materials, the demand for power converters with high power density, improved efficiency, and enhanced reliability at low cost has considerably increased. While these attributes have long been considered important for most basic power electronic systems, they are absolutely essential for a variety of developing applications, such as distributed-generation systems with renewable and alternative energy sources (e.g., photovoltaics, wind, and fuel cells), energy-storage systems, vehicle-to-grid applications, electric/hybrid-electric/fuel-cell vehicles, and battery-based uninterruptible power supplies. In such systems, galvanic isolation is often required for safety concerns in addition to voltage and current scalabilities. Moreover, fault tolerance of power converters is becoming more and more essential in many applications, such as aerospace and subsea systems. Fault tolerance involves the detection of the converter's fault(s) and the reconfiguration of the hardware/software in order to continue running the converter even with degraded performance. In this manner, a partial failure will not lead to the converter shutdown, thus improving system availability.

Pulse-width modulated (PWM) power converters with voltage dc links are well developed and widely used in various industrial applications [1]. These converters are simple, highly reliable, and relatively low-cost. However, PWM topologies have the disadvantages of considerable switching losses, high switching stresses, and significant electromagnetic interference (EMI) due to the hard-switching operation [2]. In addition, they mainly employ electrolytic capacitors in their dc link. These capacitors are bulky and

expensive with a limited lifetime, so they can be the critical components, especially in high-power or high-voltage applications. In order to achieve galvanic isolation with an ac line or ac load, PWM converters normally need to employ massive line-frequency isolation transformers.

Soft-switching topologies incorporating zero-voltage switching (ZVS) and zero-current switching (ZCS) have been introduced to increase the conversion efficiency, switching frequency, and power density of converters. Soft-switching converters mainly contain inductor-capacitor resonant networks whose voltage or current varies sinusoidally during one or more subintervals of each switching period [2]. The semiconductor devices of these converters are turned on or off at the zero crossing of the voltage or current of the L-C tank circuit. As a result, this method not only reduces or eliminates the switching losses but also substantially decreases the converter generated EMI.

Power converter topologies with high-frequency ac links are other outstanding solutions for efficient power conversion. Their noticeable advantages include non-appearance of electrolytic capacitors, fast dynamic response, high reliability, and the ability to employ a small-sized high-frequency transformer for galvanic isolation. The soft-switched class of the high-frequency ac-link power converters is remarkable due to the benefits of the high-frequency ac-link converters along with high efficiency, low EMI, and other advantages of the resonant topologies.

The basic soft-switched high-frequency ac-link universal power converter was first introduced in [3]. This novel topology is an extension of the dc-dc buck-boost converter while the input and output can be either dc or ac. Fig. 1.1 shows this converter in the basic ac-ac formation. This converter has several advantages over the conventional converters,

including soft-switching operation, step-up/down capability, bidirectional power flow, and exclusion of the dc-link electrolytic capacitors. As the power is transferred indirectly from the input to the output, the output frequency is arbitrary while the converter can have a high input power factor. In addition, the link inductor and capacitor are small with ac operation; therefore, the topology has a fast dynamic response.

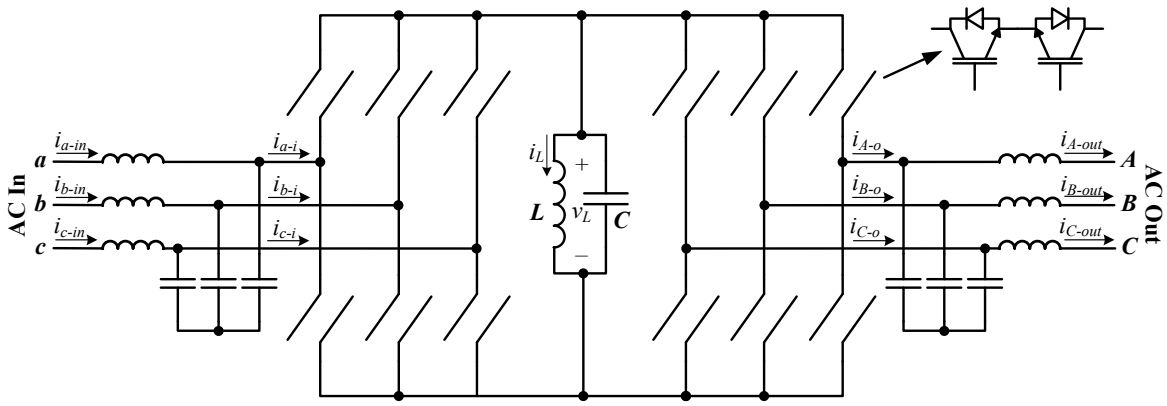

Fig. 1.1. The basic soft-switched high-frequency ac-link power converter.

The soft-switched high-frequency ac-link converter with applicable high-frequency galvanic isolation is introduced in this dissertation. The basic converter is properly modified in order to employ an air-gapped high-frequency transformer by considering the practical issues. The design of the transformer is also given. As this transformer works at a high frequency, it is much smaller than the conventional three-phase line-frequency isolation transformer. A new accurate method to analyze the converter is presented so as to reveal its behavior at different working conditions and design the converter optimally. Furthermore, two reduced-switch generations of the soft-switched high-frequency ac-link converters

(known as type-I and-II reduced-switch topologies) are proposed for low and medium power operations. Finally, the fault tolerance ability of the converter is studied. It is shown that in case of one or more faulty switches in the original converter, the type-I and type-II reduced-switch operating algorithms may be employed in order to continue running the converter with degraded performance.

Based on the introduced isolated soft-switched high-frequency ac-link converter and the reduced-switch topologies, this dissertation also proposes several low, medium, and high power converters for various applications, such as direct ac-ac wind converters, single-stage grid-tied PV inverters, multi-string inverters for PV applications, soft-switched isolated and non-isolated dc-dc converters, and multiple-input multiple-output dc-dc converters. The effectiveness of the proposed converter topologies is verified by means of the simulation and experimental results at different operating points.

2. THE ISOLATED SOFT-SWITCHED HIGH-FREQUENCY AC-LINK CONVERTERS AND THEIR APPLICATIONS*

2.1. Introduction

This section introduces the soft-switched high-frequency ac-link power converter with applicable high-frequency galvanic isolation. The basic converter is appropriately modified so as to employ an air-gapped high-frequency transformer by considering the practical issues. The design of the transformer is also given. As the transformer works at a high-frequency, it is noticeably smaller in size and lower in weight compared to conventional line-frequency three-phase isolation transformers. Furthermore, an original accurate method to analyze the converter is introduced in order to reveal its behavior at various working conditions and design the converter optimally. The advantages of this novel topology are presented for different applications [4]-[7].

2.2. An Isolated Resonant AC-Link Three-phase AC-AC Converter Using a Single High-Frequency Transformer

2.2.1. Introduction

The ac-ac power converters are the major parts of the power regulators, variable-speed ac drives, direct conversion systems in wind generators, and many other applications. The pulse width modulated (PWM) voltage source inverter (VSI) with a front-end rectifier has become the preferred choice in most industrial applications [8]. This is mainly due to its simplicity, high reliability, and relatively low cost. Nonetheless, this converter has the disadvantage of using large electrolytic capacitors on the dc link and a massive low-pass filter at the front end [8], [9]. The dc-link capacitors are bulky and expensive with a limited lifetime, so they can be the critical components, especially in high-power or high-voltage applications. In addition, to have the galvanic isolation in this topology, a bulky 60Hz three-phase transformer should be employed. The converter's switching frequency also cannot be moved up enough to have small reactive components due to the considerable switching losses, high switching stresses, and significant electromagnetic interference (EMI) as a result of the hard-switching operation [10].

Many efforts to overcome the drawbacks of the PWM voltage source inverter-rectifiers have been reported in the literature [11]–[13]. Matrix converters were primarily introduced as outstanding alternatives without the use of any intermediate energy-storage element [9], [14]–[18]. These converters provide noticeable benefits, including the single stage power conversion, bidirectional power flow, sinusoidal input/output waveforms, the possibility of compact design due to the absence of reactive components, and controllable input power factor. However, matrix converters have noticeable drawbacks, such as the

inherent restriction of the voltage transfer ratio, a complex control, no electrical isolation, hard-switching problems, and commutation and protection issues [9], [18]. A dual active bridge (DAB) topology along with the three-phase PWM rectifier and inverter can also realize ac-ac power conversion with a high input power factor and high-frequency (HF) galvanic isolation with the advantage of easier control scheme and fixed switching frequency. However, this topology employs two bulky electrolytic capacitors on both sides of the DAB and burdensome inductors at the front end. In addition, the conversion efficiency is poor due to three stages of power conversion. An interesting direct ac-ac DAB converter with the soft-switching capability was also introduced in [19]; however, it is useful for a single-phase supply to single-phase load with the same frequencies as a solid-state transformer.

High frequency ac (HFAC) link power converters have been suggested as an improved alternative to the conventional dc-link topologies [20]–[26]. These converters have several practical advantages, such as the small size of storage components, absence of electrolytic capacitors, high reliability, fast dynamic response, and the ability to employ a small-sized HF transformer for galvanic isolation. The resonant class of the HFAC-link ac-ac converters can be vastly superior because it includes the noticeable benefits of the HFAC-link converters in addition to the high efficiency, low EMI issues, and other advantages of the resonant topologies. A limited number of resonant HFAC-link ac-ac topologies have been reported [23]–[26]. Pulse-Density Modulation (PDM) was employed in [23] and [24] to control the introduced resonant converters with high power factor and low total harmonic distortion. Nonetheless, PDM controlled converters often have a slow system response with a non-linear discrete output power characteristic. In [25], a simple-structure resonant topology with 12 unidirectional switches was proposed. Although the converter can work in buck-

boost operations in both directions, it has a relatively long resonant mode, which degrades its performance at high power operation. The soft-switched HFAC-link converter in [26] does not include verified galvanic isolation using HF transformers.

This study introduces an isolated HFAC-link three-phase ac-ac converter with galvanic isolation and soft-switching operation. The HF galvanic isolation is realized by a small-sized HF transformer, and soft switching for all the power devices is achieved by two small ac capacitors. The converter can operate in buck and boost modes while achieving a high input power factor without any direct power transfer. Although the control scheme of the converter is rather involved, the topology is expected to have high reliability owing to the exclusion of short-life electrolytic capacitors, high efficiency as a result of soft switching operation, and high power density due to the use of an HF transformer for galvanic isolation. The initial cost of the proposed HFAC-link converter may be higher than the conventional PWM converters due to the use of the bidirectional switches, high-frequency magnetic materials, and a fast digital controller. However, the long life cycle and high efficiency of the proposed converter is expected to offset this initial cost. Therefore, the topology is suitable for applications where a small size and high efficiency is crucially desired, such as wind applications, aerospace industry, and compact efficient motor drives.

The switching frequency of the proposed converter is mainly limited by the speed of the digital controller; the switching frequency should be selected much lower than the controller's sampling rate. In this study, the switching frequency of about 7kHz at nominal conditions was chosen according to the available DSP. Higher switching frequency can be realized by using a faster controller, which leads to a higher power density, smaller input and output filters, and consequently, a higher input power factor.

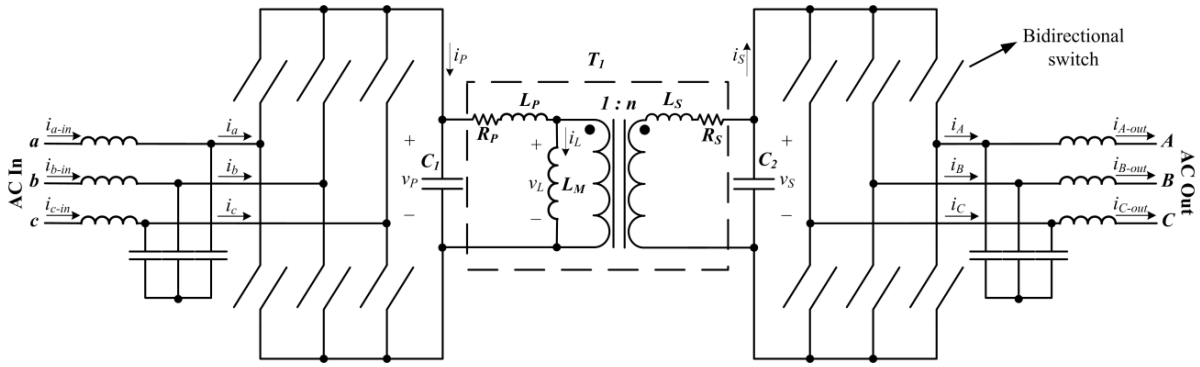

Fig. 2.1. The isolated parallel-resonant HFAC-link ac-ac converter.

2.2.2. The Proposed Topology

The isolated parallel-resonant three-phase ac-ac converter with an HFAC link and soft-switching operation is shown in Fig. 2.1. The galvanic isolation is obtained by means of the single-phase HF transformer T_1. The magnetizing inductance of the transformer, L_M, and capacitors C_1 and C_2 form the HFAC link. In order to reach an appropriate inductance value, the transformer may need to have an air gap. The link capacitors are ac capacitors with small capacitance values. As the figure shows, the converter's switches are bidirectional, e.g., two reverse-conducting switches in anti-series or two reverse-blocking switches in anti-parallel. There are small low-pass filters at the front and load ends of the converter to suppress high-frequency harmonics. In general, power transfer from the input to the output is accomplished via the link inductance, L_M, which is charged from the input voltages, and then discharged to the output phases with a precisely controllable current technique. The link capacitors, C_1 and C_2, produce partial resonance to obtain the soft switching characteristic, as will be shown later. These capacitors are placed on both sides of the transformer to also provide paths for the currents of the primary and secondary leakage inductances when the input and output switches are turned off and subsequently avoid voltage spikes.

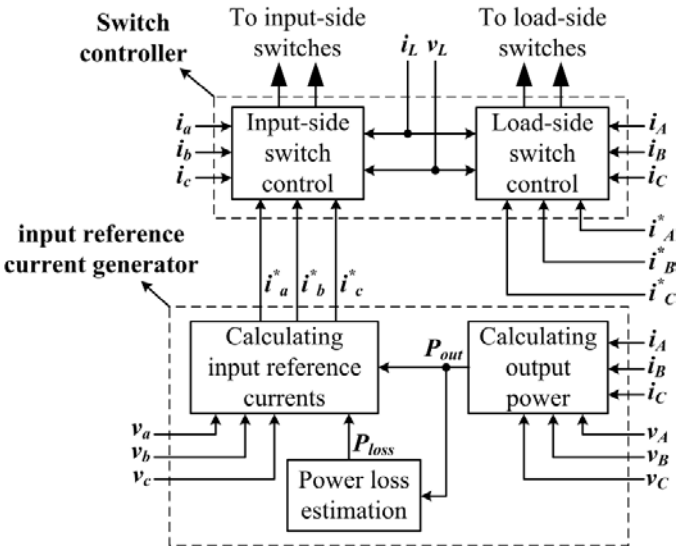

Fig. 2.2. The control scheme of the proposed converter.

2.2.2.1. The Control Scheme of the Converter

Fig. 2.2 shows the control scheme of the proposed converter. According to the figure, the control scheme is composed of two sections: the input reference current generator and the switch controller. The first section generates the input reference currents, i^*_a, i^*_b, and i^*_c, according to the calculated output power and the estimated power loss of the converter in phase with their respective input voltages [5]. The converter's operation is not highly sensitive to the precise value of the power loss because it is normally much smaller than output power. The introduced topology is fundamentally a current-source converter, and consequently, the reference currents of the output phases, i^*_A, i^*_B, and i^*_C, are required for the converter operation. The input and output reference currents are sent to the switch controller section. In this section, the converter's switches are managed properly to meet the reference currents by means of a switching algorithm, which is described in the next section.

2.2.2.2. The Switching Algorithm of the Converter

The basic operation of the proposed topology consists of 16 modes of operation in each link cycle. Typical operating modes and a link cycle of the proposed topology are shown in Figs. 2.3 and 2.4. The converter modes of operation are explained in detail as follows by ignoring the effects of the transformer parasitic elements. Their effect will be shown later.

Mode 1 [Fig. 2.4(a)]: Two proper input-side switches are turned on to connect the link to the highest instant input line-to-line voltage. As a result, the link inductance charges in the positive direction. This mode continues until the average input current of one of the connected input phases meets its reference value. Next, the switches are turned off. Therefore, the connected phase with the smaller reference current magnitude meets its reference current in this mode. The other connected phase will be linked to the HFAC-link in mode 3 again to meet its reference value accordingly.

Note that the link capacitors cause the link voltage, $v_L(t)$, to drop slowly while the mode-1 switches are turned off, and subsequently, the switch voltages increase slowly. As a result, the mode-1 switches are turned off at almost zero voltage. This soft switching operation happens at the turn-off of all the converter's switches.

Mode 2 [Fig. 2.4(b)]: By turning off the input-side switches at the end of mode 1, the link inductance, L_M, resonates with the link capacitors, C_1 and C_2, and the link voltage starts to drop. This resonance is allowed to continue until the link voltage becomes equal to the second highest input line-to-line voltage.

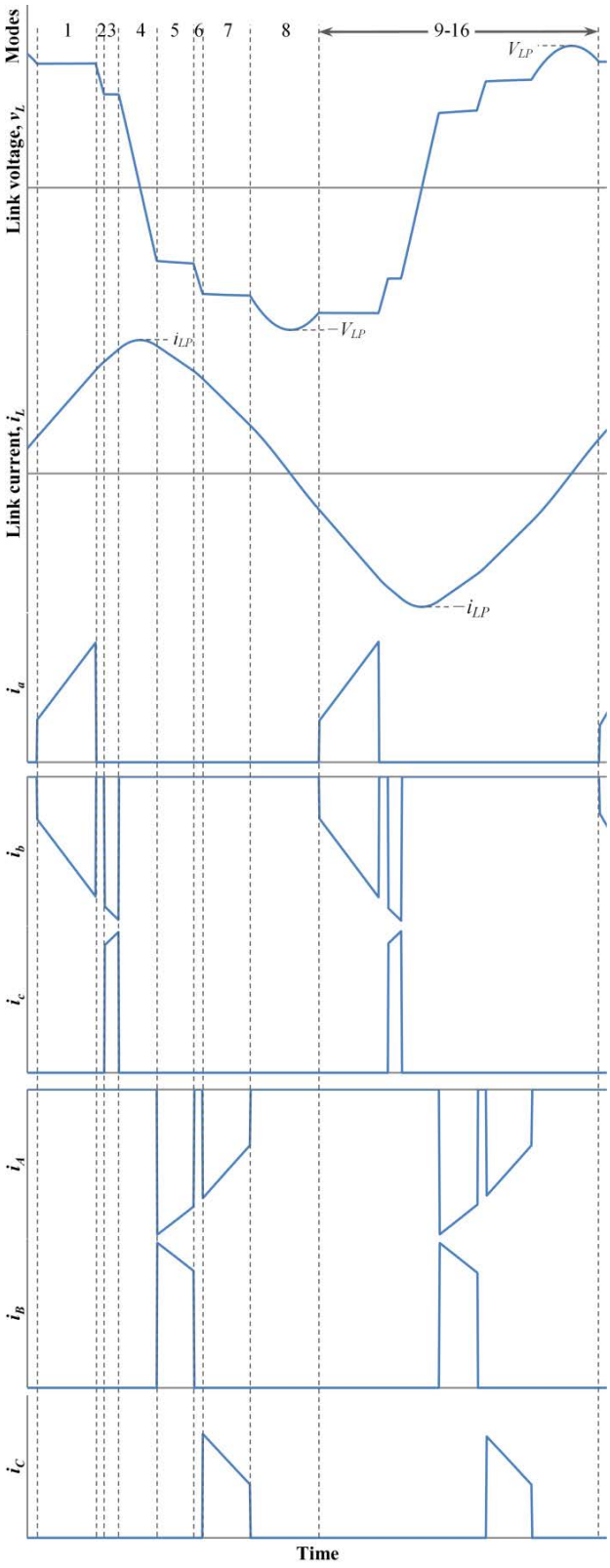

Fig. 2.3. Typical waveforms of the converter. (a) link voltage, (b) link current, (c-e) input currents, and (f-h) output currents.

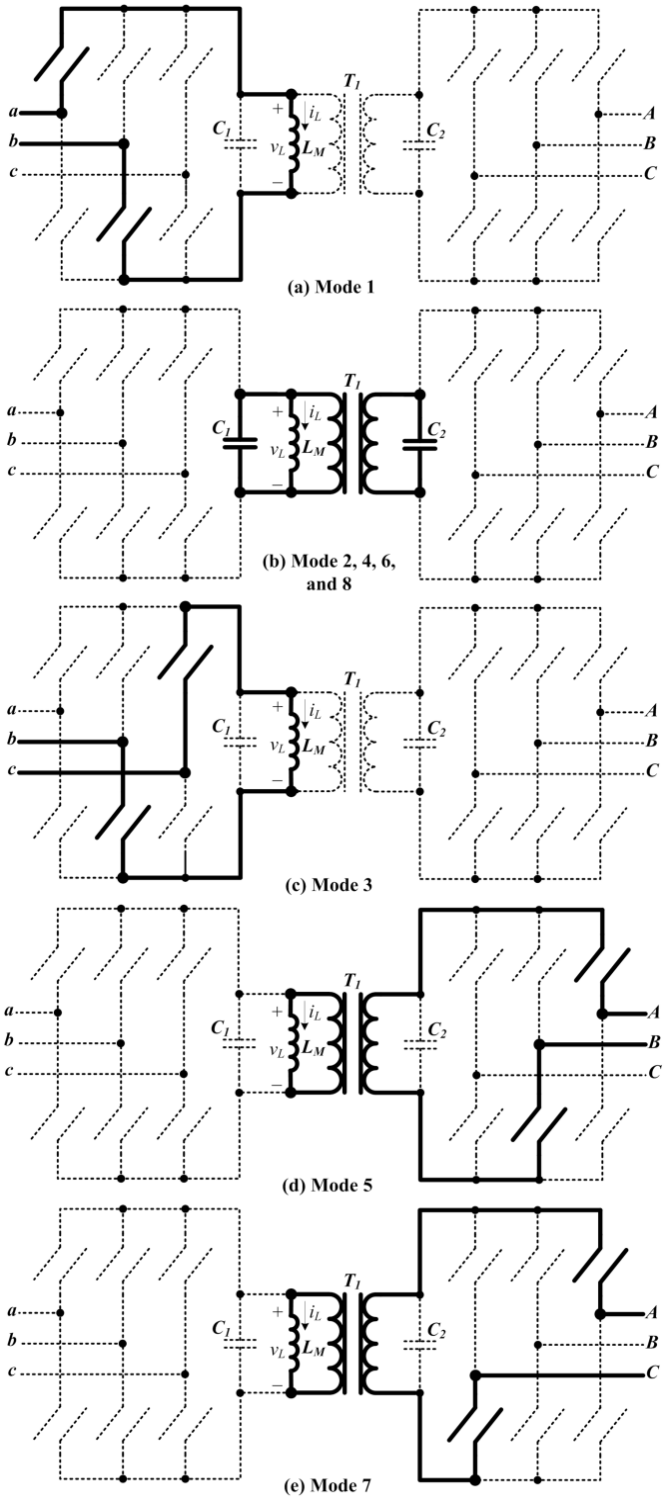

Fig. 2.4. Typical operating modes of the converter.

Mode 3 [Fig. 2.4(c)]: Two i switches corresponding to the second highest input line-to-line voltage are turned on to continue the charge of the link inductance. This charging mode is allowed to run until the average input currents of the two connected input phases meet their reference values. Since the sum of the three phase currents is zero, these two phases meet their reference values simultaneously. The switches are turned off afterwards.

Since the link voltage is equal to the selected input phase pair at the beginning of mode 3, the turn-on of the mode-3 switches occurs at zero voltage. The zero voltage switching happens at the turn-on of all the converter's switches.

Mode 4 [Fig. 2.4(b)]: The link inductance and capacitance are permitted to resonate again until the link voltage is equal to the reflected voltage of the selected output phase pair, as will be discussed later. During this mode, the link current, $i_L(t)$, reaches its peak value, i_{LP}, which can be estimated according to the energy of the link inductance and capacitance at the end of mode 3 as follows:

$$i_{LP} = \sqrt{{i_L}^2(t_3) + \frac{C_1 + n^2 C_2}{L_M} {v_L}^2(t_3)} \tag{2.1}$$

where t_3 is the time at the end of mode 3, and n is the transformer output-input turns ratio.

Two output phase pairs should be selected for modes 5 and 7. The two phase pairs that have the lowest and second-lowest reference current difference at the instant are chosen for this purpose. Among these two phase pairs, the one with lower voltage is chosen for mode 5 and the other for mode 7. In this way, the link voltages in modes 3, 5, and 7 are in descending order, and as a result, the resonant intervals between these modes are in the shortest possible case.

Mode 5 [Fig. 2.4(d)]: Two proper load-side switches are turned on at zero voltage to discharge the link inductance to the selected output phase pair for this mode. These switches

remain on until the average output current of one of the connected phases meets its reference value. Then, the switches are turned off.

Mode 6 [Fig. 2.4(b)]: The link inductance resonates with the link capacitance until the link voltage is equal to the reflected voltage of the mode-7 phase pair.

Mode 7 [Fig. 2.4(e)]: The two related switches of the chosen output phase pair for this mode are turned on to discharge the link inductance to these two phases. The switches are turned off after the link current reaches a small value, which will be discussed later. Considering the input-output power balance, the average currents of both connected phases meet their reference values at the end of this mode.

Mode 8 [Fig. 2.4(b)]: The link inductance and capacitance start to resonate. This partial resonance is allowed to run until the link voltage is equal to the lowest input line-to-line voltage, which then permits the converter to go to mode 9 with zero voltage switching. In order to ensure this process happens correctly, a certain amount of current should be left in the link inductance at the end of mode 7 so that the link voltage goes lower than the input negative peak line voltage during mode 8. Therefore, the link current at the end of mode 7 should be as follows:

$$i_L(t_7) = \sqrt{\frac{C_1+n^2C_2}{L_M}\left(V_{LP}^2 - {v_L}^2(t_7)\right)} \tag{2.2}$$

where t_7 is time at the end of mode 7, and V_{LP} is the pre-determined link peak voltage. V_{LP} can be selected 10% to 15% higher than the input peak line voltage.

Modes 9-16: These modes are similar to modes 1 through 8 with the link charges and discharges in the negative direction. As a result, the link inductance carries an ac current with a zero average value. Furthermore, as the link charges through the input and discharges to the

output twice in each link period, the ripple frequency of the input and output currents is twice the converter's link frequency, which in turn makes the input and output filters small.

The reverse power flow from the output to the input is completely possible by exchanging the output and input modes. In the reverse power direction, the link is charged from the output in modes 1 and 3 and discharged to the input in modes 5 and 7 and so on.

In the actual digital control implementation of the proposed resonant converter, there might be a delay in the turning on of the switches at the exact times stated above due to the discrete sampling and required processing time. In order to avoid this delay, the converter's switches can be turned on ahead of time in one direction while they are in the off-state voltages, and consequently, the switches start conducting when they become forward biased with zero voltage switching. For instance, mode-1 switches can be turned on in the forward direction when the link voltage reaches its positive peak value, and mode-3 switches can be turned on in the forward direction as soon as the mode-1 switches are turned off.

2.2.3. The Converter Analysis and Design

As the arrangement of the line and phase voltages of a three phase system changes periodically every *π/6 rad*, the first *π/6 rad* will be considered for the analysis of the proposed converter. In this interval, the phase pair *cb* has the highest input line-to-line voltage, and according to the converter's operation principle, this phase pair is applied to the link in mode 1. Thus, the link average voltage in mode 1 is given by,

$$V_{1,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} v_{cb}\, d(\omega t) = \frac{3\sqrt{2}}{\pi} V_{Li} \tag{2.3}$$

where V_{Li} is the input line rms voltage. The link average current in mode 1 is equal to the average current of phase *c* in this interval as follows:

$$I_{1,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} i_c d(\omega t) = \frac{3\sqrt{2}(\sqrt{3}-1)}{\pi} I_{Pi} \quad (2.4)$$

where I_{Pi} is the input phase rms current. Similarly, the phase pair *ab* has the second highest input line-to-line voltage and is applied to the link in mode 3. Thus, the link average voltage and current in mode 3 can be calculated from the following:

$$V_{3,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} v_{ab} d(\omega t) = \frac{3\sqrt{2}(\sqrt{3}-1)}{\pi} V_{Li} \quad (2.5)$$

$$I_{3,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} i_a d(\omega t) = \frac{3\sqrt{2}(2-\sqrt{3})}{\pi} I_{Pi} \quad (2.6)$$

The link voltage peaks to V_{LP} in mode 16 and then is equal to $V_{1,ave}$ at the end of this mode. Therefore, the average of the link current at the end of mode 16 can be given by,

$$I_{16} = \sqrt{\frac{C_1+n^2C_2}{L_M}\left({V_{LP}}^2 - {V_{1,ave}}^2\right)} \quad (2.7)$$

Note that *"I_x"* is defined as the average of the link current at the end of mode *"x"* and *"$I_{x,ave}$"* is defined as the average link current during mode *"x"* of the operation. By considering that the input current is equal to the average link current in mode 1, the average duration of mode 1 and also I_1 can be given by,

$$T_1 = -\frac{L_M I_{16}}{V_{1,ave}} + \sqrt{\left(\frac{L_M I_{16}}{V_{1,ave}}\right)^2 + \frac{L_M T I_{1,ave}}{V_{1,ave}}} \quad (2.8)$$

$$I_1 = \frac{V_{1,ave}T_1 + L_M I_{16}}{L_M} \quad (2.9)$$

where *T* is the average link period. Ignoring the small change of the link current in mode 2, a similar analysis gives the average length of mode 3 and I_3 as follows:

$$T_3 = -\frac{L_M I_1}{V_{3,ave}} + \sqrt{\left(\frac{L_M I_1}{V_{3,ave}}\right)^2 + \frac{L_M T I_{3,ave}}{V_{3,ave}}} \quad (2.10)$$

$$I_3 = \frac{V_{3,ave}T_3 + L_M I_1}{L_M} \quad (2.11)$$

Assuming a unity load power factor, the link average voltages, currents and time lengths in modes 5 and 7 can be found similarly from the following:

$$V_{5,ave} = -\frac{3\sqrt{2}(\sqrt{3}-1)}{n\pi} V_{Lo} \tag{2.12}$$

$$V_{7,ave} = -\frac{3\sqrt{2}}{n\pi} V_{Lo} \tag{2.13}$$

$$I_{5,ave} = \frac{3\sqrt{2}(2-\sqrt{3})n}{\pi} I_{Po} \tag{2.14}$$

$$I_{7,ave} = \frac{3\sqrt{2}(\sqrt{3}-1)n}{\pi} I_{Po} \tag{2.15}$$

$$T_5 = \frac{L_M I_6}{V_{5,ave}} + \sqrt{\left(\frac{L_M I_6}{V_{5,ave}}\right)^2 - \frac{L_M T I_{5,ave}}{V_{5,ave}}} \tag{2.16}$$

$$T_7 = \frac{L_M I_7}{V_{7,ave}} + \sqrt{\left(\frac{L_M I_7}{V_{7,ave}}\right)^2 - \frac{L_M T I_{7,ave}}{V_{7,ave}}} \tag{2.17}$$

where V_{Lo} is the output line rms voltage, I_{Po} is the output phase rms current, and I_6 and I_7 can be given by,

$$I_6 = \frac{-V_{7,ave} T_7 + L_M I_7}{L_M} \tag{2.18}$$

$$I_7 = \sqrt{\frac{C_1 + n^2 C_2}{L_M}\left({V_{LP}}^2 - {V_{7,ave}}^2\right)} \tag{2.19}$$

The average time length of modes 4 and 8 are given by,

$$T_4 = \sqrt{L_M(C_1 + n^2 C_2)}\left[\sin^{-1}\left(\sqrt{\frac{C_1 + n^2 C_2}{L_M}}\frac{V_{3,ave}}{I_{LP}}\right) + \sin^{-1}\left(\sqrt{\frac{C_1 + n^2 C_2}{L_M}}\frac{-V_{5,ave}}{I_{LP}}\right)\right] \tag{2.20}$$

$$T_8 = \sqrt{L_M(C_1 + n^2 C_2)}\left[\pi - \sin^{-1}\left(\frac{-V_{7,ave}}{V_{LP}}\right) - \sin^{-1}\left(\frac{V_{1,ave}}{V_{LP}}\right)\right] \tag{2.21}$$

where I_{LP}, the average of the link peak current, can be found by substituting (2.5) and (2.11) in (2.1). Modes 2 and 6 are very short and can be ignored. In addition, modes 9 to 16 are similar to modes 1 to 8 with a negative direction, so their average time lengths are the same.

The sum of the duration of all operating modes is equal to the average link period, T, which results in an implicit equation. Fig. 2.5 shows the average link frequency and link peak current by changing the output power, P_{out}, for different input line voltage values. As the figure shows, the link frequency and link peak current are completely dependent on the output power, and as the output power reduces, the link frequency increases while the link peak current decreases almost linearly. The input voltage value also affects the link frequency directly, and the increment of the input voltage will make the link frequency greater. Note that these main operating parameters of the converter, link frequency and link peak current, only depend on the amount of the output active power irrespective of the output reactive or apparent power values. The link frequency and link peak current at very low output power are given by,

$$f|_{P_{out}\approx 0} = \frac{1}{2\pi\sqrt{L_M(C_1+n^2C_2)}} \tag{2.22}$$

$$I_{LP}|_{P_{out}\approx 0} = \sqrt{\frac{C_1+n^2C_2}{L_M}}V_{LP} \tag{2.23}$$

Fig. 2.6 shows the average link frequency by changing the link inductance, L_M, at the different total effective link capacitance, $C_t = C_1 + n^2C_2$. According to the figure, the link inductance has a noticeable effect on the link frequency, and the decrease of the link inductance increases the resulting link frequency considerably. Therefore, the link inductance can be chosen properly to attain an appropriate average link frequency at the given input and output voltages, and output power. On the other hand, the total link capacitance value has a considerable impact on the duration of the resonant modes, which do not transfer any power. Thus, the link capacitor values can be as low as possible such that there is enough time in the resonant modes to turn on the next mode switches properly. Note that the link inductance and capacitance can be selected smaller as in [5] to reach a high link frequency. However, in

order to run the converter effectively in the digital control implementation, the link frequency should be much smaller than the sampling rate of the digital controller, about 40-50 times. This is the main practical limiting factor of the maximum link frequency. As shown later in the experimental results section, the sample time of the digital controller was 3.6μsec, and as a result, the link components were selected as such to set the link frequency at about 7kHz at full power. The link frequency can be moved higher, provided a faster controller is used.

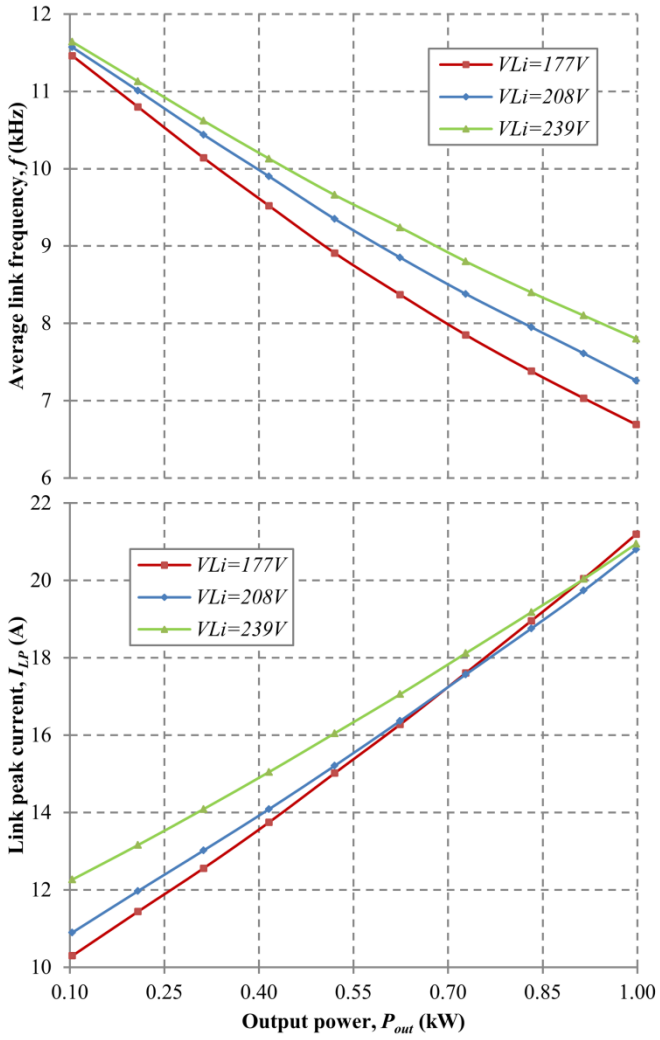

Fig. 2.5. Average link frequency and link peak current versus output power for various values of the input line voltage, V_{Lo}=208V, L_M=450μH, C_1=C_2=200nF, and n=1.

As the operating frequency of the transformer T_1 in the proposed scheme is the same as the link frequency, it yields a much smaller transformer compared to 50/60Hz transformers. In order to evaluate the impact of the frequency on the size of the transformer, the following formula can be used [27]:

$$W_a A_e = \frac{P_{out}}{K B_m f J_w} \tag{2.24}$$

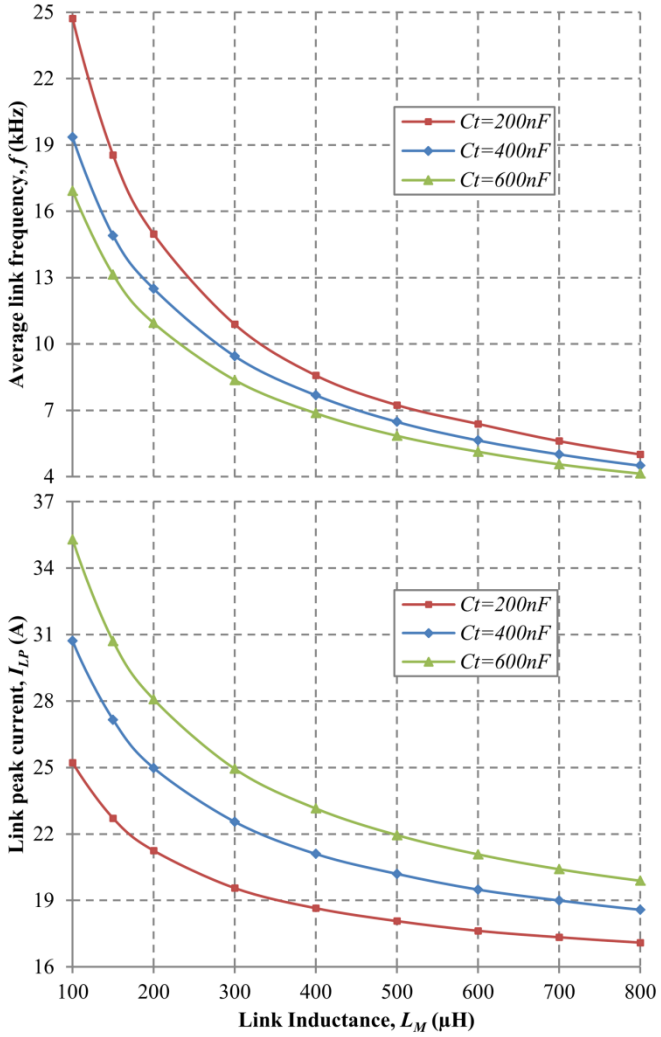

Fig. 2.6. Average link frequency versus link inductance for various values of the total effective link capacitance, V_{Li}=V_{Lo}=208V, P_{out}=1kW, and n=1.

where W_a is the core window area, A_e is core cross-sectional area, P_{out} is the output power, J_w is the wire current density, B_m is the maximum flux density, f is the operating frequency, and K is a constant. Eq. (2.24) clearly shows that as the frequency is increased, the required window area and core area product is decreased. In other words, the size of the transformer can be decreased dramatically by increasing the operating frequency of the transformer.

Although the converter can work properly in step-up and step-down operations with a 1:1 transformer, the turns ratio of the HF transformer can be selected optimally as follows:

$$n = \frac{V_{Lo}}{V_{Li}} \tag{2.25}$$

In this way, $V_{7,ave}$ becomes equal to $V_{9,ave}$, and the duration of modes 8 and 16, where do not transfer any power, can be minimized by the proper selection of V_{LP}. In addition, T_5 and T_7 as in (2.16) and (2.17) become equal to the T_3 and T_1 as in (2.10) and (2.8), respectively, and the link voltage and current waveforms become symmetrical.

2.2.4. Simulation Results

The proposed isolated resonant power converter was simulated for a 1.25kVA load at 0.8PF lagging. The input voltage was 208V/60Hz, and the output voltage was selected as 380V/50Hz. The transformer model parameters of Table 2.1 were employed in the simulation. As the transformer turns ratio was selected as 1.83 in accordance with (2.25), the link capacitors C_1 and C_2 were chosen as 200nF and 62nF respectively to have the same effective capacitances on the primary and secondary sides of the transformer. The simulation showed the average link frequency and link peak current at full load as 7.3kHz and 21A respectively, which are in agreement with the analysis results of the previous section as shown in Fig. 2.5. Note that according to (2.12) and (2.13), the reflected output voltages of

this simulation test are equal to the ones of Fig. 2.5. The absolute average and rms switch currents were estimated as 1.3A and 4.1A for the input-side switches and 0.7A and 2.4A for the load-side switches, respectively. The peak switch voltages in the forward and reverse directions were 330V for the input-side switches and 605V for the load-side switches. Fig. 2.7 shows the simulation results of the transformer primary and secondary voltages of the converter. As the figure shows, the transformer leakage inductances cause some ringing at the beginning of some operating modes, which are damped by the link capacitors and dissipated in the transformer winding resistances.

Table 2.1. The parameters of the designed HF transformer

Parameter	**Value**
Core shape	PM 74/59
Core material	N27 from EPCOS
Airgap length	3.8mm
Output-input turns ratio	1.83
Magnetizing inductance	430μH
Primary leakage inductance	1.85μH
Secondary leakage inductance	6.2μH
Primary winding resistance	53mΩ
Secondary winding resistance	177mΩ
Primary-secondary stray capacitance	784pF

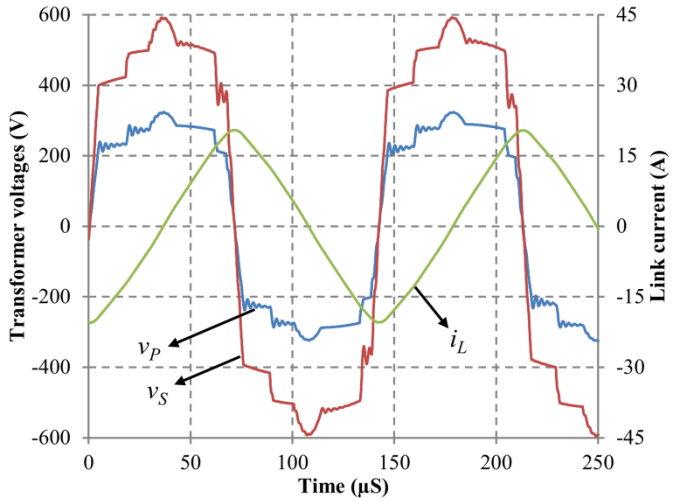

Fig. 2.7. Simulation results of the proposed converter at 1.25kVA, transformer primary and secondary voltage, and link current.

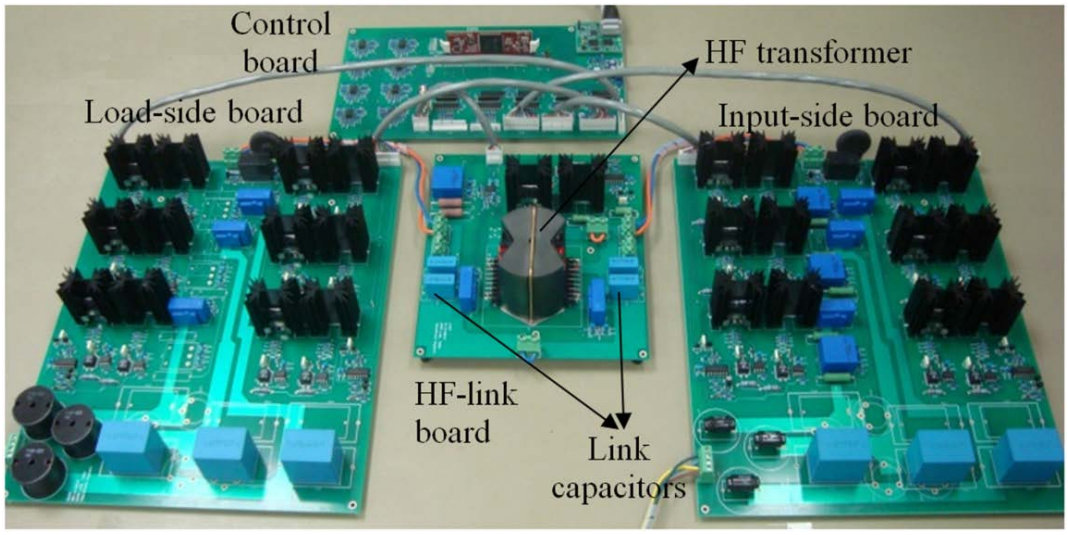

Fig. 2.8. The 1.25kVA experimental prototype of the introduced converter.

2.2.5. Experimental Results

A 1kW/1.25kVA prototype of the proposed converter topology was built to verify the operational principle, advantages, and performance. Fig. 2.8 shows the designed prototype.

TMS320F28335 Delfino DSC was employed to control the converter. The minimum reached sample time of the digital control was 3.6μs, which includes the ADC conversion time and the required processing time. Table 2.1 shows the model parameters of the designed HF transformer of this prototype. There are several issues to be carefully considered when designing the transformer as shown in Table 2.2. As the HF transformer has a considerable airgap length with a high-frequency ac current, the airgap fringing field can cause huge eddy current losses in adjacent coil conductors as Fig. 2.9 shows [28]. In order to avoid this issue, the immediate vicinity of the gap was prevented for winding and multi-stranded wires were employed. The converter was run at the same test conditions of the previous simulation section with the same link capacitors. The experimental results of the designed prototype for the 1.25kVA load at 0.8PF lagging are shown in Figs. 2.10-2.12, including the transformer voltages and link currents, and the converter's input and output currents. As expected, the three-phase input and output currents are symmetrical, which means that the converter is properly following the input and output reference currents using the described switching algorithm. Note that the input voltage waveforms were "flat-topped", which has been reflected into the input currents as Fig. 2.12 shows; however, the output waveforms in Fig. 2.12 are completely sinusoidal. The average link frequency and link peak current at these test conditions were about 6.9kHz and 22.1A respectively, which are very close to the results of the analysis and simulation sections. The small differences are mainly due to the non-linearity and power loss of the components.

Table 2.2. Design of the high-frequency air-gapped transformer with an ac current.

CONSTRAINTS	APPROACH
Core hysteresis and eddy current losses	• Use high-frequency materials, such as Ferrite, Amorphous, and Nanocrystalline
Copper loss	• Use of appropriate wire gauges
Skin effect	• Use multiple thin wire strands
Proximity effect	• Apply the interleaved winding • Use multiple thin wire strands
Leakage inductance	• Apply the interleaved winding • Use of pot-shaped cores
Stray capacitance	• Use thicker insulator between windings
Winding loss due to the fringing fields of the air-gap	• Use multiple thin wire strands • Avoid the area close to the air gap • Distribute the air gap (makes EMI if there is air gap in the outer bars of the core)

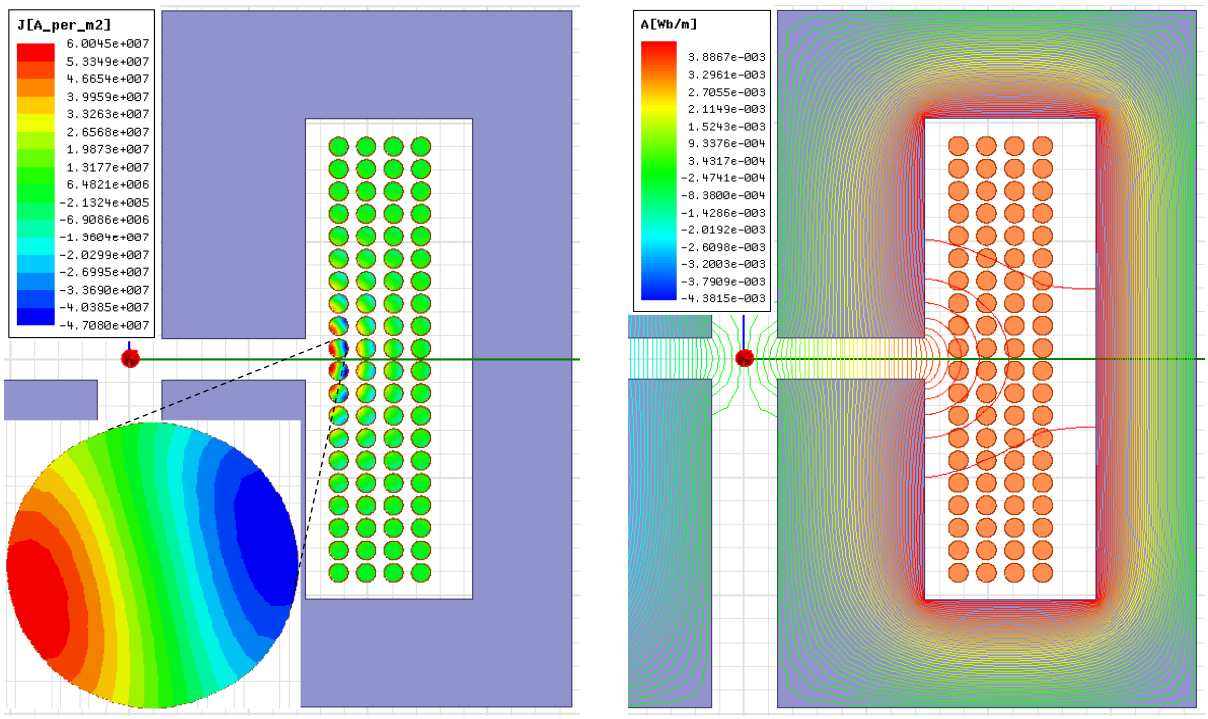

Fig. 2.9. FEA Analysis of the HF Transformer.

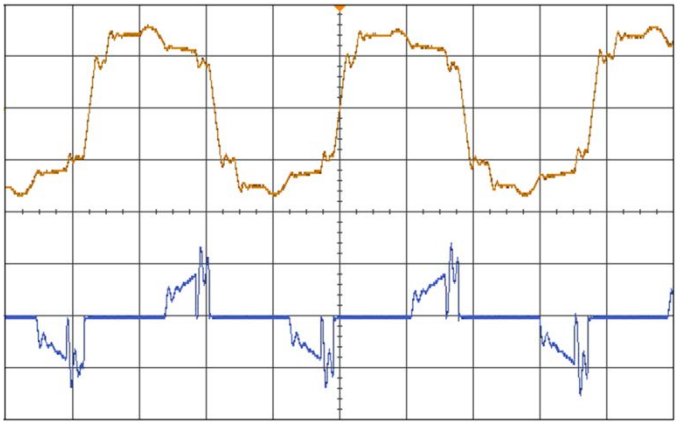

Fig. 2.10. Experimental results of the converter at 1.25kVA. Top: transformer primary voltage, v_p (200V/div), bottom: link input current, i_p (20A/div) versus time (40µs/div).

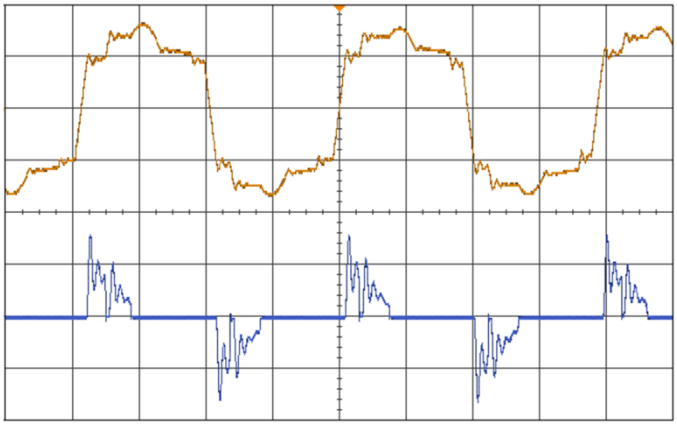

Fig. 2.11. Experimental results of the converter at 1.25kVA. Top: transformer secondary voltage, v_s (400V/div), bottom: link output current, i_s (20A/div) versus time (40μs/div).

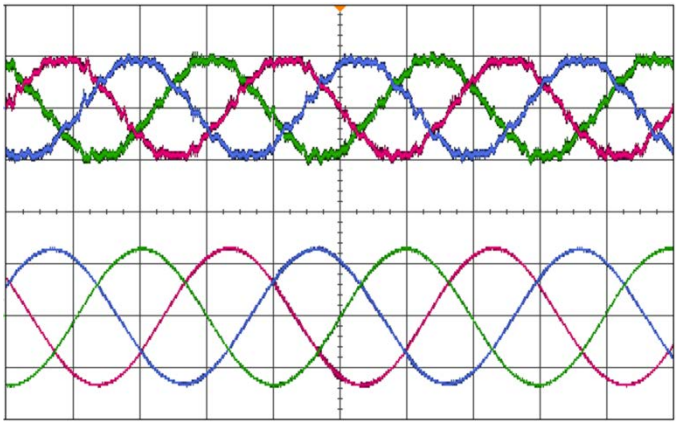

Fig. 2.12. Experimental results of the converter at 1.25kVA. Top: three-phase input currents (4A/div), bottom: three-phase output current (2A/div) versus time (5ms/div).

The experimental results of the current and voltage waveforms of an input-side bidirectional switch are shown in Fig. 2.13. As the figure shows, the switch voltage at both turn-on and turn-off is almost zero. Fig. 2.14 shows the conversion efficiency and input power factor of the designed converter versus output load for various values of the input line voltage. The measured efficiency and input power factor at full power were 94.3% and 0.97 leading respectively. The drift from unity in the input power factor is due to the impact of the

input LC filter, whose effect becomes more significant as the load power decreases. Note that the load power factor and output voltage values do not have any influence on the input power factor because there is no direct power transfer from the input to the output. More experiments showed that the input current harmonics of the developed prototype were in compliance with IEC/EN 61000-3-2 Class-A requirements, and the output harmonic voltages met IEC/EN 61000-2-2 standard. Furthermore, the thermal photography of the prototype converter working at the nominal operating conditions for 30 min. showed the transformer temperature below 60ºC and the temperature of the switches' heatsinks about 40ºC.

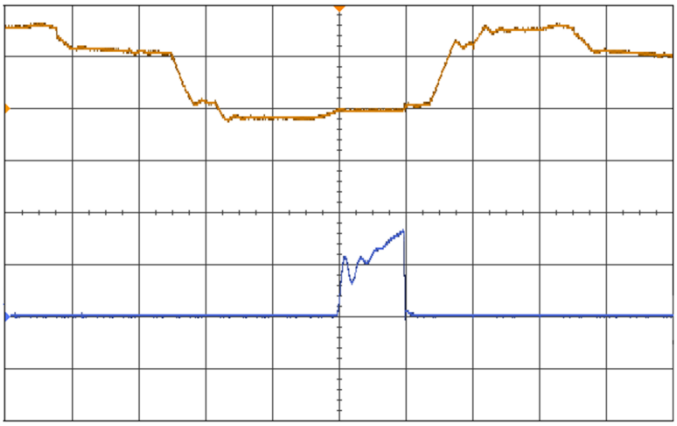

Fig. 2.13. Experimental results of an input-side switch. Top: switch voltage (200V/div), bottom: switch current (10A/div) versus time (20µS/div).

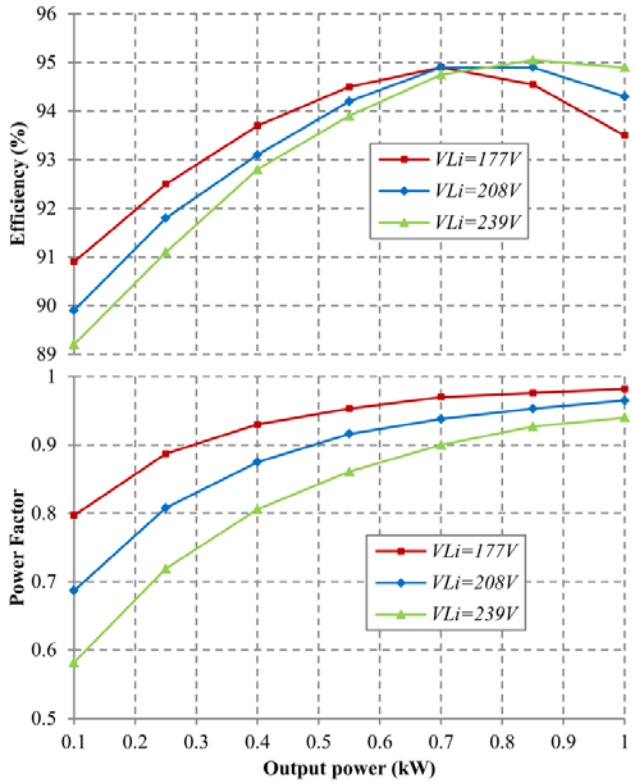

Fig. 2.14. Efficiency and power factor of the converter prototype versus output power for different values of the input line voltage.

2.3. Single-Stage Multi-String PV Inverter with an Isolated High-Frequency Link and Soft-Switching Operation

2.3.1. Introduction

The solar energy industry has grown rapidly over the past 20 years and is expected to be one of the most important alternative energy sources in the future. Photovoltaic (PV) inverters are integral parts of the solar energy systems since they collect the maximum possible power from PV cells for delivery to a utility grid or stand-alone loads. Different configurations of PV inverters have been proposed, which are mainly categorized as centralized, string, multi-string, and microinverter [29], [30]. In the centralized configuration, a number of PV modules are connected in series (called a PV string), and multiple PV strings

are connected to a main inverter using diodes [30], [31]. Although the large, centralized inverter offers economies of scale, this approach offers poor energy harvesting due to one centralized maximum power point (MPP) tracker for the whole system; partial shading or any mismatch between the PV modules causes substantial drop in the generated power output [32]. The microinverter solution employs the opposite approach by using a small inverter for individual MPP tracking of each PV module, maximizing possible energy harvesting [33]–[37]. Therefore, reducing or even losing the output of a single module due to partial shading or an inverter failure has a minimal impact on the overall system performance. However, the main drawback of the microinverter concept is a higher initial equipment cost per peak watt. This increased cost is due to the use of an inverter for each panel with much of the functionality of a centralized inverter [37]. In smaller PV systems, such as residential applications, the inverter price has less effect on the overall cost, and therefore, microinverters are the preferred solution. As the price of microinverters comes down, this technology will be more attractive in other applications.

String technology is another configuration for PV systems, where a string of PV modules is connected to a single inverter integrated with an MPP tracker [38]–[41]. Therefore, the string inverter can avoid most of the weaknesses of the centralized configuration. Nonetheless, the string technology has a power limit due to a limited number of series connections [42]. The multi-string solution is an enhanced version of the string topology and ensures optimum energy harvesting and cost [42]–[49]. In its conventional configuration, several strings are interfaced with their own MPP-tracked dc-dc converter to a common inverter as shown in Fig. 2.15 [43]. The multi-string approach allows the integration of strings with different features with respect to manufacturing technology, geographic

orientation, and number of modules per string. It also enables the enhanced operation of the PV systems in partial shading conditions when the PV strings are at different irradiance levels and operating temperatures [43]. The conventional multi-string PV topology has the disadvantage of poor conversion efficiency because of two stages of power conversion and the use of several bulky limited-lifetime electrolytic capacitors in the main dc link.

A new single-stage multi-string PV inverter with a high-frequency ac (HFAC) link and soft switching operation is introduced in this study based on the previous work on the isolated resonant HFAC-link ac-ac converters [5], [7]. Similar to the conventional multi-string topology, the proposed inverter can handle an arbitrary amount of PV strings with different electrical parameters and working conditions while obtaining the maximum possible power from each string independently. However, the proposed topology has a single stage of soft-switched power conversion with no electrolytic capacitor in the link. Therefore, this converter is expected to have an improved efficiency, high power density, and enhanced reliability. Furthermore, the new inverter has an HFAC link, so a small-sized high-frequency (HF) transformer has been employed to achieve galvanic isolation. As a result, the topology allows double grounding on both of its sides in accordance with the NEC 690 standard.

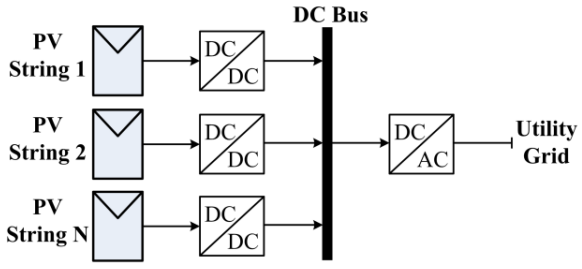

Fig. 2.15. The conventional multi-string configuration.

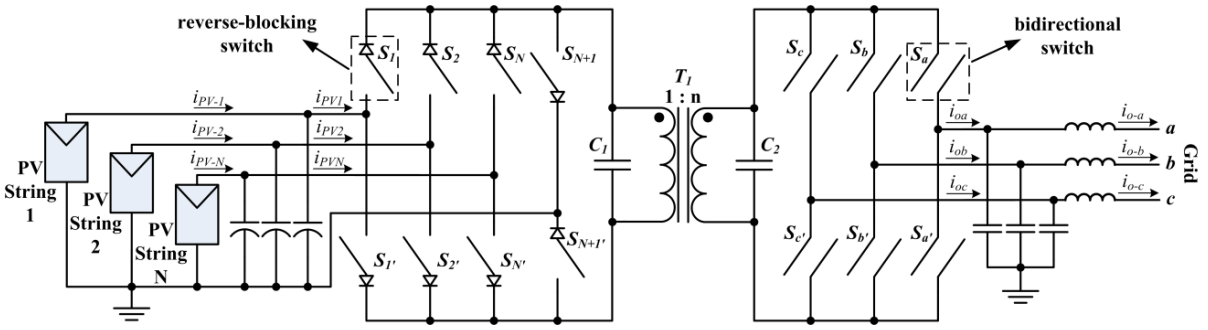

Fig. 2.16. The soft-switched HFAC-link N-string PV inverter.

2.3.2. The Proposed Multi-String PV Inverter

The soft-switched multi-string PV inverter with an HFAC link is shown in Fig. 2.16. The number of the input PV strings as well as their characteristics, operating voltages, and power levels are completely arbitrary. The proposed inverter can individually collect the maximum possible power of each string regardless of its location, orientation, irradiation level, or operating temperature. Galvanic isolation is realized by the HF transformer T_1. This transformer works at the switching frequency of the converter; therefore, it is much smaller than the 50/60Hz isolation transformers. The magnetizing inductance of the HF transformer, L_M, along with the small ac capacitors C_1 and C_2 form the HFAC link of the multi-string PV inverter. In order to have a proper inductance value, the transformer may need to have an air gap. The transformer's magnetizing inductance, which is considered as the link inductance, is the main element for handling power from the PV strings to the grid. The link capacitors, C_1 and C_2, generate partial resonances to achieve soft-switching operation, as discussed later. These capacitors are placed on both sides of the transformer to also behave as passive snubbers. In this way, they provide paths for the leakage inductance currents of the transformer when the switches are turned off and avoid voltage spikes [5]. As the figure

shows, the proposed topology has six bidirectional switches at the grid side. At the PV side, the converter needs to have two reverse-blocking switches for each PV string in addition to two more reverse-blocking switches for the return leg. A reverse-blocking switch can be realized by a conventional IGBT or MOSFET in series with a diode. The newly available individual reverse-blocking switches can also be employed with the advantage of lower total on-state voltage. The bidirectional switches for the grid side of the inverter can be made by two conventional IGBTs or MOSFETs in anti-series or two reverse-blocking switches in anti-parallel. To suppress switching-frequency harmonics from the output and PV currents, a second-order low-pass filter is used in the grid side and a simple capacitor filter is employed in parallel with each PV string. The PV-string capacitors should be large enough to control the high-frequency ripple of the PV string currents, which is detrimental to MPPT accuracy. Electrolytic capacitors are well suited to control the ripple due to their low Equivalent Series Resistance (ESR) and high capacitance per volume. However, film capacitors can also be used for this purpose to achieve a higher level of reliability. Note that in Fig. 2.16, the unfiltered PV-side currents are referred as "i_{PV1}, i_{PV2}, and i_{PVN}" and the filtered PV-string currents are mentioned as "$i_{PV\text{-}1}$, $i_{PV\text{-}2}$, and $i_{PV\text{-}N}$". A similar method is used for the grid-side currents.

2.3.2.1. The Control Scheme and MPPT Operation

The detailed control scheme of the proposed multi-string PV inverter in the two-string case is shown in Fig. 2.17. This scheme can be easily extended to more number of PV strings. According to the figure, the proposed control scheme is composed of two sections: the reference current generator and the switch controller. The first section generates the

reference currents of the PV strings and output phases by using MPP trackers and a power calculator. These reference currents are sent to the switch controller section. In this section, the converter's switches are managed properly to meet the reference currents by means of a unique switching algorithm [5], which will be described in the next section of this study.

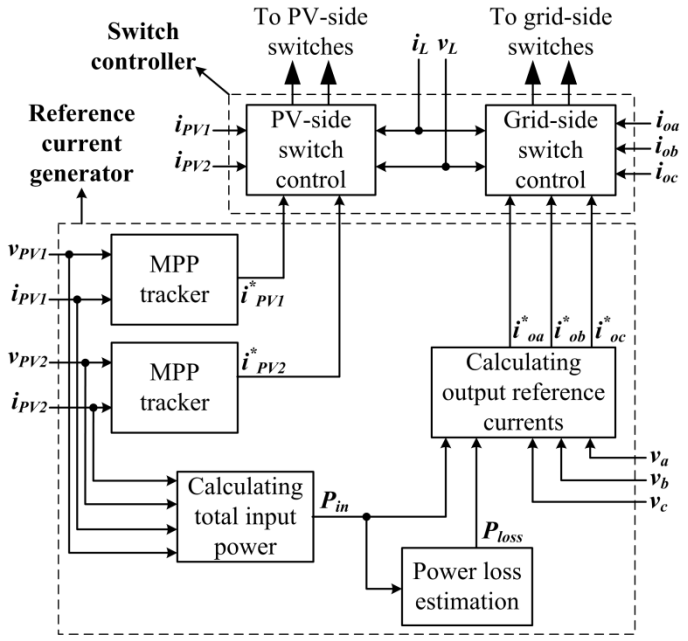

Fig. 2.17. Control scheme of the proposed multi-string PV inverter.

As Fig. 2.17 shows, PV strings 1 and 2, *PV1* and *PV2*, have independent MPP trackers. Each MPP tracker measures the voltage and current of its dedicated PV string constantly and calculates the PV reference current (i^*_{PV1} and i^*_{PV2}). Most of the available MPP tracking techniques can be employed in these MPP trackers to find the optimal PV reference currents properly, such as the perturb and observe (P&O), incremental conductance (IC), and beta methods [50]. In the P&O method, for example, the MPP tracker periodically increases

or decreases the reference current of the PV string by a small amount and measures its power. If the power increases, further adjustments are tried in that direction until the power no longer increases; otherwise, the operating point is changed in the opposite direction [50]. This process is carried out in all the other MPP trackers simultaneously to reach the maximum power point of all the connected PV strings independently.

The proposed topology is fundamentally a current-source converter and subsequently needs the reference currents of the output phases for the proper operation. As Fig. 2.17 shows, the output reference currents can be simply calculated according to the total input power resulting from the PV strings, P_{in}, and the estimated power loss, P_{loss}, as follows for phase *a*:

$$i_{oa}^{*}(t) = \frac{\sqrt{2}(P_{in}-P_{loss})}{\sqrt{3}V_{Lo}} sin(2\pi f_0 t) \tag{2.26}$$

where V_{Lo} is the output line rms voltage, and f_0 is the grid frequency. $i^{*}_{oa}(t)$ should be at the same phase of the grid voltage of phase *a* to have a unity power factor. The output reference current of phase *b* and *c* can be calculated similarly. According to Fig. 2.17, P_{in} can be found by calculating the instantaneous power of each PV string and adding them together. The inverter's power loss can also be estimated by knowing the input power. The power loss is normally much smaller than the input power, so the converter's operation is not sensitive to the accurate value of the power loss.

PV inverters are usually expected to operate at almost unity power factor without the possibility of regulating the voltage by exchanging reactive power with the grid. IEC 61727 is the only standard that limits the average power factor of PV inverter to be more than 0.9 lagging when the output is greater than 50%, but IEEE 1574 and VDE 0126-1-1 do not have any requirement. For high-power PV installations connected directly to the distribution level,

local grid requirements apply as they may participate in the grid control [51]. Eq. (2.26) was driven based on the proposed inverter operation at the unity power factor. However, the inverter has the ability to operate at a non-unity power factor in order to exchange reactive power with the grid. For this purpose, the phase angle and amplitude of the output reference currents can be controlled properly to reach the desirable power factor.

2.3.2.2. The Switching Algorithm of the Proposed Converter

The operation of the proposed soft-switched multi-string converter consists of several modes in each link cycle, depending on the number of PV strings. In short, the link inductance, L_M, charges through the PV strings one by one, and then, it discharges to the output phases in two discharge modes. There are resonant intervals between the charging and discharging modes to attain soft switching at both turn-on and turn-off for all the power switches. These partial resonances are caused by the inductance and capacitance of the HFAC link. Fig. 2.18 shows the link cycle of the proposed PV inverter in the two-string case. v_L and i_L are the voltage and current of the link inductance and are considered as the link voltage and link current. The converter modes of operation for two-string case are explained below. The described switching algorithm can easily be extended to a higher number of input PV strings. The transformer leakage inductances and winding resistances are ignored in the following and will be discussed later.

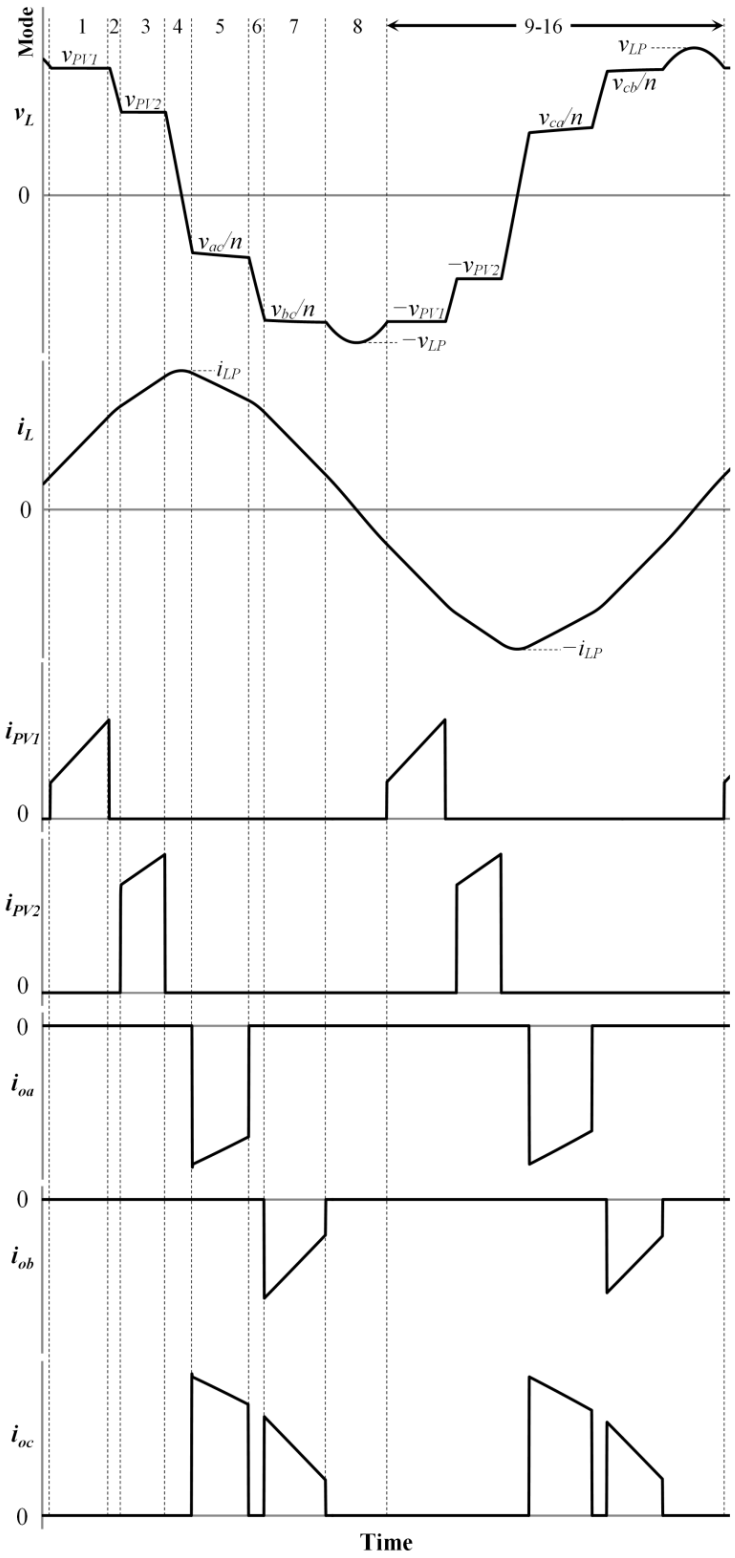

Fig. 2.18. Typical waveforms of the inverter at the instant that $v_{PV1}>v_{PV2}$, and $v_{cn}>0>v_{an}>v_{bn}$. (a) link voltage, (b) link current, (c-d) unfiltered PV-side currents, and (e-g) unfiltered grid-side currents.

Mode 1: Two PV-side switches are turned on to connect the PV string with the highest instantaneous voltage to the HFAC link in the positive direction. As a result, the link inductance starts to charge. This mode runs until the average current of the connected PV string meets its reference value. Subsequently, the switches are turned off. In Fig. 2.18, it is assumed that *PV1* voltage, v_{PV1}, is higher than *PV2* voltage, v_{PV2}. Therefore, *PV1* is connected to the link in mode 1.

In case that the irradiance level of *PV1* is zero, its MPP tracker selects I^*_{PV1}=0A. Assuming $v_{PV1}>v_{PV2}$, as soon as the converter goes to mode 1, the condition $I_1=I^*_{PV1}$ is already satisfied and the converter immediately goes to mode 2 (I_1=0A at the beginning of mode 1). Therefore, there is no mode 1.

Mode 2: The HFAC-link components, transformer's magnetizing inductance and parallel capacitors, resonates together. As a result, the link voltage, $v_L(t)$, drops initially. This resonance is allowed to continue until the link voltage is equal to the second-highest PV voltage.

Mode 3: The PV string with the second-highest voltage is connected to the HFAC link in the positive direction by turning on two input-side switches. In this mode, the link inductance continues to charge again. Once the average current of the connected PV string meets its reference value, the switches are turned off. As assumed before in Fig. 2.18, *PV2* has a lower voltage than *PV1*, so it is connected to the link in mode 3.

The described sequence of the PV strings for the link charging is important and should be followed flawlessly to operate the converter properly. If, for instance, the second-highest PV voltage is mistakenly connected to the link in mode 1, the link voltage will not reach the highest PV voltage during mode 2 (link voltage drops continuously during mode 2).

Note that the described charging procedure can be easily implemented in practice. At the beginning of mode 1, S_1, S_2, and $S_{3'}$ are turned on. Due to the unidirectional feature of the switches, the switches that are connected to the higher-voltage PV string start to conduct (S_1, and $S_{3'}$ in Fig. 2.18 where $v_{PV1}>v_{PV2}$). Once the average current of *PV1* meets its reference value, switch S_1 is turned off and the link resonates until the link voltage equals the lower PV voltage. Then, switches S_2, and $S_{3'}$ start to conduct softly and will be turned off after *PV2* reference current is met. This procedure is applied for the grid-side switches in a similar way.

Mode 4: The link inductance and capacitance are allowed to resonate again until the link voltage is equal to the reflected voltage of the selected output phase pair, which will be discussed later. During this mode, the link voltage passes zero in the negative direction, which indicates that the link current, $i_L(t)$, reaches its positive peak value. The link peak current can be calculated according to the total energy in the link components at the end of mode 3 as follows:

$$i_{LP} = \sqrt{{i_{E3}}^2 + \frac{C_p}{L_M}{v_3}^2} \tag{2.27}$$

where *"v_x"* is the link voltage during mode *"x"* ($v_3=v_{PV2}$ in Fig. 2.18), and *"i_{Ex}"* is the link current value at the end of mode *"x"*. C_p is the total link capacitance seen from the primary side of the transformer and is equal to $C_1 + n^2C_2$ by considering that n is the transformer output-input turns ratio.

The link inductance is properly charged by the PV strings up to this point, and now it should be discharged to the output phases. In order to meet all of the output reference currents in each link cycle, two discharge modes are considered, modes 5 and 7. In case that the inverter is designed for the unity power factor operation, the phase pair selection for these modes is straightforward: the output phase pair with the lowest instantaneous voltage is

chosen for mode 7 and the one with second-lowest instantaneous voltage is selected for mode 5. In this way, the link voltages in modes 1, 3, 5, and 7 are in descending order, and as a result, the resonant intervals between these modes are in the shortest possible case. As mentioned before, the proposed multi-string inverter can operate at a non-unity power factor to exchange reactive power with the grid by properly modifying the output reference currents shown in (2.26). In order to find the proper output phase pairs in this case, the priority is given to the instantaneous output reference current differences while their voltages are in the descending order. Therefore, the two output phase pairs that have lowest or second-lowest reference current differences at the instant are chosen for the discharging modes. Among these two phase pairs, the one with lower line-to-line voltage is chosen for mode 7 and the other for mode 5.

Mode 5: Two grid-side switches are turned on to discharge the link inductance stored energy to the chosen output phase pair for this mode. The switches remain on until the average current of one of the connected output phases meets its reference value. Then, the switches are turned off.

Mode 6: The link inductance and capacitance resonate until the link voltage reaches the reflected voltage of the selected phase pair for mode 7.

Mode 7: The related switches of the chosen output phase pair for this mode are turned on, which makes the link inductance discharge to these phases. The switches are turned off after the link current reaches a small value, which will be discussed later. Considering the input-output power balance, the average current of the connected outputs meet their reference values at the end of this mode.

Mode 8: A partial resonance happens again by the link components. Note that the HFAC link will be connected to the highest-voltage PV string in the negative direction during mode 9 (so v_9 is equal to the negative of the highest PV-string voltage). Therefore, as Fig. 2.18 shows, the link voltage should resonate properly to softly reach v_9 in the up-going direction during mode 8. In case that v_7 is less than v_9, this process happens naturally. So, there is no need to leave any current in the link inductance at the end of mode 7 (i_{E7} can be selected as 0). However, when v_7 is more than v_9, i_{E7} should have a positive value to force the link voltage to go lower than v_9 during mode 8. In this case, i_{E7} can be given by,

$$i_{E7} = \sqrt{\frac{C_p}{L_M}\left({v_{LP}}^2 - {v_7}^2\right)} \tag{2.28}$$

where v_{LP} is the link peak voltage and is practically selected 10% to 15% more than the highest PV-string voltage. In order to implement this process in practice, the link current and voltage is measured consecutively. As soon as the link current reaches (2.28), the switches are turned off and the inverter goes to mode 8.

Modes 9-16: During these modes, the link inductance charges through the PV strings and discharges to the outputs in the negative direction. As a result, the link inductance carries an ac current with zero average. Additionally, as the link charges through the input and discharges to the output twice in each link cycle, the ripple frequency of the input and output currents is twice the link frequency of the inverter, which in turn makes the input and output filters small.

2.3.2.3. The Soft Switching Operation

As described in the previous section, the power switches of the proposed HF-link multi-string PV inverter are turned on at the beginning of the odd-numbered modes when the

link voltage is equal to the selected input or output voltage. As a result, all the power switches are turned on at zero voltage. In addition, due to the existence of the link capacitors, the link voltage changes slowly while the switches are turned off at the end of odd-numbered modes. Consequently, the switch voltages change slowly at their turn-off. If the link capacitors are large enough so that the change of the link voltage is much slower than the switch turn-off speed, the switches are turned off at zero voltage. This zero voltage switching (ZVS) at turn-off occurs for all the converter's switches accordingly.

The ZVS behavior at both turn-on and turn-off of the switches does not depend on the operating parameters of the proposed inverter, such as the working voltage and power of the PV strings, the grid voltage, and power factor; as long as the switching algorithm is properly working, ZVS is realized accordingly. Note that if the algorithm is not followed properly, the inverter might get damaged. For instance, if the mode-1 switches are turned on when the link voltage is lower than the highest PV-string voltage, the switches can break due to the created surge current.

2.3.3. The Converter Analysis and Design

In this section, the analysis of the proposed PV inverter with two PV strings is presented. The provided analysis method can be easily extended to a higher number of input PV strings. In this case, the link voltage peaks to v_{LP} in mode 16 and then is equal to v_1 at the end of this mode. Therefore, the average of the link current at the end of mode 16 can be given by,

$$I_{E16} = \sqrt{\frac{C_p}{L_M}\left({V_{LP}}^2 - {V_1}^2\right)} \tag{2.29}$$

Note that the parameters with capital letters are used to represent the average of the corresponding parameters that use lower case letters. Taking into consideration that the reference current of the highest-voltage PV string is equal to the average link current in mode 1, the average duration of mode 1, T_1, and I_{E1} can be expressed from the following:

$$T_1 = -\frac{L_M I_{E16}}{V_1} + \sqrt{\left(\frac{L_M I_{E16}}{V_1}\right)^2 + \frac{L_M T_{ave} I_1}{V_1}} \tag{2.30}$$

$$I_{E1} = I_{E16} + \frac{V_1 T_1}{L_M} \tag{2.31}$$

where *"I_x"* is expressed as the average of the link current during mode *"x"* and T_{ave} is the average period of the link cycle. I_1 is equal to the reference current of the connected PV string during mode 1. As mentioned before, V_1, the link voltage in mode 1, is equal to the highest PV-string voltage. Ignoring the small link current change in mode 2, a similar analysis gives the average length of mode 3 and I_{E3} as follows:

$$T_3 = -\frac{L_M I_{E1}}{V_3} + \sqrt{\left(\frac{L_M I_{E1}}{V_3}\right)^2 + \frac{L_M T_{ave} I_3}{V_3}} \tag{2.32}$$

$$I_{E3} = I_{E1} + \frac{V_3 T_3}{L_M} \tag{2.33}$$

As mentioned in the switching algorithm of the proposed PV inverter, the second-lowest and lowest instantaneous grid line-to-line voltages are connected to the HFAC link during modes 5 and 7 at the unity power factor operation. However, these voltages change slightly during the course of an ac cycle. If the ordering of the line and phase voltages of a three phase system is considered, this arrangement changes periodically every *π/6 rad*. Therefore, the first *π/6 rad* is considered for the proposed inverter analysis. Phase pair *ba* has the second-lowest output voltage in this interval and is connected to the link in mode 5 by considering the unity power factor. Thus, the average of the link voltage in mode 5 can be given by,

$$V_5 = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} \frac{v_{ba}}{n} d(\omega t) = -\frac{3\sqrt{2}(\sqrt{3}-1)}{n\pi} V_{Lo} \tag{2.34}$$

As phase *b* is connected to the link in mode 7, the link average current in mode 5 is equal to the average reflected current of phase *a* in this interval as follows:

$$I_5 = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} n i_a d(\omega t) = \frac{3\sqrt{2}(2-\sqrt{3})n}{\pi} I_{Po} \tag{2.35}$$

where I_{Po} is the output phase rms current. Similarly, phase pair *bc* has the lowest output voltage, which is applied to the converter's link in mode 7. Therefore, the average of the link voltage and current in mode 7 can be expressed by,

$$V_7 = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} \frac{v_{bc}}{n} d(\omega t) = -\frac{3\sqrt{2}}{n\pi} V_{Lo} \tag{2.36}$$

$$I_7 = \frac{6n}{\pi}\int_0^{\frac{\pi}{6}} n i_c d(\omega t) = \frac{3\sqrt{2}(\sqrt{3}-1)n}{\pi} I_{Po} \tag{2.37}$$

With the average link voltage and current of modes 5 and 7 stated above, the average durations of modes 5 and 7 can be similarly given by,

$$T_5 = \frac{L_M I_{E6}}{V_5} + \sqrt{\left(\frac{L_M I_{E6}}{V_5}\right)^2 - \frac{L_M T_{ave} I_5}{V_5}} \tag{2.38}$$

$$T_7 = \frac{L_M I_{E7}}{V_7} + \sqrt{\left(\frac{L_M I_{E7}}{V_7}\right)^2 - \frac{L_M T_{ave} I_7}{V_7}} \tag{2.39}$$

where I_{E6} and I_{E7} can be given by,

$$I_{E6} = I_{E7} - \frac{V_7 T_7}{L_M} \tag{2.40}$$

$$I_{E7} = \sqrt{\frac{C_p}{L_M}\left({V_{LP}}^2 - {V_7}^2\right)} \tag{2.41}$$

The average time lengths of modes 4 and 8 are given by,

$$T_4 = \sqrt{L_M C_p}\left[\sin^{-1}\left(\frac{V_3}{I_{LP}}\sqrt{\frac{C_p}{L_M}}\right) - \sin^{-1}\left(\frac{V_5}{I_{LP}}\sqrt{\frac{C_p}{L_M}}\right)\right] \tag{2.42}$$

$$T_8 = \sqrt{L_M C_p}\left[\pi + \sin^{-1}\left(\frac{V_7}{V_{LP}}\right) - \sin^{-1}\left(\frac{V_1}{V_{LP}}\right)\right] \tag{2.43}$$

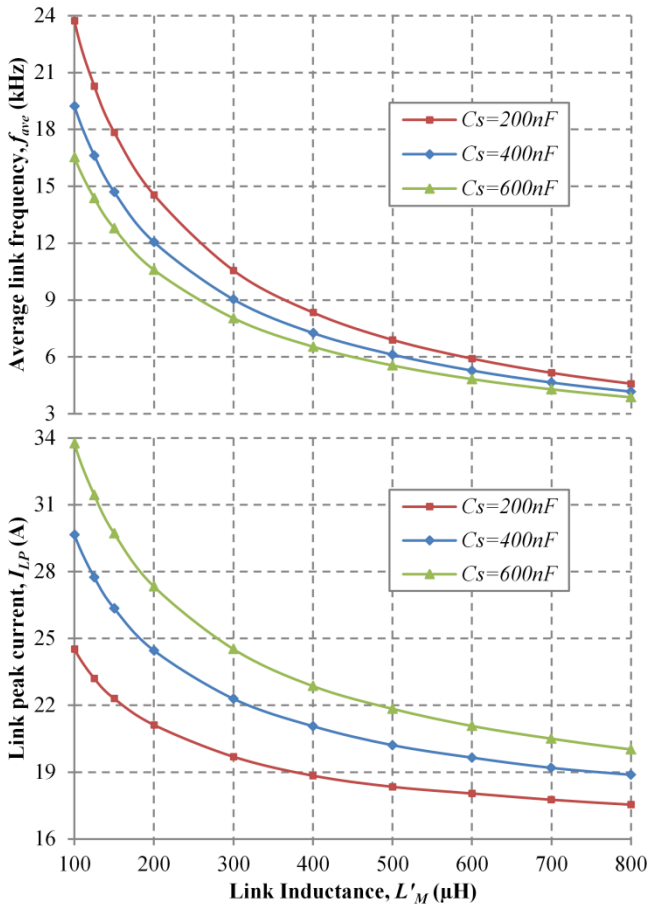

Fig. 2.19. Average link frequency and link peak current versus link inductance for different total link capacitance, V_{PV1}=150V, V_{PV2}=100V, V_{Lo}=208V, P_{PV1}=600W, P_{PV2}=400W, and n=1.8.

where I_{LP} can be found by substituting (2.33) in (2.27). The duration of the short modes 2 and 6 can be found in a similar way. Modes 9 through 16 are similar to modes 1 through 8 with a negative direction, and therefore, their average durations are the same. The sum of the time intervals of all operating modes is equal to the average link period, which results in a set of implicit equations that must be solved simultaneously. Fig. 2.19 shows the average link frequency and link peak current versus L'_M for the different values of C_s at the given

operating point. L'_M and C_s are the link inductance and total link capacitance seen from the secondary side of the transformer ($L'_M=n^2L_M$, and $C_s=C_2+C_1/n^2$). P_{PV1} and P_{PV2} are the delivering power of *PV1* and *PV2*. Note that the turns ratio of the transformer has been selected as 1.8 in Fig. 2.19, which will be discussed later. As the figure shows, the link inductance has a considerable effect on the link frequency, and the decrease of the link inductance increases the resulting link frequency considerably. The reason for this is that the decrease of the link inductance reduces the durations of the charging and discharging modes (see (2.30), (2.32), (2.38), and (2.39)) as well as the resonating modes (see (2.42) and (2.43)). In addition, the link peak current increases by the reduction of the link inductance, which can be verified by considering (2.27). On the other hand, the change of the link capacitance mainly affects the resonant mode durations according to (2.42) and (2.43), which results in a mild change of the link frequency. The dependency of the link peak current on the link capacitance can also be verified by observing (2.27).

The graph of the link frequency and peak current versus the link components for a given operating point (Fig. 2.19) can be used to design the proposed PV inverter for a desirable working condition. Note that the conduction loss of the switches and the transformer power loss depend on the link peak current; in order to decrease these losses, the link peak current should be reduced. The link frequency is also another important parameter determining the size of passive components, and therefore, it is desirable to increase the link frequency as much as possible. However, the link frequency should be much smaller than the sampling frequency of the inverter's digital controller to get enough samples in each link cycle to control the converter effectively. As shown later in the experimental results section, the sampling time of the digital controller was 3μsec. As a result, L'_M and C_s were selected as

450µH and 400nF to set the link frequency at about 7kHz for the given operating point. It should be noted that the digital controller's speed is the only main limiting factor of the link frequency, and by using a faster digital controller, the link frequency can be increased accordingly.

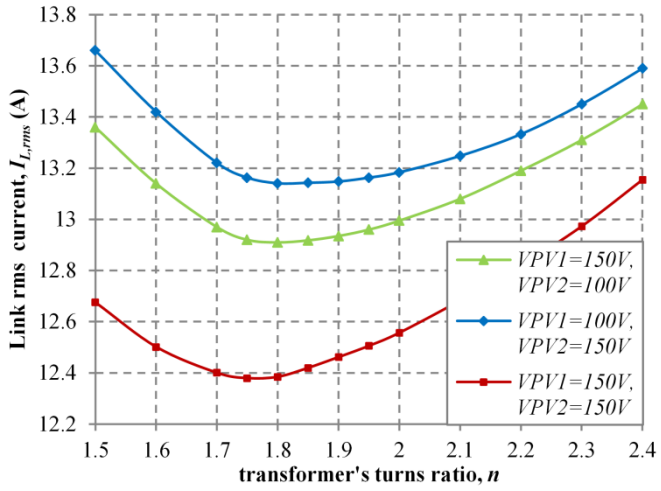

Fig. 2.20. Link rms current versus the transformer's turns ratio for different PV voltages, V_{Lo}=208V, P_{PV1}=600W, P_{PV2}=400W, L'_M=450µH, and C_s=400nF.

Although the proposed multi-string PV inverter can work effectively with a 1:1 HF transformer in both step-up and step-down operations, the transformer's turns ratio can be optimally selected for the best operation of the converter. Fig. 2.20 shows the link rms current versus the transformer's turns ratio for different PV voltages at the given operating point. As the graph shows, the link rms current, $I_{L,rms}$, reaches its lowest value when n is almost equal to 1.8 in the different PV voltage cases. This optimal turns ratio can be found by equating V_7 as in (2.36) with $-V_1$ ($n_{opt} \approx \frac{3\sqrt{2}V_{Lo}}{\pi V_1}$). The reason this happens is that by equating V_7 with $-V_1$, the duration of resonant modes 8 and 16 is minimized by the proper selection of

V_{LP}. In addition, T_7 become almost equal to T_9, and the link voltage and current waveforms become almost symmetrical. Fig. 2.20 also shows that the $I_{L,rms}$ drops by using higher PV-string voltages as expected.

Fig. 2.21 shows the average of the link frequency and link peak current versus the output power, P_{out}, for different PV-string voltages. The PV strings 1 and 2 are considered to deliver 60% and 40% of the output power respectively (it is assumed that they have the same shading degrees at each operating point). According to the figure, the link frequency depends on the output power, and the reduction of the output power increases the link frequency. The reason for this behavior is that by decreasing the PV power levels and output power, the input and output reference currents are reduced subsequently. As a result, the time-lengths of odd-numbered modes decline by considering (2.30), (2.32), (2.38), and (2.39). On the other hand, the link peak current drops by the reduction of i_{E3} as a result of output power drop in (2.27). Fig. 2.21 also shows how the link frequency and peak current change by the variations of the PV-string voltages as a result of the temperature change. Although the increment of the PV-string voltages at any given power increases the link frequency slightly, the change in the link peak current depends on the output power and PV-string voltages at the operating point of the converter. The link frequency and link peak current of the proposed multi-string at a very small output power can be given by,

$$f_{ave}|_{P_{out}\approx 0} = \frac{1}{2\pi\sqrt{L_M C_p}} \tag{2.44}$$

$$I_{LP}|_{P_{out}\approx 0} = \sqrt{\frac{C_p}{L_M}} V_{LP} \tag{2.45}$$

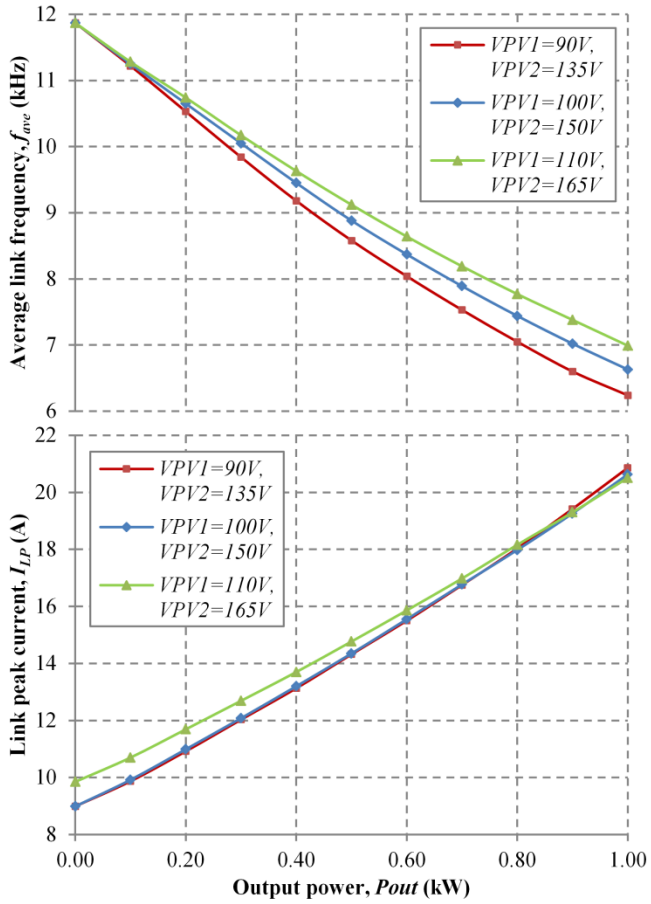

Fig. 2.21. Average link frequency and link peak current versus output power for different PV voltages, L'_M=450μH, C_s=400nF, V_{Lo}=208V, $P_{PV1}=0.6P_{out}$, $P_{PV2}=0.4P_{out}$, and n=1.8.

2.3.4. Experimental Results

To facilitate understanding of the operating principle and verification, a 1kW two-string prototype of the proposed HFAC-link PV inverter was fabricated. The sample time of the digital controller was 3μsec, which includes the ADC conversion time and the required processing time. An HF transformer with the turns ratio of 1.8 and the secondary-side magnetizing inductance of 450μH was designed using a ferrite pot core. Its total secondary-side leakage inductance and winding resistance was measured as 3.5μH and 103mΩ respectively. C_1 and C_2 were also selected as 680nF and 180nF respectively to have C_s of

about 400nF, while the effective capacitances on both sides of the transformer are almost equal. The grid voltage was 208V/60Hz. Two PV-string emulators were employed with the parameters shown in Table 2.3. In the first experiment, the PV-string emulators were adjusted at the STC (Standard Test Conditions). Fig. 2.22 shows the link current and the transformer primary voltage, which is almost equal to the link voltage. The link current was found by properly subtracting the currents of the transformer's primary and secondary currents. There is a limited ringing in the link voltage at the beginning of the odd-numbered modes, which is due to the leakage inductances of the HF transformer. The average link frequency and link peak current at these test conditions were about 6.84kHz and 20.2A respectively, which are very close to the analysis result shown in Fig. 2.20. The small differences are mainly a result of the power loss of the components. The filtered PV-string and output currents of the inverter are depicted in Fig. 2.23. The sum of the input power was almost 1kW in agreement with the data of Table 2.3. The measured efficiency and power factor were 95.1% and 0.97 respectively. The drift from unity in the power factor is due to the impact of the output filter and the discrete sampling time of the digital controller. In addition, the output current total harmonic distortion (THD_i) was about 1.5%, which is in compliance with IEEE 1574/IEC 61727 standards. Figs. 2.24 and 2.25 show the current and voltage waveforms of a PV-side and grid-side switch. As the figure shows, the voltages of the switches at their turn-on and turn-off are almost zero.

Table 2.3. Specifications of the Emulated PV Strings.

PV string specifications	**PV String 1**	**PV String 2**
Rated Maximum Power at STC, P_{max}	600W	400W
Open Circuit Voltage, V_{oc}	180V	120V
Maximum Power Voltage, V_{MPP}	150V	100V
Maximum Power Current, I_{MPP}	4A	4A
Short Circuit Current, I_{sc}	5A	4.9A
Temperature Coefficient of I_{sc}	+0.062%/℃	
Temperature Coefficient of V_{oc}	−0.330%/℃	
Temperature Coefficient of P_{max}	−0.450%/℃	

STC: Irradiance 1000W/m^2, Module Temperature 25℃, Air Mass 1.5

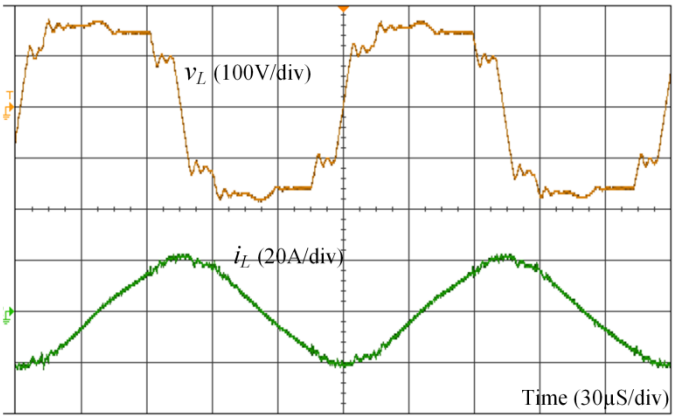

Fig. 2.22. Experimental results of the Inverter at STC. Link voltage, and link current.

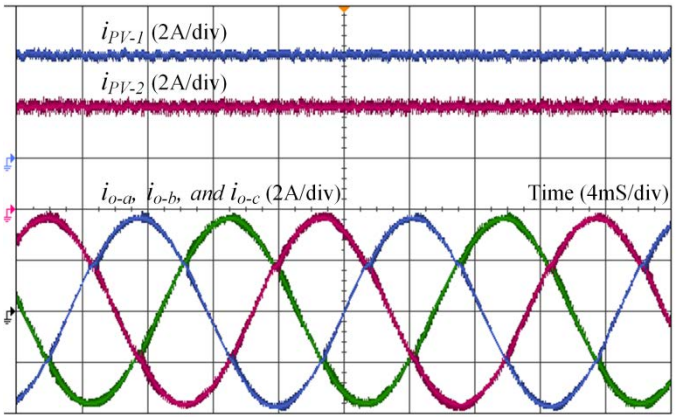

Fig. 2.23. Experimental results of the Inverter at STC. Filtered PV-string currents, and filtered output currents.

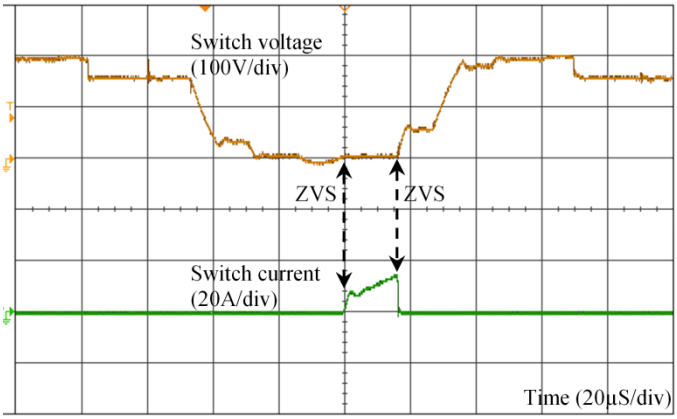

Fig. 2.24. Experimental results of a PV-side switch. Switch voltage, and switch current.

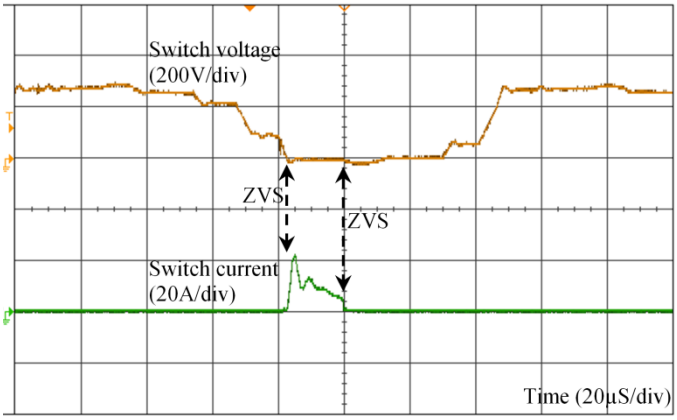

Fig. 2.25. Experimental results of a grid-side switch. Switch voltage, and switch current.

To verify the proposed inverter operation at different PV irradiance levels and temperature conditions, more experiments were run. Figs. 2.26 and 2.27 show the link voltage and current when the *PV1* irradiance level (IR_{PV1}) was set to 500W/m^2 and 0W/m^2, respectively, while *PV2* still works at the STC. As the figures show, mode 1 has shrunk in Fig. 2.26 and vanished in Fig. 2.27. This demonstrates that the MPP trackers are completely functional by adjusting the charging modes to reach the maximum power point for each string individually. The average link frequency in these tests was increased to 7.92kHz and 9.02kHz, respectively, while the link peak current was decreased to 16.6A and 13.1A respectively. The variation of the link peak current and frequency by changing the power is compatible with the analysis reasoning, as explained earlier. Table 2.4 and 2.5 summarize the analysis and experimental results of the proposed inverter operation at the described test conditions as well as more test conditions at different PV irradiance levels and temperatures.

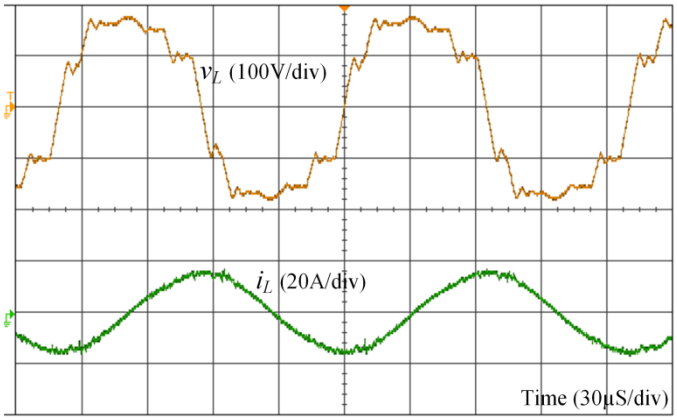

Fig. 2.26. Experimental results of the Inverter when IR_{PV1}= 500W/m^2 and IR_{PV2}=1000W/m^2. Link voltage, and link current.

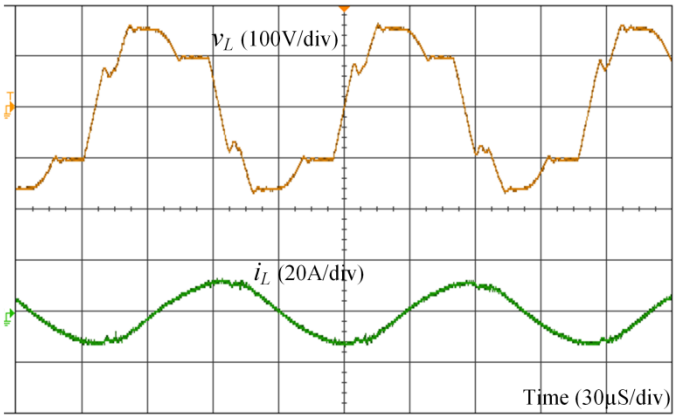

Fig. 2.27. Experimental results of the Inverter when IR_{PV1}= 0W/m^2 and IR_{PV2}=1000W/m^2. Link voltage, and link current.

Table 2.4. Results Summary of the Converter Operation for V_{Lo}=208V, and T_{PV1}=T_{PV2}=25℃.

PV Irradiance (W/m^2)		**PV power (W)**		**Link frequency (kHz)**		**Link peak current (A)**		**Effic-iency (%)**	**THD_i (%)**
PV1	***PV2***	***PV1***	***PV2***	**Ana.**	**Exp.**	**Ana.**	**Exp.**		
1000	**1000**	600	400	6.63	6.84	20.6	20.2	95.1	1.5
1000	**500**	600	204	7.62	7.86	17.8	17.4	95.4	1.9
500	**1000**	309	400	7.68	7.92	16.9	16.6	95.6	2.1
500	**500**	309	204	8.88	9.15	14.4	14.1	95.2	2.5
1000	**0**	600	0	8.79	9.06	15.3	15	95.0	2.4
0	**1000**	0	400	8.76	9.02	13.3	13.1	94.8	2.7

Ana.: Analysis, and Exp.: Experiment.

Table 2.5. Results Summary of the Converter Operation for V_{Lo}=208V, and IR_{PV1}=IR_{PV2}=1000W/m^2.

PV Temper-ature (°C)		**PV power (W)**		**Link frequency (kHz)**		**Link peak current (A)**		**Effic-iency (%)**	**THD_i (%)**
PV1	***PV2***	***PV1***	***PV2***	**Ana.**	**Exp.**	**Ana.**	**Exp.**		
25	**25**	600	400	6.63	6.84	20.6	20.2	95.1	1.5
25	**50**	600	355	6.69	6.90	20.1	19.7	95.1	1.5
50	**25**	533	400	6.69	6.92	19.7	19.3	95.2	1.6
50	**50**	533	355	6.75	6.95	19.2	18.8	95.2	1.7

Ana.: Analysis, and Exp.: Experiment.

The transient response of the multi-string converter by changing the irradiance levels of the PV strings can be observed in Fig. 2.28. The figure shows the PV string currents and the output current of phase *a* by changing the PV irradiance levels. The perturb and observe (P&O) algorithm was employed for the MPP tracking of the PV strings. In this figure, *PV1* and *PV2* were working with the irradiance levels of 500W/m^2 and 1000W/m^2, respectively, at the beginning. At t=0.3s, a step increase in the irradiance level was performed for *PV1* from 500W/m^2 to 1000W/m^2, and at t=0.7s, the *PV2* irradiation level was reduced to 500W/m^2. As the figure shows, the maximum power of each string was tracked properly without affecting the operating condition and control of the other string. The dynamic response is similar to the conventional converters employing the P&O algorithm [50].

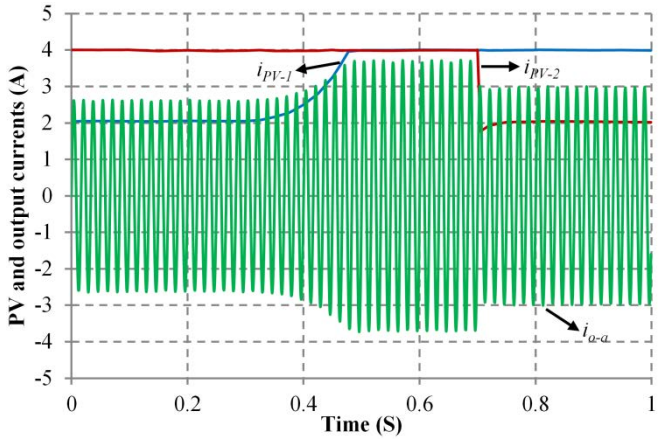

Fig. 2.28. The transient response of the converter by changing the irradiance levels of the PV strings.

3. THE TYPE-I REDUCED-SWITCH RESONANT HIGH-FREQUENCY AC-LINK CONVERTERS*

3.1. Introduction

The partial-resonant HFAC-link converters, presented in the previous section, transfer power twice in each link cycle by having 12 bidirectional or 24 unidirectional switches. Therefore, they are good candidates for high power applications. This section introduces a reduced-switch generation of the partial-resonant HFAC-link converters, which is suitable for low and medium power applications. Several applications of this topology are also presented [52]-[54]. In addition, as will be discussed in section 5, this topology may be used as an alternative to the original converter when one or more power switches are broken. As a result, a switch failure may not force the converter to shut down, and consequently system availability is improved.

3.2. Isolated ZVS High-Frequency-Link AC-AC Converter with a Reduced Switch Count

3.2.1. Introduction

A soft-switched isolated HF-link ac-ac converter for low and medium power applications is introduced in this study. 12 reverse-blocking switches and an air-gapped HF

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transformer are the major components of the proposed converter. This converter is able to provide arbitrary voltage and frequency to a load while having sinusoidal currents and a high power factor at the input side. Compared to the conventional ac-dc-ac converters, the proposed converter has the same number of switches with unique advantages, such as zero-voltage switching (ZVS), use of a small-sized HF transformer for galvanic isolation, step-up/down ability, and a high input power factor. The introduced converter is appropriate for low to medium power applications due to discontinuous input and output currents with considerable peak values. However, the use of faster microcontrollers can yield lower peak current values and higher power rating. Although the control scheme of the converter is rather involved, the topology is expected to have high reliability owing to the exclusion of short-life electrolytic capacitors, high efficiency as a result of soft switching operation, and high power density due to the use of an HF transformer for galvanic isolation. The initial cost of the proposed HF-link converter may be higher than the conventional PWM converters due to the use of high-frequency magnetic materials and a fast digital controller. However, the long life cycle and high efficiency of the proposed converter is expected to offset this initial cost.

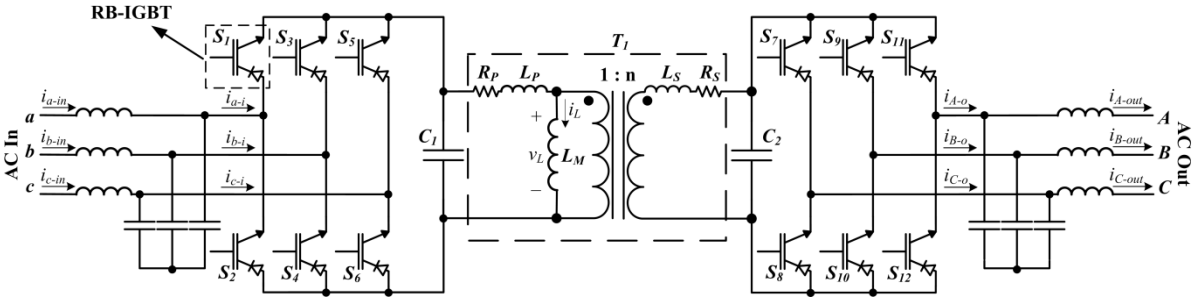

Fig. 3.1. The proposed ZVS isolated HF-Link three-phase ac-ac converter.

3.2.2. Topology Description

Fig. 3.1 shows the proposed soft-switched HF-link three-phase ac-ac converter. Galvanic isolation is realized by the HF transformer T_1. The HF link of the converter is formed by the magnetizing inductance of the transformer, L_M, and capacitors C_1 and C_2. These capacitors also act as passive snubbers and avoid voltage spikes due to the leakage inductances of the transformer when the input or output switches are turned off [7]. An air gap may be used in the design of the transformer T_1 to create a proper magnetizing inductance. As the figure shows, the converter employs 12 reverse-blocking IGBTs (RB-IGBT). The RB-IGBT has a symmetrical blocking voltage characteristic, which means that it can block both forward and reverse voltage in its off state. RB-IGBTs are now available in the market by IXYS and Fuji Electric. A series combination of a conventional IGBT and a diode can also make a reverse-blocking switch; nonetheless, individual RB-IGBT has the advantage of lower total on-state voltage. Although the converter's switches are unidirectional, the converter can transfer power in both forward and reverse directions conveniently as will be shown later. There are two low-pass filters at both ends of the converter to suppress high-frequency harmonics. It should be noted that if the galvanic isolation is not required, the HF-transformer can be easily replaced by an inductor and capacitors C_1 and C_2 can be merged. Power transfer from the converter's input to the output is achieved by the link inductance, L_M, by charging from the input phases and discharging to the output phases cycle-by-cycle. There is no direct power transfer from the input to the output. The link capacitors, C_1 and C_2, realize partial resonances between the charging and discharging modes to obtain soft-switching operation, as discussed later.

3.2.3. Principle of Operation

The proposed resonant HF-link converter is primarily a current-source converter and, as a result, the reference currents of the output phases are necessary in the control scheme. The reference currents of the input phases are also required in this converter's control scheme. The input reference currents can be calculated using the output power and the estimated power loss of the converter. For example, the input reference current of phase *a* can be given by,

$$i_{a-i,ref}(t) = \frac{\sqrt{2}(P_{out}+P_{loss})}{\sqrt{3}V_{Li}}\sin(\omega t) \tag{3.1}$$

where V_{Li} is the input line rms voltage, P_{out} is the output active power, and P_{loss} is the estimated power loss of the converter. The input reference currents of phases *b* and *c* can be calculated similarly. These reference currents should have the same frequency and phase angle respective to their corresponding input phase voltages to achieve a unity input power factor. The operation of the converter is not highly sensitive to the exact value of the power loss ($P_{out}>>P_{loss}$); however, to reach an accurate value of the power loss, both the input and output active powers can be measured frequently.

The introduced converter has eight modes of operation in each link cycle. The operating modes and link cycle of the converter are shown in Figs. 3.2 and 3.3. Basically, there are two modes for charging the link inductance from the input phases and two modes for the link inductance to be discharged to the output phases. In addition, there are four resonant modes between these active modes to create zero voltage switching at both turn-on and turn-off for all the converter's switches. The basic equivalent circuits of the proposed converter in different modes and the state-plane diagram of the converter are shown in Fig. 3.4. The converter modes of operation in the forward power flow are explained in detail as

follows by ignoring the effects of the transformer's leakage inductances and winding resistances. The effects of these elements will be shown later.

Mode 1 (charging): The HF link is connected to an input phase pair with the highest instantaneous voltage by turning on two proper input-side switches. Therefore, the link inductance, L_M, charges in the positive direction. This mode is allowed to run until the average current of one of the connected input phases meets its instantaneous reference value. The switches are turned off afterwards. Therefore, the connected phase with the smaller instantaneous reference current magnitude meets its reference current in this mode. The other connected phase will be linked to the HF link in mode 3 again to meet its reference value accordingly.

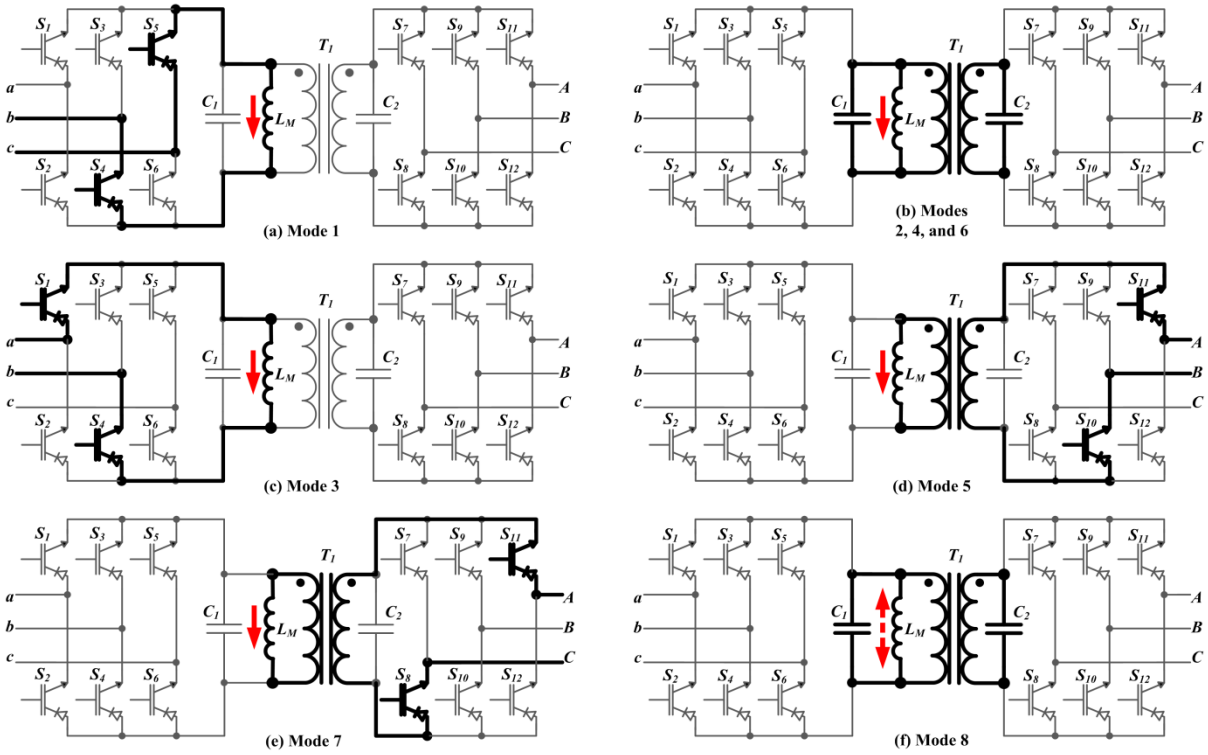

Fig. 3.2. The operating modes of the proposed isolated converter at the instant that $v_{cn}>v_{an}>0>v_{bn}$, $i_{C\text{-}o,ref}>i_{B\text{-}o,ref}>0>i_{A\text{-}o,ref}$, and $v_{CN}>v_{BN}>0>v_{AN}$.

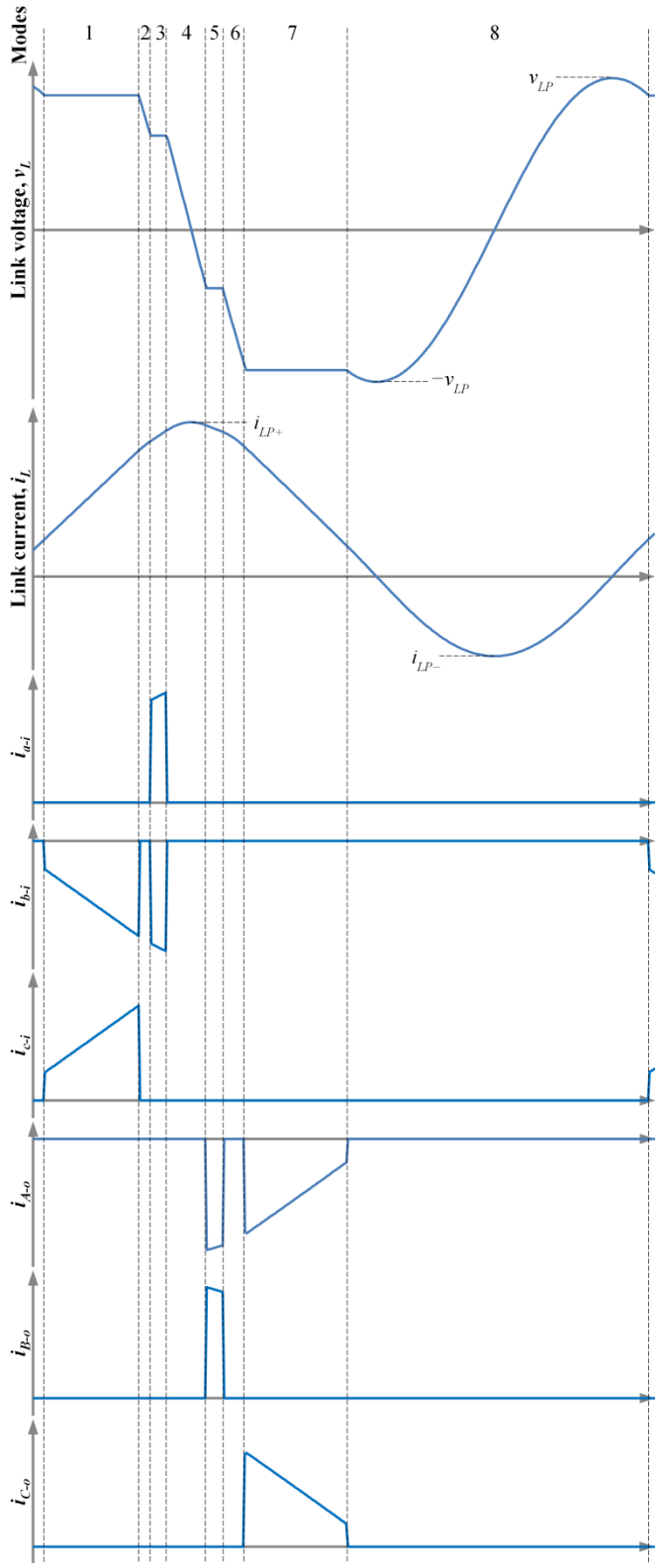

Fig. 3.3. The waveforms of the proposed isolated converter at the instant that $v_{cn}>v_{an}>0>v_{bn}$, $i_{C\text{-}o,ref}>i_{B\text{-}o,ref}>0>i_{A\text{-}o,ref}$, and $v_{CN}>v_{BN}>0>v_{AN}$. (a) link voltage, (b) link current, (c) input currents, (d) output currents, (e) switch commands.

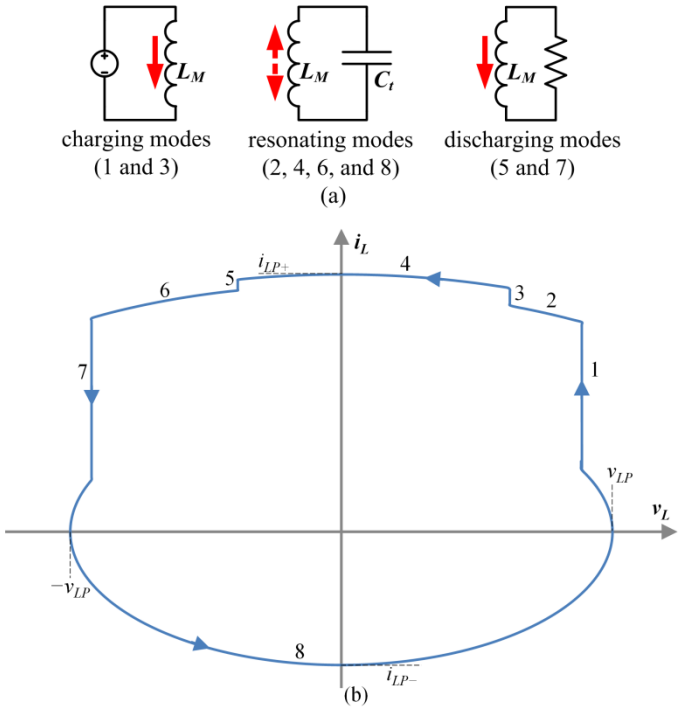

Fig. 3.4. (a) The basic equivalent circuits of the proposed converter in different modes, and (b) the state-plane diagram of the converter.

Owing to the existence of the link capacitors, the link voltage, $v_L(t)$, drops slowly when the mode-1 switches are turned off. As a result, the voltages of mode-1 switches increase slowly at their turn-off, which concludes that the switches are turned off at almost zero voltage. This zero-voltage turn-off occurs similarly for all the converter's other switches at all line and load conditions.

Mode 2 (partial resonance): The link inductance starts to resonate with its parallel capacitors, and the link voltage starts to drop. This partial resonance continues until the link voltage is equal to the second-highest instantaneous input line-to-line voltage.

Mode 3 (charging): Two input-side switches are turned on to connect the HF link to an input phase pair with the second-highest instantaneous voltage. The link inductance continues to charge in this mode until the average input current of the two connected phases

meet their instantaneous reference values. As the sum of the three phase currents is zero, these two phases meet their references simultaneously. Afterwards, the switches are turned off.

Note that the mode-3 switches are turned on as soon as the link voltage is equal to the second-highest input line-to-line voltage. Accordingly, the turn-on of the switches occurs at zero voltage. All the converter's switches are turned on at zero voltage in a similar way irrespective of the line and load conditions.

Mode 4 (partial resonance): By turning off the mode-3 switches, the link components start to resonate again. This resonance is allowed to continue until the link voltage is equal to the reflected voltage of the mode-5 phase pair. The proper selection of the mode 5 phase pair will be discussed later. During this mode, the link current, $i_L(t)$, reaches its positive peak value, i_{LP+}, which can be estimated according to the energy of the link at the end of mode 3 from the following:

$$i_{LP+} = \sqrt{{i_L}^2(t_3) + \frac{C_t}{L_M}{v_L}^2(t_3)} \tag{3.2}$$

where t_3 is the time at the end of mode 3, and C_t is the total link capacitance, which is equal to $C_1 + n^2C_2$ by considering that n is the transformer output-input turns ratio.

Two proper output phase pairs should be chosen for the discharging modes 5 and 7. As the load may have a non-unity power factor, the phase reference currents are considered for the selection of the output phase pairs (remember that for the selection of the input phase pairs in modes 1 and 3, phase pair voltages were considered since the input power factor was considered as one). Therefore, the two output phase pairs with the lowest and second-lowest reference current difference at the instant are chosen for the discharging modes. Among these two, the phase pair that has higher instantaneous voltage is chosen for mode 5 and the other

for mode 7. In this way, the link voltages in modes 3, 5, and 7 are in descending order, and as a result, the resonant intervals between these modes are in the shortest possible case.

Mode 5 (discharging): Two load-side switches are turned on at zero voltage to connect the HF link to the chosen output phase pair, discussed before. As a result, the link inductance starts to discharge to that phase pair. When the average current of one of the connected phases meets its instantaneous reference value, this mode ends and the switches are turned off. Similar to mode 1, the connected phase with the smaller instantaneous reference current magnitude meets its reference current, and the other connected phase will be linked to the HF link in mode 7 again to meet its reference value accordingly.

Mode 6 (partial resonance): The link components resonate together again until the link voltage is equal to the reflected voltage of the selected phase pair for mode 7.

Mode 7 (discharging): The switches corresponding to the chosen phase pair are turned on to connect the HF link to that phase pair. These switches are turned off after the link current reaches a small value, as will be defined later. Considering the input-output power balance, the average currents of the connected phases meet their reference values at the end of this mode.

Mode 8 (considerable resonance): The HF-link components resonate together again. This partial resonance runs until the link voltage becomes equal to the highest instantaneous input line-to-line voltage, and consequently, the converter goes to mode 1 with zero-voltage switching. For this procedure to occur appropriately, the link voltage should go higher than the input peak line voltage during this mode, which may require that a small amount of current be left in the link inductance at the end of mode 7 according to the following:

$$i_L(t_7) = \begin{cases} \sqrt{\frac{C_t}{L_M}\left(\left(\sqrt{2}kV_{Li}\right)^2 - {v_L}^2(t_7)\right)}, & |v_L(t_7)| < \sqrt{2}kV_{Li} \\ 0, & |v_L(t_7)| > \sqrt{2}kV_{Li} \end{cases} \quad (3.3)$$

where t_7 is time at the end of mode 7, and k is a constant, which can be chosen as 1.1−1.15. Eq. (3.3) ensures the link peak voltage, v_{LP}, to be equal or higher than $\sqrt{2}kV_{Li}$. As (3.3) indicates, in the case that $|v_L(t_7)|$ is lower than $\sqrt{2}kV_{Li}$, there should be a limited current in the link inductance at the end of mode 7 so that the link peak voltage is equal to $\sqrt{2}kV_{Li}$. However, when $|v_L(t_7)|$ is more than $\sqrt{2}kV_{Li}$, there is no need to leave any current in the link inductance at the end of mode 7, and link voltage peaks at $|v_L(t_7)|$ during mode 8 naturally (which is more than $\sqrt{2}kV_{Li}$).

The link current reaches its negative peak value, i_{LP-}, during mode 8, which can be given by,

$$i_{LP-} = -\sqrt{\frac{C_t}{L_M}}v_{LP} \quad (3.4)$$

The proposed control algorithm of the introduced ZVS HF-link converter can be easily implemented using a microcontroller. However, due to the discrete sampling and required processing time, a delay may appear in the turning on of the switches at the exact moments specified before. Although this delay is small, it results in hard-switching operation of the converter. To avoid this unwanted delay, the converter's switches can be turned on sooner in one direction while they are in the off-state voltages, and consequently, the switches start conducting when they become forward biased with zero-voltage switching. For instance, mode-1 switches can be turned on in the forward direction when the link voltage reaches its positive peak value, and mode-3 switches can be turned on as soon as the mode-1 switches are turned off. The positive zero crossing of the link current can be used as a sign to

find out when the link voltage reaches its peak value. In addition, note that the link frequency should be much smaller than the sampling rate of the microcontroller to get enough samples in each link cycle and run the converter effectively. This is the main practical limiting factor of the maximum allowable link frequency.

The reverse power flow from the output to the input is completely possible in the introduced converter. In order to do so, the input and output modes should be simply exchanged. In this way, the link inductance is charged from the output phases in modes 1 and 3, and is discharged to the input phases in modes 5 and 7 in a similar way.

3.2.4. Analysis and Design

The highest and the second highest instantaneous line-to-line voltages of the input and output change slightly over the course of an ac cycle; therefore, the link voltage and duration of each mode change slightly over the ac cycle, as well. For example, the mode-1 link voltage is equal to the highest instantaneous input line-to-line voltage, which can fall between $\sqrt{1.5}V_{Li}$ and $\sqrt{2}V_{Li}$. However, the arrangement of the line and phase voltages of a three phase system changes every *π/6 rad*. Therefore, the first *π/6 rad* will be considered for the analysis of the introduced converter. In this interval, phase pair *cb* has the highest instantaneous voltage, and as stated by the converter's operating principle, it is applied to the HF link during mode 1. As a result, the average link voltage of mode 1 can be given by,

$$V_{1,avg} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} v_{cb}\,d(\omega t) = \frac{3\sqrt{2}}{\pi}V_{Li} \tag{3.5}$$

Subsequently, the average link current of mode 1 is equal to the average current of phase *c* in this interval as follows:

$$I_{1,avg} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} i_c\,d(\omega t) = \frac{3\sqrt{2}(\sqrt{3}-1)}{\pi}I_{Pi} \tag{3.6}$$

where I_{Pi} is the input phase rms current. Phase pair *ab* has the second-highest instantaneous voltage and is applied to the HF link in mode 3. Therefore, the average voltage and current of the link in mode 3 can be given by,

$$V_{3,avg} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} v_{ab}\, d(\omega t) = \frac{3\sqrt{2}(\sqrt{3}-1)}{\pi} V_{Li} \tag{3.7}$$

$$I_{3,avg} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} i_a\, d(\omega t) = \frac{3\sqrt{2}(2-\sqrt{3})}{\pi} I_{Pi} \tag{3.8}$$

The link voltage peaks at v_{LP} during mode 8 and is equal to $V_{1,avg}$ at the end of this mode. Hence, the average of the link current at the end of mode 8 can be written as follows:

$$I_8 = \sqrt{\frac{C_t}{L_M}\left({V_{LP}}^2 - {V_{1,avg}}^2\right)} \tag{3.9}$$

where V_{LP} is the average of the link peak voltage. "I_x" is defined as the average of the link current at the end of mode "x" (note that "$I_{x,avg}$" was stated as the average link current during mode "x"). By employing the inductor principal relation to find the average of the link current in mode 1 and then equating it with $I_{1,avg}$, the average duration of mode 1, T_1, and I_1 can be given by,

$$T_1 = -\frac{L_M I_8}{V_{1,avg}} + \sqrt{\left(\frac{L_M I_8}{V_{1,avg}}\right)^2 + \frac{2L_M T I_{1,avg}}{V_{1,avg}}} \tag{3.10}$$

$$I_1 = \frac{V_{1,avg} T_1 + L_M I_8}{L_M} \tag{3.11}$$

where T is the average period of the link cycle. Ignoring the small change of the link current in mode 2, a similar analysis gives the average length of mode 3 and I_3 as follows:

$$T_3 = -\frac{L_M I_1}{V_{3,avg}} + \sqrt{\left(\frac{L_M I_1}{V_{3,avg}}\right)^2 + \frac{2L_M T I_{3,avg}}{V_{3,avg}}} \tag{3.12}$$

$$I_3 = \frac{V_{3,avg} T_3 + L_M I_1}{L_M} \tag{3.13}$$

Assuming a unity load power factor, the average of the link voltages, currents, and duration of operating modes 5 and 7 are similar to modes 3 and 1, respectively, and are given as follows:

$$V_{5,avg} = -\frac{3\sqrt{2}(\sqrt{3}-1)}{n\pi} V_{Lo} \tag{3.14}$$

$$V_{7,avg} = -\frac{3\sqrt{2}}{n\pi} V_{Lo} \tag{3.15}$$

$$I_{5,avg} = \frac{3\sqrt{2}(2-\sqrt{3})n}{\pi} I_{Po} \tag{3.16}$$

$$I_{7,avg} = \frac{3\sqrt{2}(\sqrt{3}-1)n}{\pi} I_{Po} \tag{3.17}$$

$$T_5 = \frac{L_M I_6}{V_{5,avg}} + \sqrt{\left(\frac{L_M I_6}{V_{5,avg}}\right)^2 - \frac{2L_M T I_{5,avg}}{V_{5,avg}}} \tag{3.18}$$

$$T_7 = \frac{L_M I_7}{V_{7,avg}} + \sqrt{\left(\frac{L_M I_7}{V_{7,avg}}\right)^2 - \frac{2L_M T I_{7,avg}}{V_{7,avg}}} \tag{3.19}$$

where V_{Lo} is the output line rms voltage, I_{Po} is the output phase rms current, and I_6 is given by,

$$I_6 = \frac{-V_{7,avg}T_7 + L_M I_7}{L_M} \tag{3.20}$$

I_7 can be found by substituting (3.15) in (3.3). The average lengths of mode 4 and 8 can be expressed by,

$$T_4 = \sqrt{L_M C_t}\left[\sin^{-1}\left(\frac{V_{3,avg}}{I_{LP+}}\sqrt{\frac{C_t}{L_M}}\right) - \sin^{-1}\left(\frac{V_{5,avg}}{I_{LP+}}\sqrt{\frac{C_t}{L_M}}\right)\right] \tag{3.21}$$

$$T_8 = \sqrt{L_M C_t}\left[2\pi + \sin^{-1}\left(\frac{V_{7,avg}}{V_{LP}}\right) - \sin^{-1}\left(\frac{V_{1,avg}}{V_{LP}}\right)\right] \tag{3.22}$$

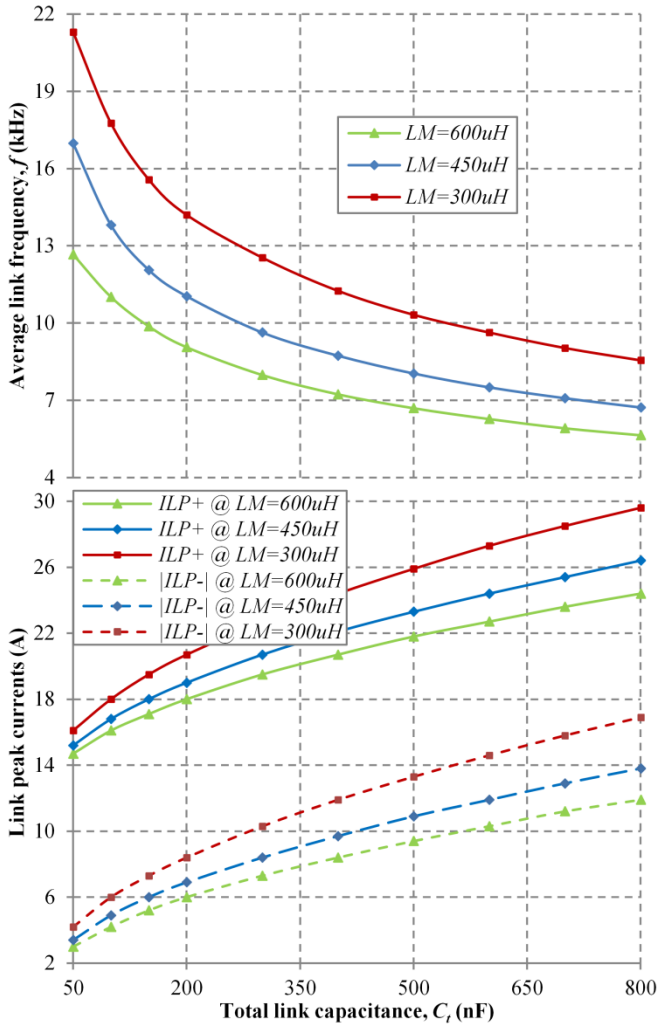

Fig. 3.5. The average link frequency and the magnitudes of the link current peak values versus total link capacitance for various values of the link inductance, V_{Li}=V_{Lo}=208V, P_{out}=750W, k=1.1, and n=0.9.

where I_{LP+}, the average of the link positive peak current, can be found by substituting (3.7) and (3.13) in (3.2). The duration of the short modes 2 and 6 can be found in a similar way. Finally, the sum of the time intervals of all the operating modes is equal to the average link period, T, which results in a set of implicit equations to be solved simultaneously. Fig. 3.5 shows the average link frequency, link positive peak current, and the absolute value of the link negative peak current versus the total link capacitance for various values of the link

inductance. According to the figure, as the link capacitance reduces, the magnitudes of the link current peak values decrease, which can be verified by considering (3.2) and (3.4). Note that the reduction of the total link capacitance also lessens the duration of the resonant modes (see (3.21) and (3.22)), where there is no transfer of power; consequently, $i_L(t_3)$ in (3.2) reduces as well. It is apparent that the average link frequency increases by lessening the resonant intervals as a result of reducing the total link capacitance. As Fig. 3.5 shows, these three mentioned parameters also depend on the link inductance value; the reduction of the link inductance increases the magnitudes of the link current peak values as well as the link frequency.

The link current peak values specify the conduction power loss of the switches and the transformer power loss; therefore, lowering the magnitudes of the link current peak values yields smaller power losses on the switches and transformer. In addition, it is desirable to increase the link frequency as much as possible to shrink the size of passive components. However, as mentioned before, the link frequency should be much smaller than the sampling rate of the converter's microcontroller. As shown later in the experimental results section, the sample time of the microcontroller was 3.5μsec, which includes the ADC conversion time and the required processing time. Therefore, the link inductance and capacitance were selected as 450μH and 400nF to set the link frequency at 8.7kHz at the given operating point. The link frequency can be moved higher, if a faster microcontroller is used. The transformer's turns ratio was selected as 0.9 in this analysis, which will be discussed later.

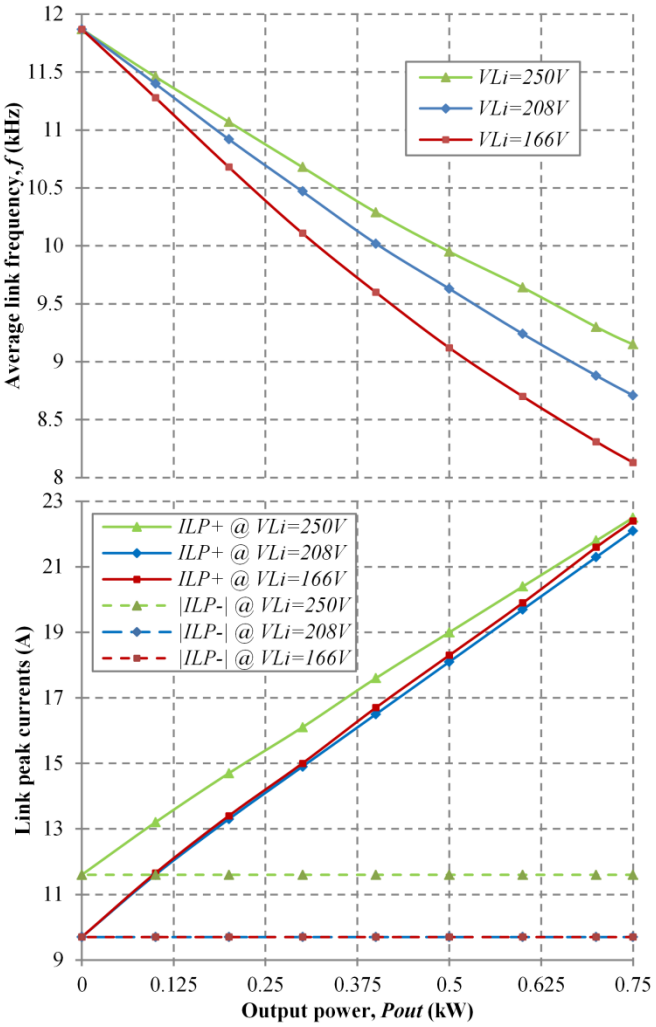

Fig. 3.6. The average link frequencyand the magnitudes of the link current peak values versus output power for various values of the input line voltage, V_{Lo}=208V, L_M=450µH, C_t=400nF, k=1.1, and n=0.9.

Fig. 3.6 displays the magnitudes of the link current peak values as well as the average link frequency versus the output active power for different input voltages. According to the figure, the link positive peak current is completely dependent on the output power, and as the output power reduces, I_{LP+} decreases almost linearly. The reason this occurs is that by decreasing the output power, the input reference current magnitudes should also reduce in accordance with (3.1). Therefore, the time-lengths of modes 1 and 3 (and also modes 5 and

7) decrease, which results in the reduction of $i_L(t_3)$ in (3.2) and consequently i_{LP+}. The decrease of the odd-numbered modes also results in the increase of the link frequency. Note that according to (3.4), i_{LP-} does not depend on the output power, but it may depend on the input voltage (v_{LP} is equal or higher than $\sqrt{2}kV_{Li}$). As Fig. 3.6 shows, the magnitudes of the link current positive and negative peak values become equal and non-zero at low output power, which means that there is a current circulation in the tank elements at their natural frequency. This current circulation decreases the converter's efficiency at light load. Decreasing C_t or increasing L_M helps in lowering the circulating current as (3.4) denotes.

The operating frequency of the HF transformer T_1 in the introduced topology is the same as the link frequency, which is selected to be much more than the input or output frequencies. Therefore, this transformer is much smaller than the conventional line-frequency isolation transformers. The proposed topology with a 1:1 transformer can operate in both step-up and step-down modes by properly adjusting the input and output reference currents. As Fig. 3.6 shows, the magnitudes of the link current peak values may increase due to the step-up/down operation (note that in Fig. 3.6 the output voltage is 208V constant while the input voltage varies from 166V to 250V). Therefore, the range of step-up/down operation is practically limited by the voltage and current ratings of the utilized switches. Although the converter can work in both step-up and step-down operations with a 1:1 transformer, the turns ratio of the HF transformer can be selected optimally. Fig. 3.7 depicts the graph of the link rms current versus the transformer's turns ratio for various values of the output power for equal input and output voltages. According to the figure, the link rms current reaches its lowest value in the nominal output power (750W) when n is almost equal to 0.9. The reason for this is that by decreasing the turns ratio from unity, $|v_L(t_7)|$ increases (remember that

$|v_L(t_7)|$ is normally equal to the output highest instantaneous line-to-line voltage divided by n). If $|v_L(t_7)|$ reaches $\sqrt{2}kV_{Li}$ in average, according to (3.3), there is no need to leave any current in the link inductance at the end of mode 7 and $V_{LP} = V_{7,avg}$. As a result, the mode-8 duration reaches its minimum value (note the second term in (3.22)), and the converter operates more efficiently. Decreasing n lower than the optimized value will increase $|v_L(t_7)|$ and v_{LP} more, which lengthens the mode-8 duration (note to the third term in (3.22)). It should be noted that the analysis results in Fig. 3.7 are based on equal input and output voltages. In the case that these voltages are not equal, the optimum turns ratio of the equal input-output voltage case should be multiplied by the output-input voltage ratio to get the same results.

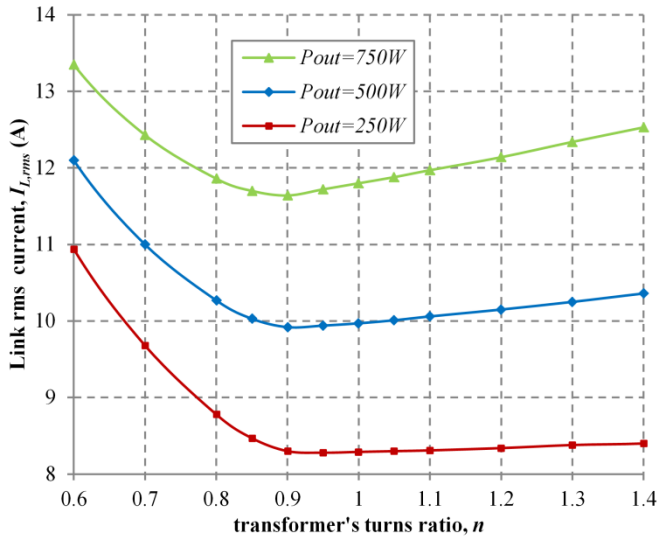

Fig. 3.7. Link rms current versus the transformer's turns ratio for various values of the output power, V_{Li}=V_{Lo}=208V, L_M=450µH, C_t=400nF, and k=1.1.

It can be shown that the peak forward and reverse voltage of the input-side switches, $PFRV_I$, and output-side switches, $PFRV_O$, are given by,

$$PFRV_I = \sqrt{\frac{2}{3}}V_{Li} + \frac{1}{2}V_{LP} \tag{3.23}$$

$$PFRV_O = \sqrt{\frac{2}{3}}V_{Lo} + \frac{1}{2}nV_{LP} \tag{3.24}$$

3.2.5. Simulation Results

The introduced partial-resonant ac-ac converter was simulated with the input of 208V/60Hz and output of 380V/50Hz for a 1kVA load at 0.75PF lagging. The transformer's turns ratio was selected as 1.64 ($= 0.9 \times \frac{380}{208}$ in accordance with Fig. 3.7). The magnetizing inductance and total link capacitance were 450μH and 400nF as selected in the previous section. In order to have almost the same effective capacitances on both sides of the transformer, the link capacitors C_1 and C_2 were chosen as 180nF and 82nF, respectively. The total leakage inductance and winding resistance of the transformer was considered as 3.7μH and 110mΩ, respectively (same as the values of the designed HF transformer in the prototype converter). Fig. 3.8 shows the simulation results of the link voltage and current at these test conditions. The small oscillations in the link voltage at the beginning of the odd-numbered modes are due to the effect of the transformer leakage inductances, which are damped by the link capacitors and dissipated in the transformer winding resistances. The average link frequency, link positive peak current, and link negative peak current were measured as 8.73kHz, 22.1A, and −9.7A, respectively, which are in agreement with the analysis results as shown in Fig. 3.6. Note that according to (3.14) and (3.15), the reflected output voltages of this simulation test are equal to the ones of Fig. 3.6, and the output active power is also the

same (750W). Although the input and output frequencies are different, the results of Figs. 3.5−3.7 are still valid for different input and output frequencies as long as the link frequency is much more than the input and output frequencies.

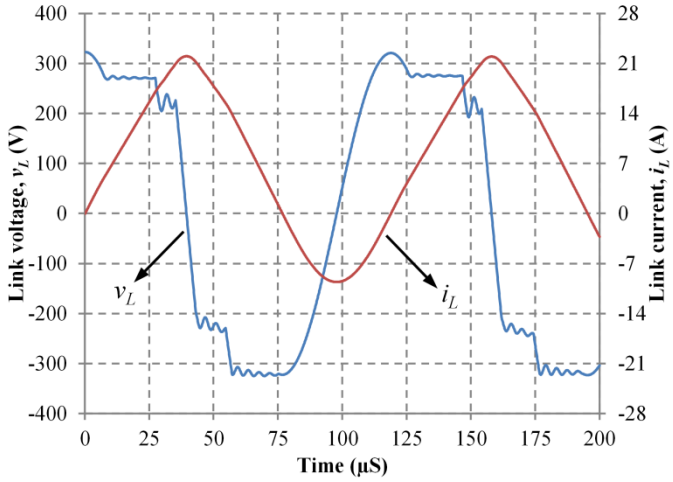

Fig. 3.8. Simulation results of the proposed converter at 1kVA. Link voltage and link current.

In order to filter out the high frequency harmonics from input and output waveforms, appropriate input and output low-pass filters were designed. Note that the input low-pass filter also affects the input power factor of the converter, and a stronger filter yields to a lower power factor. Therefore, a compromise should be made between the harmonic contents of the input currents and the input power factor when designing the input filter. The simulation results of the input and output currents of the converter are shown in Fig. 3.9. The input power factor was measured as 0.97 leading, which drifted from unity due to the effect of the input power filter. This verifies that although the load has a non-unity power factor (0.75 lagging), the input power factor of the proposed converter remains at almost unity. This

is due to the fact that there is no direct power transfer from the input to the output. The simulation also showed the average and rms currents of the converter's input-side switches as 0.9A and 3.7A and the average and rms currents of the load-side switches as 0.5A and 2.1A. In addition, the peak forward and reverse voltages of the input-side switches were expected as 330V while these values for the load-side switches were 580V.

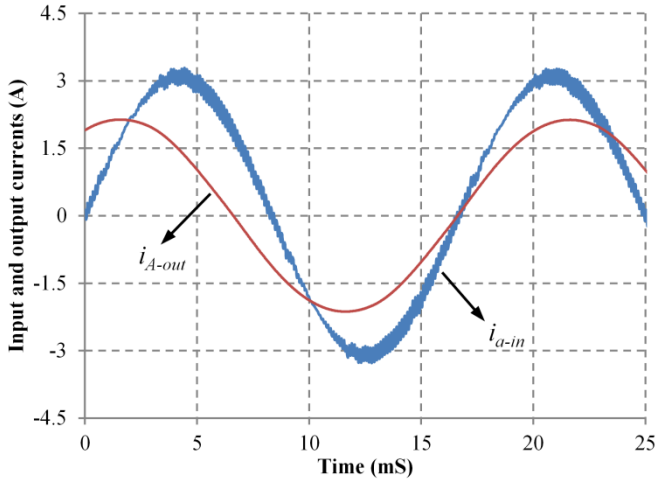

Fig. 3.9. Simulation results of the proposed converter at 1kVA. Input current of phase *a*, and output current of phase *A*.

Fig. 3.10 shows the current control transient response of the proposed converter. The converter was initially working at the nominal conditions (Input: 208V/60Hz, output: 380V/50Hz, and load: 1kVA at 0.75PF lagging). At t=20ms, the output reference currents were reduced by half, which led to the output power decrease by 25%. Due to the inductive behavior of the load and the existence of the output and input filters, it took a short interval until the converter reached the new steady state condition. Note that the input currents also contain the input filter capacitor currents, whose effect become more significant as the load

power decreases. At t=60ms, the output reference currents were changed to its nominal value, and the converter quickly returned back to its nominal steady state condition.

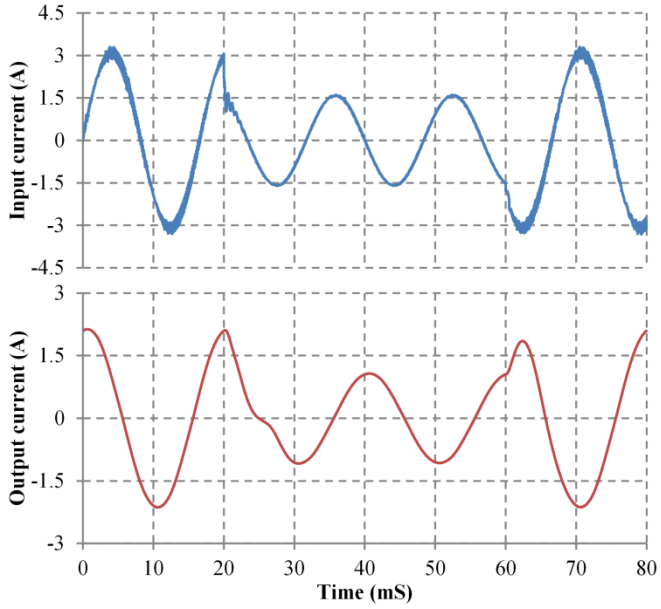

Fig. 3.10. Current control transient response of the proposed converter. (a) Input current of phase *a*, and (b) output current of phase *A*.

Since the highest and second-highest instantaneous input and output voltages change slightly over the course of the ac cycle, the durations of charging and discharging modes also change slightly over the ac cycle. As a result, the link frequency also varies slightly (less than 5% at the nominal conditions) in the course of the ac cycle. The normalized harmonics (FFT spectrum) of the link voltage is shown in Fig. 3.11. As the figure shows, the spectrum contains sideband harmonics, which are due to the slight fluctuation of the link frequency. In the designed converter, the link frequency was selected as about 8.7kHz at the nominal conditions; therefore, it generates audible noise. However, if the link frequency is selected

well above the 20kHz such that all the sideband harmonics remain above 20kHz, the audible noise issue does not exist.

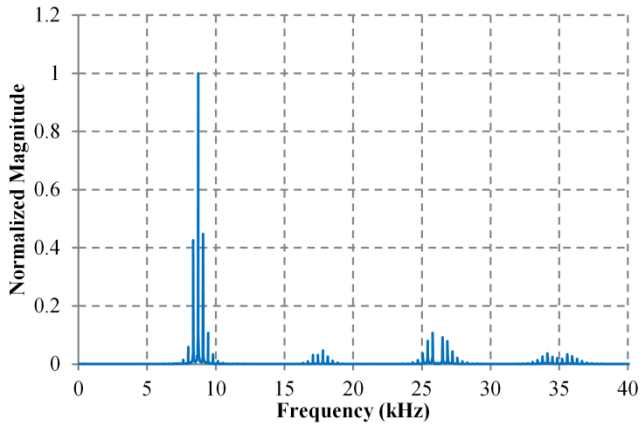

Fig. 3.11. FFT spectrum of the converter's link voltage at V_{Li}=208V, V_{Lo}=380V, P_{out}=750W, L_M=450µH, C_t=400nF, k=1.1, and n=0.9.

3.2.6. Experimental Results

In order to verify the effectiveness of the proposed ZVS HF-link ac-ac converter and the theoretical analysis, an experimental prototype with 1kVA power rating was built and tested. The reverse-blocking switches were realized by two IRG7PH42UD IGBTs in series, in which an IGBT is always off (to have more flexibility for running other similar converters). TMS320F28335 Delfino™ DSC was employed to control the converter. The minimum reached sample time of the digital control was 3.5µs, which includes the ADC conversion time and the required processing time. An HF transformer was built using the PM 74/59 ferrite core with the airgap length of 3.8mm to attain the magnetizing inductance of about 450µH and the turns ratio of 1.64. The transformer's primary and secondary numbers of turns were 37 and 61, respectively. Its total leakage inductance and winding resistance was

measured as 3.7μH and 110mΩ. As the HF transformer has a noticeable airgap length with a high-frequency ac current, the airgap fringing field can cause substantial eddy current losses in adjacent coil conductors [28]. In order to avoid this problem, the immediate vicinity of the airgap was prevented from winding and multi-stranded wires were employed. Consistent with the analytical and simulation sections, C_1 and C_2 were also selected as 180nF and 82nF, respectively. In the first test, the prototype converter was run with the input voltage of 208V/60Hz to supply a 380V/50Hz, 1kVA load at 0.75PF lagging, similar to the previous section. Fig. 3.12 shows the resulting link voltage and current, and Fig. 3.13 depicts the input and output currents of the converter. The average link frequency, link positive peak current, and link negative peak current at this test condition were about 8.35kHz, 22.8A, and −9.8A, respectively, which are very close to the results of the analytical and simulation sections. The small differences are primarily due to the non-linearity and power loss of the components. The measured efficiency and input power factor at full power were 94.7% and 0.97 leading, respectively. The current and voltage waveforms of an input-side switch are shown in Fig. 3.14. As the figure shows, the switch voltage at both turn-on and turn-off is almost zero.

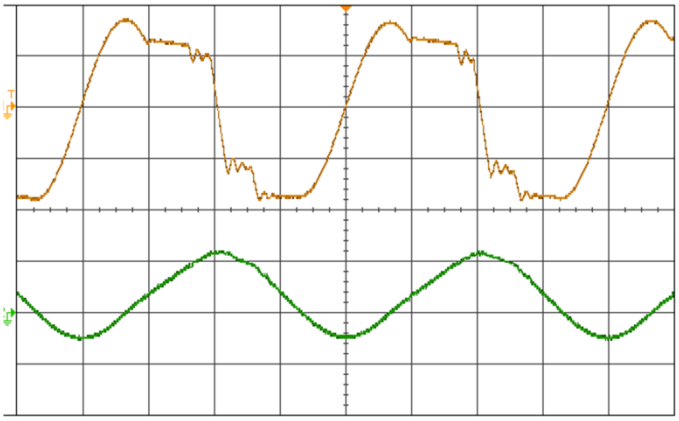

Fig. 3.12. Experimental results of the converter at 1kVA with 208V input. Top: link voltage, v_L (200V/div), bottom: link current, i_L (20A/div) versus time (30μs/div).

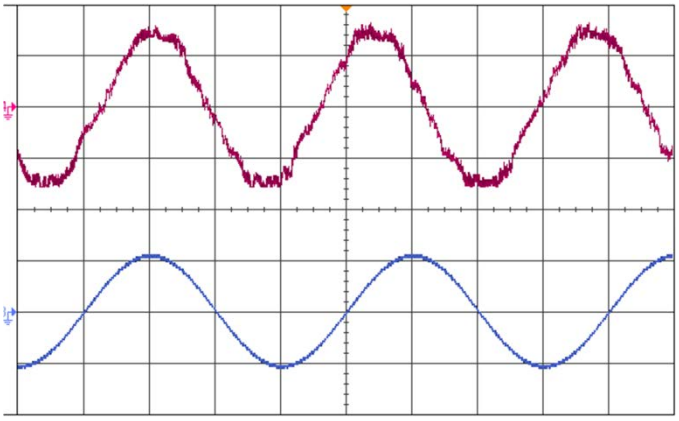

Fig. 3.13. Experimental results of the converter at 1kVA with 208V input. Top: input current of phase a, $i_{a\text{-}in}$ (2A/div), bottom: output current of phase A, $i_{A\text{-}out}$ (2A/div) versus time (5ms/div).

The prototype converter was also run with ±20% change in the input voltage to compare with the analytical results. Figs. 3.15 and 3.16 show the experimental results of the link voltage and current with the input of 166V/60Hz and 250V/60Hz, respectively. The load in both cases was 380V/50Hz, 1kVA at 0.75PF lagging, similar to the first experiment. The change of the input voltage can be revealed by observing the link voltages in modes 1 and 3, which are decreased in Fig. 3.15 and increased in Fig. 3.16. Note that the link current at the

end of mode 7 is zero with the input voltage of 208V and 166V (Figs. 3.12 and 3.15) while it is non-zero with the 250V input (Fig. 3.16) in consistent with (3.3). As a result, v_{LP} and $|i_{LP\text{-}}|$ are higher in Fig. 3.16. According to the experimental results, the link frequency modifies less than 7% by the 20% change in the input voltage, which is in agreement with the analytical results shown Fig. 3.6. The conversion efficiency of the designed converter versus output power for various values of the input line voltage is shown in Fig. 3.17.

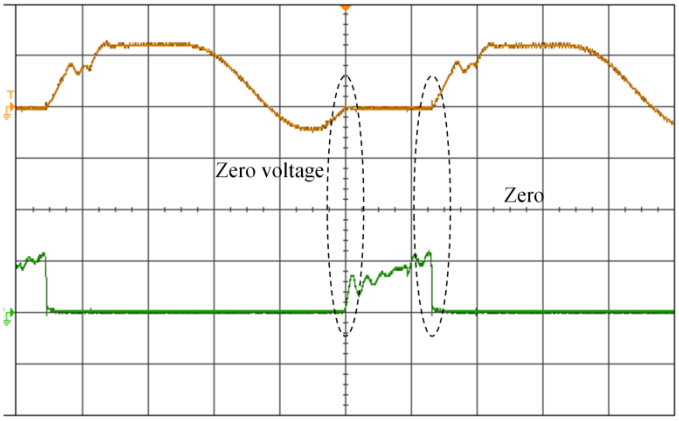

Fig. 3.14. Experimental results of an input-side switch. Top: switch voltage (200V/div), bottom: switch current (20A/div) versus time (20µS/div).

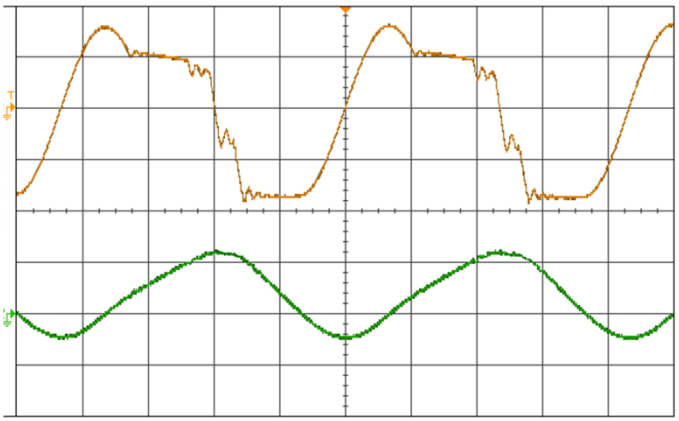

Fig. 3.15. Experimental results of the converter at 1kVA with 166V input. Top: link voltage, v_L (200V/div), bottom: link current, i_L (20A/div) versus time (30µs/div).

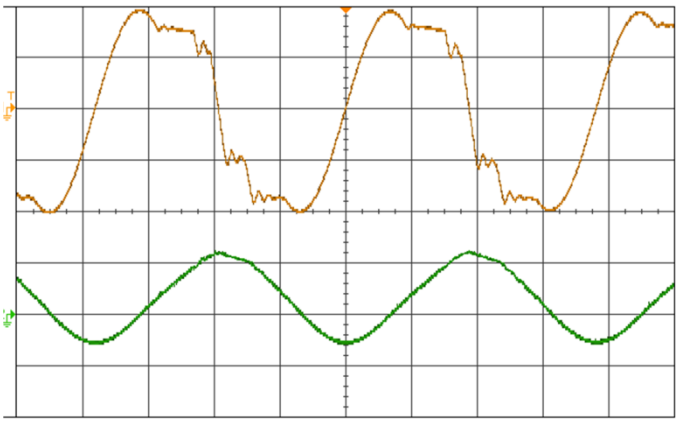

Fig. 3.16. Experimental results of the converter at 1kVA with 250V input. Top: link voltage, v_L (200V/div), bottom: link current, i_L (20A/div) versus time (30µs/div).

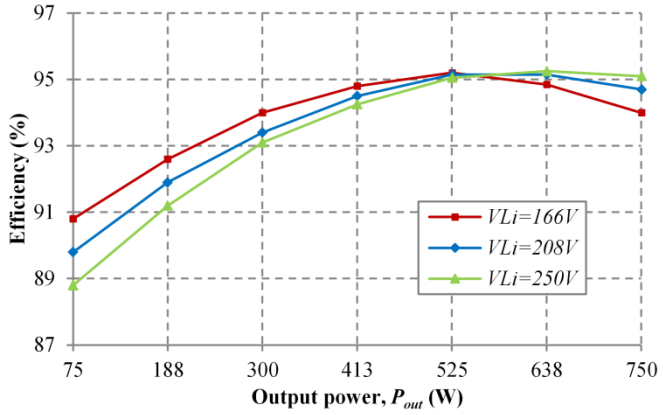

Fig. 3.17. Efficiency of the converter prototype versus output power for different values of the input line voltage.

3.3. Partial-Resonant Buck-Boost and Flyback DC-DC Converters

3.3.1. Introduction

Several soft-switching dc-dc topologies have been proposed in the literature; they can be mainly categorized as quasi-resonant, multi-resonant, resonant-transition, active-clamp, phase-controlled, and resonant-load converters [55]–[78]. Quasi-resonant converters are obtained by replacing the power switch in conventional PWM converters with a switch

network containing resonant elements [55]–[59]. Although the output voltage in these converters can be regulated by varying the switching frequency, the switch could suffer from excessive voltage or current stresses. Multi-resonant converters are the extension of quasi-resonant converters providing soft switching for all the semiconductor devices in the circuit [60], [61]. Resonant-transition dc-dc converters shape the switching waveforms of the conventional PWM converters without significantly increasing the voltage and current stresses of the power devices with the expense of adding an auxiliary resonant circuit [62], [63]. This auxiliary circuit is composed of a switch and resonant components. Active-clamp topologies employ a large capacitor and auxiliary switch to make a resonant circuit with the transformer leakage inductance in isolated converters, which leads to ZVS in addition to non-dissipative voltage clamping [64]–[66]. In a phase-controlled topology, a full-bridge network is loaded by an effective inductive load to achieve ZVS for the primary-side semiconductor devices [67], [68]. In this way, the switching frequency is fixed and the output voltage is controlled via phase control. In resonant-load dc-dc converters, a square waveform is applied to a resonant tank network connected to a load through a rectifier [69]–[78]. By moving the switching frequency closer to or further from the resonant frequency of the tank network, the load voltage can be controlled. According to the formation of the resonant network, resonant-load converters can also be subdivided as series resonant [69], [70], parallel resonant [71], [72], series-parallel LCC resonant [73]–[75], and LLC topologies [76]–[78]. Care should be taken in the consideration of various soft-switching dc-dc converters; several introduced resonant power converters have noticeable drawbacks besides their soft-switching privileges. The drawbacks include poor performance over a wide range of input voltages and load

resistances, poor efficiency at the light load due to current circulation in the tank elements, increased conduction losses, and high device voltage stress [10].

The soft-switched partial-resonant dc-dc converters in the isolated and non-isolated configurations are introduced in this study. The non-isolated topology is the new reformation of the conventional buck-boost converter with the advantage of soft switching. An ac capacitor and two reverse-blocking switches are added to achieve this benefit. Compared to the quasi-resonant converters, the true zero-voltage switching happens in the proposed topology at both turn-on and turn-off of all the semiconductor devices regardless of the load level and voltage values. Galvanic isolation can be realized by employing an air-gapped high-frequency transformer similar to the flyback converter without any snubber circuitry.

3.3.2. The Proposed Resonant DC-DC Converters

The basic partial-resonant buck-boost dc-dc converter is proposed in Fig. 3.18(a). Similar to the conventional buck-boost converter, inductor L is responsible for transferring power from the input to the output. This inductor is charged from the input and then discharged to the output cycle-by-cycle with a precise control scheme. Small ac capacitor C is placed in parallel with this inductor. The main role of capacitor C is to produce partial resonances with the inductor to realize zero-voltage switching for the power devices, as will be shown later. As the figure depicts, the converter needs two reverse-blocking (RB) switches. An RB-switch can be realized by a conventional reverse-conducting switch (IGBT or MOSFET) in series with a diode. However, the newly-available individual RB-switches can be employed for this purpose with the advantage of lower total on-state voltage. In order to transfer power in both forward and reverse directions, the reverse-blocking switches of the

converter can be replaced by bidirectional switches. The bidirectional switches can be made by using two back-to-back reverse-conducting switches in series or two reverse-blocking switches in anti-parallel.

Fig. 3.18(b) shows the isolated configuration of the proposed topology. In this converter, the magnetizing inductance of the high-frequency transformer is used for transferring power. In order to reach an appropriate inductance value, the transformer may need to have an air gap. Two smaller capacitors, C_1 and C_2, provide partial resonance. These capacitors are placed on both sides of the transformer to also provide paths for the currents of the primary and secondary leakage inductances and subsequently, avoid voltage spikes when the input and output switches are turned off [5]. As a result, no extra snubber circuit is required. The isolated bidirectional form of the proposed topology can also be made by replacing the converter switches of Fig. 3.18(b) with bidirectional switches.

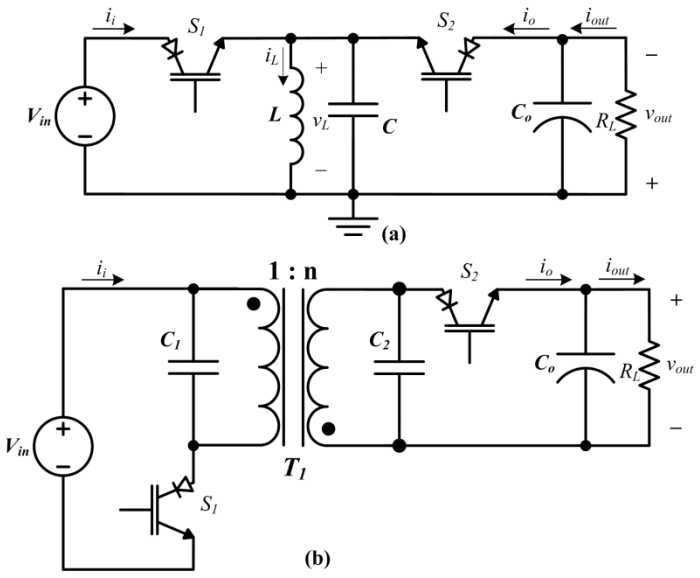

Fig. 3.18. The proposed partial-resonant dc-dc converters. (a) the non-isolated buck-boost topology, (b) the isolated flyback topology.

3.3.3. The Operation of the Proposed DC-DC Converters

The operation of the proposed soft-switched dc-dc converter in both non-isolated and isolated configurations is composed of four operating modes in each switching cycle. In the forward power flow, the converter's main inductance charges through the input in mode 1 and discharges to the output in mode 3. Modes 2 and 4 are for partial resonance of the main inductance with its parallel capacitance to achieve zero-voltage switching at both turn-on and turn-off of the power switches. A typical switching cycle of the isolated partial-resonant topology is shown in Fig. 3.19, and its corresponding operating modes are shown in Fig. 3.20. The state-plane diagram is also depicted in Fig. 3.21. The detailed operating modes of the isolated converter are explained in detail as follows by ignoring the transformer's leakage inductances and winding resistances. Their effects will be shown later.

Mode 1 [inductance charges from the input, Fig. 3.20(a)]: Switch S_1 is turned on to connect the input dc voltage across the magnetizing inductance of the transformer, L_M. As a result, L_M charges in the positive direction. This mode is allowed to run until the average of the input current meets the input reference current, I^*_i. Subsequently, switch S_1 is turned off.

Note that due to the existence of capacitors C_1 and C_2, the magnetizing inductance voltage, $v_L(t)$, decreases slowly when switch S_1 is turned off. As a result, the voltage of switch S_1 goes up slowly in its turn-off transition. Therefore, the turn-off of switch S_1 occurs at almost zero voltage. Switch S_2 has a similar zero-voltage switching in its turn off. As the ZVS behavior at the turn-off of the power switches is caused by the existence of C_1 and C_2, it happens at any input voltage, output voltage, or load value.

Mode 2 [partial resonance, Fig. 3.20(b)]: The transformer's magnetizing inductance starts to partially resonate with its total parallel capacitance, $C_t=C_1+n^2C_2$ (n is the

transformer's turns ratio), and therefore, $v_L(t)$ starts to drop. This partial resonance is permitted to run until $v_L(t)$ becomes equal to the output reflected voltage ($-V_{out}/n$), which then allows the converter to go to mode 3 with soft transition. During this mode, the magnetizing inductance current, $i_L(t)$, reaches its positive peak value, I_{LP+}, and can be expressed as follows:

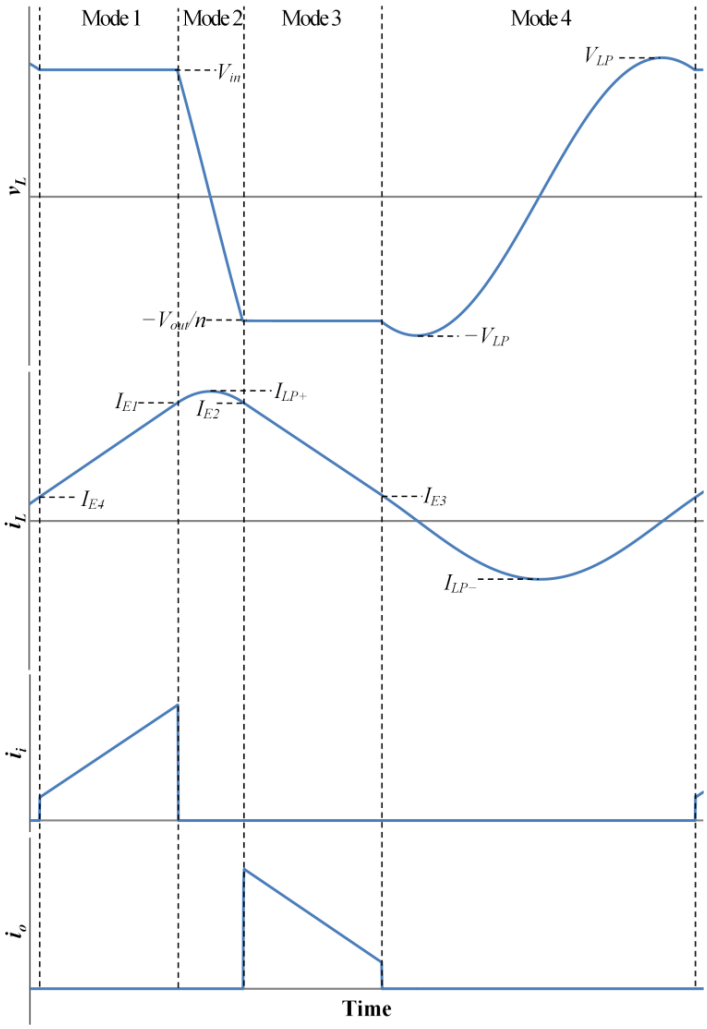

Fig. 3.19. Waveforms of the proposed isolated converter. a) magnetizing inductance voltage, b) magnetizing inductance current, c) input current, and d) output current.

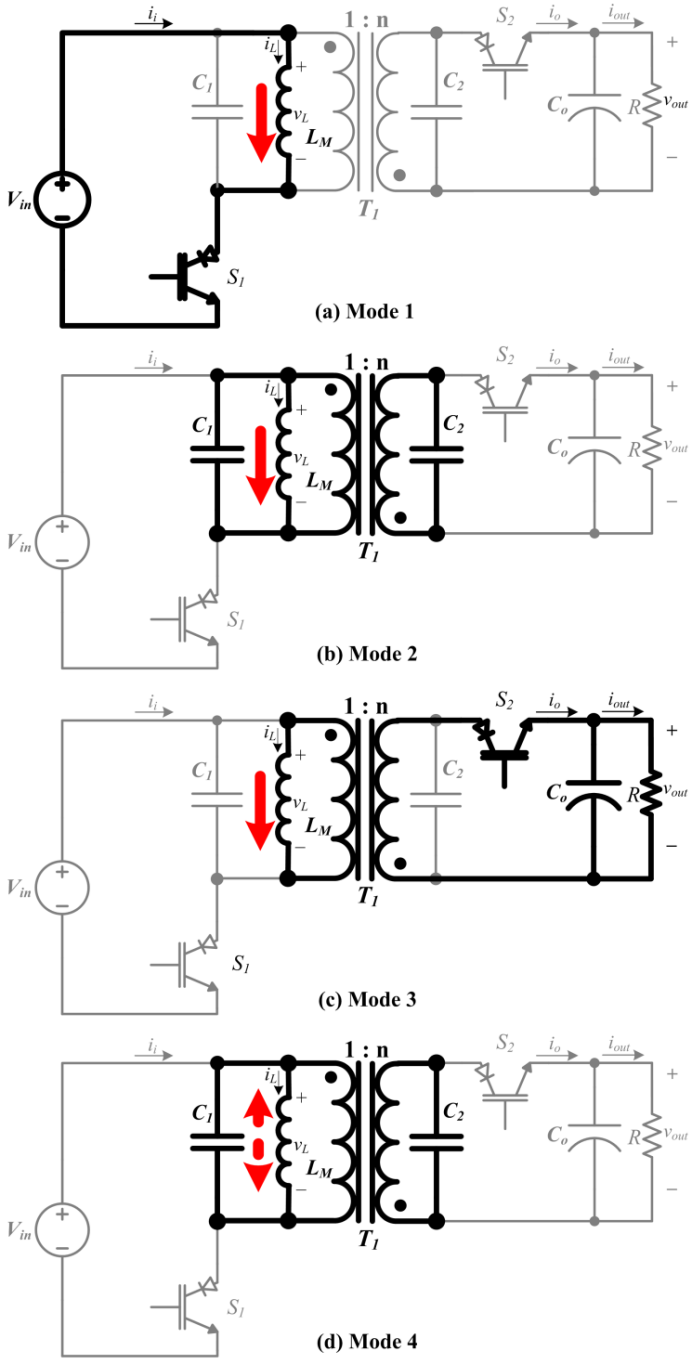

Fig. 3.20. Operating modes of the proposed isolated partial-resonant converter.

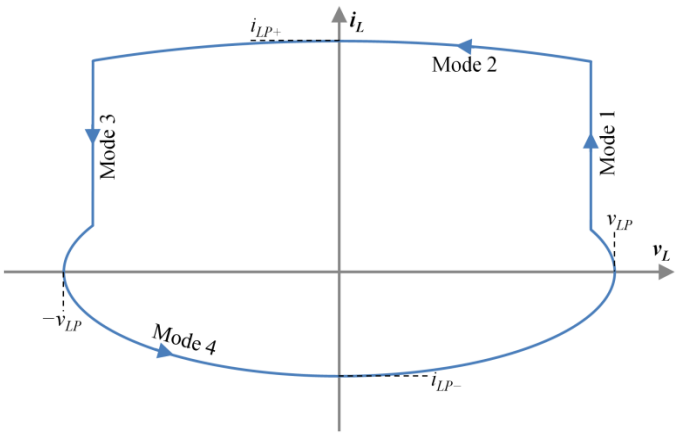

Fig. 3.21. the state-plane diagram of the proposed converter.

$$I_{LP+} = \sqrt{{I_{E1}}^2 + \frac{C_1 + n^2 C_2}{L_M} {V_{in}}^2} \tag{3.25}$$

where I_{E1} is the magnetizing inductance current at the end of mode 1, and V_{in} is the input dc voltage.

Mode 3 [inductance discharges to output, Fig. 3.20(c)]: The load-side switch, S_2, is turned on to discharge the magnetizing inductance energy to the output. This mode continues until $i_L(t)$ reaches a small value of I_{E3}, which will be defined later. After that, this mode ends and switch S_2 turns off. In order to leave a certain amount of current in the magnetizing inductance at the end of mode 3 in the digital control implementation, $i_L(t)$ is constantly measured. Once $i_L(t)$ reaches the desired value, switch S_2 is turned off and the converter goes to mode 4.

Note again that the magnetizing inductance voltage is equal to the output reflected voltage at the beginning of mode 3 when switch S_2 is turned on. As a result, the turn-on transition of switch S_2 occurs at zero voltage. The zero-voltage turn-on also happens for

switch S_1 in a similar way. This ZVS at the turn-on of the power switches does not depend on the load level and voltage values.

Mode 4 [partial resonance, Fig. 3.20(d)]: L_M and C_t resonate together again. This considerable partial resonance is maintained until $v_L(t)$ is equal to the input voltage in the down-going direction, which then permits the converter to go to mode 1 with soft transition. Therefore, $v_L(t)$ should go higher than the input voltage during this mode as shown in Fig. 3.19. In the case that V_{out}/n is more than the input voltage, this process happens naturally, and I_{E3} can be selected as zero (the peak value of the magnetizing inductance voltage, V_{LP}, will be equal to V_{out}/n). However, when V_{out}/n is smaller than the input voltage, a certain amount of current should be left in the magnetizing inductance at the end of mode 3 to force $v_L(t)$ to peak higher than the input voltage as follows:

$$I_{E3} = \sqrt{\frac{C_1+n^2C_2}{L_M}\left({V_{LP}}^2 - \left(\frac{V_{out}}{n}\right)^2\right)} \tag{3.26}$$

where V_{LP} is the pre-determined peak value of the magnetizing inductance voltage and can be selected to be 10% to 15% higher than the input voltage in practice.

In addition, the magnetizing inductance current reaches its negative peak value, I_{LP-}, during mode 4, which can be given by,

$$I_{LP-} = -\sqrt{\frac{C_1+n^2C_2}{L_M}}V_{LP} \tag{3.27}$$

In the practical digital control implementation of the proposed resonant converter, there might be a delay in the turn-on of the switches at the exact instants stated above. This delay is mainly due to the discrete sampling and required processing time and may create an unwanted hard-switching operation. In order to avoid this problem, the converter's switches can be turned on ahead of time while they are in the negative off-state voltages, and

consequently, they start conducting when they become forward biased with zero-voltage switching. For instance, switch S_1 can be turned on when $v_L(t)$ reaches its positive peak value; since it is a reverse-blocking switch, it does not conduct until $v_L(t)$ become equal to the input voltage. Switch S_2 can also be turned on as soon as the switch S_1 is turned off. As Fig. 3.19 shows, when $v_L(t)$ reaches its positive peak value, $i_L(t)$ passes zero in the positive direction. Therefore, the zero crossing of $i_L(t)$ can be used as a sign to appropriately turn on switch S_1.

The proposed topology can transfer power in the reverse direction as well as the forward direction by using bidirectional switches. In the reverse power flow direction, the magnetizing inductance is charged firstly from the output in the negative direction. After a resonant mode, the inductance is discharged to the input by properly turning on the converter's input-side switches.

3.3.4. The Analysis of the DC-DC Converter

The starting point of the analysis of the proposed isolated partial-resonant topology is the specified peak voltage of the magnetizing inductance. Knowing that $v_L(t)$ peaks at V_{LP} during mode 4, $i_L(t)$ at the end of mode 4 can be given by,

$$I_{E4} = \sqrt{\frac{C_1+n^2C_2}{L_M}\left({V_{LP}}^2 - {V_{in}}^2\right)} \tag{3.28}$$

The input reference current is equal to the average of the $i_L(t)$ in mode 1 as follows:

$$I_i^* = \frac{(I_{E4}+I_{E1})T_1}{2T} \tag{3.29}$$

where T_1 is the time length of mode 1, and T is the switching period. Applying the inductor principal equation to the transformer's magnetizing inductance in mode 1 gives,

$$I_{E1} = \frac{V_{in}T_1+L_MI_4}{L_M} \tag{3.30}$$

By substituting (6) into (5) and then solving for T_1, the time length of mode 1 can be given by,

$$T_1 = -\frac{L_M I_{E4}}{V_{in}} + \sqrt{\left(\frac{L_M I_{E4}}{V_{in}}\right)^2 + \frac{2L_M T I_i^*}{V_{in}}} \tag{3.31}$$

A similar analysis gives the time duration of mode 3 as follows:

$$T_3 = -\frac{nL_M I_{E3}}{RI_{out}} + \sqrt{\left(\frac{nL_M I_{E3}}{RI_{out}}\right)^2 + \frac{2n^2 L_M T}{R}} \tag{3.32}$$

where I_{out} is the output dc current of the converter and can be found according to the input-output power balance from the following:

$$I_{out} = \sqrt{\frac{V_{in} I_i^*}{R}} \tag{3.33}$$

The time lengths of the partial resonant modes 2 and 4 can be expressed by,

$$T_2 = \sqrt{L_M(C_1 + n^2 C_2)}\left[sin^{-1}\left(\frac{V_{in}}{I_{LP+}}\sqrt{\frac{C_1+n^2C_2}{L_M}}\right) + sin^{-1}\left(\frac{R_L I_o}{nI_{LP+}}\sqrt{\frac{C_1+n^2C_2}{L_M}}\right)\right] \tag{3.34}$$

$$T_4 = \sqrt{L_M(C_1 + n^2 C_2)}\left[2\pi - sin^{-1}\left(\frac{R_L I_o}{nV_{LP}}\right) - sin^{-1}\left(\frac{V_{in}}{V_{LP}}\right)\right] \tag{3.35}$$

Finally, the sum of the time intervals of all the operating modes of the converter is equal to the switching period as follows:

$$T_1 + T_2 + T_3 + T_4 = T \tag{3.36}$$

Substituting (3.31), (3.32), (3.34), and (3.35) into (3.36) results in a set of implicit equations that should be solved simultaneously to find the switching period and other main parameters of the converter.

Fig. 3.22 depicts the graph of the output current of the proposed isolated converter versus the input reference current for the different values of the input dc voltage. According to the figure, the converter's output current is a function of the input reference current, and as the input reference current increases, the output dc current of the converter rises nonlinearly.

The figure clearly illustrates that the converter works in the step-down mode of operation in the low input reference currents and gradually switches to the step-up mode of operation by increasing the input reference current. Therefore, in order to have a fixed output voltage, a closed-loop controller can be employed by measuring the output voltage of the converter and adjusting the input reference current according to the desired output voltage.

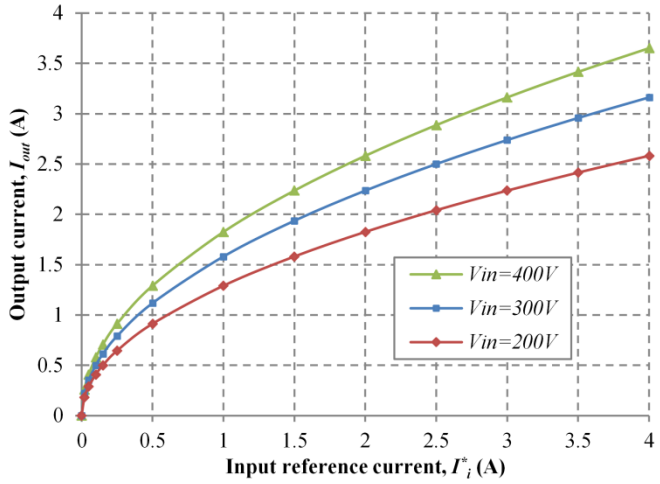

Fig. 3.22. Output current versus input reference current for the various values of the input voltage, R=120Ω.

The graph of the switching frequency, the positive peak value of the magnetizing inductance current, and the absolute value of the negative peak of the magnetizing inductance current versus L'_M for the various values of C_s are shown in Fig. 3.23. L'_M and C_s are the magnetizing inductance and total parallel capacitance seen from the secondary side of the transformer ($L'_M=n^2L_M$, and $C_s=C_2+C_1/n^2$). According to the figure, as the total parallel capacitance reduces, the magnitudes of the magnetizing current peak values decrease; this can be verified by considering (3.25) and (3.27). According to (3.34) and (3.35), the

reduction of the total parallel capacitance also lessens the duration of the resonant modes where there is no transfer of power; consequently, i_{EI} in (3.25) reduces as well. It is apparent that the switching frequency increases by lessening the resonant intervals due to the reduction of the total parallel capacitance. As Fig. 3.23 displays, the switching frequency and the peak values of the magnetizing inductance current also depend on the magnetizing inductance value; the reduction of the magnetizing inductance increases the magnitudes of the magnetizing current peak values as well as the switching frequency. Note that the transformer's turns ratio was selected as 0.92 in this analysis, which will be discussed later.

The graph of the switching frequency and the peak values of the magnetizing inductance current versus L'_M and C_s for a given operating point (Fig. 3.23) can be used to design the proposed converter effectively. The magnitudes of the magnetizing current positive and negative peak values specify the conduction power loss of the switches and the transformer power loss; therefore, lowering these peak values yields smaller power losses on the switches and transformer. In addition, it is desirable to increase the switching frequency as much as possible to shrink the size of passive components. Nonetheless, the switching frequency should be much smaller than the sampling rate of the digital controller to get enough samples in each switching cycle and run the converter properly. As shown later in the experimental results section, the sample time of the digital controller was 1.1μs. Therefore, the magnetizing inductance and the total parallel capacitance were selected as 225μH and 100nF to set the switching frequency at about 22kHz at the given operating point. The switching frequency can be moved higher provided that a faster digital controller with a smaller sample time is employed.

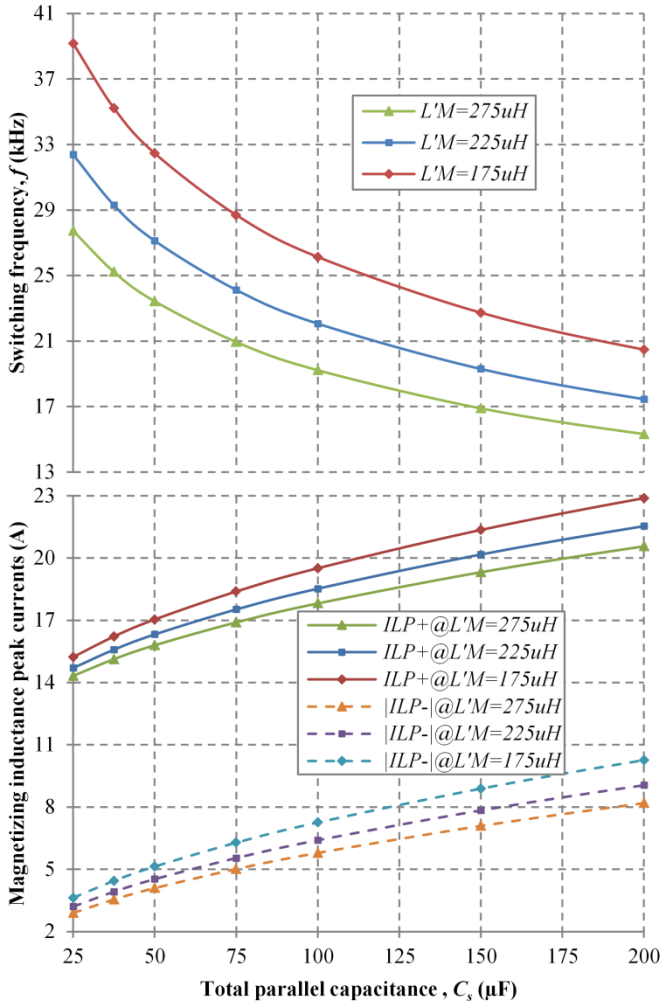

Fig. 3.23. The switching frequency and the magnitudes of the magnetizing current peak values versus the total parallel capacitance for various values of the magnetizing inductance, V_{in}=300V, R=120Ω, n=0.92, and P_{out}= 750W.

Although the proposed partial-resonant isolated dc-dc converter can work with the transformer's turns ratio of 1 in both step-up and step-down operations, the turns ratio can be selected optimally for the best operation of the converter. Fig. 3.24 shows the magnetizing inductance rms current, $I_{L,rms}$, versus the transformer's turns ratio for different input voltage values at the given operating point. As the graph shows, the magnetizing inductance rms current reaches its lowest value when n is almost equal to 0.92 for the input voltage of 300V

(same as the output voltage). This occurs because as the turns ratio decreases from unity, the mode-3 magnetizing inductance voltage, $-V_{out}/n$, decreases. If V_{out}/n reaches the required peak value of the magnetizing inductance voltage, there is no need to leave any current in the magnetizing inductance at the end of mode 3 as stated before and $V_{LP}=V_{out}/n$. As a result, the mode-4 duration reaches its minimum value (note the second term in (3.35)), and the converter operates more efficiently. Decreasing n lower than the optimized value will cause an increase in V_{LP}, which lengthens the mode-4 duration (note to the third term in (3.35)). As Fig. 3.24 reveals, the optimum turns ratio depends on the input voltage; in the case of a different input voltage, the optimum turns ratio can be found by multiplying 0.92 by the output-input voltage ratio.

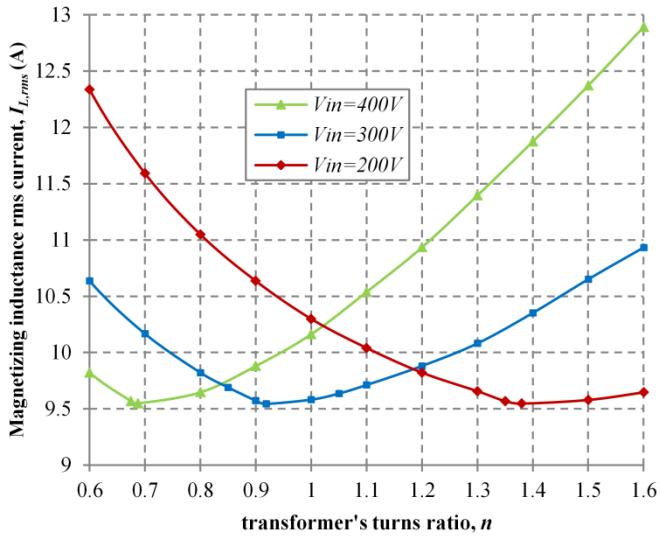

Fig. 3.24. Magnetizing inductance rms current versus the transformer's turns ratio for various input voltage values, R=120Ω, L'_M= 225μH, C_s=100nF, V_{LP}=1.1V_{in}, and P_{out}= 750W.

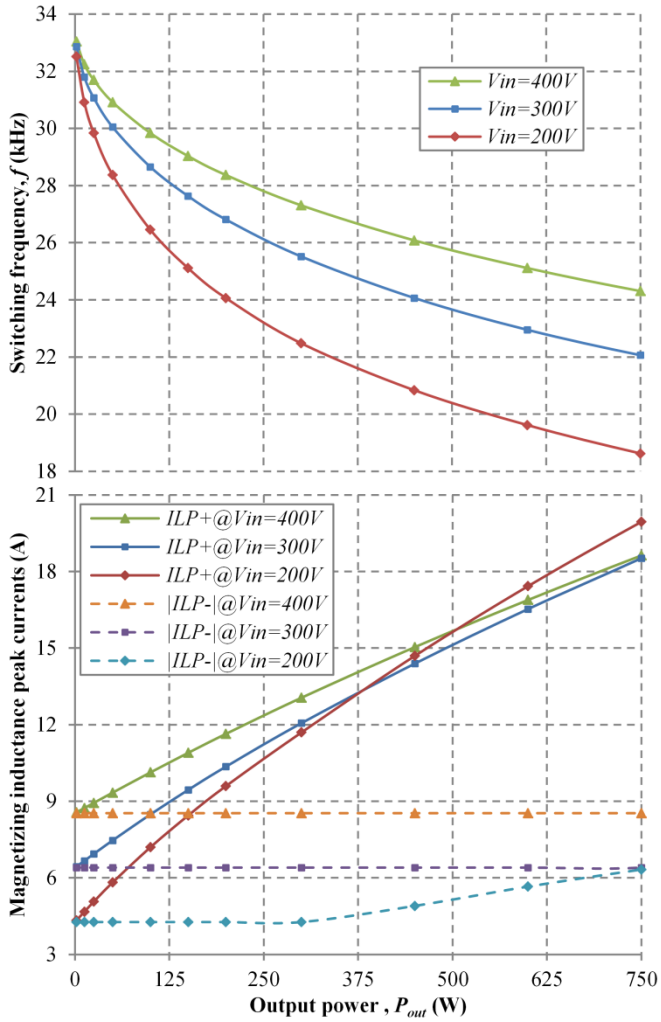

Fig. 3.25. The switching frequency and the magnitudes of the magnetizing current peak values versus the output power for various input voltage values, R=120Ω, L'_M= 225μH, C_s=100nF, and n=0.92.

Fig. 3.25 shows the switching frequency and the magnitudes of the magnetizing current peak values versus the converter's output power for different values of the input voltage. According to the figure, the positive peak value of the magnetizing inductance current is completely dependent on the output power, and as the output power reduces, I_{LP+} decreases almost linearly. This occurs because as the output power drops, the input reference current should decrease accordingly. Therefore, the time-lengths of modes 1 and 3 decrease,

which results in the reduction of I_{EI} in (3.25) and consequently I_{LP+}. In addition, the reduction in duration of the odd-numbered modes results in the increase of the switching frequency. Note that according to (3.27), I_{LP-} does not depend on the output power, but it may depend on the input voltage (V_{LP} should be higher than the input voltage). The switching frequency and the magnitudes of the magnetizing current peak values at a very small amount of the output power can be given by,

$$f|_{P_{out}\approx 0} = \frac{1}{2\pi\sqrt{L_M(C_1+n^2C_2)}} \tag{3.37}$$

$$I_{LP+}|_{P_{out}\approx 0} = -I_{LP-}|_{P_{out}\approx 0} = \sqrt{\frac{C_1+n^2C_2}{L_M}}V_{LP} \tag{3.38}$$

According to Fig. 3.25, the change of the input dc voltage at a given output power affects the operating parameters of the proposed converter moderately. Although the increment of the input voltage at any given power increases the switching frequency, the change of the peak values of the magnetizing inductance current depends on the output power and input voltage values at the operating point of the converter.

3.3.5. Experimental Results

To test the performance of the introduced topology, a prototype of the proposed isolated partial-resonant converter was built and tested. The sample time of the digital control was minimized to reach better control performance, which resulted in the sample time of 1.1μs. This sample time includes the ADC conversion time and the required processing time. An air-gapped Ferrite transformer was designed for the prototype with the secondary-side magnetizing inductance of 225μH and turns ratio of 0.92. Since the transformer has a considerable airgap length with a high-frequency ac current, the airgap fringing field can

cause huge eddy current losses in adjacent coil conductors [28]. To avoid this problem, windings were intentionally not placed in the immediate vicinity of the gap and multi-stranded wires were employed. The total leakage inductance and winding resistance of the transformer were measured as 2μH and 95mΩ respectively. The parallel capacitors C_1 and C_2 were chosen as 47nF to have C_s of about 103nF at the primary-side of the transformer.

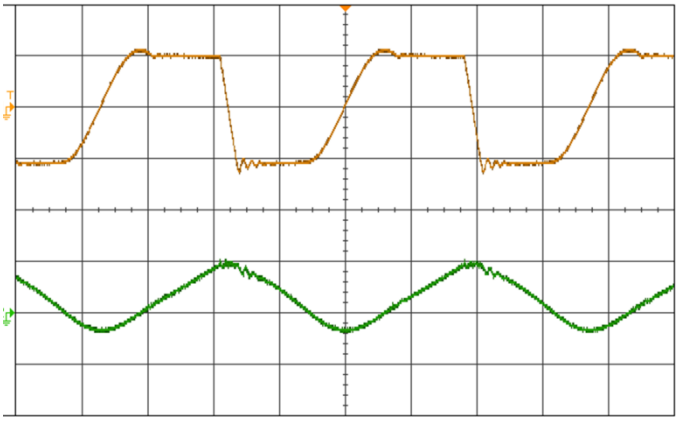

Fig. 3.26. Experimental results with 300V input at 750W. Top: magnetizing inductance voltage (300V/div), and bottom: magnetizing inductance current (20A/div) versus time (12μS/div).

In the first test, the prototype converter was run with the input voltage of 300V to supply 750W to a 120Ω load, which yielded the output voltage of 300V. Fig. 3.26 shows the magnetizing inductance current and the transformer primary-side voltage, which is almost equal to the magnetizing inductance voltage. The magnetizing inductance current was found by properly subtracting the currents of the transformer's primary and secondary currents. As the figure shows, the transformer's leakage inductances cause some ringing at the beginning of active modes 1 and 3, which are damped by the parallel capacitors and dissipated in the winding resistances of the transformer. The resulting switching frequency and the positive

and negative peak values of the magnetizing inductance current were 22.4kHz, 18.9A, and −6.4A, respectively, at this test condition. These values are very close to the analytical results shown in Fig. 3.25. The small differences are mainly due to the non-linearity and power loss of the components. The measured efficiency was 96.2%. Figs. 3.27 and 3.28 depict the voltage and current waveforms of switches S_1 and S_2. As the figure shows, the true zero-voltage switching happens at both turn-on and turn-off of the power switches as expected.

In order to verify the converter operation in step-up and step-down modes of operation, two more tests with ±100V change in the input voltage were run. Fig. 3.29 shows the magnetizing inductance voltage and current with the input voltage of 200V, and Fig. 3.30 depicts these parameters with the input voltage of 400V. The output load and power at these test conditions were 120Ω and 750W, same as the first test. The change of the input voltage can be revealed by observing the magnetizing inductance voltage during mode 1, which is decreased in Fig. 3.29 and increased in Fig. 3.30. As a result, the mode-1 duration is increased with the 200V input and decreased with the 300V input to draw the same amount of power from the input. Therefore, consistent with the analytical results, the switching frequency decreased to 18.7kHz in the step-up operating case and increased to 24.6kHz in the step-down test condition. Note that the magnetizing inductance current at the end of mode 3 is zero with the input voltage of 200V and 300V (Figs. 3.26 and 3.29) while it is non-zero with the 400V input (Fig. 3.30), according to (3.26). As a result, V_{LP} and $|I_{LP-}|$ are higher in Fig. 3.30.

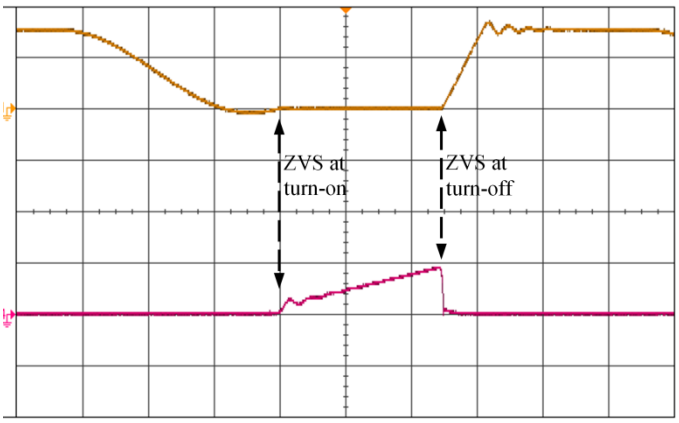

Fig. 3.27. Experimental results with 300V input at 750W. Top: voltage of switch S_1 (400V/div), and bottom: current of switch S_1 (20A/div) versus time (5µS/div).

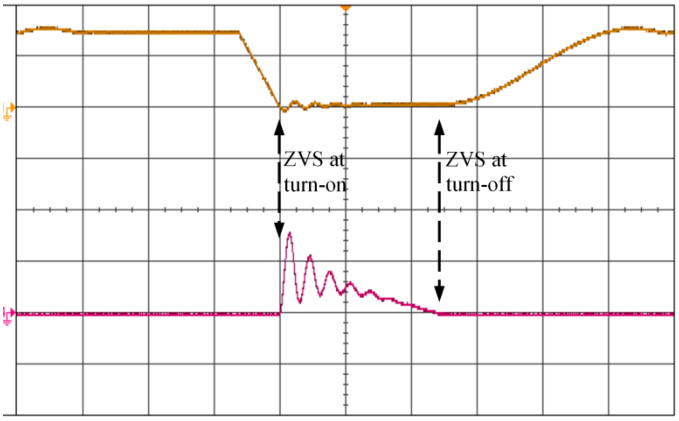

Fig. 3.28. Experimental results with 300V input at 750W. Top: voltage of switch S_2 (400V/div), and bottom: current of switch S_2 (20A/div) versus time (5µS/div).

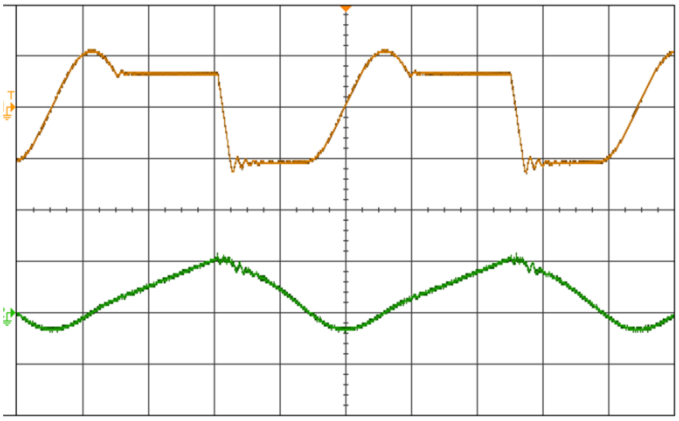

Fig. 3.29. Experimental results with 200V input at 750W. Top: magnetizing inductance voltage (300V/div), and bottom: magnetizing inductance current (20A/div) versus time (12μS/div).

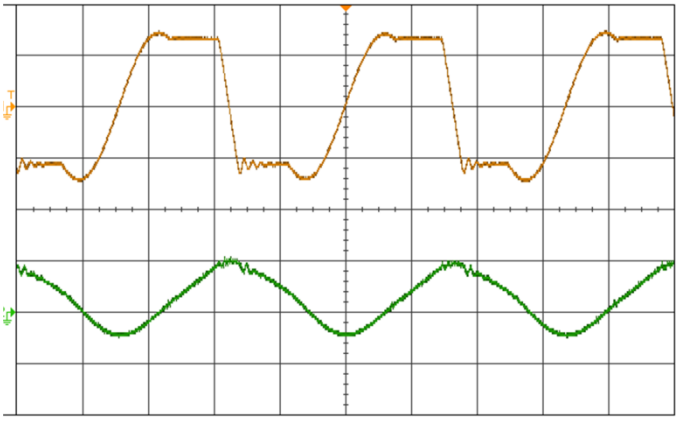

Fig. 3.30. Experimental results with 400V input at 750W. Top: magnetizing inductance voltage (300V/div), and bottom: magnetizing inductance current (20A/div) versus time (12μS/div).

3.4. A Soft-Switched Highly-Reliable Grid-Tied Inverter for PV Applications

3.4.1. Introduction

PV inverters are the key components in solar energy systems by collecting the maximum possible power from PV cells to deliver to a utility grid or stand-alone loads. The conventional PV inverters are normally composed of an isolated dc/dc stage for maximum

power point (MPP) tracking and voltage boosting, a number of electrolytic capacitors for the intermediate dc bus, and a dc/ac inverter for grid interface [29], [30], and [79]. Although this configuration is simple and effective, it suffers from low efficiency due to two stages of power conversion, low power density because of using several switches and passive components, and low reliability as a result of employing limited lifetime electrolytic capacitors [80]–[82]. Several solutions have been introduced to overcome these issues [39], [83]–[85]. High-frequency (HF) link PV inverters are outstanding candidates that allow a single-stage of power conversion with a fast dynamic response while excluding the electrolytic capacitors [48], [86]–[93]. This study proposes a new HF-link PV inverter with soft switching operation. This converter is able to harvest the maximum possible power of the PV array in a single stage without any intermediate dc bus. The proposed 7-switch PV inverter has the step-up ability and can easily employ an optional HF transformer for galvanic isolation.

3.4.2. The Proposed PV Inverter

Fig. 3.31(a) shows the proposed PV inverter with an HF link and soft-switching operation. The inductor L and small parallel capacitor C form the resonant HF link. Power transfer is accomplished via the link inductor, L, which is charged from the PV voltage and discharged to the grid phases. The link capacitor, C, realizes zero-voltage switching for the power switches as explained later. The converter's seven switches need to have the reverse-blocking capability, e.g. an IGBT and diode in series. Fig. 3.31(b) reveals the isolated version of the topology, in which the link inductor is replaced with an HF air-gapped transformer and the link capacitor is split between both sides of the transformer. In this case, the

transformer's magnetizing inductance is used as the link inductance. The link capacitors also behave as passive snubbers to avoid voltage spikes due to the transformer's leakage inductances [7].

The control scheme of the proposed PV inverter includes a maximum power point (MPP) tracker. This MPP tracker measures the voltage and current of the PV array constantly and calculates the PV reference current, i^*_{PV}. The reference current is sent to the inverter's operating algorithm to be handled accordingly. Most of the available MPP tracking techniques can be employed in these MPP trackers to find the optimal PV reference current properly, such as the perturb and observe (P&O), incremental conductance (IC), and beta methods [50].

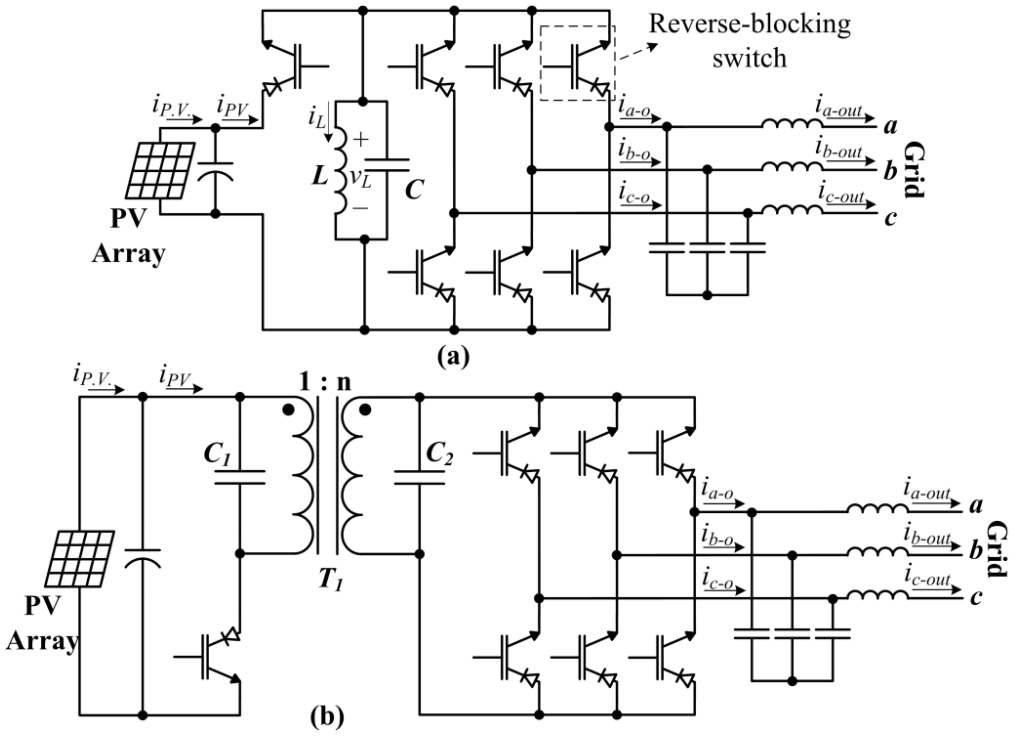

Fig. 3.31. The proposed soft-switched HF-link PV inverter. (a) The non-isolated topology, and (b) the isolated topology.

The proposed converter is a current-source converter, and consequently, the reference currents for the output phases are needed for the proper operation. The output reference currents can be simply calculated according to the input power resulting from the PV array and the estimated power loss of the converter. The output reference currents should be at the same phase angle and frequency of their corresponding grid voltage to have a unity power factor.

3.4.3. The Principle of Operation

The operating algorithm of the introduced HF-link PV inverter consists of six modes of operation in each link cycle. A typical link cycle of the topology is shown in Fig. 3.32. The modes of operation are explained as follows.

Mode 1 (link charges): The input-side switch is turned on to connect the HF-link to the PV array. As a result, the link inductor, L, starts to charge. This mode is allowed to continue until the average of the PV current, i_{PV}, meets the PV reference current, i^*_{PV}. Afterwards, the switch is turned off.

In the turn-off process of the mode-1 switch, due to the existence of the link capacitor C, the voltage of the switch goes up slowly while its current is quickly reduced. As a result, the switch turns off at almost zero voltage. This soft switching operation happens at the turn-off of all the converter's switches in all operating modes.

Mode 2 (link resonates): The link inductor and capacitor starts to resonate. This resonance continues until the link voltage is equal to the voltage of the selected output phase pair, which will be discussed later. During this mode, the link current, $i_L(t)$, reaches its positive peak values, i_{LP+}, as follows:

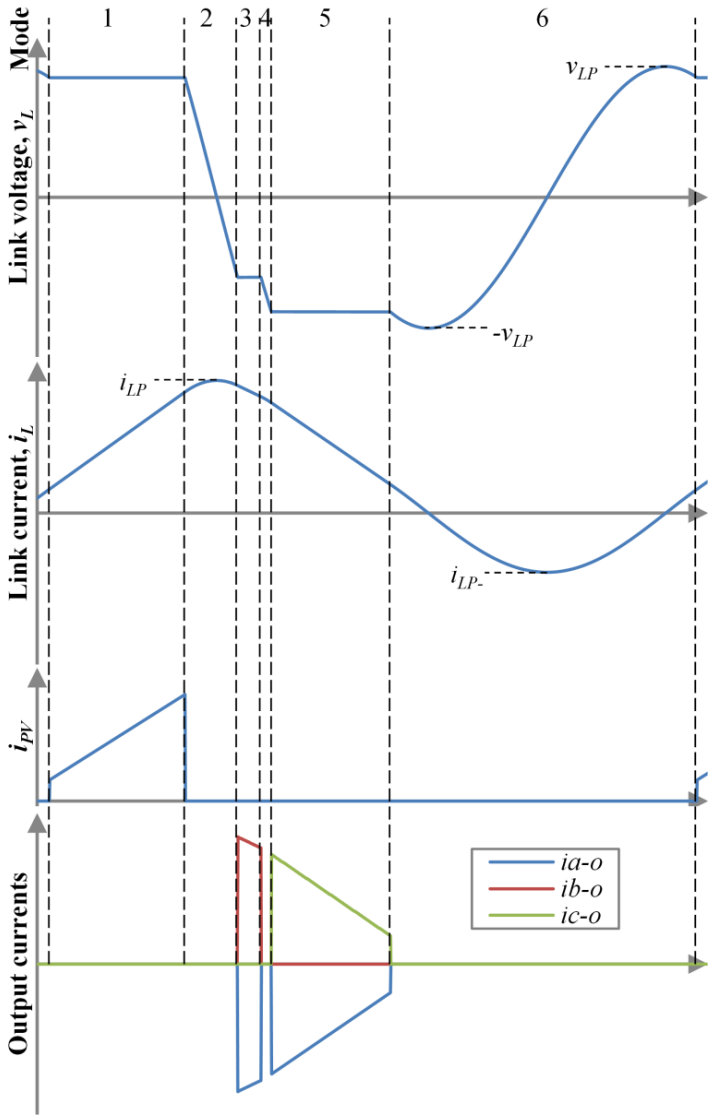

Fig. 3.32. Typical waveforms of the proposed converter. (a) link voltage, (b) link current, (c) PV current, d) output currents.

$$i_{LP+} = \sqrt{{i_L}^2(t_1) + \frac{C}{L}{v_{PV}}^2} \tag{3.39}$$

where t_1 is the time at the end of mode 1, and v_{PV} is the instantaneous PV array voltage.

Mode 3 (link discharges): Two proper grid-side switches are turned on to connect the HF link to a grid phase pair with the second-lowest voltage at the instant. As a result, the link

inductor starts to discharge to that phase pair. This mode runs until the average current of one of the connected phases equals its reference value. After that, the switches are turned off.

The link voltage is equal to the selected output phase pair at the beginning of mode 3. Thus, the turn-on of the switches occurs at zero voltage. The zero voltage turn-on happens at the beginning of all the odd-numbered modes.

Mode 4 (link resonates): The link components resonate till the link voltage is equal to the voltage of the phase pair of mode 5.

Mode 5 (link discharges): Two grid-side switches are turned on to connect the inverter's HF link to a grid phase pair with the lowest instantaneous voltage. In this way, the link voltages in modes 1, 3, and 5 are in descending order, and as a result, the resonant intervals between these modes are in the shortest possible case. This mode ends and the switches are turned off after the link current reaches a small value, which will be described later.

Mode 6 (link resonates): The HF-link components resonate together. This partial resonance runs until the link voltage becomes equal to PV array voltage, and thus, the converter goes to mode 1 with zero-voltage switching. For this procedure to occur properly, the link voltage should go higher than the PV array voltage during this mode, which may require that a small amount of current be left in the link inductor at the end of mode 5 according to the following:

$$i_L(t_5) = \begin{cases} \sqrt{\frac{C}{L}\left((kv_{PV})^2 - {v_L}^2(t_5)\right)}, & |v_L(t_5)| < kv_{PV} \\ 0, & |v_L(t_5)| > kv_{PV} \end{cases} \tag{3.40}$$

where t_5 is time at the end of mode 5, and k can be chosen as 1.1−1.15. Eq. (3.40) ensures the link peak voltage, v_{LP}, to be equal or higher than kv_{PV}. In the case that $|v_L(t_5)|$ is lower than

kv_{PV}, there should be a limited current in the link inductance at the end of mode 5 so that the v_{LP} is equal to kv_{PV}. However, when $|v_L(t_5)|$ is more than kv_{PV}, there is no need to leave any current in the link inductance at the end of mode 5, and the link voltage peaks at $|v_L(t_5)|$ during mode 6 naturally. The link current reaches its negative peak value, i_{LP-}, during mode 6, which can be given by,

$$i_{LP-} = -\sqrt{\frac{C}{L}} v_{LP} \tag{3.41}$$

3.4.4. The Analysis and Optimal Design of the PV Inverter

The link voltage peaks at v_{LP} during mode 6 and is equal to v_{PV} at the end of this mode. Hence, the average of the link current at the end of mode 6 can be written as follows:

$$I_{\mathrm{E6}} = \sqrt{\frac{C}{L}\left({V_{LP}}^2 - {V_{PV}}^2\right)} \tag{3.42}$$

where "I_{Ex}" is defined as the average of the link current at the end of mode "x". The parameters with capital letters are used to represent the average of the corresponding parameters that use lower case letters. By finding the average of the link current in mode 1 and then equating it with I^*_{PV}, the average duration of mode 1, T_1, can be given by,

$$T_1 = -\frac{LI_{E6}}{V_{PV}} + \sqrt{\left(\frac{LI_{E6}}{V_{PV}}\right)^2 + \frac{2LTI^*_{PV}}{V_{PV}}} \tag{3.43}$$

where T is the average period of the link cycle. As the arrangement of the line and phase voltages of a three phase system changes periodically every *π/6 rad/s*, the first *π/6 rad/s* will be considered for the analysis. In this interval, phase pair *ba* has the second-lowest output voltage and is selected for mode 3. Thus, the average of the link voltage and current in mode 3 is given by,

$$V_3 = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} v_{ba}\, d(\omega t) = -\frac{3\sqrt{2}(\sqrt{3}-1)}{\pi} V_{Lo} \tag{3.44}$$

$$I_3 = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} i_a\, d(\omega t) = \frac{3\sqrt{2}(2-\sqrt{3})}{\pi} I_{Po} \tag{3.45}$$

where V_{Lo} is the output line rms voltage, and I_{Po} is the output phase rms current. Similarly, phase pair *bc* has the lowest instantaneous voltage and is selected for the mode 5. Hence, the link average voltage and current in mode 5 can be given in a similar way. In addition, using the same method for finding T_1, the average time-length of modes 3 and 5 can be obtained. The lengths of mode 4 and mode 8 can be obtained as follows:

$$T_4 = \sqrt{LC}\left[\sin^{-1}\left(\frac{V_{PV}}{I_{LP+}}\sqrt{\frac{C}{L}}\right) - \sin^{-1}\left(\frac{V_3}{I_{LP+}}\sqrt{\frac{C}{L}}\right)\right] \tag{3.46}$$

$$T_6 = \sqrt{LC}\left[2\pi + \sin^{-1}\left(\frac{V_5}{V_{LP}}\right) - \sin^{-1}\left(\frac{V_{PV}}{V_{LP}}\right)\right] \tag{3.47}$$

The duration of the short modes 2 and 4 can be found in a similar way. Finally, the sum of the time intervals of all the modes is equal to the average link period, T, which results in a set of implicit equations to be solved simultaneously. Fig. 3.33 shows the average of the link frequency, link positive peak current, and the absolute value of the link negative peak current versus the link capacitance for various values of the link inductance. This graph can be used to design the proposed PV inverter for a desirable working condition. Note that the conduction loss of the switches and the inductor power loss depend on the link peak current; in order to decrease these losses, the link peak current should be reduced. The link frequency is also another important parameter determining the size of passive components, and therefore, it is desirable to increase the link frequency as much as possible.

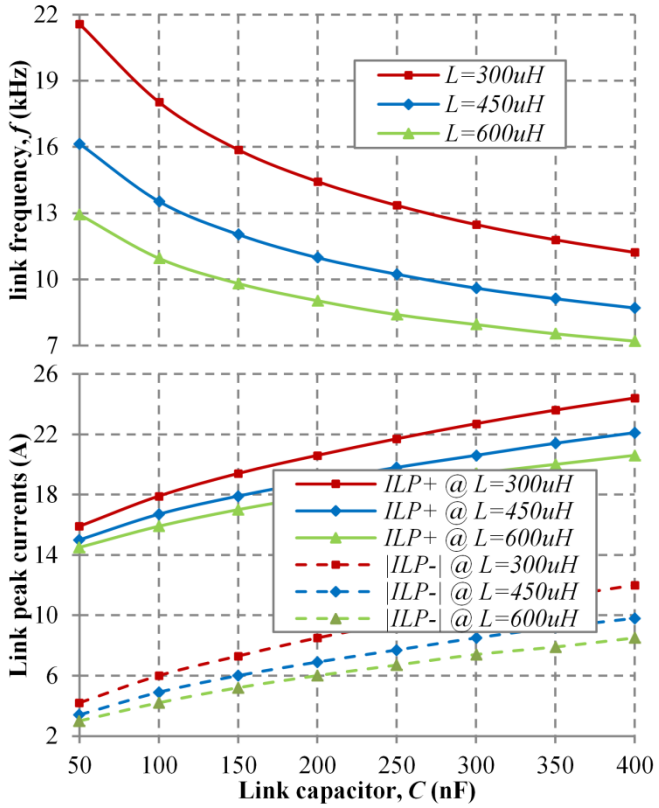

Fig. 3.33. Link frequency, and link positive and negative peak currents versus C for V_{PV}=300V, V_{Lo}=208V, and P_{out}=750W.

3.4.5. Experimental Results

A 750W prototype was developed to verify the performance of the proposed PV inverter. The link components were selected as 450μH and 200nF, and the grid voltage was 208V. A PV array emulator was employed with the open-circuit voltage of 360V and the maximum power of 750W. Figs. 3.34 and 3.35 show the experimental results when the PV was adjusted at STC. At this test, the PV voltage and power was measured as 305V and 746W, which shows the proper MPP operation. Moreover, the link frequency was 11.3kHz, which is very close to the analysis results given above (11.0kHz). The efficiency and THD was 95.4% and 1.6%, respectively.

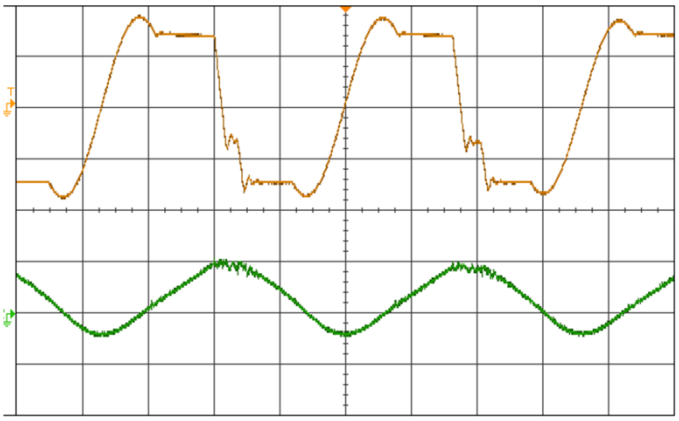

Fig. 3.34. Experimental results. Top: link voltage (200V/div), bottom: link current (20A/div) versus (25μS/div).

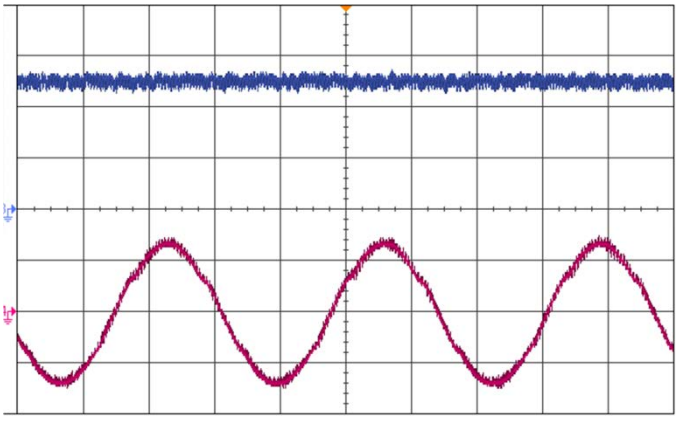

Fig. 3.35. Experimental results. Top: PV current (1A/div), bottom: output current of phase *a* (2A/div) versus (5mS/div).

4. THE TYPE-II REDUCED-SWITCH RESONANT HIGH-FREQUENCY AC-LINK CONVERTERS*

4.1. Introduction

A generation of reduced-switch partial-resonant HFAC-link converters and their applications were proposed in section 3. This section introduces another family of soft-switched reduced-switch HFAC-link converters and their applications [94]-[99]. Furthermore, as will be shown in section 5, this generation presents another alternative to the original converter when one or more power switches are broken.

4.2. A Soft-Switched Three-Phase AC-AC Converter with a High-Frequency AC Link

4.2.1. Introduction

An innovative HFAC-link ac-ac resonant converter with outstanding performance is introduced in this study for low and medium power applications. The proposed converter is

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composed of twelve reverse-blocking power switches, an ac inductor-capacitor pair as the HFAC link, and small low-pass filters at its input and output sides. The link inductor is responsible for transferring power, and the link capacitor creates the zero-voltage switching (ZVS) condition for the converter's switches. The proposed ac-ac resonant converter has the following benefits: 1) zero-voltage switching at both turn-on and turn-off of all the converter's switches, 2) higher power density and higher reliability compared to conventional dc-link PWM converters due to the minimization of magnetic components and the nonappearance of bulky limited-lifetime electrolytic capacitors, 3) unity input power factor independent of the load current, 4) bidirectional power flow, 5) step-up and step-down operations in both directions, 6) very fast dynamic response, and 7) provide optional galvanic isolation using a single small-sized HF transformer in the HFAC link, which is substantially smaller than the three-phase 50/60Hz transformers used in conventional PWM converters for isolation. The control algorithm of the proposed converter is rather involved and needs a fast digital controller to get sufficient samples in each link cycle. In addition, voltage stresses on power devices are slightly increased, and the converter's switching frequency varies moderately with the changes of input voltage and load power.

4.2.2. The Proposed AC-AC Resonant Converter

Fig. 4.1 shows the proposed three-phase ac-ac resonant converter with an HFAC link. The ac inductor L and small ac capacitor C in parallel make the HFAC link. As the figure shows, the converter's switches should have the reverse-blocking capability. A series combination of an IGBT or MOSFET with a diode can make a reverse-blocking switch; nonetheless, individual reverse-blocking switches are now available in the market with the

advantage of lower total on-state voltage. The low-pass filters at the input and output sides suppress switching-frequency harmonics. Power transfer from the input to the converter's output is accomplished via the link inductor, *L*, which is charged from the input voltages and then discharged to the output phases with a precisely controllable current technique. Hence, there is no direct power transfer from the input to the output. The link capacitor, *C*, produces partial resonances to obtain soft switching operation, as will be shown later. An optional small-sized high-frequency transformer can be utilized in the converter's HFAC link to achieve galvanic isolation similar to [7].

The proposed converter is fundamentally a current-source converter and, consequently, it needs the reference currents of the output phases for proper operation. As will be shown later, the reference currents of the input phases are also required in the converter control scheme. The input reference currents can be easily calculated using the output power and the estimated power loss of the converter. For example, the input reference current of phase *a* can be given by,

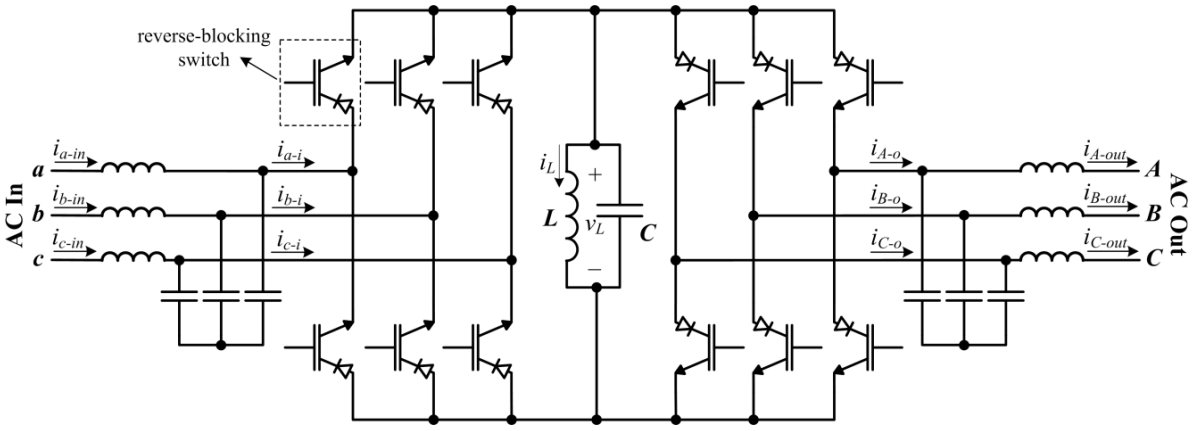

Fig. 4.1. The proposed HFAC-link three-phase ac-ac resonant converter.

$$i_{a-i,ref}(t) = \frac{\sqrt{2}(P_{out}+P_{loss})}{3V_{Pi}}\sin(\omega t) \quad (4.1)$$

where V_{Pi} is the input phase rms voltage, P_{out} is the output active power, and P_{loss} is the estimated power loss of the converter. The input reference currents of phases *b* and *c* can be calculated similarly. These references should have the same frequency and phase angle respective to their related input phase voltages to achieve unity input power factor. The operation of the converter is not highly sensitive to the exact value of the power loss; however, to reach an accurate value of the power loss, both the input and output active powers can be measured frequently. If it is desirable to have a non-unity input power factor, leading or lagging, the input reference currents of the converter can be modified properly to have the required phase angle and amplitude.

The operation of the introduced HFAC-link converter is composed of eight separate modes in each link cycle. Typical operating modes and a link cycle of the proposed topology are shown in Figs. 4.2 and 4.3, and the switch states for each mode of the proposed converter are summarized in Table 4.1. In brief, the link inductor charges through the input in modes 1 and 3 and discharges to the output in modes 5 and 7. The even-numbered modes are for partial resonances to achieve zero-voltage switching. The converter modes of operation are explained in detail as follows.

Mode 1 (the link charges): The highest instantaneous input line-to-line voltage is connected to the HFAC link in the positive direction by turning on two appropriate input-side switches. Therefore, the link inductor, *L*, charges positively. This mode ends as the average current of one of the connected input phases meets its reference value. The switches are turned off afterwards.

Due to the existence of the link capacitor, the link voltage, $v_L(t)$, drops slowly while the mode-1 switches are turned off. Consequently, the switch voltages slowly increase at their turn-off. Therefore, the mode-1 switches are turned off at almost zero voltage. This zero-voltage turn-off occurs for all the converter's other switches correspondingly.

Mode 2 (the link exhibits partial resonance): The link inductor starts to resonate with its parallel capacitor, and the link voltage starts to drop. This partial resonance is permitted to run until the link voltage is equal to the second highest input line-to-line voltage.

Table 4.1. The switch states for each mode of the proposed converter.

Mode	**Switches to be turned on**
1	Two switches that connect the link to an input phase pair with the highest instantaneous voltage
2	–
3	Two switches that connect the link to an input phase pair with the second-highest instantaneous voltage
4	–
5	Two switches that connect the link to an output phase pair with the highest or second-highest instantaneous current difference (whichever has lower voltage)
6	–
7	Two switches that connect the link to an output phase pair with the highest or second-highest instantaneous current difference (whichever has higher voltage)
8	–

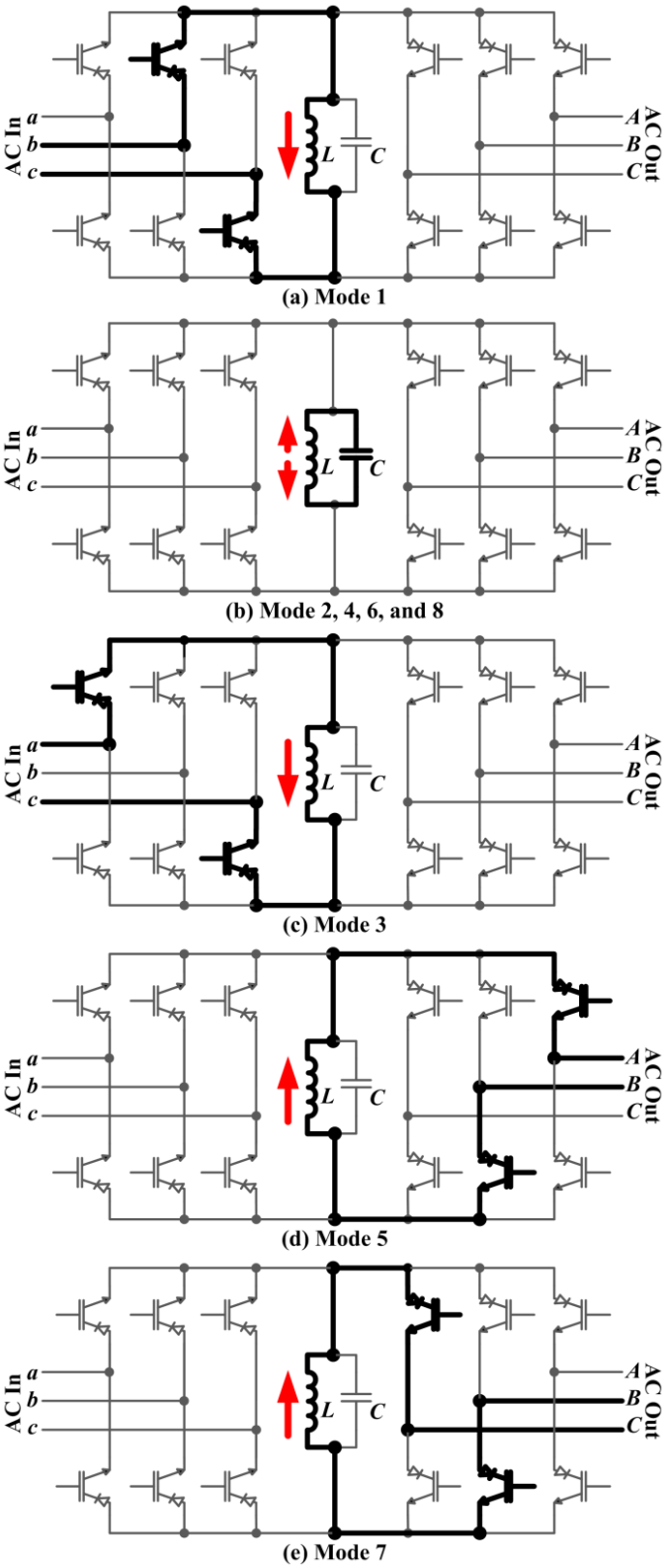

Fig. 4.2. Typical operating modes of the proposed converter.

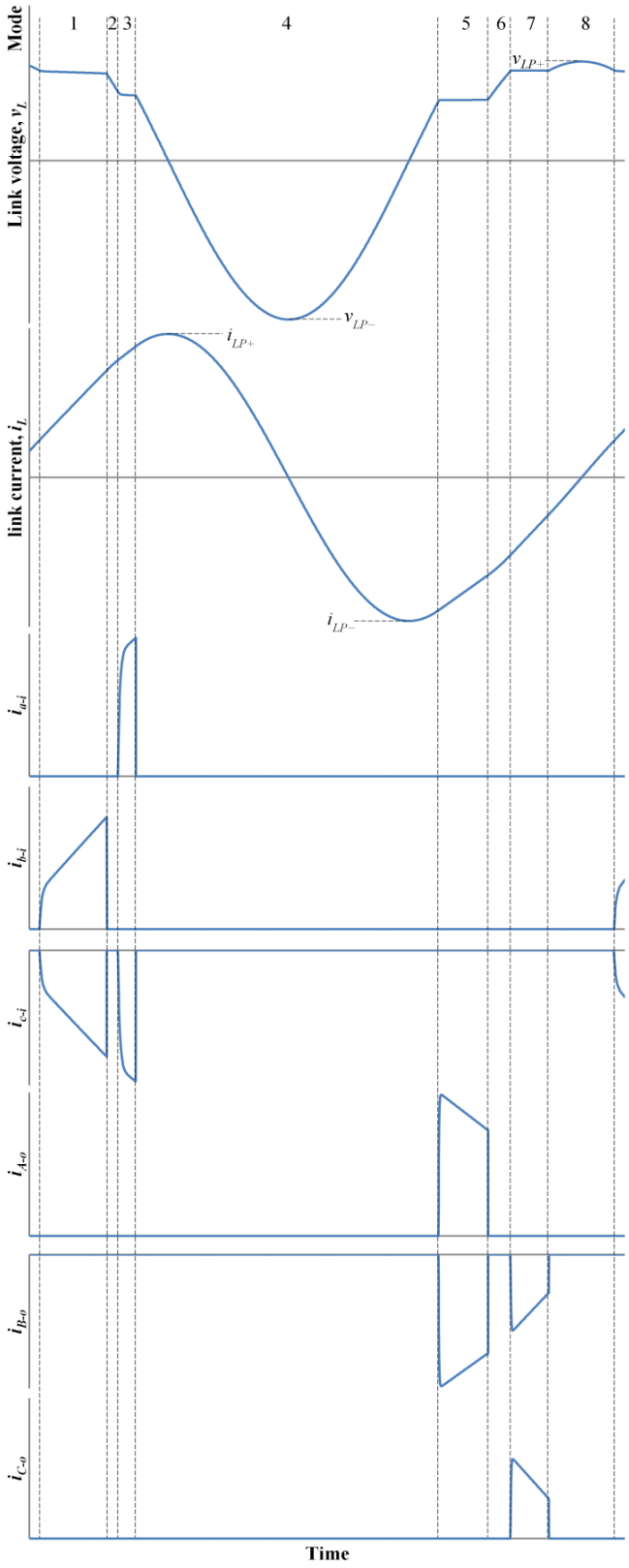

Fig. 4.3. Typical waveforms of the proposed converter. (a) link voltage, (b) link current, (c-e) input currents, (f-h) output currents.

Mode 3 (the link charges again): Two appropriate input-side switches are turned on to connect the second-highest input line-to-line voltage to the HFAC link. The link inductor continues to charge until the average input current of the two connected input phases meet their reference values. Since the sum of the three phase currents is zero, these two phases meet their references simultaneously. Afterwards, the switches are turned off.

Note that the mode-3 switches are turned on as soon as the link voltage is equal to the second-highest input line-to-line voltage. Thus, the switches turn on at zero voltage. All the converter's switches are turned on at zero voltage similarly.

Mode 4 (the link exhibits considerable resonance): By turning off the switches of mode 3, the link components start to resonate again. This resonance is allowed to continue until the link voltage is equal to the voltage of the mode-5 phase pair in the up-going direction. The proper selection of the mode-5 phase pair is discussed later. During this mode, the link current, $i_L(t)$, reaches its positive and negative peak values, i_{LP+} and i_{LP-}, which can be estimated according to the energy of the link at the end of mode 3 from the following:

$$i_{LP+} = -i_{LP-} = \sqrt{{i_L}^2(t_3) + \frac{C}{L}{v_L}^2(t_3)} \tag{4.2}$$

where t_3 is the time at the end of mode 3. In addition, the link voltage reaches its negative peak value in this mode, v_{LP-}, as follows:

$$v_{LP-} = -\sqrt{{v_L}^2(t_3) + \frac{L}{C}{i_L}^2(t_3)} \tag{4.3}$$

Two proper output phase pairs need to be chosen for the discharging modes 5 and 7. As the load may have a non-unity power factor, the phase reference currents are considered for the selection of the output phase pairs (remember that for the selection of the input phase pairs in modes 1 and 3, phase pair voltages were considered since the input power factor was

considered as one). The two phase pairs with the highest and second-highest instantaneous current difference at the instant are chosen for this purpose. Among these two, the phase pair that has a lower instantaneous voltage is chosen for mode 5, and the other phase pair is selected for mode 7. This procedure is mainly done to minimize the duration of the resonant modes.

Mode 5 (the link discharges to output): Two load-side switches are turned on at zero voltage to discharge the link inductor to the chosen output phase pair, as discussed before. When the average current of one of the connected phases meets its reference value, this mode ends and the switches are turned off.

Mode 6 (the link exhibits partial resonance): The link components resonate together until the link voltage is equal to the voltage of the selected phase pair for mode 7.

Mode 7 (the link discharges to output again): The switches corresponding to the chosen phase pair are turned on to discharge the link inductor to these two phases. These switches are turned off after the link current reaches a small value of $i_L(t_7)$, which is defined as the link current at the end of mode 7 and will be formulated later. Considering the input-output power balance, the average currents of the connected phases meet their reference values at the end of this mode.

Mode 8 (the link exhibits partial resonance): The link components resonate together again. This partial resonance is maintained until the link voltage is equal to the highest input line-to-line voltage, which then permits the converter to go to mode 1 with zero voltage switching. For this procedure to occur properly, a certain amount of current should be left in the link at the end of mode 7 so that the link voltage peaks at a determined amount above the

input highest line-to-line voltage, as shown in Fig. 4.3. So, the link current at the end of mode 7 should be as follows:

$$i_L(t_7) = -\sqrt{\frac{C}{L}\left(V_{LP+}^2 - {v_L}^2(t_7)\right)} \tag{4.4}$$

where t_7 is time at the end of mode 7, and V_{LP+} is the pre-determined link peak voltage. V_{LP+} can be chosen 10% to 15% higher than the input peak line-to-line voltage. In case that $v_L(t_7)$ is more than V_{LP+}, there is no need to leave any energy in the link inductance at the end of mode 7 and $i_L(t_7)$ can be selected as zero.

In order to transfer power from the output to the input of the converter, the input and output modes can simply be exchanged. In this way, the link is charged from the output in modes 1 and 3, and after a resonant mode to change its current direction, it is discharged to the input in modes 5 and 7 in a similar way.

4.2.3. The Converter's Operation and ZVS in Different Line And Load Conditions

The control algorithm of the converter specifies two input phase pairs to charge the link inductor in modes 1 and 3 and two output phase pairs for the link inductor to be discharged to them in modes 5 and 7. Zero-voltage turn-on happens for the converter's switches due to turning on the switches when the link voltage is equal to the desired input or output voltage. In addition, ZVS occurs at the turn-off of the power switches owing to the existence of the link capacitor, which does not allow the switch voltages to change rapidly. The control algorithm operation and the resultant soft switching behavior does not depend on the voltage values or load condition and can be achieved effectively in the ac cycle. To verify the converter's operation in the course of an input ac cycle, the 6 input phase-pair voltages are shown in Fig. 4.4. According to the control algorithm, the mode-1 link voltage, v_1, is

equal to the highest instantaneous input line-to-line voltage. As the figure shows, v_1 can be between $\sqrt{1.5}V_{Li}$ and $\sqrt{2}V_{Li}$. The mode-3 link voltage, v_3, is also shown in the figure, which is equal to the second-highest instantaneous voltage and varies between $\sqrt{0.5}V_{Li}$ and $\sqrt{1.5}V_{Li}$. Note that the described control algorithm of the converter is not limited to a specified voltage for each mode; based on the control algorithm, the charging modes 1 and 3 continue until their respective reference currents are met. Since v_1 and v_3 changes slightly over the course of the input ac cycle, the durations of charging modes also change slightly over the ac cycle. As a result, the link frequency also slightly varies in the course of the ac cycle. According to Fig. 4.4, v_1 is higher or equal to v_3; when v_1 is higher than v_3, the soft transition between the charging modes (and the subsequent ZVS) is realized through the resonant mode 2. v_1 and v_3 become equal when $\omega = \frac{\pi}{6}, \frac{\pi}{2}, \frac{5\pi}{6}, \ldots$, which means that there is no mode 2 at those instances and the converter goes directly and softly to mode 3 after mode 1.

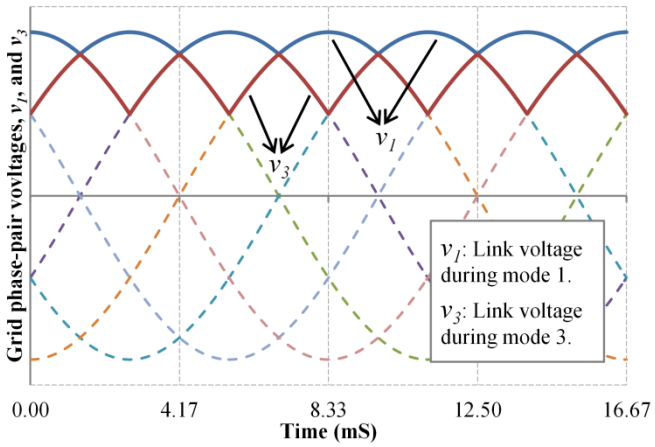

Fig. 4.4. Grid phase-pair voltages, v_1, and v_3.

As the link inductor is charged from the input and then discharged to the output, there is no direct power transfer from the input to the output of the converter. According to (4.1), output power is the only output parameter that affects the input reference currents, and consequently, the charging modes. By changing the output power, the durations of modes 1 and 3 change to meet the new reference current values. Therefore, as long as the output power is constant, the change of output conditions, such as output voltage during the ac cycle, output frequency, or power factor, does not have any effect on the charging modes.

In the case that the output power factor is one, the converter behavior at the output is the same as the input and the above discussions can be applied directly. In this case, the mode-5 link voltage and mode-7 link voltage are equal to the second-highest and highest instantaneous output line-to-line voltages, respectively. As stated by the introduced control algorithm, in the general case with a non-unity load power factor, the output phase pairs are selected based on their current differences and sorted according to their voltages. Therefore, the range of the link voltages in modes 5 and 7 depend on the power factor in this general case. However, as the link voltages in these discharging modes are sorted in the ascending order, the soft transition between these modes and the resulting ZVS happens flawlessly. It should be note that if the load power factor falls lower than a certain value, leading or lagging, the mode-5 link voltage becomes negative, which leads to the incorrect operation of the converter.

4.2.4. The Analysis and Design of the Converter

The arrangement of the line and phase voltages of a three phase system changes every *π/6 rad*, so the first *π/6 rad* will be considered for the converter analysis. In this interval,

phase pair *cb* has the highest voltage, and according to the converter's operating principle, it is applied to the HFAC link in mode 1. Hence, the link average voltage in mode 1 can be given by,

$$V_{1,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} v_{cb}\, d(\omega t) = \frac{3\sqrt{2}}{\pi} V_{Li} \tag{4.5}$$

where V_{Li} is the input line-to-line rms voltage. Consequently, the link average current in mode 1 is equal to the average current of phase *c* in this interval as follow:

$$I_{1,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} i_c\, d(\omega t) = \frac{3\sqrt{2}(\sqrt{3}-1)}{\pi} I_{Pi} \tag{4.6}$$

where I_{Pi} is the input phase rms current. Phase pair *ab* has the second highest voltage and is applied to the HFAC link in mode 3. Therefore, the average voltage and current of the link in mode 3 can be given by,

$$V_{3,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} v_{ab}\, d(\omega t) = \frac{3\sqrt{2}(\sqrt{3}-1)}{\pi} V_{Li} \tag{4.7}$$

$$I_{3,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} i_a\, d(\omega t) = \frac{3\sqrt{2}(2-\sqrt{3})}{\pi} I_{Pi} \tag{4.8}$$

The link voltage peaks at V_{LP+} during mode 8 and is equal to $V_{1,ave}$ at the end of this operating mode. Hence, the average of the link current at the end of mode 8 can be written as follows:

$$I_8 = \sqrt{\frac{C}{L}\left({V_{LP+}}^2 - {V_{1,ave}}^2\right)} \tag{4.9}$$

Note that "I_x" is expressed as the average of the link current at the end of mode "*x*", and "$I_{x,ave}$" is defined as the average link current during mode "*x*". Knowing that the average of the link current in mode 1 meets $I_{1,ave}$, the average duration of mode 1, T_1, and I_1 can be given by,

$$T_1 = -\frac{LI_8}{V_{1,ave}} + \sqrt{\left(\frac{LI_8}{V_{1,ave}}\right)^2 + \frac{2LTI_{1,ave}}{V_{1,ave}}} \tag{4.10}$$

$$I_1 = \frac{V_{1,ave}T_1 + LI_8}{L} \tag{4.11}$$

where T is the average period of the link cycle. By ignoring the small change of the link current in mode 2, the average length of mode 3 and I_3 can be obtained similarly from the following:

$$T_3 = -\frac{LI_1}{V_{3,ave}} + \sqrt{\left(\frac{LI_1}{V_{3,ave}}\right)^2 + \frac{2LTI_{3,ave}}{V_{3,ave}}} \tag{4.12}$$

$$I_3 = \frac{V_{3,ave}T_3 + LI_1}{L} \tag{4.13}$$

Assuming a unity load power factor, the average of the link voltages, currents, and duration of operating modes 5 and 7 are similar to modes 3 and 1, respectively, as follows:

$$V_{5,ave} = \frac{3\sqrt{2}(\sqrt{3}-1)}{\pi} V_{Lo} \tag{4.14}$$

$$V_{7,ave} = \frac{3\sqrt{2}}{\pi} V_{Lo} \tag{4.15}$$

$$I_{5,ave} = -\frac{3\sqrt{2}(2-\sqrt{3})}{\pi} I_{Po} \tag{4.16}$$

$$I_{7,ave} = -\frac{3\sqrt{2}(\sqrt{3}-1)}{\pi} I_{Po} \tag{4.17}$$

$$T_5 = \frac{LI_6}{V_{5,ave}} + \sqrt{\left(\frac{LI_6}{V_{5,ave}}\right)^2 - \frac{2LTI_{5,ave}}{V_{5,ave}}} \tag{4.18}$$

$$T_7 = \frac{LI_7}{V_{7,ave}} + \sqrt{\left(\frac{LI_7}{V_{7,ave}}\right)^2 - \frac{2LTI_{7,ave}}{V_{7,ave}}} \tag{4.19}$$

where V_{Lo} is the output line-to-line rms voltage, I_{Po} is the output phase rms current, and I_6 is given by,

$$I_6 = \frac{-V_{7,ave}T_7 + LI_7}{L} \tag{4.20}$$

I_7 can be found by substituting (15) in (4). The average lengths of mode 4 and 8 can be expressed by,

$$T_4 = \sqrt{LC}\left[\pi + \sin^{-1}\left(\frac{V_{3,ave}}{-V_{LP-}}\right) + \sin^{-1}\left(\frac{V_{5,ave}}{-V_{LP-}}\right)\right] \tag{4.21}$$

$$T_8 = \sqrt{LC}\left[\pi - \sin^{-1}\left(\frac{V_{7,ave}}{V_{LP+}}\right) - \sin^{-1}\left(\frac{V_{1,ave}}{V_{LP+}}\right)\right] \tag{4.22}$$

As mentioned earlier, V_{LP+} is a pre-determined value higher than the input peak line voltage and V_{LP-} can be found by substituting (4.7) and (4.13) in (4.3). The duration of short modes 2 and 6 can be found in a similar way. Finally, the sum of the time intervals of all the operating modes is equal to the average link period, T, which results in a set of implicit equations. Fig. 4.5 shows the average of the link frequency, link peak current, and link negative peak voltage of the introduced converter versus the link capacitor for various values of the link inductor. According to the figure, as the link capacitor decreases, the link negative peak voltage also decreases. This is because the lessening of the link capacitor decreases the duration of resonant mode 4; therefore, according to the inductor volt-second balance principle, the link voltage should peak at the lower negative voltage to have a zero average voltage. Thus, the decrease of the link capacitor increases the link frequency and declines the link peak current. As Fig. 4.5 shows, these three mentioned parameters also depend on the link inductor value, and the reduction of the link inductor increases the link frequency, link peak current, and link negative peak voltage.

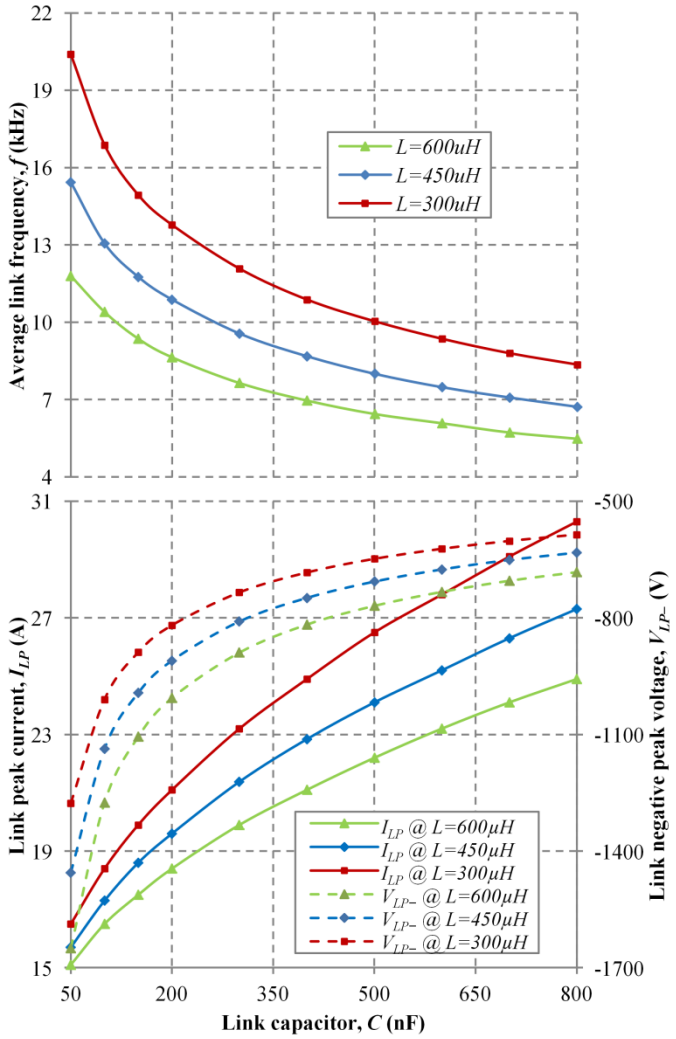

Fig. 4.5. Average link frequency, link peak current, and link negative peak voltage versus link capacitance for various values of the link inductance, V_{Li}=V_{Lo}=208V, P_{out}=750W.

By using the graph of the converter's main parameters versus the link inductor and capacitor for a given input-output operating point (Fig. 4.5), the link components can be selected optimally for the desirable performance of the proposed converter. Note that the link peak current specifies the conduction loss of the switches and the inductor power loss; therefore, lowering the link peak current yields smaller power losses on the switches and inductor. On the other hand, the link negative peak voltage determines the peak forward

voltage of the input-side switches and peak reverse voltage of the output-side switches as will be formulated later. In order to decrease these switch voltage stresses, the magnitude of the link negative peak voltage should be reduced. In addition, it is desirable to increase the link frequency as high as possible to shrink the size of passive components. However, the link frequency should be much smaller than the sampling frequency of the converter's digital controller to operate effectively. As Fig. 4.5 demonstrates, it is impossible to drop the link peak current and link negative peak voltage magnitude together; decreasing C or increasing L results in a smaller link peak current but a higher link negative peak voltage magnitude while increasing C or decreasing L has the reverse effect. Therefore, a trade-off should be made between the power losses of the switches and inductor on one side and the voltage stress on the switches on the other side. As shown later in the experimental results section, typical 900V IGBTs were used, and the sampling time of the digital controller was 3.5μsec. Therefore, the link inductor and capacitor were selected as 450μH and 400nF to set the switch peak voltages at 540V and the link frequency at 8.7kHz for the given operating point. The link frequency can be moved higher, provided a faster digital controller is used.

Fig. 4.6 displays the graph of the average link frequency, link peak current, and link negative peak voltage by the change of the output active power. According to the figure, the absolute value of the link negative peak voltage and the link peak current are completely dependent on the output power, and as the output power reduces, they both decrease almost linearly. On the other hand, the link frequency increases slowly by decreasing the output power. The link frequency, link peak current, and link negative peak voltage of the proposed converter at a very small output power are obtained from the following:

$$f|_{P_{out}\approx 0} = \frac{1}{2\pi\sqrt{LC}} \tag{4.23}$$

$$I_{LP}|_{P_{out}\approx 0} = \sqrt{\frac{C}{L}} V_{LP+} \tag{4.24}$$

$$V_{LP-}|_{P_{out}\approx 0} = -V_{LP+} \tag{4.25}$$

It can be shown that the peak forward voltage and peak reverse voltage of the input-side switches, PFV_I and PRV_I, are given by,

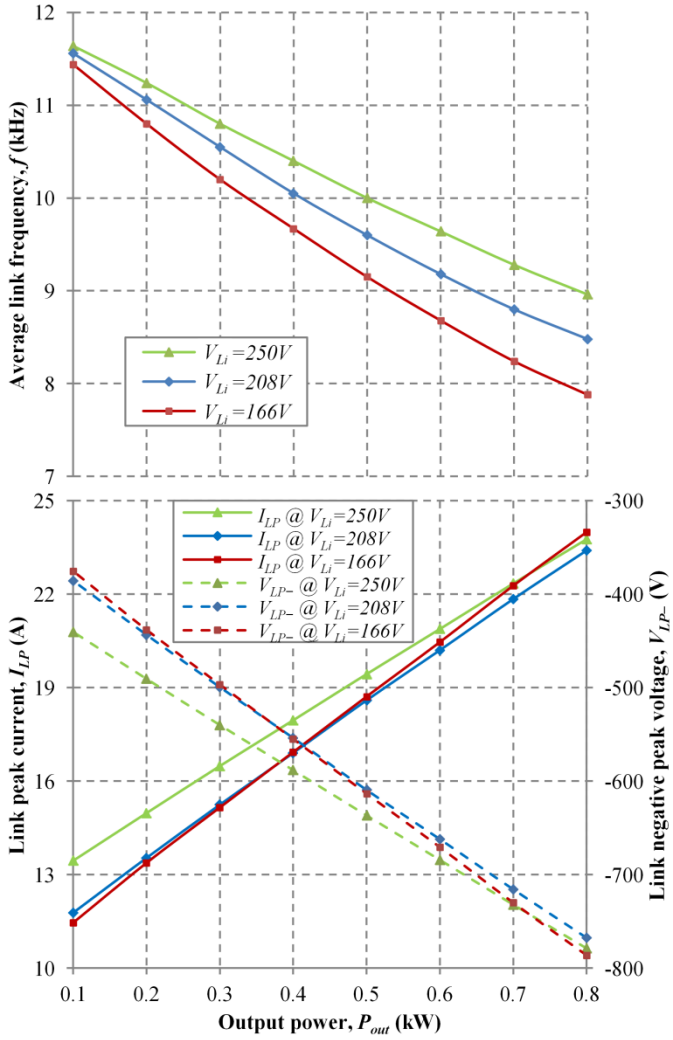

Fig. 4.6. Average link frequency, link peak current, and link negative peak voltage versus output active power for various values of the input line voltage, V_{Lo}=208V, L=450µH, and C=400nF.

$$PFV_I = \sqrt{\frac{2}{3}} V_{Li} - \frac{1}{2} V_{LP-} \tag{4.26}$$

$$PRV_I = \sqrt{\frac{2}{3}} V_{Li} + \frac{1}{2} V_{LP+} \tag{4.27}$$

and the peak forward voltage and peak reverse voltage of the output-side switches, PFV_O and PRV_O, can be expressed by,

$$PFV_O = \sqrt{\frac{2}{3}} V_{Lo} + \frac{1}{2} V_{LP+} \tag{4.28}$$

$$PRV_O = \sqrt{\frac{2}{3}} V_{Lo} - \frac{1}{2} V_{LP-} \tag{4.29}$$

4.2.5. Simulation Results

To validate the model presented, a computer simulation was carried out. The introduced ac-ac converter was designed for a 1kVA load at 0.75PF lagging with the input and output voltages of 208V/60Hz. The link inductor and capacitor were selected as 450μH and 400nF, and V_{LP+} was adjusted as 325V (10% higher than the input peak line voltage). Fig. 4.7 depicts the simulation results of the link voltage and current at these test conditions. As the figure clearly shows, the link inductor is charged through two input phase pairs in modes 1 and 3. Next, the link inductor and capacitor are allowed to resonate until the link current changes its direction (mode 4). The link inductor is then discharged to two output phase pairs in mode 5 and 7. Finally, the link resonates again during mode 8 to go back to mode 1. Although the duration of resonant modes 2 and 6 are very small, these modes provide soft transition among modes 1 to 3 and modes 5 to 7. As mentioned before, the voltage of the selected phase pair for each mode varies slightly with time; therefore, the link voltage and duration of mode change slightly by time too. The average link frequency, link

peak current, and link negative peak voltage at full load were measured as 8.6kHz, 22.6A, and −742V respectively. These results are in agreement with the analysis results as shown in Fig. 4.6 (note that the output active power is 750W). The simulation also showed the average and rms currents of the converter's switches as 1.1A and 4A. In addition, the peak forward and reverse voltages of the input-side switches were expected as 540V and 330V while these values for the load-side switches were 330V and 540V.

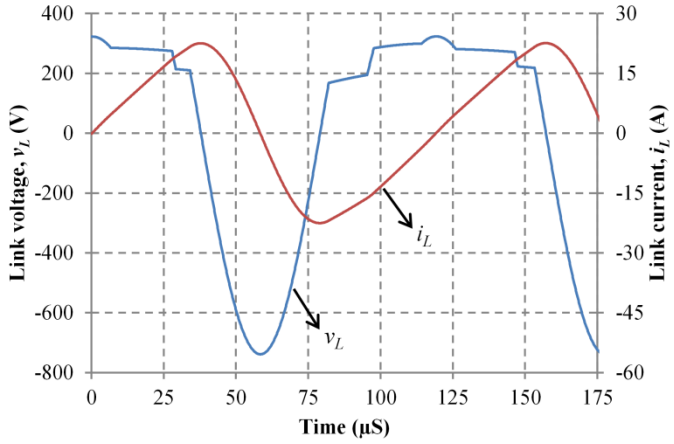

Fig. 4.7. Simulation results of the proposed converter at 1kVA, including the link voltage and link current.

Fig. 4.8 shows the simulation results of converter's input and output currents at the mentioned test conditions. An intentional phase shift was made between the input and output currents to show that there is no direct power transfer from the input to the output. To filter out high-frequency harmonics from the input and output waveforms, applicable low-pass filters was employed. The proper configurations of the second-order low-pass filters at the input and output sides are shown in Fig. 4.1: LC at the input side and CL at the output side. In these configurations, there are continuity paths for the input, output, and filter inductor

currents when the switches are turned off. According to (4.1), the displacement power factor (DPF) of the input unfiltered currents ($i_{a\text{-}i}$, $i_{b\text{-}i}$, and $i_{c\text{-}i}$) is adjusted to 1. However, the input-side filter also drifts the phase angle slightly and drops the input power factor from one. A stronger low-pass filter yields a lower power factor at the input side. Therefore, a compromise should be made between the harmonic contents of the input currents and the input power factor when designing the input-side filter. The input power factor was measured as 0.97 leading at these test conditions while the input current THD is acceptable as shown in Fig. 4.8. This verifies that although the load has a non-unity power factor (0.75 lagging), the input power factor of the proposed converter remains at almost unity. This is due to the fact that there is no direct power transfer from the input to the output. It should be noted that if the load power factor drops significantly (leading or lagging) so that it effectively cancels out the output low-pass filter of the converter or strengthens it too much, the converter will fail to operate appropriately.

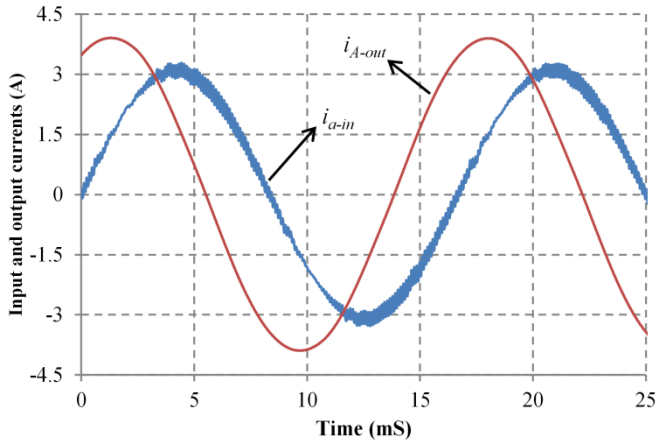

Fig. 4.8. Simulation results of the proposed converter at 1kVA, including the input current of phase *a* and output current of phase *A*.

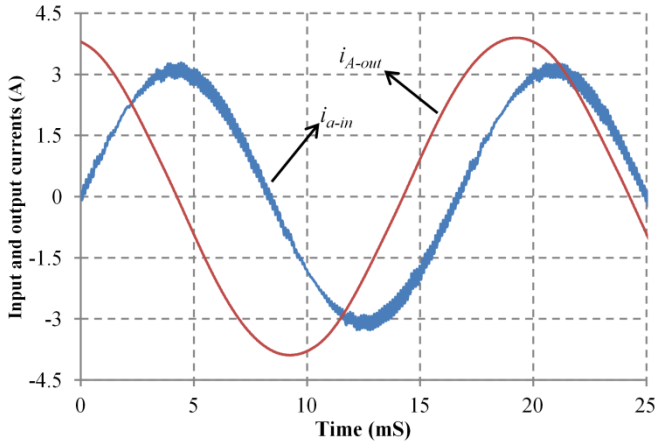

Fig. 4.9. Simulation results of the proposed converter at 1kVA/50Hz, including the input current of phase *a* and output current of phase *A*.

If the input or output voltage is modified or the output power or frequency needs to be changed, the input and output reference currents and V_{LP+} should be simply adjusted in the control algorithm for the proper operation of the converter. The simulation results of the converter with the output frequency of 50Hz at 1kVA test conditions are displayed in Fig. 4.9. Compared to Fig. 8, the input current waveform was not affected while the frequency of the output current has changed. Because the output power and voltage amplitude of this test are the same as the test with the output frequency of 60Hz, the link voltage and current waveforms remain the same as the one in Fig. 4.7. In essence, the analysis results shown in Figs. 4.5 and 4.6 are valid for different input and output frequencies as long as the link frequency is much higher than the input and output frequencies. Fig. 4.10 shows the simulation results of the link voltage and current of the converter when the load is reduced to 0.5kVA/60Hz at 0.75PF lagging at the same output voltage. The figure clearly illustrates that the proposed converter is properly working using the described control algorithm while achieving ZVS. As the figure displays, the magnitudes of the link negative peak voltage and

the link peak current are reduced while the link frequency is increased in agreement with Fig. 4.6.

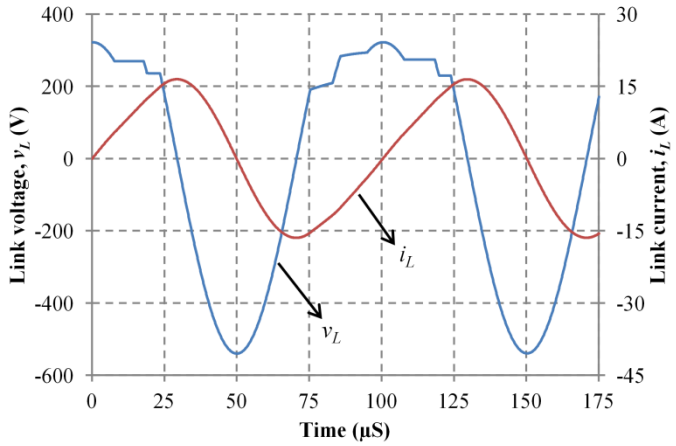

Fig. 4.10. Simulation results of the proposed converter at 0.5kVA, including the link voltage and link current.

4.2.6. Experimental Results

A 750W/1kVA prototype of the introduced HFAC-link ac-ac resonant converter was designed to validate its performance. In order to control the converter, TMS320F28335 Delfino™ DSC was employed with the sample time of 3.5µsec. The link inductor and capacitor were selected as 450µH and 400nF. The converter prototype was run with the input voltage of 208V/60Hz to supply a 208V/60Hz, 1kVA load at 0.75PF lagging, similar to the simulation section. Fig. 4.11 shows the resulting link voltage and current, and Fig. 4.12 depicts the input and output currents. The input current waveform has higher harmonic contents in the experiment compared to simulation (the experimental waveform has low-frequency harmonics), which is mainly due to the distortion in the utility voltage and natural resonance of the input filter. The average link frequency, link peak current, and link negative

peak voltage at this test condition were about 8.4kHz, 23.3A, and −756V respectively, which are very close to the results of the analysis and simulation sections. The small differences are primarily because of the non-linearity and power loss of the components. The current and voltage waveforms of an input-side switch are shown in Fig. 4.13. As the figure shows, the switch voltage at both turn-on and turn-off is almost zero.

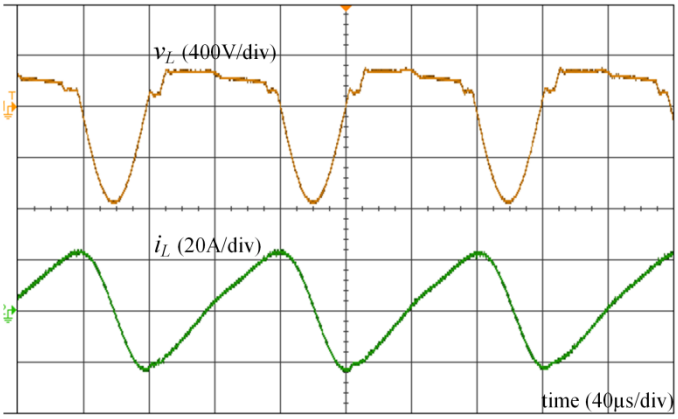

Fig. 4.11. Experimental results of the converter at 1kVA in the normal operation. Link voltage, and link current.

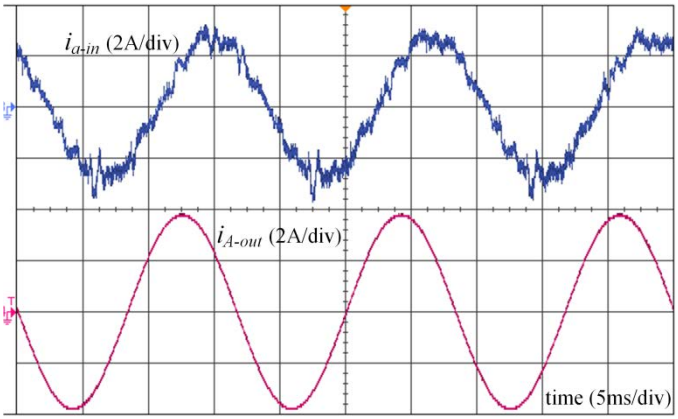

Fig. 4.12. Experimental results of the converter at 1kVA in the normal operation. Input current of phase *a*, and output current of phase *A*.

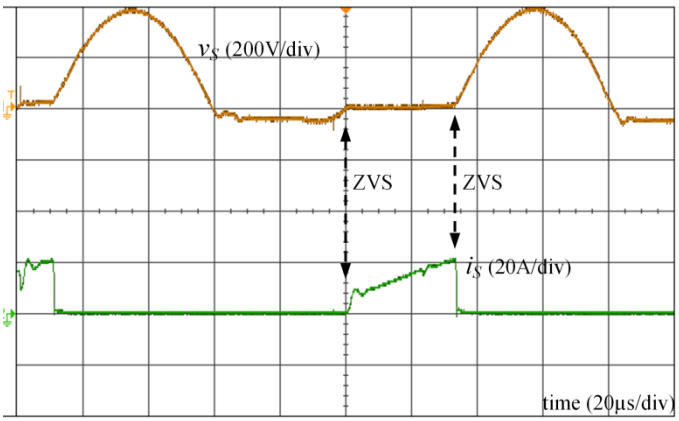

Fig. 4.13. Experimental results of an input-side switch. Switch voltage, and switch current.

To verify the proposed converter operation in the step-up and step-down conditions, two more experiments were run. Figs. 4.14 and 4.15 show the converter operations with the input voltage of 104V/60Hz and 312V/60Hz respectively (±50% of the nominal input voltage.) The load in both cases was 208V/60Hz, 1kVA at 0.75PF lagging, similar to the first experiment. The average link frequency, link peak current, and link negative peak voltage for the step-up case was 6.4kHz, 25.7A, and −835V respectively. These values for the step-down operation were 9.3kHz, 24.8A, and −812V respectively. As the result shows, the converter is completely capable of the step up/down operation. Fig. 4.16 shows the analysis results of the link negative peak voltage and the link peak current versus the input voltage at the mentioned test conditions. According to the figure, the magnitudes of the link negative peak voltage and the link peak current reach their minimum values when the input voltage is almost equal to the output voltage. As the input voltage goes lower or higher than the output voltage, the magnitudes of these parameters increase slightly. Their increase can be significant if the input voltage is modified substantially (approximately a 40% increase in both when the input voltage reaches 50V). Therefore, the maximum and minimum of the converter's voltage

transfer ratio is practically limited by the voltage rating and allowable power loss of the switches and inductor. Fig. 4.17 shows the conversion efficiency of the designed converter versus output load for various values of the input line voltage. The measured efficiency and the input power factor at the nominal conditions were 93.4% and 0.97 leading respectively.

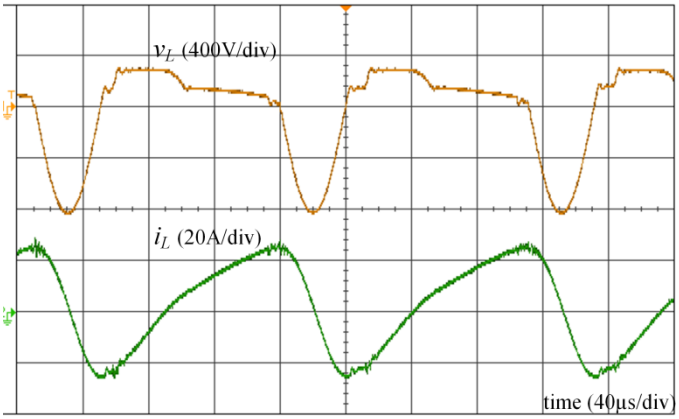

Fig. 4.14. Experimental results of the converter at 1kVA in the step-up operation. Link voltage, and link current.

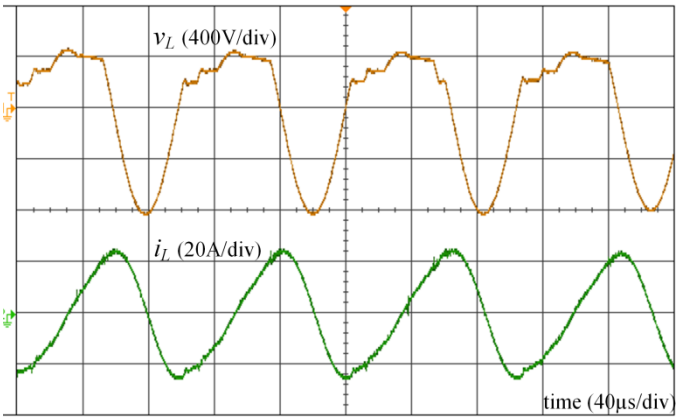

Fig. 4.15. Experimental results of the converter at 1kVA in the step-down operation. Link voltage, and link current.

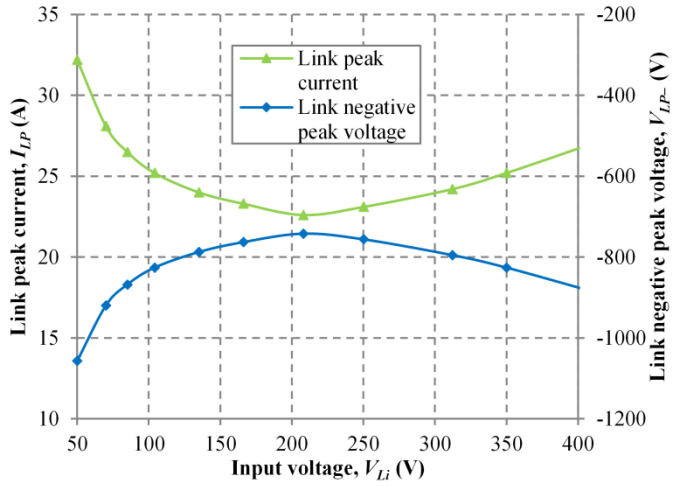

Fig. 4.16. Link peak current and link negative peak voltage versus input voltage for V_{Lo}=208V, P_{out}=750W, L=450µH, and C=400nF.

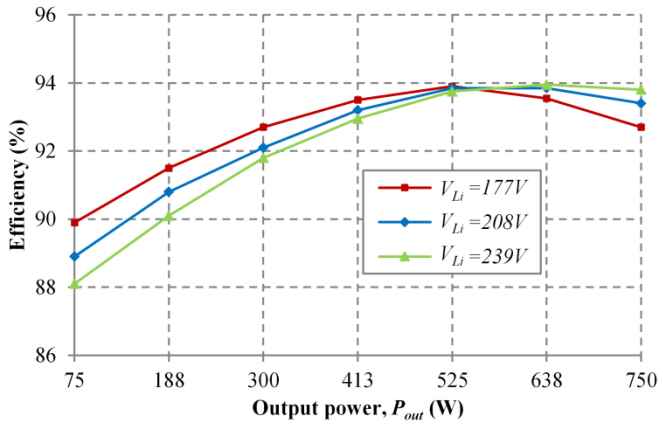

Fig. 4.17. Efficiency of the converter prototype versus output power for different values of the input line voltage.

4.3. Step-Up/Down Three-Phase Resonant High-Frequency AC-Link Inverters

4.3.1. Introduction

Several soft-switched dc-ac converters have been proposed in the literature [10], [100]. In general, they can be classified by the position of the resonant circuit as load resonant [101]–[104], resonant transition [105]–[109], and resonant link inverters [110]–

[117]. As the LC tank is added at the load side in the load resonant converters, they are mainly limited to constant load applications and their switches suffer from high voltage and current stresses. Resonant transition converters mostly employ the parasitics of the circuit to achieve soft switching for the power switches. Although their switching frequency is constant, they typically have a higher component count and the increased control complexity required to obtain the resonant switching transition [100]. Resonant link inverters employ the resonant network between the input and the inverter bridge. Therefore, the link voltage or current oscillates in order to create the soft-switching conditions for the power devices [10], [100]. According to the resonant network configuration and the switching scheme, the resonant link topologies can be subdivided into series and parallel dc links [110]–[115], and series and parallel ac links [24], [116], [117].

This study introduces new parallel-resonant high-frequency ac (HFAC) link inverters with the step-up/down capability. An ac inductor in parallel with a small ac capacitor makes the HFAC link without the use of bulky short-life electrolytic capacitors. The HFAC link transfers power at a high frequency while achieving soft-switching operation; direct power transfer from the input to the output does not exist. In addition, the maximum output voltage is not limited to the dc-bus voltage, and the converter has the ability to operate easily in the buck and boost operation modes in both forward and reverse directions. The proposed three-phase inverter can provide galvanic isolation using a single-phase high-frequency (HF) transformer, which has a noticeably small size and low weight compared to traditional line-frequency three-phase isolation transformers. Therefore, this topology is suitable for industrial applications where a small size with high performance is critically desired, such as

aerospace applications, compact efficient variable-speed drives, and renewable energy systems. The proposed topology can also be considered for three-phase microinverter.

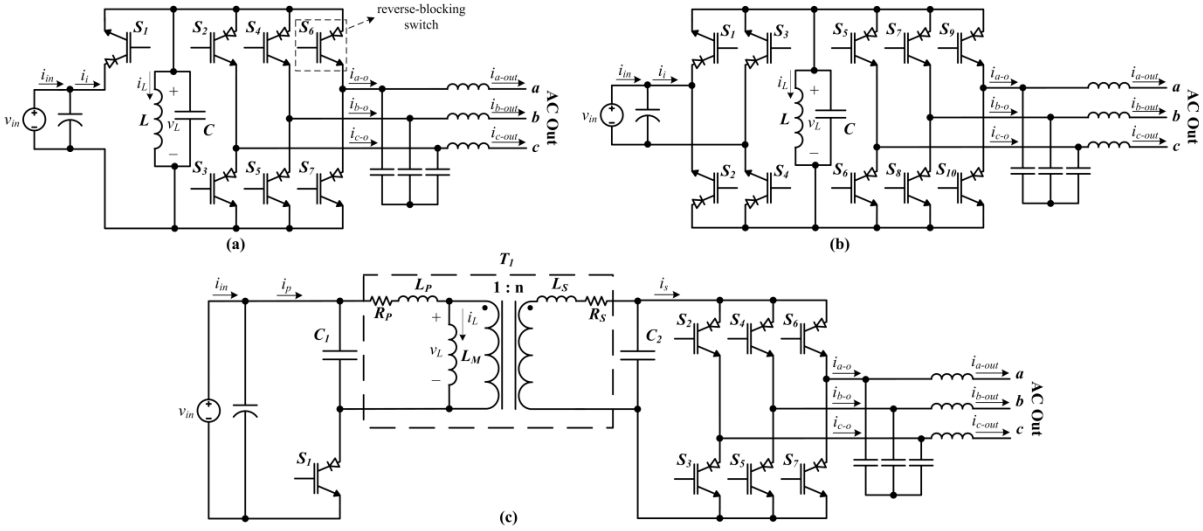

Fig. 4.18. The proposed parallel resonant HFAC-link dc-ac converters. (a) the basic unidirectional topology, (b) the bidirectional topology, and (c) the isolated unidirectional topology.

4.3.2. Topology Description

Fig. 4.18(a) shows the basic unidirectional topology of the proposed parallel-resonant dc-ac converter with a HFAC link and soft-switching operation. The HFAC link is composed of the inductor L and parallel capacitor C. The link capacitor, C, is a considerably small capacitor with an ac voltage operation; therefore, highly-reliable ac capacitors can be used for it. The link inductor, L, also carries an ac current; so, it is smaller and more efficient than dc-current inductors due to full use of the magnetic core in both positive and negative directions. In general, power transfer from input to output is accomplished via the link inductor, which is charged from the input voltage and then discharged to the output phases

with a precisely controllable current technique. The link capacitor produces partial resonance to realize the soft switching condition for the power devices, as will be shown later. The small filters at the input side and load side of the converter suppress switching-frequency harmonics.

As shown in Fig. 4.18(a), the converter's switches need to have reverse blocking capability. A reverse-blocking (RB) switch can be realized by a conventional reverse-conducting (RC) switch in series with a diode. However, the newly-available individual RB-switches can be employed for this purpose with the advantage of lower total on-state voltage. Bidirectional power flow can be provided by replacing the converter's switches with bidirectional switches. Fig. 4.18(b) presents a more effective topology for the bidirectional operation. The four input-side switches in this topology can create a forward path to charge the link from the input as well as a reverse path to charge the input from the link. Galvanic isolation can be provided by replacing the link inductor with a small single-phase high-frequency transformer as shown in Fig. 4.18(c). As the operating frequency of the transformer T_1 is the same as the switching frequency, it yields a much smaller transformer compared to line-frequency three-phase transformers. In order to have an appropriate link inductance value, the transformer may need to have an air gap. Instead of one link capacitor, two smaller capacitors C_1 and C_2 are placed on both sides of the transformer T_1 in this topology. These capacitors provide paths for the currents of the primary and secondary leakage inductances when the input or output switches are turned off in order to avoid voltage spikes. The bidirectional isolated topology can also be made by employing a high-frequency transformer in the Fig. 4.18(b) topology in a similar way.

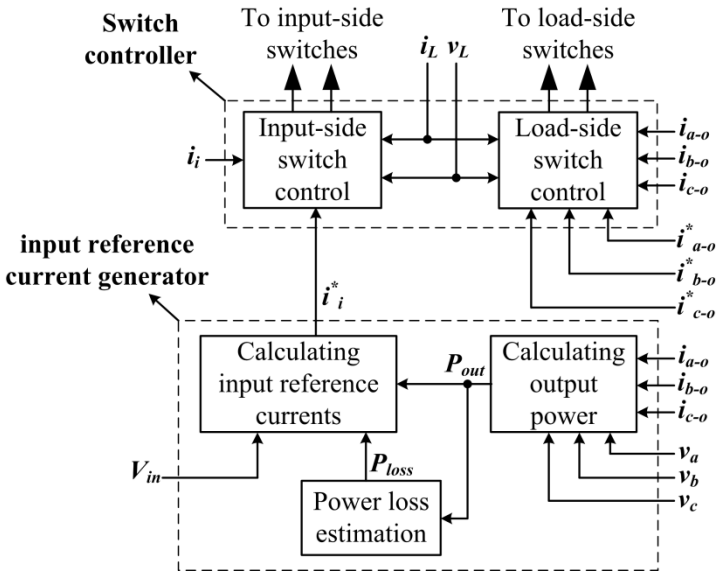

Fig. 4.19. The control scheme of the proposed soft-switched inverter.

4.3.3. The Operation of the Proposed Converters

Fig. 4.19 shows the control scheme of the proposed converters. According to the figure, the control scheme is composed of two sections: the input reference current generator and the switch controller. The first section generates the input reference currents, i^*_i, according to the calculated output power and the estimated power loss of the converter from the following:

$$i_i^* = \frac{P_{out}+P_{loss}}{\mathrm{V}_{in}} \tag{4.30}$$

where V_{in} is the input dc voltage, P_{out} is the output active power of the converter, and P_{loss} is its estimated power loss. As P_{loss} is normally much smaller than the P_{out}, the converter operation is not highly sensitive to the exact value of the P_{loss}. The introduced topology is fundamentally a current-source inverter, and consequently, the reference currents of the output phases, i^*_{a-o}, i^*_{b-o}, and i^*_{c-o}, are required for the inverter operation. The input and

output reference currents are sent to the switch controller section. In this section, the converter's switches are managed properly so that the input and output currents meet their reference values at each switching cycle. As a result, by using a small low-pass filter at the front and load ends, desired input and output currents are achieved. In order to do this, the switch controller section employs an algorithm at a high operating frequency that is described below.

The operation of the introduced soft-switching HFAC-link converter topology consists of six modes of operation in each link cycle. Briefly, in forward power direction, the link inductance charges through the input in mode 1, and then it discharges to the output phases in modes 3 and 5. The even-numbered modes are for partial resonance of the link inductance with its parallel capacitance to achieve zero-voltage switching. A typical link cycle of the isolated unidirectional topology is shown in Fig. 4.20. The modes of operation of this converter are explained in detail as follows. The transformer parasitics elements, primary and secondary leakage inductances and resistances, are not considered now. Their effect will be shown later.

Mode 1 (link charges): The input-side switch of the converter is turned on so as to connect the input dc voltage to the HFAC-link. As a result, the link inductance, L_M, starts to charge in the positive direction. This mode is allowed to continue until the average input current meets its reference value, i^*_i. Subsequently, the switch is turned off.

In the turn-off process of the input-side switch, due to the existence of the link capacitance, the voltage of the switch goes up slowly. As a result, the switch turns off at almost zero voltage. This soft switching operation happens at the turn-off of the other converter's switches similarly.

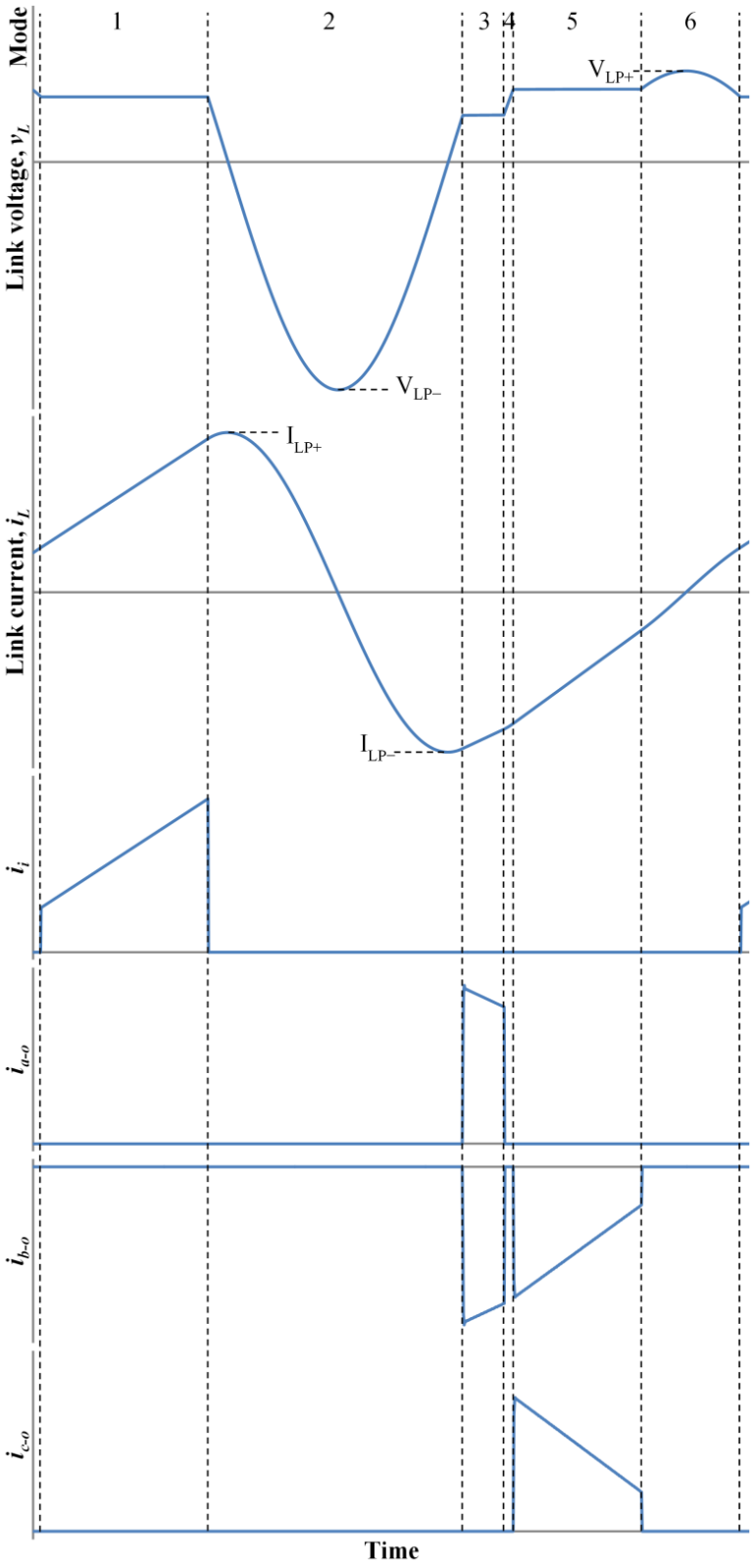

Fig. 4.20. Typical waveforms of the proposed resonant converter. (a) link voltage, (b) link current, (c) input current, and (d-f) output currents.

Mode 2 (link resonates considerably): The link inductance starts to resonate with the link capacitances, C_1 and C_2. This resonance is continued until the link voltage, $v_L(t)$, becomes equal to the reflected voltage of the selected output phase pair in the up-going direction. The proper selection of the output phase pairs will be discussed later. During this mode, the link voltage reaches its negative peak value, V_{LP-}, which can be found according to the energy of the link at the end of mode 1 as follows:

$$V_{LP-} = -\sqrt{{V_{in}}^2 + \frac{L_M}{C_1+n^2C_2}{i_L}^2(t_1)} \tag{4.31}$$

where t_1 is the time at the end of mode 1, and n is the transformer turns ratio. In mode 2, The link current, $i_L(t)$, also reaches its positive and negative peak values, I_{LP+} and I_{LP-}, which can be expressed by,

$$I_{LP+} = -I_{LP-} = \sqrt{{i_L}^2(t_1) + \frac{C_1+n^2C_2}{L_M}{V_{in}}^2} \tag{4.32}$$

Two output phase pairs should be selected for discharge modes 3 and 5. The two phase pairs that have the highest and second-highest current difference at the instant are chosen for this purpose. Among these two phase pairs, the one with lower voltage is chosen for mode 3 and the other for mode 5. In this way, the link voltages in modes 3 and 5 are in the ascending order, and therefore, the link voltage will reach these phase-pair voltages in the proper order as it is going up.

Mode 3 (link discharges to output): Two proper load-side switches are turned on to discharge the link inductance to the chosen phase pair for mode 3, discussed before. This mode runs until the average current of one of the connected output phases meets its reference value. After that, this mode ends, and the switches are turned off.

Note that the link voltage is equal to the reflected voltage of the selected phase pair at the beginning of mode 3. As a result, the turn-on of the mode-3 switches occurs at zero voltage. The zero voltage switching happens at the turn-on of the other converter's switches in the same way.

Mode 4 (link resonates partially): The link inductance and capacitance are allowed to resonate again until the link voltage becomes equal to the reflected voltage of the mode-5 phase pair.

Mode 5 (link discharges to output again): The link inductance is discharged to the selected mode-5 phase pair by turning on two appropriate load-side switches. Once the link current reaches a small value, which will be discussed later, this mode ends and the switches are turned off. Considering the input-output power balance, the average currents of both connected phases meet their reference values at the end of this mode.

Mode 6 (link resonates partially): The link reactive components start to resonate again. This partial resonance is maintained until the link voltage is equal to the input voltage in the down-going direction, which then permits the converter to go to mode 1 with zero voltage switching. In order to make this process happen properly, a small amount of current should be left in the link inductance at the end of mode 5 so that the link voltage rises up to a certain amount higher than the input voltage. Therefore, the link current at the end of mode 5 should be as follows:

$$i_L(t_5) = -\sqrt{\frac{C_1+n^2C_2}{L_M}\left({V_{LP+}}^2 - {v_L}^2(t_5)\right)} \tag{4.33}$$

where t_5 is time at the end of mode 5, and V_{LP+} is the pre-determined link peak voltage. V_{LP+} can be selected %10 to %15 higher than the input voltage. It should be noted that in the step-up operation of the converter, the mode-5 voltage is higher than the input voltage, and

consequently, the link voltage can softly decreases during mode 6 to reach the input voltage. As a result, $i_L(t_5)$ can be selected as zero in the boost operation.

As mentioned before, the reverse power flow from the output to the input is possible by using the topology of Fig. 4.18(b). The operation of the forward power transfer of this topology is similar to Fig. 4.18(a), as discussed above. In this case, switches S_1 and S_4 turn on together to charge the link in mode 1. In the reverse power direction, the HFAC-link is connected to the output phase pairs with the lowest and second-lowest instantaneous voltages in two modes. As a result, the link inductance is charged in the negative direction. Then, the link inductance is allowed to resonate in order to change its current direction. Finally, the link inductance is discharged to the input by turning on switches S_2 and S_3.

4.3.4. Converter Analysis and Optimal Design

As the arrangement of the line and phase voltages of a three phase system changes every π/6 rad, the first π/6 rad will be considered for the analysis of the introduced isolated converter. By assuming a unity load power factor, phase pair *ab* has the second-highest current difference in this interval, and according to the converter operation, it is selected for mode 3. Thus, the link average voltage in mode 3 is given by,

$$V_{3,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} \frac{v_{ab}}{n}\, d(\omega t) = \frac{3\sqrt{2}(\sqrt{3}-1)}{n\pi} V_{Lo} \tag{4.34}$$

where V_{Lo} is the output line-to-line rms voltage. The absolute value of the phase-*a* current is lower than the absolute value of the phase-*b* current in the assumed interval. Therefore, the link average current in mode 3 can be given as follows:

$$I_{3,ave} = -\frac{6}{\pi}\int_0^{\frac{\pi}{6}} n i_a d(\omega t) = -\frac{n3\sqrt{2}(2-\sqrt{3})}{\pi} I_{Po} \tag{4.35}$$

where I_{Po} is the output phase rms current. Similarly, phase pair *cb* has the highest current difference in that interval and is selected for discharge mode 5. Hence, the link average voltage in mode 5 is given by,

$$V_{5,ave} = \frac{6}{\pi}\int_0^{\frac{\pi}{6}} \frac{v_{cb}}{n} d(\omega t) = \frac{3\sqrt{2}}{n\pi} V_{Lo} \tag{4.36}$$

Subsequently, the link average current in mode 5 can be obtained from the following:

$$I_{5,ave} = -\frac{6}{\pi}\int_0^{\frac{\pi}{6}} n i_c d(\omega t) = -\frac{n3\sqrt{2}(\sqrt{3}-1)}{\pi} I_{Po} \tag{4.37}$$

The link voltage peaks to V_{LP+} in mode 6 and then equals V_{in} at the end of mode 6; so, the link current at the end of mode 6 can be given by,

$$I_6 = \sqrt{\frac{C_1+n^2C_2}{L_M}\left({V_{LP+}}^2 - {V_{in}}^2\right)} \tag{4.38}$$

By considering that the input reference current is equal to the average link current in mode 1, the mode-1 duration, T_1, and the link current at the end of mode 1, I_1, can be obtained respectively from the following:

$$T_1 = -\frac{L_M I_6}{V_{in}} + \sqrt{\left(\frac{L_M I_6}{V_{in}}\right)^2 + \frac{2L_M T I_{i,ref}}{V_{in}}} \tag{4.39}$$

$$I_1 = \frac{V_{in}T_1 + L_M I_6}{L_M} \tag{4.40}$$

where T is the average period of the link cycle. A similar analysis gives the average length of mode 3 and 5, T_3 and T_5, as follows:

$$T_3 = \frac{L_M I_3}{V_{3,ave}} + \sqrt{\left(\frac{L_M I_3}{V_{3,ave}}\right)^2 + \frac{2L_M T I_{3,ave}}{V_{3,ave}}} \tag{4.41}$$

$$T_5 = \frac{L_M I_5}{V_{5,ave}} + \sqrt{\left(\frac{L_M I_5}{V_{5,ave}}\right)^2 + \frac{2L_M T I_{5,ave}}{V_{5,ave}}} \tag{4.42}$$

where I_3 and I_5 are the link current at the end of mode 3 and 5 respectively and can be calculated by,

$$I_3 = \frac{-V_{5,ave}T_5 + L_M I_5}{L_M} \tag{4.43}$$

$$I_5 = -\sqrt{\frac{C_1 + n^2 C_2}{L_M}\left({V_{LP+}}^2 - {V_{5,ave}}^2\right)} \tag{4.44}$$

Equation (4.43) is derived by neglecting the link current change in the short mode 4. The average time-lengths of mode 2 and mode 6 can be obtained as follows:

$$T_2 = \sqrt{L_M(C_1 + n^2 C_2)}\left[\pi + \sin^{-1}\left(\frac{V_{in}}{-V_{LP-}}\right) + \sin^{-1}\left(\frac{V_{3,ave}}{-V_{LP-}}\right)\right] \tag{4.45}$$

$$T_6 = \sqrt{L_M(C_1 + n^2 C_2)}\left[\pi - \sin^{-1}\left(\frac{V_{in}}{V_{LP+}}\right) - \sin^{-1}\left(\frac{V_{5,ave}}{V_{LP+}}\right)\right] \tag{4.46}$$

As mentioned before, V_{LP+} is a pre-determined value, and V_{LP-} can be calculated by substituting (4.40) in (4.31). The duration of the short mode 4 can be found in a similar way. Finally, the sum of the time intervals of all the operating modes is equal to the average period of the link cycle as follows:

$$T_1 + T_2 + T_3 + T_4 + T_5 + T_6 = T \tag{4.47}$$

The resulting implicit equation can be solved to find T and the other main parameters of the converter. Fig. 4.21 shows the average link frequency, link negative peak voltage, and link peak current versus the total link capacitance, $C_t = C_1 + n^2 C_2$, for various values of the link inductance. The reduction of the total link capacitance mainly decreases the mode-2 duration. As a result, the link voltage should peak at the lower negative value in this mode to have zero average voltage in accordance with the inductor volt-second balance principle. On the other hand, the increment of the total link capacitance increases the duration of mode 2, in which there is no power transfer. Consequently, the link current should peak at a higher value at the end of mode 1 in order to meet the input average reference current. In addition, the link

frequency modifies due to the change in the link capacitance value and mode-2 duration. As Fig. 4.21 shows, the increase of the link inductance decreases the link frequency, link peak current, and link negative peak voltage, which means that the increase of the link inductance reduces the conduction power losses of the switches but increases their voltage stresses. As mentioned before, the link capacitance value has the opposite effect in these parameters. Therefore, the optimal value of the link inductance and capacitance can be selected from this figure to reach the desirable voltage and current ratings of the switches and the proper link frequency.

The link peak current specifies the conduction loss of the switches and the inductor power loss; therefore, lowering the link peak current yields smaller power losses on the switches and inductor. On the other hand, the link negative peak voltage determines the peak forward voltage of the input-side switches and peak reverse voltage of the load-side switches as will be formulated later. In order to decrease these switch voltage stresses, the magnitude of the link negative peak voltage should be reduced. As Fig. 4.21 demonstrates, it is impossible to drop the link peak current and link negative peak voltage magnitude together. Decreasing C_t or increasing L_M results in a smaller link peak current but a higher link negative peak voltage magnitude while increasing C_t or decreasing L_M has the reverse effect. Therefore, a trade-off should be made between the power losses of the switches and inductor on one side and the voltage stress on the switches on the other side. Hence, the converter's efficiency depends on the selected type of power switches (individual RB-switch or a RC-switch in series with a diode) and their voltage rating. Employing individual RB-switches with high voltage rating can result in high conversion efficiency.

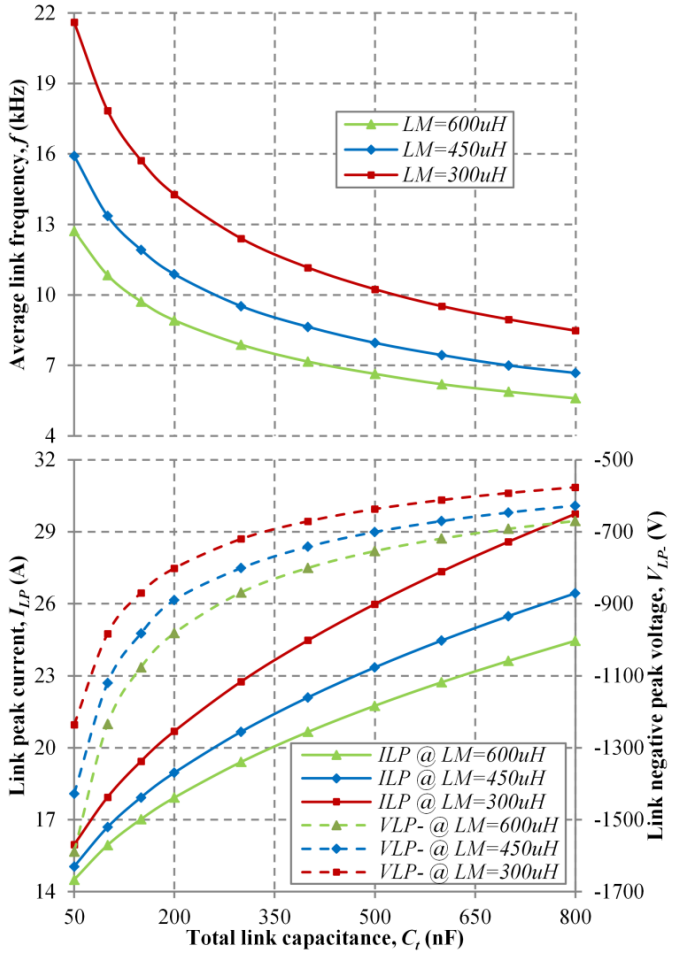

Fig. 4.21. Average link frequency, link negative peak voltage, and link peak current versus total link capacitance for various values of the link inductance, V_{in}=300V, V_{Lo}=208V, n=1, P_{out}=750W.

The variation of the link frequency, link negative peak voltage, and link peak current by changing the output active power and input voltage are shown in Fig. 4.22. As the figure depicts, the absolute value of the link negative peak voltage and the link peak current depend on the output power, and as the output power reduces, they both decrease almost linearly. Alternatively, the link frequency increases slowly and almost linearly with the decreasing of the output power. Note that these three major converter parameters are only dependent on the active power amount of the output power irrespective of the output reactive or apparent

power. The link frequency, link negative peak voltage, and link peak current of the proposed isolated converter at a very small amount of the output power can be given by,

$$f|_{P_{out}\approx 0} = \frac{1}{2\pi\sqrt{L_M(C_1+n^2C_2)}} \tag{4.48}$$

$$V_{LP-}|_{P_{out}\approx 0} = -V_{LP+} \tag{4.49}$$

$$I_{LP}|_{P_{out}\approx 0} = \sqrt{\frac{C}{L}}V_{LP+} \tag{4.50}$$

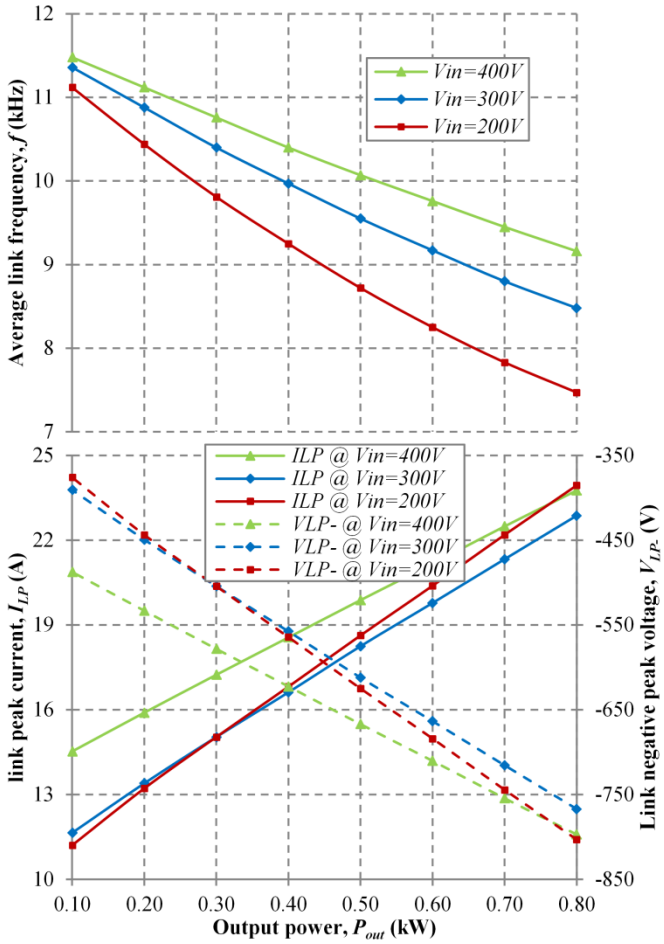

Fig. 4.22. Average link frequency, link negative peak voltage, and link peak current versus output power for various values of the input voltage, V_{Lo}=208V, n=1, L_M=450µH, and C_t=400nF.

Since the highest and second-highest instantaneous output voltages change slightly over the course of the ac cycle, the durations of the discharging modes (3 and 5) also change slightly over the ac cycle. As a result, the link frequency also varies slightly in the course of the ac cycle. It can be shown that the range of variation of the link frequency is less than 3% at the nominal conditions. In addition, the link frequency variation decreases as the output power reduces and vanishes at very light output power.

The peak forward voltage and peak reverse voltage of the input-side switches of the isolated bidirectional topology can be expressed as follows:

$$PFV_I = \frac{1}{2}V_{in} - \frac{1}{2}V_{LP-} \tag{4.51}$$

$$PRV_I = \frac{1}{2}V_{in} + \frac{1}{2}V_{LP+} \tag{4.52}$$

and the peak forward voltage and peak reverse voltage of the load-side switches of that converter can be given by,

$$PFV_O = \sqrt{\frac{2}{3}}V_{Lo} + \frac{n}{2}V_{LP+} \tag{4.53}$$

$$PRV_O = \sqrt{\frac{2}{3}}V_{Lo} - \frac{n}{2}V_{LP-} \tag{4.54}$$

4.3.5. Simulation Results

Computer simulation was used to test the introduced parallel resonant topology of Fig. 4.18(c). The transformer model parameters of Table 4.2 were employed in the simulation with the magnetizing inductance of 450μF and turns ratio of 1. The link capacitors, C_1 and C_2, were both chosen as 200nF to have the total capacitance of 400nF. Fig. 4.23(a) shows the simulation results of the link voltage and current with the input voltage of 200V, and Fig. 4.23(b) depicts the results with the input voltage of 400V. The load voltage

and power at these two tests were 208V/60Hz and 1kVA at 0.75PF lagging. The small oscillations in the link voltage at the beginning of the operating modes are due to the stored energy in the transformer leakage inductances, which are damped by the link capacitors and dissipated in the transformer winding resistances. The simulation showed the average link frequency, link peak current, and link negative peak voltage as 7.56kHz, 23.1A, and −773.7V for the step-up test and 9.24kHz, 23.2A, −778.2V for the step-down test. These results are compatible with the outcomes of the theoretical analysis as shown in Fig. 4.22 with the consideration that the output active power in both tests was 750W.

Table 4.2. The parameters of the designed HF transformer.

Parameter	**Value**
Core shape	PM 74/59
Core material	N27 from EPCOS
Airgap length	3.8mm
Output-input turns ratio	1
Magnetizing inductance	450µH
Primary leakage inductance	1.8µH
Secondary leakage inductance	1.8µH
Primary dc winding resistance	54mΩ
Secondary dc winding resistance	54mΩ
Primary-secondary stray capacitance	780pF

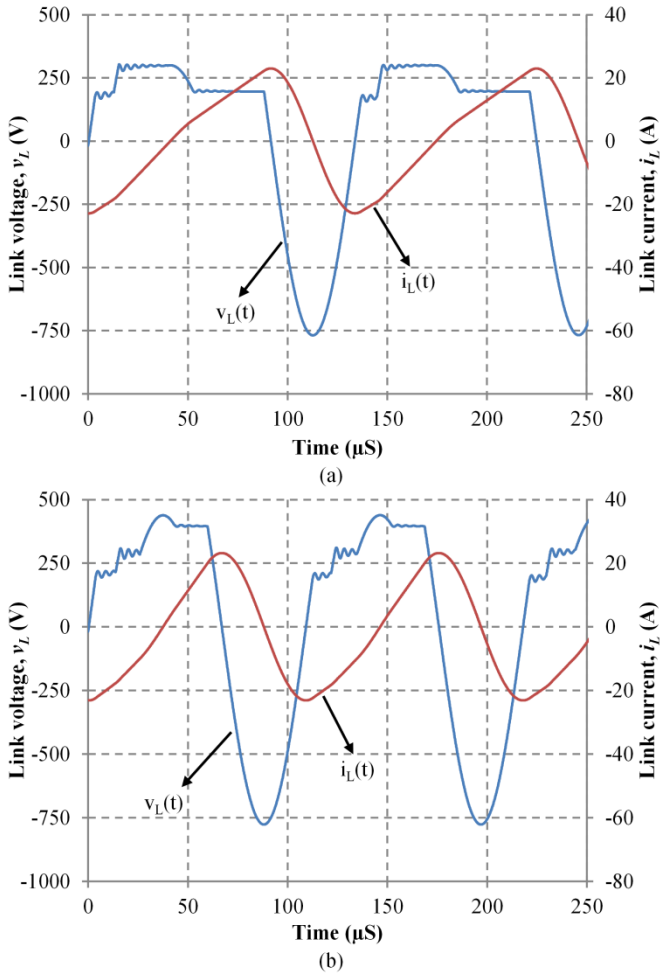

Fig. 4.23. Simulation results of the proposed converter at 1kV including link voltage and link current. (a) step-up case, and (b) the step-down case.

Figs. 4.24(a), 4.24(b), and 4.24(c) show the dynamic response of the proposed inverter by a step change in the load, output reference current, and output frequency respectively. In all cases, the converter was initially working at the nominal conditions (Input: 300V, output: 208V/60Hz, and load: 1kVA at 0.75PF lagging). A step change was performed in the three cases at t=15ms, and the converter was returned back to its nominal conditions at t=45ms. As the figures show, the proposed HFAC-link inverter has a fast dynamic response as a result of small passive components in the link. Due to the inductive

behavior of the load and the existence of the output and input filters, it takes a short interval until the converter reaches the new steady state condition.

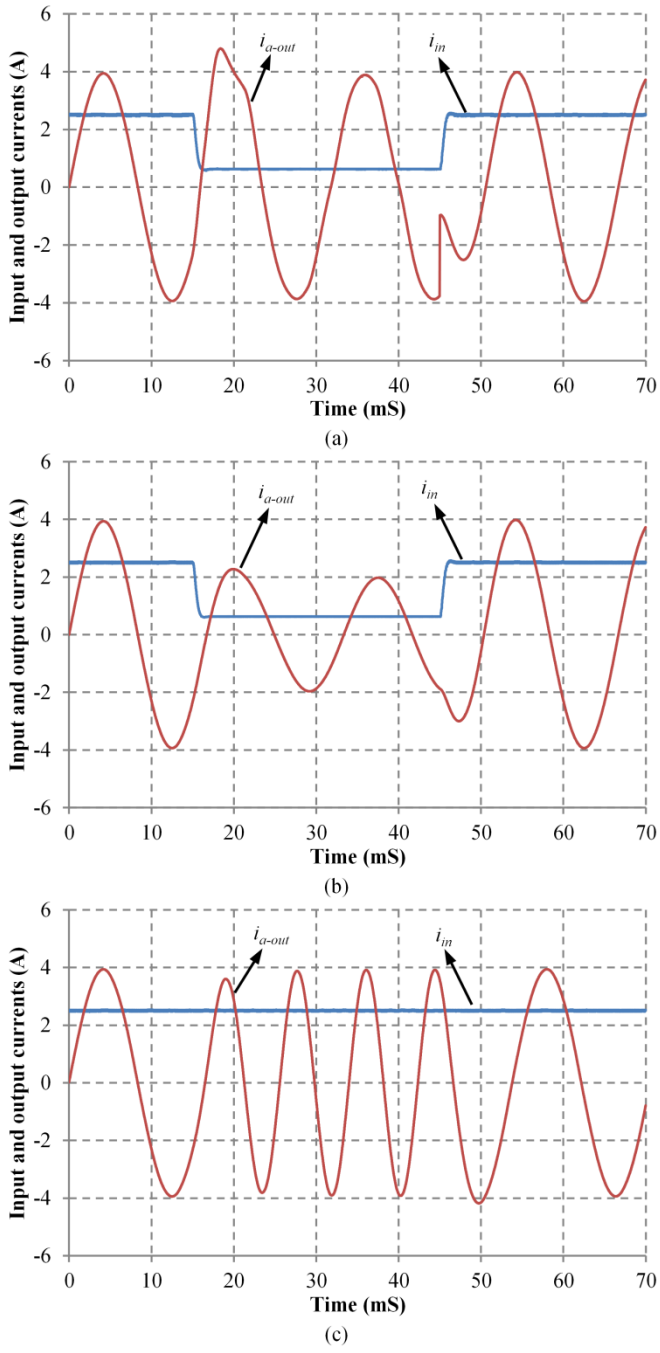

Fig. 4.24. Dynamic response of the proposed inverter. (a) load change to 25% of the nominal value, (b) output reference current change to 50% of the nominal value, and (c) output frequency change to 200% of the nominal value.

4.3.6. Experimental Results

A 750Watts/1000VA prototype of the proposed isolated bidirectional topology was developed to verify its performance. The sample time of the digital control was 3μs, which included the ADC conversion time and the required processing time. Both link capacitors were selected as 200nF, similar to the previous section. The model parameters of the designed HF transformer for this prototype are shown in Table 4.2. The designed converter prototype was run in the same step-up and step-down conditions as the simulation section with the load voltage and power of 208V/60Hz and 1kVA at 0.75PF lagging. Fig. 4.25(a) shows the transformer primary voltage (v_p) as well as the input and output currents of the link (i_p and i_s) in the step-up case with the input voltage of 200V. Fig. 4.25(b) depicts these parameters in the step-down case with the input voltage of 400V. As the figures show, these experimental results are very close to the results of the analysis and simulation sections. The small differences are mainly due to the non-linearity and power loss of the components. Fig. 4.26 displays the input current and output current of phase *a* in the step-up case. The measured efficiencies at full power were 93.5% and 95.4% for the step-up and step-down cases respectively. The voltage and current waveforms of input-side switches as well as the load-side switches at different instants are shown in Fig. 4.27. The zero-voltage switching at turn-on and turn-off of switches can be clearly seen in the figure.

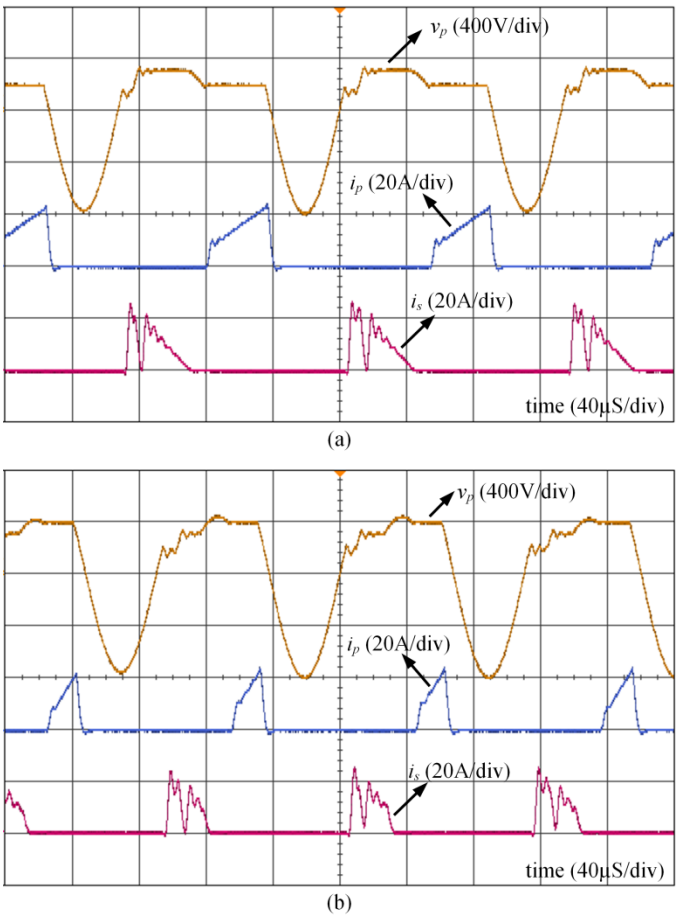

Fig. 4.25. Experimental results of the proposed converter at 1kVA. (a) step-up case. (b) step-down case.

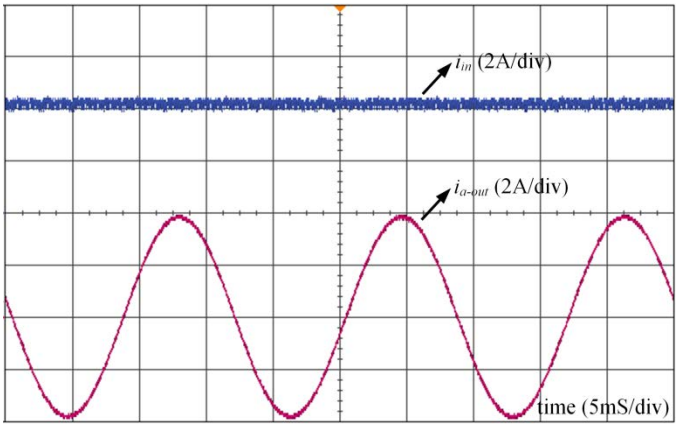

Fig. 4.26. Experimental results of the filtered input and output currents in the step-up case at 1kV.

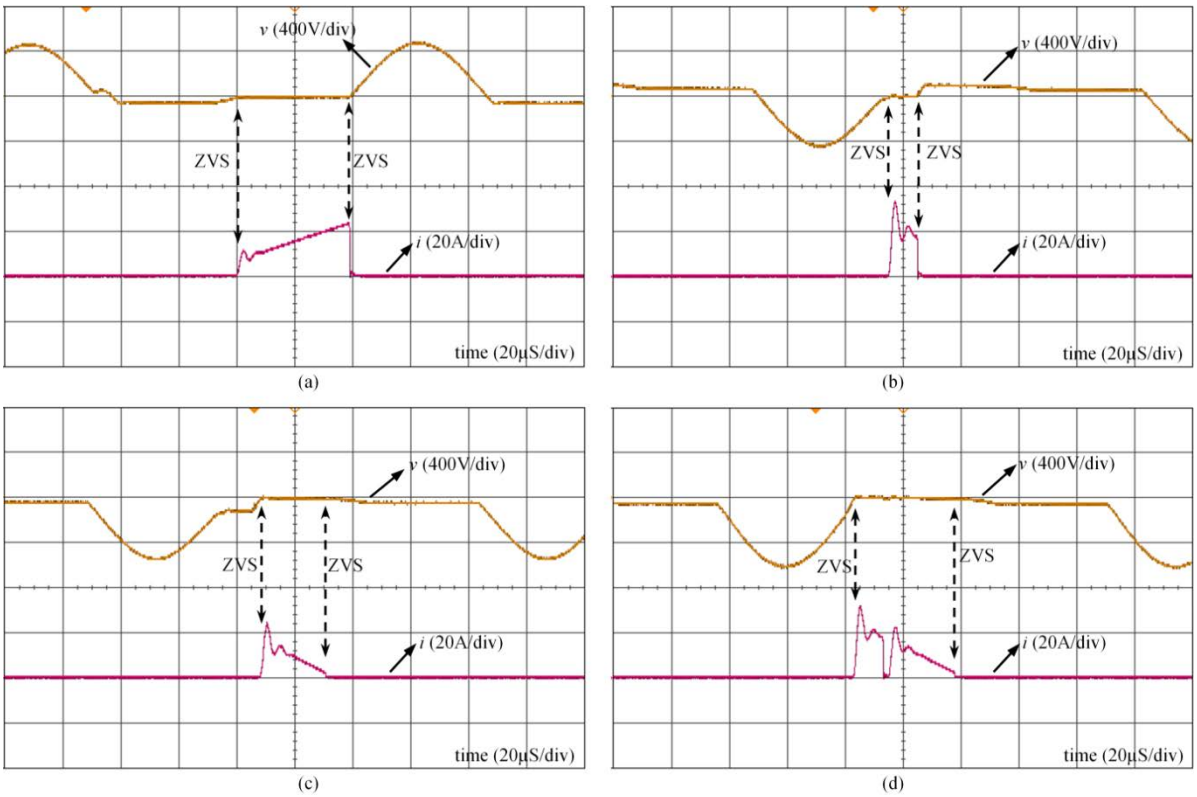

Fig. 4.27. Experimental results of the proposed converter in the step-up case at 1kVA. (a) voltage and current waveforms of input-side switches. (b), (c), and (d) The different possible voltage and current waveforms for the load-side switches.

4.4. A ZVS Single-Inductor Multi-Input Multi-Output DC-DC Converter with the Step Up/Down Capability

4.4.1. Introduction

The electric power generated by renewable energy resources, such as photovoltaic (PV) and wind power, depends on the weather conditions and is not constantly available. In order to have a reliable and flexible clean power system, a combination of the renewable sources together or with the fuel cell, commercial ac line, battery, or supercapacitor should be used. In such a hybrid power-conversion system, a multiple-input power converter should be employed to combine several input power sources with different electrical characteristics

and to generate a regulated output voltage [118], [119]. In recent literature, various circuit topologies of multi-input converters have been proposed for the applications of the hybrid PV–wind power system [120]–[122], PV–utility system [123]–[127], hybrid-electric vehicle (HEV) [128]–[131], and others [132]–[135]. Furthermore, several applications have a number of simultaneous loads with different power and voltage levels, and therefore, multi-output converter topologies are vital for such systems [136]–[138]. The general form of a multi-input multi-output dc-dc converter consists of several input sources and several output loads, as shown in Fig. 4.28. In general, all of the input sources can deliver power to the loads either individually or simultaneously through the converter [139], [140]. The main dc-dc converter can be isolated or non-isolated according to the application.

An innovative multi-input multi-output (MIMO) partial-resonant dc-dc converter with a high-frequency (HF) link is introduced in this study. The proposed MIMO dc-dc converter can handle an arbitrary number of input sources and output loads. These inputs and outputs can be at different voltage values and power levels. The proposed topology only needs to have a reverse-blocking switch for each input or output of the converter. An ac inductor and a small ac capacitor are the main components of the power converter and form the so-called HF link. The link inductor is responsible for transferring power from the input to the outputs while the link capacitor's role is to create zero-voltage turn-on and turn-off conditions for all the power devices. The zero-voltage switching (ZVS) always happens in this converter irrespective of the input and output voltage values or load power levels. The link inductor is the only inductor of the converter, which is small and efficient by having an ac current. The converter can be easily isolated by using an air-gapped HF transformer. The proposed power

converters can perform step-up and step-down operations conveniently in both isolated and non-isolated topologies.

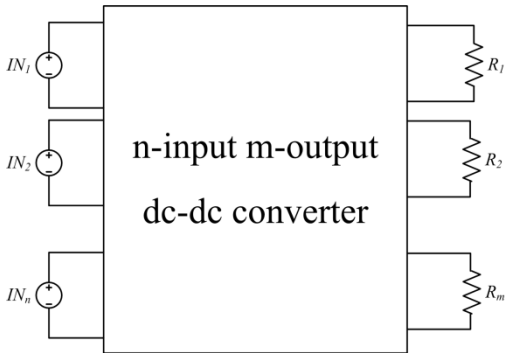

Fig. 4.28. The general form of a multi-input multi-output dc-dc converter.

4.4.2. The Proposed MIMO DC-DC Converter

Fig. 4.29(a) shows the proposed single-inductor partial-resonant dc-dc converter in the non-isolated form with an arbitrary number of inputs and outputs. Each input and output of the converter can have its own suitable voltage level and reference current value; however, input-output power balance should be satisfied, i.e. the total input power should be equal to the total output power plus the converter's power loss. The inductor L and the capacitor C form the HF link of the proposed topology. The link capacitor C is an ac capacitor with a considerably small capacitance value, so there is no bulky short-life electrolytic capacitor in the link. The link inductor, L, is the main element for transferring the power from the inputs to outputs, and the link capacitor, C, causes partial resonances to achieve the soft-switching operation. As the figure shows, each input and output is associated with one reverse-blocking switch, which can be realized by a customary IGBT or MOSFET in series with a diode.

Individual reverse-blocking switches are now available in the market with the advantage of lower total on-state voltage.

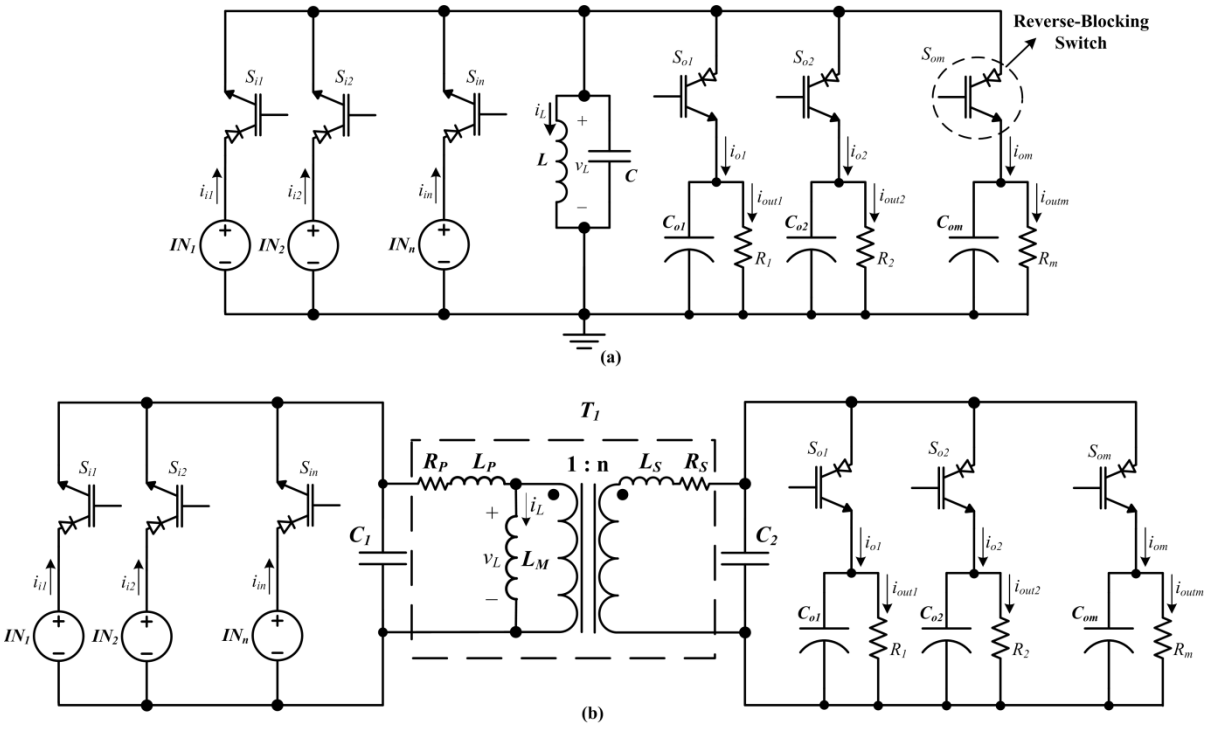

Fig. 4.29. The proposed partial-resonant multi-input multi-output dc-dc converter. (a) non-isolated topology, and (b) isolated topology.

In order to transfer power in both forward and reverse directions, the reverse blocking switches of the converter should be replaced by bidirectional switches. The bidirectional switches can be made by using two back-to-back switches in series or two reverse-blocking switches in anti-parallel. Galvanic isolation can be provided by utilizing a HF transformer in the converter's link, as shown in Fig. 4.29(b). Instead of one link capacitor, two smaller link capacitors C_1 and C_2 are placed on both sides of the transformer T_1 [7]. These capacitors provide paths for the currents of the primary and secondary leakage inductances when the

input and output switches are turned off, and subsequently, they avoid voltage spikes. In order to reach an appropriate link inductance value in this topology, the transformer may have air gap.

4.4.3. The Principle of Operation

The operation of the proposed soft-switching MIMO dc-dc converter consists of several modes in each link cycle, depending on the number of inputs and outputs. In short the converter's link inductor firstly charges through the inputs one-by-one, and then it discharges to the outputs in a sequential manner. There are partial resonance modes between these charging and discharging intervals to achieve zero-voltage switching at both turn-on and turn-off for the converter's switches. Fig. 4.30 shows the typical link cycle of the non-isolated topology in the two-input two-output case, which will be explained in detail in the following. The described modes of operation can be extended to the n-input m-output conveniently.

Mode 1: The switch associated with the highest-voltage input is turned on, and as a result, the link inductor starts to charge in the positive direction. This mode runs until the average current of the connected input meets its reference value. Subsequently, the switch is turned off. It is assumed that IN_1 has higher voltage than IN_2 in Fig. 4.30; therefore, it is connected to the link in mode 1 by turning on switch S_{i1}.

Note that the link capacitor causes the link voltage, $v_L(t)$, to drop slowly while the mode-1 switch is turned off, and subsequently, the switch voltage increases slowly. As a result, the mode-1 switch is turned off at almost zero voltage. This soft switching operation happens at the turn-off of all the converter's switches in all operating modes.

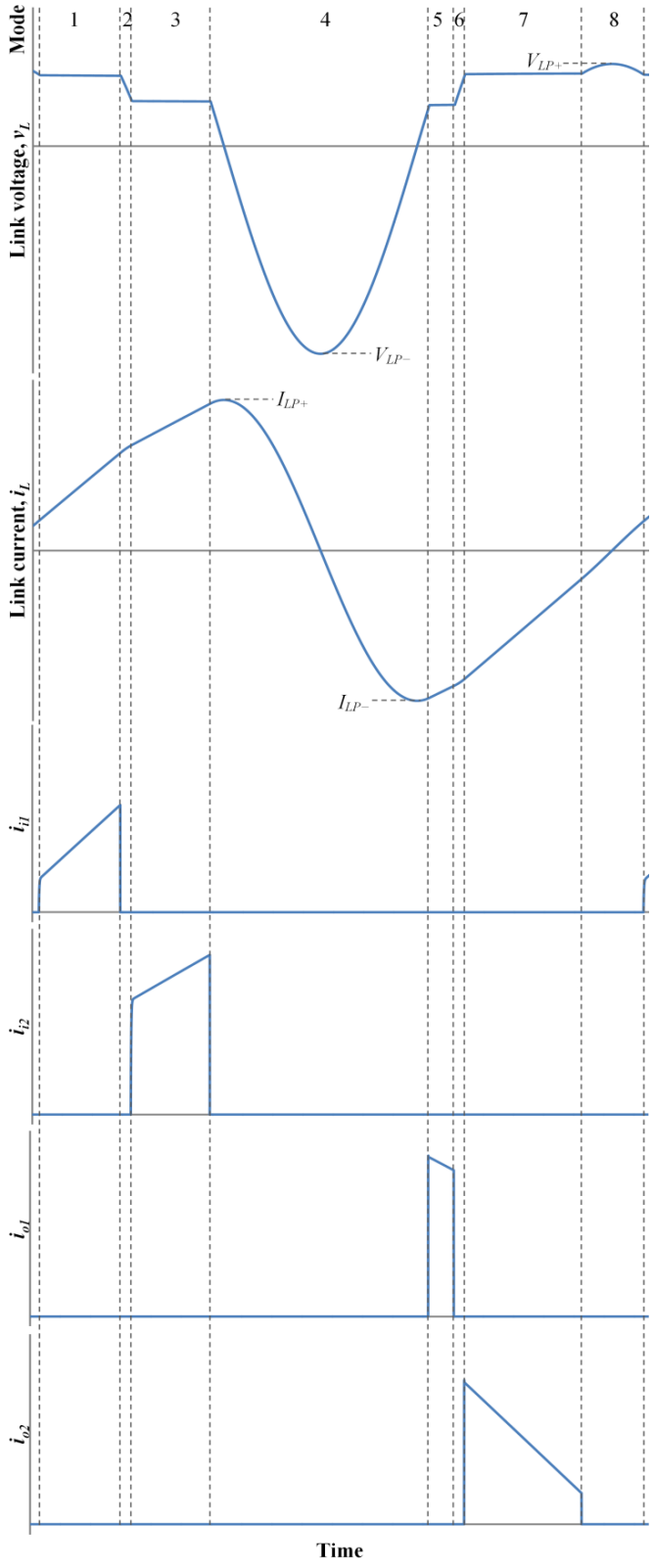

Fig. 4.30. Typical waveforms of the proposed converter in the 2-input 2-output case. (a) link voltage, (b) link current, (c-d) input currents, (e-f) output currents.

Mode 2: The link inductor resonates with its parallel capacitor until the link voltage is equal to the second highest input voltage.

Mode 3: The switch related to the input with the second-highest voltage is turned on to continue the charge of the link inductor in the positive direction. This switch is turned off when the average current of the connected input meets its reference value.

Note again that the link voltage is equal to the voltage of the selected input at the beginning of mode 3. As a result, the turn-on of the switch occurs at zero voltage. The zero voltage turn-on happens for all the converter's switches in a similar way.

Mode 4: The link inductor resonates considerably with the link capacitor again. This resonance is permitted to run until the link voltage is equal to the lowest output voltage of the converter in the rising direction. During this mode, the link current, $i_L(t)$, reaches its positive and negative peak values, I_{LP+} and I_{LP-}, as follows:

$$I_{LP+} = -I_{LP-} = \sqrt{{I_3}^2 + \frac{C}{L}{V_3}^2} \tag{4.55}$$

where "V_x" is defined as the link voltage in mode *"x"* and *"*I_x*"* is link current value at the end of mode *"x"* of the operation. The link voltage, $v_L(t)$, also reaches its negative peak value, V_{LP-}, in this mode and can be given by,

$$V_{LP-} = -\sqrt{{V_3}^2 + \frac{L}{C}{I_3}^2} \tag{4.56}$$

Mode 5: The switch connected to the lowest-voltage output is turned on to discharge the link inductor to that output. The switch remains on until the average current of the connected output reaches its reference value. After that, the switch is turned off. It is assumed that R_1 has a lower voltage than R_2 in Fig. 4.30; therefore, R_1 is connected to the link in mode 5 by turning on switch S_{o1}.

Mode 6: The link inductor and capacitor of the converter resonate together until the link voltage is equal to the second-lowest output voltage.

Mode 7: The HF link is connected to the second-lowest output voltage by turning on the proper switch. As a result, the link inductor discharges to that output. This mode runs until the link current reaches a small value of I_7, which will be defined later. After that, the switches are turned off. Considering the input-output power balance, the average current of the connected output meets its reference value at the end of this mode.

Mode 8: The link inductor and capacitor start to resonate again. This partial resonance is maintained until the link voltage is equal to the highest input voltage, which then permits the converter to go to mode 1 with zero voltage switching. In order for this procedure to happen appropriately, the link voltage should rise up to a certain amount above the input highest voltage as shown in Fig. 4.30. Therefore, the link current at the end of mode 7 should be as the following:

$$I_7 = -\sqrt{\frac{C}{L}\left({V_{LP+}}^2 - {V_7}^2\right)} \tag{4.57}$$

where V_{LP+} is the peak link voltage in mode 8 and can be selected 10% to 15% higher than the highest input voltage. It should be noted that if V_7 (the highest output voltage) is higher than V_1 (the highest input voltage), there is no need to leave any current in the link inductor at the end of mode 7 (I_7 can be selected as 0). In this case, the link voltage constantly drops during mode 8 to reach the highest input voltage and mode 1 of the operation.

In the digital control implementation of the proposed partial-resonant multi-input multi-output converter, there might be a delay in the turning on of the switches at the exact times stated above due to the discrete sampling and required processing time. In order to avoid this delay, the converter's switches can be turned on ahead of time while they are in the

negative off-state voltages, and consequently, they start conducting when they become forward biased with zero voltage switching. For instance, switch S_{i1} can be turned on when the link voltage reaches its positive peak value, V_{LP+}, and switch S_{i2} can be turned on as soon as switch S_{i1} is turned off. Similarly, switch S_{o1} is turned on when the link voltage reaches its negative peak value, V_{LP-}, and so on. As Fig. 4.30 shows, when the link voltage reaches its positive and negative peak value, the link current passes through zero in the positive and negative directions, respectively. Therefore, the zero crossing of the link current can be used as a sign to understand when the link peak voltages occur.

The proposed topology can transfer power in the reverse direction as well as the forward direction by using bidirectional switches. In the reverse power flow direction, the link inductor is charged from the outputs, and after a resonant mode, it is discharged to the input by properly turning on the converter's input-side switches.

4.4.4. Experimental Results

In order to verify the operational principle, advantages, and performance of the proposed power converter, a two-input one-output prototype was developed. The sample time of the microcontroller was 1.5μS. The link inductor and capacitor of the converter were selected as 430μH and 400nF, respectively. The input voltages were selected as 100V and 150V, and the output resistance was 200Ω. Figs. 4.31 and 4.32 show the experimental results of the designed prototype for two different tests. In the first test, almost 75% of the output power was drawn from the first input by setting the reference currents of the 100V and 150V inputs as 1.5A and 0.33A, respectively. In the second run, the 150V input was delivering almost 75% of the output power by assigning the reference currents of the 100V and 150V

inputs as 0.5A and 1A, respectively. As it is seen from the Figs. 4.31 and 4.32, the duration of modes 1 and 3, in which the inputs are delivering power, are considerably different in these tests. The output voltage was almost 194V in both tests. The measured link frequency was 8.7 kHz for the first test and 9.2 kHz for the second one. The experimental results clearly show that the proposed power converter is completely capable of drawing any value of power from each input independently.

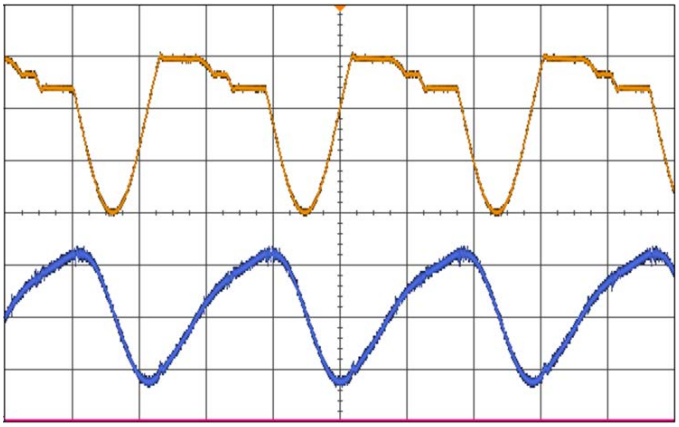

Fig. 4.31. Experimental results for V_{in1}=100V, V_{in2}=150V, $I_{i1,ref}$=1.5A, $I_{i2,ref}$=0.33A, and R_1=200Ω. Top: link voltage (200V/div), and bottom: link current (10A/div) versus time (40μS/div).

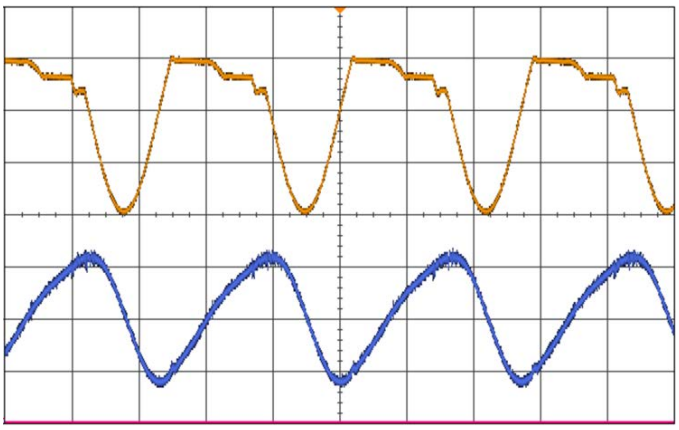

Fig. 4.32. Experimental results for V_{in1}=100V, V_{in2}=150V, $I_{i1,ref}$=0.5A, $I_{i2,ref}$=1A, and R_1=200Ω. Top: link voltage (200V/div), and bottom: link current (10A/div) versus time (40μS/div).

5. FAULT-TOLERANCE ABILITY OF THE PROPOSED HIGH-FREQUENCY AC-LINK CONVERTER

5.1. Introduction

The isolated soft-switched high-frequency ac-link converter was introduced in section 2, and two reduced-switch generations of the soft-switched high-frequency ac-link converters (known as type-I and-II reduced-switch topologies) were proposed in sections 3 and 4. This section studies the fault tolerance ability of the converter. It will be shown that in the case of one or more faulty switches in the original converter, the type-I and type-II reduced-switch operating algorithms may be employed in order to continue running the converter with degraded performance. In this way, a switch failure may not result in the converter shutdown, thus improving system availability.

5.2. The State-Plane Diagram of the Proposed Original, Type-I, and Type-II Soft-Switched HFAC-Link Topologies

A state-plane diagram (link current vs. link voltage) is a good tool to have a better view of the operation and performance of proposed topologies. Fig. 5.1 shows the state-plane diagram of the original soft-switched HFAC-link ac-ac converter introduced in section 2. As the figure shows, the link inductance charges and discharges twice in each link cycle, and there is a soft transition (resonant mode) between each charging and discharging modes. The diagram of the type-I reduced-switch HFAC-link converter is displayed in Fig. 5.2(a). According to section 3, this converter has only one charging and discharging sequence in each link cycle. It should be noted that all the switches of the type-I topology can be flipped

to transfer power in the negative direction as Fig. 5.2(b) shows. This topology will be referred to as the "type-I reduced-switch converter in the negative direction". Similarly, Fig. 5.3 depicts the state-plane diagram of the type-II topology as well as the type-II topology in the negative direction with all the switches flipped. Note that the long resonant mode is after the charging modes in type-II topology while it happens just after the discharging modes for the type-I converter.

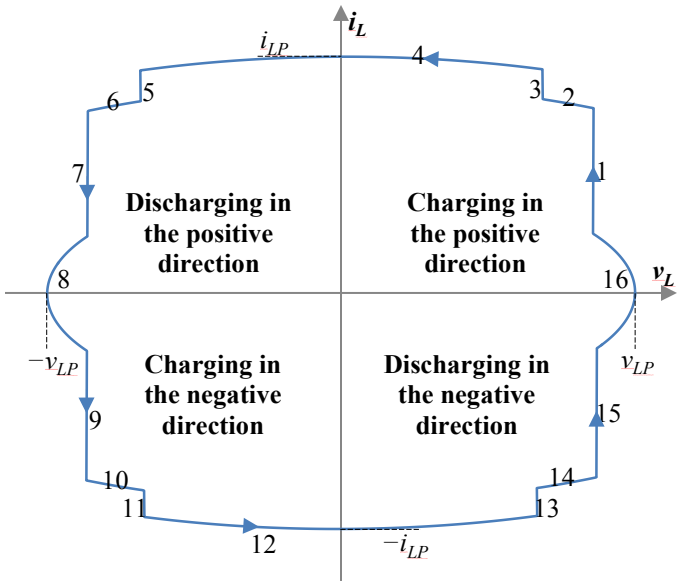

Fig. 5.1. The state-plane diagram of the original soft-switched HFAC-Link converter.

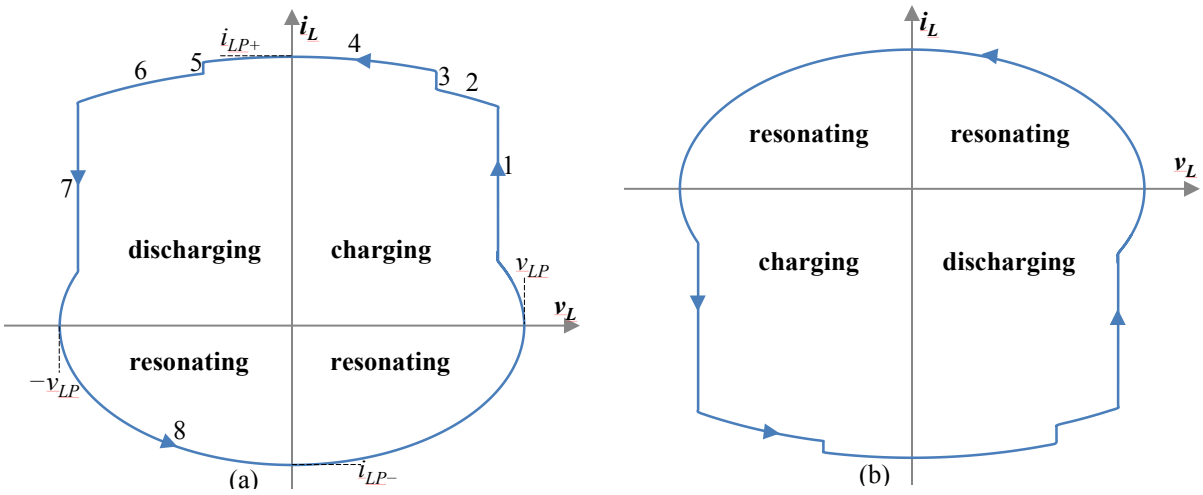

Fig. 5.2. The state-plane diagram of the reduced-switch HFAC-link converter. (a) type-I topology, and (b) type-I topology in the negative direction.

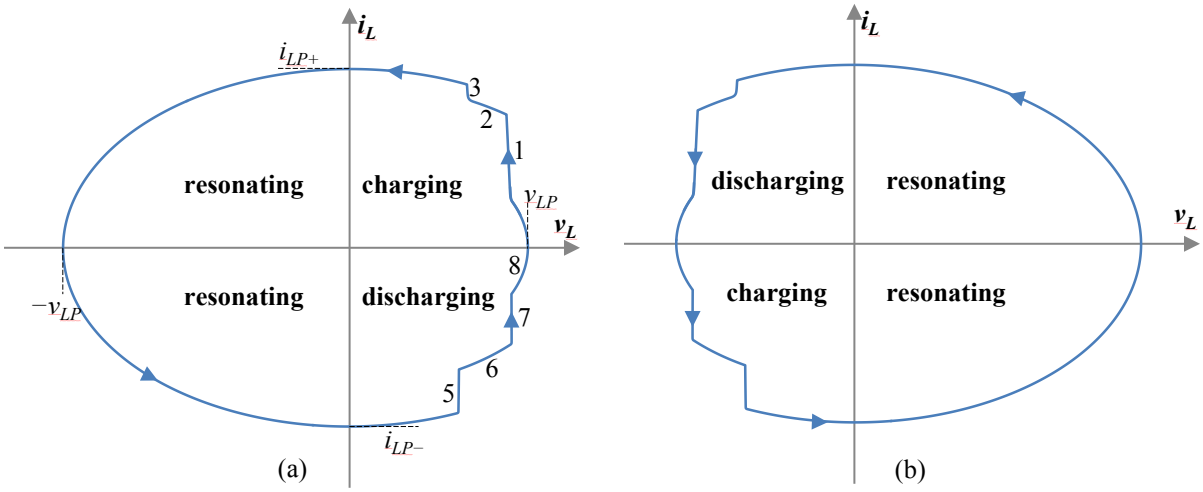

Fig. 5.3. The state-plane diagram of the reduced-switch HFAC-link converter. (a) type-II topology, and (b) type-II topology in the negative direction.

5.3. Categorizing the Switch Faults in the Partial-Resonant High-Frequency AC-Link Converter

The original soft-switched HFAC-link converter presented in section 2 in dc-ac form is shown in Figs. 5.4 and 5.5. In Fig. 5.4, the bidirectional switches of the converter are

realized by the conventional reverse-conducting (RC) switches, e.g. conventional IGBTs. As mentioned before, two RC switches in anti-series make a bidirectional switch. It is also possible to realize the bidirectional switches using the newly available reverse-blocking (RB) switches as shown in Fig. 5.5. Although the soft-switched HFAC-link converter in any form of the switch realization has the advantages of high conversion efficiency and the exclusion of the short-life electrolytic capacitors in the main link, it has a higher switch count compared to the conventional pulse-width-modulated (PWM) voltage-source converters. Therefore, the chance of a power switch fault is higher in this converter. In this section, the possible faults in the power switches of the introduced converter are considered, and alternative solutions are given to survive the load with one or several faulty switches. In order to do that, the possible switch faults of the HFAC-link converter are categorized as follows:

I. An input-side switch or load-side switch remains open.

II. An input-side switch remains closed.

III. A load-side switch remains closed.

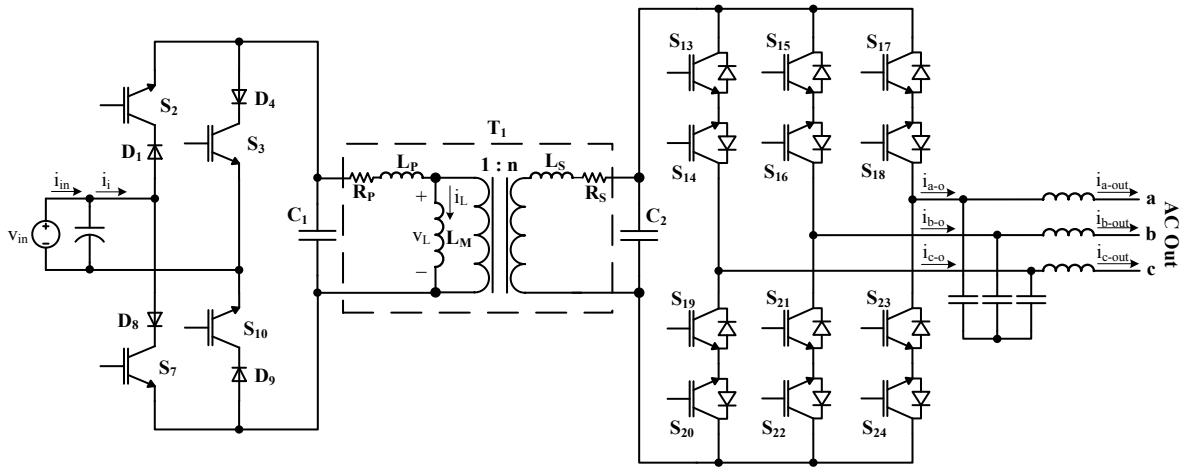

Fig. 5.4. The original soft-switched HFAC-link dc-ac converter, realized by the conventional reverse-conducting switches.

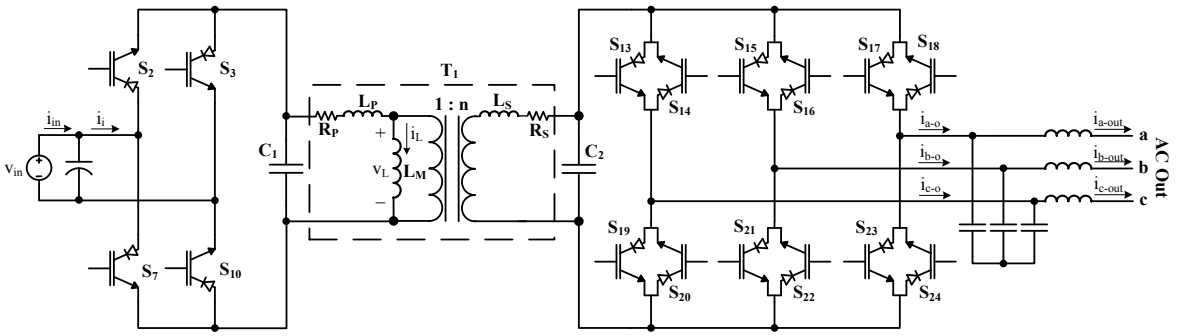

Fig. 5.5. The original soft-switched HFAC-link dc-ac converter, realized by the reverse-blocking switches.

Each of these cases is investigated separately in the following sections and possible solutions to run the converter during these faulty cases are investigated. Note that it is impossible to run the converter in all possible switch faults; for example, if all the switches of an input-side leg break to open-circuit, it is impossible to continue running the converter in any way since there is no path to charge the link from the input. However, if just one of the switches of an input-side leg breaks (either to open-circuit or short-circuit), it is possible to run the converter and survive the load. In order to do that, the faulty status of all the converter's power switches should be sent to the main controller of the converter. The controller monitors the status of the power switches and may modify the operating algorithm in case of a faulty condition to effectively run the converter as described in the following sections. The faulty status of the power switches can be revealed by having extra circuitry near each power switch to monitor its gate-emitter and collector-emitter voltages and returns error signals in case the power switch remains consistently open or closed. In the following analysis, the soft-switched HFAC-link converter with RC-switches is considered; the same concept can also be employed with the converter with the RB-switches.

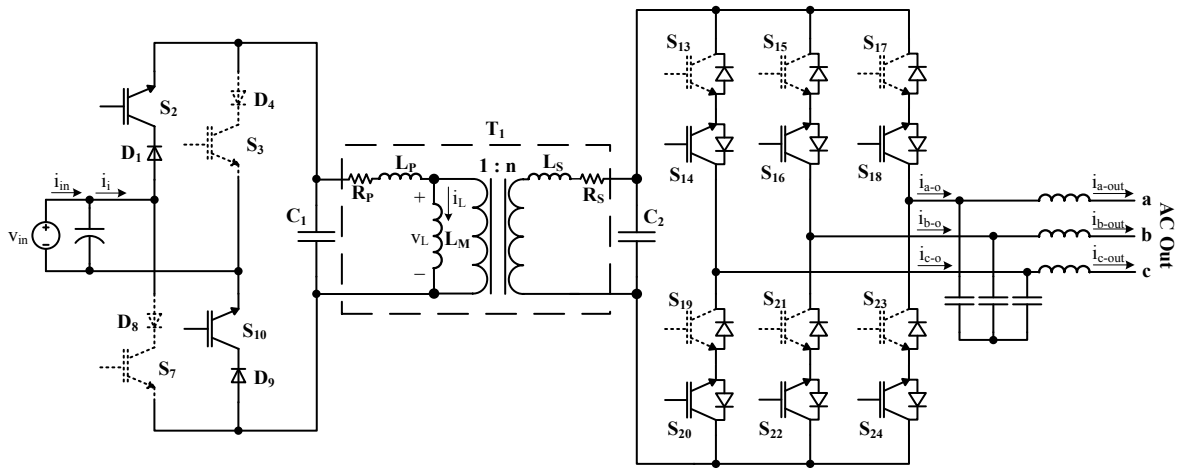

Fig. 5.6. Case I.A: An input-side switch or load-side switch remains open

5.4. Case I: An Input-Side Switch or Load-Side Switch Remains Open

This faulty case is sub-categorized into four possible cases according to the formation of the faults in the input-side and load-side switches. Fig. 5.6 shows the first possible case and is designated as case I.A. If any or several of the dashed-line switches and diodes (S_3, D_4, S_7, D_8, S_{13}, S_{15}, S_{17}, S_{19}, S_{21}, and S_{23}) break to open-circuit, the resulting converter is similar to the type-I reduced-switch topology discussed in section 3. Note that switches S_2 and S_{10} in Fig. 5.6 should be turned on and off together to behave as the single input-side switch. As a result, the faulty converter of Fig. 5.6 can work with the type-I reduced-switch algorithm, explained in section 3, to feed the load. Since the switch utilization of the type-I reduced-switch operating mode is low due to the long resonant mode 8, it yields higher link peak current than the original converter at the same power level. Therefore, the maximum power of the converter with the type-I reduced-switch algorithm is lower than the original algorithm and depends on the link inductor and capacitor values. Comparing the analysis results of the prototype converter with the original algorithm and the type-I operating algorithm reveals

that the prototype converter can provide about 750W output power with the type-I operating algorithm compared to 1kW power with the original algorithm.

The second possible faulty case is that the dashed-line devices in the converter shown in Fig. 5.6 are functioning properly, but any or several of the solid-line switches and diodes (D_1, S_2, D_9, S_{10}, S_{14}, S_{16}, S_{18}, S_{20}, S_{22}, and S_{24}) break to open-circuit. This case is considered as I.B and the resulting converter is similar to the type-I reduced-switch topology discussed in section 3 in the negative direction. In this scheme, the link inductance is charged through the input in the negative direction, and subsequently, it is discharged to the output. The performance and operating behavior of the converter with type-I reduced-switch algorithm in the negative direction is the same as the one in the positive direction, explained in section 3, and all the analysis results can be directly applied.

Faulty case I.C occurs when any or several of the dashed-line diodes and switches shown in Fig. 5.7 (S_3, D_4, S_7, D_8, S_{14}, S_{16}, S_{18}, S_{20}, S_{22}, and S_{24}) break to open-circuit. Note that this case is different from case I.A since the formation of faulty output-side switches is dissimilar. The converter with the faulty dashed-line switches shown in Fig. 5.7 is similar to the type-II reduced-switch resonant converter, explained in section 4. Note that switches S_2 and S_{10} in Fig. 5.7 should be turned on and off together in order to behave as the single input-side switch of type-II converter. Therefore, the faulty converter of Fig. 5.7 can work with the type-II reduced-switch algorithm, explained in section 4, to feed the load. Similar to the type-I converter, the switch utilization is lower than the original converter, and as a result, the power capacity of the converter running with type I or II is lower than the one running with the original operating algorithm. The type-II operating algorithm has also another problem: it yields higher voltage stress on the power switches, as explained in section 4. As a result, the

output power may be required to go even lower to limit the voltage stress on the power switches.

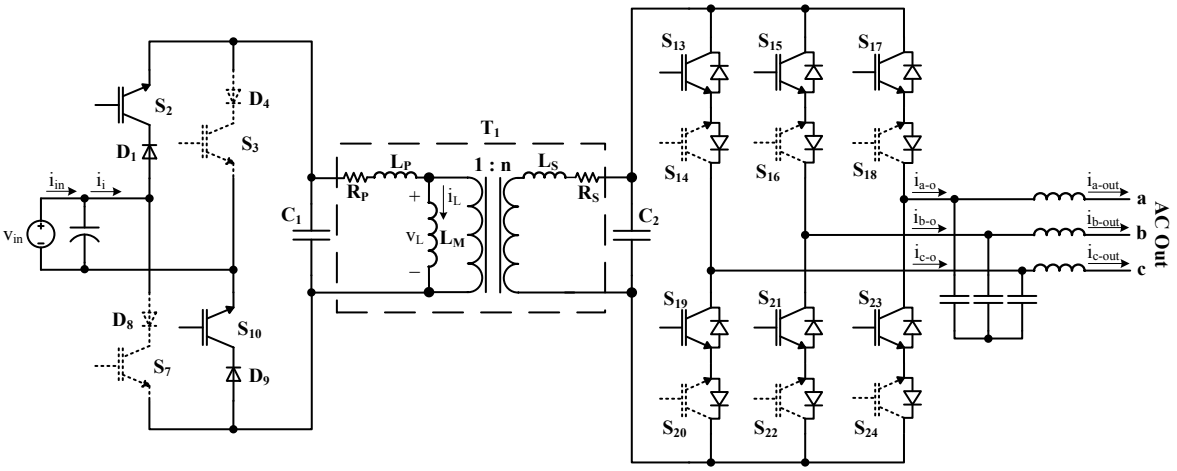

Fig. 5.7. Case I.C: An input-side switch or load-side switch remains open

The final possible scenario in case I is when all the dashed-line switches of the converter shown in Fig. 5.7 are working correctly, but one or several solid-line power switches (D_1, S_2, D_9, S_{10}, S_{13}, S_{15}, S_{17}, S_{19}, S_{21}, S_{23}) break to open-circuit. This case is considered as case I.D, and the resulting faulty converter can work in type-II reduced-switch algorithm in the negative direction. In this case, the link inductance charges through the input in the negative direction, and after a resonant mode, it discharges to the output. Table 5.1 summarizes all the possible switch faults cases in case I.

It should be noted that the type-I reduced-switch mode of operation is always preferred over type-II operation. The reason is that type-II of operation causes higher voltage stress on the switches. Therefore, when both types I and II can be employed, type I should be selected. For example, if switches S_3 and S_7 break to open-circuit, the faulty case can be

considered as either case I.A or case I.C according to Table 5.1. Based on Table 5.1, case I.A works in the type-I algorithm while case I.C operates with the type-II mode of operation. Therefore, case I.A and the subsequent type-I algorithm is selected for the converter's operation during this fault.

Table 5.1. Summary of the switch faults states in Case I.

SWITCH FAULT	**CASE #**	**OPERATING ALGORITHM**
One or several of these devices break to open-circuit: S_3, D_4, S_7, D_8, S_{13}, S_{15}, S_{17}, S_{19}, S_{21}, S_{23} (dashed-line devices in Fig. 5.6)	Case I.A	Type-I reduced-switch algorithm
One or several of these devices break to open-circuit: D_1, S_2, D_9, S_{10}, S_{14}, S_{16}, S_{18}, S_{20}, S_{22}, S_{24} (solid-line devices in Fig. 5.6)	Case I.B	Type-I reduced-switch algorithm in the negative direction
One or several of these devices break to open-circuit: S_3, D_4, S_7, D_8, S_{14}, S_{16}, S_{18}, S_{20}, S_{22}, S_{24} (dashed-line devices in Fig. 5.7)	Case I.C	Type-II reduced-switch algorithm
One or several of these devices break to open-circuit: D_1, S_2, D_9, S_{10}, S_{13}, S_{15}, S_{17}, S_{19}, S_{21}, S_{23} (solid-line devices in Fig. 5.7)	Case I.D	Type-II reduced-switch algorithm in the negative direction

5.5. Case II: An Input-Side Switch Remains Closed

In case II, the short-circuit faults of the input-side power switches are considered. Based on the formation of the switch fault, this case is sub-categorized into two states. Fig. 5.8 shows case II.A in which either or both of D_9 and S_{10} break to short-circuit. In this case switch S_2 is considered as the only input-side switch, which can charge the link inductance in the positive direction. Switches S_3 and S_7 should not be turned on as they will short the input voltage or the link. The converter with only one working switch S_2 is similar to the type-I reduced-switch resonant converter, presented in section 3. As a result, the type-I operating algorithm can be employed during this fault to run the converter effectively. Note that power switches S_{13}, S_{15}, S_{17}, S_{19}, S_{21}, and S_{23} are not required for type-I operating mode and they should remain off.

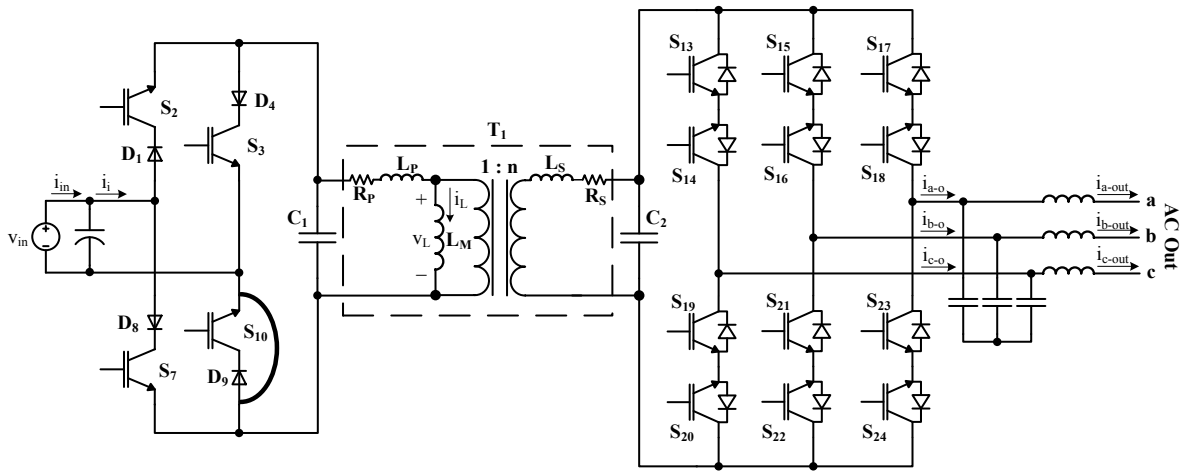

Fig. 5.8. Case II.A: An input-side switch remains closed

In case one or both of the D_1, S_2 break to short-circuit, the similar scheme II.A can be used to run the converter with the type-I operating algorithm. In this case, switch S_{10} is used

as the only input-side switch to charge the link inductance in the positive direction, and output-side switches transfer this energy to the output. Similarly, devices S_{13}, S_{15}, S_{17}, S_{19}, S_{21}, and S_{23} are not required for the type-I operating mode and they should remain off.

If one or both of the S_3 and D_4 break to short-circuit, the faulty case is considered as case II.B. Similar to the above discussed cases, the converter can work with the input-side switch S_7 to charge the link inductance in the negative direction. As a result, the faulty converter can work effectively in the type-I reduced-switch algorithm in the negative direction and feed the load at a reduced output power. Break to short-circuit of the devices S_7 and D_8 can also be managed in this scenario. Table 5.2 summarizes the faulty states considered in case II.

5.6. Case III: A Load-Side Switch Remains Closed

In case one of the load-side switches gets shorted, there is no general solution. However, for high-power applications in which each power switch of the proposed converter is realized by two or three IGBTs in series, there is a solution. In this case, the circuit of Fig. 5.9 can be considered where each power switch of the converter is made by three IGBTs in series and one of the IGBTs of switch S_{17} has broken to short circuit. Since the other two IGBTs of S_{17} are working properly, it is still possible to run the converter effectively. However, the voltage stress on switch S_{17} should be decreased so that these two IGBTs will not experience over voltage stress. Note that the peak forward voltage and peak reverse voltage of the input-side switches of the original isolated HFAC-link topology can be expressed as follows:

$$PFRV_I = \frac{1}{2}V_{in} + \frac{1}{2}V_{LP} \tag{5.1}$$

Table 5.2. Summary of the switch faults states in Case II.

SWITCH FAULT	CASE #	OPERATING ALGORITHM
One or both of these devices break to short-circuit: D_1, S_2	Case II.A	Type-I reduced-switch algorithm
One or both of these devices break to short-circuit: D_9, S_{10}	Case II.A	Type-I reduced-switch algorithm
One or both of these devices break t short-circuit: S_3, D_4	Case II.B	Type-I reduced-switch algorithm in the negative direction
One or both of these devices break to short-circuit: S_7, D_8	Case II.B	Type-I reduced-switch algorithm in the negative direction

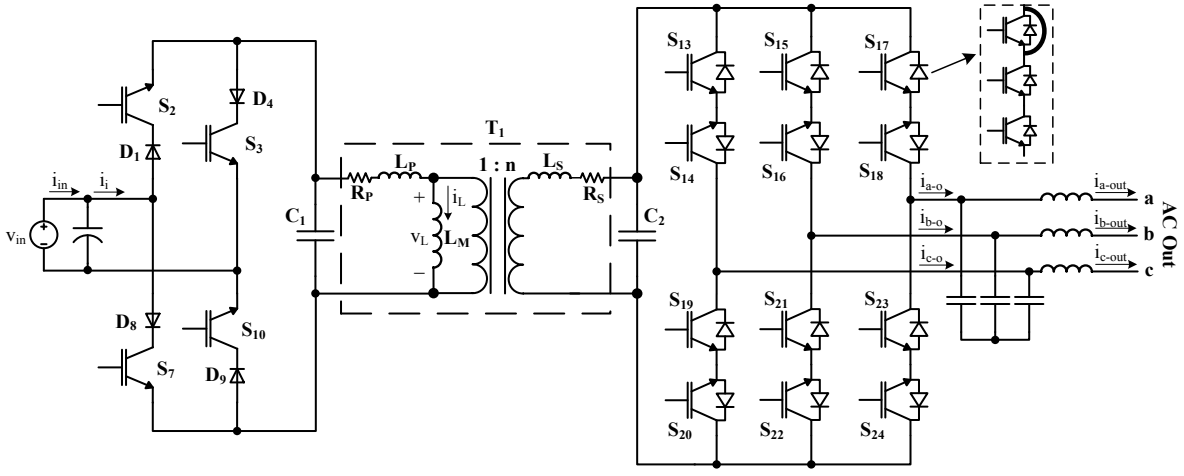

Fig. 5.9. Case III: A load-side switch remains closed

where V_{in} is the input voltage, and V_{LP} is the link peak voltage. The peak forward voltage and peak reverse voltage of the output-side switches of that converter can be given by,

$$PFRV_O = \sqrt{\frac{2}{3}}V_{Lo} + \frac{n}{2}V_{LP} \tag{5.2}$$

where V_{Lo} is output line rms voltage. Since one of the three IGBTs of switch S_{17} is broken to short circuit, the peak forward voltage of S_{17} should be reduced by 67%. As a result, $\sqrt{\frac{2}{3}}V_{Lo} + \frac{n}{2}V_{LP}$ should be decreased by 67%. V_{LP} is selected at least 10%-15% higher than the input voltage and should be at least equal to the output peak line-to-line voltage ($\sqrt{2}V_{Lo}$). Therefore, in order to decrease the peak forward voltage of switch S_{17}, the output line rms voltage should be mainly reduced. By decreasing the output voltage, the output power is decreased, but the converter can still work to survive the load under this faulty condition until the broken switch is replaced.

6. CONCLUSIONS AND FUTURE WORK

This study introduced several isolated and non-isolated power converters with high-frequency ac links and soft-switching operation for low, medium, and high power applications. The converters can be employed in various configurations, such as direct ac-ac wind converters, single-stage grid-tied PV inverters, multi-string inverters for PV applications, soft-switched isolated and non-isolated dc-dc converters, and multiple-input multiple-output dc-dc converters. These topologies are expected to have high reliability owing to the exclusion of short-life electrolytic capacitors, high efficiency as a result of soft switching operation, and high power density due to the use of a high-frequency transformer for galvanic isolation. The partial-resonant high-frequency ac link of the introduced topologies is composed of a small inductor in parallel with a small ac capacitor. The main role of the inductor is to transfer power by charging from the input and discharging to the output, or vice versa. The parallel capacitor creates partial resonances to realize zero-voltage turn-on and turn-off for the power switches. The inductor can be simply replaced by an air-gapped high-frequency transformer to achieve galvanic isolation. In this dissertation, the control schemes and switching algorithms of the proposed converters were described. The detailed behaviors of the converters were shown analytically, and the effectiveness of the proposed power topologies was verified by means of the simulation and experimental results. It was also demonstrated that some of the proposed topologies have fault-tolerance capability; in case of one or more faulty switches, they may still be able to operate with alternative operating algorithms.

For future work, it is suggested that a prototype of the proposed converters be built with a much higher switching frequency to reveal the converters' benefits more effectively. In order to accomplish this project, a faster DSP or an FPGA may be employed with a smaller sampling time. As a result, the link inductance and capacitance can be properly decreased to increase the switching frequency. The prototype's bidirectional switches can also be realized by reverse-blocking switches to get higher conversion efficiency. Reverse-blocking IGBTs are now available on the market, such as IXRH40N120 from IXYS. Another future research option includes modifying the operating algorithms of the original soft-switched high-frequency ac-link converter and the reduced-switch topologies to extend the range of the allowable load power factor. In addition, modifying the operating algorithms of the converters in order to remove the second short charging or discharging modes can be a beneficial research topic. In this way, the conversion efficiency can be increased considerably while the stresses on the switches are diminished. Finally, multi-objective design optimization of the introduced converters in terms of power density and conversion efficiency is critically proposed.

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