ANALYSIS AND DESIGN OF NEW HARMONIC MITIGATION APPROACHES

A Dissertation

by

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Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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December 2012

Major Subject: Electrical Engineering

ABSTRACT

Numerous approaches have been proposed in order to resolve the problems of current harmonics in electrical distribution systems. The rapid development of power semiconductors along with the revolutionary advances on microprocessors consolidated the motor drives industry and with it a massive proliferation of non-linear loads. It was thought that these very same technological advances would trigger an explosive development of harmonic solutions based on power electronics. Moreover, the introduction of the instantaneous active and reactive power theory or the so-called p, q theory which simplifies and gives more robustness to the control strategies of active filters reinforced this idea. Three decades have passed since the first IGBT was introduced in early 1980s, and active harmonic solutions are not the first choice to solve harmonic pollution in electrical distribution systems, mainly due to the high cost and the perception of low reliability. Given this scenario, in this work two main approaches are explored. First, the combination of an asymmetric 18-pulse rectifier with a reduced KVA active harmonic filter to improve the performance under abnormal utility conditions. Second, an interleaved active harmonic filter using multiple inverters connected in parallel at the ac and dc size, which will allow for higher power ratings and power density increase.

The performance issues of the asymmetric 18-pulse rectifier under unbalanced voltage and pre-existing harmonic components are analyzed, as well as the current distortion improvement, achieved when an active power filter is introduced.

On the other hand, the high frequency harmonic cancellation when interleaved inverters are used, the circulation of zero-sequence current and the impact of interleaving on dc bus capacitor are analyzed. Finally, some methods to mitigate the low frequency circulating currents based on eliminating the zero-sequence component, and the introduction of common mode inductors to reduce the high frequency circulating current are studied.

Without a doubt the search for new cost-effective topologies able to reach broader power levels and voltage ranges will continue emerging giving more alternatives to users. Moreover, extensive research on wide band gap devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN), with which it is possible to reach higher voltage breakdown and at least an order-of-magnitude lower switching losses, makes the future more promising for active solutions.

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CHAPTER I

INTRODUCTION

1.1. Introduction

Significant advances on power semiconductors and microprocessors enabled the massive proliferation of motor drives and switching power supplies in the 1980s and early 1990s. Concurrently, harmonics problems raised serious concerns among electrical engineers. Overheating of transformers and cables, failure of capacitor banks due to resonance and interference with telecommunication systems were common symptoms of distributions systems overloaded with current harmonics [1]-[13]. Excessive third harmonic current was also frequently observed on the neutral conductors of commercial buildings as a result of multiple single phase power supplies [14]-[17].

Extensive research has been conducted and multiple approaches to reduce current harmonics have been proposed, developed and commercialized over the years. Ones are based on increasing the tolerance of existing electric devices to withstand harmonics currents such as K-rated transformers, and increased cross section of neutral conductors [18]-[21]. Others are based on eliminating or reducing the circulation of current harmonics. Amongst the latter, are passive tuned filters and power electronics based converters such as multi-pulse rectifiers, active front end converters and active harmonic filters.

Passive filters or harmonic traps are cost effective and can provide an acceptable current harmonic cancellation however, they are bulky, heavy, can introduce resonance in the power system and can only be tuned to effectively cancel a single harmonic. Therefore multiple filters have to be installed in order to eliminate more than one harmonic [22].

Multi-pulse rectifiers are based on the principle of harmonic cancellation through phase shifting and are the preferred solution to eliminate harmonics in high power converters in large motor drives, electro-winning rectifiers and HVDC transmission systems [23]-[37]. However, they need bulky phase shifting transformers and are usually used in conjunction with passive filters to eliminate the rest of harmonics that the multi-pulse rectifier is not able to cancel out [38], [39].

Active solutions - power electronics approaches based on hard switching semiconductors are a viable solution which presents a better alternative when weight and footprint is a constraint. Among them are active front ends (AFE) or active PWM rectifiers [40], active harmonics filter (AHF) or also called active power filters (APF) [41]-[60]. Active power filters are usually classified depending on the way they are connected to the electric system and are divided in shunt APFs and series APFs [60]. Furthermore, hybrid APFs; approaches based on a combination of a passive tuned filter and a reduced KVA APF have been extensively studied [61]-[66].

Hard switching active power filters are practically only used in very special cases, usually at very large horsepower ratings or when size and footprint constrains prohibit the utilization of bulky passive solutions. This is the case of oil offshore

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platforms, marine vessels and more recently, aircrafts. However, the majority of active power filters on transmission and distribution systems are for reactive power compensation and not for harmonics mitigation. For industrial distribution systems the situation is similar, large rectifying plant for electro-winning or electro-refinery still prefer passive solutions [22]. A similar scenario occurs in compensating harmonics for adjustable speed drives, the preferred solution is either a passive filter or a drive furnished with a multi-pulse diode rectifier.

Moreover, active solutions offer higher flexibility, high performance over a large zone of operating conditions and they guarantee high reliability due to state-of-the-art semiconductors. However, at large horse power rating and at medium voltage the present technology on hard switching devices do not allow operating at high switching frequencies necessary to guarantee the reconstruction of the harmonics to mitigate. This is the main drawback of active solutions which forces the utilization of cutting edge switching devices and complex control strategies which consequentially make them more expensive and in some cases incapable to be a viable solution for very large horse power ratings.

In this work two approaches will be studied, which can serve, in part, to fill the gap for lack of semiconductor devices capable of switching at high switching frequencies with low losses and that guarantee high performance for large APFs. The first one is a combination of an asymmetric 18-pulse rectifier with a reduced KVA active harmonic filter to mitigate harmonics at the front end of adjustable speed drives [37]. The asymmetric 18-pulse rectifier guarantees low harmonic injection for great portion of

operating conditions. It is highly reliable since not active components are present and allows for reduced footprint and lighter weight than conventional 18-pulse rectifiers since a fractionally rated autotransformer is used. However, this topology evidences some drawbacks in the presence of abnormal input voltage conditions such as; voltage unbalance and pre-existing harmonic distortion - the theoretical harmonic injection profile is deteriorated. A shunt APF is proposed in order to operate when abnormal voltage conditions are present and cancel out the current harmonics the 18-pulse rectifier fails to mitigate. A simple control strategy based on forcing the current waveform to track the input voltage waveform is employed.

The second approach consists on an APF based on interleaved parallel inverters. The inverters are connected at the ac and dc bus and no isolation transformers are employed as proposed on previous publications. The utilization of interleaved carriers allows for the reduction of semiconductor's switching losses, increase of effective carrier frequency, and reduced size of linkage reactors. The manifestation of low and high frequency (HF) circulating current between the parallel converters will be analyzed. The introduction of common mode inductors is proposed to reduce the HF circulating current and a zero-sequence control loop to mitigate the low frequency circulating current is also proposed [56]-[58].

1.2. Power Quality Standards

1.2.1 IEEE 519-1981 [67]

In 1981, the institute of electrical and electronics engineers released the "Guide for harmonic control and reactive compensation of static power converters." This guideline intended to help electrical engineers with the application of rapidly emerging adjustable speed drives and power electronics based converters. Even though many large companies, such as metal rolling mills and mining operations had recognized the problems with harmonics and developed mitigation techniques by the utilization of multi-pulse converters, the massive proliferation of small size power converters made the harmonic problem much more complicated to resolve. New users of power converters did not have engineers helping to mitigate harmonics problems. Extensive analysis was necessary to determine whether or not the new converters were going to be a problem. It was impractical and not economical to mitigate the harmonics for each non-linear load. Therefore, the IEEE 519-1981 was designed to help these users with the application of emerging non-linear loads.

However, the harmonics guidelines on IEEE 519-1981 were limited to voltage distortion only (TABLE I and TABLE II) and did not prevent a user from using all power capacity with large harmonics. Even though a user could have been complying with the voltage standard limits, large current harmonics that potentially overheat transformers or cause other system's interference could circulate through the power systems. It was clear the need of a revision to these guidelines where current harmonics

limits were a function of the power system ability to withstand the circulation of harmonics. The standard was revised and the well-known IEEE 519-1992 was born.

TABLE I
LOW-VOLTAGE SYSTEMS CLASSIFICATION AND DISTORTION LIMITS FOR 460V SYSTEMS [67].

Class	ρ	DF (%)
Special Application (*)	10	3
General System	5	5
Dedicated System	2	10

(*) Special applications are those where the rate of change of voltage of the notch might mistrigger an event.

DF= Voltage Distortion Factor

ρ= impedance ratio of total impedance to impedance at common point in system.

TABLE II
VOLTAGE DISTORTION LIMITS FOR MEDIUM AND HIGH VOLTAGE POWER SYSTEMS [67]

Power System Voltage Level	Dedicated System Converter (*)	General Power System
Medium Voltage 2.4 – 69kV	8%	5%
High Voltage 115 kV and above	1.5%	1.5%

 (*) A dedicated system is one servicing only converters or loads not affected by voltage distortion.

1.2.2 IEEE 519-1992 [68]-[70]

The IEEE 519 -1992 was an update to the 1981 guidelines. It was a significant improvement and it was upgraded to the category of "Recommendation practices and requirements".

The new IEEE-519 standard established the limits for current distortion that customers need to comply with and voltage distortion that the utility company should comply with (TABLE III and TABLE IV). The 1992 revision gave a more comprehensive understanding that the harmonic problem was a responsibility of both users and utility companies.

The standard set the limits for individual current harmonics and for total demand distortion (TDD) for a given short circuit current to load current ratio (I_{sc}/I_L). The spirit of standard is that stiffer systems, the ones that feature larger I_{sc}/I_L ratios, have the ability to withstand larger current harmonics distortion. The concept of TDD or total demand distortion was introduced in order to properly weigh the impact of harmonics on the system. The TDD corresponds to the ratio between the rms value of current harmonics of order higher than two and the maximum fundamental demand load current (I_{ML}) sustained for 15 to 30 min. This figure of merit differs from the distortion factor (DF) which quantifies how distorted is the signal from a sine-wave without considering if those harmonic levels are actually a real threat to the system.

$$TDD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_{ML}}$$

TABLE III

CURRENT DISTORTION LIMITS FOR GENERAL DISTRIBUTION SYSTEMS (120V THROUGH 69,000 V) [68]

I_{sc}/I_L	Individual Harmonic Order (Odd Harmonics)					
	<11	$11 \leq h \leq 17$	$17 \leq h \leq 23$	$23 \leq h \leq 35$	$h \leq 35$	TDD
<20 *	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

TDD: Total Demand Distortion is the harmonic current distortion in % of the maximum 60 Hz demand load current taken at the PCC (15-30 min).

I_{sc}: Maximum Short Circuit Current at PCC.

I_L : Maximum Demand Load Current (fundamental frequency component) at the PCC.

* Even harmonics are limited to 25% of the odd harmonic limits above.

 Where I_{ML} is the maximum 60Hz demand load current (15-30 min demand)

TABLE IV

VOLTAGE DISTORTION LIMITS [68]

Bus Voltage at PCC	Individual Voltage Distortion (%)	Total Voltage Distortion THD (%)
69 kV and below	3.0	5.0
69.001 kV through 161 kV	1.5	2.5
161.001 kV and above	1.0	1.5

Note: High-voltage systems can have up to 2.0% THD where the cause is an HVDC terminal that will attenuate by the time it is tapped for user.

1.2.3 IEC 61000 EMC [71]-[74]

The main difference between the IEEE 519 standard and Electromagnetic compatibility standard from the International Electromechanical Commission EMC IEC 61000 is the fact that the latter is aimed to limit the harmonic contribution of electrical equipment as oppose to merely electrical system recommendations that mitigates the impact of current harmonics. In that regards, it explicitly applies to electrical manufactures while IEEE 519 means to give recommendations to users on the application of power electronics converters.

The IEC 61000 comprises several standards that limit harmonic contribution:

- **IEC 61000-3-2 (1998-04):** Electromagnetic Compatibility (EMC) – Limits for harmonic current emissions (equipment input current up to and including 16 A per phase) [71].

- **IEC 61000-3-4 (1998-10):** Electromagnetic Compatibility (EMC) – Limitation of emission of harmonic currents in low-voltage power supply systems for equipment with rated current greater than 16 A (TABLE V) [72].

- **IEC 61000-3-3 (1994-12):** Limits - Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current ≤ 16 A per phase and not subject to conditional connection [73].

- **IEC 61000-3-5 (1994-12):** Limits - Limitation of voltage fluctuations and flicker in low-voltage power supply systems for equipment with rated current > 16 A [74]

TABLE V

REVIEW OF IEC 61000-3-4 (FIRST EDITION 1998-10)[1] [72]

Stage 1 current emission values for simplified connection of equipment

Harmonic number n	Admissible harmonic current $I_n/I_1 *\%$	Harmonic number n	Admissible harmonic current $I_n/I_1 *\%$
3	21, 6	21	$\leq$0, 6
5	10, 7	23	0, 9
7	7, 2	25	0, 8
9	3, 8	27	$\leq$0, 6
11	3, 1	29	0, 7
13	2	31	0, 7
15	0, 7	33	$\leq$0, 6
17	1, 2		
19	1, 1	Even	$\leq$ 8/n or $\leq$ 0, 6

I_1 = rated fundamental current; I_n = harmonic current component

$$R_{sce} = \frac{Short\ Circuit\ VA}{Rated\ VA}$$

1.3. Conventional current harmonic elimination solutions [22]

There are several ways to reduce current harmonics in electrical systems. Without loss of generality, they can be divided in to two main methods. There are ones that aim to reduce the contribution of current harmonics from the non-linear loads by modifying the front end of the equipment with multi-pulse converters or active front ends, and the ones that aim to eliminate or mitigate the propagation of the harmonics upstream from a the point of harmonic source. Among the latter, the most common

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[1] IEC 61000-3-4 ed.1.0 "Copyright © 1998 IEC Geneva, Switzerland.www.iec.ch"

devices are passive filters. The underlying mechanism behind passive filters is to present low impedance for the harmonic to be eliminated. The impedance presented by the filter should be significantly lower than the equivalent impedance of the power source at the frequency to be filtered. Therefore, the current harmonic will circulate between filter and load and it will not propagate to the rest of the electrical system. In other words, the harmonic will be trapped in the filter; that is the reason why passive filters are often referred to as harmonic traps.

Fig. 1 shows a simple equivalent circuit of a passive filter.
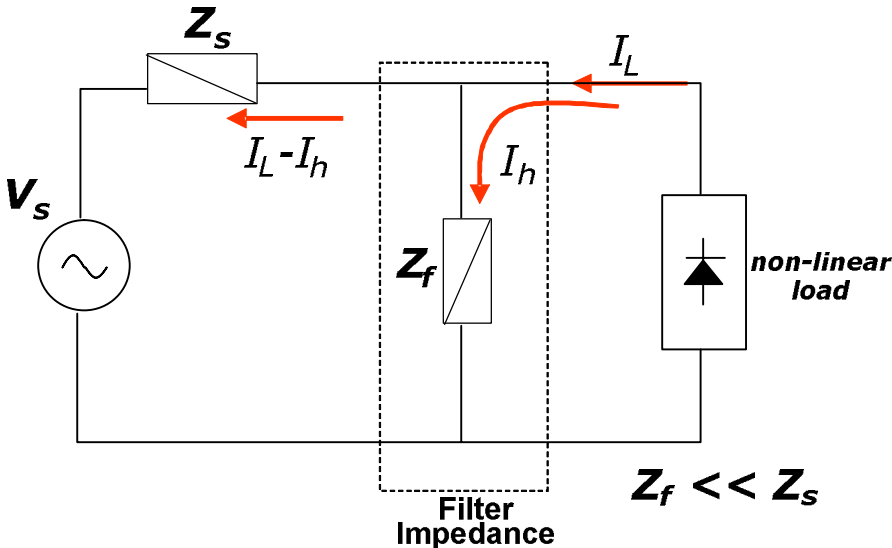
Fig. 1. Passive harmonic filter equivalent circuit.

Where;

Zs : Source impedance

Zf: Filter impedance

Other methods to reduce harmonics consist on providing equipment furnished with front ends that inject lower harmonic contents. Multi-pulse rectifiers are well known and they have extensively studied. They work based on the principle of harmonic cancellation. The most command multi-pulse converter is the twelve pulse rectifier. It is typically composed for 2 six-pulse rectifiers and a shifting transformer. The rectifier can be connected in parallel or series connection and the transformer has two secondaries supplying the same voltage but with a phase angle shift of 30°.

1.3.1 Tuned passive filter

As mentioned on the previous section, the tuned passive filters (Fig. 2) work based on the principle of providing and alternative branch that would trap the harmonic to be eliminated. The impedance of the filter has to be significantly lower than the source impedance. A tuned harmonic filter is typically composed of an inductor in series with a capacitor. The values of L and C are selected in a way such that the cut-off or resonance frequency of the circuit corresponds to the harmonic frequency to be mitigated.

In general, the impedance of the filter branch can be expressed as:

$$\left| Z_f \right| = \left| R_f + 2\pi f L_f - \frac{1}{2\pi f C_f} \right|$$

Making $Z_f \to 0$

$$2\pi f_c L_f - \frac{1}{2\pi f_c C_f} = 0$$

Therefore, the frequency f_c at which the tuned filter's impedance is minimum is:

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}}$$
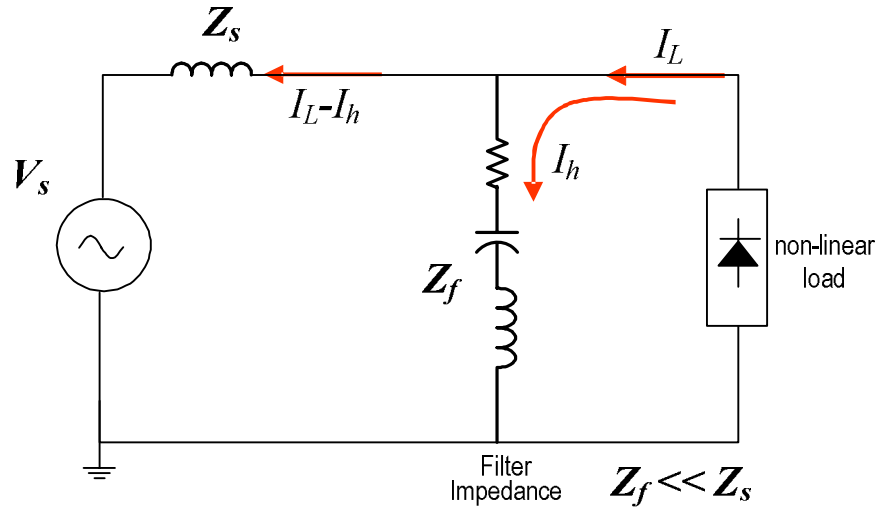
Fig. 2. Tuned passive harmonic filter
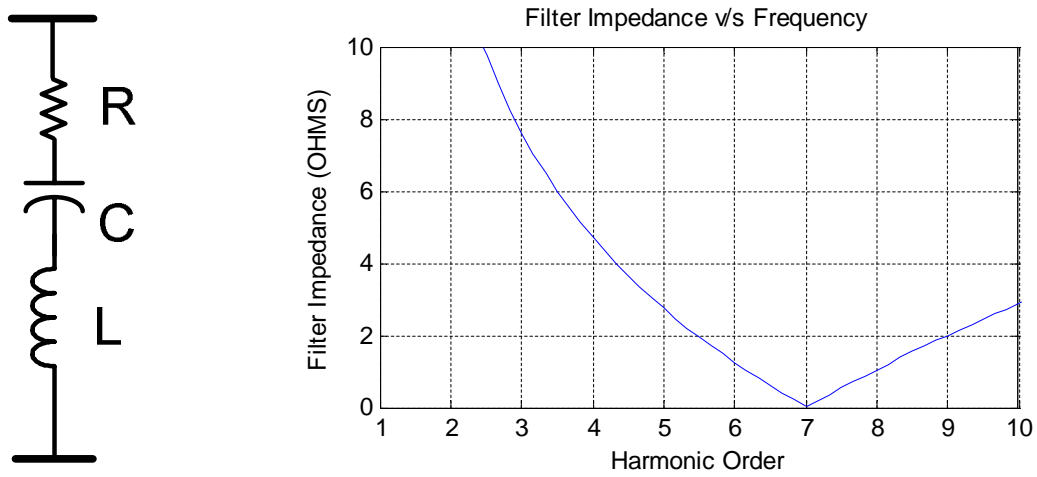
Fig. 3. Tuned passive harmonic filter and frequency response characteristic.

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The typical design criterions for tuned passive filters typically consider; the reactive power to compensate displacement power factor (DPF - at 60Hz), resonance frequency equal to 0.95 times the frequency to be eliminated and a quality factor (Q) between 30 and 60. The quality factor Q is a dimensionless figure of merit that characterizes the filter bandwidth relative to its resonance frequency. In other words, it gives an indication of the damping of the filter structure. For a tuned passive filter as shown in Fig. 3, the quality factor is:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

The main advantages of tuned passive filters are their simplicity and low cost. However, issues such as resonance, prone to overload, detuning, and the fact that they can only be designed to mitigate a single frequency are a big concern. The effectiveness of the passive filters depends upon presenting an impedance, for a given harmonic, lower than the source's impedance, however, the source impedance can change unexpectedly and modify the response of the filter. They can also serve as a low impedance path for unintended harmonics, resulting in unwanted overloading. On the other hand, the tuned filters depend upon inductor and capacitor values. But the capacitor and inductors are susceptible to parameter tolerance deviations that can detune the filter.

Tuned filters can only be tuned to effectively filter a single harmonic therefore multiple branches must be used when more harmonics want to be filtered.

1.4. High pass filter [22]

A high pass filter presents low impedance for frequency above the resonant frequency. The objective is to mitigate more than one harmonic. However, they draw high current at fundamental frequency which increases the resistive losses.

Fig. 4.a shows a high-pass filter equivalent circuit and Fig. 4.b its typical frequency response.
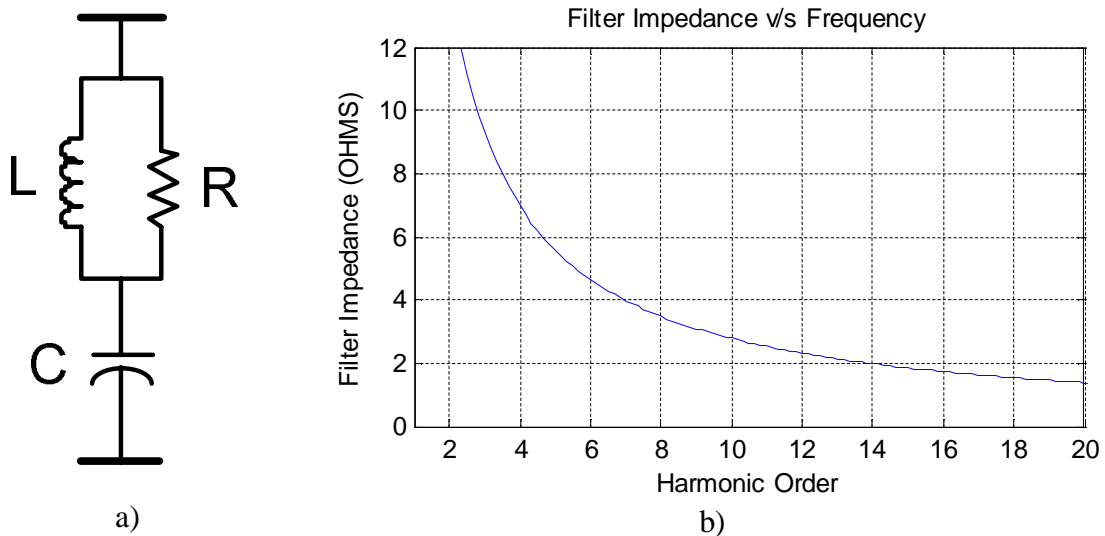
Fig. 4. a) High-pass passive harmonic filter and b) its frequency response characteristic.

A modification of the high pass filter is the circuit shown in Fig. 5.a, the capacitor C2 reduces the filter's fundamental current which reduces the losses. Fig. 5.b shows its typical frequency response. The filter can be designed to more effectively mitigate a band of harmonics.
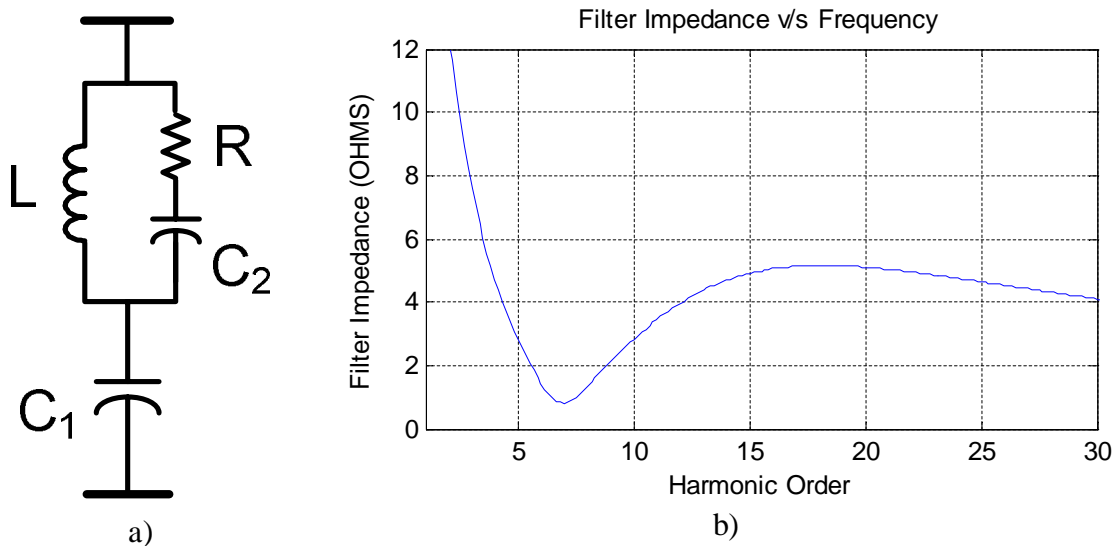
Fig. 5. a) High-pass (modified) passive harmonic filter and b) its frequency response characteristic.

1.5. Active harmonic filters (AHF)

1.5.1 Shunt Active Filter [42][43][60]

Shunt active harmonic filters (SAHF) are power electronics based devices used as controlled current sources. Modern active filters are microprocessor controlled which gives them high flexibility and versatility. The SAHF would inject a current with the same magnitude of the harmonic to be eliminated but with a perfect 180° phase angle, resulting in the cancellation of the current harmonic and preventing it from circulating to the rest of the electrical system. The main advantage of active filters is the fact that it is possible to cancel a wide range of harmonics with the same device. The active filter can simultaneously inject a current which is composed of several harmonics with different phase angle. Since they are precisely controlled, they can also be selective in the way the generate harmonics, giving the user the option to mitigate a single harmonic or a group

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them. Graphic human interfaces make them easy to use and monitor their performance.

Fig. 6 shows a conceptual single line diagram of a shunt active filter.
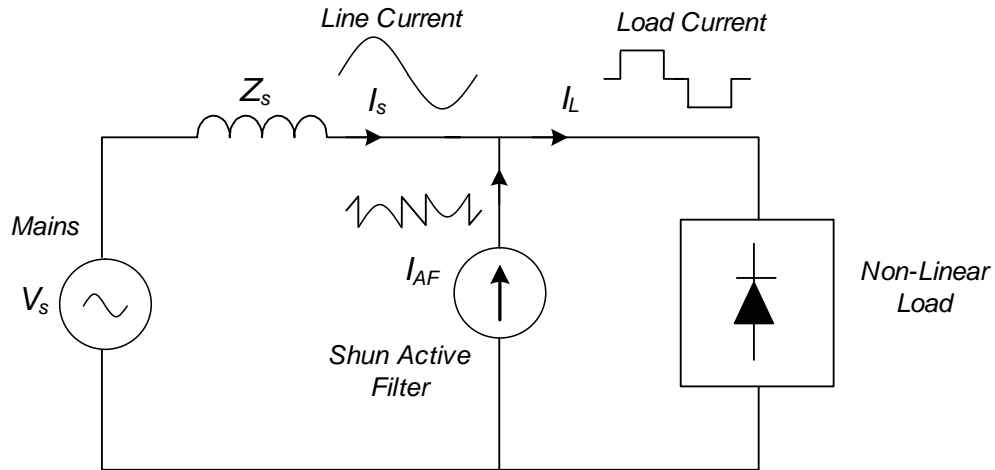
Fig. 6. Shunt active power filter conceptual circuit.

1.5.2   Series Active Filter [60]-[62]

Series active filters (SAF) are power electronics based devices used as controlled voltage sources. They are connected in series with the electrical systems, between the source and the nonlinear load. Series active filters are based on the principle of harmonic isolation by controlling the voltage injected by the filter at the frequency to be eliminated. By increasing the voltage, the SAFs are able to present high impedance for the harmonic currents, resulting on the blocking of the unwanted harmonics and preventing them from flowing to the source. In other words, the SAF can cancel out the virtual equivalent harmonic voltage source imposed by the load. The main drawback of SAFs is the fact that a series injection transformer needs to be used to interface with the system in order to inject the active filter's voltage. This transformer requires a special

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design which increases its cost. The transformer must provide very low voltage for line frequency load current circulation. The other practical disadvantage of SAFs hinges on the complexity of the protection system for the active filter converter which must be designed to withstand load's short circuits. During a short circuit event, the high load current will reflect on the secondary of the injection transformer generating dangerous voltages and potentially damaging the active filter converter [62]. Typical protection schemes consider a thyristor based bypass that closes to bypass the converter when the load suffers high current fault conditions and consequently protects the converter from catastrophic failure. Fig. 7 shows a conceptual diagram of a series active filter.
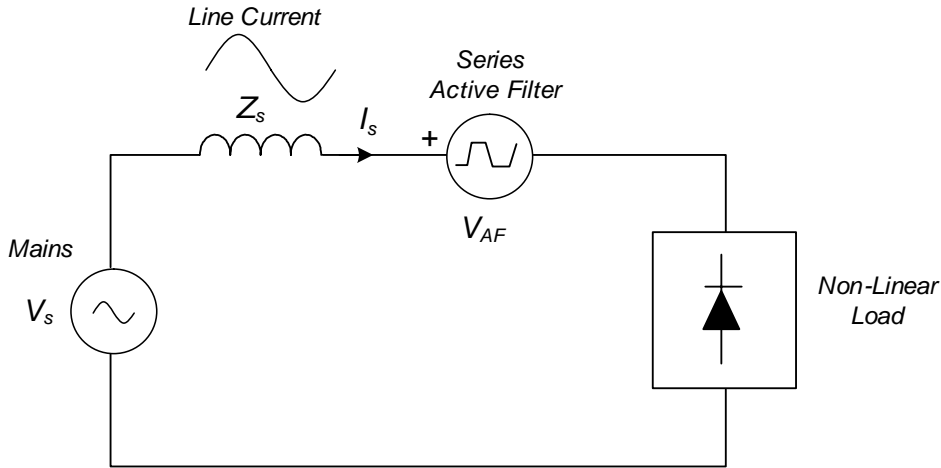
Fig. 7. Conceptual visualization of a series active filter

1.5.3 Hybrid Active filters [60][63]-[66]

In principle, hybrid filters are a combination of a passive filter and an active filter. Typically a hybrid filter consists of a passive tuned (shunt) filter and a series active filter. The addition of the series active filter yields to significantly improvements

on the passive filter frequency response, extending the filtering capabilities. The main practical advantage of hybrid active filters is the fact that the KVA rating of the inverter can be a small fraction of the total load kVA (<5%). This is reduces significantly the efforts and cost on power electronics. Low kVA rating inverters with higher current bandwidth can then be used since no large blocks of power need to be handled with power electronics converters.

The series active filter in a hybrid filter can be connected in series with the systems between the source and the passive filter or in series with each branch the shunt passive filters, the latter it is referred to as parallel hybrid active filter.

1.5.4 Combination of shunt and series active filters [60] [75]-[79]

Another trend on active harmonic filters consists on a combination of a series active filter and a shunt active power filter. They can be configured to either control active and reactive power flow or mitigate current and voltage harmonics. A very popular configuration is the so called unified power flow controller (UPFC) which was introduced by Gyugi [77] to enable flexible ac transmission systems (FACTS). Another topology is the unified power quality controller (UPQC) which aim to mitigate power quality problems such as current harmonics and voltage disturbances.

A. The Unified Power Flow Controller (UPFC) [75]-[79]

The unified power flow controller is a combination of a series and a shunt active filter (Fig. 8), and it is typically conceived to provide power control on a meshed power

transmission system. The main advantage of UPFCs is the ability to control reactive power and active power flow. It was initially proposed by Gyugyi and Hingorani and it is considered a key component of the so called flexible ac transmission systems (FACTS), a concept first introduced by the latter author.

The shunt active filter is composed of a PWM inverter which is connected to the system with the objective to control reactive power at the point of common coupling. Dynamic reactive power control can improve the stability of the ac system by increasing the maximum active power that can be transmitted and flatten voltage profile. A series active filter composed of a PWM inverter is connected in series with the load side through a series injection transformer with the objective to provide; power flow by modifying the line effective impedance and damping of sub-synchronous resonance. The dc buses of both inverters are tied together allowing the flow of active power between shunt and series converter as needed. Even though both shunt and series active converters have the ability to control independently active and reactive power, the active power must be set equal for both converters in order to guarantee energy balance and maintain rated dc bus voltage. In practice small difference in active power would be allowed to compensate for losses in the converters.

In the case of the unified power flow controller, the active filters are not designed to provide harmonics cancellation rather to control of the fundamental components. However, the topology is still capable of doing so if provided the proper bandwidth.
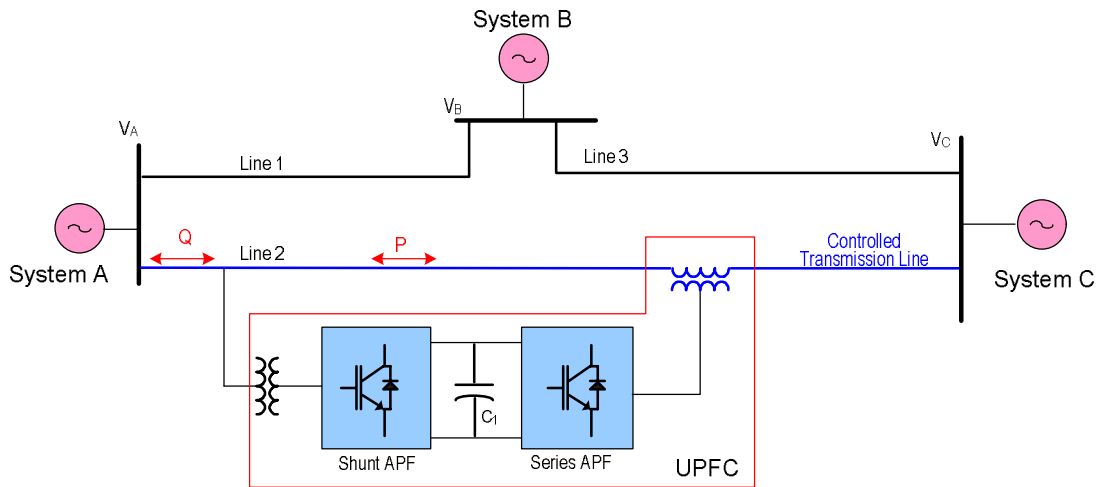
Fig. 8. Unified power flow controller (UPFC)

B. **The Unified Power Quality Conditioner (UPQC)** [60]

The unified power quality controller (Fig. 9) consists also on a combination of a shunt and series active filter; however it is properly designed with the objective to compensate for harmonics components. It constitutes one the most flexible power electronics devices for harmonic compensation. The shunt active filter is in charge of current harmonics cancellation and the series active filter can compensate for voltage harmonics and imbalances of the power supply. The way the UPQC is connected to the electric system is somewhat different than the UPFC. The shunt active filter is connected as close as possible to the non-linear load and the series active filter is connected between the source and the shunt active filter point of common coupling. Even though the topology is suitable to compensate for fundamental reactive power, it is preferable to avoid it and therefore reduce the power rating of the converter.

The typical converter topology is identical to the UPFC consisting of a back-to-back two level inverter. Passive LC or RLC filters at both sides are necessary to eliminate high frequency ripple caused by the converter switching frequency.

The series active filter will be responsible for compensating pre-existent voltage harmonic due to non-linear loads upstream of the system. It can also be designed to compensate voltage unbalance by providing the proper fundamental negative-sequence component.
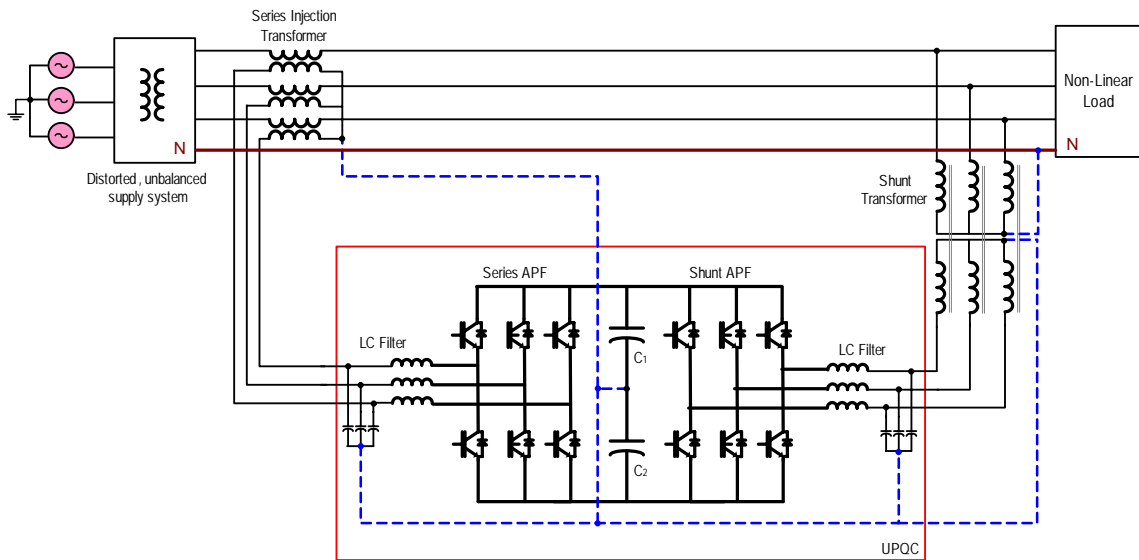
Fig. 9. Unified power quality conditioner.

1.6. Previous work

Multiple has been the efforts in order to mitigate harmonics generated by power electronics converters with minimum demand on extra components such as; additional power electronics converters, transformers or passive LC based filters. It is highly

desired that not significant weight, volume and cost is added to the already costly power electronic converters. Choi and Enjeti in [55] proposed a converter front end with reduced kVA 12-pulse rectifier system utilizing an autotransformer and dc side interface reactor; where the autotransformer KVA rating is only 0.18 (p.u.) and the six-pulse rectifiers feature equal current sharing. Also, the same approach is extended to an 18-pulse rectifier system, where the transformer kVA rating is 0.16p.u. In [54] the same authors proposed a 12-pulse rectifier with active interphase reactor where a low kVA rated PWM converter is used to provide near sinusoidal input current.

Kamath in [32], proposed an ASD front end rectification method with autotransformer that is suitable for 18-pulse rectification and is rated at 0.33p.u. It differs from existing schemes by achieving harmonic current reduction without the need for equal diode-bridge current sharing, and eliminating the need for line-impedance matching inductors. The approach employs two extra auxiliary six-pulse rectifiers rated at 0.166p.u each, which significantly reduces the overall power converter kVA rating. This topology is referred to as asymmetric 18-pulse rectifiers, since not all the rectifiers share the current equally. An extensive analysis of similar asymmetric 18-pulse rectifier approach has been done in [33], however, no analysis under abnormal utility supply conditions, such as voltage unbalance and pre-existing harmonic distortion has been provided in this or in previous references. Furthermore, an equivalent asymmetric 18-pulse rectifier topology has been patented and commercialized by Toshiba Corp. [34] as a low harmonic adjustable speed drive to comply with the stringent harmonic requirement from the water and waste water market segment or in weak systems. Even

though, asymmetric 18-pulse rectifiers present good balance between performance cost and reliability, no significant research is found that analyze their performance under abnormal voltage conditions. The author *et al*. presented in [37] a reduced kVA active power filter to improve the performance of an asymmetric 18-pulse rectifier.

On the other hand, harmonic compensation using active solutions have been studied for decades. The principle of active compensation can be traced back to 1958, when McFarlane and Harris [41] proposed a method to compensate for voltage harmonics generated by non-linearity on the B-H curve in ferromagnetic materials. More than a decade later, Sasaki and Machida in 1971 [42], aiming to eliminate current harmonics in high-voltage DC transmission systems, introduced the modern concept of harmonic compensation in power systems. Their method was based on the principle of the magnetic flux compensation in a transformer core by injecting a compensating current into a tertiary winding. However, in the early 1970's, the hardware technology necessary to implement the compensation principle was not available. During the last three decades, however, remarkable progress on semiconductors with fast switching characteristics and higher current and voltage breakdown levels has been attained. Initially, great success with the development of thyristors and gate turn on devices (GTO) and more recently, multiple generations of insulated gate bipolar transistors (IGBT) are shaping the way active power filter technology is being deployed.

Theoretically, active power filters would compensate the entire unwanted harmonics spectrum, however, to do so converters with infinite bandwidth are necessary. In order to compensate for high order harmonics, the converter needs to accurately

reproduce the harmonics with the opposite phase to the harmonic to compensate; therefore high switching frequencies are necessary. Large power converters still cannot commutate at high switching frequencies, due to excessive switching losses. Significant advances such as in GTOs and IGCTs have enabled large power converters however the practical switching frequencies of these devices are still below ~600Hz. The last developments in IGBT like non-punch through and trench gate have increased the reliability of motor drives, however large IGBT based adjustable speed drives can only reach practical switching frequencies of around 2-3kHz. Certainly, not high enough to re-construct 7th or higher order harmonics. In addition, semiconductor's technology is also limited by the available current and voltage ratings. In order to cope with high-power requirements, several solutions, such as hybrid topologies [63]-[66], multilevel structures [80]-[86], and paralleled inverters are proposed in the literature [87]-[101].

Akagi *et al*. [88] proposed a parallel structure by using four inverters and solidly connecting the dc side. The reason for adopting this structure is to suppress the harmonics caused by switching operation without increasing the switching frequency, paying attention to practical applications. The ac side includes a power transformer for galvanic isolation. However, an isolation transformer is has a bulky design and suffers of larger power losses since it has to support the nominal current of the APF. Furthermore, the transformer for APF applications is an expensive component; it has to be designed with a high bandwidth according to the maximum compensated harmonic current. On the other hand, removing the transformer and connecting the inverters directly on the ac side, could contribute to circulation currents between the inverters.

Morán, Fernández, *et al.* in [53] proposed a simple and low cost shunt active power filter structure composed of two voltage source inverters in cascade; one GTO based located close to the non-linear load and operating at low switching frequency with the objective to compensate for reactive power and low frequency harmonics. And a second, IGBT based, shunt APF, operating at higher switching frequency and responsible for mitigation of higher order harmonics.

Kim and Enjeti in [30] and [55] proposed a new hybrid APF topology based on two voltage source inverts; one based on IGBTs and another one with lower kVA rating and based on MOSFETs. The former is designed with the ability to support utility fundamental and to compensate reactive power, and the latter designed for lower voltage rating and with the ability to compensate current harmonics. The dc bus of the MOSFET-based inverter is connected from one of the split capacitors of the IGBT based inverter dc bus. In [101] Moran, et al. proposed a shunt APF composed of three voltage source inverters connected in parallel at dc and ac side. Each inverter is operating at different switching frequency so that wider bandwidth can be attained and different semiconductors technology can be used according to their switching speed limitations. However, no analysis or acknowledgement regarding circulating current among the inverter is reported. And Z. Ye, et al. in [96] provides a comprehensive analysis and modeling of circulating currents for two parallel connected PWM rectifiers. However, no application for harmonics mitigation is reported.

1.7. Research Objective

The main objective of this dissertation is to analyze new cost effective topologies for harmonic mitigation in three-phase high power applications. Traditionally, harmonics mitigation has been done by passive filters and multi-pulse rectifiers. The former have the disadvantage that they are bulky, heavy, and its harmonic attenuation performance is highly dependent on the system impedance and that parallel resonance can occur between the source and filter impedances. Multi-pulse rectifiers have the disadvantage that bulky line frequency transformers specially designed to handle large harmonics are necessary and that passive filters are usually also needed to achieve high performance. To overcome these problems active power filters have emerged as a technically feasibly solution to mitigate harmonics. However when large current needs to be compensated limitations of semiconductor switching losses prohibit the realization of a large current active power filter since the practical switching frequencies cannot reach the bandwidth necessary to reconstruct the harmonics to be compensated. A prospect solution to this problem is the availability of high performance switching devices that can operate at high switching frequencies with low losses, and can withstand large reverse voltages. Extensive research has been done in switching devices made of different materials such as Silicon Carbide and Nitride Gallium; however these devices are still not developed or matured enough to provide a practical solution for large current applications. Therefore alternative power electronics converter topologies could offer a more immediate solution to mitigate harmonics in large current harmonics systems. When searching for new topologies, several key aspects need to be considered for the design which resides in five

main equally weighted pillars: high performance, high power-density, high efficiency, high reliability and low cost.

This work focuses on two topologies to mitigate current harmonics based on these design principles. One topology is based on extending the capabilities of an asymmetric 18-pulse rectifier to mitigate harmonics in motor drives by adding a shunt active power filter conforming a hybrid between a passive and active approach. The asymmetric 18-pulse rectifier provides high reliability and low losses since no active devices are involved in the current rectification process and since the phase-shifting input auto-transformer and active filter, are not rated for full load power.

A second topology based on parallel interleaved inverters is also studied. This topology can enable a modular structure for high current active power filters with reduced size of its passive components. The issues with the parallel connection of the inverters are studied such as the circulation of low and high frequency zero-sequence current. Even though this topology per se is not new, its practical application for active power filters has not been extensively reported.

1.8. Dissertation Outline

In the first chapter of this work is presented an introduction to conventional current harmonic mitigation methods and standards, designed and refined over the years in order to give guidance to engineers on how to operate the electrical systems in the presence of current harmonics. The characteristic of different approaches such as passive and active methods are explored. Among the formers, L-C network based filters and

multi-pulse rectifiers among the latters. Chapter II presents the state-of-the-art of harmonic mitigation methods for adjustable speed drives. It is pointed out the influence of the line or source reactance on drives' harmonic performance. The use of tuned L-C harmonic filters and the harmonic cancellation process when multi-pulse front ends are used as well as active front ends with multilevel converter is presented.

Chapter III presents an analysis of a high-power density asymmetric 18-pulse rectifier under abnormal input voltage conditions. It is shown how the current harmonic THD and the harmonic cancellation process are deteriorated when pre-existing voltage harmonic distortion and unbalance is present in the incoming voltage. Extensive experimental data is demonstrated to validate the theoretical analysis. In Chapter IV is introduced a solution to overcome the issues with the high-power density asymmetric 18-pulse rectifier under unbalance or voltage distortion. A reduce kVA active power filter is proposed to compensate the extra current harmonics generated during the abnormal conditions. With the objective to avoid impairing the power density of the approach, the kVA rating of the APF is specified to only 20% of the overall system power rating.

Chapter V presents an analysis of a modular converter structure to achieve high power density and high reliability for active power filters. The approached is based on interleaved parallel two-level converters with direct connection at the dc side and connection through linkage reactors at the ac side. An analysis of the reduction on the linkage reactors and impact of the interleaving approach on the dc bus capacitor is

presented as well as the generation of high frequency and low frequency zero-sequence among the converters.

Finally Chapter VI presents the general conclusions and remarks obtained from this work.

CHAPTER II

ANALYSIS OF CURRENT HARMONIC ELIMINATION SOLUTION FOR ADJUSTABLE SPEED DRIVES

2.1. Introduction

The vast proliferation of adjustable speed drives was in great part the result of the realization of significant energy savings; especially for variable torque loads (e.g. pumps, fans) where the demanded power proportional to the cube of shaft seeped. However, these benefits have been overshadowed by the well-known harmonics problems encountered with six diode front end drives. Six pulse rectifiers are a significant source of harmonics which is exacerbated by the utilization of a DC bus capacitor . The total harmonic distortion of the current in adjustable speed drives can vary from a range of 35% to more 100%, depending upon the short circuit to load current ratio (I_{sc}/I_L). For stiff or strong systems (large I_{sc}/I_L) the current harmonic distortion is higher than for weaker systems (low I_{sc}/I_L).

Numerous approaches have been investigated and commercialized over the years in order to reduce current harmonic contribution from adjustable speed drives. One of the most popular approaches, typically found in large drives, is the 12 pulse rectifier which with the help of a phase shifting transformer is able to cancel harmonic components and significantly reduce the total harmonic distortion at the input of the drive system. Other approaches such as 18-pulse rectifiers and larger number of pulses - up to 24 and 36 - are common to see for medium voltage applications.

For low voltage adjustable speed applications, the typical configuration is a six pulse front end; however, cost limitation and market response usually prohibits the utilization of more costly multi-pulse configurations, for which a specially designed phase-shifting transformer is inherently needed. Therefore, in order to resolve the harmonic problems, passive harmonic filters are available from several manufacturers. In this chapter, a review of the most common alternatives and industrial practices to reduce current harmonics pollution from adjustable speed drives is analyzed.

2.2. Harmonics on 6-pulse front end drives [23][40]

The most common front end for low voltage adjustable speed drives is the 6-pulse rectifier (Fig. 10); it is composed of six diodes switching by natural commutation; each diode having a current conduction period of 120°. It is widely preferred for its simplicity and low cost. However, it has the disadvantage of drawing large current harmonics which makes necessary the use of external harmonic mitigation methods such as passive filters.

It is well known that 6-pulse rectifiers have a distinct harmonic spectrum pattern characterized by orders $6n\pm1$, where **n** is a positive integer. (n=1, 2, 3…∞). The magnitude of each harmonic is $1/(n\pm1)$ p.u. which leads to a THD of approximately 35%. However, these magnitudes are valid only for current source rectifiers where a large inductance is connected on the dc bus providing continuous dc current. If the converter adopts a voltage source approach by connecting a capacitor in the dc bus instead, the harmonic characteristics of the rectifier will be quite different. The order of

the current harmonics will be the same than for current source rectifiers but, the magnitudes will depend on the load current to short circuit ratio (I_L/I_{sc}); the larger the load current to short-circuit current ratio I_L/I_{sc}, the lower the THD. Fig. 11 depicts the asymptotic characteristic of the THD when the I_L/I_{sc} is larger and larger. It is worth noticing that for very stiff systems (very small I_L/I_{sc}) the distortion can be so high that the THD can be larger than 100%. If the input impedance is small enough, the dc current can be even discontinuous as depicted in Fig. 12, where the typical double hump waveform is discontinuous reflecting the discontinuity in the dc current. The reason of the discontinuity is that when the input impedance is small, the capacitor is able to store enough energy, during charging time, such that it can supply the load current for some period of time (during discharging) without the need of drawing current form the ac source.
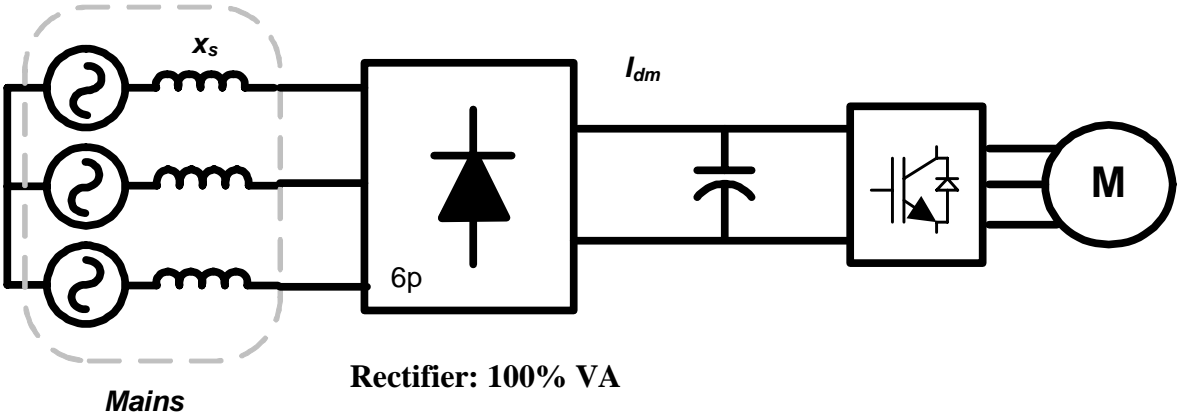
Fig. 10. Six pulse rectifier front end adjustable speed drive.

THD$_i$ versus I$_L$/I$_{sc}$ ratio
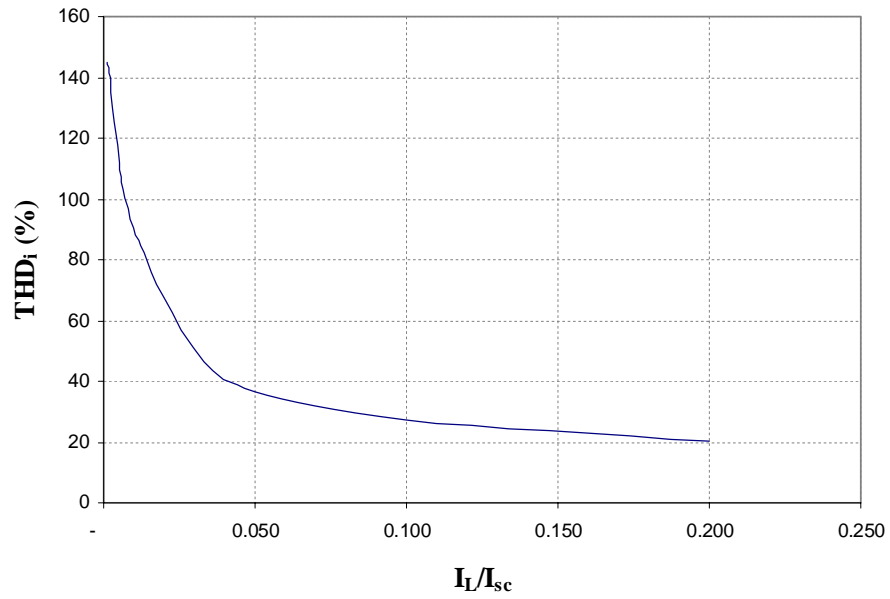
Fig. 11. Total harmonic distortion versus load current to short circuit current ratio (I$_L$/I$_{sc}$)
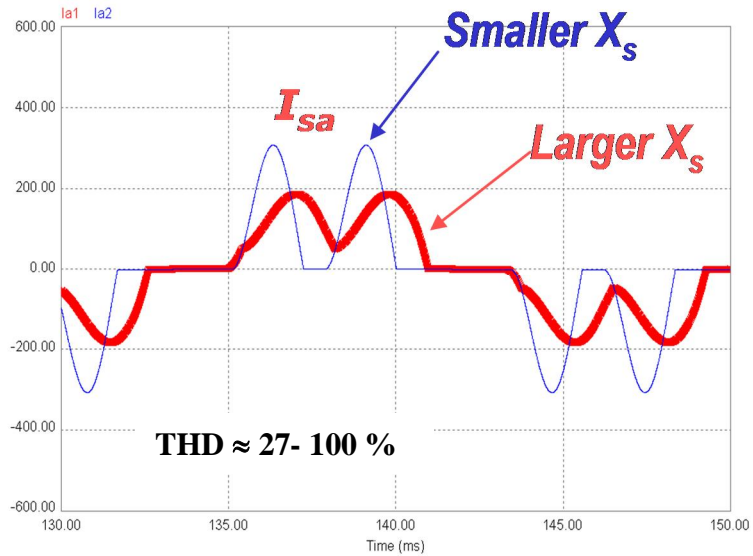
Fig. 12. Input current wave forms of voltage 6-pulse drive for large and small input impedance.

2.3. 12-pulse rectifier front end [23]

For large adjustable speed drives, a typical front-end configuration is the 12-pulse rectifier as depicted in Fig. 13. Two 6-pulse rectifiers connected in parallel at the dc side and supplied by two secondaries from a phase-shifting transformer is the standard configuration. Each three-phase set of voltages are rated at the same level with a shift phase angle of 30°. This configuration is usually done with a primary in delta connection and the two secondaries in delta and wye connection respectively. The dc side can also be connected in series, however for motor drives application it is typically found in parallel connection.
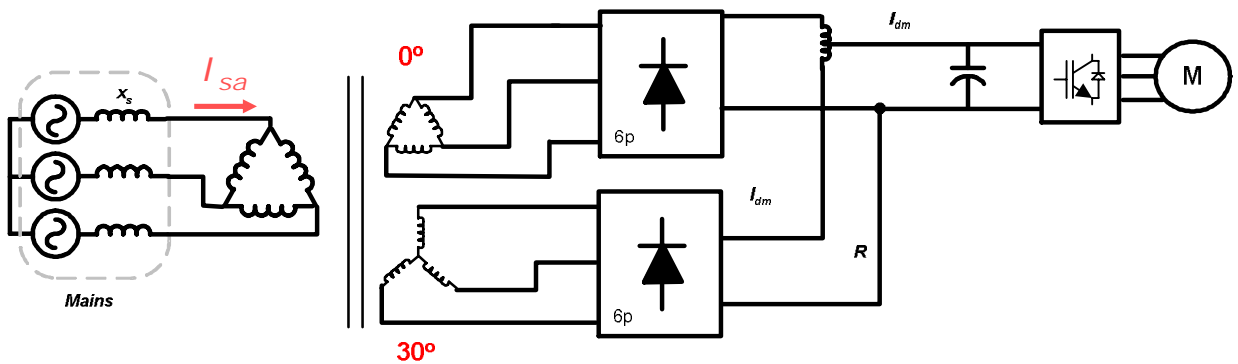
Fig. 13. 12-pulse rectifier front end adjustable speed drive.

The 12-pulse rectifier configuration can work in two different ways. If interphase reactors are connected in the dc side, each rectifier will work as a 6-pulse rectifier with current conduction of 120° and carrying half of the total dc current as shown in Fig. 14.

The rectifiers input currents will have the typical 6-pulse waveform but with a 30° shift between them (Fig. 15). The phase shift will provide the cancellation of 5th, 7th, 17th and 19th harmonics and low THD around 10-12% can be attained (Fig. 16).
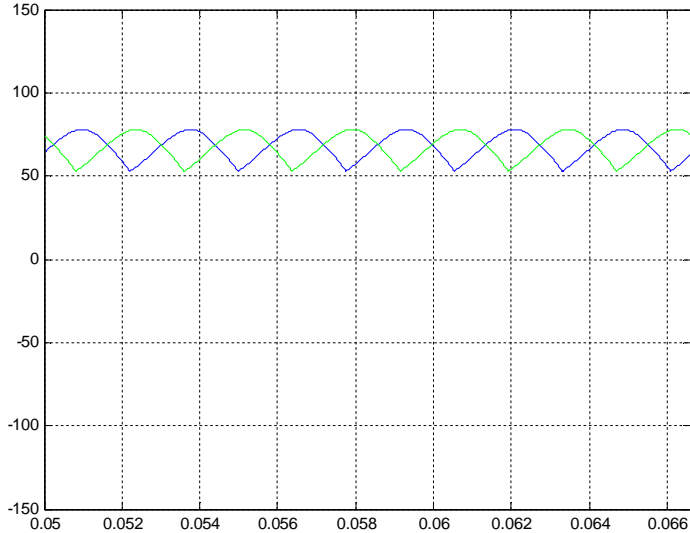
Fig. 14. 12-pulse rectifier. 6-pulse rectifier bridges dc output currents.
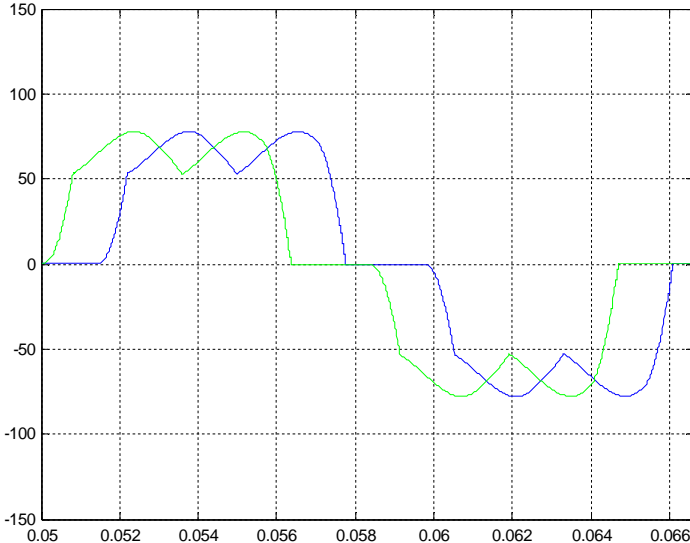
Fig. 15. Input current for bridges.
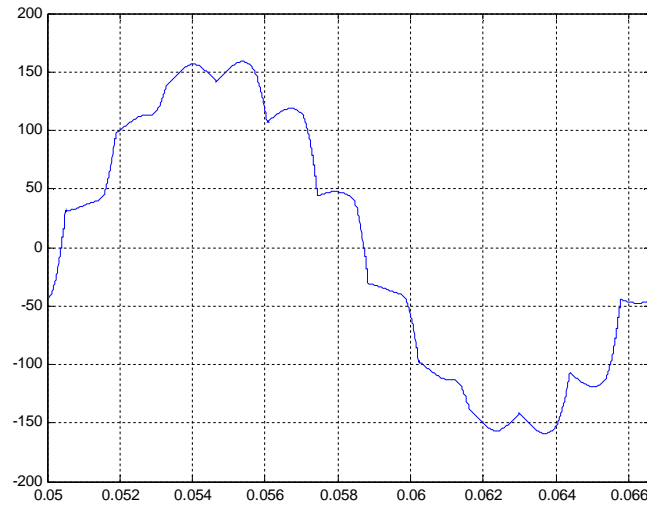
Fig. 16. 12-pulse rectifier input current waveform.

If the dc sides are directly connected, the rectifiers will work as a 6-phase rectifier. The main difference with the 12-pulse rectifier with dc interphase reactors, is the fact that the rectifier current conduction period is 30° instead of 120° and that the peak current will be as high as the total dc current. In Fig. 17, the blue and green waveforms represent the dc output currents of each rectifier.
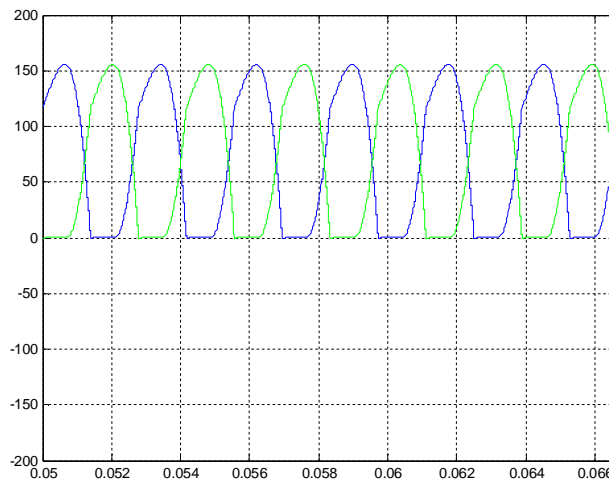
Fig. 17. Direct connected 12-pulse rectifier (bridges output currents).

The input ac current of each rectifier bridge will be two 30° pulses per half-cycle as shown in Fig. 18. Significant cancellation of 5th, 7th, 17th and 19th harmonic is also attained and reaching a THD of around 9-10% (Fig. 19).
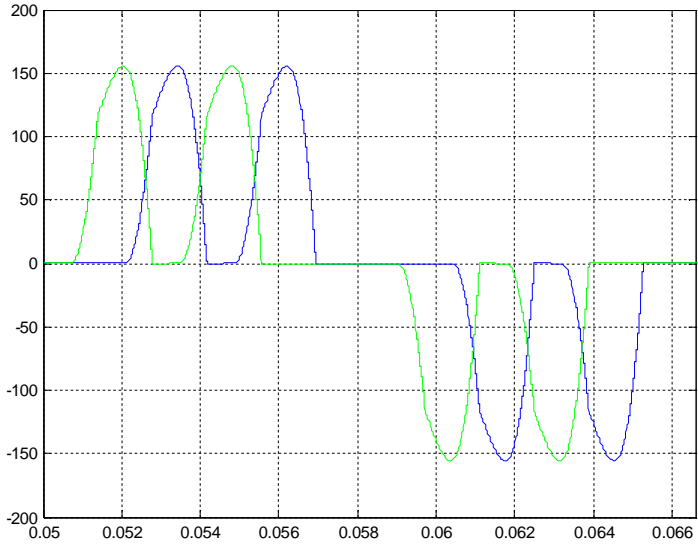
Fig. 18. Direct connection 12-pulse rectifier (bridges ac input waveforms).
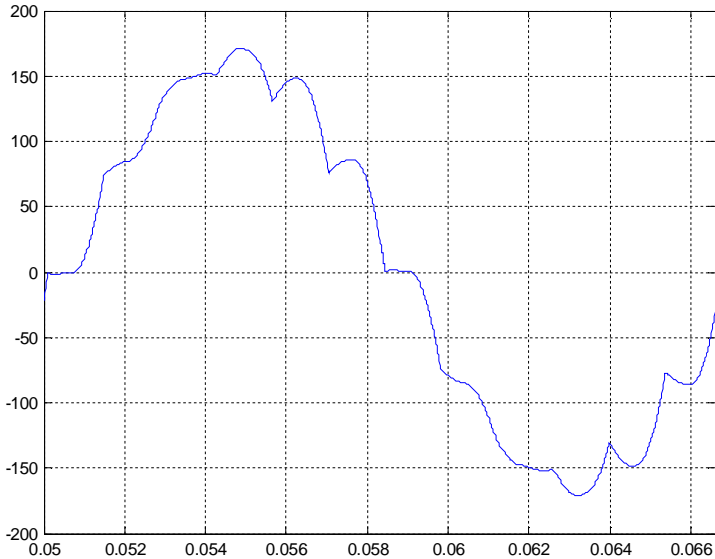
Fig. 19. 12-pulse rectifier front end drive input current.

2.4. 18-pulse rectifier front end [23]

Eighteen pulse rectifiers can be accomplished with three 6-pulse rectifier bridges (Fig. 20). The rectifier bridges must be fed from three sets of three-phase voltages. There are several ways to realize an 18-pulse rectifier. Conventional configurations consider phase shifting transformer providing three sets of three-phase voltage with phase shift angle -20°, 0 and 20°. Also, it can be accomplished by phase shifts of -40°, 0 and 40°.
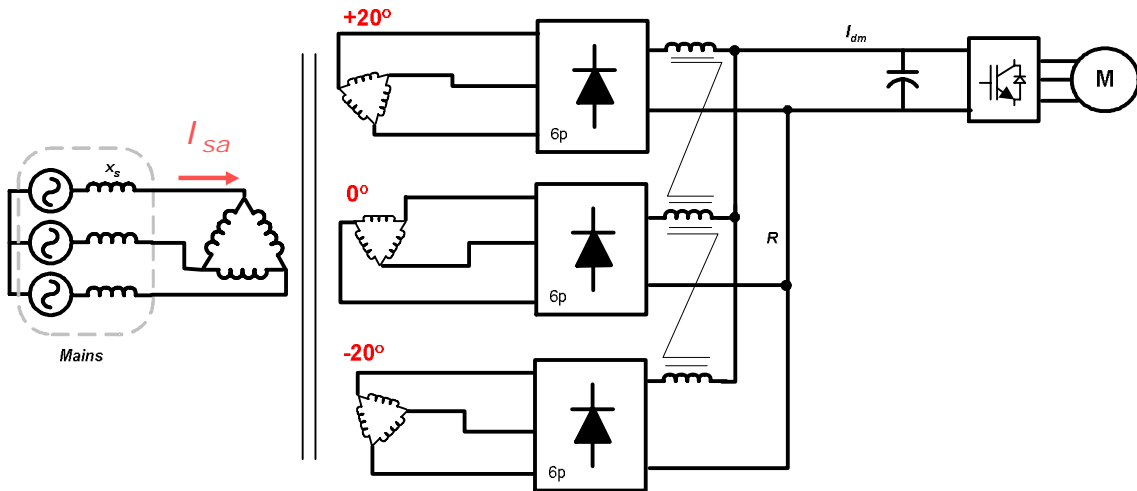
Fig. 20. 18-pulse symmetric rectifier front end adjustable speed drive. ±20° shifting transformer.

If no interphase reactors are connected in the dc bus, the conduction angle of each rectifier is 20°. Each diode will conduct for 20° twice per cycle so that the dc current will be composed of eighteen 20° wide pulses. Fig. 21 and Fig. 22 show the dc current for one cycle. The ac input current of each rectifier will be composed of two 20° pulses for each half-cycle as shown in Fig. 23 and Fig. 24, the overall input currents at the primary of the phase shifting transformer will have mainly multiple of 18n±1

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harmonics with significantly reduced THD of approximately 6-8%. It is important to mention that a 3-5% dc reactor should be used in order to smooth the dc current and avoid the occurrence of other uncharacteristic harmonics on the ac side.
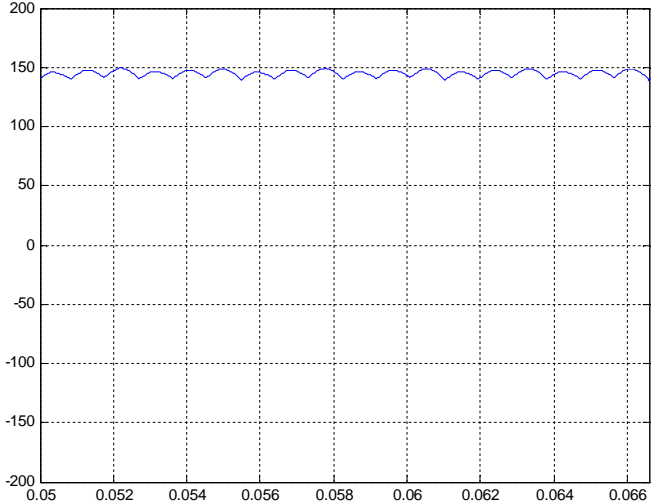
Fig. 21 18-pulse rectifier, output dc current for one 60Hz cycle.
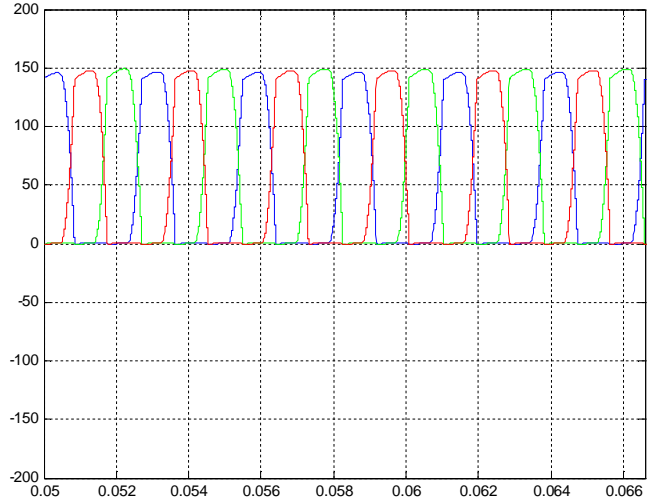
Fig. 22. 18-pulse rectifier (direct dc connection), dc output current of each bridge.
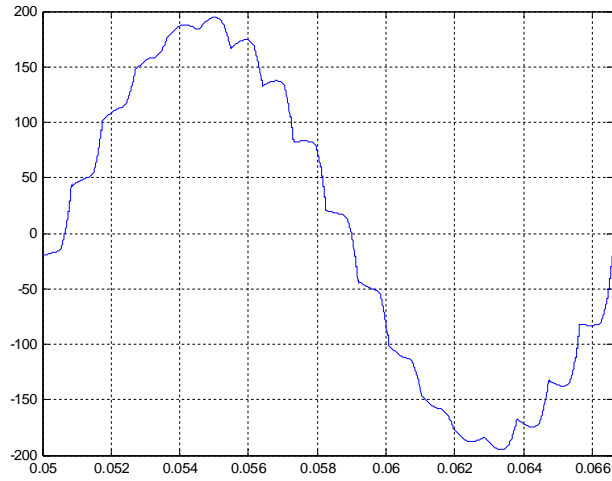
Fig. 23. 18-pulse pulse rectifier, input ac current.
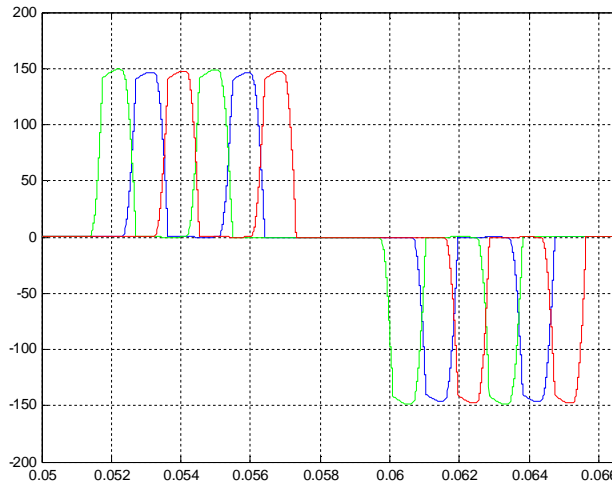
Fig. 24. 18-pulse rectifier (direct dc connection), rectifiers' ac input currents.

If interphase reactors are used, each rectifier work as an independent 6-pulse rectifier with conduction angles of 120°. The ac currents will have phase shift of 20° as shown in Fig. 25 and significant cancellation of harmonics is attained at the input. The dc currents are shown in Fig. 26. The ac current (Fig. 27) will present a harmonic pattern characterized for order 18±1 and the THD is around 6-8% as in the previous case. The

main disadvantage of this topology is that large dc interphase reactors are needed and precise impedance matching is required to guarantee current sharing among the converters.
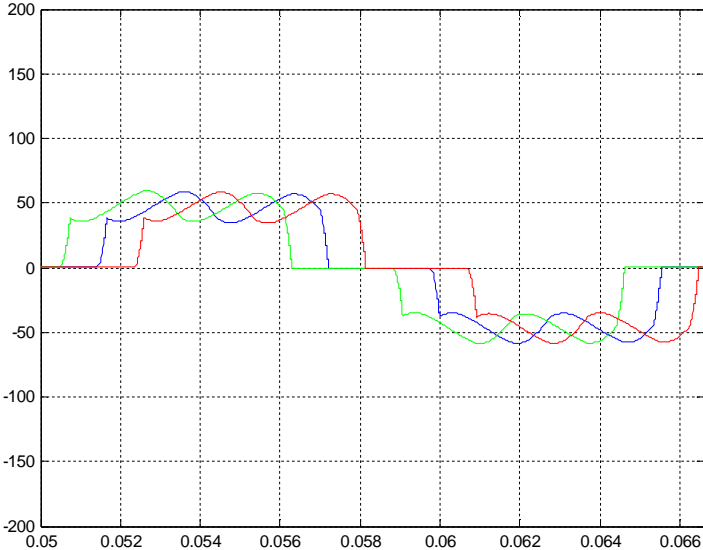
Fig. 25. 18-pulse rectifier with interphase reactor, ac input currents.
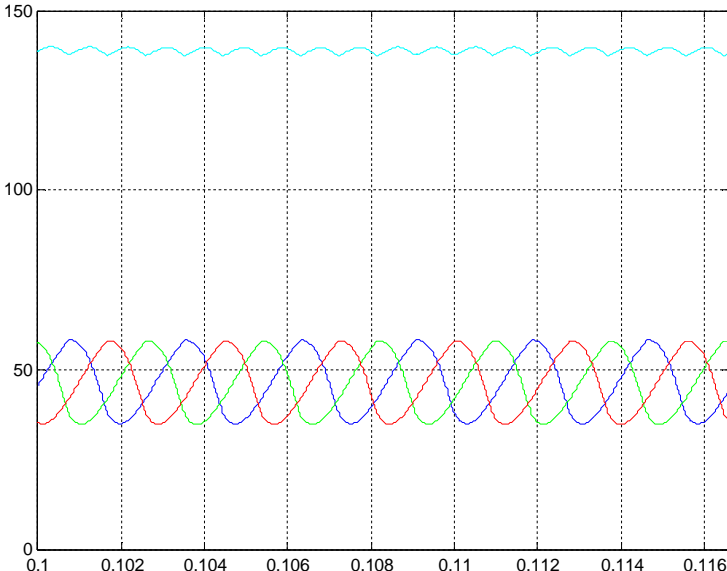
Fig. 26. 18-pulse rectifier' dc output currents (red, blue green), total dc current (light blue).
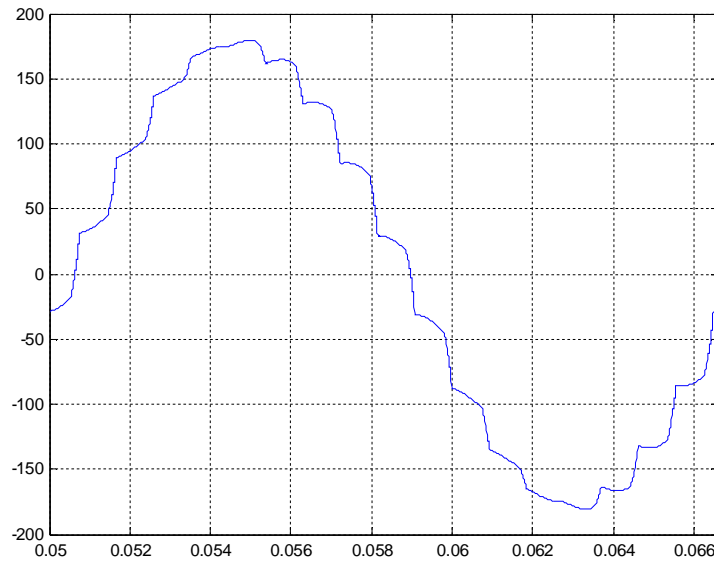
Fig. 27. 18-pulse rectifier, input ac current.

2.5. 24-pulse rectifier front end [23]

For large drives, especially for medium voltage applications, a larger number of pulses are preferred in some cases. Often rectifiers with 24 or even 36-pulses are employed. The larger power rating and lower short circuit capacity relative to the load make more justifiable the utilization of a more complex and costly topology to comply with current harmonic s standards. The disadvantage of these topologies is that a bulky line frequency multi winding transformer must be used to provide the right set of voltages to supply each rectifier.

A 24-pulse rectifier can be realized with four 6-pulse rectifier bridges which are supplied with set of voltages 15° apart.

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2.6. Multi-level front end adjustable speed drives [80]-[86]

Multilevel inverters have been investigated for almost four decades. However most of the industrial development has been made during the past fifteen years. Multiple concepts and approaches has been proposed, from the popular multilevel converter concept introduced by Nabae *et al.* in [81] "A New Neutral-Point-Clamped PWM Inverter" to the M^2LC Modular Multilevel Converter introduced by Lesnicar and Marquartd in 2002 [83], [84] and the cascaded multi-cell converter also known as "Robicon" drive which was practically introduced by Hammond in the late 90's [85], [86].

Multilevel converters consist of utilizing small voltage levels to synthesize a sine voltage waveform and perform the power conversion. This concept was patented by Dr. R. Baker more than thirty years ago [80].

The general advantages of multilevel converters include; increase converter operating voltage, good power quality (low input THD and power factor control), good electromagnetic compatibility, low switching loses, and high voltage capability. However, the main drawbacks of this approach are the large number of switching semiconductors required for lower-voltage systems and that complicated voltage control schemes are necessary to guarantee voltage balancing among the dc voltage levels. More than often, dc bus capacitors provide the voltage steps necessary to generate the different voltage levels. Among the multilevel active converters topologies (Fig. 28) it can be found:

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a) Diode clamped

b) Cascaded H-bridges

c) Flying capacitor
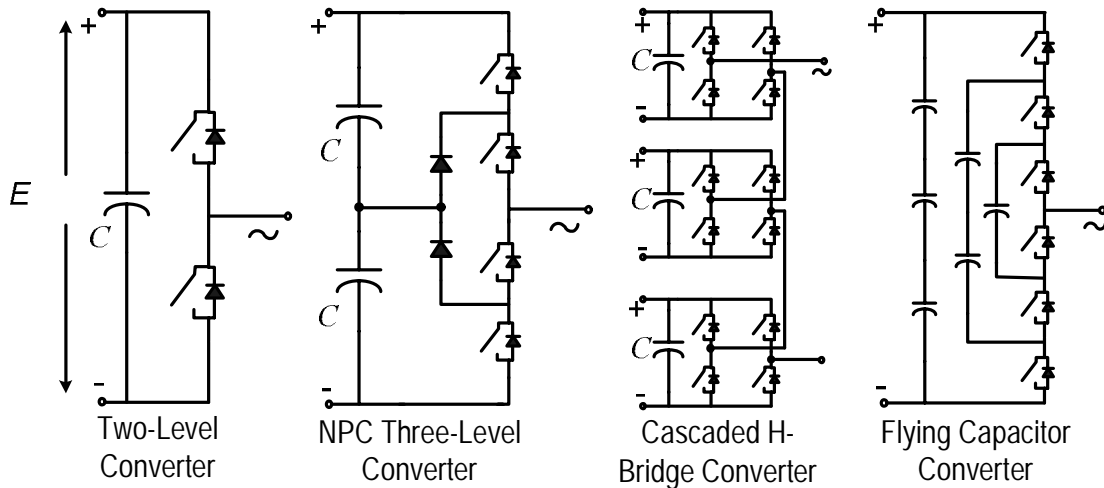
Fig. 28. Multilevel converter topologies.

Recent advances in power electronics technologies have made multilevel converters a practical industrial solution for high voltage DC transmission and high power medium voltage motor drives in multiple applications such as naval, mining & metal, water, cement and other industrial applications, with power ratings ranging from couple kilowatt at low voltage to megawatts at medium voltage. The versatility of the multilevel approach makes it suitable also for application such as active PWM rectifiers and active harmonic and reactive power compensation. PWM active front ends for motor drives can achieve low current harmonic distortion since the voltage imposed in the grid is conformed of multiple steps Fig. 29 shows a multilevel voltage waveform for

a 3-level diode clamped or NPC (Neutral Point Clamped) PWM rectifier and Fig. 30 shows the input current of the active converter. The THD achieved with these topologies fluctuated between 4 and 5%.

Even though input filters are necessary to guarantee low harmonic distortion; their size is significantly smaller than the ones utilized for 6-pulse rectifiers.
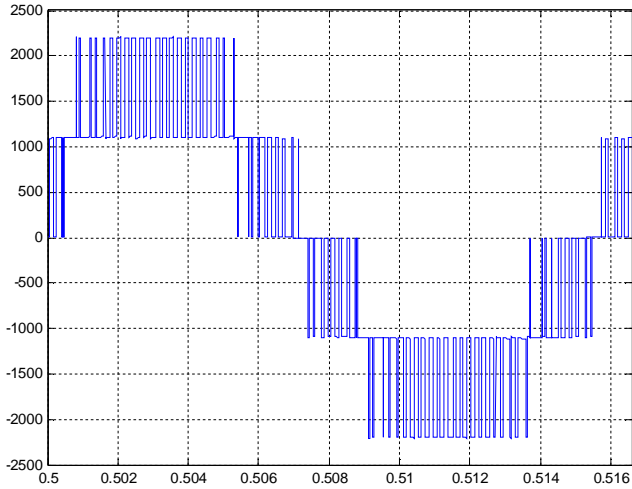
Fig. 29. NPC 3-level PWM rectifier, converter input voltage waveform.
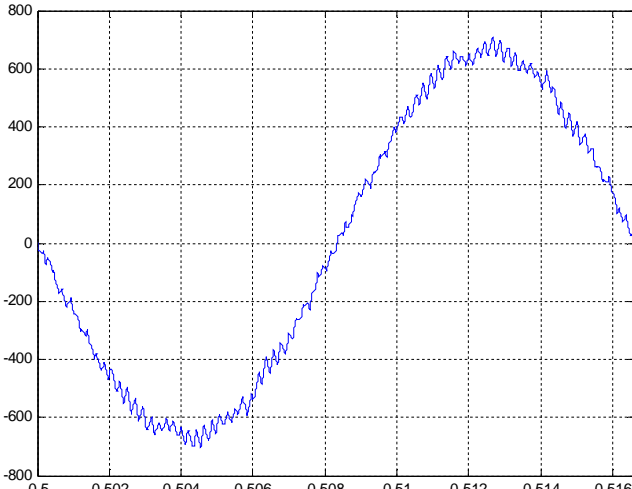
Fig. 30. NPC 3-level PWM rectifier, converter input current waveform.

2.7. Lineator (Mirus International Inc.) [102]

Several companies provide passive harmonic filters for ASDs. One in particular is Mirus International who manufactures a passive harmonic filter that is capable of reducing a wide range of harmonics along with minimizing the risk of overload and resonance.

Their approach consists on a combination of a tuned L-C filter which reactor is coupled with two additional reactors X_1 and X_2, as shown in Fig. 31. With the objective of improving the filter's performance and prevent source harmonics overloading the shunt X_{CL} branch, a reactance X_1 is connected between the source and the filtering branch. The reactance X_1 is chosen to be larger than X_{CL} so significant harmonics attenuation can be achieved. In principle this X_1 reactance would result in high voltage drop, however this topology add another reactance X_2 with opposite polarity to X_1 such that the trough-supply-to-load reactance between source and load is reduced and the voltage drop is minimized. The X_1 reactance is large enough such that it also serves for blocking the harmonics from the source side and thus prevents resonance and overloading.

The shared magnetic core for reactance X_1, X_2 and X_3 should be preferable built with at least one air-gap. The magnetic characteristics of ferrous materials are nonlinear and change significantly with load; therefore with an entire ferromagnetic core it would be very difficult to control the reactance of the filter.

Even though several drawbacks associated with passive filters are tackled with this topology, it is not guarantee the elimination of all the harmonics necessary to

comply with harmonics standards. Moreover, for lighter load there is the risk of operating with a capacitive power factor and overvoltage on the drive's input voltage. A practical solution to this problem is disconnecting the capacitor branch for this condition.
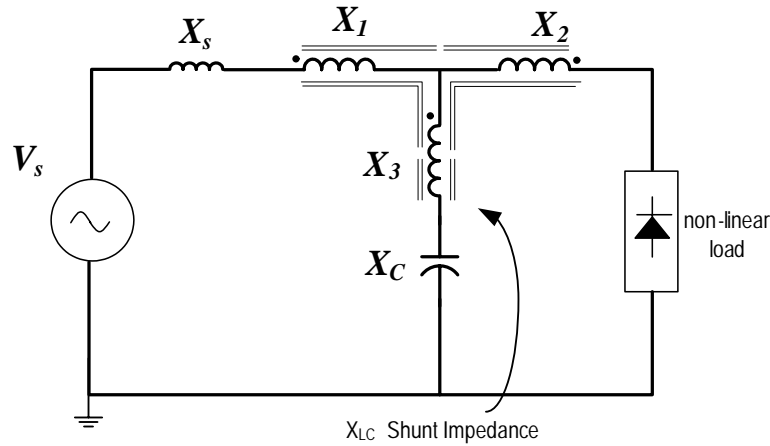
Fig. 31. MIRUS lineator harmonic filter [102].

2.8. Conclusions

A summary of the most conventional current harmonic mitigation techniques for adjustable speed drives has been presented. Most approaches rely on either passive filters or multi-pulse rectifier technology. Some new topologies deal with the associated drawbacks with passive filters and reducing the risk of resonance and overloading. However, in many cases they do not guarantee the compliance with harmonics standards. Multi-pulse rectifiers offer a good alternative for large power however bulky and complex multi-winding must be used to provide the proper voltage phase shifts.

CHAPTER III

ASYMMETRIC 18 PULSE RECTIFIER FOR ADJUSTABLE SPEED DRIVE FRONT ENDS

3.1. Introduction

Amongst the passive harmonics mitigation solutions, the 18-pulse rectifier topology seems to be the one that ensures better balance of performance ($THD_i = 6\text{-}8\%$) and cost. It provides better performance than a 12-pulse rectifier but it is less costly than a 24 or 36-pulse rectifier. An asymmetric 18-pulse autotransformer rectifier is a very attractive solution since it enables the reduction of both rectifier and input shifting transformer kVA rating. These types of topologies have been introduced conceptually by Kamath [32] and commercially by Toshiba Corporation [34].

Even though significant harmonic reduction and other benefits can be achieved with these topologies, some drawbacks are observed on the presence of voltage unbalanced and pre-existent voltage harmonic. Moreover, when a large capacitor is connected in the dc-side of the rectifier, as in motor drives, the performance of the 18-pulse rectifier can be deteriorated. The performance also depends on the short-circuit current to load ratio.

3.2. Asymmetric 18 pulse rectifier

An asymmetric 18-pulse rectifier can be employed to achieve substantive harmonic cancellation [32], 146[33]. The asymmetric 18-pusle rectifier is realized with three 6-pulse rectifiers (Fig. 32) in a similar fashion than conventional symmetric 18-pulse rectifiers as describe in Chapter 2, however, there are some distinctive and crucial differences. The three set of voltages and rectifiers' kVA rating are not symmetric, as oppose symmetric 18-pulse rectifiers where each rectifier must handle 33% of the total converter kVA. In addition, an autotransformer is used to provide the proper voltages. A main rectifier is directly connected to the utility and it needs to be design to handle 66.67% of the total converter kVA. Moreover, two auxiliary rectifiers are connected to the secondaries of the especially designed autotransformer and are rated for 16.67% of the total kVA. Therefore, the autotransformer kVA rating is only 33% of the ASD. This constitutes one of the main advantages of this topology since higher power density can be achieved.
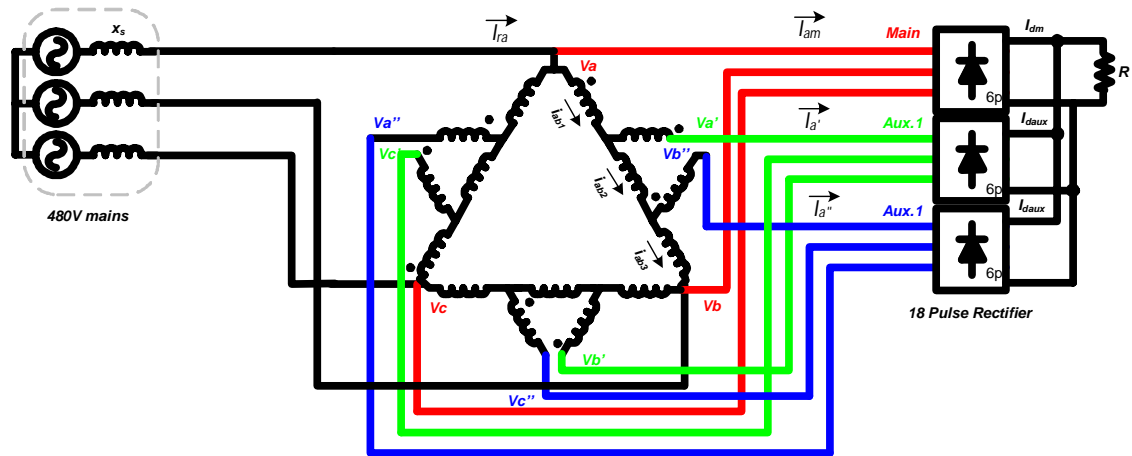
Fig. 32. Asymmetric 18-pulse rectifier with resistive load [32].

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The voltage rating for the main rectifier is 1 p.u., however the voltage for the auxiliary rectifier is 0.767 p.u. with a phase shifting angle of $\pm 37°$ respect to the mains. These particular set of voltages are obtained from the fact that one set of conditions to obtain 18-pulse rectification relies on the following [32]:

a) Three sets of balanced 3-$\varnothing$ *line* (phase-to-phase) voltage sources should be generated where two of the sets are phase displaced $\pm 20°$ with respect to the third voltage set.

b) The amplitude of these line voltages should be equal to each other.

These three set of voltages can be realized by establishing auxiliary *phase* voltage sources such that the phase-to-phase voltages respect to the mains yields the desired voltage magnitude and $\pm 20°$ phase shift. Fig. 33 shows a phasor diagram of three particular sets of three phase phase-voltages necessary to create the aforementioned requirements for 18-pulse rectification.
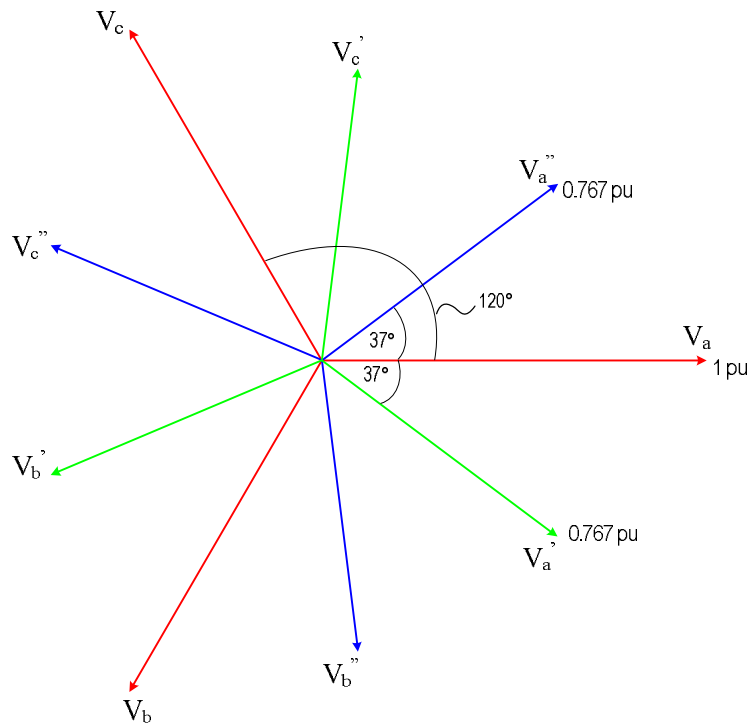
Fig. 33. Phasor diagram of the asymmetric 18-pulse rectifier.

Fig. 34 shows the phasor diagram of the resulting phase-to-phase voltages constructed from the asymmetric set of phase voltages of Fig. 33. These voltages are constructed It is interesting to observe that the asymmetric phase voltages yield to symmetric set of voltages with ±20° phase shift and of equal magnitude.
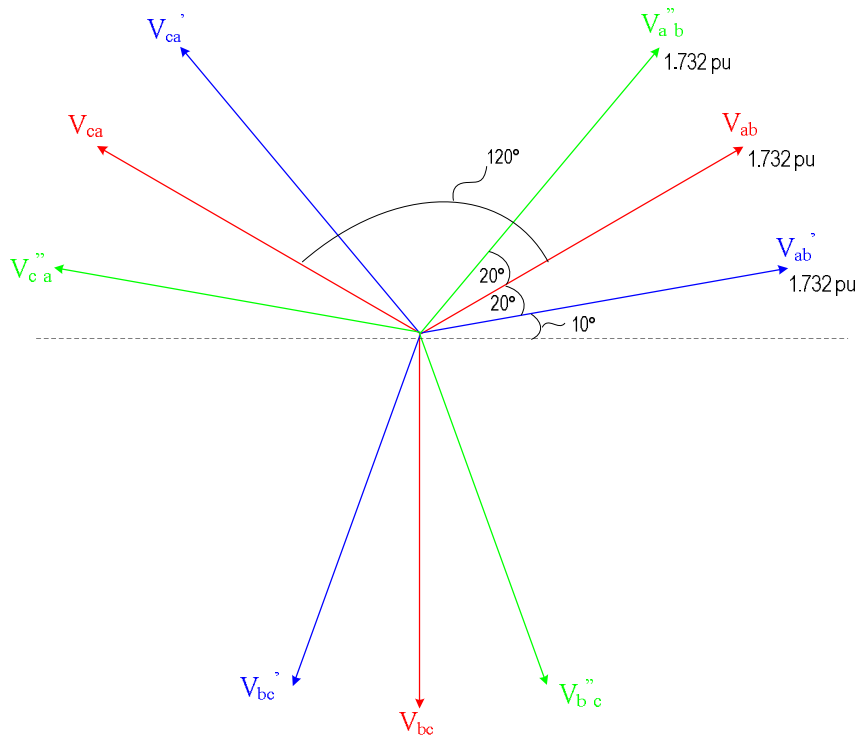
Fig. 34. Phasor diagram of voltage requires for 18-pulse rectification.

The vector diagram of Fig. 34 is obtained from equations (1) to (9)

$$V_{ab} = V_a - V_b \tag{1}$$
$$V_{bc} = V_b - V_c \tag{2}$$
$$V_{CA} = V_C - V_A \tag{3}$$

$$V_{ab}' = V_a' - V_b' \tag{4}$$
$$V_{bc}' = V_b' - V_c' \tag{5}$$
$$V_{CA}' = V_C' - V_A' \tag{6}$$

$$V_{a\,b}'' = V_a'' - V_b \tag{7}$$
$$V_{b\,c}'' = V_b'' - V_c \tag{8}$$
$$V_{C\,A}'' = V_C'' - V_A \tag{9}$$

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The autotransformer can be constructed with three windings per phase; one main primary winding and two auxiliary secondary windings as shown in Fig. 35. The main primary winding will hold the whole phase-to-phase voltage and it will have two taps. The taps will split the winding in three sections, a central section with turn ratio (respect to the main primary) of k1 and two symmetric sections with turn ratio of k2. The two auxiliary secondary windings will have a turn ratio k3.
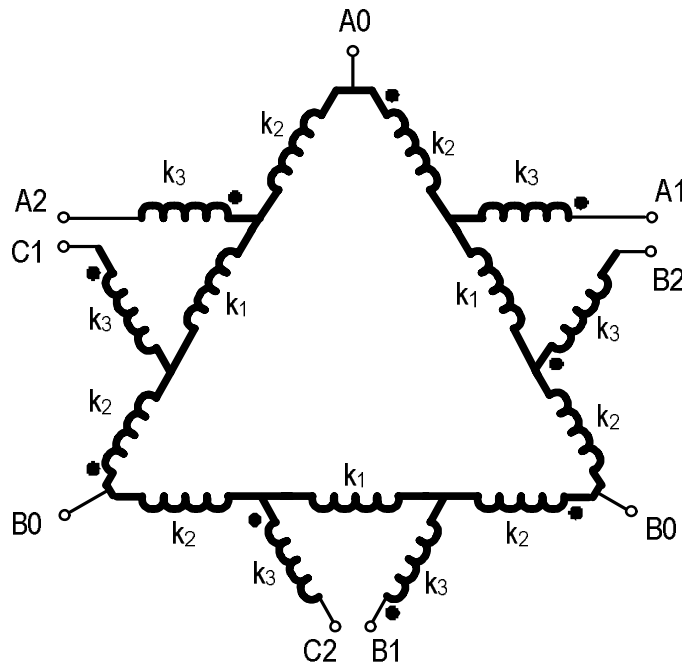
Fig. 35. Autotransformer for asymmetric 18-p rectifier [32].

Notice that it is required the following constrain.

$$k_1 + 2\,k_2 = 1$$

The values of the turn ratios are approximately:

$$k_1 = 0.482,\ k_2 = 0.253,\ k_3 = 0.135$$

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The set of three-phase balanced voltages enable the 18-pulse rectification and harmonic cancellation, however the conduction angles of each three phase diode bridge are different from conventional 18-pulse symmetric configurations. Each diode of the two auxiliary rectifiers conducts for a period of only 20° and carry full dc load current. Conversely, each diode of the main rectifier conducts for a period of 80° completing the total 120° conduction period. This results in a kVA rating for the auxiliary and main rectifiers of:

$$KVA\ \textbf{(}Auxiliary\ Rectifier\textbf{)}\ in\ p.u. = \frac{20°}{120°} = \frac{1}{6} \tag{10}$$

$$KVA\ \textbf{(}Main\ Rectifier\textbf{)} in\ p.u. = \frac{80°}{120°} = \frac{2}{3} \tag{11}$$

Consequently, the kVA rating of the autotransformer corresponds to the power drawn by the auxiliary rectifiers which leads to a total 33.3 % or $\frac{1}{3}\ p.u.$ The low kVA rating necessary to construct the autotransformer constitutes the main advantage of this topology.

A derivation of the rectifier's input current I_{as} can be obtained from Fig. 36 by resolving current Kirchhoff's law at node A0 and transformer's current relationships.
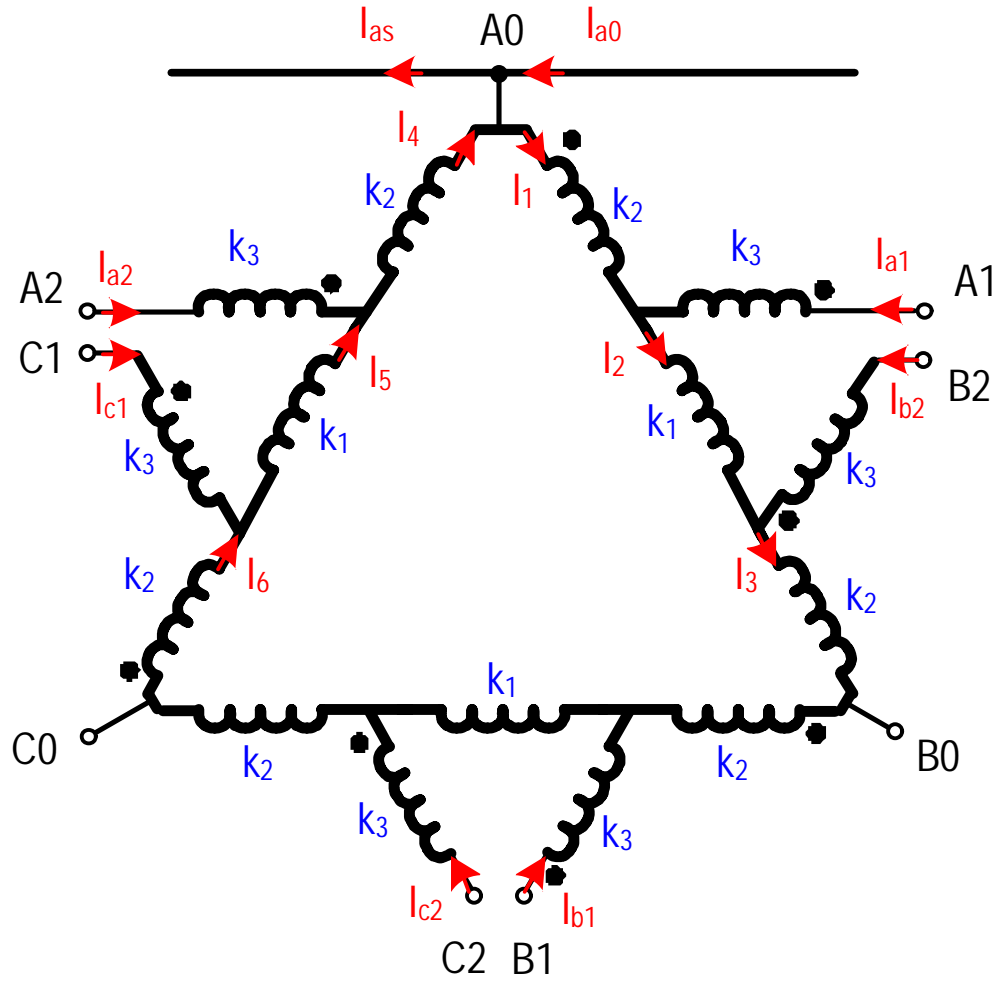
Fig. 36. 18-pulse autotransformer and currents flow detail [32] .

From current Kirchhoff's law:

$$I_{as} = I_{a0} + I_4 - I_1 \tag{12}$$

$$I_1 = I_2 - I_{a1} \tag{13}$$

$$I_2 = I_3 - I_{b2} \tag{14}$$

I_3 can be calculated by the induced currents of all windings of A_0B_0,

$$I_3 = -\frac{k3}{k2}I_{c1} + \frac{k3}{k2}I_{c2} - \frac{k1}{k2}I_2 - I_1 \tag{15}$$

$$I_3 = I_1 + I_{a1} + I_{b2} \tag{16}$$

Equating (15) and (16),

$$-\frac{k3}{k2}I_{c1} + \frac{k3}{k2}I_{c2} - \frac{k1}{k2}(I_1 + I_{a1}) = 2I_1 + I_{a1} + I_{b2} \tag{17}$$

Multiplying by k_2 and grouping terms:

$$(2k_2 + k_1)I_1 = -k_3 I_{c1} + k_3 I_{c2} - k_1 I_{a1} - k_2 I_{a1} - k_2 I_{b2} \tag{18}$$

$$I_1 = \frac{-k_3 I_{c1} + k_3 I_{c2} - (k_1 + k_2)I_{a1} - k_2 I_{b2}}{(2k_2 + k_1)} \tag{19}$$

On the other hand,

$$I_4 = I_{a2} - I_5 \tag{20}$$

$$I_5 = I_{c1} - I_6 \tag{21}$$

I_6 can be calculated by the induced currents of all windings of $C_0 A_0$,

$$I_6 = -\frac{k3}{k2}I_{b1} + \frac{k3}{k2}I_{b2} - \frac{k1}{k2}I_5 - I_4 \tag{22}$$

$$I_6 = I_4 - I_{a2} - I_{c1} \tag{23}$$

Equating (22) and (23),

$$-\frac{k3}{k2}I_{b1} + \frac{k3}{k2}I_{b2} - \frac{k1}{k2}(I_4 + I_{a2}) = 2I_4 - I_{a2} - I_{c1} \tag{24}$$

Multiplying by k_2 and grouping terms:

$$(2k_2 + k_1)I_4 = -k_3 I_{b1} + k_3 I_{b2} + k_1 I_{a2} + k_2 I_{a2} + k_2 I_{c1} \tag{25}$$

$$I_4 = \frac{-k_3 I_{b1} + k_3 I_{b2} + (k_1 + k_2) I_{a2} + k_2 I_{c1}}{(2k_2 + k_1)} \tag{26}$$

$$I_{as} = I_{a0} + \frac{(k_1 + k_2) I_{a1} + (k_1 + k_2) I_{a2} - k_3 I_{b1} + (k_2 + k_3) I_{b2} + (k_2 + k_3) I_{c1} - k_3 I_{c2}}{(2k_2 + k_1)}$$

$$\tag{27}$$

Where the currents I_{a0}, I_{a1}, I_{a2}, I_{b0}, I_{b1}, I_{b2}, I_{c0}, I_{c1}, I_{c2} have the shape as shown in Fig. 37a. By applying equation (27) it is possible to obtain the 18-pulse waveform I_{as} depicted on Fig. 37b. With k_1=0.482, k_2=0.253, k_3=0.135.

x = a, b, c
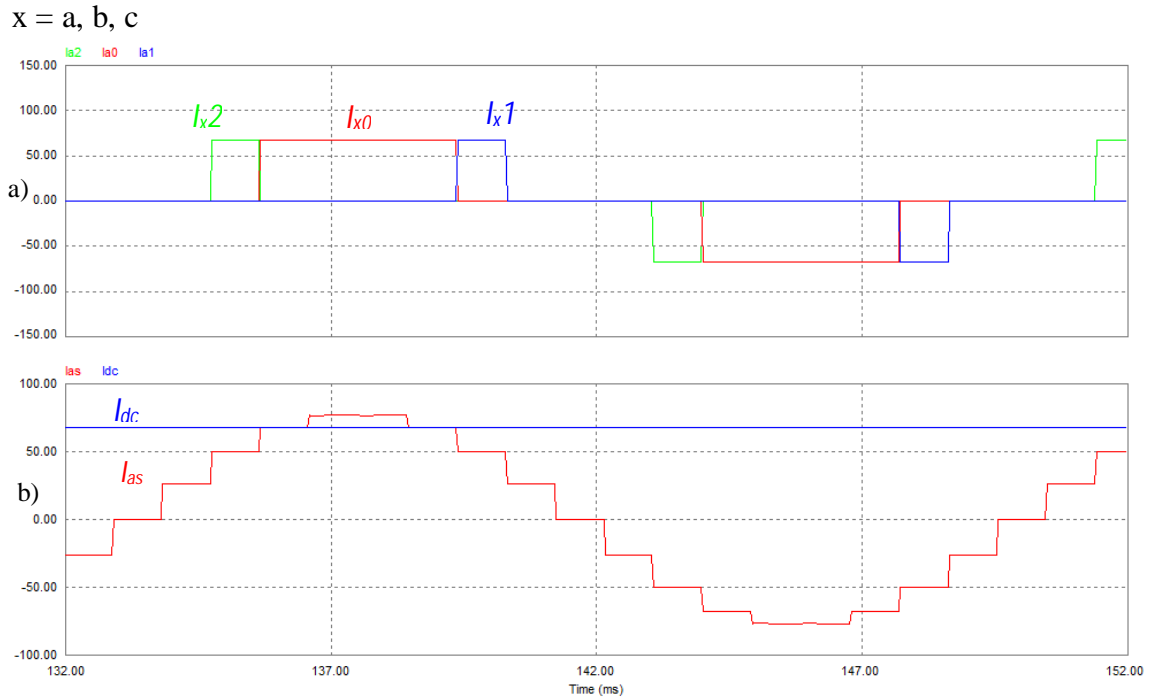
Fig. 37. a) Main and auxiliary rectifiers' current, b) output dc I_{dc} current and overall input current I_{as}.

Fig. 38 shows simulation results of the asymmetric 18-pulse rectifier corresponding to a 480 V system and 42.5 kW. It is possible to distinguish the conduction angles for the main and auxiliary rectifiers. The input current waveform is remarkable similar to the conventional symmetric 18-pulse rectifiers and its total harmonic distortion (THD) index is ~7.5 %.
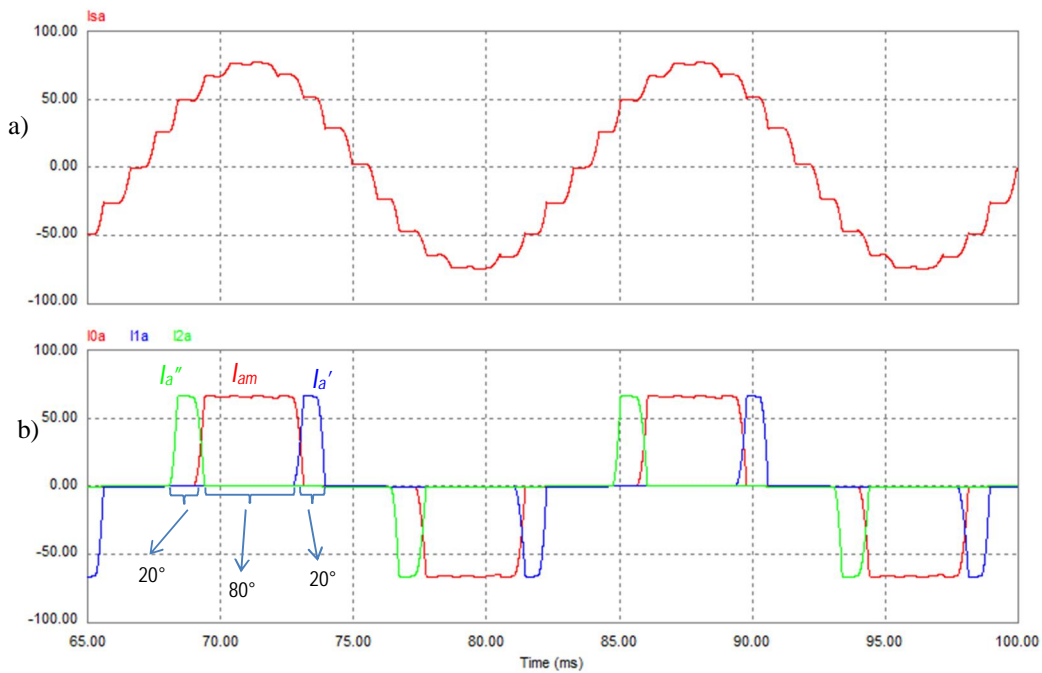
Fig. 38. a) 18-pulse rectifier input current I_{ra}, b) diode bridges currents I_{am}, I_a', I_a''.

The effectiveness of the rectifier to achieve an optimal current cancellation hinges on its ability to maintain the balance on their bridges' current conduction times. Since the auxiliary rectifiers conduct for a short period of time, small disturbances and impedance mismatch can impair the ability to an adequate current cancellation and low current distortion.

It is recommended to use a balancing reactor in order to guarantee symmetric conduction angles for the auxiliary rectifiers. Fig. 39 shows the additional balancing reactor on the main rectifier current path. The current THDi will be affected by the value of the balancing reactor (or matching impedance).
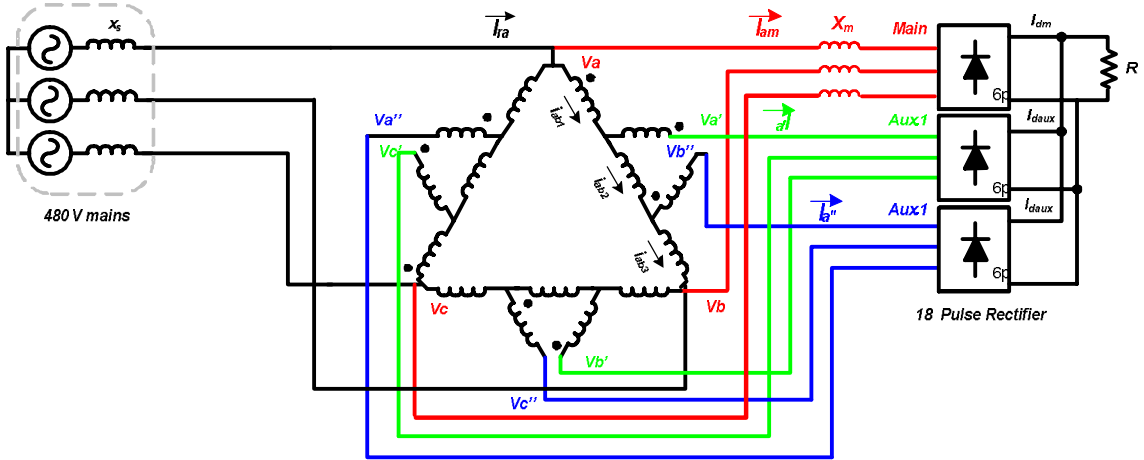
Fig. 39. Asymmetric 18-pusle rectifier with balancing reactor X_m.

Fig. 40 shows the input current THDi for different values of balancing reactor X_m. It can be seen that there is a sweet spot where the THDi is minimum. This value is similar to the transformer leakage impedance feeding the auxiliary rectifiers.
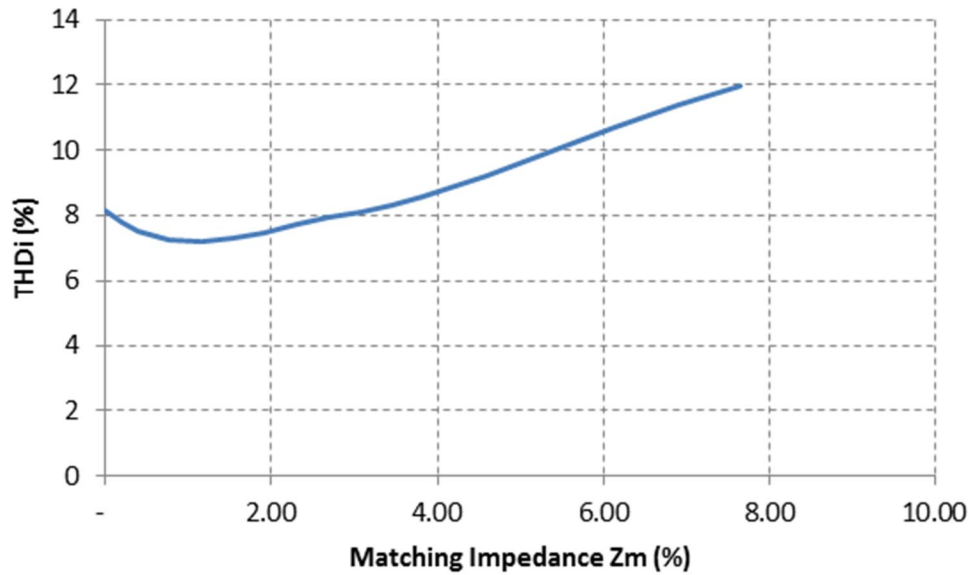
Fig. 40. Asymmetric 18-p rectifier input THDi vs. matching impedance Z_m (%).

3.3. Analysis of asymmetric 18 pulse rectifier's performance under utility voltage disturbances

Under clean power supply conditions, the input current THD of a conventional 18-pulse rectifier is low as expected, if only if, the dc current ripple is kept low. Usually, motor drives employ a combination of dc link reactor and a large capacitor to keep stiff dc bus voltage and to avoid uncharacteristic harmonics in the motor current. In some cases, Dc link current ripple might be quite significant and input current THD larger than expected.

The input current THD_i increases when the relationship between the dc output current and the available short circuit current of the utility line (I_d/I_{sc}) decreases. In other words, for lighter loads or stronger utility systems the harmonics mitigation performance is impaired. Fig. 41 shows the behavior of the asymmetric 18-pulse rectifier input THDi

for different I_d/I_{sc} rates. Even though some deterioration of the THD is observed, it is not significant taking into account the less stringent requirements imposed by IEEE 519 when the short circuit (I_{sc}) to load current (I_d) increases (or I_d/I_{sc} decreases).

% THD
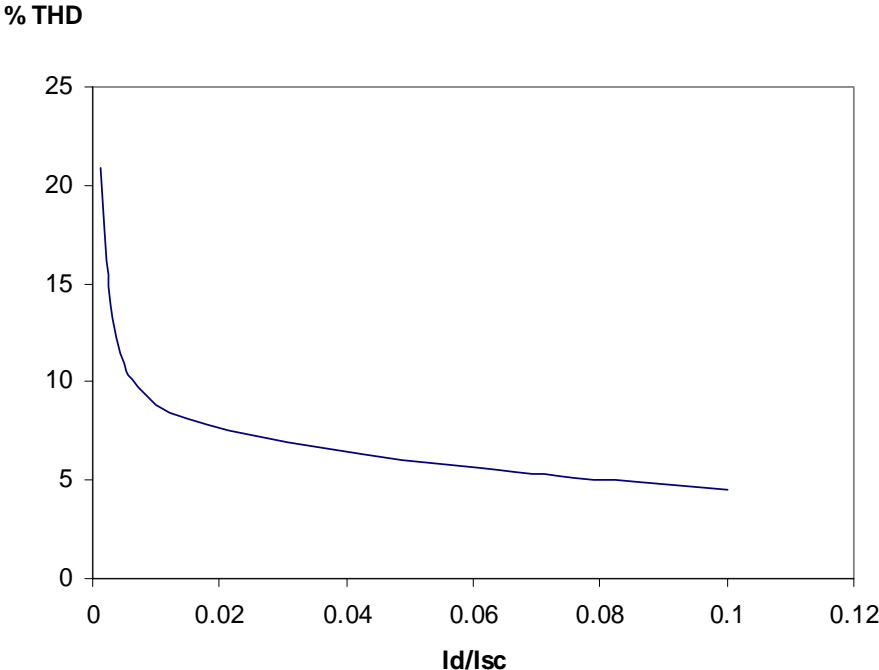
Fig. 41. Asymmetric 18-pulse rectifier input THD_i vs. I_d/I_{sc} ratio.
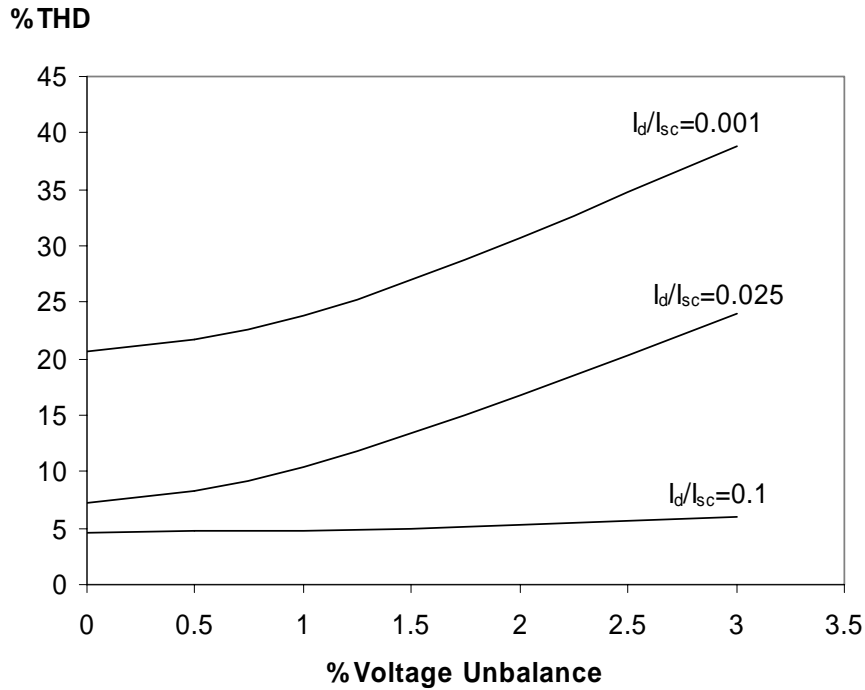
Fig. 42. Asymmetric 18-p rectifier THD_i vs. % voltage unbalance for different I_d/I_{sc} rates.

Similarly, the THD_i is further affected when the utility line suffers voltage unbalance or voltage harmonic distortion. It is not uncommon to measure 1% to 3% voltage unbalance and/or 2.5% to 5% pre-existing 5th and 7th harmonic voltage distortion. Fig. 42 shows how the THDi changes with voltage unbalance between 0 and 3%, for several I_d/I_{sc} rates. Analysis of the performance of the asymmetric 18-pulse rectifier (Fig. 43) is presented which was validated by extensive experimental data.

On the other hand, small unbalance or harmonic distortion in the three phase input supply will significantly deteriorate the input THD. Current sharing is affected and non-characteristics harmonics circulates between the bridges. Typically 3rd and 5th might be present in the input current harmonic content under this condition. An asymmetric 18-pulse rectifier is affected in the same manner.
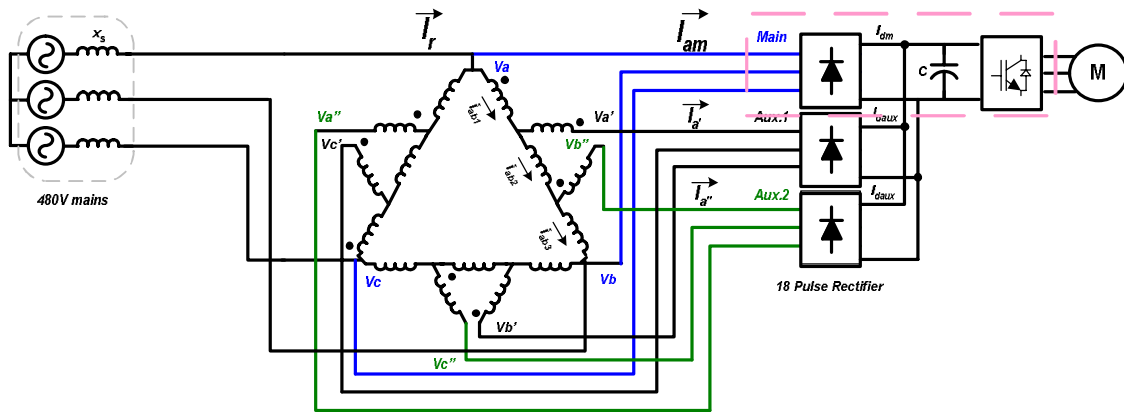
Fig. 43. Asymmetric autotransformer 18 pulse rectifier adjustable speed drive.

Fig. 44 to Fig. 47 show some experimental data taken for several input supply conditions. Fig. 44 shows the 18-pulse rectifier's input current for ideal voltage source conditions. Fig. 44.a shows the input current when the load is pure resistive rendering a THD of 6.5%. Conversely, Fig. 44.b shows input current for the same voltage source conditions however in this case the load corresponds to a motor drive, where a capacitor is connected in the DC bus. The THD in this case is significantly higher rendering a 13%.
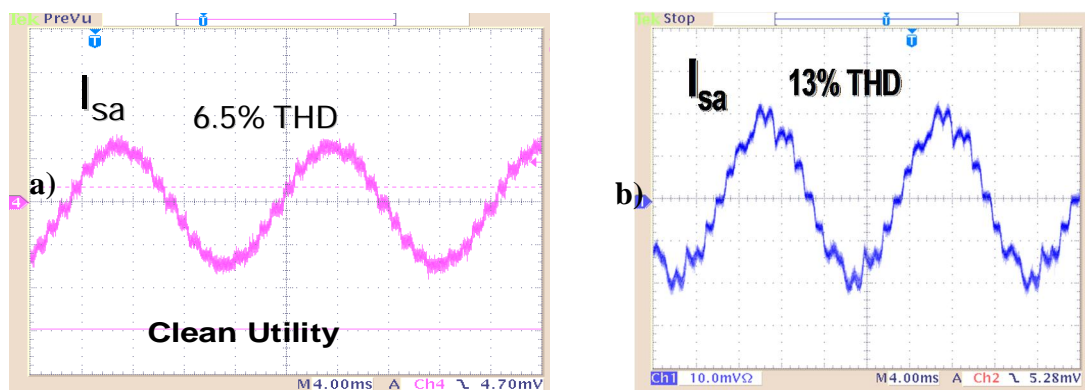
Fig. 44. 18p rectifier input current under clean power supply. a) only resistive load in dc bus b) LC filter in dc bus.

Fig. 45 shows in more detail the input current for each rectifier bridge for the sane voltage conditions. Fig. 45.c and Fig. 45.a show the input current for auxiliary rectifiers 1 and 2 respectively. Fig. 45.b shows the input current for the main rectifier and Fig. 45.d shows the overall input current.

Fig. 46 shows the rectifiers input current for some abnormal voltage conditions. A three-phase programmable power supply 47-66Hz/135-270V/63kVA California Instruments FCS Series was employed. Fig. 46.a shows the rectifier's current when the voltage source experiences a 1% voltage unbalanced. The THD is measured to be 14%. Likewise, for 2% input voltage unbalanced condition the THD is 19% (Fig. 46.b) and for 3% unbalance the THD is found to be 27% (Fig. 46.c). Similar results are encountered while voltage harmonic distortion is present in the input supply. This data was collected for a 60% load. It is expected to achieve better performance for full load.
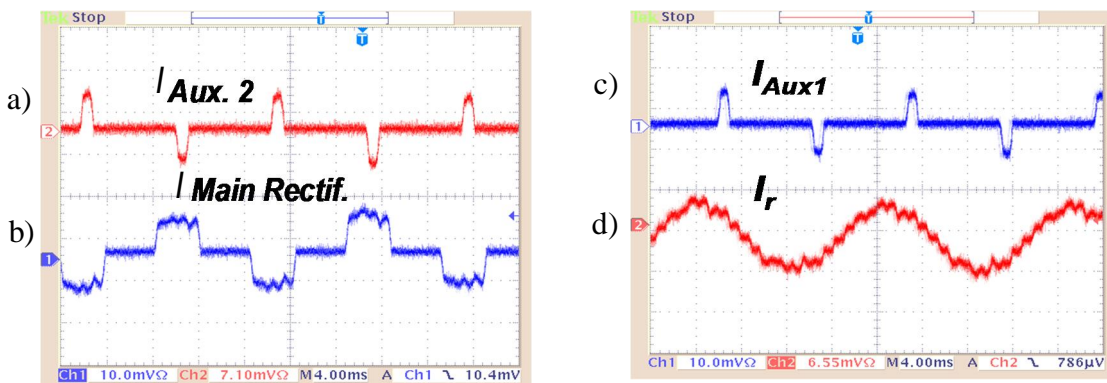
Fig. 45. 18p rectifier currents under clean power supply. a) current |auxiliary rectifier-2. b) main rectifier's current c) current auxiliary rectifier-1 d) overall rectifier's input current
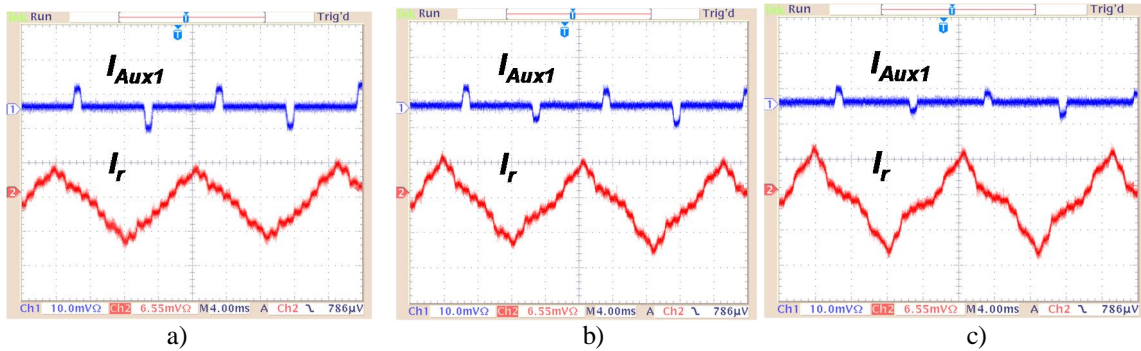
Fig. 46. a) 18 pulse rectifier current under 1% input unbalance: auxiliary rectifier input current (blue) and rectifier's input current (red), b) 18 pulse rectifier current under 2% input unbalance: auxiliary rectifier input current (blue) and rectifier's input current (red), c) 18 pulse rectifier current under 3% input unbalance: auxiliary rectifier input current (blue) and rectifier's input current (red).

In summary, asymmetric autotransformer 18-pulse rectifiers subjected to realistic utility conditions can behave far from ideal. Fig. 47 shows a summary of rectifier's performance under several utility and load conditions.
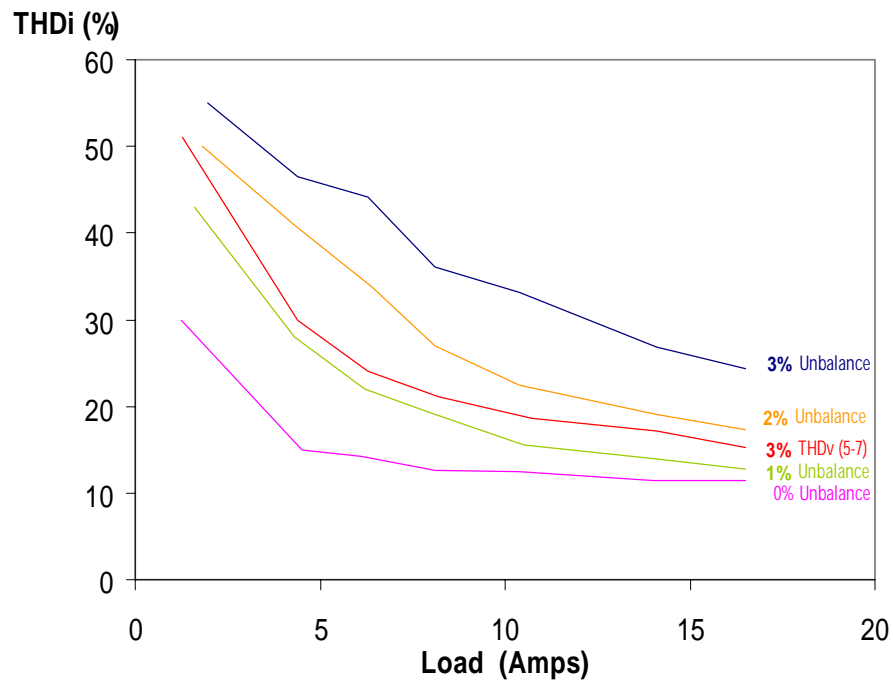
Fig. 47. Experimental results showing asymmetric 18-pulse rectifier performance for several input voltage conditions [37].

3.4. Conclusions

Even though 18-pulse rectifiers present a viable, technically and cost effective, solution for harmonic cancellation, their performance may be critically susceptible to voltage disturbances, such as unbalance and voltage distortion. These conditions might be often found on typical industrial facilities, impairing the rectifier from achieving low harmonic content.

Moreover, the input transformer can be costly and undesirably bulky. An asymmetric 18-pusle rectifier can improve the power density of the 18-pulse rectifier approach by reducing the size of the input auto-transformer; however special attention must be put into the sensibility of the rectifiers to non-ideal voltage conditions.

CHAPTER IV

AN ACTIVE HARMONIC FILTER FOR AN ASYMMETRIC 18-PULSE RECTIFIER FRONT END ADJUSTABLE SPEED DRIVE *

4.1. Introduction

Numerous researches have been conducted in order to minimize the input current distortion in adjustable speed drives. Years of investigation have resulted in passive and active solutions. Active approaches typically use high frequency controllable PWM rectifiers, which significantly decrease the input current harmonic distortion (THD_i = 4-5%). Nevertheless, the introduction of high frequency hard-commutated power electronics devices in the AC/DC conversion process results in poorer reliability compared with traditional diode rectifiers. The rectification process relies on a sophisticated PWM technology and on a suitable control strategy, which makes the rectifier more vulnerable to fail, due to the large number of components. Moreover, active rectifier cannot achieve very high efficiency due to switching frequency losses and losses associated to the required input filter. Since they feature high part count and circuit complexity, its cost is significantly high compared with passive alternatives. On the other hand, even though passive rectifier and controlled rectifiers are affected y these drawbacks to a much lesser extent they suffer of poor input power quality.

The input current THD is high and highly dependent on the converter's input impedance.

In this chapter, an alternative to traditional rectification methods in order to achieve high input power quality and high reliability without trading down converter efficiency is proposed. The approach is based on a combination of an asymmetric 18-pulse front-end rectifier as described in chapter III and a fractionally rated active power filter used to reduce the input current distortion in adjustable speed drives. The 18-pulse rectifier is used in the ac/dc conversion process and reduces the overall input current THD. Further reduction in the current THD is accomplished by using the reduced KVA active power filter (APF). The APF is capable of providing the 18-pulse rectifier with high performance over a wide spectrum of load and system's conditions.

An asymmetric 18-pulse autotransformer rectifier is utilized in order to reduce the kVA rating of the input shifting transformer and rectifier, with a topology similar to the one described in [32]. This in turn, contributes to improve the overall efficiency of the approach.

Although the performance of multi-pulse rectifiers can be improved by mean the implementation of line reactors, harmonic blocking reactors or even some type of harmonic trap [35], [102], the input current THD improvements are limited, hard to predict, and also, higher losses will be expected since usually large inductors are needed. Furthermore, the ever increasing cost of copper and iron, and the significant cost reductions in both power semiconductor devices and signal processors, make silicon

based active approaches more attractive when high performance and low footprint are desired.

The fact that the active filter is responsible for just small portion of the current harmonic reduction allows for a VA rating of only 20% of the total ASD volt amperage. This strategy improves the reliability of the whole approach, because the ac/dc conversion is performed by using a robust uncontrolled 18-pulse rectifier technology. Moreover, high efficiency can be achieved due to the reduced size of the APF. The approach also has the characteristic of maintaining a balance of performance, cost and reliability.

Simulation results under several operating conditions are discussed and experimental results for a three phase 460 V/20 kVA unit are presented.

4.2. Active Harmonic Filter (AHF) design considerations

In order to achieve further harmonic distortion improvement of the 18-pulse rectifier, a shunt active power filter is connected at the input. Fig. 48 depicts a schematic the proposed approach. A lab prototype was built and tested and a control strategy based on source current detection was implemented.

The reduced kVA APF is used in order to:

i) Mitigate part of the remaining current harmonic that the 18-pulse rectifier could not compensate

ii) Achieve satisfactory performance under wide range of operating conditions

iii) Improve the performance under abnormal input voltage conditions.

In Fig. 48 it can be seen that the topology employs the conventional six IGBT inverter. It is connected to the common connection point between the ac source and the rectifier through a linkage reactor. The APF filter is able to inject the proper reactive power to achieve displacement power factor near to one and provide the suitable current harmonic content to reduce the input current THD. However, in order to reduce the APF kVA rating only current harmonic mitigation is targeted. The APF is controlled by means of a fixed switching frequency carrier based control. The control strategy allows providing the suitable harmonic current profile (I_{AF}) while the voltage dc (V_{dc}) is kept constant.
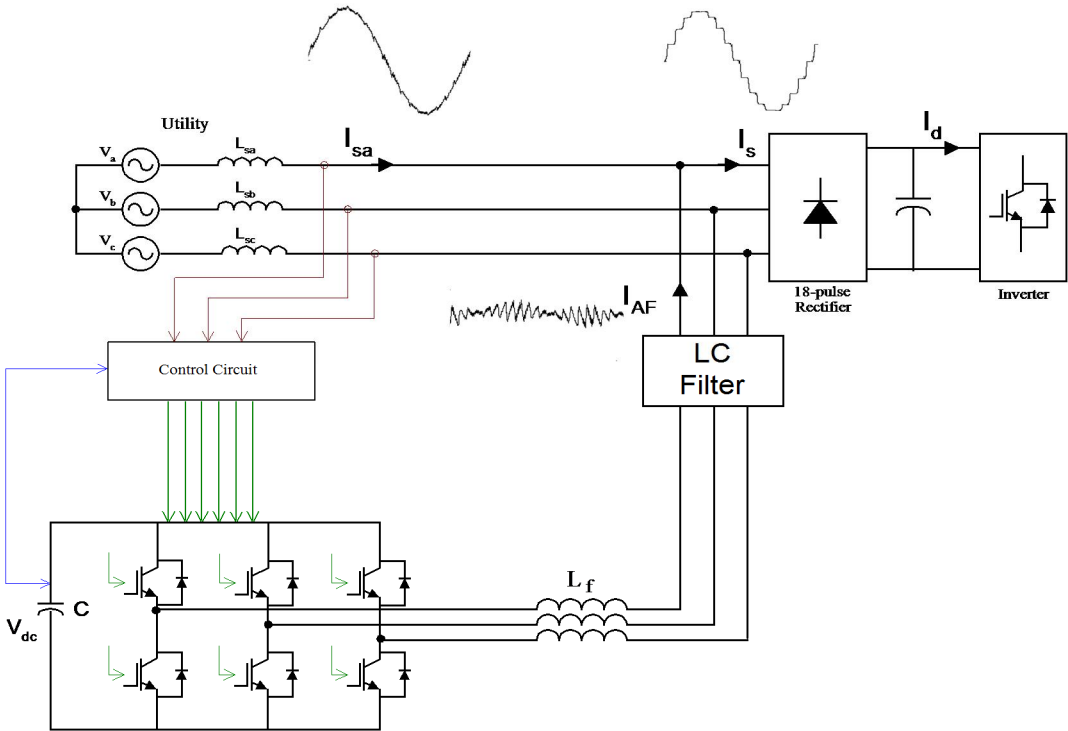
Fig. 48. 18-pulse rectifier with active power filter compensation.

The VA rating of the AHF depends on both the total reactive power to be compensated and the current distortion component of the 18-pulse rectifier's input current. Thereby, the active filter VA rating estimation need to take into account these two variables.

Generally, the total current (in per unit) that the active filter has to compensate is:

$$I_{AF} = \sqrt{I_q^2 + I_{dis}^2} \tag{28}$$

Where:

I_{AF} : active filter RMS current.

I_q: the current component due to the reactive power to compensate.

I_{dist} : the distortion component of the current that need to be compensated (I_s).

Since,

$$I_r = \sqrt{I_{r1}^2 + I_{dist}^2} \tag{29}$$

And,

$$I_{r1}^2 = I_p^2 + I_q^2 \tag{30}$$

Where,

I_r : the RMS value of the 18-pulse (18-P) rectifier *total input* current.

I_{r1} : the RMS value of the *fundamental* component of rectifier input current I_r.

I_p : the RMS value of the *active* component of 18-P rectifier's fundamental (I_{r1})

I_q : the RMS value of the *reactive* component of 18-P rectifier's fundamental (I_{r1})

Given the conventional definition of THD,

$$THD_i = \frac{\sqrt{\sum_{i=2}^{n} I_{ri}^2}}{I_{r1}} = \frac{I_{dist}}{I_{r1}} \tag{31}$$

the definition of Displacement Power Factor DPF,

$$DPF = \frac{I_p}{I_{r1}} \tag{32}$$

and using I_r as a base, it possible to redefine the expression(29) and the other variables in per unit base. Therefore;

$$I_r = \sqrt{I_{r1}^2 + I_{dist}^2} = 1\,p.u. \tag{33}$$

$$I_{r1} = \sqrt{1 - I_{dist}^2} \tag{34}$$

Replacing (34) in (31) it is possible to compute for I_{dist} and I_{r1} as a function of THD_i,

$$I_{dist} = \frac{THD_i}{\sqrt{1 + THD_i^2}} \tag{35}$$

$$I_{r1} = \frac{1}{\sqrt{1 + THD_i^2}} \tag{36}$$

Now, from basic circuit theory (Fig. 49), I_q can also be expressed in per unit base,

$$I_q = I_{r1}\sqrt{1 - DPF^2} \tag{37}$$
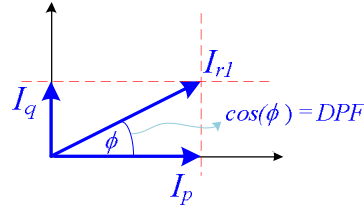
Fig. 49. Rectifier's fundamental current phasor diagram.

Replacing (36) in (37) yields,

$$I_q = \frac{1}{\sqrt{1 + THD\,_i^2}}\sqrt{1 - DPF^2} \tag{38}$$

and by replacing (35) and (38) in (28), the total active filter current (I_{AF}) is:

$$I_{AF} = \sqrt{1 - \frac{DPF^2}{1 + THD_i^2}} \tag{39}$$

Based on equation (39), the active filter's kVA rating versus THDi for different displacement power factors (DPF) is plot in Fig. 50. It can be seen that the kVA rating is considerably dependent upon the DPF to be compensated. Typically, multipulse rectifiers present very high DPF (> 0.98). Therefore, is very convenient to not compensate for DPF in order to reduce the active filter VA rating. Fig. 50 shows just that, for DPF equal to 1.0 and THD equal to 21%, the required active filter VA rating is only 20% of the total system kVA.

74
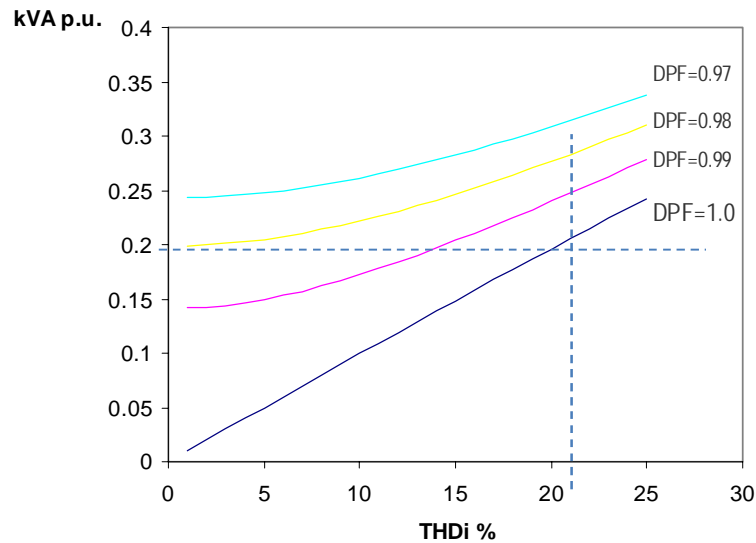
Fig. 50. APF kVA rating versus compensating current THDi for different rectifier's displacement power factor (DPF).

4.3. Control strategy

The control strategy is based on a supply current detection method. Fig. 51 depicts the active filter control scheme. A proportional integral (PI) controller is used to maintain the dc bus voltage and three PI current controllers are used to shape the input currents. The input voltage waveforms are used as current references such that the APF tries to make the input currents to follow the input voltage waveforms while the dc bus voltage is kept constant. This control method will make the rectifier be seen as a purely resistive load. This simple strategy avoids harmonic overcompensation and the burden phase lock loops to synchronize with the grid providing significant immunity to grid synchronization issues typically found with zero-crossings methods. However, it does not have the capability to discriminate between harmonics and reactive power, and lack

of harmonic selectivity. Nevertheless, for its simplicity and testing purposes this strategy is preferred.

4.3.1 DC bus controller

Since the control scheme is based on input current measurements, only one set of three-phase current sensors is needed, which reduces the cost of the approach. The dc bus voltage sensor is implemented by an isolation differential amplifier. The output of the voltage controller serves to modify the amplitude of the rectifier's input current reference (input rectifier current). By controlling the rectifier's input current amplitude, which is intended to be in phase with the input voltage, it is possible to control the active power given and drawn by the inverter and therefore to control its dc bus voltage. If the voltage controller is allowing flowing more active power (from source to load) than what the load can absorb, some portion of the power will go to the rectifier and another portion will go to the active filter inverter. The extra active-power going to the APF's inverter will increasing its dc bus voltage. Conversely, if the input active-power is lower than the rectifier's load active-power, the inverter will have to provide the difference; thereby its dc bus voltage will inevitably decrease. If there is no load, the active power transfer is done between the grid and the inverter, supplying only converter losses. In this way the active filter dc bus voltage is controlled.
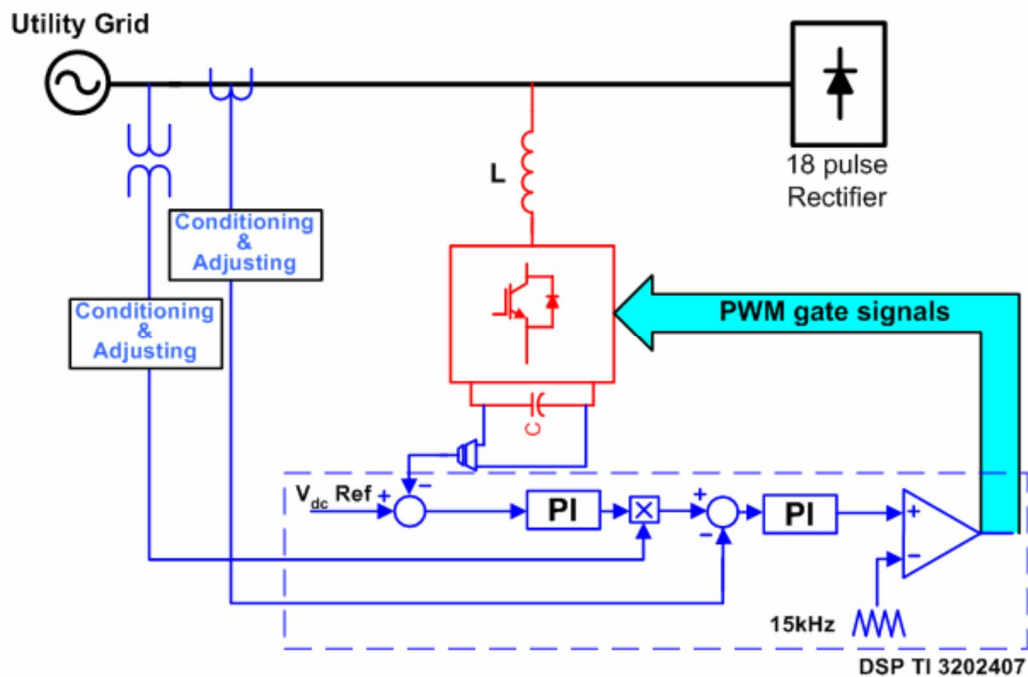
Fig. 51. Active Power Filter's control block scheme.

4.3.2 Current Controller

An inner PI current control loop is used for each of the three phases. The references of these controllers are modified by the same voltage controller single output as previously mentioned. The outputs of the current controllers are then compared with a 15 kHz triangle carrier in order to generate the inverter gating signals.

The PI current controller time constant is adjusted to be at least ten times faster than the voltage controller time constant in order to guarantee enough decoupling. Since a carrier PWM scheme is used, the current through the reactor cannot be modified faster than one switching cycle. Therefore the current controller time constant (K_i) should not be set faster than one switching period (T_s) and it was set to $2T_s$.

The control algorithm was implemented on fixed-point DSP Texas Instruments TMS320LF2407A.

4.4. Performance of 18-pulse rectifier with AHF

In order to have an estimation of the 18-pulse rectifier active filter approach performance, several simulations were executed by using PSIM 6.0 software. The rectifier load rated power is 30kW and the ac input voltage is 480Vrms. The autotransformer model is done by using three single phase transformer with multiple secondaries. The turn ratios of the multiple secondaries are selected accordingly in order to provide the magnitude and phase as described in Chapter III. TABLE VI shows a summary of the parameters used in the simulations.

TABLE VI

ACTIVE FILTER SIMULATION PARAMETERS

Input Voltage	V_{ac} = 480VRMS
Rectifier Load Rated Power	P_n=30kW
Active Filter Inductor	L = 1mH
Active Filter DC link Voltage	E = 815V
Switching Frequency	f_{sw}= 15kHz

The PSIM model of the 18-pulse transformer is shown in Fig. 52. Three single phase transformer are used, each with 4 secondaries. The turn ratios of the secondaries in p.u. are: a=0.135/0.482, b=0.135/0.482, c=0.253/0.482, d=0.253/0.482.
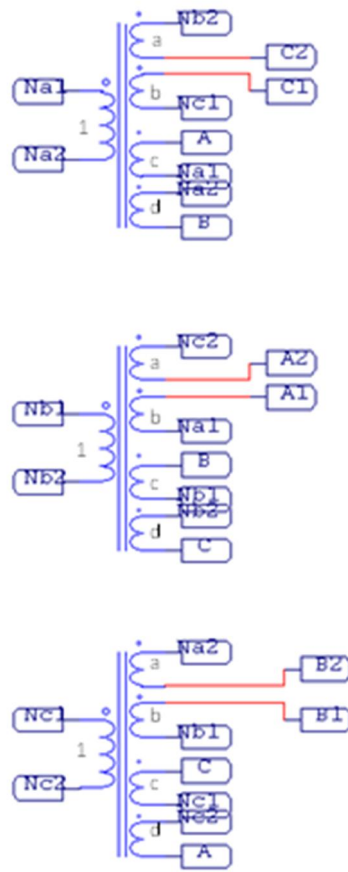
Fig. 52. 18-Pulse Autotransformer Rectifier PSIM model.
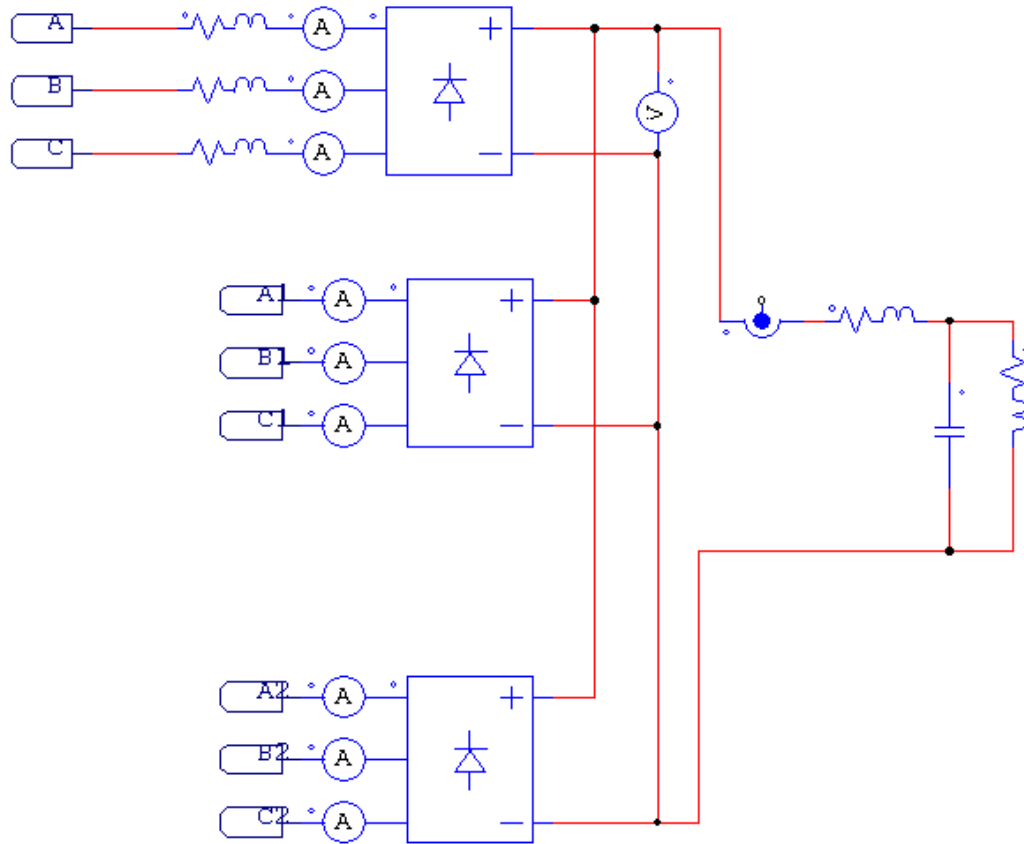
Fig. 53. 18-pulse rectifier PSIM model.

The 18-pulse rectifier is modeled (Fig. 53) with three 6-pulse rectifiers, where the main rectifier is fed directly from the input grid through some impedance matching reactors and the two auxiliary rectifiers are fed from the autotransformer.

The active filter is modeled with six IGBTs connected to a capacitor at the dc side and to three line reactors at the ac side as shown in Fig. 54.
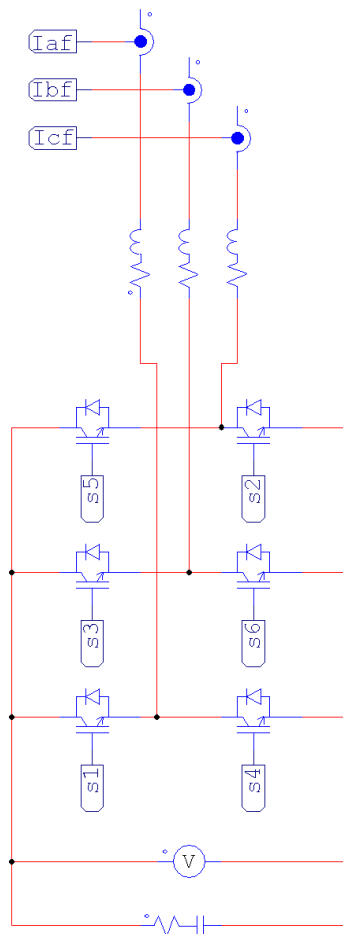
Fig. 54. PSIM model – APF IGBT 2-Level converter.

Fig. 55 shows simulation results for 30kW/480V system under ideal voltage conditions. The THD of the rectifier's input current (I_s) is 8.7% and the THD of the total input current is reduced to 1.3% when the active filter starts to operate. On Fig. 56, the steady state total input currents for the same input voltage conditions are shown to demonstrate the effectiveness of the active filter.
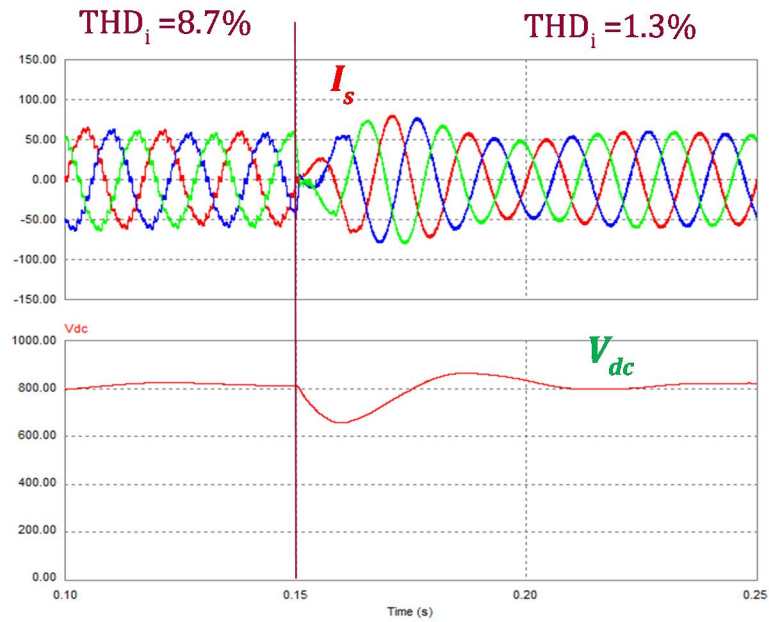
Fig. 55. 18-p rectifier w/APF simulation results for ideal input voltage conditions. Total input currents (top). APF's DC bus voltage (bottom).
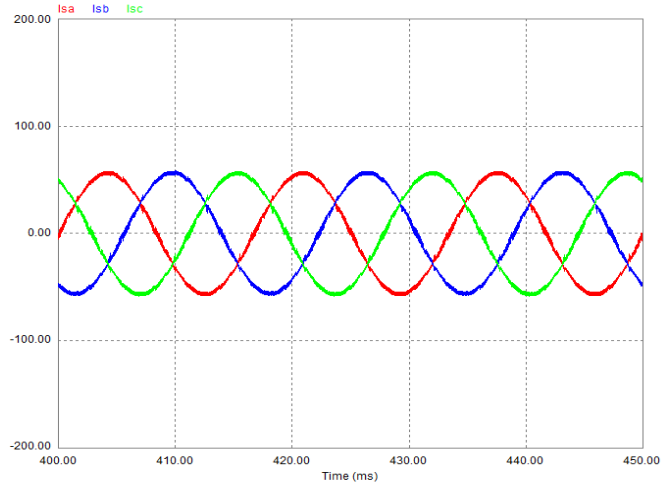
Fig. 56. 18-p rectifier w/APF simulation results for ideal input voltage conditions. Total input currents in steady state.

4.5. Harmonics of 18-pulse rectifier under unbalanced and distortion.

In order to determine the approach's performance under abnormal voltage conditions, simulations results for pre-existent voltage distortion and unbalance voltage conditions were performed. Fig. 57 shows the APF performance under 2.5% 5th harmonic voltage distortion. The THD before compensation is 37% and it gets reduced to 2.9% when the APF is operating. It is interesting noting that the inputs current have larger distortion than the previous case (ideal voltage conditions) since the current references are obtained from the input voltage waveforms which are distorted. In this manner, the overall rectifier approach is seeing as a purely resistive load, where the input currents adopt virtually the same shape than the voltage waveform.

Fig. 58 shows the steady state input currents for the same voltage distortion conditions.
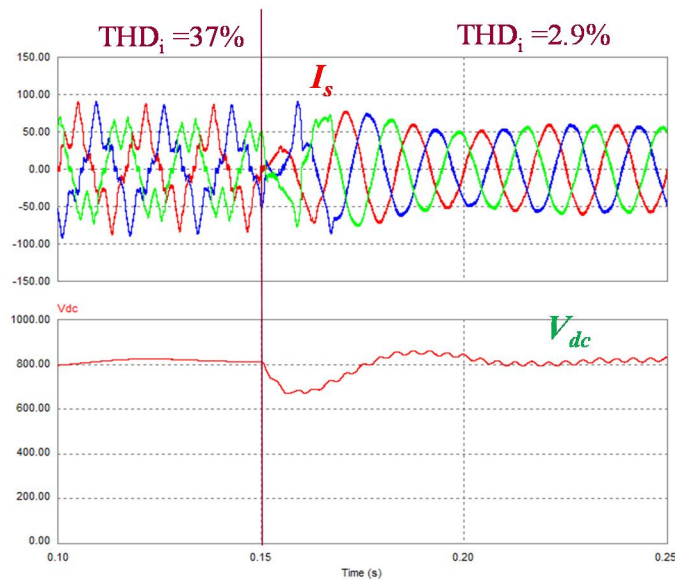
Fig. 57. 18-p rectifier w/APF simulation results for 2.5% 5th harmonic voltage distortion. Total input currents (top). APF's DC bus voltage (bottom).
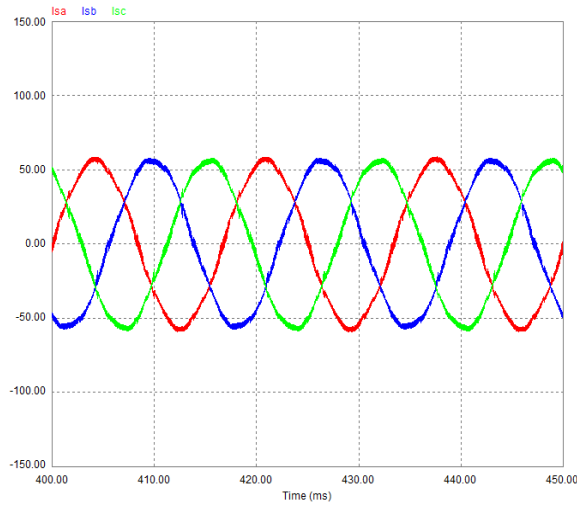
Fig. 58. 18-p rectifier w/APF simulation results for 2.5% 5th harmonic voltage distortion. Total input currents in steady state.

On the other hand, the results for a 3% input voltage unbalance condition are shown in Fig. 59. The THD is reduced from a 33% down to 3.2% when the APF is operating. Fig. 60 shows the steady state input currents for the same voltage unbalance conditions. Similarly than the previous case, the current waveforms adopt the shape of the input voltages, which in this case are unbalanced.
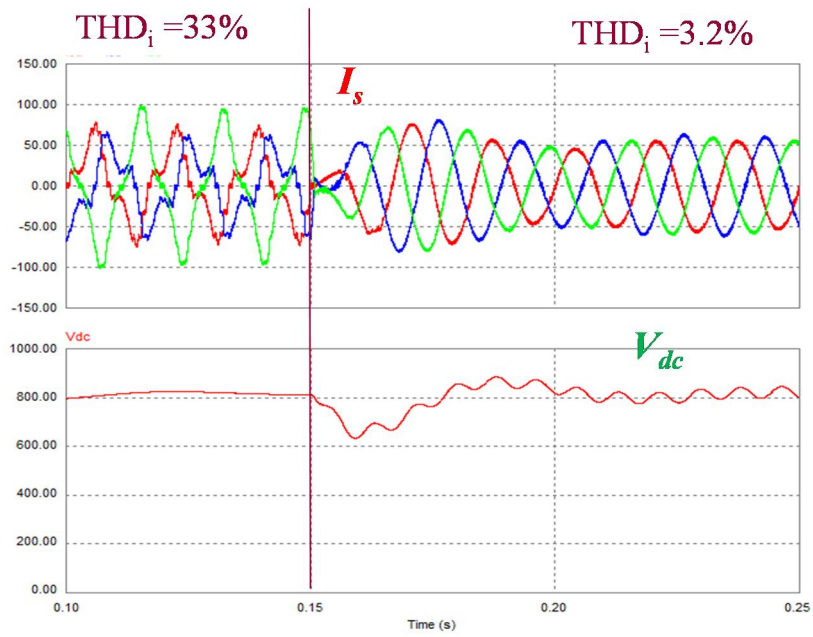
Fig. 59. 18-p rectifier w/APF simulation results for 3% input voltage unbalance. Total input currents (top). APF's DC bus voltage (bottom)
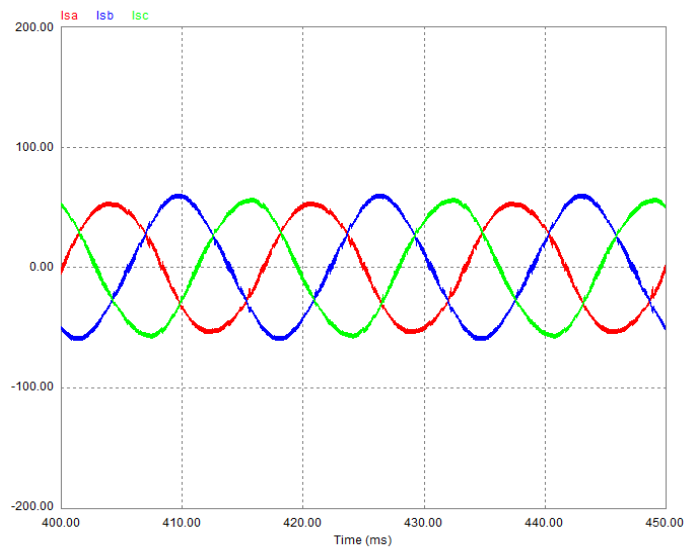
Fig. 60. 18-p rectifier w/APF simulation results for 3% input voltage unbalance. Total input currents in steady state.
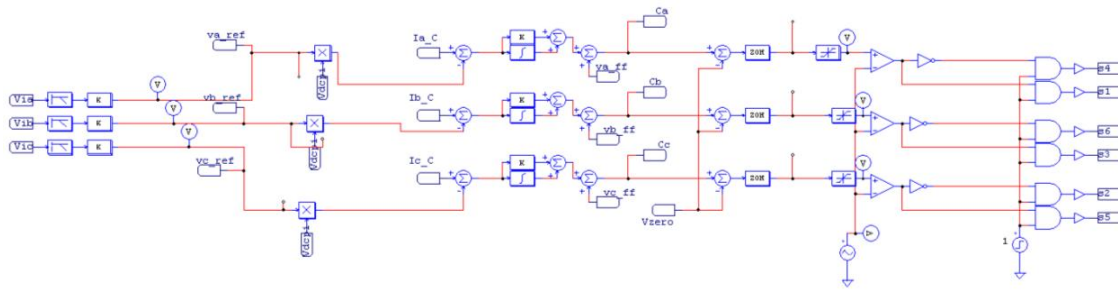
Fig. 61. PSIM model - APF's current controllers.

Fig. 62. PSIM model – 18-pulse asymmetric rectifier w/APF.

Fig. 61and Fig. 62 show the PSIM simulation models.

Fig. 63 shows current injected by the active filter. It can be observed that the filter injects mostly current harmonics and small fundamental component. The rms value of the input current is 38.1 A, while the active filter current is only 5.9 A which corresponds to 15.4 %.

Fig. 63 also shows the response of the approach during a change in the load operating condition from 50% to 100%. Similarly, Fig. 64 shows the response of the approach during a load step from 0 to 100%. The APF takes approximately two line cycles to stabilize and fully compensate since the dc voltage experience a transient. The overall response of the APF is adequate.
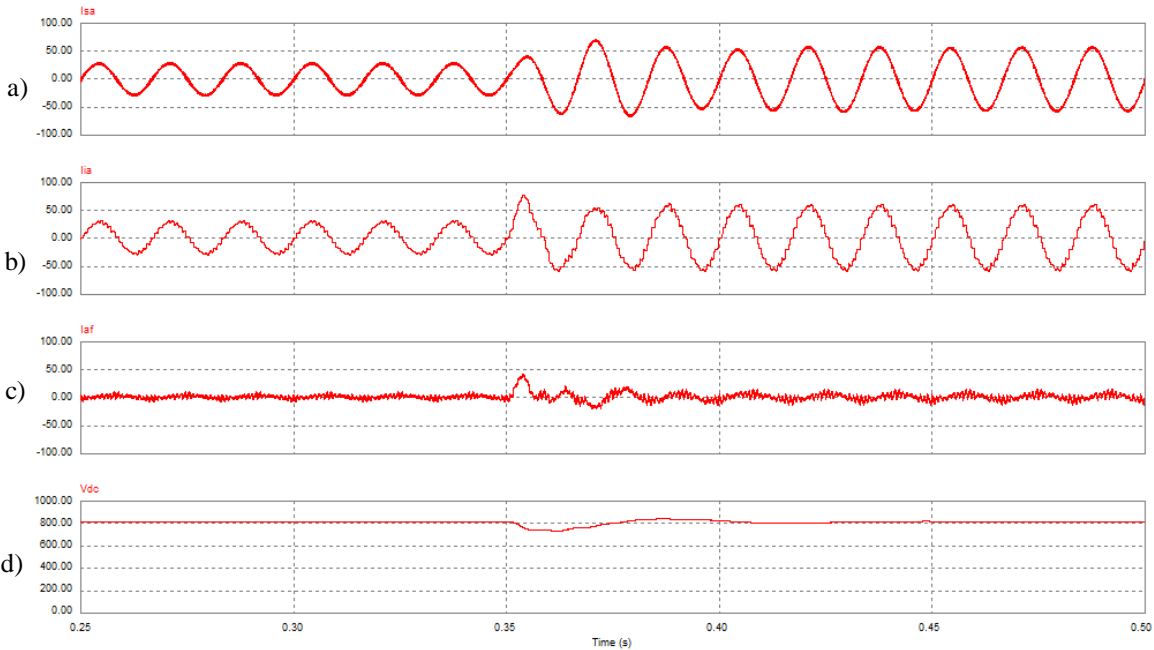
Fig. 63. Simulation results for 50% to 100% change in the load operating condition a)Total input current b) Rectifier input current c) APF current d) APF dc link voltage.
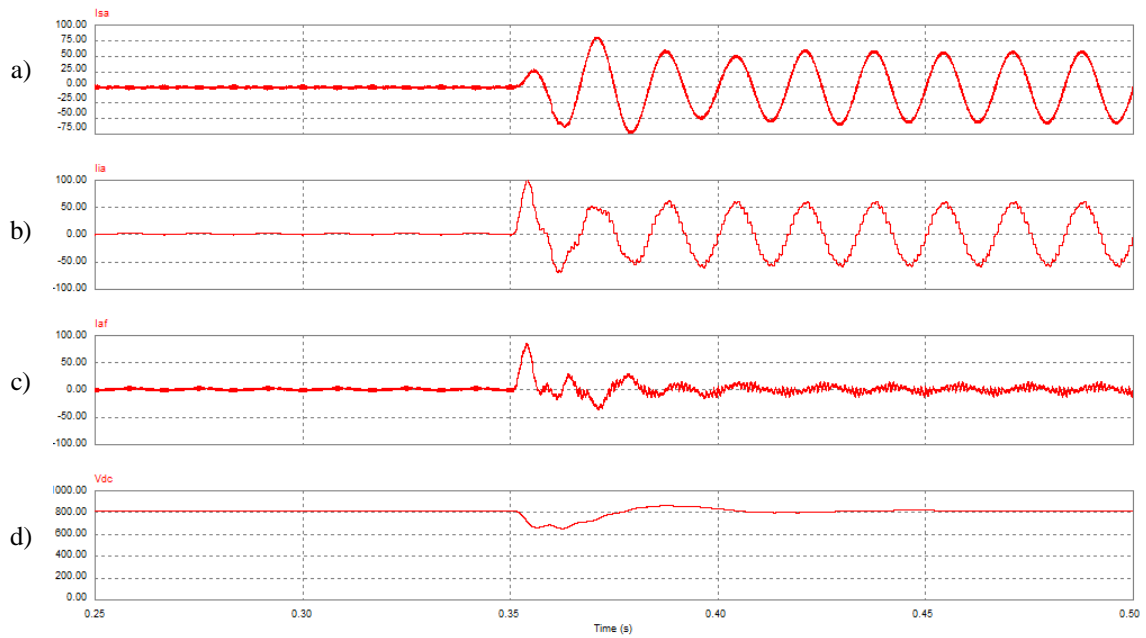
Fig. 64. Simulation results for 0% to 100% change in the load operating condition a)Total input current b) Rectifier input current c) APF current d) APF dc link voltage.

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4.6. Experimental results

A three phase 460V/20kVA unit ASD was tested. Fig. 65 shows a diagram of the lab set up.
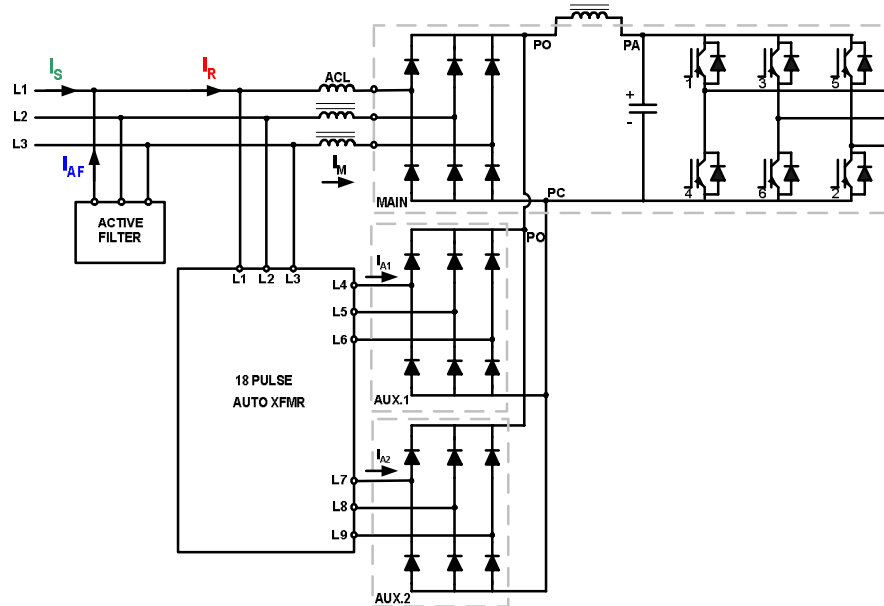
Fig. 65. Asymmetric autotransformer 18-pulse rectifier and active filter experimental set up.

Before the active filter starts to operate, the supply current corresponds to the rectifier's input current thereby it has the same shape. The filter starts with the gating signals on the off position therefore none of the IGBTs are on. The dc bus capacitors are charged through the IGBTs' body diodes. A pre-charge resistor in series limits the capacitor's inrush current and it is by-passed by a contactor once the dc bus is charged to the peak of the input phase-to-phase voltage (~650V). The instant when the active filter starts to operate for clean utility conditions and light load is shown on Fig. 66. Initially some instability in the supply current is observed since the inverter dc bus has to be

charged to the reference value of 815Vdc. In about 120ms after starting, the supply

current is fairly stable and the current harmonic cancellation is observed.
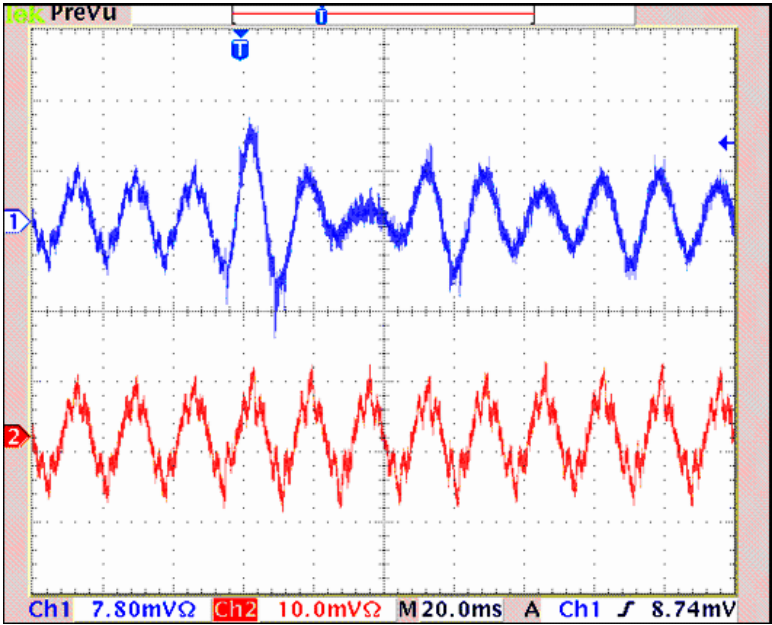
Fig. 66. Active filter starting operation instant.

Fig. 67 shows in more detail the rectifier's input current and the overall input

supply current. It is clear that some harmonic cancellation is achieved.
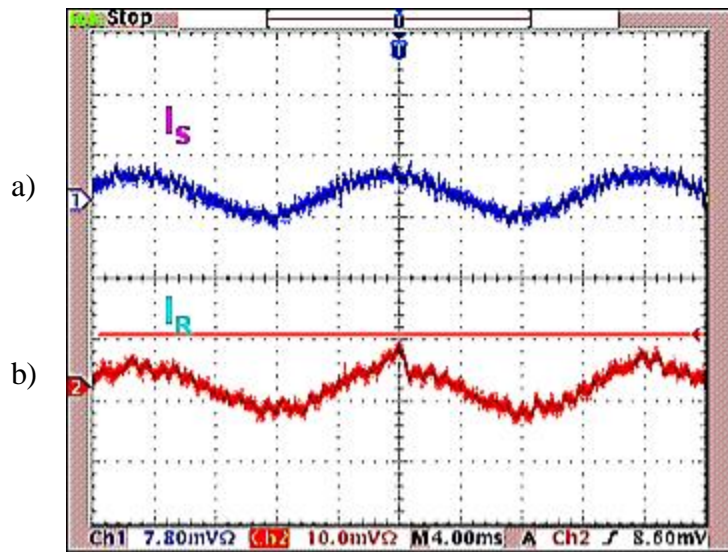
Fig. 67. a) Input supply current b)18-P rectifier input current.

Fig. 68 shows the active filter current during compensation. It is worth noting that this current is composed mainly of harmonic components and very small fundamental.
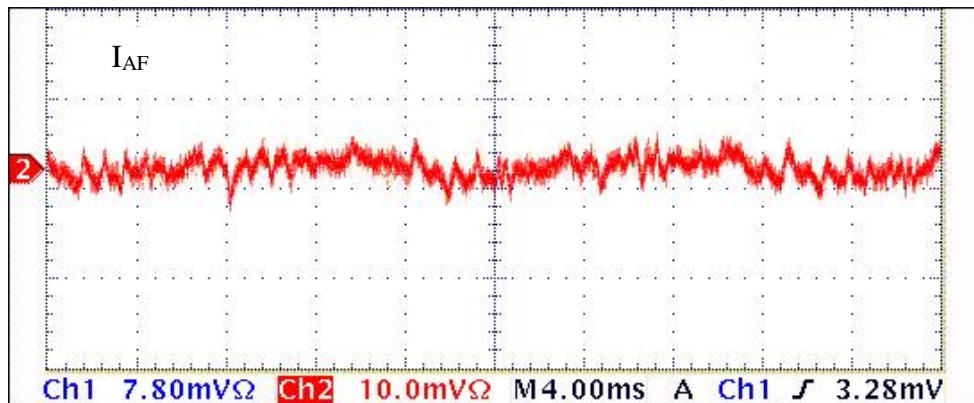
Fig. 68. Active Power Filter current. .

The system was tested under a variety of simulated input voltage abnormal conditions. A three-phase programmable ac power supply 47-66Hz/135-270V/63kVA California Instruments FCS Series was employed for this purpose.

Fig. 69 shows the supply current and input rectifier's when not abnormal condition in the supply voltage is present. The rectifiers input THD is 13% and it is brought down to 6.5% when the active filter is operating. The input current is approximately 20A.
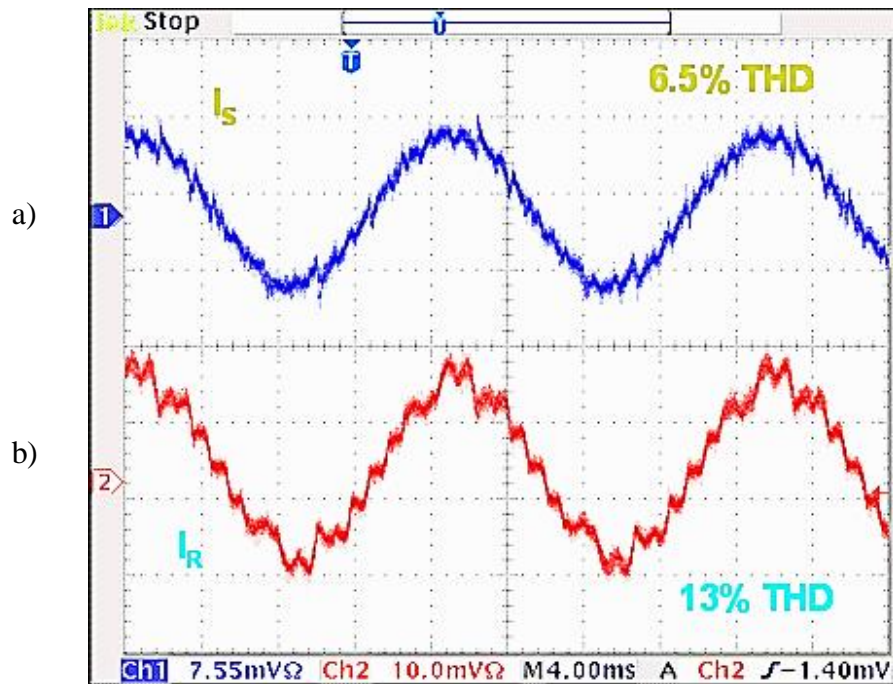
Fig. 69. APF performance for ideal voltage supply conditions. a) Input supply current. b) Rectifier's input current.

Fig. 70 and Fig. 71 shows the active filter performance for 2% voltage supply unbalance. The THD observed in the rectifier's current was 22% while the THD at the

supply current was 8%. Similarly, the unit was tested under pre-existent voltage harmonic distortion. The supply was programmed to provide 3% of 5th harmonic and 2% of 7th. The rectifier current THD was 20% and the APF brought it down to 8% as well.
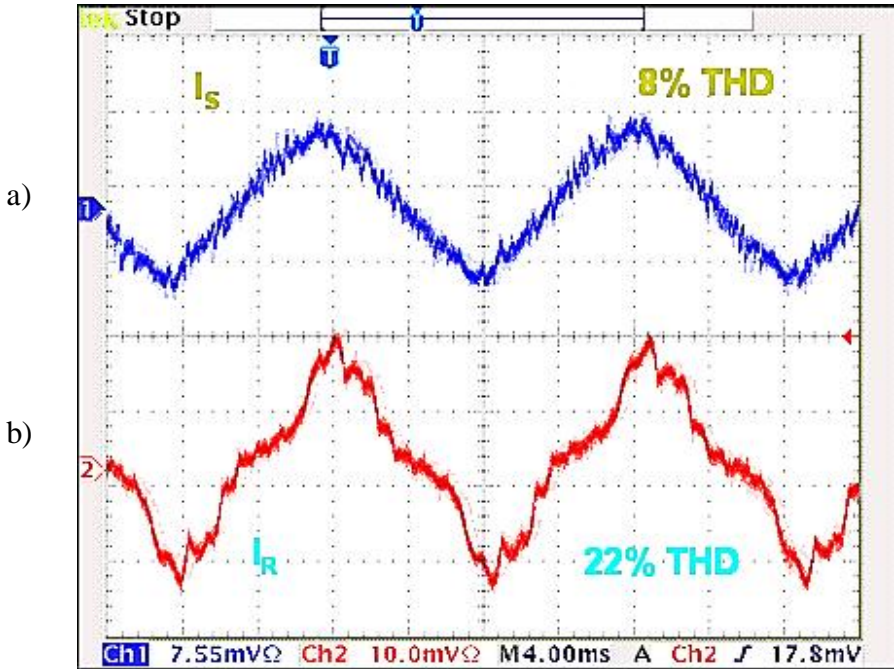
Fig. 70. APF performance for 2% voltage unbalance. . a) Input supply current. b) Rectifier's input current.
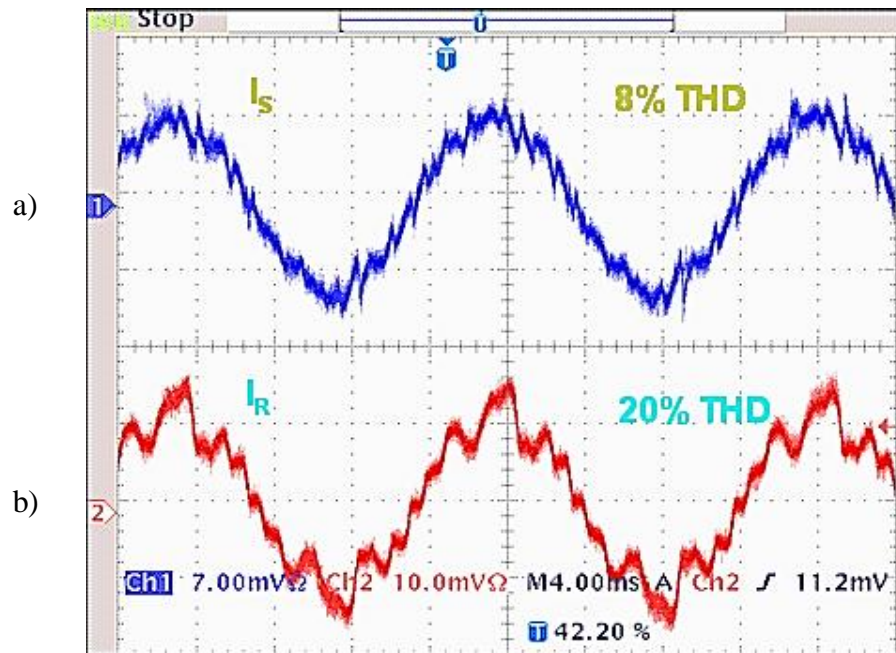
Fig. 71. APF performance for voltage harmonic distortion 5th (3%) & 7th (2%). a) Input supply current. b) Rectifier's input current.

A second APF unit was built and additional tests were performed. At the testing lab, the input supply voltage was fairly clean and balanced within typical standard recommendations. However, occasionally the input voltage experienced some harmonic distortion. It was observed a harmonic distortion as high as 3.5% at some given point. Fig. 72 shows the results for load condition of 70%. The 18-pulse rectifier input THD was 11%, without active compensation and 4% when the active filter was operating.
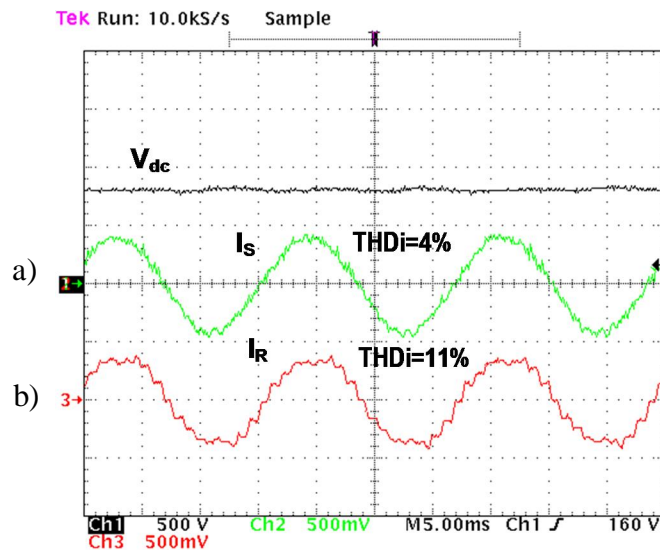
Fig. 72. Rectifier-APF's input current for clean utility. a) with active compensation b) without active compensation.

Similarly, when the utility presented some harmonic distortion (~3.5%) the input current THD was 27% for the same load condition. The harmonic distortion was reduced to 11% when the active filter was applied (Fig. 73)
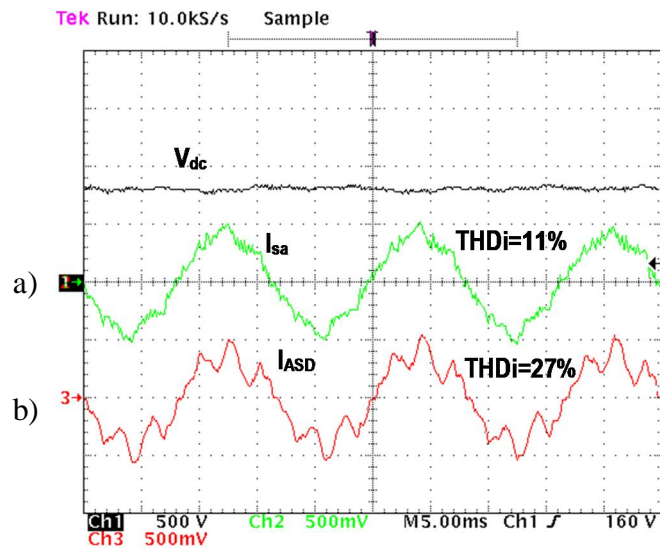
Fig. 73. Rectifier-APF's input current for distorted utility. a) with active compensation b) without active compensation.

Fig. 74 shows a summary of the 18-P rectifier-APF's performance for several load conditions when the input voltage was free from disturbances. The input current THD was significantly lower than the rectifier input current THD for all loads conditions, verifying the proper operation of the active harmonic filter.
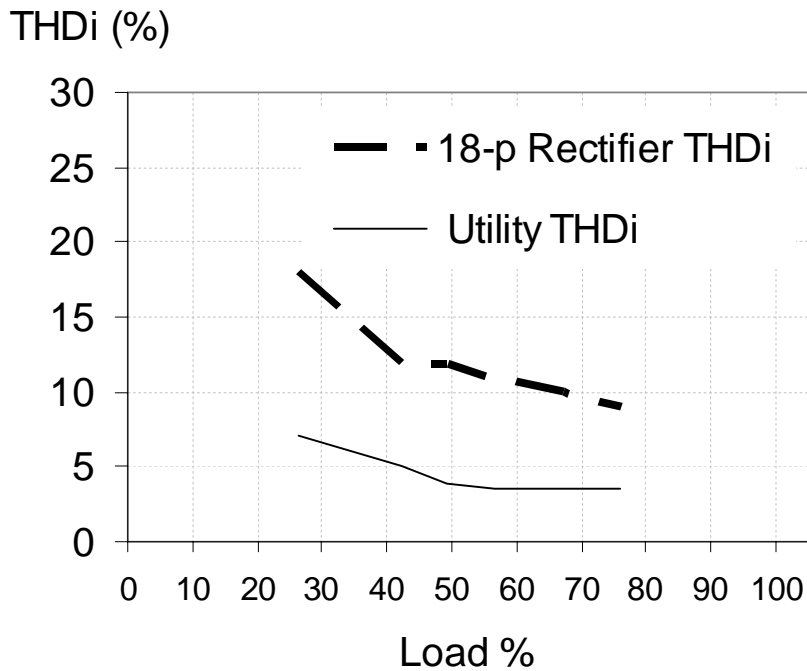
THDi (%)

Fig. 74. 18p rectifier-APF performance for clean utility

4.7. Conclusions

An 18 pulse rectifier with Active Filter compensation to improve the input current THD in adjustable speed drive is proposed. The fact that the 18 pulse rectifier is responsible for the main current distortion compensation and no reactive power is compensated allows the APF to be specified as a fraction of the total ASD VA rating.

The APF provides the 18-pulse rectifier with the ability to achieve a high performance over a wide spectrum of operating conditions. Simulation results show that the approach can compensate up to 2.5% current THD. The approach also has the characteristic of maintaining a balance of performance, cost and reliability. The reliability of the system is maximized due to the fact that the AC/DC conversion process relies on a passive 18-pulse rectifier technology.

CHAPTER V

AN INTERLEAVED THREE PHASE ACTIVE POWER FILTER WITH

REDUCED SIZE OF PASSIVE COMPONENTS *

5.1. Introduction

In this part of the work an interleaved active power filter concept with reduced size of passive components will be discussed. The topology is comprised of two PWM interleaved voltage source inverters - however it can be extended to a larger number of inverters - connected at the ac-line and sharing the same dc-link capacitor (Fig. 75). The advantages of the proposed approach include: i) reduction in the linkage inductor size by decreasing the line current ripple due to the interleaving, ii) reduction of the switching stress in the dc-link capacitor, due to the reduction on the current ripple, iii) more efficient implementation for high power applications because of the power sharing and possibility of a lower switching frequency. This work analyzes the design of the passive components and gives a practical and low cost solution for minimization of the circulation currents between inverters, by using a zero-sequence control loop and common mode coils. Several simulations results will be discussed and experimental results in a three-phase 10 kVA, 400 V unit are presented that validate the theoretical analysis.
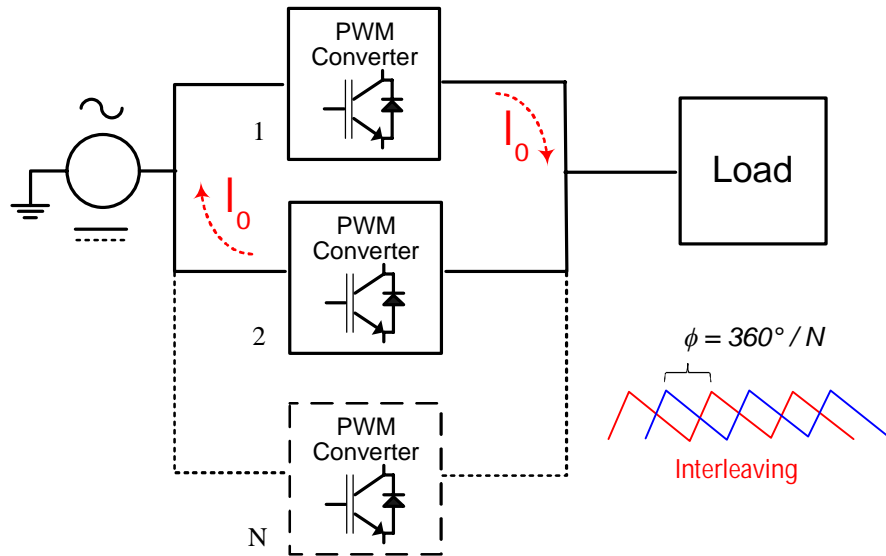
Fig. 75. Principle of paralleling multiple power inverters for a shunt active power filters.

5.2. Interleaved inverters for active power filtering

Active methods for harmonic mitigation are a viable and increasing practice in industrial applications. However, the harmonic compensation using active solutions for high power applications is usually limited by the available semiconductor technology, due to the maximum voltage ratings and losses limiting practical switching frequencies. In order to cope, with high power requirements, several solutions, such as hybrid topologies, multilevel structures, and paralleled inverters are proposed in the literature. Paralleling multiple inverters makes the design, production, installation and maintenance much simpler, flexible and provides higher reliability since the N+1 redundancy principle can be applied.

The present part of the work analyzes the application of parallel interleaved inverters for current harmonic mitigation and reactive power compensation. The

topology consists of a parallel connection of two identical three-phase interleaved two-level PWM inverters, sharing the same dc-capacitor an ac input source (Fig. 76),.
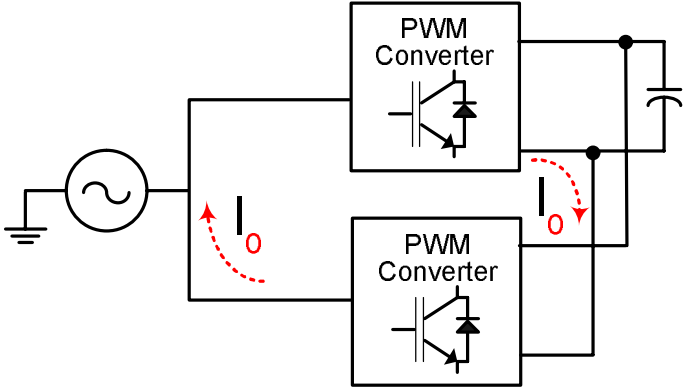
Fig. 76. Interleaved Active Power Filter with two inverters.

Previous work proposed a similar structure where the dc-side is interconnected (Fig. 77), but the ac-side includes a power transformer for galvanic isolation [87]. However, it is highly desired to avoid the use of this transformer since it is bulky and expensive. The transformer has to be designed to withstand the harmonic current spectrum and prevent overheating as well as furnished with suitable EMI filters to preserve its lifetime.
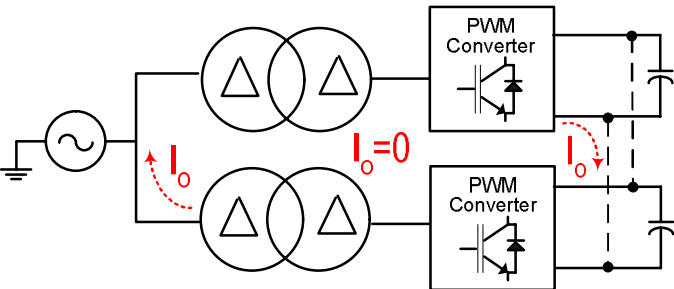
Fig. 77. Conventional parallel active power filter with isolation transformer.

On the other hand, removing the isolation transformer and connecting the inverters directly on the ac-side as in Fig. 76, contributes to the circulation of currents between the inverters. These currents are manifested in the form of high frequency zero-sequence components or cross-currents and low frequency currents referred here as the zero-sequence component or average zero-sequence component.

This approach proposed an effective and low cost method to minimize the circulation currents by installing common-mode inductors on each inverter to limit the high-frequency components, and the addition of a zero-sequence controller to eliminate the low frequency circulating current. It is expected that due to the interleaving, the line inductors size can be reduced comparing to a typical three-phase 2-Level PWM single inverter or to two parallel 2-Level inverters without using interleaving.

Fig. 78 and Fig. 79 show the principle of interleaving. Two carrier of equal switching frequency ($f_{sw}=1/T_s$) are used to generate the parallel inverters' gating signals. The relevant signals for only phase *a* are considered to simplify the explanation. Carrier 1 is 180° apart from Carrier 2. D_a is the instantaneous duty cycle or modulator. The intersection of the duty cycle D_a and Carrier 1 generates the gating signals for phase *a* of converter 1, and the intersection of D_a and Carrier 2 generates the gating signals for phase *a* of converter 2. This results on the generation of currents I_{a1} and I_{a2} which have similar average value over each switching period but different instantaneous value. In other words the ripple is generated at different instants. The objective is to generate the current ripples with opposite phase such that some cancellation at the point of coupling

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is achieved. The result is a current signal I_a with a ripple which magnitude is lower than its subcomponents and frequency N times the original components.
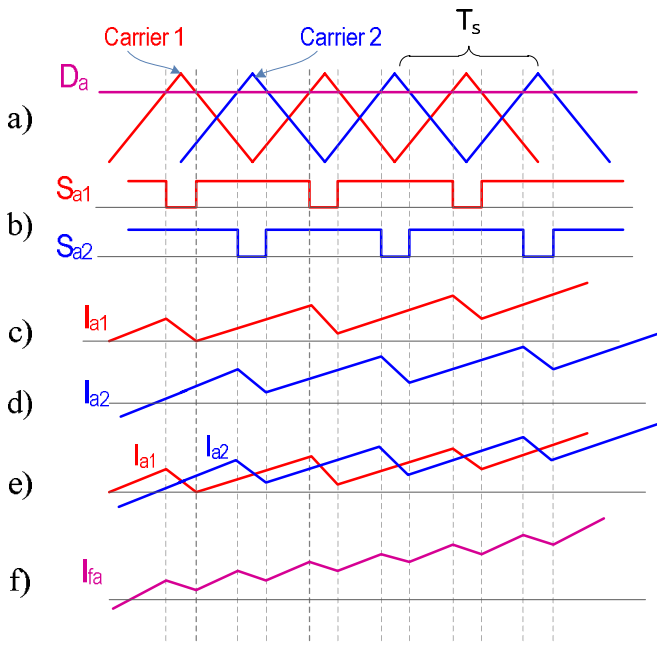
Fig. 78. Instantaneous interleaving signals. a) Triangle carriers and modulator b) Inverter's IGBTs Sa1 and Sa2 gating signals. c) Inverter 1 input current, I_{a1}. d) Inverter 2 input current I_{a2}. e) Inverter input current I_{a1} and I_{a2}. f) Aggregate input current: sum of I_{a1} and I_{a2}.
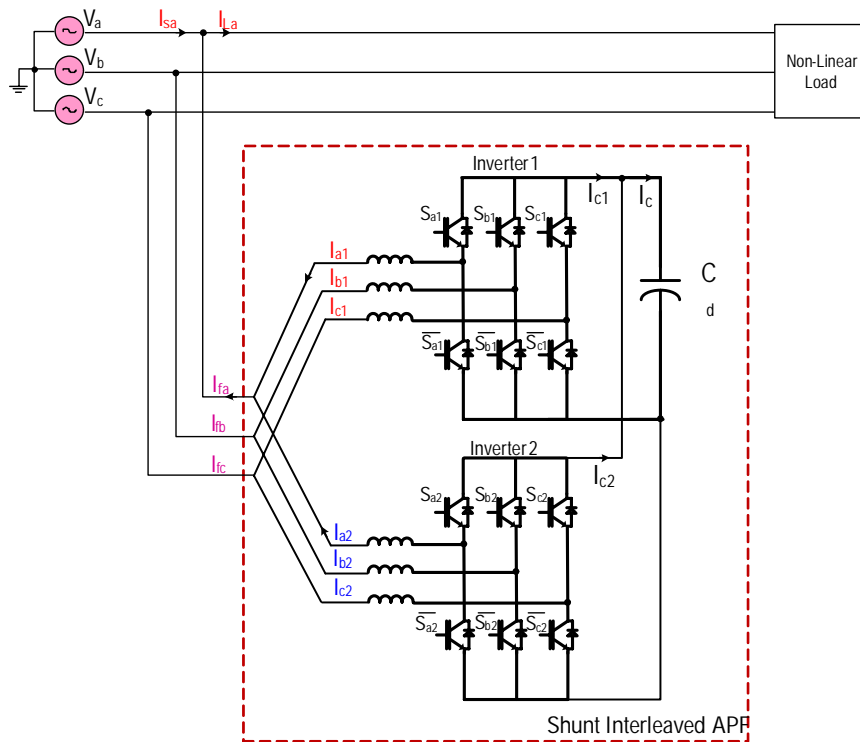
Fig. 79. Dual-interleaved-inverter APF

The magnitude of the cancellation depends upon the value of the duty cycle Da. For sine wave duty cycle like the case of an inverter, the degree of cancellation is variable and it depends on the point on wave; however it will be shown that the maximum ripple is always lower for the interleaved inverters, compared with the non-interleaving case.

5.3. Current ripple cancellation with interleaved inverters

When interleaved inverters are used, the current ripple can be significantly reduced for equivalent values of linkage inductors and same switching frequency. For example, if a single inverter with a linkage reactor of 5% is compared to a dual

interleaved-inverter case, as depicted in Fig. 79, the value of its linkage inductance L_F (respect to each inverter kVA) for the dual interleaved-inverter case is 5% as well but, rated at half the current. This means that its inductance value will double. If each inverter is running at 10kHz and a switching-frequency filter with the same corner frequency (same parameters) is used for both cases, the input current for the dual interleaved-inverter case (Fig. 81) will have significantly less 10 kHz ripple than a single-inverter case (Fig. 80) or when the two inverters are using interleaved carriers. The ripple cancellation will allow reducing the size of the linkage reactor respect of the single case or non-interleaving case. Fig. 80 and Fig. 81 show the two cases when the APF is generating only reactive power.
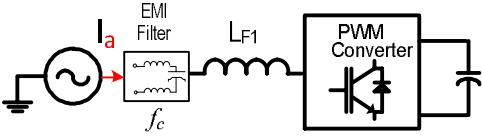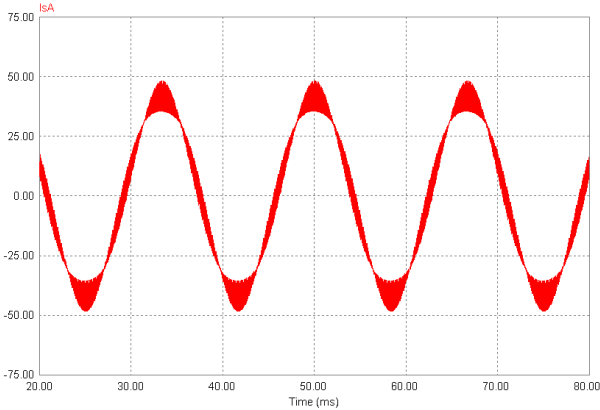
Fig. 80. Active power filter compensating reactive power with single inverter.

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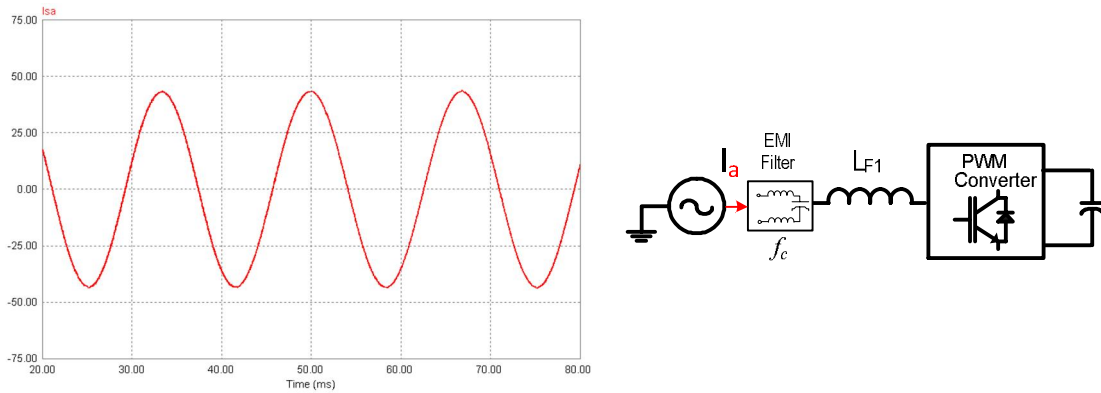
Fig. 81. Active power filter compensating reactive power with two interleaved inverters.

This converter topology and modulation strategy can be used to generate harmonics to realize a high performance APF. Fig. 82 shows the dual-interleaved-inverter structure compensating a 6-pulse non-linear load. The active filter is able to compensate the unwanted harmonics with minimal introduction of high frequency components to the systems. This is achieved by interleaving and the utilization of an EMI filter. The current injected by the APF is composed by the sum of the two inverters' currents. Even though, the current of each inverter has large ripple, the total current has significantly less ripple and at a frequency twice the one of each inverter. Therefore the high frequency components are much easier to filter, resulting on potential reduction of the size and weight of the linkage reactor, and switching frequency filter. Fig. 83 shows a detail of the current ripple cancellation process. It is worth noting that the ripple cancellation is not always the same and it will depends on the value of the duty cycle or modulator. TABLE VII shows the design parameters and Fig. 84 shows the design criteria.
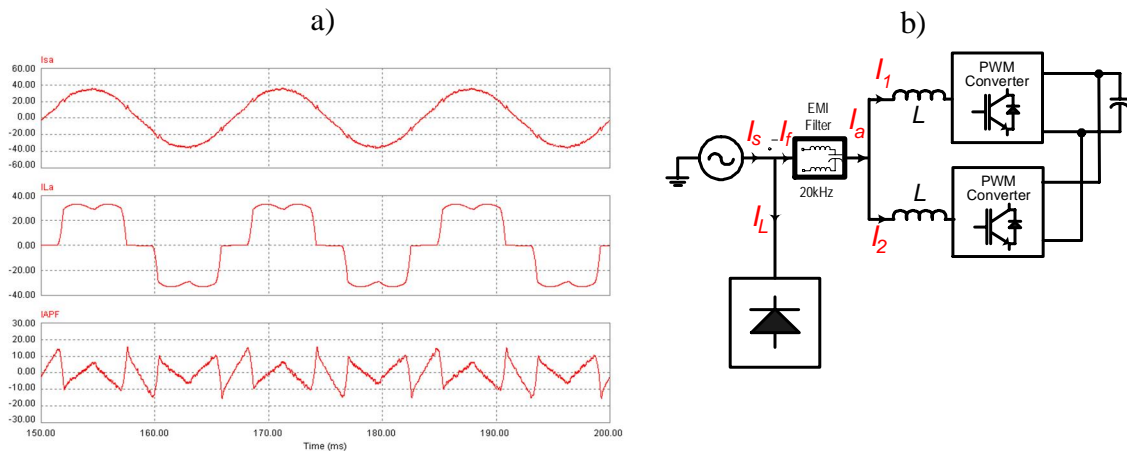
Fig. 82. Dual-interleaved-inverter APF structure compensating a six pulse non-linear load. a) Top to bottom. Source current I_s, load current I_L, APF's current I_f. b) APF single line diagram.
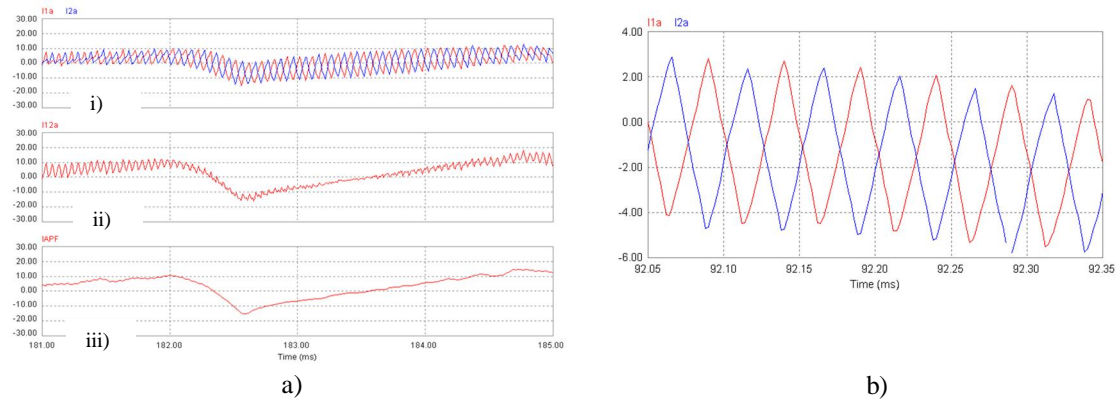
Fig. 83. Detail of APF compensating current. a) APF Currents i) Inverter currents I_1 and I_2, ii) Aggregate inverters' current I_a. iii) APF filtered current I_f. b) Zoom on Fig. 83.a.i) - inverters' current I_1 and I_2.

TABLE VII

VALUES OF THE INPUT PARAMETERS USED IN DESIGN.

Parameter	Symbol	Normalized value
Source voltage phase-neutral (peak)	V_S	1 pu
Line current (peak)	$I_{inv\,(pk)}$	1 pu
Current ripple (peak)	Δi_{max}	20 % · $I_{inv\,(pk)}$ = 0.2 pu
Voltage ripple	Δv_{max}	1 % · V_{dc}
Fundamental frequency	f_0	1
Switching frequency	f_{sw}	166 · f_0
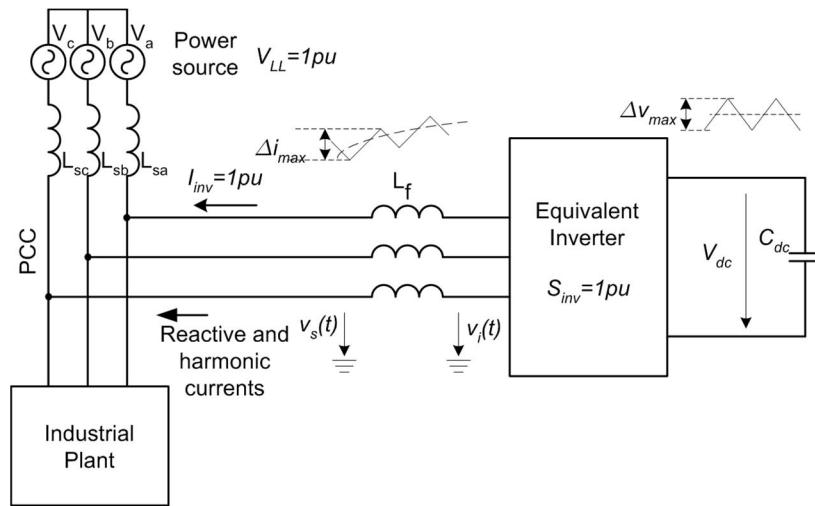
Fig. 84. Illustration of design criteria for the APF.

5.4. Linkage inductor considerations

The linkage inductor on an APF plays a crucial role in achieving a good dynamic response. Having a high value of the inductor gives a small current ripple but a low inductance is actually needed to be able to compensate the higher gradient of the load current. For a typical three-phase type APF these two principles have to reach a compromise depending on the imposed design criteria. However, since using two

interleaved inverters connected in parallel gives a certain amount of current ripple cancellation, the inductors may be intentionally selected of a low value, which allows an increase in the dynamic response of the APF and more importantly reduction of weight and volume as mentioned before. It is of interest of this work to determine how low the linkage inductors can be selected to achieve similar performance than when no interleaving technique is used.

For a PWM triangle carrier modulation technique and choosing the appropriated dc-bus voltage, the modulator or duty cycle (D_a, D_b, D_c) will vary in a sinusoidal way. It is fairly true, to assume that the inverter will provide mainly first harmonic voltage close to the utility rated voltage. The harmonic currents and/or reactive power will be injected by making only small changes to the sinusoidal duty cycles. Therefore, it is possible to assume that the duty cycle for each instant is known as well as the duration Δt of each state. Thus, a theoretical current ripple Δi can be estimated for each instant. In the case of one inverter, the maximum current ripple will always occur during the voltage zero crossing.

The magnitude of current ripple depends on a) the dc-bus voltage, b) the magnitude of the utility voltage at the given instant, c) the linkage inductance and d) the state duration Δt. By using an equivalent circuit, it is possible to calculate the current ripple for the each inverter state. TABLE VIII shows the equations of the current ripple for each state when the APF is composed from a single inverter. Taking into account that the maximum current ripple occurs during the voltage zero crossing, its magnitude can be calculated according to the present state of the inverter and its duration.

TABLE VIII

CURRENT RIPPLE Δi FOR EACH STATE IN A SINGLE INVERTER.

State	Line current ripple Δi
000, 111	$\Delta i = \dfrac{V_a\,\Delta t}{L_F}$
001, 010	$\Delta i = \dfrac{(3V_a/2 + V_{dc}/2)\,\Delta t}{3L_F/2}$
011	$\Delta i = \dfrac{(3V_a/2 + V_{dc})\,\Delta t}{3L_F/2}$
100	$\Delta i = \dfrac{(3V_a/2 - V_{dc})\,\Delta t}{3L_F/2}$
101, 110	$\Delta i = \dfrac{(3V_a/2 - V_{dc}/2)\,\Delta t}{3L_F/2}$

Fig. 85. Inverter states when the maximum current ripple occurs. Single inverter case. a) Instantaneous duty cycles and phase-A voltage to ground. b) Detail of the duty cycles and triangle carrier (top). Inverter's Phase-A current (bottom).

Fig. 85 shows the respective states and duration Δt at that instant. FromTABLE VIII it can be extracted that the equation that rules the current ripples for those states are shown in TABLE IX.

TABLE IX

CURRENT RIPPLE ΔI FOR A SINGLE INVERTER EVALUATED AT V_A=0.

State 110	$\Delta i = \dfrac{(3V_a/2 - V_{dc}/2)\,\Delta t}{3L_F/2}\bigg|_{Va=0} = -\dfrac{V_{dc}\Delta t}{3L_F}$
State 010	$\Delta i = \dfrac{(3V_a/2 + V_{dc}/2)\,\Delta t}{3L_F/2}\bigg|_{Va=0} = \dfrac{V_{dc}\Delta t}{3L_F}$
State 000	$\Delta i = \dfrac{V_a\,\Delta t}{L_F}\bigg|_{Va=0} = 0$
State 111	$\Delta i = \dfrac{V_a\,\Delta t}{L_F}\bigg|_{Va=0} = 0$

According to Fig. 85.b, the current in phase-a increases twice (intervals②) during the state 010 and it decreases twice (intervals ①) during the state 110. Therefore the total current ripple is:

$$\Delta i = 2\frac{V_{dc}\Delta t}{3L_F} = 2\frac{k_1\hat{V}_a\Delta t}{3L_F} \tag{40}$$

Generally, the dc-bus voltage can be expressed as a function of the phase to neutral voltage peak. So, $V_{dc}=k_1 \cdot V_{a(pk)}$, with $k_1 > 2$, depending on APF filter power.

Thereby, when the APF is implemented with one single inverter the maximum current ripple is:

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$$\Delta i_1 = \frac{k_1 \hat{V}_a \, 0.433 T_s}{3 L_F} \tag{41}$$

In the case of 2 interleaved inverters, the equation that rules the current ripple for each instant is different. Assuming that the maximum ripple of the resultant current always occurs at the phase-voltage peak $\hat{V}_a$ (obtained by observing multiple simulations), an equivalent circuit can be determined for this state based on Fig. 86.
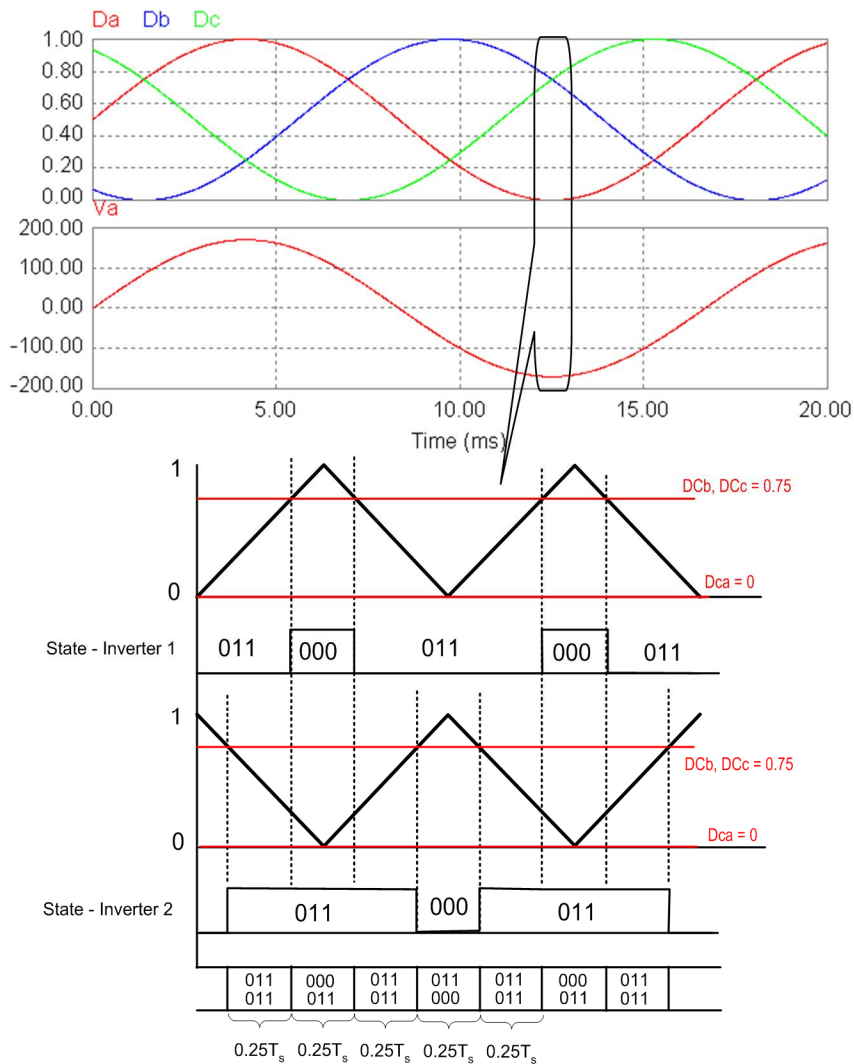
Fig. 86. Inverter states when the maximum current ripple occurs. Two interleaved inverters case.

Fig. 87 to Fig. 89 show the equivalent circuit respective the states when the maximum current ripple occurs. It can be demonstrated that the equations for states 011-011, 000-011 and 011-011 yields to the same values for the current ripple Δi.
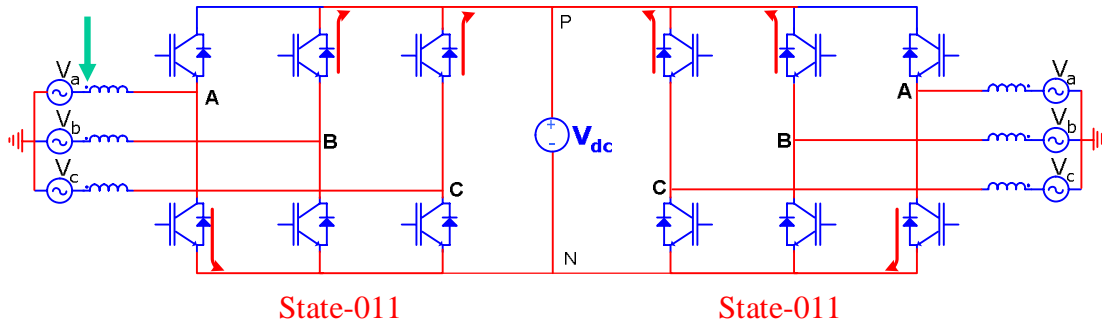
State-011   State-011

Fig. 87. Interleaved inverters model. State 011 on inverter 1 and 2.
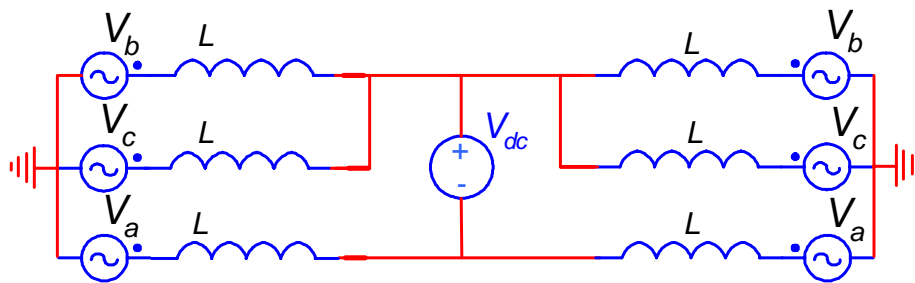
Fig. 88. Interleaved inverters equivalent circuit.

a)   b)
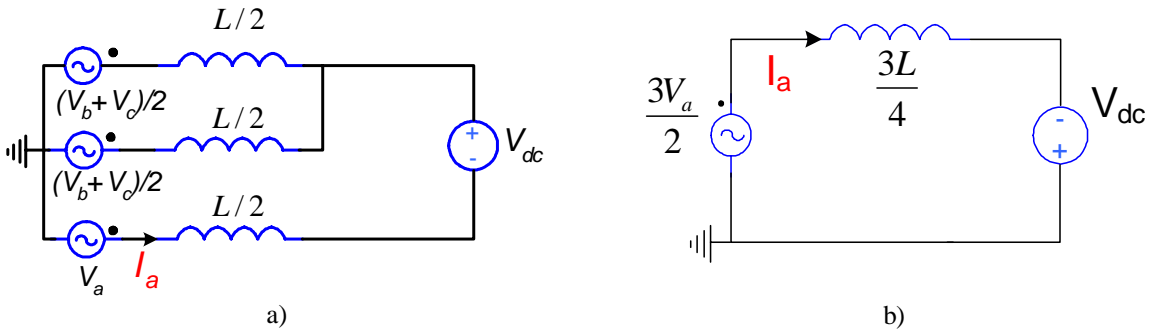
Fig. 89. a) Simplified diagram of the APF with 2 interleaved inverters. b) Equivalent circuit for the current in phase-a.

The following equation represents the current ripple during the states 011 on inverter 1 and state 011 on inverter 2.

$$\Delta i_2 = \frac{(3V_a/2 + V_{dc})\,\Delta t}{3L_F/4} \tag{42}$$

This equation assumes that $V_a = -\hat{V}_a$, since this is the value of V_a on this instant; therefore:

$$\Delta i_2 = \frac{4\left(K_2\hat{V}_a - \frac{3\hat{V}_a}{2}\right)0.25T_s}{3L_F} \tag{43}$$

If $k_1=k_2=2.05$ and replacing in (41) and (43), the ripple is:

$$\frac{\Delta i_1}{\Delta i_2} = \frac{k_1 0.433}{k_2 - 3/2} = 1.61 \tag{44}$$

Consequently, the ratio between the line inductors (1 inverter versus 2 inverters) that gives the same total current ripple is 0.62. For larger power APF the value of k_1 may increase greater than 2.1. On the other hand, when two inverters are used the value of k_2 can be chosen closer to 2. Since the voltage drop across the linkage reactor is reduced. The reason for this is that when multiples inverters are used it will be not necessary to increase too much the value of the dc-bus voltage in order to transfer a higher current to the utility. TABLE X shows a comparison between two active power filters where the same parameters are used. The first column is given for an APF with one single inverter and the second column for 2 interleaved inverters.

TABLE X

SINGLE AND 2-PARALLEL INVERTER COMPARISON PARAMETERS.

Parameters	1 INV	2 INV
Apparent power [KVA]	100%	100%
Line voltage (peak)	1 pu	1 pu
Switching frequency (f_{sw})	$200 \cdot f_0$	$200 \cdot f_0$
Current ripple $\Delta_{i\,max}$	Δi_1	$0.62 \cdot \Delta i_1$
Inductor nominal current (peak)	1 pu	0.5 pu

With the help of Fig. 90 and Fig. 91 it is intended to give more clarity on the advantages of interleaving and the differences on the maximum current ripple Δi. Fig. 90 shows an entire 60 Hz cycle for total active power filter current (the sum of the two inverters contribution) for two-parallel inverters without and with interleaving. The switching frequency is 15 kHz. The red circles on the current waveforms depict the instants when the maximum current ripple occurs. For the case of non-interleaving (Fig. 91.a), the Δi occurs at the zero crossing of the incoming phase-voltage of the same phase of the current. Fig. 91.a shows a zoom of the red circle. It can be seen that the maximum Δi is around 14 A. On the other hand, Fig. 90.b shows an entire 60 Hz cycle of the total APF current with interleaving. The red circle demarks the instant when the maximum Δi occurs for the interleaved case. That instant corresponds to the peak of the phase-voltage of the same phase of the current. The magnitude of the Δi can be extracted from Fig. 91.b which shows a zoom of this instant and it corresponds to approximately 6.5 A . From this figures it can be deduce that not only the magnitude of maximum current ripple Δi is significantly reduced for the interleaved case but that the frequency of the ripple is doubled which ease the efforts on switching-frequency filtering.
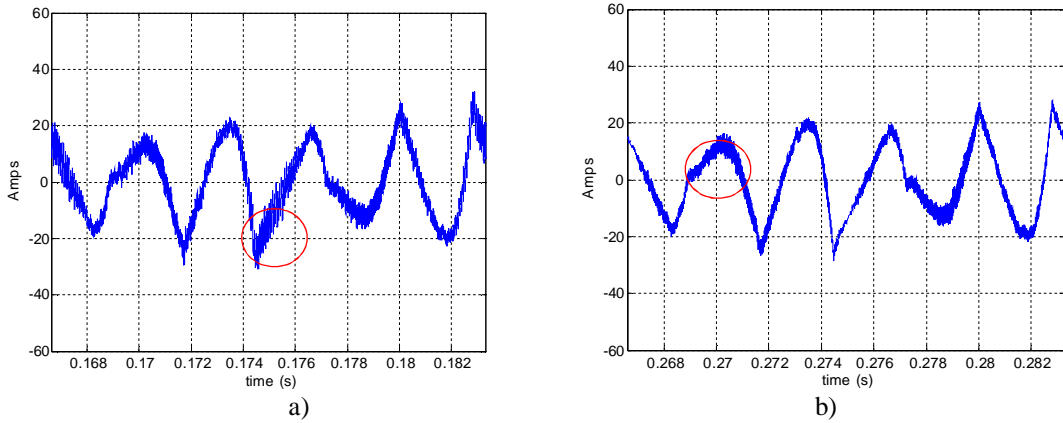
Fig. 90. Entire 60Hz cycle for the total APF current. a) Non-interleaved case. b) Interleaved case.
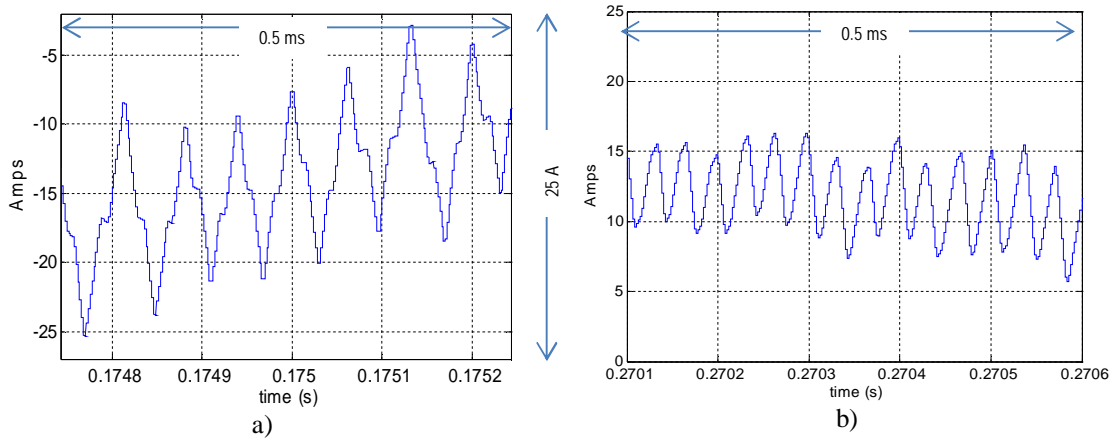
Fig. 91. Instant when the maximum current ripple Δi occurs. a) Non-interleaved case b) Interleaved case.

A comparison of the line current (I_s) THD for different value of linkage inductor when two-inverter APF are used with and without interleaving was conducted. The results are shown in Fig. 92. The harmonic spectrum up to the order 600 was employed for the calculation in order to quantify the impact of the high frequency ripple. The source current THD was always lower for the interleaving case than the non-interleaving case. The difference is even higher for low values of linkage inductance which is the

case pursuing when interleaving. The difference on THD, favoring the interleaving case, fluctuates from 15%, when high inductance used (L_f = 5 mH), up to 60% when low inductance is used. The values of inductance are expressed in mH where 1 mH corresponds to 5% and the switching frequency is 15 kHz.
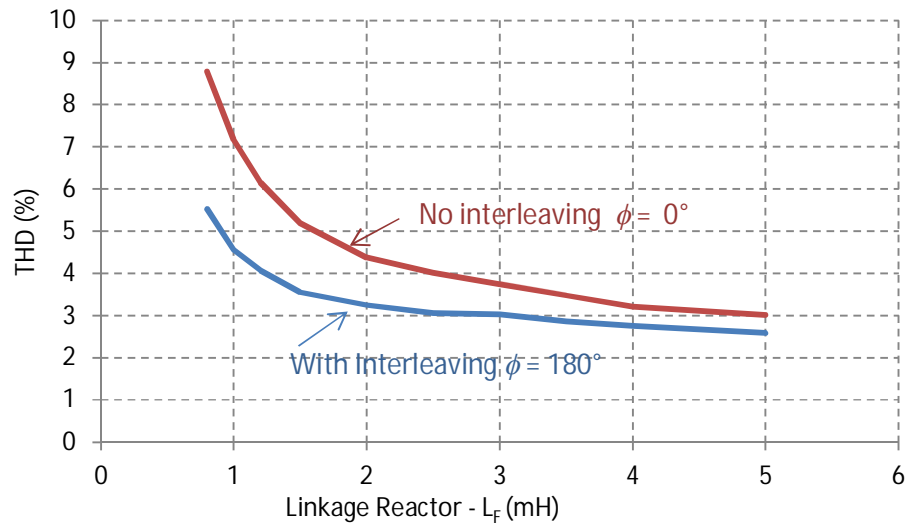
Fig. 92. Input Current THD vs. L_F with and without interleaving

5.5. Analysis of circulation currents

The interleaving of the inverters allows for significant cancellation of the switching frequency harmonics at the ac side however the fact that both, ac and dc side of the inverters are connected leads to the circulation of unwanted currents between them. Since the I_q component is precisely controlled on each inverter, the circulation current corresponds to a zero sequence component (I_z). The incorporation of a zero sequence controller that forces I_z to be equal to zero would eliminate the low frequency

zero-sequence component. However, a zero-sequence component of higher frequency is observed between the inverters, even in the presence of the zero-sequence controller.
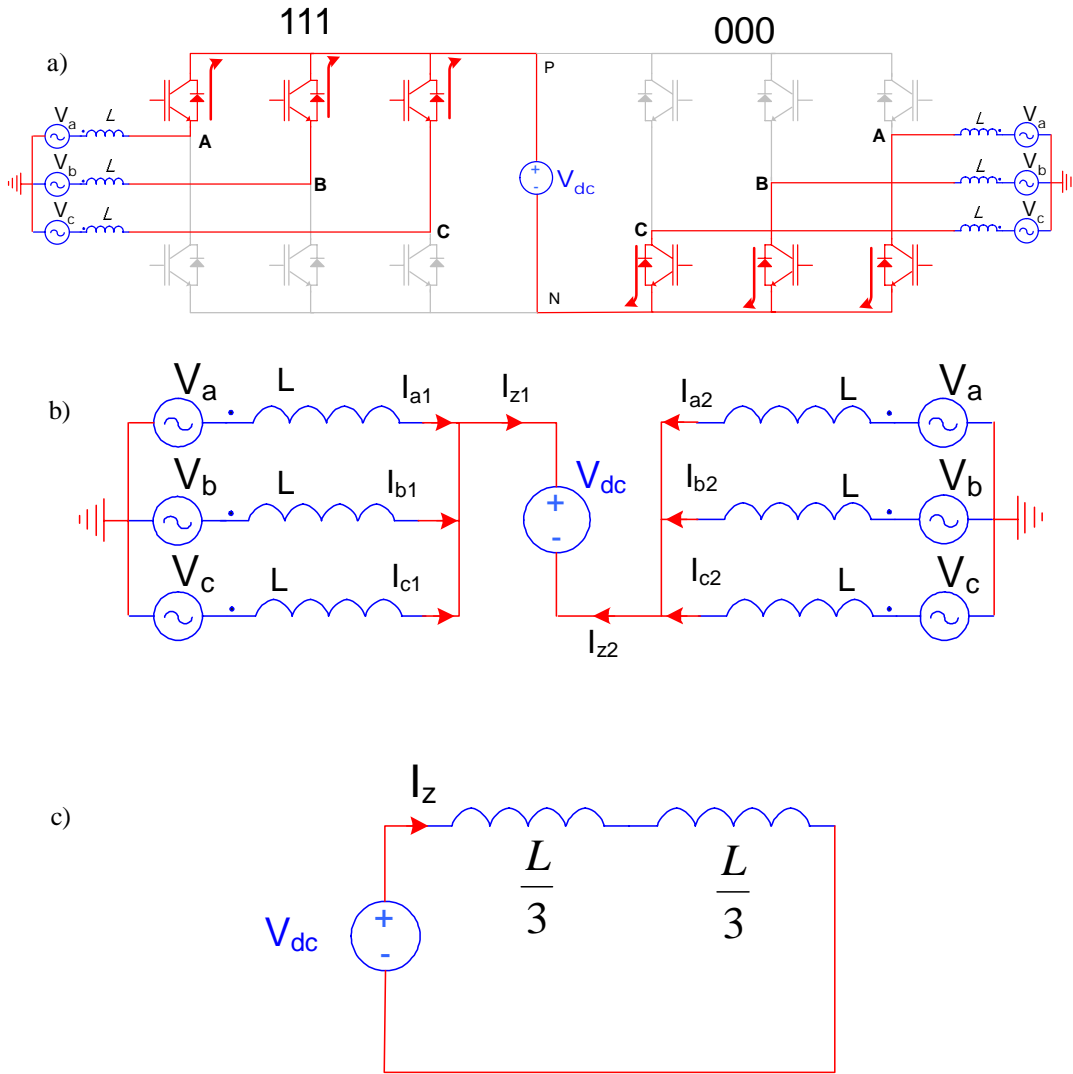
Fig. 93. Equivalent circuit and current path for the zero-sequence current. a) Inverters' zero-sequence current path. b) Inverter equivalent circuit. c) Thevenin's equivalent circuit.

Fig. 93 shows one particular case for the current path for the zero sequence current. The Thevenin's equivalent circuit when inverter 1 is at state 111 (all three input

phases connected to the positive of the dc bus) and inverter 2 is at state 000 (all three input phases connected to the negative of the dc bus) is shown in Fig. 93.c). In the equivalent circuit only the dc bus voltage source is present.

This is true since:

$$V_a + V_b + V_c = 0 \qquad (45)$$

Therefore the zero-sequence current (Fig. 94) of converter 1, I_{z1}, is equal to the negative of the zero-sequence current (I_{z2}) of converter 2.

$$I_{a1} + I_{b1} + I_{b1} = I_{z1} = -I_{z2} \qquad (46)$$

It is clear to see that for states 111 for inverter 1 and state 000 for inverter 2 it will be a circulation of high-frequency current. The magnitude of the zero sequence current will depend on the dc bus voltage magnitude, linkage inductance, and the duration of these two states (t_o). Its frequency will depend on the switching frequency of one inverter. From the equivalent circuit it is possible to deduce the magnitude of the zero-sequence current ripple ΔI_z for this instant as follow:

$$\Delta I_z = \frac{V_{dc}}{2L/3} t_o \qquad (47)$$

Where t_o is the time interval that the states 111 and 000 stay active. Based on observation of multiple simulations it was possible to approximate the value of t_o and the maximum current ripple ΔI_z for the zero sequence current.

$$\Delta I_z = \frac{V_{dc}}{2L/3} t_o \approx \frac{V_{dc}}{2L/3} 0.23 T_s \qquad (48)$$
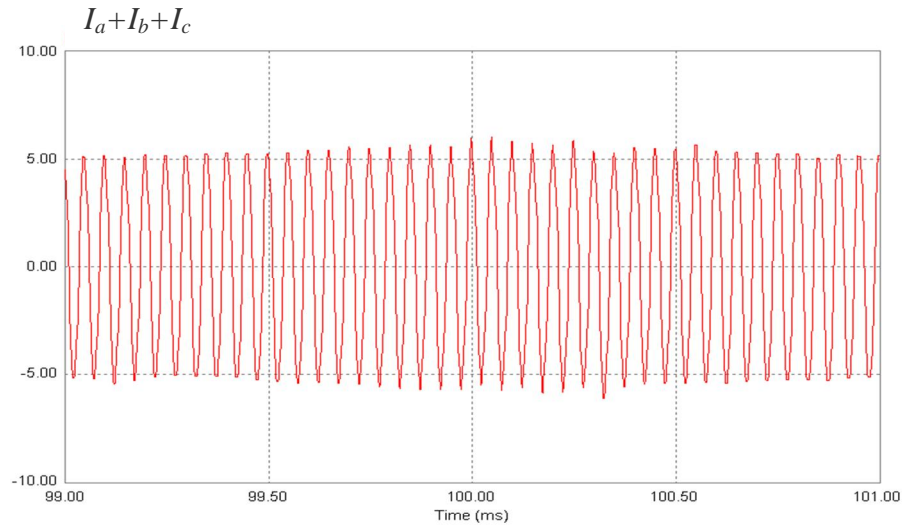
Fig. 94. Inverter's zero-sequence current.

A zero-sequence controller will be proposed to maintain the average zero-sequence current close to zero. However, this controller cannot eliminate the circulation of this high frequency current. Therefore, a common mode inductor will be proposed to mitigate the peak value of the high-frequency zero-sequence current. A common mode inductor will present inductive impedance only when the sum to the three phase currents of each inverter (Ia1, Ib1, Ic1) differs from zero. In principle, it is only necessary to add a common mode inductor to only N-1 inverters (where N is the number of inverter). Since the total zero-sequence current will cancel out (add to zero) at the point of common coupling. Fig. 95 shows a typical construction of a three-phase common mode choke by using single toroidal core (courtesy of VAC). The three phases are wound around the core such that they all generate a magnetic flux pointing at the same direction. If no zero-sequence current present, the sum of three current and therefore

magnetic flux will be zero. On the other hand, if the sum is not zero, a resultant magnetic flux will be induced and then an impedance will be developed.
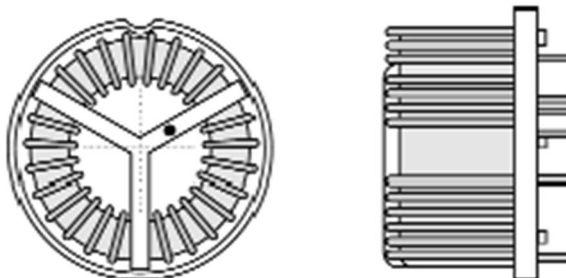
Fig. 95. Common-mode choke – VAC [103].

Fig. 96 shows the APF approach with the additional common mode chokes, also called zero-sequence blockers (ZSB). The ZBSs are shown on each inverter in order to avoid losing modularity on the construction.
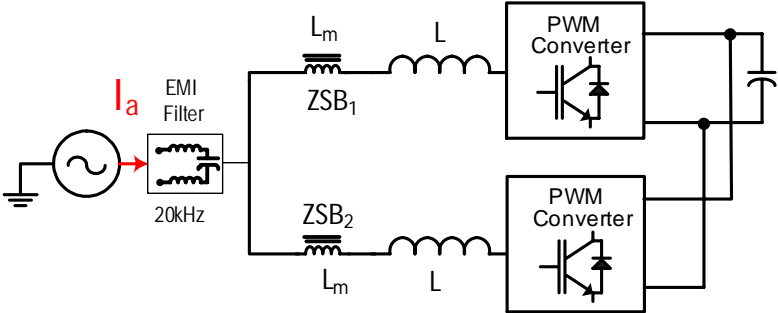
Fig. 96. Interleaved APF with common mode choke (ZBS-zero sequence blocker).

Other benefit of the interleaved connection is the fact that when APF supplies only reactive power, the RMS value of the dc current flowing through the dc link

capacitor is significantly reduced. The reduction of the dc rms current will reduce the heat and increase the life time of the dc bus capacitors. Electrolytic capacitors, commonly used in dc links, due to its high energy density, can be benefited by the utilization of interleaved structures.

Fig. 97 shows the current through the dc bus capacitor (I_c) when using interleaving. The rms value is 6.26 A, and its mean value is zero. Similarly, Fig. 98 shows the current through the dc bus capacitor for the same system but without interleaving. The rms value of I_c is 11.39 A and its mean value is also zero. The current for the interleaving case is almost 50% smaller than without interleaving.
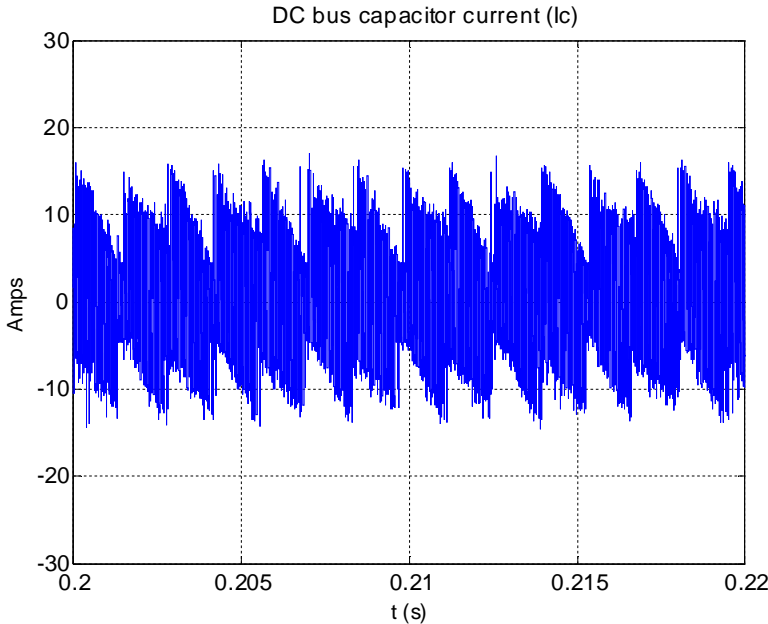
Fig. 97. APF dc bus capacitor current Ic with interleaving. I_{c_rms}=6.26A.
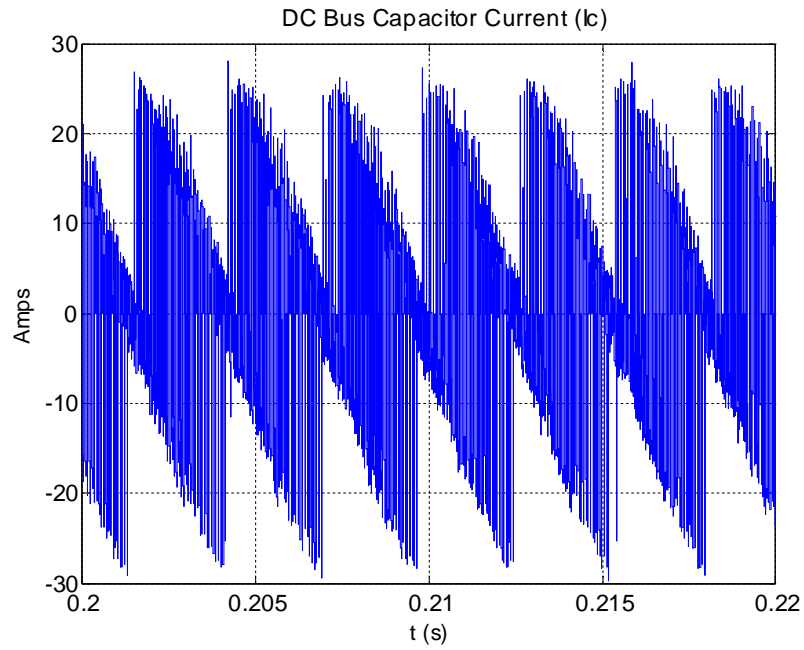
Fig. 98. APF dc bus capacitor current Ic without interleaving. I_{c_rms}=11.39A.

Fig. 99 shows the current contribution (Ic1, Ic2) of each inverter to the dc bus capacitor current for the interleaving case.
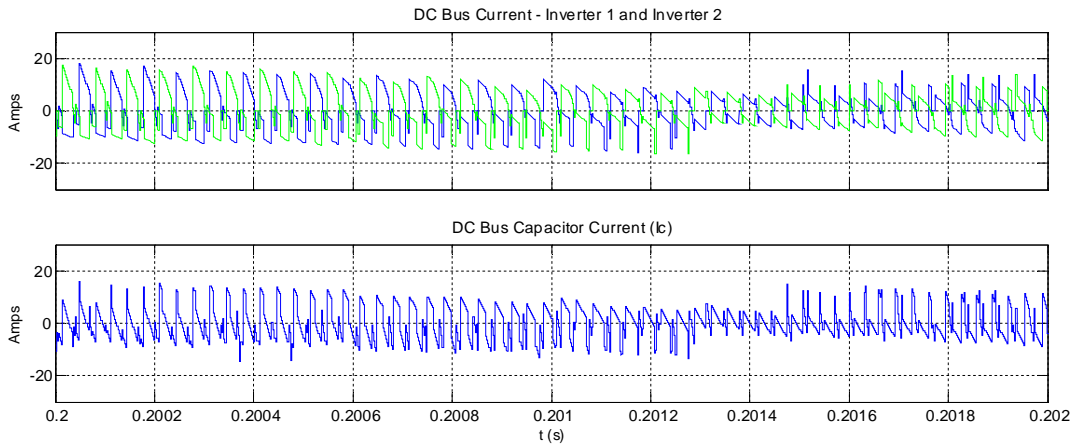
Fig. 99. Inverters dc currents I_{c1} and I_{c2} (top). Dc bus capacitor current Ic.

Fig. 100 shows the current harmonic spectrum of the dc bus capacitor current for single-inverter and Fig. 101 the current harmonic spectrum for the dual-interleaved-inverter case when the switching frequency is 15 kHz. The rms current is reduced in half for the interleaved dual case and the characteristic harmonics are shifted to multiple of twice the switching frequency. This will reduce the heat and losses in the capacitor thus contributing to improvements in the overall efficiency and power density. Fig. 102 and Fig. 103 show the dc bus capacitor current harmonic spectrum for similar scenario when the switching frequency is 4920 Hz.
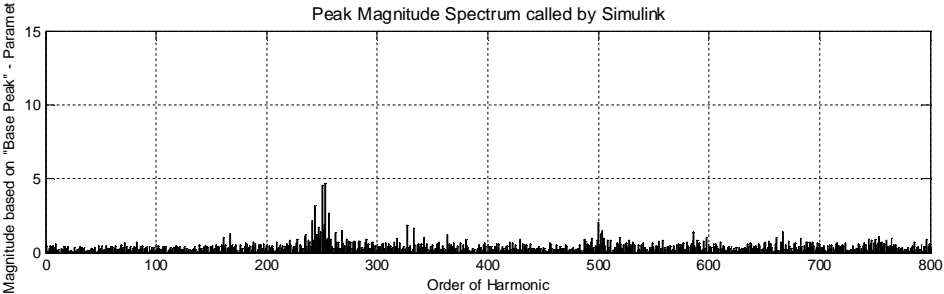
Fig. 100. Harmonic spectrum of dc capacitor current for Single inverter APF (f_{sw} =15 kHz).
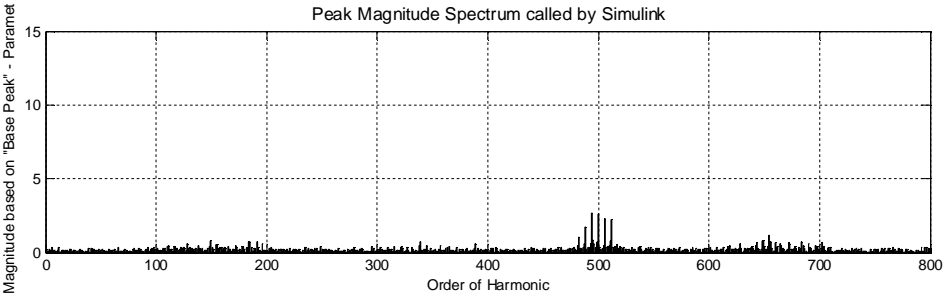
Fig. 101. Harmonic spectrum of dc capacitor current for dual-Interleaved-inverter structure (f_{sw} =15 kHz).

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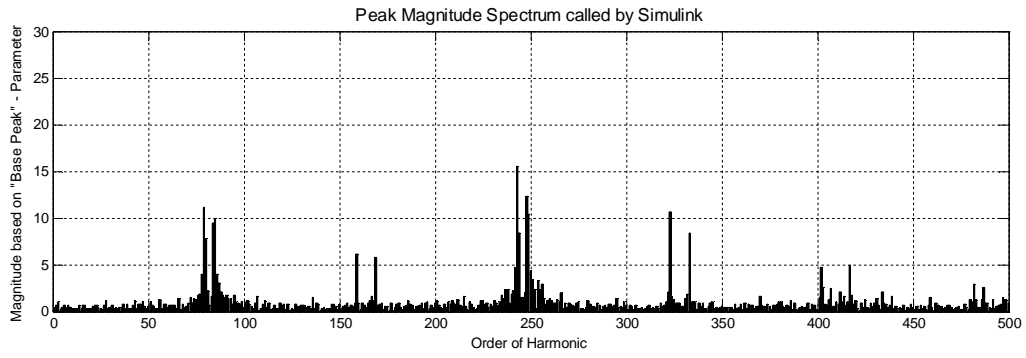
Fig. 102. Harmonic spectrum of dc capacitor current for Single inverter APF (f_{sw}=4920Hz). Ic_rms=1 p.u.
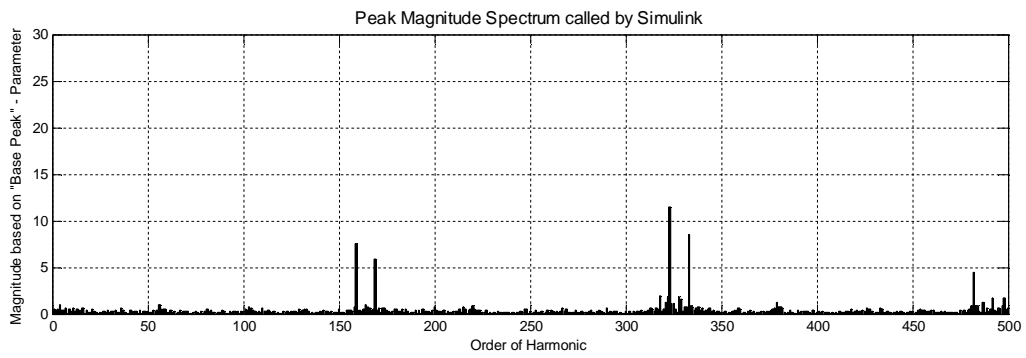
Fig. 103. Harmonic spectrum of dc capacitor current for dual-interleaved-inverter structure (f_{sw}=4920Hz). Ic_rms=0.5p.u.

5.6. Simulation Results

Simulations results using MATLAB/SIMULINK SimPower-Systems toolset were obtained for a 480V / 60Hz supply and a 30kW six pulse rectifier non-linear load when a two-inverter interleaved shunt APF is compensating for current harmonics. The control schemes for invert 1 and inverter 2 are shown in Fig. 104 and Fig. 105 respectively. The scheme is based on a load current detection method.

Fig. 104. Control block diagram for interleaved inverter 1.

Fig. 105. Control block diagram for interleaved inverter 2.

A synchronous reference frame used to control the APF current of each inverter [104]-[108]. The load and filter currents are transformed to *dqz* components through the conventional park transform.

$$
\begin{bmatrix} I_d \\ I_q \\ I_z \end{bmatrix} = \begin{bmatrix} \frac{2}{3}\mathbf{sin}(\varpi t) & \frac{2}{3}\mathbf{sin}(\varpi t - \mathbf{2}\pi/\mathbf{3}) & \frac{2}{3}\mathbf{sin}(\varpi t + \mathbf{2}\pi/\mathbf{3}) \\ \frac{2}{3}\mathbf{cos}(\varpi t) & \frac{2}{3}\mathbf{cos}(\varpi t - \mathbf{2}\pi/\mathbf{3}) & \frac{2}{3}\mathbf{cos}(\varpi t + \mathbf{2}\pi/\mathbf{3}) \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}
$$

Fig. 106. Park's transform.

A quadrature PLL is used to synchronize with the grid's voltage obtaining *sin(wt)* and *cos(wt)*. The load currents are filtered in order to obtain the current harmonics components which will be used as a reference for the APF. The I_d component is modified by the output of the dc bus voltage controller and it is compared with the APF's current I_f in order to obtain the current error. A PI controller is used to reduce error to zero. Similar process is followed for the I_q component with exception that the I_q component is not modified by the dc bus voltage controller.

A resonant controller (REZ 6th) tuned to the 6th harmonic is used in order to improve the performance of the *d* and *q* current controllers. This resonant controller help to compensate for the 5th and 7th harmonic since those frequencies are represented as a single harmonic (6th) in the *dqz* synchronous frame.

Before transforming the load current I_L and the APF current (I_f) to *dqz* components, they are divided by two since two converters are in parallel and naturally the harmonic reference for each inverter must be half the total load-harmonic current.

Only one dc bus capacitor voltage controller is used and its output is also divided by two and added to the I_d component reference.

A controller for the zero-sequence component is added for inverter 1. In general this controller will be used on N-1 parallel inverters. The objective is to maintain the average value of the zero-sequence component close to zero.

The outputs of the *d*, *q* and *z* current controllers are transformed back to *abc* components by using the Park's inverse transform and then a zero-sequence vector is added in order to converter from SPWM to SVM equivalent and provide inverter voltage gain close to unity.

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} \sin(\varpi t) & \cos(\varpi t - 2\pi/3) & 1 \\ \sin(\varpi t - 2\pi/3) & \cos(\varpi t - 2\pi/3) & 1 \\ \sin(\varpi t + 2\pi/3) & \cos(\varpi t + 2\pi/3) & 1 \end{bmatrix} \begin{bmatrix} I_d \\ I_q \\ I_z \end{bmatrix}$$

Fig. 107.Inverse Park's transform.

Results while compensating the 6-pulse rectifier are shown in Fig. 108. The input current THD is 33% before compensation and it goes down to 2.3% during compensation (at instant 0.1s).
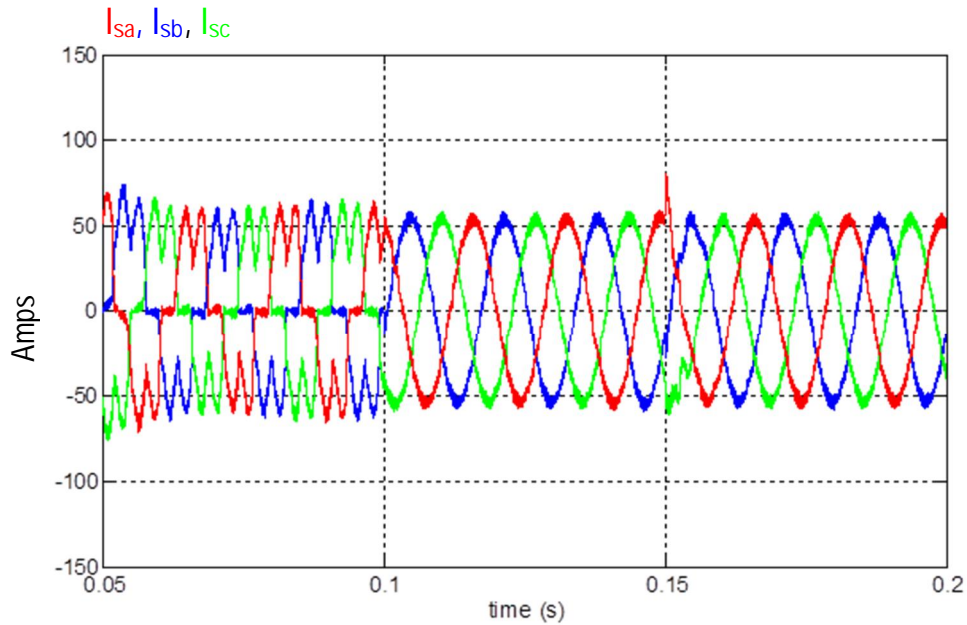
Fig. 108. Input current waveforms for APF compensation with two interleaving inverters. Compensation starts at 0.1s.

In order to demonstrate the effectiveness of the zero-sequence controller, the APF started to compensate at 0.1s without the zero-sequence controller enabled. The zero sequence currents diverge until instant 0.15s when the zero-sequence controller is enabled. Fig. 109 shows the zero-sequence current before and after the controller is enabled.
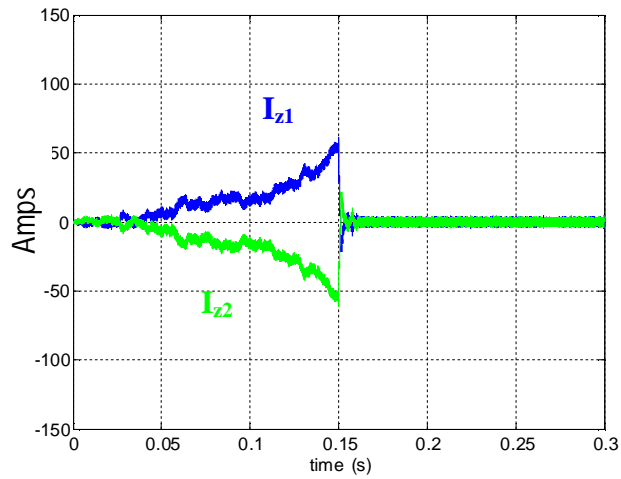
Fig. 109. Zero sequence currents of each inverter before and after the zero sequence controller starts (at 0.15s).

The ac side current contribution of each inverter is shown in Fig. 110. The current of each inverter presents a dc component of equal magnitude but opposite sign for the same case of Fig. 109.
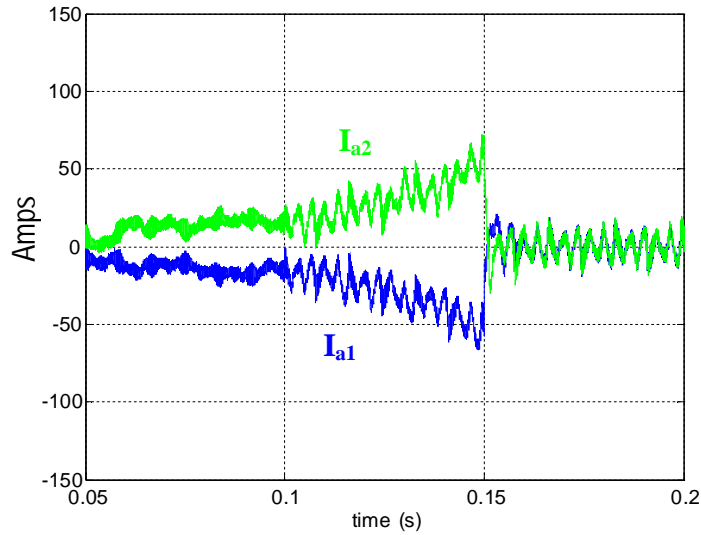
Fig. 110. Compensating APF currents (I_{f_a1} and I_{f_a2}). Before and after compensation

The total APF's current is shown in Fig. 111. Although, the currents from inverter 1 and inverter 2 have the some dc components before the zero-sequence controller starts operating, the total sum of the two current does not have a dc component. The reason for this is that the zero sequence component of inverter 1 is equal to the negative to the zero-sequence component of inverter 2 so they cancel out.

Since the system is a 3-wire system, there is no path for the zero-sequence current going to the 3-phase source.
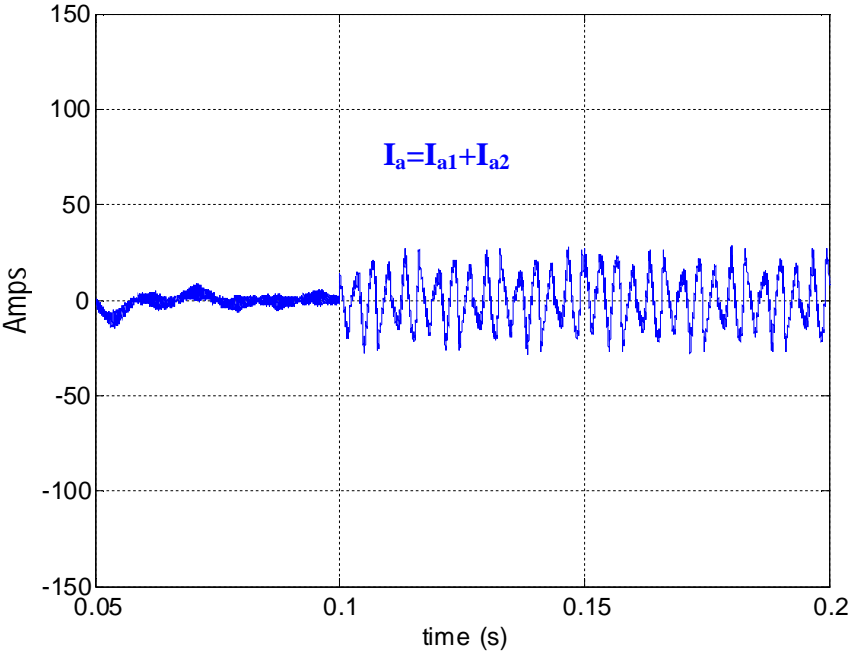
Fig. 111. Interleaved APF's filter total current.

5.7. Experimental Results

In order to validate the theoretical analysis and simulations, experimental results were obtained in collaboration with the University of Aalborg on a 400 V, 5 kVA 6-pulse nonlinear load. Two commercial inverters were used and controlled with a dSpace system based on a TMS320F240 DSP.

A typical synchronous reference APF control algorithm was used as shown in Fig. 112. It contains an outer slower dc voltage loop and an inner faster current loop which is reinforced by a resonant controller tuned for the 6th harmonic.
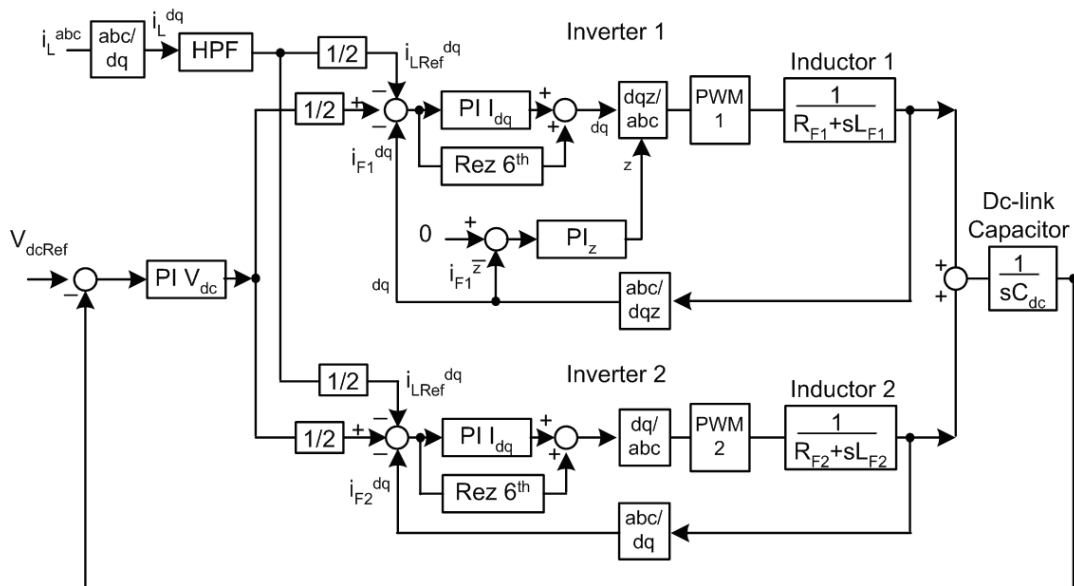
Fig. 112. Control scheme for dual interleaved inverters

The load current is measured and the harmonic currents are extracted by low pass filters divided in half and imposed as current reference for each inverter. As both inverters use the same dc-capacitor there is one single voltage control loop. The output

of the voltage controller is equally divided to be the reference for both inner current controllers. This creates a balance in the power losses dissipation for both inverters and also assures closer symmetry in the voltage references for each inverter, which is needed in order to have a good cancellation in the current ripple.

The lab setup is shown in Fig. 113 depicting the two inverter, linkage reactor, common mode chokes and control platform. The unit was tested with a 6-pulse diode rectifier load.
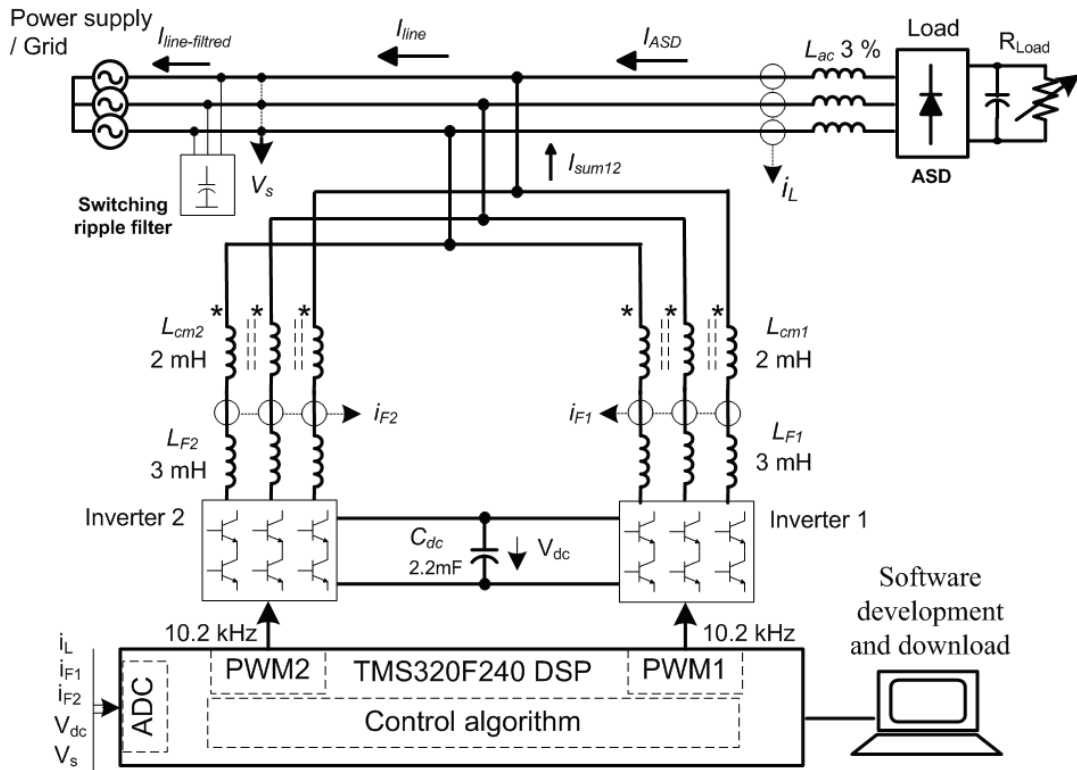
Fig. 113. Lab setup for interleaved inverters based APF.

Fig. 114 shows each inverter current and the overall APF current when only reactive power is injected. The current of each inverter has some evident ripple which is reduced at the point of the inverters connection (signal in blue). The circulation current (signal in green) is also shown with and RMS value of 3.6 A. Without loss of generality, the maximum current ripple of the circulation current can be expressed as :

$$\Delta i_{cc}(t) = \frac{V_{dc}}{L_{f1} + L_{f2} + L_{cm1} + L_{cm2}} t_0(t)$$
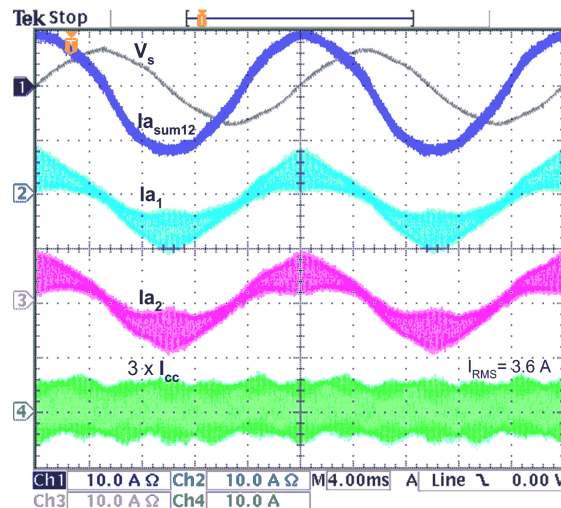
Fig. 114. Without a common mode coil. Sinusoidal current reference

If a common mode inductor is added to each inverter, the circulation current can be reduced to 2.6 A as shown in Fig. 115.
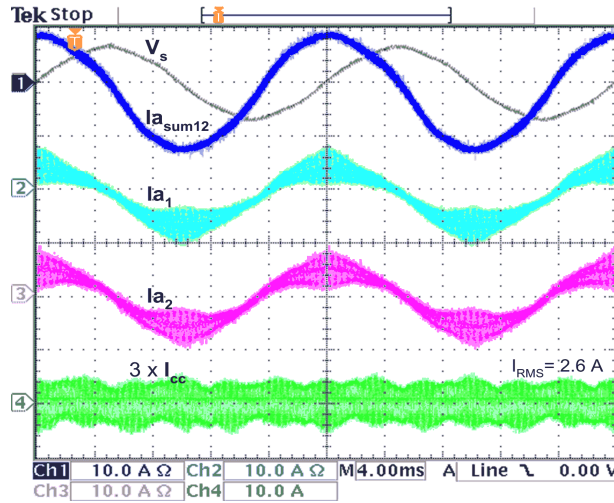
Fig. 115. With a common mode. Sinusoidal current reference coil of 2mH.

In this case the maximum current ripple of the circulation current can be expresses as.

Fig. 116 shows the APF when compensating the 6-puse diode rectifier. Each inverter contributes with half the APF's current. A current ripple of approximately 33% on each inverter is observed which is reduced in half after the current are added up.
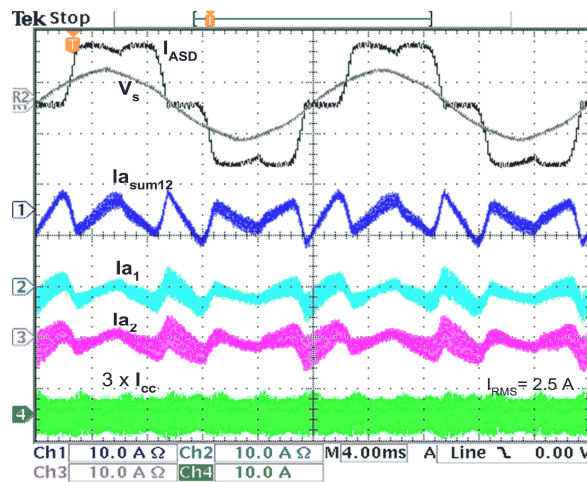
Fig. 116. APF current for harmonic compensation. With a common mode Harmonic current reference coil of 2mH.

Fig. 117 shows the supply current for the interleaved APF when compensation a non-linear load. The load THD is 27% and it is brought down to 2% at the supply side after a switching frequency filter was added.
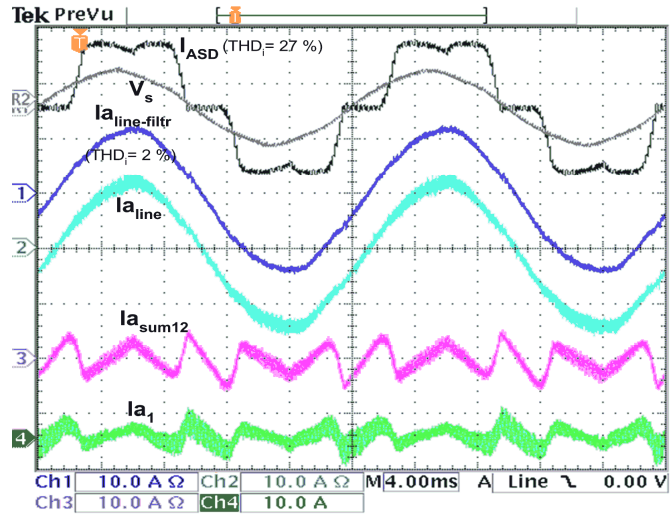
Fig. 117. Measured waveforms. APF efficiency of reducing the switching ripple by interleaving two inverters.

5.8. Conclusions

This part of the work discusses the advantages of two interleaved inverters connected in parallel and sharing the same dc capacitor for reactive power and current-harmonic compensation. Design specification analysis shows that the values of the passive components can be significantly reduced. The intrinsic modularity characteristic of the topology increases the reliability and makes it suitable for high-current applications. Simulation results and experiments validated the presented analysis. The usage of smaller line inductors and the replacement of the isolation transformer with

common mode coils allows for lower costs and high performance, which makes the topology very attractive for high-power industrial APFs.

CHAPTER VI

CONCLUSIONS

6.1. Conclusions

Current harmonics in electrical distribution systems continue to be a great concern among electrical engineers. Large current non-linear loads such as adjustable speed drives used in milling processes and pumping, rectifiers for electro-wining applications, high voltage dc transmission systems and converters, used in the ever increasing distributed energy source market such as wind and solar, could not operate without incorporating effective harmonics mitigation methods. Lower cost, higher power density, higher efficiency and high performance over a broader range of operating conditions are the main drivers for developing new topologies for harmonics mitigation devices. In this work an analysis of a high power density asymmetric 18-pulse rectifier operating under unbalance and pre-existing voltage harmonic distortion was performed. It was found that small variance on the input voltage supply could generate large deviations on the harmonic mitigation performance. On a worst case scenario, a 3% voltage unbalance could increase the input current THD to 33% from an 8.7% on the absence of unbalance. Similarly, if there is pre-existent voltage distortion of 2.5% at 5th harmonic on the incoming voltage, the current THD could increase up to 37%.

A reduced kVA active power filter was introduced to resolve these issues and provide lower THD under unbalance and voltage distortion conditions. By means of simulations a current THD lower than 4% was obtained when the APF was operating for

these harsh voltage conditions. The kVA rating of the APF could be selected to be 20-25% of the load kVA rating by limiting the current compensation for a load with a THD lower than 25%.

During the absence of abnormal voltage conditions, the APF can enhance the performance of the asymmetric 18-pulse rectifier and achieve a theoretical input current THD lower than 2%.

A simple control strategy based on obtaining the incoming phase voltages as current reference templates was used in order to control the APF under abnormal voltage conditions. This control scheme makes the asymmetric 18-pulse rectifier be seen as a purely resistive load from the source side.
Simulations and experimental results on 480V/30kW system were obtained in order to validate the analysis.

On the other hand, a modular structure based on interleaved two-level inverters in order to realize a high-power density APF was investigated. Although, the topology per se, is not new, its application for active harmonic filtering has not been extensively reported. The analysis was based on two 2-level inverters connected in parallel with the dc-bus directly connected and the ac side connected through line reactors. It was found that maximum current ripple is reduced to about 62% when two interleaved inverters are used for the same value of linkage inductance L_F and identical other parameters. These findings lead to determine that the relationship between the linkage inductor of a single-inverter APF and 2-interleaved inverters APF that produces the same maximum current ripple is about 3. In other words, when using a single-inverter APF, the linkage

inductance has to be 3 times bigger than the inductance of the 2-interleaved inverters case in order to limit to maximum current ripple to the same value. These results have a significant impact on the volume and weight of the linkage inductor and ac switching-frequency filter of APFs, therefore enabling the increase of the power density of APFs. Moreover, since interleaved-inverter based APFs can lead to smaller linkage inductors and ac filters, it is possible to infer that the dynamic response of the APF can be improved by the use of this approach.

A zero-sequence controller was introduced on the *dqz* synchronous reference frame in order to mitigate the development of zero-sequence current or circulating current amount the parallel inverters. This zero-sequence controller cannot mitigate the zero-sequence current generated at the switching frequency, therefore common mode inductors connected at the ac input of each converter are proposed. The common mode inductors present an inductance when the sum of the three-phase currents of each inverter differs from zero, therefore reducing the magnitude of the peak of the zero-sequence high-frequency current.

The analyzed approaches can contribute to the future of active harmonic mitigation technology. Nevertheless, more research is foreseen in order to enable the development of cost effective current harmonic mitigation approaches with high power density, high efficiency and high performance over a wide range of operating conditions.

6.2. Suggestions for future work

Future work can be done on the search of modular, cost effective, high-power density structures to realize APFs to compensate high-current non-linear loads. The

interleaved-inverter based approach can be extended to interleaving multilevel structures which could enable further reduction of the linkage reactor and ac filters and achieve higher voltage levels. Higher number of interleaved inverters can be connected in parallel in order to reach higher current levels. These structures can enable the use of lower current rating sub-inverter-modules which can be realized with faster and less-lossy switching devices. The advent of SiC switching devices can enable higher voltage levels and even higher efficiencies. On the other, the practical limitations as far as how many units can be interleaved or what is the maximum numbers of levels per module are not really known as well as the optimal control architectures in order to control these multi-module interleaved structures with the minimum computational resources.

These structures not only can be used for active power filtering purposes but, also to enable high power density grid-interface converters to harness the energy of renewables sources such as those from the sun and wind.

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APPENDIX A

Asymmetric 18-pulse rectifier with Active Filter electric schematic.
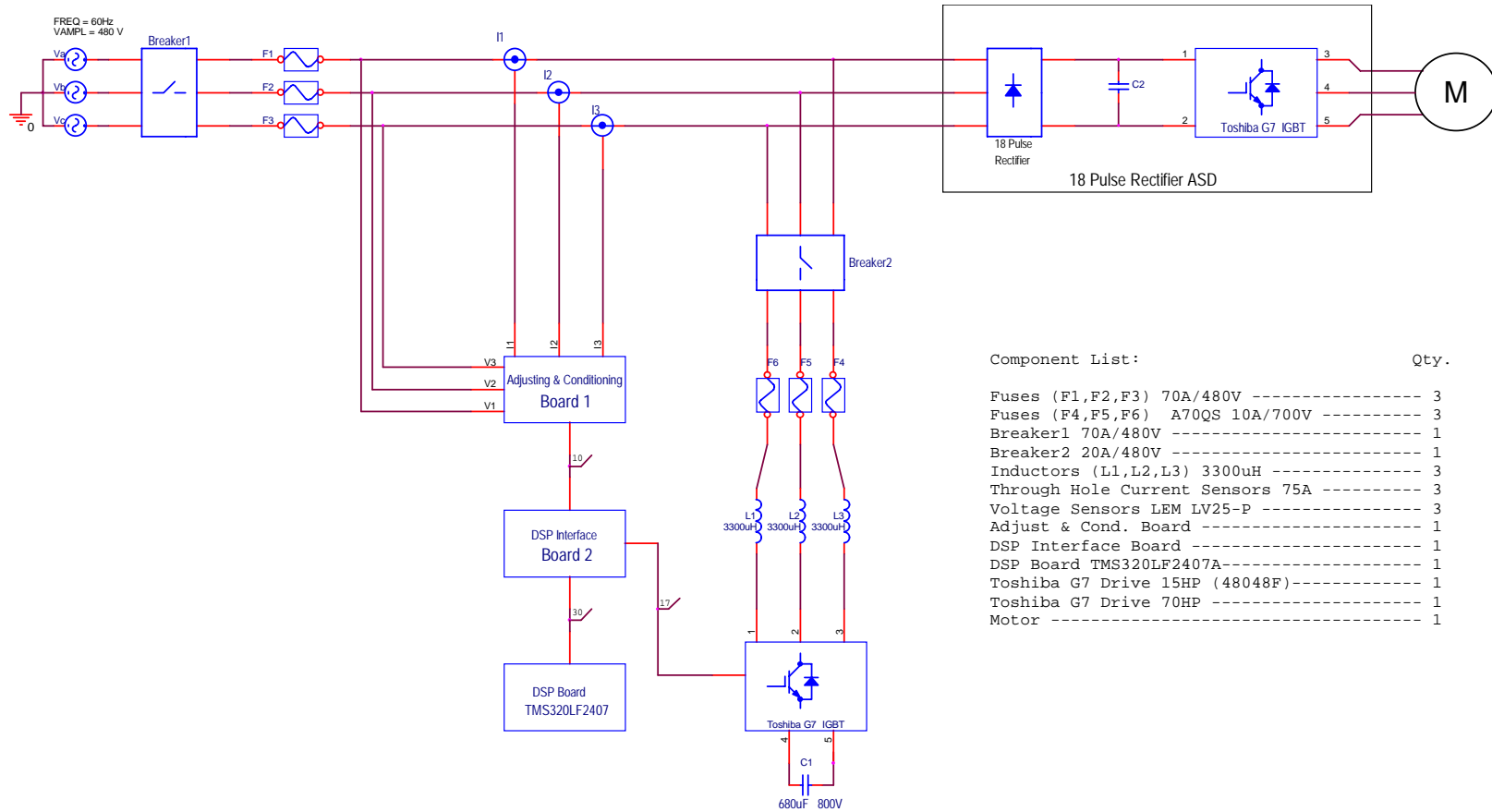
```
Component List:                                             Qty.

Fuses (F1,F2,F3) 70A/480V ------------------ 3
Fuses (F4,F5,F6)  A70QS 10A/700V ---------- 3
Breaker1 70A/480V ------------------------- 1
Breaker2 20A/480V ------------------------- 1
Inductors (L1,L2,L3) 3300uH --------------- 3
Through Hole Current Sensors 75A ---------- 3
Voltage Sensors LEM LV25-P ---------------- 3
Adjust & Cond. Board ---------------------- 1
DSP Interface Board ----------------------- 1
DSP Board TMS320LF2407A-------------------- 1
Toshiba G7 Drive 15HP (48048F)------------- 1
Toshiba G7 Drive 70HP --------------------- 1
Motor ------------------------------------- 1
```
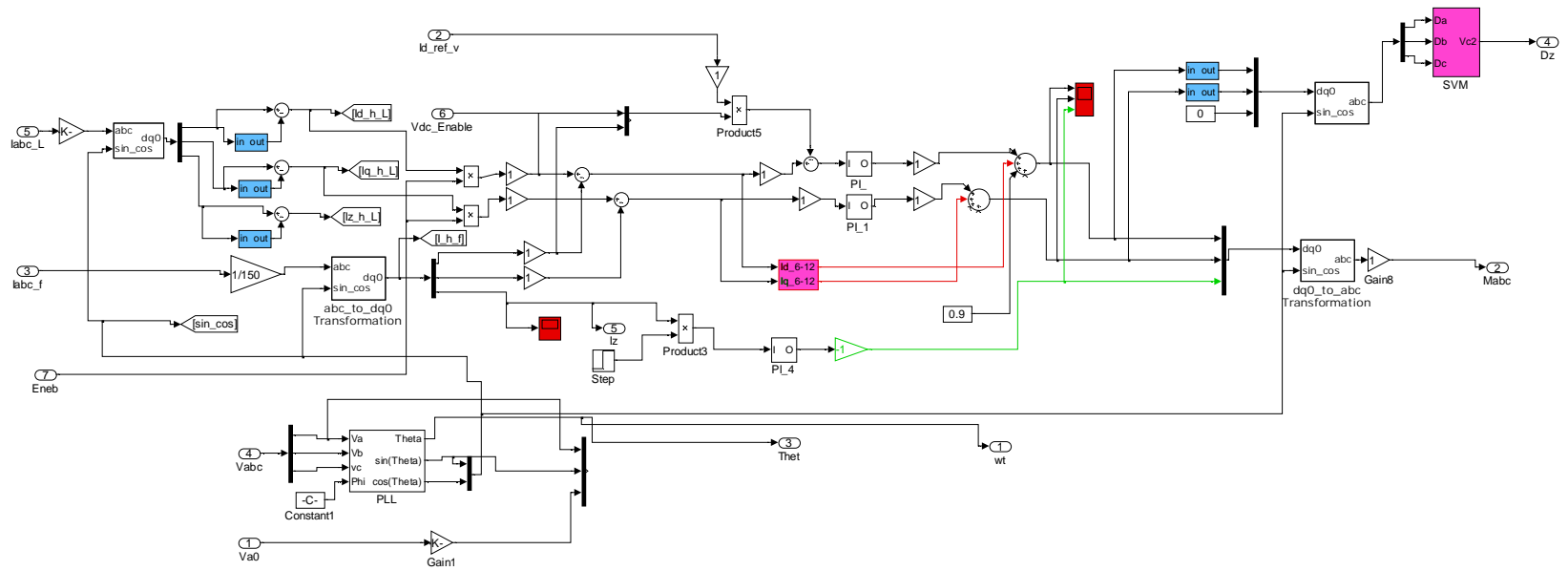
APPENDIX B

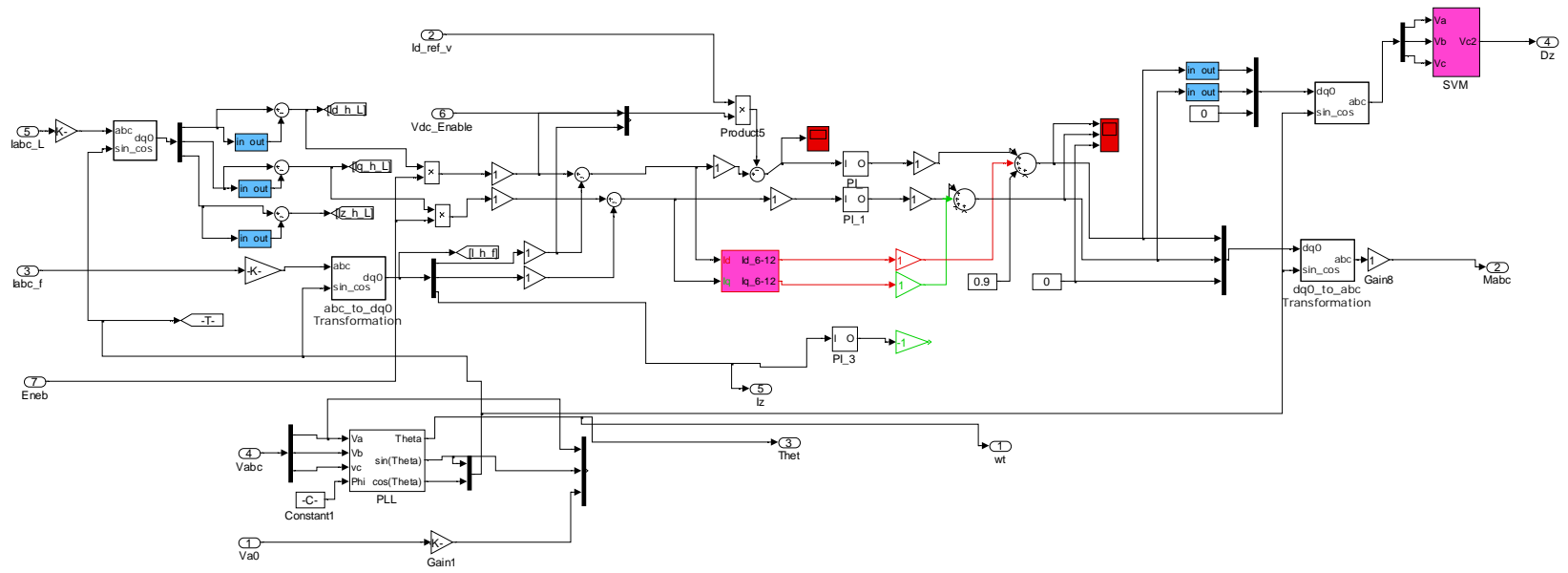## Matlab/Simulink Simulation Model of 2-interleaved inverters APF
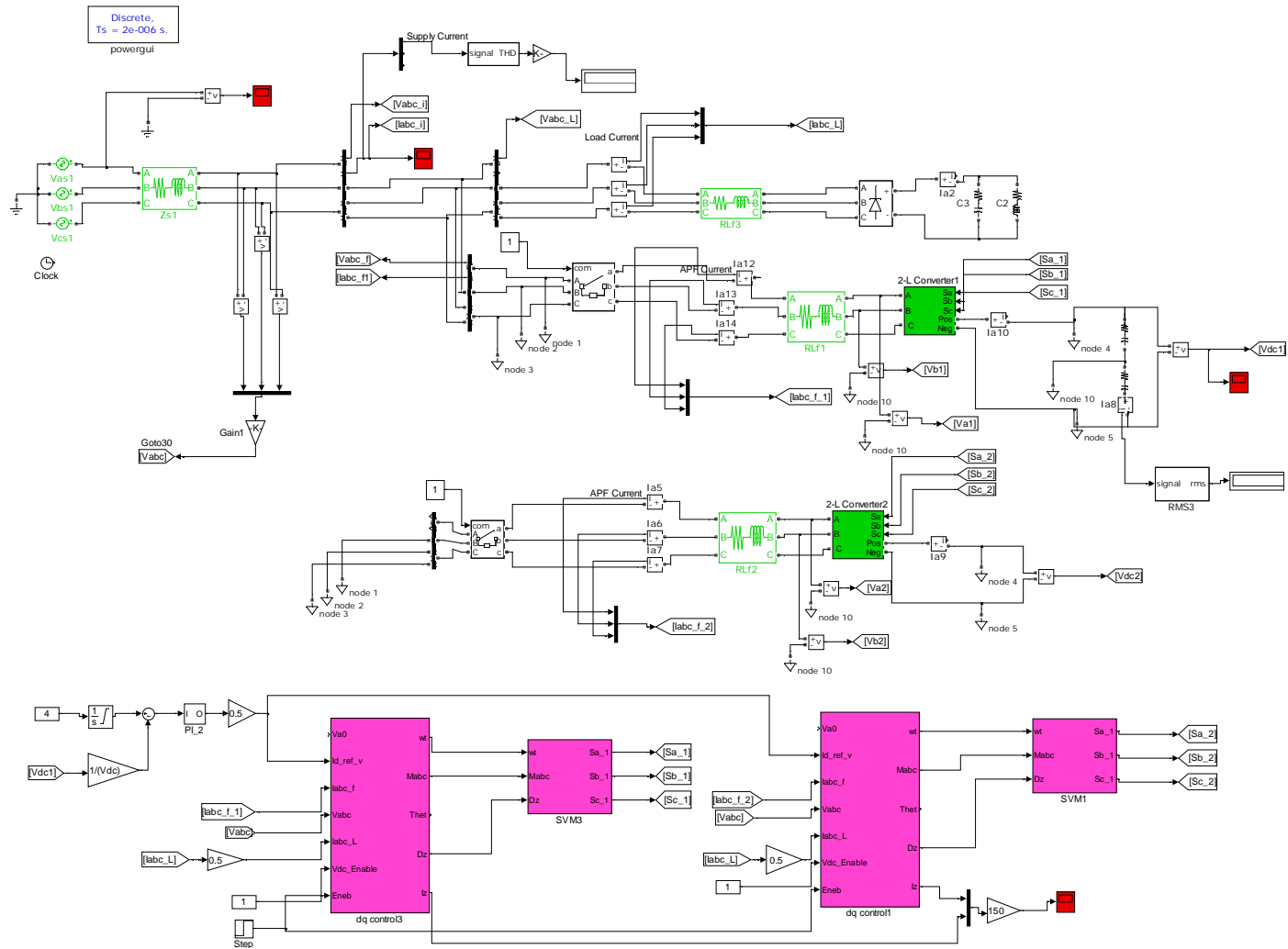
Matlab/Simulink "dq control" control scheme of Interleaved Inverter 1

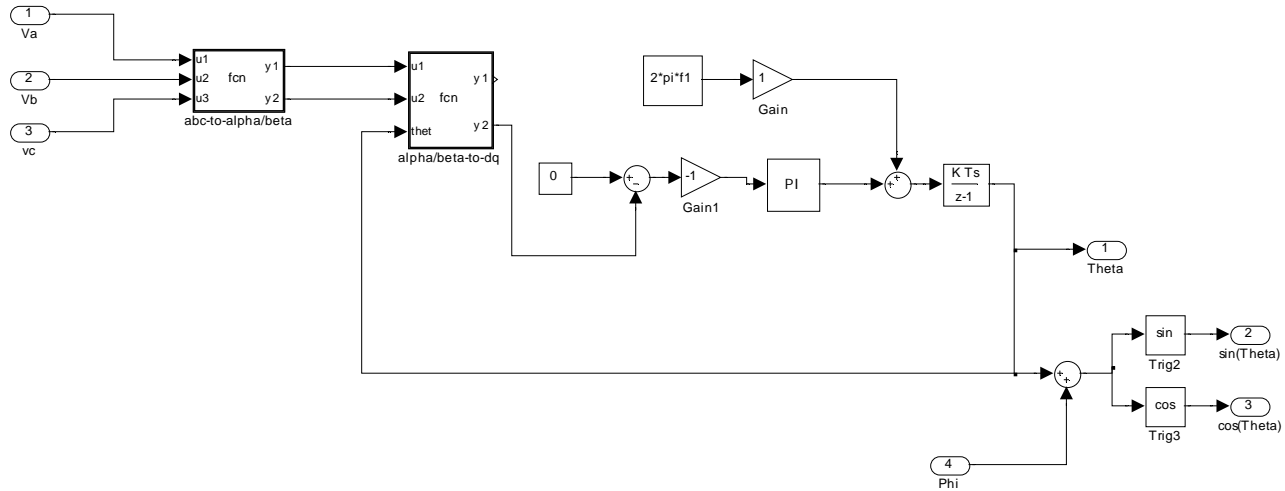# Matlab/Simulink "dq control" control scheme of Interleaved Inverter 2

PLL block

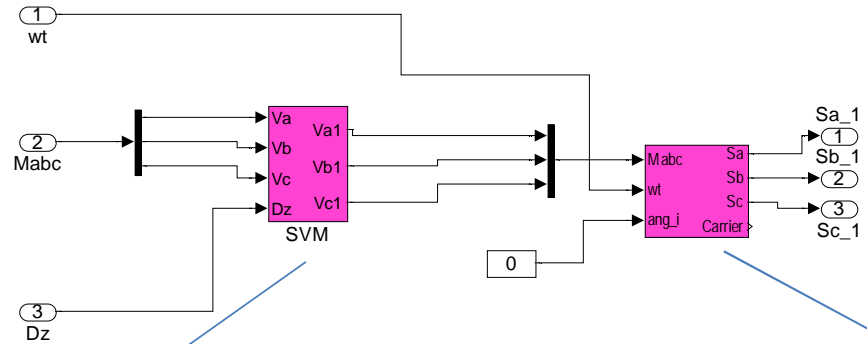**abc-to-alpha/beta block**
```
function [y1, y2]= fcn(u1,u2,u3)
%#eml

y1 = (2/3)*(u1-0.5*u2-0.5*u3);
y2 = (2/3)*(-0.5*sqrt(3)*u2+0.5*sqrt(3)*u3)
```

alpha/beta-to-abc block
```
function [y1, y2]= fcn(u1,u2,thet)
%#eml

y2 = u1*cos(thet)-u2*sin(thet);
y1 = u1*sin(thet)+u2*cos(thet);
```

SVM1 & SVM3