ZIRCONIUM-DOPED TANTALUM OXIDE HIGH-K GATE DIELECTRIC FILMS

A Dissertation

by

JUN-YEN TEWG

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2004

Major Subject: Chemical Engineering

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Approved as to style and content by:

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ABSTRACT

Zirconium-Doped Tantalum Oxide High-k Gate Dielectric Films.

(December 2004)

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Chair of Advisory Committee: Dr. Yue Kuo

A new high-k dielectric material, i.e., zirconium-doped tantalum oxide (Zr-doped TaO_x), in the form of a sputter-deposited thin film with a thickness range of 5-100 nm, has been studied. Important applications of this new dielectric material include the gate dielectric layer for the next generation metal-oxide-semiconductor field effect transistor (MOSFET). Due to the aggressive device scaling in ultra-large-scale integrated circuitry (ULSI), the ultra-thin conventional gate oxide (SiO_2) is unacceptable for many practical reasons. By replacing the SiO_2 layer with a high dielectric constant material (high-k), many of the problems can be solved. In this study, a novel high-k dielectric thin film, i.e., TaO_x doped with Zr, was deposited and studied. The film's electrical, chemical, and structural properties were investigated experimentally. The Zr dopant concentration and the thermal treatment condition were studied with respect to gas composition, pressure, temperature, and annealing time. Interface layer formation and properties were studied with or without an inserted thin tantalum nitride (TaN_x) layer. The gate electrode material influence on the dielectric properties was also investigated. Four types of gate

materials, i.e., aluminum (Al), molybdenum (Mo), molybdenum nitride (MoN), and tungsten nitride (WN), were used in this study. The films were analyzed with ESCA, XRD, SIMS, and TEM. Films were made into MOS capacitors and characterized using I-V and C-V curves. Many promising results were obtained using this kind of high-k film. It is potentially applicable to future MOS devices.

For my dearest Mother, Father, Brother, and Linda

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CHAPTER I

INTRODUCTION

1.1 Background

1.1.1 Challenges for Sub-100 nm ULSI Technologies

Since the dawn of semiconductor industry, continuous efforts have been made to increase the number of devices on the same chip area. Two major benefits are gained: cost reduction of fabrication and improvement of device performance.[1] The fabrication cost reduction is due to roughly the same cost to fabricate one wafer regardless of the number of devices on it. Increasing the wafer size and decreasing the device size, i.e., scaling, are reasonable approaches.[2] As for device performance, the shrinkage of the MOSFET gate length results in a higher drive current.[1] The drive current (on-current) is the figure of merit while scaling down the device. This on-state transistor current (I_D) is approximately modeled as,[3]

$$I_D = (W/L)\mu_n C'_{ox}(V_{GS} - V_{th})V_{DS} \qquad [1]$$

where L and W are the effective gate length and width of the transistor, respectively, μ_n is the carrier mobility (assuming an NMOSFET), V_{th} is the threshold voltage, V_{GS} and V_{DS} are the gate to source and drain to source voltages, respectively, and C_{ox}' is the gate oxide capacitance density. Figure 1 shows the structure of an NMOSFET for illustration.

This dissertation follows the style and format of *Journal of the Electrochemical Society*.

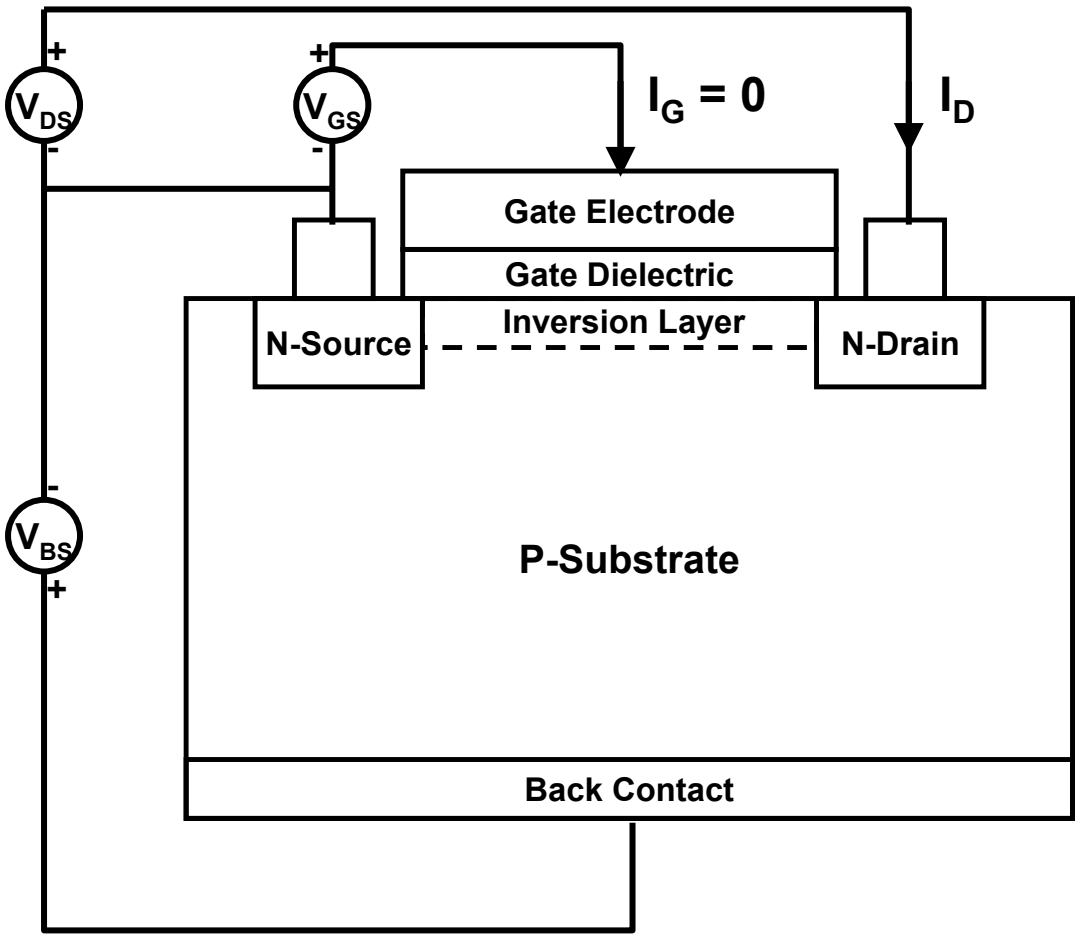

Figure 1. NMOSFET structure.

In Eq. 1, reducing L increases the current and improves the device performance.[4] The increase of the packing density is best presented with Moore's law, as illustrated in Figure 2 with Intel® processors, stating that the number of devices roughly doubles every 18 months.[5,6] Moore's law has been successfully observed for the past thirty years by the semiconductor industry, and still expected to be followed for years to come. However, formidable challenges have been continuously revealed along the way, which have to be solved in a strict time frame for Moore's law to continue.

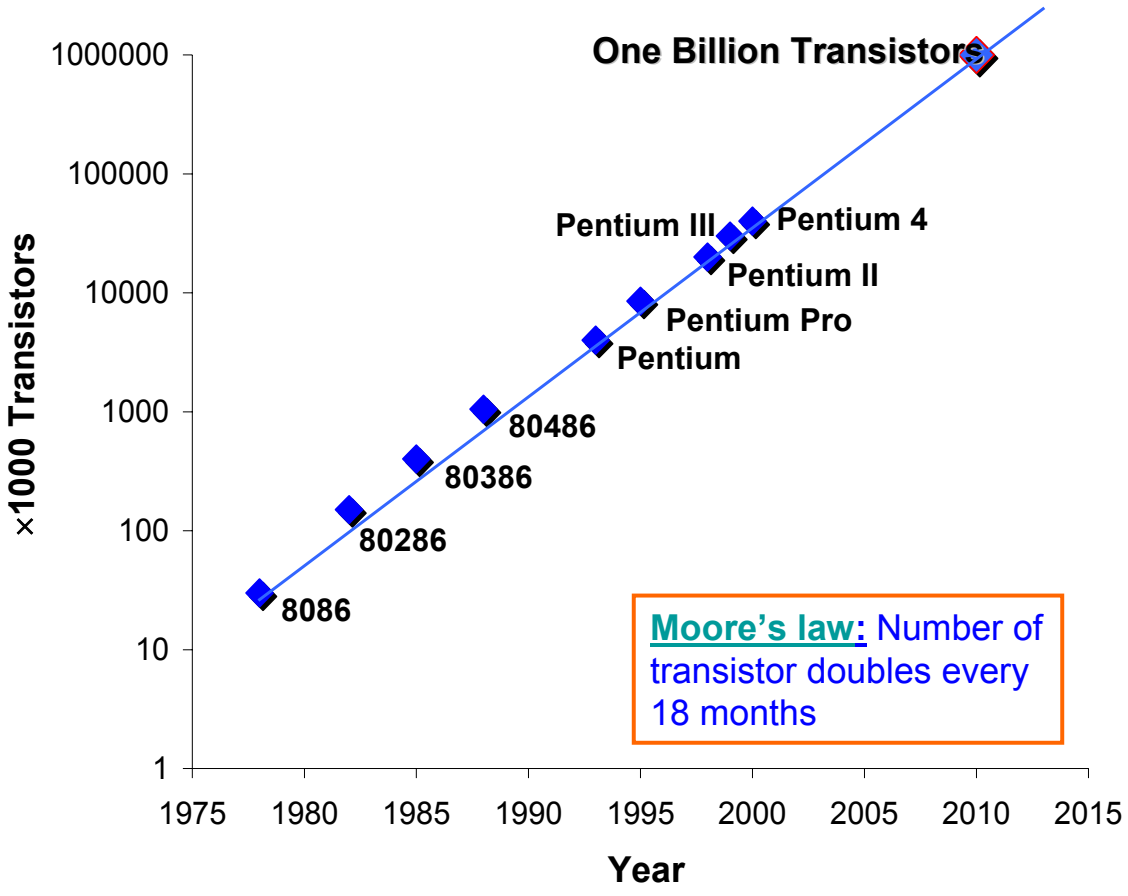

Figure 2. Illustration of Moore's law.[6]

One of the most crucial elements that allow the successful scaling is certainly the outstanding material and electrical properties of SiO_2.[7-9] First, it can be thermally grown on Si with excellent control of thickness and uniformity, which forms a very stable interface on the Si substrate with a low defect density. The interface state, mainly trivalent Si dangling bonds or P_{b0} center, can be effectively passivated by a post-metal annealing of hydrogen or forming gas. SiO_2 is very thermally stable up to 1000°C, which is required for the MOSFET fabrication. The band gap of SiO_2 is large, i.e., ~9 eV, with sufficiently large conduction and valence band offsets. The dielectric breakdown field is ~ 13 MV/cm. In addition, SiO_2 is water insoluble, which facilitates photolithography. The use of a polysilicon (Poly-Si) gate electrode in the self-aligned CMOS technology was also a determining factor in the scaling.

According to the International Technology Roadmap for Semiconductor (ITRS, 2003 version), the operating voltage (V_{DD}) should be less than 1.1 V for the high performance processor and 0.8 V for the low operating power device at the 65 nm technology node, which is expected in the year 2007.[10] The motive for the low V_{DD} is to reduce the power consumption and maintain good device reliability. At this low voltage, the equivalent oxide thickness (EOT) has to be less than 1 nm to obtain a high current, as shown in Eq. 1. Three fundamental scaling limits associated with this thin EOT have been revealed:[4]

1. Scaling limits of the SiO_2 gate dielectric layer
2. Quantum mechanical effect in the Si substrate
3. Poly depletion and boron penetration from the ploy-Si gate

These three fundamental limits are regarding the gate dielectric itself, the substrate, and the gate, respectively. The following sections will be devoted to detailing these issues.

1.1.2 Scaling Limit of Silicon Dioxide Gate Dielectric Layer

The reduction of the gate length L inevitably decreases the gate area ($A = L \times W$), which reduces the gate capacitance C_{ox}. In order to maintain a good control over the channel, the thickness (d) of the gate dielectric layer has to be reduced as well,[4,8]

$$C_{ox} = \frac{\varepsilon_0 k A}{d} \qquad [2]$$

where ε_0 is the vacuum permittivity (8.85×10^{-14} F/cm), and k is the dielectric constant. Traditionally, SiO_2 has been used for the gate dielectric layer. The scaling of the gate oxide is about the same rate as the gate length, shown in Figure 3.[11] For Intel® process technology, the ratio of the gate length to the gate oxide thickness has been roughly the same, i.e., ~45, for the past 30 years. Table I listed the near-term of scaling on the gate oxide thickness proposed by ITRS.[10] The gate oxide thickness has to be shrunk to ~1 nm at this moment. At this thickness regime, the electron tunneling effect of the gate oxide is the dominant conduction mechanism.[4] The tunneling current increases exponentially as the gate oxide thickness decreases, which results in unbearable power consumption and device performance problems.[12]

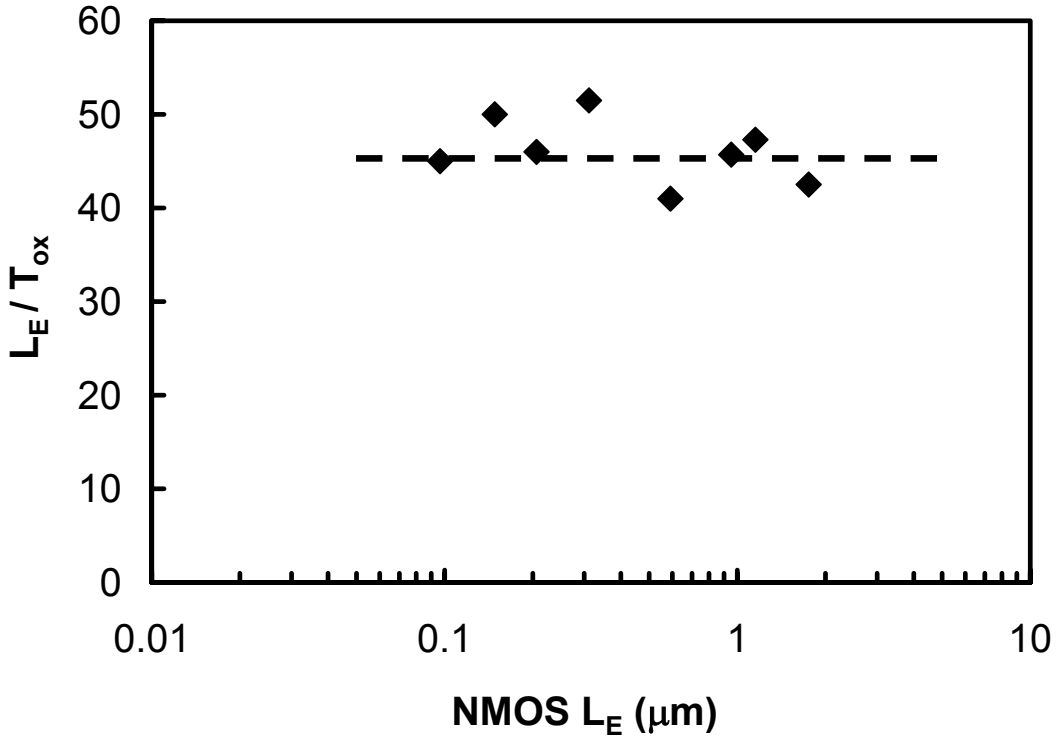

Figure 3. Intel® process technology over 30 years. The L_E/T_{ox} ratio was ~45.[11]

Table I. Gate dielectric layer technology requirements.[10]

Year of Production	2004	2005	2006	2007	2008	2009	Driver
Technology Node	90 nm			65 nm			
EOT for processor	1.2 nm	1.1 nm	1.0 nm	0.9 nm	0.8 nm	0.8 nm	processor
EOT for low power	1.5 nm	1.4 nm	1.3 nm	1.2 nm	1.1 nm	1.0 nm	power

In addition to the excess tunneling current, the thickness uniformity control of ultra-thin films is another critical issue.[1] For example, a 1 nm-thick SiO_2 layer contains only three monolayers. The variation over a 300 mm wafer during the SiO_2 growth is a substantial concern. Only 1 Å of variation is enough to change the device operating condition at this thickness, such as capacitance and current density. Therefore, the device margin is extremely difficult to control. As a result, the scaling limit of SiO_2 depends on both fundamental physics and available technology.

It has been reported that a MOSFET with SiO_2 as thin as 12 Å continued to operate satisfactory, even though a high leakage current of 1-10 A/cm^2 at V_{DD} was measured.[4] However, the scaling of CMOS structures with SiO_2 thinner than 10-12 Å has no more gain in the drive current.[13] Muller et al. predicted a fundamental limit of 7 Å (four Si atoms) of the thinnest usable SiO_2 gate dielectric. In addition, a technical limit of 12 Å was proposed due to the interface roughness.[14] Therefore, for the present technology, 10-12 Å could be taken as the scaling limit of a conventional SiO_2 gate oxide.

1.1.3 Quantum Mechanical Effect in Silicon Substrate

The quantum mechanical (QM) effect occurs when the carriers are confined in a narrow potential well close to an inverted or accumulated semiconductor surface, where their motion in the direction normal to the surface must be treated quantum mechanically.[15] The energy levels in the conduction and the valence bands split into sub-bands due to the QM effect and the lowest sub-band is located slightly above and below

the conduction and the valence band edges. The Si energy bandgap slightly increases, making the threshold voltage increase.[8,15] A simple model can be used to estimate the lowest quantized energy level from the band edge,[15]

$$\Delta E = \left(\hbar^2 / 2m*\right)^{1/3}\left(\frac{9}{8}\pi q E_S\right)^{\frac{2}{3}} \qquad [3]$$

where E_S is the surface electric field, $\hbar$ is the reduced Plank constant ($h/2\pi$), m^* is the effective mass, and q is the charge of one electron, i.e., 1.6×10^{-19} C.

Since the electrons are confined in the potential barrier, the charge centroid, i.e., the average distance of the inversion charges from the interface, is moving into the Si substrate, resulting in a thin depletion region. Consequently, the device sees an additional dielectric layer with a dielectric constant of 11.7 (Si), which increases the EOT. In general, the increase of EOT due to QM effect is about 3-5 Å.[15]

1.1.4 Poly Depletion and Boron Penetration from Polysilicon Gate

Poly-Si gate electrodes have been used with the MOSFET structure since the 1970's because it offered excellent thermal stability and implemented a self-aligned process.[9] In addition, for sub-0.5 μm CMOS technology, dual poly-Si gates have been used for making both types of surface channel devices.[16] The implanted and activated dopants have to be uniformly distributed in the poly-Si so that the concentration at the interface should be higher than 1×10^{19} cm^{-3}, which is successfully achieved due to a twice as high dopant diffusivity along the grain boundary in poly-Si than in single crystal Si.

However, as the device is scaled down and the source/drain junction depths get shallower, the thermal budget becomes limited and may cause insufficient dopant activation with the active dopants $<1\times10^{19}$ cm^{-3}.[10] This insufficiently activated poly-Si gate will be depleted under inversion, which adds another capacitance to the device and increases the EOT. This depletion becomes aggravated when the gate oxide gets thinner.[17-19]

A p-type poly-Si gate may have another problem.[1,4,8] Boron dopants in the poly-Si gate can diffuse through SiO_2 aggressively, resulting in threshold voltage instability, degradation of the subthreshold swing, and gate oxide reliability problems.[4] This problem becomes acerbated when the gate oxide gets thinner.

1.2 Motivation for Using High-k Materials as Future Gate Dielectrics

As stated in the ITRS (2003 Edition), "The gate dielectric has emerged as one of the most difficult challenges for future device scaling."[10] Indeed, the conventional gate dielectric SiO_2 obviously can not survive the challenge of an EOT = 1 nm. According to Eq. 2, if a dielectric material with a higher dielectric constant (high-k) can replace SiO_2 (k = 3.9), the dielectric layer thickness can be increased proportionally while keeping the same capacitance C_{ox}. A figure of merit to judge a high-k gate dielectric layer is the equivalent oxide thickness (EOT), defined as,[4]

$$EOT = (k_{SiO_2} / k_{high-k}) d_{high-k} \qquad [4]$$

The EOT shows the electrical equivalent thickness of the high-k layer to SiO_2 when the capacitance is the same. Since a thicker layer is used for insulating, the tunneling current

is drastically reduced in this thickness regime. However, before a new high-k material can be integrated into the present ULSI process flow, many requirements have to be met first.[4,8-10] The following sections will give a brief introduction.

1.2.1 Requirements for Alternative High-k Gate Dielectrics

There have been many review papers, books, and industry consensus that proposed a criteria for choosing alternative high-k materials for different applications.[4,7,8,10,20,21] To stress this issue, Figure 4 shows the vertical structure of an MOS gate stack with a high-k gate dielectric layer.[4,21] Notice that the high-k gate dielectric, unlike a thermal SiO_2, forms two interface layers with both the top poly-Si gate and the bottom Si substrate due to the thermodynamic instability with Si.[22] It is clearly identified that these two interfaces, as well as the bulk dielectric film, have to be considered when choosing the alternative gate dielectric film. Actually, the interface engineering has become the main issue of the high-k dielectric integration.[23-30] For example, the bottom interface affects the Si channel mobility and thus the transistor drive current, while the defects at the top interface may cause the Fermi level pinning when a poly-Si gate is used.[4,8,31,32]

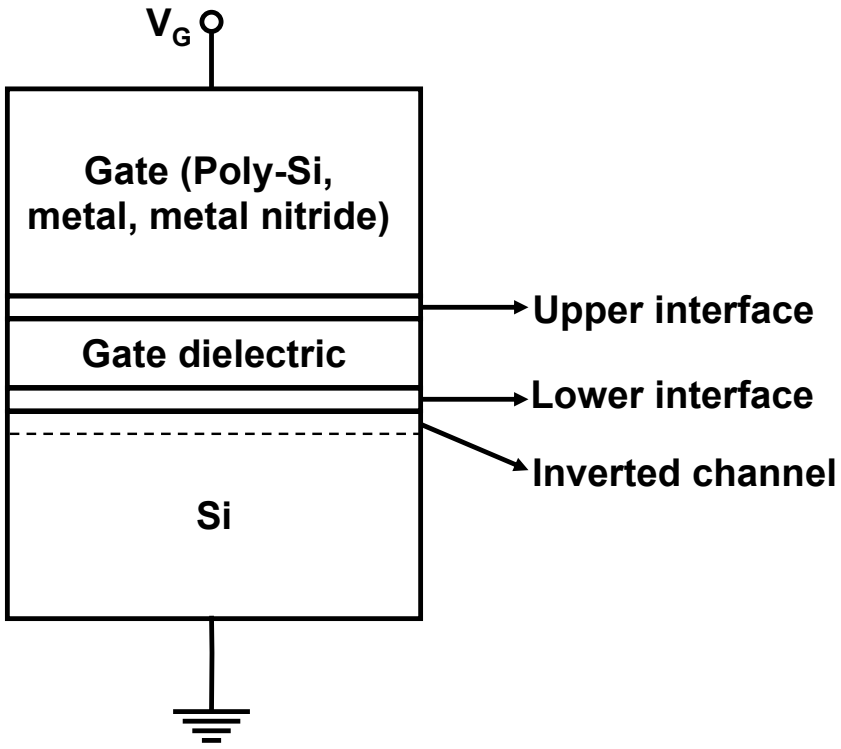

Figure 4. The stack structure of gate/gate dielectric/substrate.

The requirements for a promising candidate for the high-k gate dielectric can be divided into two categories: (a) structural and (b) electrical requirements. In general, the structural requirements include:[4,20,33]

1. Thermodynamic stability when in contact with Si
2. Low oxygen diffusion coefficient to prevent interface formation
3. Low structural defect density at interface and bulk regions
4. High amorphous-to-crystalline transition temperature
5. High density for blocking impurity diffusion

And the electrical requirements, except for a high dielectric constant (k), are:[4,20,33]

1. Large bandgap and large barrier heights with Si
2. Negligible frequency dispersion
3. Negligible hysteresis
4. Low electrical defect density at interface and bulk regions
5. Good reliability

In addition, the new high-k material should be easy to deposit and compatible with the other standard ULSI fabrication techniques. The following sections will discuss some of the most crucial requirements, i.e., thermodynamic stability, amorphous-to-crystalline temperature, bandgap, and barrier height. Some of the other requirements will be illustrated by the experimental results of this study.

Thermodynamic stability in contact with Si

Thermodynamic stability of the high-k dielectric layer when it is in contact with the underlying Si substrate may be one of the most important requirements for the successful integration of the material.[4,22] An unstable interface contact results in a solid state reaction, which forms a low quality interface layer between high-k and Si. This undesired interface layer has a low dielectric constant similar to SiO_2, which creates an additional capacitor in series with the high-k layer and reduces the overall effective dielectric constant. This effect can be expressed by the following equation,[4,22]

$$\frac{d_1 + d_2}{k_{eff}} = \frac{d_1}{k_1} + \frac{d_2}{k_2} \qquad [5]$$

where d_1 and d_2 are the film thicknesses of the high-k bulk and interface, respectively; likewise, k_1 and k_2 are the corresponding dielectric constants. In Eq. 5, increasing the thickness d_2 and/or decreasing the dielectric constant k_2 of the interface layer result in the decrease of the effective dielectric constant k_{eff}. Consequently, the minimization of this interface formation by choosing a thermodynamically stable high-k material has become the real task.

Hubbard and Schlom comprehensively collected all of the thermodynamic data ever published for metal oxides and calculated their thermodynamic stabilities when in contact with Si.[22] Based on the phase diagrams among the three involved elements, i.e., Si, O, and the metal (M), there should be a tie line between the stable metal oxide phase, i.e., the high-k dielectric, and Si (substrate) in order to have a thermodynamically stable interface. This survey was done at 1000K, which was a routinely used temperature range

in ULSI processing, e.g., the poly-Si gate and S/D dopant activation.[4] For this tie line to exist, the Gibb's free energy (ΔG) of any possible reaction between the metal oxide (MO_x) and Si should be strongly positive. There were mainly two reactions that had to be considered, i.e., silicide formation (silicidation) and metal dissociation,

$$MO_x + Si \leftrightarrow MSi_y + SiO \qquad \text{Silicidation} \qquad [6]$$

$$MO_x + Si \leftrightarrow M + SiO_2 \qquad \text{Dissociation} \qquad [7]$$

If ΔG of either reaction was negative, the metal oxide was not thermodynamically stable with Si and an interface layer of SiO_2 or MSi_y would form. This conclusion has been confirmed experimentally on different high-k dielectrics by different groups.[4,30,34-38] Table II shows the calculated ΔG of some metal oxides for these two interface reactions at T = 1000K.[22] Figure 5 shows the ternary phase diagrams of (a) Ta-Si-O and (b)Zr-Si-O at 1000K.[22,39,40] In Fig. 5(a), there was no tie line between Ta_2O_5 and Si when the thermodynamic equilibrium state was reached, suggesting the formation of an interface layer between them as a transition region. ZrO_2, however, did have a tie line with Si, as shown in Fig. 5(b). This indicated a thermodynamically stable contact. Solely based on this thermodynamic concern, the choice favors ZrO_2 over Ta_2O_5.

Table II. Thermodynamic stability test with calculated Gibb's free energy.[22]

Metal Oxide	ΔG_{1000}^{0} (KJ/mol) for silicide formation	ΔG_{1000}^{0} (KJ/mol) for metal dissociation
Ta_2O_5	NA	-219.588
ZrO_2	+24.720	+176.923
HfO_2	NA	+199.169
Al_2O_3	NA	+265.009
TiO_2	-96.199	+31.463
Y_2O_3	NA	+488.320

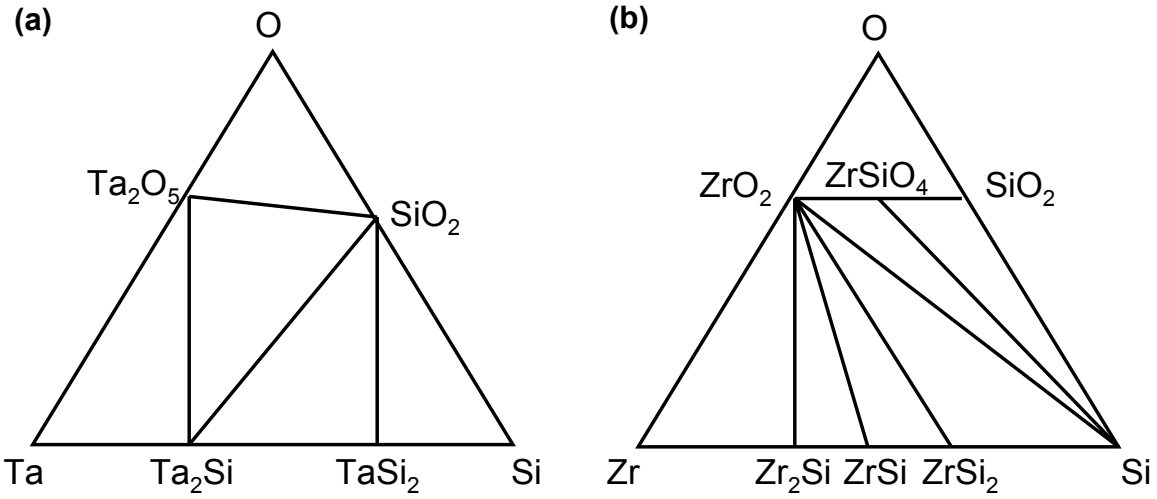

Figure 5. Ternary phase diagrams of (a) Ta-Si-O and (b) Zr-Si-O at 1000K.[22,39,40]

Amorphous to crystalline transition

In general, a polycrystalline form of a gate dielectric layer is not preferred for transistor applications.[7,41-44] The grain boundaries inside the polycrystalline film act as extra conduction paths for the carriers, which increase the leakage current.[45,46] A large number of defects and/or microcracks due to the increased internal mechanical stress may also contribute to the enhanced leakage.[47,48] Except for the leakage current, the non-uniformity of grain size and orientation in the crystallized film pose a topological problem at both interfaces. For example, the dielectric constant of a polycrystalline material depends on the grain orientation and can vary over a wide range, which makes the gate capacitance different from one device to another.[46] As a result, an amorphous form of the high-k gate dielectric layer is always preferred.

The morphology of an as-deposited dielectric film depends on the deposition technique and experimental condition.[7,46] Most of the high-k films deposited at a low temperature have an amorphous state before annealing. However, they transform to the polycrystalline form after a high temperature treatment.[43,49] This high temperature thermal treatment, normally ~1000°C, is necessary for the source/drain and poly-Si dopant activation and damage repairing after the ion implantation step. Therefore, the transition temperature to the polycrystalline state has to be maximized. Pure ZrO_2 and HfO_2 are known to crystallize at a low temperature around 500°C, which is inappropriate for the ULSI process.[50,51] However, adding impurities such as Si or N into the film is effective to increase the transition temperature with the trade-off of reducing dielectric constant.[52,53]

Energy bandgap and barrier heights with Si

In addition to a high dielectric constant, a potential candidate for high-k gate dielectrics should possess a large energy bandgap (E_g) as well as large barrier heights (band offsets) with both the conduction and valence Si band edges, i.e., ϕ_{Be} and ϕ_{Bp}, so the carrier generation and conduction can be minimized.[4,54,55] In general, with the increase of the metal atomic number, the metal ionic radius increases but the cohesive force decreases in the metal oxide, which results in a large dielectric constant but a narrow bandgap.[56,57] The small bandgap then results in smaller energy band offsets with Si. The bandgap is inversely related to the dielectric constant,[57]

$$E_g \approx 20 \times \left(\frac{3}{2 + k} \right)^2 \qquad [8]$$

Figure 6 shows the bandgap and dielectric constant of some dielectric materials, where the inverse relationship suggested by Eq. 8 was clearly demonstrated.[58] Figure 7 shows the electron and hole barrier heights with Si for some potential high-k candidates.[59] Notice that Ta_2O_5 has a smaller electron barrier height compared to ZrO_2 and HfO_2, which makes the pure Ta_2O_5 an inappropriate gate dielectric for the Si substrate. The silicate of Zr, i.e., $ZrSiO_4$, which is also under intense research, has similar electron and hole barrier heights as ZrO_2. Table III summarizes some important electrical properties regarding the high-k gate dielectric applications for some potential candidates in the literature.[4,20,54]

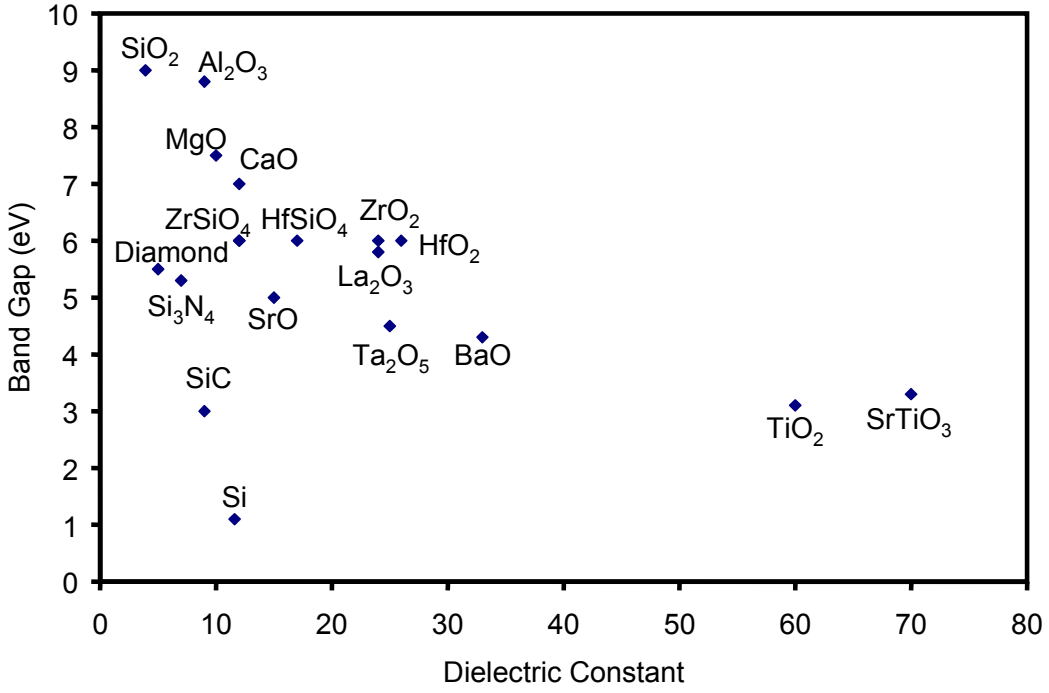

Figure 6. Band gap vs. dielectric constant for some dielectric materials.[58]

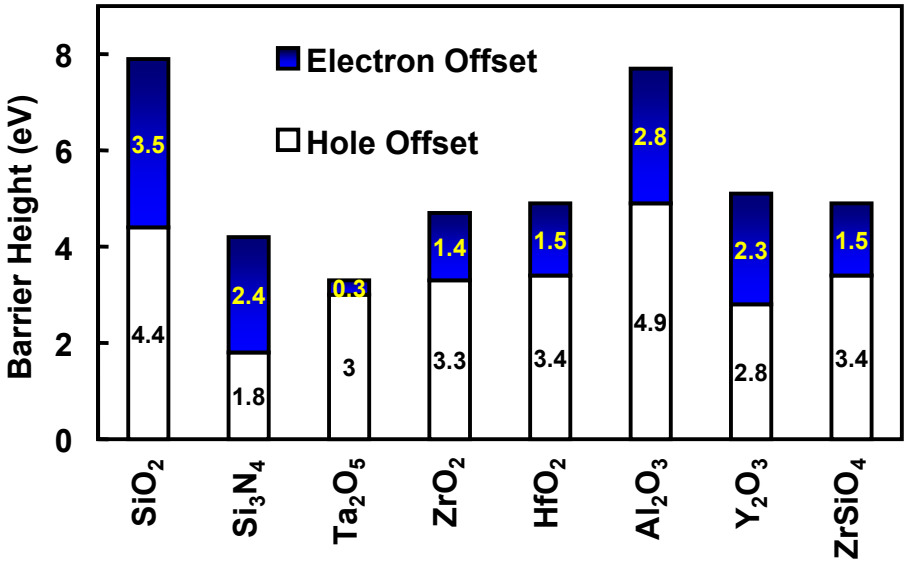

Figure 7. Electron and hole barrier heights with Si for some high-k gate dielectrics.[59]

Table III. Key parameters of selected gate dielectric materials.[4,20,54]

	Dielectric Constant (k)	Band Gap (E_g, in eV)	Electron Offset (Φ_{Be}, in eV)	Hole Offset (Φ_{Bp}, in eV)	Breakdown Field (E_{BD}, in MV/cm)
SiO_2	3.9	9	3.5	4.0	10
Al_2O_3	8	8.8	3	4.7	10
TiO_2	80	3.5	1.1	1.3	3
ZrO_2	25	5.8	1.4	3.3	4-5
HfO_2	25	6	1.5	3.4	4-5
Ta_2O_5	25	4.4	0.3	3	5
Zr_xSi_yO	8-12	6.5	1.5	3.9	5-10

1.3 Motivation for Using Doped TaO_x as a Future Gate Dielectric

1.3.1 Zr-doped TaO_x Gate Dielectrics

Tantalum pentoxide (Ta_2O_5) has been widely studied both experimentally and theoretically over the past three decades.[45,46] Extensive applications of Ta_2O_5 have been found in different fields, such as antireflective layers in optical devices, dielectric layers for DRAM and MOS devices, insulating layers in thin-film electroluminescent (TFEL) devices, and dielectric layers in biological sensors.[60-64] It has a high dielectric constant (~25) and a reasonably wide bandgap (~4.4 eV).[46] However, some drawbacks have been found when the effort was made to integrate Ta_2O_5 with Si. First, the thermodynamic instability with Si, which was discussed in a previous section, reduces the effective dielectric constant tremendously.[22,46] Second, the quite small electron barrier height with the Si conduction band exacerbates the film leakage.[54,55] The thermal stability is another issue for integration, as discussed previously. Pure Ta_2O_5 was reported to crystallize at around 650-700°C, depending on deposition techniques, which is too low to survive the thermal budget of ULSI processing.[47,65] As a result, the pure Ta_2O_5 has almost been abandoned as a candidate for future MOSFET applications.[4,33]

There are many studies regarding the applications of zirconium dioxide (ZrO_2) as a potential high-k gate dielectric layer for next generation MOSFET devices.[28,66-71] First, ZrO_2 has a high dielectric constant (~24) and a wide bandgap (~5.8 eV), as shown in the last section. Second, the thermodynamic stability with Si is excellent, as seen in Table II and Fig. 5(b). However, the amorphous-to-polycrystalline transition temperature is about 500°C, which is definitely too low for ULSI processing.[41] The transition temperature can

be increased, fortunately, by adding impurities (dopants) into the film.[34-36,41,72] This occurs because the dopant atoms distort the originally more ordered structure and thus increase entropy, which suppresses the crystallization process.[20] Elements such as silicon (Si), aluminum (Al), and nitrogen (N) were reported as effective dopants for this purpose.[20,23,24,34-36,73]

The doping technique, i.e., adding a third element into the binary oxide high-k gate dielectrics, is considered a plausible way to improve the structural and electrical properties for various applications.[74-78] Especially for Ta_2O_5, of which a pure form may not be suitable for MOSFET applications, its structure does not significantly changed by doping even with an appreciable amount.[79] Cava et al. systematically studied several dopant types for thick ceramic Ta_2O_5 films, including Zr, Ti, and Al.[79-81] The dielectric constant, temperature coefficient (TCK), and dissipation factor were found to be improved with an optimized doping concentration. Salam et al. studied the doping effect on thin Ta_2O_5 films and claimed that the mixing of TiO_2 or WO_3 with Ta_2O_5 improved several dielectric and insulating properties.[82] In addition to the MOS application, Ta_2O_5 has also been researched as an insulator for thin film electroluminescent (TFEL) devices.[46] In order to obtain better insulating properties, it was prepared in multilayer structures with Al_2O_3, HfO_2, or ZrO_2.[63,75,83] The best dielectric properties were obtained with a ZrO_2-Ta_2O_5 structure, which achieved a dielectric constant of 28.

As a result, Zr was proven to be a potential dopant for Ta_2O_5. In this study, the reactive co-sputtering technique has been applied to introduce the Zr dopant into the

TaO_x film. Electrical and structural characterizations were done to investigate the applicability of this new high-k material.

1.3.2 Other Dopant Types for TaO_x Films

In addition to Zr, other dopants have also been investigated for the dielectric improvement of the TaO_x film. For example, Ti was found to increase the dielectric constant drastically with a substantial dopant concentration in TaO_x.[34,35,79] However, the amorphous-to-crystalline transition temperature as well as leakage current were degraded by the Ti doping. A low-quality interface layer was also observed between the Ti-doped TaO_x film and the Si substrate, as shown by the TEM image in Figure 8.

Figure 9 shows the dielectric constants as a function of the dopant concentration. Among all the dopants in the figure, Zr was the only one that was beneficial for dielectric constant enhancement. Hafnium (Hf) was another promising dopant for TaO_x.[23,26,37,84] Many electrical properties, such as dielectric constant, leakage current, flatband shift, and hysteresis, showed great improvements with the Hf doping. Please refer to the listed references for details.

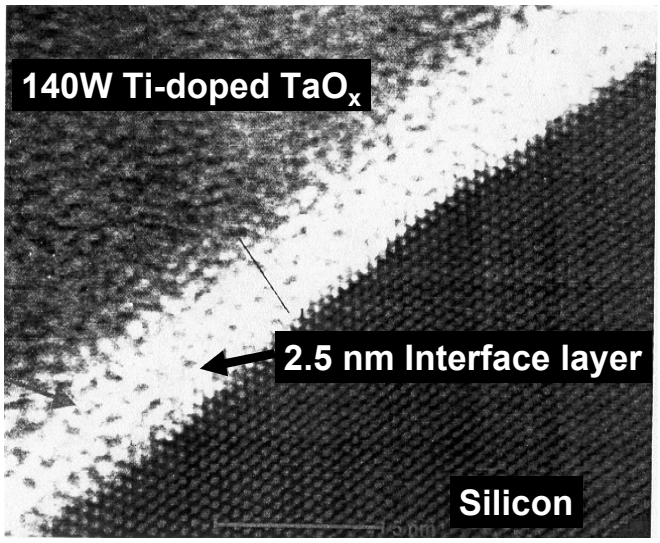

Figure 8. TEM of a 140W Ti-doped TaO_x film annealed at 700°C for 10 minutes in O_2 (courtesy of Dr. A. Agarwal from International SEMATECH).

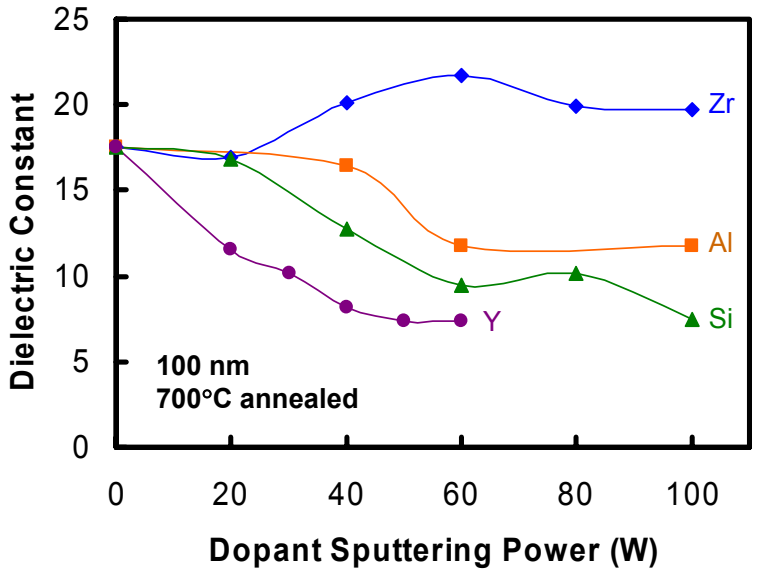

Figure 9. Dielectric constants of the doped TaO_x as a function of dopant concentration. All the films were ~100 nm thick and annealed at 700°C for 10 minutes in O_2.

1.3.3 Motivation for Using Nitrided Interface for Zr-Doped TaO_x Films

It has been experimentally proven that the properties of the high-k/Si interface layer is dependent on the composition and fabrication process of the bulk high-k dielectric layer.[30,85] Even though the equilibrium thermodynamics predicted that some promising high-k dielectrics can be stable in contact with Si without growth of a low-quality interface transition region, the experimental results always showed the existence of this interface layer after a high temperature annealing step.[4,30,38,86,87] Typical examples are ZrO_2 and HfO_2, which always have an obvious interface layer with TEM images. Although this interface layer, basically SiO_x, is detrimental for the EOT scaling, it seems necessary for the MOSFET device performance.[88] For example, interface traps, fixed charges, and channel mobility were found to be improved with an intentionally deposited ultra-thin SiO_2 interface.[86,89] Consequently, the key issue for integrating the high-k materials for the MOSFET applications is optimizing this interface layer.

Forming a silicon nitride layer before the deposition of Ta_2O_5 has been used for years to solve the interfacial SiO_2 film overgrowth problem and to enhance the interface properties.[46,90,91] Si_3N_4 is known to be one of the best diffusion barriers for water and ions.[46] By introducing N atoms at the interface or into the bulk film, oxygen diffusion can be minimized to prevent the SiO_x formation.[87] Therefore, the interface layer has a higher dielectric constant and a smaller thickness, which increases the overall effective dielectric constant.[92] In addition, the N atoms help to block the electron transport at the interface as well as release the interface stress, which reduces the leakage current.[23,26] The thermal stability with the N incorporation is also improved.[93,94] Nitrogen atoms have

one more valence than oxygen atoms, i.e., N≡ vs. O=, which makes the atom arrangement more flexible. For example, Figure 10 illustrates the possible atomic configurations.[7] (i) and (ii) show the nitrogen bridging between two N atoms and among three Si atoms, and (iii) shows the defect of the N-H bond. These atomic configurations due to N≡ may be responsible for the excellent electrical properties.[7] In this study, a nitridation step was used to incorporate N atoms at the interface by depositing a thin (~5 Å) TaN_x layer before the high-k deposition.[23,26]

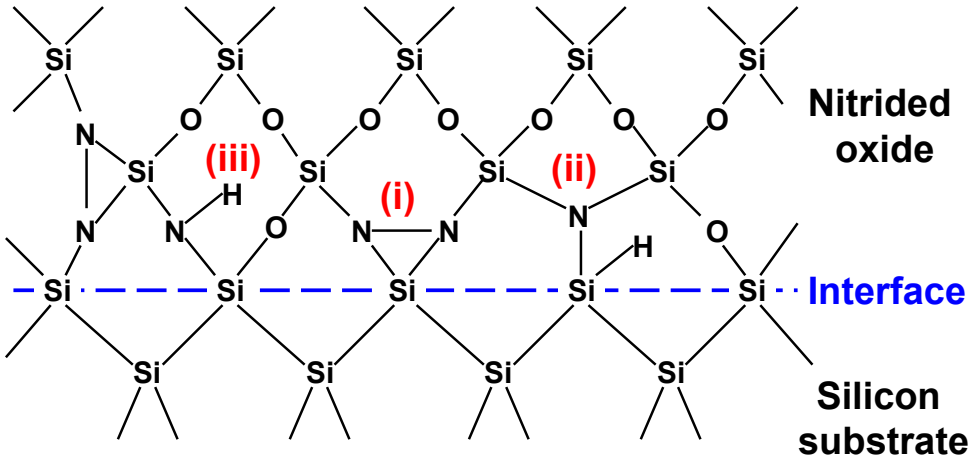

Figure 10. Possible atomic configurations and defects near the nitrided interface.[7]

1.3.4 Motivation for Using Metal Gate Electrode for Zr-Doped TaO_x Films

The conventional poly-Si gate has problems such as poly depletion, high gate resistance, high gate tunneling current, and boron penetration.[10] For example, ITRS predicts that an active dopant density of 1.87×10^{20} cm^{-3} for L_G = 25 nm technology has to be reached for a poly depletion layer less than 25% of EOT.[10] This poses a great challenge because the solid solubility at the gate/dielectric interface are 6×10^{19} cm^{-3} and 1×10^{20} cm^{-3} for p^+ and n^+ poly-Si respectively.[95]

New electrode materials have been investigated to replace the poly-Si gate. For example, molybdenum (Mo), molybdenum nitride (MoN), tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), and platinum (Pt) were proposed.[60,96-102] Replacing the poly-Si gate by a metal or metal nitride gate minimizes the reaction between a high-k gate dielectric and the poly-Si, which forms a SiO_x interface layer. It also naturally eliminates the poly depletion and boron out-diffusion problems and reduces the gate sheet resistance.[4,103] In addition, the use of metal gates in a replacement gate process can lower the thermal budget due to the lack of the poly-Si dopant activation annealing.[104]

In this study, the Mo, MoN, and WN gate electrodes were thoroughly investigated for the integration with the Zr-doped TaO_x high-k dielectric films.

1.4 Outline

Chapter II covers the experimental methods and the corresponding background theories adopted in this study. Starting with the explanation of the entire process flow for the fabrication of the Zr-doped TaO_x films, the detailed experimental conditions were provided. A reactive co-sputtering technique with both Ta and Zr metallic targets was used for the film deposition. A variety of instrumentation for the physical, chemical, and electrical characterizations was introduced. Several extraction techniques of the interface state density (D_{it}), which is crucial to quantify the quality of the high-k gate dielectrics, were presented in detail. The optimization of the experimental parameters was demonstrated; specifically the sputtering gas composition and the annealing gas pressure. Finally, the measurement methodology regarding the capacitor gate area was explained and standardized.

Chapter III focuses on the characterizations of the Zr-doped TaO_x films. The film thickness was about 15 nm. The Zr dopant concentration and the annealing condition were varied to optimize the electrical and structural properties for the MOS device applications. The results of ESCA, XRD, SIMS, and TEM were presented. The core levels of Zr_{3d}, Ta_{4f}, and O_{1s} shifted to lower binding energies as the Zr dopant concentration was increased. The transition temperature from an amorphous to a polycrystalline state in the TaO_x film was increased by at least 200-300°C with the Zr doping. The crystal structures were found to be between pure Ta_2O_5 and ZrO_2, depending on the Zr dopant concentration, annealing temperature, and film thickness. The compositional profiling with SIMS indicated that Zr diffused into the interface

region to form a Zr silicate, i.e., Zr_xSi_yO, interface layer, while Ta was not incorporated at the interface. The TEM images confirmed the interface layer formation with a thickness of 2-3 nm. The C-V and I-V curves were shown to extract important dielectric and insulating properties. There was a maximum of dielectric constant roughly at the Zr co-sputtering power of 40-60 W, corresponding to the atomic ratio of Zr/(Ta+Zr) = 0.33-0.40. This maximum dielectric constant of Zr-doped TaO_x was about 15-16. The leakage current of the Zr-doped TaO_x film was much lower than SiO_2 at the same EOT because of the higher dielectric constant. The conduction mechanism of the Zr-doped TaO_x film was between Schottky emission and Poole-Frenkel conduction, depending on the Zr dopant concentration and annealing condition. The interface layer difference between Ta_2O_5 and ZrO_2 was applied to explain the different I-V behaviors between doped and undoped TaO_x samples. The flatband shift and hysteresis of the C-V curves were analyzed, both of which were found to be strongly influenced by the Zr dopant concentration. Finally, the conclusion was drawn on the Zr dopant effect for the doped TaO_x dielectric film.

Chapter IV focuses on the dielectric properties of the Zr-doped TaO_x films with the insertion of a TaN_x interface layer. The dielectric film thickness was about 8 nm with an extra ~5 Å TaN_x interface. The structural and electrical characterizations were used to compare the films with and without this TaN_x interface. ESCA indicated the TaN_x layer was oxidized into TaO_xN_y during the high temperature O_2 annealing at 700°C, which was a better insulator with a higher dielectric constant than TaN_x. The compositional profiling with SIMS supported this conclusion. Electrical properties, such as dielectric

constant, EOT, current density, and dielectric breakdown, were found to be improved. However, the flatband voltage shift and interface state density were slightly degraded. Hysteresis was about the same regardless of the TaN_x interface layer.

Chapter V shows the structural and electrical characterizations of the Zr-doped TaO_x films integrated with metal and metal nitride gate electrode materials, i.e., Mo, MoN, and WN. The Zr-doped TaO_x film was optimized with the atomic ratio Zr/(Ta+Zr) = 0.33, or the Zr co-sputtering power of 40 W, which had been obtained in Chapter III. A single metallic alloy target of Zr/Ta was used for the sputter-deposition. The in-situ deposition-annealing system with a load lock transfer chamber was used here for the entire deposition/annealing/metallization process. A wet etching was applied for the Mo gate patterning, while a dry reactive ion etching (RIE) was used for the MoN and WN gates. The resistivities of the MoN and WN gates were optimized by adjusting the N_2 flow rate during sputtering. The microstructures of different gates were analyzed with XRD, which showed highly crystallized phases after a post-metal annealing. The device characterizations of the Zr-doped TaO_x films were found to change appreciably with the choice of gate electrode. The influences of metal (nitride) gates were mainly through the metal work function and thermal stability. Current density, EOT, flatband voltage, hysteresis, frequency dispersion, and interface state density were all found to be altered by the different gate electrodes. The compatibility and robustness of the Zr-doped TaO_x dielectric films were thus confirmed with this gate electrode integration experiment.

In the end, chapter VI summarizes this study and draws conclusions.

CHAPTER II

EXPERIMENTAL METHOD AND BACKGROUND THEORY

2.1 Introduction

The first part of this chapter discusses the sample preparations of Zr-doped TaO_x films. Details of the experimental parameters will be given. The Al gate electrode was adopted as the example for the capacitor fabrication, which was used for the electrical characterizations. The second part of the chapter will be devoted to the structural and electrical characterizations. The instrumentation and theories of secondary ion mass spectroscopy (SIMS), electron spectroscopy for chemical analysis (ESCA), X-ray diffraction (XRD), transmission electron microscopy (TEM), and C-V and I-V curves will be shortly reviewed. Interface state density extraction, which is important for characterizing a high-k dielectric material in MOS devices, will be discussed in detail since the physics behind the measurement is complicated. Several techniques, such as low frequency C-V, high-frequency C-V, and conductance method, will be presented with corresponding illustrated examples. The third part focuses on the process optimization, including sputtering gas composition and post-deposition annealing pressure. The important electrical properties regarding device performance, e.g., dielectric constant, current density, breakdown strength, flatband shift, and hysteresis, will be used for tuning the experiment parameters. The last part of the chapter will be contributed to the methodology of C-V and I-V curves, which are influenced extrinsically by the test structures, such as the gate electrode area.

2.2 Experimental Procedures

2.2.1 Process Flow

All of the Zr-doped TaO_x thin films were deposited by a magnetron-assisted radio frequency (13.56 MHz RF) reactive sputtering in a vacuum chamber (base pressure ~5×10^{-7} Torr). The Zr dopant was introduced in two ways: (a) using two separate metallic targets of Zr and Ta, and (b) using a metallic alloy target of Zr/Ta with a pre-defined atomic ratio, i.e., Zr/(Zr+Ta) = 0.33. This ratio corresponds to 40 W of Zr co-sputtering power and 100 W of Ta co-sputtering power when two separate targets are used. Figure 11 shows the sputtering chamber configuration. The target sizes were 2 in. diameter × 0.25 in. thick. Shutters in front of the targets were used to control the start and stop of the deposition.

The substrate for the Zr-doped TaO_x film was cut from a 150 mm (100) p-type Si wafer (manufactured by MEMC). The wafer doping concentration was 10^{14}-10^{15} cm^{-3}, which corresponded to a resistivity of 10-80 Ω-cm. The substrate size was around 1 in. × 1 in. Before loading the substrate into the sputtering chamber, it was cleaned with a piranha solution to remove any organic contamination. The piranha solution was composed of 3 parts of sulfuric acid (H_2SO_4, 98 %) and 1 part of hydrogen peroxide (H_2O_2, 30%), which was self-heated to ~98°C. This piranha solution dipping of substrates usually lasted for 10 minutes. A second beaker of heated DI water at ~90°C and then a third beaker of room-temperature DI water ended this cleaning step. During the piranha cleaning, the organic contaminants were oxidized on the substrate surface. Then a diluted hydrofluoric acid (HF, 10%) was used to remove the Si native oxide

together with the oxidized organics on the surface. A DI water rinse followed by a N_2 blow drying ended this cleaning step.

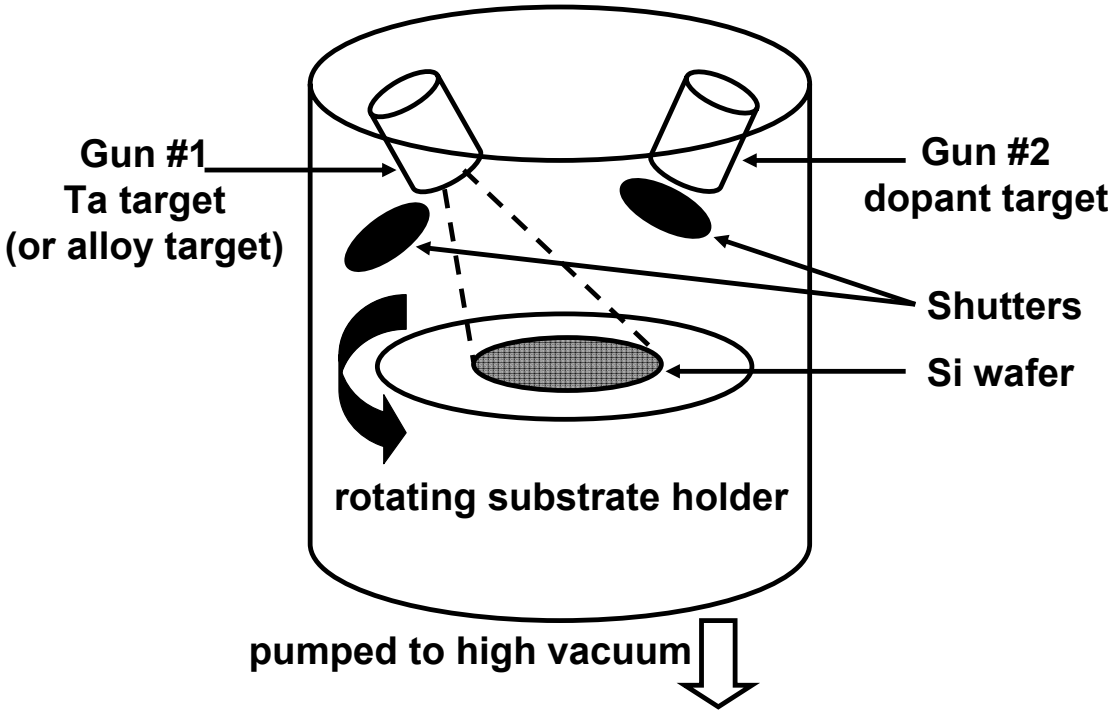

Figure 11. Sputtering chamber configuration.

A load lock system was used to transfer the substrate (sample) into the sputtering chamber for deposition, as shown in Figure 12. The sputtering chamber was kept at very high background vacuum, i.e., ~5×10^{-7} Torr, without being open to the atmosphere. The sample was loaded into the load lock chamber at atmospheric pressure and pumped down to ~10^{-6} Torr within 20 minutes. When the desired pressure was reached, the gate valve between the load lock chamber and the sputtering chamber was opened to transfer the sample to the deposition chamber. Once the sputtering chamber was isolated again with the sample inside, the pumpdown continued until a base pressure of ~5×10^{-7} was obtained. The pumping system for the sputtering chamber included a mechanical pump (Alcatel 2063 CPI) and a turbomolecular pump (Leybold TurboVac 360). For the load lock chamber, a combination of a mechanical pump (Edwards RV8) and a turbomolecular pump (Pfeiffer TPH170) was used. The turbo pumps were cooled by a water chiller (Neslab CFT-33).

To adjust the Zr dopant concentration in the high-k film, two metal targets of Ta and Zr were used simultaneously for co-sputtering. The Ta target sputtering power was fixed at 100 W while the Zr target co-sputtering power was varied. The power density of the target at 100 W was 5 W/cm^2. A pre-sputtering step was done for 10 minutes with pure Ar to clean the target surface. For comparison purposes, undoped TaO_x and ZrO_y films were also deposited under the same experimental conditions. The distance from the target surface to the sample, i.e., throw distance, was 10 cm. The gas mixture used during the sputter deposition was Ar/O_2 (1 : 1) with a total flow rate of 40 sccm and an operation pressure of 5 mTorr. The optimization of this sputtering gas composition will

be presented later in this chapter. The substrate temperature influences the film's conformity and topology.[105] In our case, the substrate was unheated. However, the substrate was rotated at 20 rpm in order to improve the film uniformity. It was reported that the high sputtering power resulted in the film's high density and low interfacial layer thickness, which made the film a smaller EOT.[70,106] However, the damages from the plasma and ion bombardment could be aggravated as the sputtering power is increased, which is a concern for the high-k gate dielectric.[46] In addition, the heat dissipation from the target would be a potential problem if the cooling circulation was not properly installed. As a result, we optimized the sputtering power at 100 W thereafter.

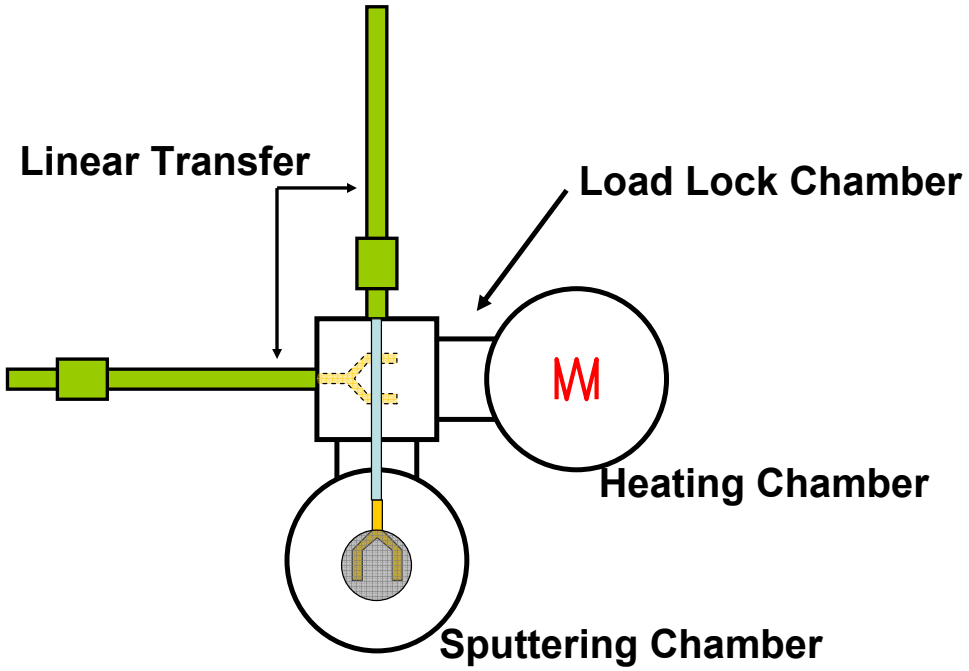

Figure 12. Load lock system connecting the sputtering chamber and the heating chamber.

The as-deposited Zr-doped TaO_x film was annealed at 600°C for 60 minutes or at 700°C for 10 minutes, both in an O_2 ambient. This post-deposition annealing was done in two ways, i.e., in-situ and ex-situ. The in-situ annealing was performed in the heating chamber with a resistive button heater (Heatwave Inc., CA), which was connected to the sputtering chamber via the load lock system, as shown in Fig. 12. The sample transfer was done without breaking the vacuum. The heating chamber had a base pressure of $\sim 10^{-8}$ Torr and the annealing could be done at 10-500 Torr. On the other hand, the ex-situ annealing was operated in a LPCVD furnace after the as-deposited sample was taken out from the vacuum. This LPCVD furnace annealing was done at ~200 Torr.

The in-situ heating method is preferred over the ex-situ method because of less possibility of sample contamination. High-k gate dielectrics, e.g., ZrO_2, are infamous for the susceptibility to airborne contaminants such as moisture and organics.[107] The moisture induces the particle formation, impurity binding promotion, oxidation, and corrosion. It is the most difficult to control due to its small size, high polarity, and strong hydrogen bond.[107] On the other hand, the organics in the air can change the wetting property, assist in the particle formation, and affect the dielectric performance. Both the moisture and organic contaminants affect the accuracy of the optical measurement of the film thickness. In addition, a significant amount of moisture has detrimental impact during the post-deposition thermal process, such as interface overgrowth.[107]

For the purpose of electrical characterization, the Zr-doped TaO_x film was fabricated into MOS capacitors. The top gate electrode was made of a ~400 nm thick aluminum (Al) film, which was deposited by direct current (DC) sputtering in Ar. Two

different methods for defining the gate electrode area were used: by photolithography or through a shadow mask.[105] A g-line sensitive positive photoresist layer (AZ 1512, Clariant, Somerville, NJ) was coated on the Al surface around 4000 rpm using a spinner (Headway Research, Inc., Garland, TX). A soft-bake on a hot plate at 90°C for 1 minute was performed before the UV exposure. A Quintel Q4000 contact aligner was used for the exposure. The sample was dipped into a DI water-diluted developer (1 part of DI water and 2 parts of AZ MIF 300, Clariant, Somerville, NJ), followed by a thorough DI water rinse. After that, the sample was blow-dried with a nitrogen gun and was hard-baked on a hot plate at 135°C for 1 minute. The Al gate was etched with the solution of H_3PO_4 : HNO_3 : CH_3COOH : H_2O = 16 : 1 : 1 : 2. A very high etch rate was observed for the etch process, e.g., the entire etch was finished within 10 seconds. The photoresist was stripped by acetone, isopropyl alcohol (IPA), and DI water, consecutively. The gate area was between 1×10^{-3} and 1×10^{-5} cm^2.

To obtain a better contact on the backside of the Si substrate, i.e., Ohmic contact, a ~200 nm Al film was deposited on the backside after removing the native oxide that was grown during the post-deposition annealing (PDA). Finally, a post-metal annealing (PMA) was done at 300-400°C for 30 minutes in the LPCVD furnace, with forming gas (10% H_2 and 90% N_2). This annealing step served two purposes: (a) to warrant the back wafer Ohmic contact, and (b) to reduce the high-k/silicon interface traps.[16,105] Al, like B, is a p-type dopant in the Si wafer. The heat treatment could drive the Al atoms slightly into the backside Si contact to increase the p-type dopant concentration and reduce the

resistivity. The atomic H from the H_2 gas could passivate the interface dangling bonds due to the incomplete oxidation and thus improve the device performance and reliability.

2.2.2 Measurement Setup

The dielectric film thickness was measured with an ellipsometer (Rudolph i1000) at the wavelength of 632.8 nm. The refractive index of the film was estimated with the same measurement by the iteration of a self-consistent data fitting.[108] The measured refractive index of the Zr-doped TaO_x film was between 1.8 and 2.2, which is consistent with that of pure Ta_2O_5 or ZrO_2.[46,109-111] The electrode layer film thicknesses, including Al, Mo, MoN, and WN, were measured with a profilometer (Veeco Dektak^3 stylus).

The Zr-doped TaO_x film was characterized with various techniques. A time of flight secondary ion mass spectroscopy (ToF-SIMS) was used for the compositional depth profiling. Electron spectroscopy for chemical analysis (ESCA, Kratos Axis His 165), or known as X-ray photoelectron spectroscopy (XPS), was applied for the chemical bonding and elemental composition analysis. X-ray diffractometry (XRD, Bruker D8) was used for the study of film morphology. Transmission electron microscopy (TEM) was used to investigate the film structure and interface. Details of these techniques will be discussed in the following sections.

The setup of the electrical measurement was extremely important to obtain physically meaningful results.[7] The test geometries in this study were in general very small. For example, the gate areas used for the C-V and I-V measurements were in the range of 10^{-5}-10^{-6} cm^2. Therefore, the corresponding electrical signals were very weak,

e.g., the capacitance value C was 1-10 pF and the current value I was 1-10 pA. As a result, extra precautions were required for the instrumentation such as meters, probe station, cabling, and cable routing.[112] All of the electrical measurements were performed with a tri-axial gold-coated hot chuck that was integrated into a probe station (Signatone S-1160). The entire probe station with the corresponding wiring was then encapsulated inside an Al-made black box. This metal black box was electrically grounded to shield against exterior interferences, i.e., energy sources, such as electrical noises, light, heat, and vibration.[7] In addition, dry N_2 could also be gently blown on the surface of the tested sample to ensure the absence of moisture, which could induce a surface leakage current. The entire setup for the C-V and I-V measurements is illustrated in Figure 13.

An HP 4284A LCR meter was used to obtain high-frequency C-V curves. An HP 4140B pico-ampere meter or an HP 4155C semiconductor parameter analyzer was used for I-V curves. Quasistatic C-V curves could also be measured by the HP 4155C. Details of individual measurement will be discussed in following sections. A Labview 6®-programmed computer interface (National Instruments) was applied to manipulate the measurements and record the data.

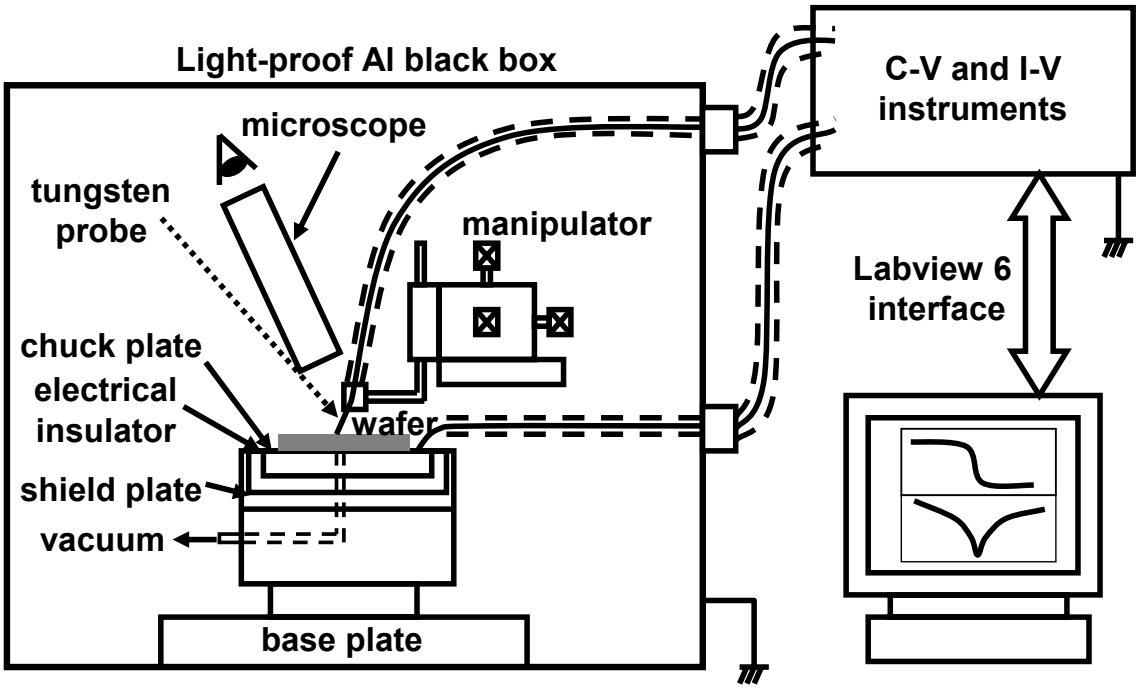

Figure 13. Setup of C-V and I-V measurements.

2.3 Structural and Chemical Characterizations

2.3.1 Time of Flight Secondary Ion Mass Spectroscopy (ToF-SIMS)

SIMS analyzes elemental as well as ion cluster concentrations in the film by sputtering atoms off the sample surface and detects them by a mass spectroscope.[108,113] A primary ion beam composed of O_2^+, Cs^+, or Ga^+ with energy of 5-20 keV impinges on the sample surface, from which the atoms are sputtered and ejected. A small portion of the ejected atoms become ionized and detected by the mass spectroscope. The mass to charge ratio of each ion is analyzed to identify the element. The sensitivity of SIMS is in the ppma range (10^{14}-10^{15} cm^{-3}) with a 1-10 μm contact area. The depth resolution is usually 5-10 nm. The mass resolution m/Δm for identification can achieve ~40000 for the state of the art instrument. Figure 14 shows the schematic illustration of SIMS.

The detection with the correct mass to charge ratio requires narrow slits, which significantly reduces the transmittance of the spectrometer to a value as low as 0.001%.[108] Time-of-flight SIMS, however, does not have this limitation. Instead of using a continuous primary ion beam for sputtering, ToF-SIMS uses pulsed ions from a liquid Ga^+ gun with a small beam diameter of ~0.3 μm. The time needed for the sputtered ions to reach the detector (flight time) is measured. The mass to charge (m/q) ratio can be related to the flight time (t_f) by,[108]

$$\frac{m}{q} = \frac{2Vt_f^{\,2}}{L^2} \qquad [9]$$

where L is the flight length, i.e., the distance from the sample to the detector, and V is the potential difference. Because ToF-SIMS does not have the narrow slits, the ion

collection is increased by 10-50%. However, it inevitably reduces the ion current and the sputtering rate. The low sputtering rate is suitable for surface analysis, which is beneficial. Since the m/q is determined solely by the time of flight, very large and very small ion fragments can be detected.

In this study, ToF-SIMS was performed on the Zr-doped TaO_x sample for profiling the different atomic concentrations from the surface of the high-k film deep into the Si substrate. The impurity diffusion and interface composition were investigated.

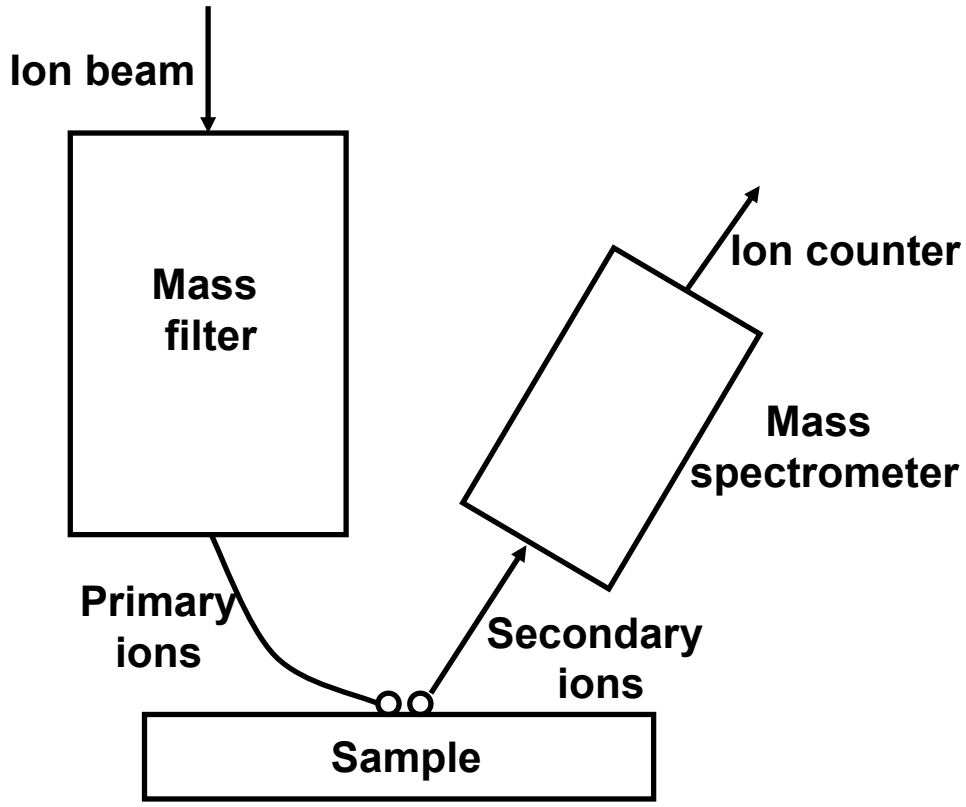

Figure 14. Schematic illustration of SIMS.

2.3.2 Electron Spectroscopy for Chemical Analysis (ESCA)

ESCA, or XPS, is a powerful tool for investigating the chemical structure and composition of the constituent elements.[108,113] Except for hydrogen (H) and helium (He), all other elements in the periodic table can be detected. When photons with an energy <50 eV are incident on a solid, electrons are ejected from the valence band, which is called ultraviolet photoelectron spectroscopy (UPS). On the other hand, if the photon energy is higher, i.e., X-ray, the electrons deeper in the core levels can be ejected, which is known as XPS. The electrons can be emitted from all the levels as long as the photon energy is larger than the electron binding energy. It is this binding energy information we seek for constructing the chemical structure. Figure 15 illustrates the XPS electron emission. An X-ray with 1-2 keV, e.g., monochromatic AlK_α (1486.6 eV), is suitable for this purpose. The measured energy of the ejected electrons E_{sp} is related to the binding energy E_b by,[108]

$$E_b = h\upsilon - E_{sp} - q\Phi_{sp} \qquad [10]$$

where $h\upsilon$ is the X-ray energy and Φ_{sp} is the work function of spectrometer (3-4 eV).

The major use of ESCA in this study was used for the chemical compound identification. By investigating the binding energy shift due to the change of chemical structure, the oxidation state of the constituent atom, i.e., Ta, Zr, O, and Si, could be identified. For example, a metal oxide showed a different binding energy than a pure metallic element. The charging effect on an insulator sample has to be compensated to obtain the real binding energy information.[108] Usually, the carbon C_{1s} emission at 284.6 eV was used as a reference to correct for this charging effect. By calculating the area

under the spectrum, a quantitative analysis of different chemical compound structures could also be performed.

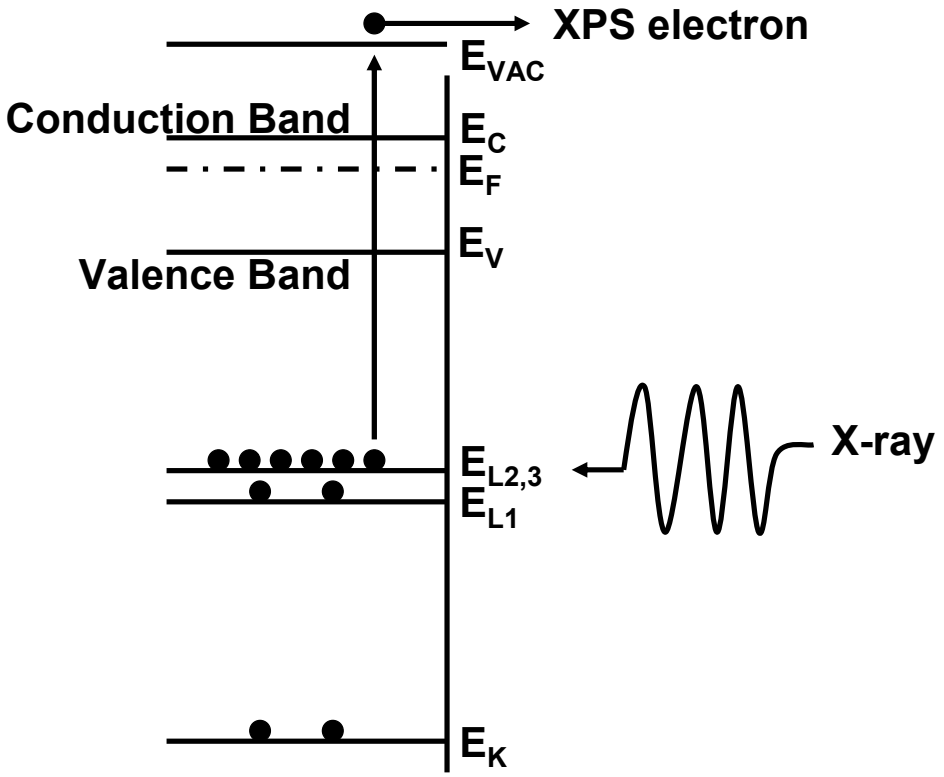

Figure 15. ESCA (XPS) theory. A core level electron is excited by X-ray into the vacuum level (E_{VAC}) and detected.

2.3.3 X-ray Diffraction (XRD)

XRD can be used to detect the transformation of the high-k gate dielectric film from amorphous to polycrystalline state.[44,106,110,114-116] The as-deposited film is usually amorphous, which does not show any sharp XRD peaks. As the annealing temperature increases, the film may transform into a well organized polycrystalline phase, which shows defined XRD peaks.[117] By comparing the XRD patterns to the reference, the crystal structures can be identified.[118]

For the XRD instrumentation, the most common X-ray source is a monochromatic CuK_α X-ray (λ = 1.5418 Å). The X-ray beam is incident on the sample surface with an angle θ, as indicated in Figure 16. A constructive interference is formed between two reflected X-ray beams by the parallel crystal plains if Bragg's law is met,[119]

$$n\lambda = 2d_{hkl} \sin\theta \qquad [11]$$

where d_{hkl} is the distance between two parallel Miller planes, i.e., spacing, with the Miller index (hkl) and n is an integer. With the fixed wave length λ = 1.5418 Å, the crystal spacing d_{hkl} is related to the scan angle θ. Both d_{hkl} and 2θ can be used to identify a diffraction peak. In addition, with the XRD information such as peak location and width (FWHM), the averaged crystallite (grain) size can also be estimated.[117]

In this study, the XRD data was recorded on a Bruker D8 Powder X-ray diffractometer, which was equipped with CuK_α radiation, a diffracted beam graphite monochromater to cut the K_β component, and a scintillation detector.[120] The data was collected at room temperature in the Bragg-Brentano geometry with a 2θ range of 10° to 70°, a step size of 0.04°, and a counting time of 2 second/step.

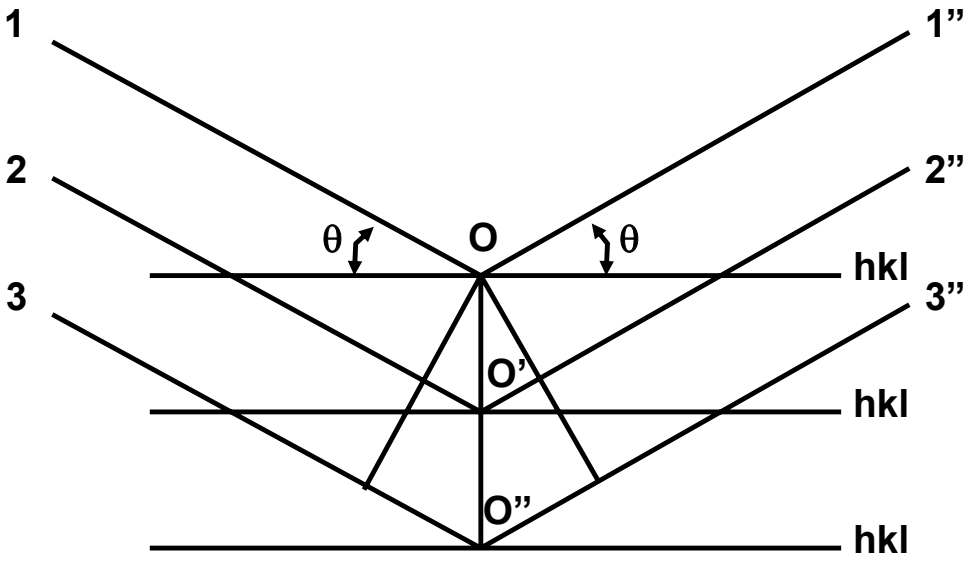

Figure 16. X-ray diffraction by parallel crystal planes.

2.3.4 Transmission Electron Microscopy (TEM)

A transmission electron microscope in principle is somewhat similar to an optical microscope.[108] It contains a series of lenses, which magnify the sample with a very high resolution of around 0.15 nm. This high resolution comes from the extremely small wave length of the electron, i.e., ~0.004 nm. The magnification of TEM can be several hundred thousand times. However, the limited depth of resolution is its main drawback, which requires an extremely small sample thickness (10-100 nm) for electrons to transmit. This increases the difficulty of sample preparation.

A schematic of TEM is shown in Figure 17. Electrons from an electron gun are accelerated to a high voltage, e.g., 100-400 kV, and focused by the condenser lenses. The transmitted and forward scattered electrons form a diffraction pattern in the back focal plane and a magnified image in the image plane. It is this diffraction pattern that provides the structural information.

Three TEM imaging modes are available: bright-field, dark-field, and high-resolution (HR). The TEM image contrast does not depend on the absorption, but on the scattering and diffraction of electrons. Images formed only by the transmitted electrons are bright-field images, and images formed by the diffracted beam are dark-field images. The image contrast is affected by mass contrast, thickness contrast, diffraction contrast, and phase contrast.[108] A high-resolution TEM (HRTEM) offers structural information on the atomic level, i.e., lattice imaging, which can be used for interface analysis. It contains a number of different diffracted beams, which combine together to form an interface image.

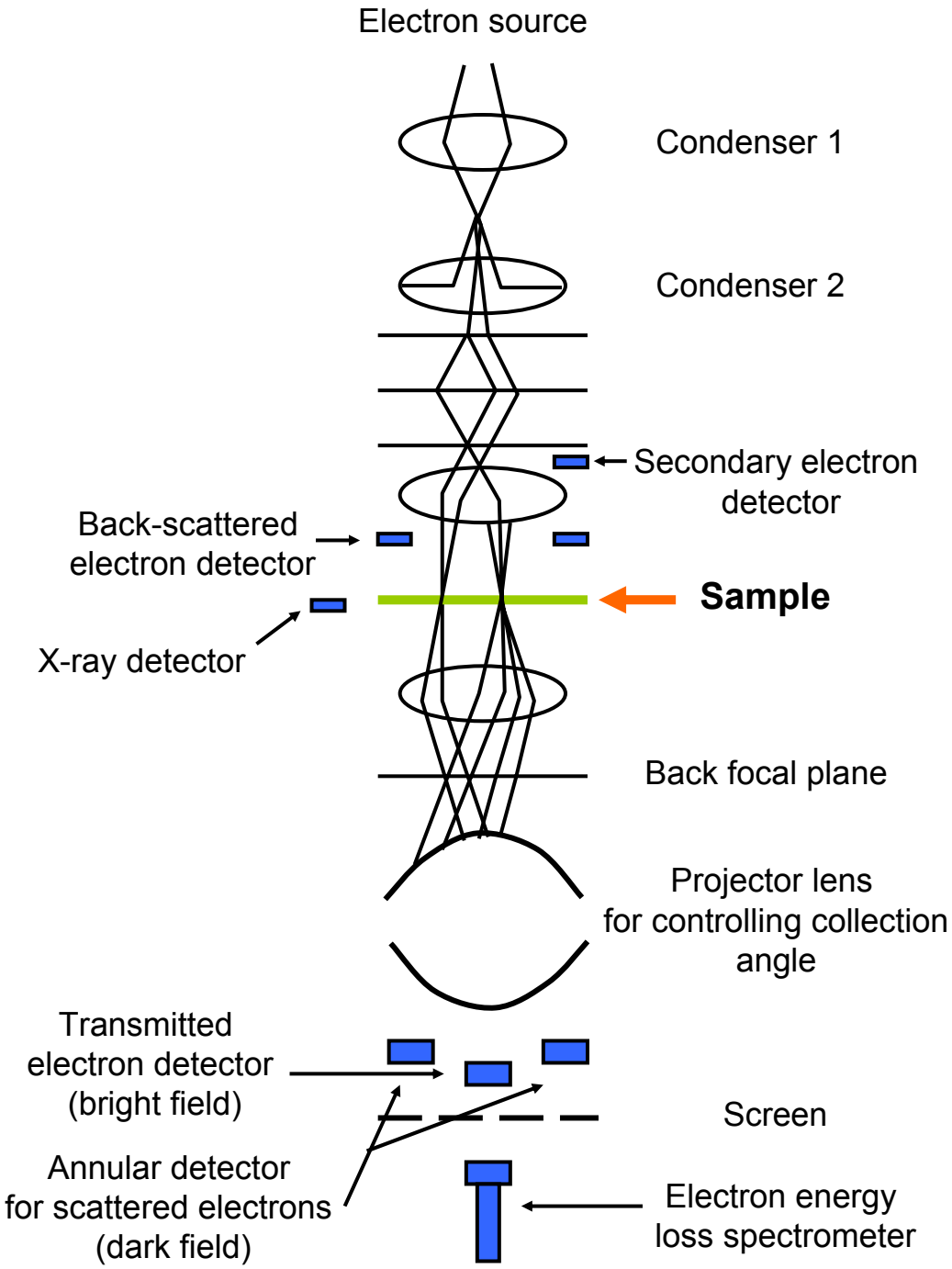

Figure 17. Schematic illustration of TEM.

2.4 Electrical Characterizations

2.4.1 High-Frequency Capacitance-Voltage (C-V) Measurement

A high-frequency C-V curve measurement can extract the film properties such as dielectric constant, EOT, fixed charges, electron traps, and mobile charges.[7,108] It also detects interface properties such as the interface state density.[8,121] The flatband voltage obtained from a C-V curve can be used to calculate the work function of the metal gate.[103,121-123] The inversion capacitance can be used to estimate the Si substrate doping concentration.[3,108] The frequency dispersion of a C-V curve can be used to indicate the film leakage characteristics.[124] The high-frequency C-V measurement is a very important technique for characterizing the dielectric film.

An HP 4284A precision LCR meter was used for the high-frequency C-V measurement in this study. If the parallel mode is chosen, both capacitance (C) and conductance (G) are obtained at the same time. It uses a linear DC voltage ramp to sweep over the bias range from accumulation to inversion or the opposite way. A small sinusoidal AC voltage (20-1M Hz) is superimposed on the DC ramped voltage to permit the measurement of differential capacitance,

$$C_{dif} = dQ / dV \qquad [12]$$

and the conductance,

$$G = dI / dV \qquad [13]$$

The LCR meter measures the device impedance, i.e., ratio of the output AC current to the input AC voltage, of the parallel G-C circuit.[108] The impedance is expressed as:

$$Z = \frac{G}{G^2 + (\omega C)^2} - \frac{j\omega C}{G^2 + (\omega C)^2} \quad [14]$$

The first term is a conductance, which is in phase (0°) with the input AC signal, and the second term is a susceptance, which is out of phase (90°) with the input. By feeding the output to a phase detector and dissociating the complex impedance into 0° and 90° phases, G and C are obtained.

There are several issues when using an LCR meter to measure a high-frequency C-V curve, especially for a very thin SiO_2 or high-k gate dielectric with a large leakage current and a substantial series resistance.[125] For example, Nicollian and Brews suggested a criteria that a small AC signal range is the one which the capacitance and conductance are independent of the AC amplitude.[126] Normally, 25-50 mV is applicable for this criteria. There are two measurement modes using the HP 4284A meter, i.e., parallel model and series mode. The results from these two modes can be transformed to each other by,[108,125]

$$C_S = C_P(1 + D^2) \quad [15]$$

where the dissipation factor is defined as,

$$D = \frac{G_P}{(2\pi f)C_p} \quad [16]$$

The appropriate mode must be used to extract the meaningful C-V data. Device qualities, such as the Si substrate doping concentration, gate electrode sheet resistance, film thickness, and gate area, have to be taken into consideration for this purpose. In addition, an improper measurement setup, e.g., cabling, can cause uncertainty. Erroneous

frequency dispersion, capacitance roll-over, or even negative capacitance can be observed if the measurement implementation is incorrect.[125] For example, a model attempting to correct for the cabling effect suggested,

$$C_p = \frac{C(1-\omega^2 CL) - G^2 L}{(Gr_S - \omega^2 CL + 1)^2 + \omega^2 (Cr_S + GL)^2} \quad [17]$$

in which a negative sign is associated with the series inductance L, which can result in a negative capacitance value. In addition to an extrinsic factor such as cabling, L may also come from an intrinsic factor of device physics.[127]

2.4.2 Low-Frequency (Quasistatic) C-V Measurement

For a high-frequency C-V measurement, e.g., the probe frequency >100 kHz, the inversion part of C-V is pinned at a minimum value because the minority carriers in the Si substrate cannot follow the frequency to contribute to the capacitance.[3] The minimum capacitance results from a series combination of the high-k gate dielectric capacitance and the Si space charge capacitance. The space charge region, i.e., depletion region, acts like a parallel plate capacitor of Si (k = 11.7) with the maximum depletion region width. To recover from the minimum capacitance, a very low probe frequency has to be used to allow the minority carriers to respond. A DC C-V measurement, i.e., a quasistatic C-V, can fulfill this requirement.[108] The quasistatic C-V is measured by the displacement current with a ramped DC bias,[108]

$$C = \frac{I_{dis}}{\left(\frac{dV}{dt}\right)} \quad [18]$$

The capacitor is charged by the displacement current I_{dis} induced by the voltage ramp dV/dt. For this technique to succeed, the leakage current through the gate dielectric layer should be negligible compared to I_{dis}. It is true for a thick SiO_2 or high-k gate dielectric film with an extremely low leakage current, e.g., $<10^{-12}$ A. However, a very large tunneling current from a very thin SiO_2 layer makes the above assumption invalid. The measured current, which includes a displacement component and a leakage component, has to be corrected in order to obtain a true quasistatic C-V curve.[128]

The HP 4155C semiconductor analyzer contains the function of compensating the leakage current through estimating the average leakage current during the DC voltage ramp. The measurement mechanism is shown in Figure 18.[129] A combination of stepwise and ramped voltage sweeps are used. As shown in the inset, the currents are measured at the stepwise portions before and after each ramp, i.e., IL_0 and IL, to obtain the average leakage current during the ramp. This average leakage current will be deducted from the measured ramp current I to obtain the true displacement current. The quasistatic capacitance is calculated by the following equation,[129]

$$C = \left(c_{int} \times \left(I - \left(1-\alpha\right) \times IL - \alpha \times IL_0\right)\right) / \left(V - V_0\right) \qquad [19]$$

where V_0 and V are the voltages before and after the ramp respectively, as defined in the inset. The integration time (c_{int}) is the time interval for measuring the ramp current I. The weighting coefficient α is given by,[129]

$$\alpha = (2k-1)/4n \qquad [20]$$

where n is the number of power line cycles required for the integration time c_{int}, and k is the number of power line cycles until the current becomes stable at each sweep step. Note that the HP 4155C can be used to measure the average leakage current, i.e., $(1-\alpha)\times IL+\alpha\times IL_0$, and the compensated quasistatic capacitance at the same time.

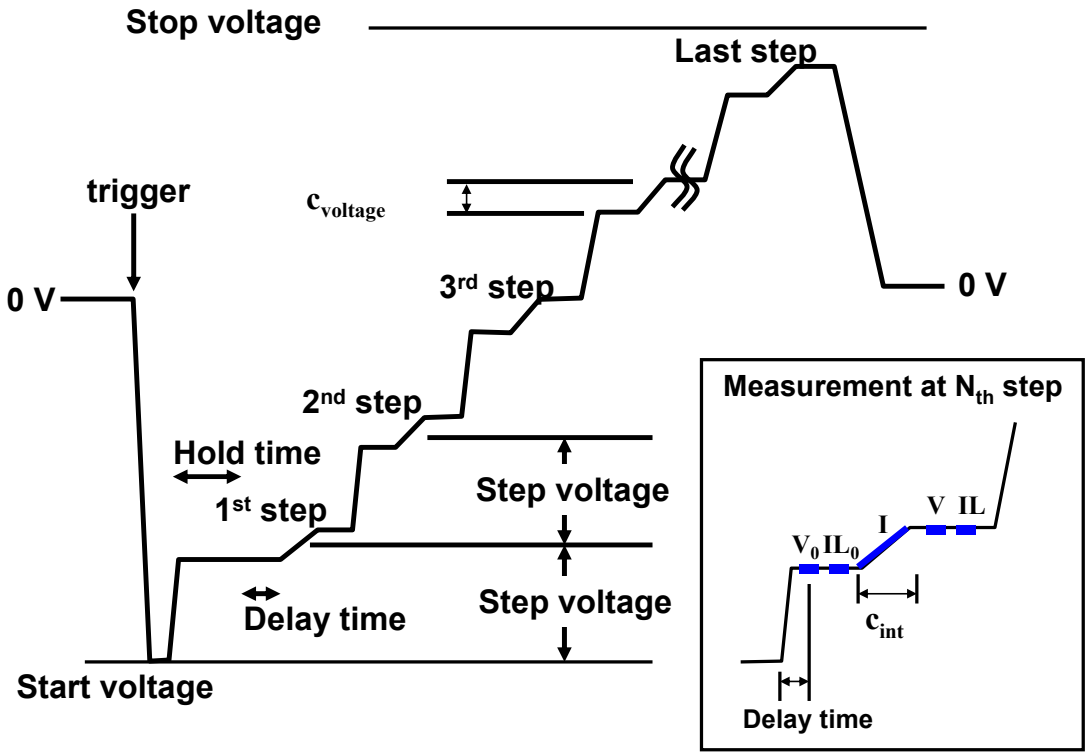

Figure 18. Mechanism of the quasistatic C-V measurement. The inset shows the measurement at the N_{th} step.[129]

A set of carefully chosen measurement parameters is the key to a successful quasistatic C-V measurement. For example, the following parameters were used in this study of an MOS capacitor containing an 8 nm-thick Zr-doped TaO_x film: hold time = 1 s, delay time = 0.5 s, step voltage = 0.05 V, $c_{voltage}$ = 0.03 V, l_{int} = 500 ms, c_{int} = 500 ms, and leakage current compliance = 1 nA.[129] If a very thin high-k gate dielectric film is too leaky, a smaller gate electrode area has to be used to prevent the leakage current from exceeding 1 nA. A higher current compliance, i.e., 10 nA, can also be used. Figure 19 shows the result of a quasistatic C-V measurement with the inset showing the average leakage current. Notice that the unsaturated inversion capacitance was observed above V_G = 2 V, which was due to the excessive leakage current as shown in the inset.

As discussed before, a quasistatic C-V curve is not always available, especially for an ultra-thin SiO_2 or high-k gate dielectric layer with a large leakage current.[108,130,131] For example, Oehrlein showed an unsuccessful endeavor to measure quasistatic C-V curves with either a ramp voltage (I-V) or a charge voltage (Q-V) method on the Al/Ta_2O_5/p-Si capacitor due to the excessive dominance of leakage current.[109] In addition, the leakage current, which either adds to or subtracts from the displacement current, usually distorts the resulting quasistatic C-V curve. The obtained inversion capacitance is not exactly the same as the accumulation capacitance.[108]

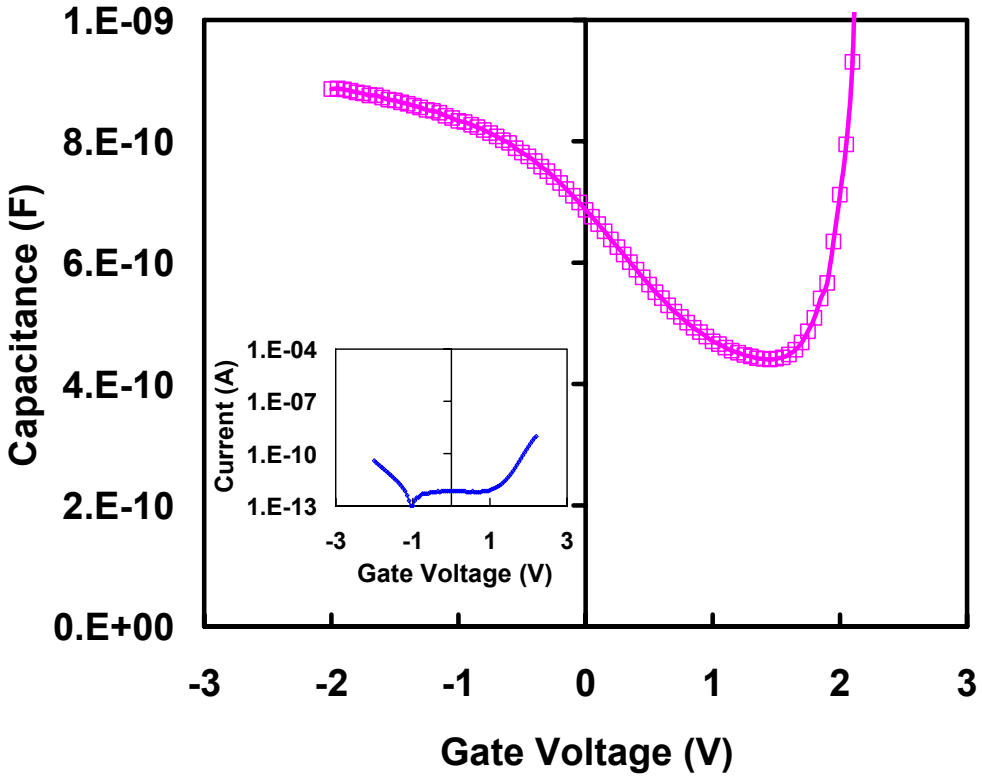

Figure 19. A typical quasistatic C-V curve after being corrected for leakage current (shown in the inset).

2.4.3 Current-Voltage (I-V) Curve Measurement

The current densities at different gate voltages, or electric fields, are measured by applying a ramped or stepwise DC bias on the top gate electrode of an MOS capacitor. The Si substrate contact, i.e., backside contact, should be electrically grounded. This was done by grounding the gold-coated hot chuck in our experiment. To realize this measurement configuration, the tungsten (W) probe that contacts the top gate electrode has to function as both a voltage source and a current detector at the same time. With an HP 4140B pico-ampere meter, the voltage source (V_A) and the current meter (I) were separated. Therefore, a special connection selector HP 16053A, which connected the guard ring of the triaxial cable on the current meter to the voltage source, is required for this purpose.[132] The guard ring of the triaxial cable needs to have the same electrical potential as that of the current meter so that no current flows through it.[7] For an HP 4155C semiconductor analyzer, however, the source/monitor unit (SMU) configuration of the voltage/current source has this function as its default.[129] No additional connector is required.

Similar to the quasistatic C-V measurements, both a displacement component and a leakage component contribute to the measured current when using a ramped voltage sweep. In the case of I-V measurements, however, the displacement current contribution has to be minimized to avoid the screening effect.[132] A very slow voltage ramp, e.g., 0.01 V/second, should be applied to reduce the displacement current, especially at the low voltage range where the leakage current is very small. Another approach is to use a stepwise voltage sweep with a long delay time, e.g., 1-2 seconds.

However, the delay time should not be set too large either to avoid an excessive electron trapping during this constant voltage stress.

2.5 Interface State Density Extraction

2.5.1 Introduction

Interface states, or interface traps, are the defects located at the interface between the Si substrate and the gate dielectric layer.[126] The origin of these traps is mainly due to the incomplete bonding of Si atoms, i.e., dangling bonds, at the transition from a perfectly arranged single crystal lattice to a completely random amorphous phase. The dangling bonds create undesired energy levels within the Si bandgap. Because these interface traps are located at the border with Si, they are electrically active and able to change their occupancy quickly by capturing and releasing electrons and holes. This quick change of trap occupancy is a distinctive difference between the interface states and other electrical defects, e.g., fixed charges and mobile ions within the gate dielectric. Because of this fast charging and discharging effect with the change of gate voltage (or more precisely the change of surface potential), the device performance is unpredictable, which causes reliability problems.[126]

Interface state density, i.e., D_{it} ($cm^{-2}eV^{-1}$), depends on the gate dielectric material itself as well as the fabrication technique. The value of D_{it} is an important index for the effectiveness of the fabrication process as well as the device performance.[108] The interface states are distributed within the Si bandgap, other than located at a single

energy level. Normally, D_{it} shows a minimum at the midgap level and increases drastically when close to the band edges.[7,108,126]

The following sections will be aimed to provide a brief discussion on various measurement techniques of D_{it}, including the low-frequency C-V method, high-frequency C-V method, high-low frequency C-V method, and conductance method. These techniques can be easily performed on a simple MOS capacitor.[7,108] Other methods, such as charge pumping and deep level transient spectroscopy (DLTS), require a more complicated MOSFET structure[133-137], which are not included in this study. The working theory and experimental setup associated with each technique will be presented. However, as the dielectric film gets thinner, the D_{it} measurements based on the interface capacitance effect is no longer applicable due to the decreased voltage shift associated with the interface traps. This phenomenon has been observed in the Terman and high-low frequency C-V methods.[125] Precautions must be taken for getting physically meaningful data.

2.5.2 Low-Frequency Capacitance-Voltage Method

The low-frequency C-V, or quasistatic C-V, measures the capacitance at a frequency so low that all the interface traps can respond and contribute to the capacitance value.[108] Actually, only the quasistatic C-V curve that is measured with a DC voltage sweep can meet this stringent requirement. The low frequency measured C-V curve can be compared with an ideal calculated C-V curve that is free of interface states. The difference between these two curves can be used to extract D_{it}.[138] The

sensitivity of this technique is ~10^{10} $cm^{-2}eV^{-1}$, depending on how accurate the quasistatic C-V measurement can be done.[126]

The calculation of the ideal C-V curve can be found in many textbooks.[3,108,126] First, the induced semiconductor carrier density ($Q_{Si}^{'}$) is calculated.[3] For accumulation and depletion regions (assuming a p-Si substrate), it is,

$$Q_{Si}^{'} = \mp 9.282\times10^{-17}\sqrt{N_A^-}\left[\frac{q\Psi_S}{kT}+\exp\left(-q\Psi_S/kT\right)-1\right]^{1/2} \quad [21]$$

in which a positive sign (+) is applied for the accumulation and a negative sign (-) for the depletion. Ψ_S is the surface potential. For inversion, $Q_{Si}^{'}$ is given by,

$$Q_{Si}^{'} = -\sqrt{2}\varepsilon_{Si}\left(\frac{kT}{qL_D}\right)\times\left\{\left[\frac{q\Psi_S}{kT}+\exp\left(-q\Psi_S/kT\right)-1\right]+\left(\frac{n_i}{N_A^-}\right)^2\left[\exp\left(q\Psi_S/kT\right)-1\right]\right\}^{1/2} \quad [22]$$

where the Debye length is,

$$L_D = \sqrt{\frac{\varepsilon_{Si}kT}{q^2N_A^-}} \quad [23]$$

and the Si bulk potential is,[3]

$$\Psi_b = -\left(kT/q\right)\ln\left(N_A^-/n_i\right) \quad [24]$$

Then, the gate voltage (V_G) under accumulation is given by,

$$V_G = V_{FB}^0 - \frac{|Q_{Si}^{'}|}{C_{ox}^{'}} + \Psi_S \quad [25]$$

and under depletion and inversion,

$$V_G = V_{FB}^0 + \frac{|Q'_{Si}|}{C'_{ox}} + \Psi_S \quad [26]$$

where V_{FB}^0 is the ideal flatband voltage. Therefore, the semiconductor capacitance density under accumulation and depletion is given by,

$$C'_{Si} = 1.785 \times 10^{-15} \sqrt{N_A^-} \left| \frac{\left[1 - \exp(-q\Psi_S / kT)\right]}{\left[\frac{q\Psi_S}{kT} + \exp(-q\Psi_S / kT) - 1\right]^{1/2}} \right| \quad [27]$$

Finally, the ideal MOS capacitance, which is a series combination of the gate dielectric capacitance and the semiconductor capacitance, is,

$$C'_{dif} = \frac{1}{1/C'_{ox} + 1/C'_{Si}} \quad [28]$$

With Eqs. 21-28, we can construct the ideal high-frequency C-V curve by assuming the inversion capacitance is pinned at $\Psi_s = 2|\Psi_b|$, where C_{Si}' is due to the space charge capacitance at the maximum depletion depth x_{dmas},

$$C'_{dif} = \frac{1}{\frac{t_{ox}}{\varepsilon_{ox}} + \frac{x_{d\,max}}{\varepsilon_{si}}} \quad [29]$$

where,

$$x_{d\,max} = \sqrt{\frac{2\varepsilon_{si}(2\Psi_b)}{qN_A^-}} \quad [30]$$

For the ideal low-frequency C-V curve, which only differs from the high-frequency C-V under inversion ($\Psi_s > 2|\Psi_b|$),[3]

$$C'_{Si} = \frac{\varepsilon_{Si}}{\sqrt{2}L_D} \times \left| \frac{\left[1 - \exp(-q\Psi_s / kT) + \left(\frac{n_i}{N_A^-} \right)^2 \exp(q\Psi_s / kT) \right]}{\left\{ \left[\frac{q\Psi_s}{kT} + \exp(-q\Psi_s / kT) - 1 \right] + \left(\frac{n_i}{N_A^-} \right)^2 \left[\exp(q\Psi_s / kT) - 1 \right] \right\}^{1/2}} \right| \quad [31]$$

Putting the result of Eq. 31 back into Eq. 28, the ideal low-frequency C-V curve is obtained. Figure 20 shows an example of this calculation for a 5 nm-thick ideal SiO_2 layer on a p-type Si substrate ($N_A^- = 1\times10^{15}$ cm^{-3}) and with an Al gate ($V_{FB}^0 = -0.806$ V).

The existence of the interface traps modifies the low frequency capacitance (C_{LF}') under depletion and weak inversion by contributing to the semiconductor capacitance.[7,108,126] An additional interface capacitance (C_{it}') is in parallel with C_{Si}':

$$C'_{LF} = \frac{1}{\frac{1}{C'_{ox}} + \frac{1}{C'_{Si} + C'_{it}}} \quad [32]$$

where the interface state density is related to the interface state capacitance by $D_{it} = C_{it}'/q$. Therefore, D_{it} is calculated by,[108]

$$D_{it} = \frac{1}{q}\left(\frac{C'_{ox} C'_{LF}}{C'_{ox} - C'_{LF}} - C'_{Si} \right) \quad [33]$$

Eq. 33 is the final form that is used for the D_{it} extraction.

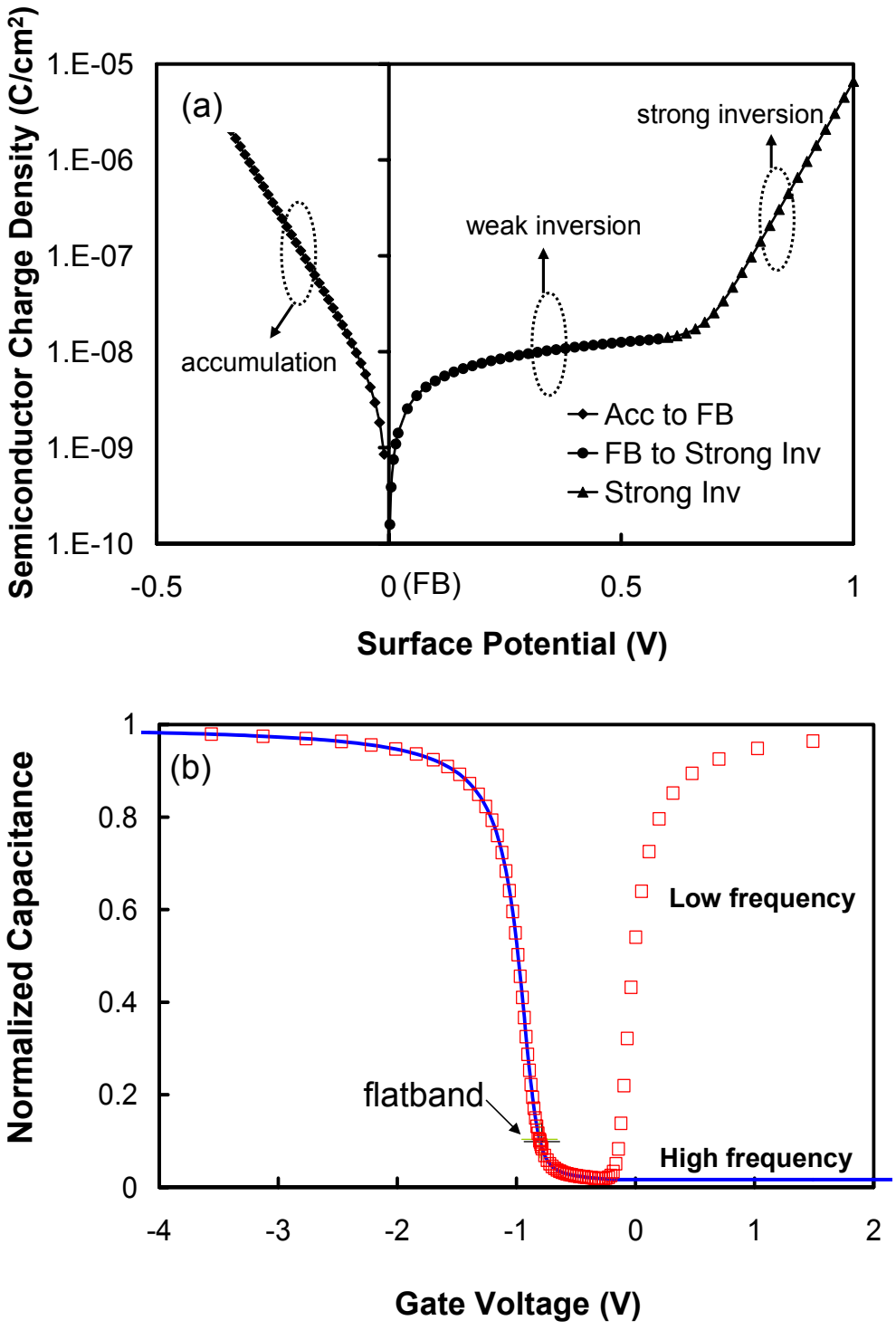

Figure 20. (a) Semiconductor charge density, and (b) ideal high- and low-frequency C-V curves for an 5 nm-thick ideal SiO_2 layer.

The calculation of the surface potential (Ψ_S) from the measurable gate voltage (V_G) was proposed as,[138]

$$\Psi_S = \int_{V_{FB}}^{V_G} \left(1 - \frac{C'_{LF}}{C'_{ox}}\right) \Delta V_G \qquad [34]$$

where the flatband voltage (V_{FB}) can be estimated by,[108]

$$\frac{C'_{FB}}{C'_{ox}} = \frac{1}{1 + \frac{136\sqrt{T/300}}{EOT \times \sqrt{N_A^-}}} \qquad [35]$$

in which the EOT is in cm, N_A^- in cm^{-3}, and T in Kelvin. However, Eq. 35 is only applicable to a sufficiently thick Si substrate with a uniform doping concentration. For a thin active Si layer, such as in the case of silicon-on-insulator (SOI) wafers, and/or a nonuniformly doped substrates, an alternative method based on a measured high-frequency C-V curve has been proposed.[139] This method calculates the second derivative of $(1/C_{HF})^2$ with respect to V_G. By plotting this second derivative versus V_G, a maximum occurs at the flatband voltage V_{FB}. Figure 21 demonstrates this technique, which shows the capacitance (C), the reciprocal of its square ($1/C^2$), the 1st and 2nd derivative of ($1/C^2$) with respect to V_G. A maximum shows up at V = 0.05 V, indicating the flatband voltage location. The sample in the figure contained a 40 W Zr-doped TaO_x film (EOT = 3.2 nm) with a Mo gate.

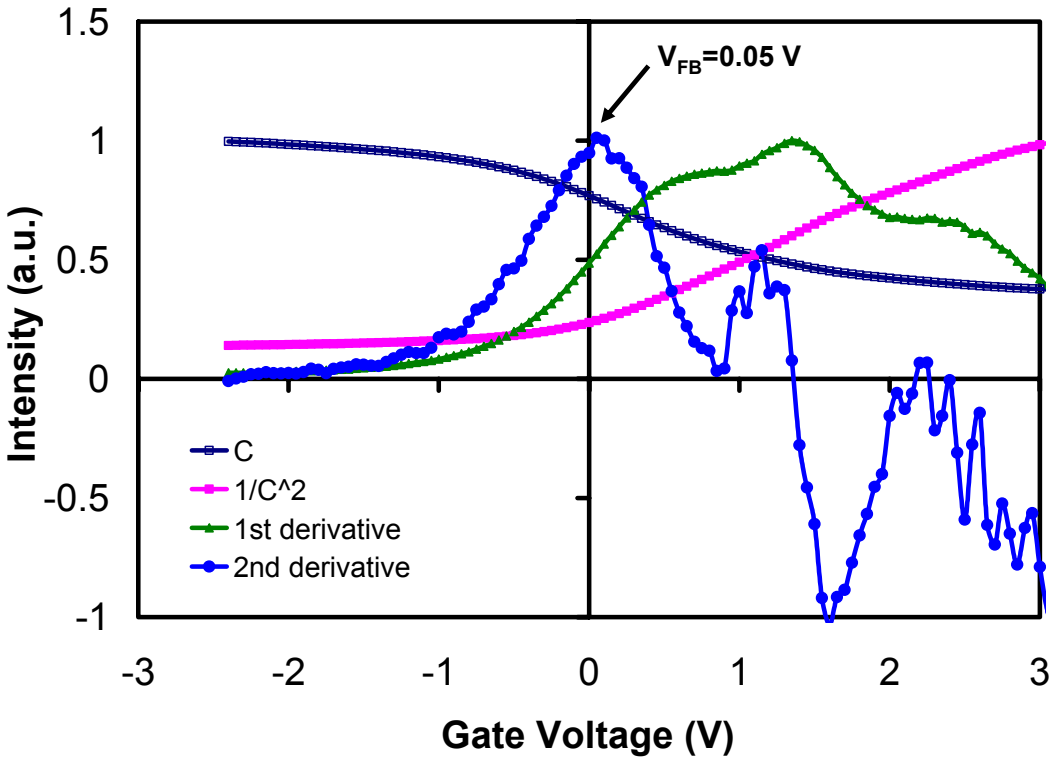

Figure 21. Flatband voltage (V_{FB}) determination using the second derivative of ($1/C_{HF}^2$) with respect to V_G. The maximum of this 2nd derivative indicates V_{FB} = 0.05 V. The sample contained a 40 W Zr-doped TaO_x film (EOT = 3.2 nm) with a Mo gate.

2.5.3 High-Low Frequency Capacitance-Voltage Method

The calculation of the ideal C-V curve, i.e., Eq. 21-31, is not only time consuming, but also introduces uncertainty especially for aggressively scaled gate dielectrics.[108] It was proposed to combine a high-frequency C-V curve with a low-frequency C-V curve to avoid the ideal C-V calculation.[140] From the high frequency C-V, we have

$$C'_{HF} = \frac{C'_{ox} C'_{Si}}{C'_{ox} + C'_{Si}} \qquad [36]$$

Therefore,

$$C'_{Si} = \frac{C'_{ox} C'_{HF}}{C'_{ox} - C'_{HF}} \qquad [37]$$

Substituting Eq. 37 into Eq. 33, we have,[108]

$$D_{it} = \frac{C'_{ox}}{q}\left(\frac{C'_{LF}/C'_{ox}}{1 - C'_{LF}/C'_{ox}} - \frac{C'_{HF}/C'_{ox}}{1 - C'_{HF}/C'_{ox}} \right) \qquad [38]$$

With Eq. 38, D_{it} can be calculated without the calculation of an ideal C-V curve.

D_{it} is commonly presented as a function of the trap energy level (E_t) with respect to the valance band edge E_V. Figure 22 shows an example of D_{it} distribution with the high-low frequency C-V method. The sample under testing was a 40 W Zr-doped TaO_x film, i.e., the atomic ratio Zr/(Ta+Zr) = 0.33, with EOT = 4 nm and an Al gate electrode. The inset shows the measured high and low frequency C-V curves.

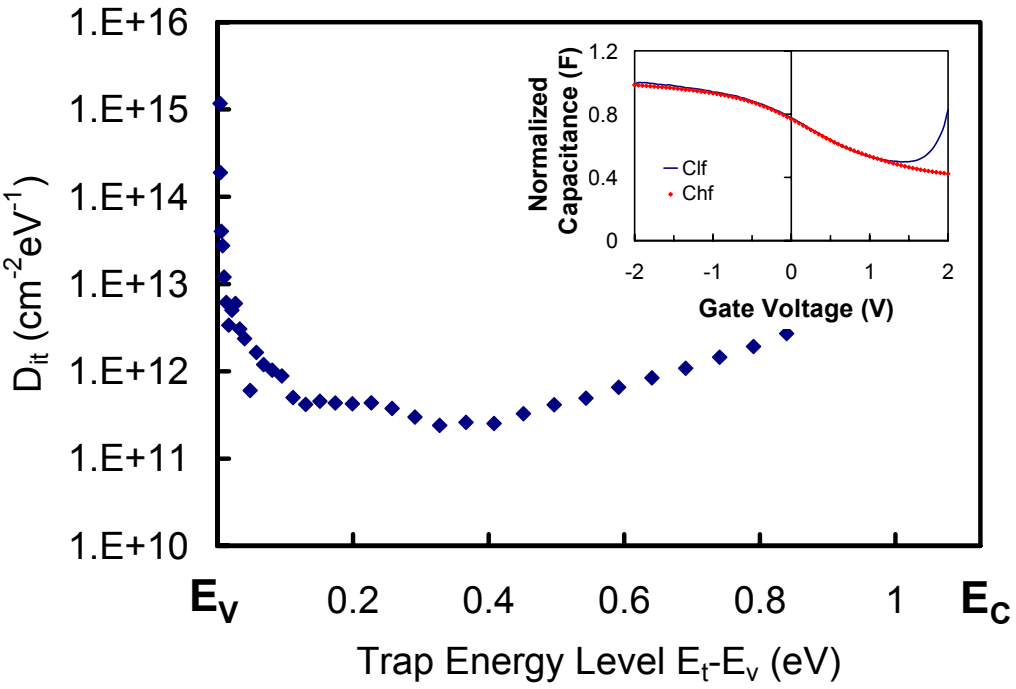

Figure 22. Interface state density (D_{it}) extracted by the high-low frequency C-V method, with the inset showing the C-V curves. The sample was a 40 W Zr-doped TaO_x film, i.e., the atomic ratio Zr/(Ta+Zr) = 0.33, with EOT = 4 nm and an Al gate electrode.

2.5.4 High Frequency Capacitance-Voltage Method

Terman first used the high-frequency C-V method to calculate D_{it}.[141] A sufficiently high probe frequency for the small AC signal is used so that no interface traps can respond and contribute to the measured capacitance value. However, the interface traps can still respond to the slowly varying DC gate bias due to the occupancy changes during deletion and weak inversion.[7,108,126] This response causes the C-V curve to stretch out along the gate bias axis. In other words, an extra gate voltage is required for an MOS capacitor due to the interface trap charging Q_{it},[108]

$$V_G = V_{FB} + \Psi_S + V_{ox} = V_{FB} + \Psi_S + \frac{\left(Q_{sp} + Q_{inv} + Q_{it}\right)}{C_{ox}} \qquad [39]$$

where Q_{sp} and Q_{inv} are the space charges and inverted charges, respectively. For a given surface potential Ψ_s, V_G varies proportionally with the interface state density. By comparing the measured high-frequency C-V curve with an ideal one, the extent of stretch-out can be used to extract D_{it}. The procedure is as follows: on the ideal high-frequency C-V curve, find Ψ_s for a given C_{HF}. Then find the V_G on the measured C-V curve for the same C_{HF}, which gives one data point of (Ψ_s,V_G). Repeat this procedure until the whole (ψ_s vs. V_G) plot is constructed. This plot contains the relevant D_{it} information.[108]

The interface state density can be found by,[126]

$$D_{it} = \frac{C'_{ox}}{q}\left(\frac{dV_G}{d\Psi_S} - 1\right) - \frac{C'_{Si}}{q} = \frac{C'_{ox}}{q}\frac{d\left(\Delta V_G\right)}{d\Psi_S} \qquad [40]$$

where ΔV_G is the gate voltage deviation from the ideal C-V curve to the experimental curve. The Terman method is applicable to D_{it} as low as ~10^{10} $cm^{-2}eV^{-1}$.[108] It is limited by the inaccurate capacitance measurement and insufficient high probe frequencies.[142] The numerical differentiation of the gate voltage shift (ΔV_G) with respect to the surface potential introduces additional uncertainty. Figure 23 shows an example of Terman method.

There is a simplified version of the high-frequency C-V method that was proposed by Lehovec.[143] This method, however, is only suitable for estimating the D_{it} value at the flatband condition,

$$D_{it} = \frac{\left(C'_{ox} - C'_{FB}\right)C'_{FB}}{3\left(dC'/dV\right)_{FB} qkT} - \frac{C'^{\,2}_{ox}}{\left(C'_{ox} - C'_{FB}\right)q^2} \qquad [41]$$

where C_{FB}' is the capacitance density at the flatband voltage V_{FB}. This method is not as sensitive as the original high-frequency C-V method and is incapable of obtaining the D_{it} distribution inside the bandgap.[108] However, it offers a fast and convenient way to assess the process parameters among different experiments and then facilitate the process optimization.[144,145] Fig. 23(b) compares the D_{it} value (at V_{FB}) from Lehovec's method with that from Terman's method. Good agreement was achieved.

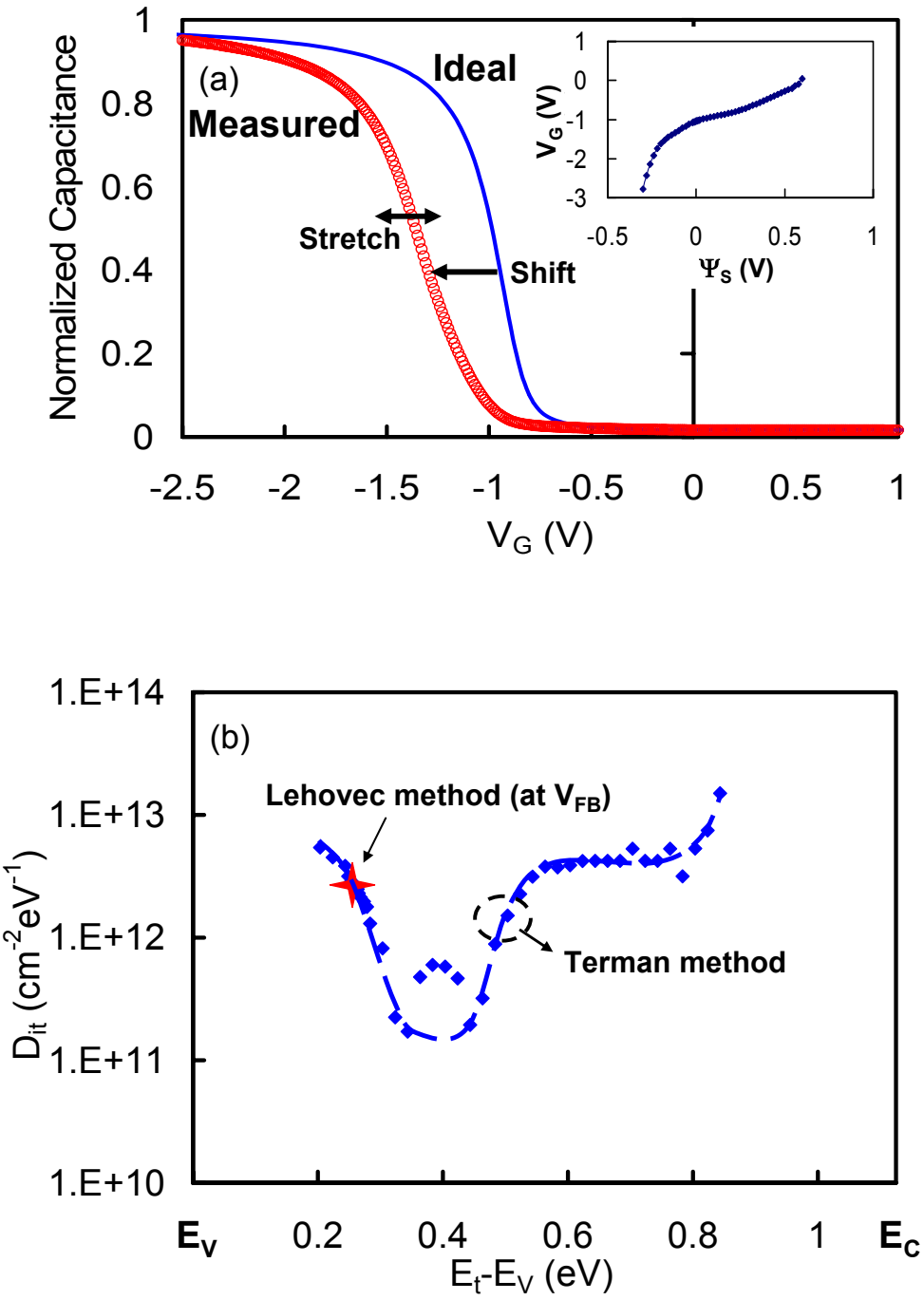

Figure 23. (a) Ideal and measured C-V curves. The inset shows the plot of V_G vs. Ψ_S. (b) D_{it} extracted with Terman and Lehovec methods. The sample was an 8 nm, 700°C-annealed 40 W Zr-doped TaO_x film with an Al gate.

2.5.5 Conductance Method

The conductance method, proposed by Nicollian and Goetzberger, has been considered the most sensitive technique for determining D_{it}, i.e., ~10^9 $cm^{-2}eV^{-1}$.[121,126] In addition, it provides information on the corresponding capture cross section as well. However, the measurement is tedious. The equivalent parallel conductance G_p, which indicates the energy loss due to the capture and emission of carriers by interface traps, has to be measured as a function of probe frequency (G_p vs. f) at different gate biases (V_G). Each (G_p vs. f) plot gives one point of D_{it} inside the Si bandgap. To construct the entire D_{it} distribution in the bandgap, the same measurement has to be repeated at several V_G, corresponding to different Ψ_S.[126]

Figure 24(a) shows the equivalent circuit of an MOS capacitor with interface traps in the gate dielectric layer. It contains the oxide capacitance C_{ox}, the semiconductor capacitance C_{Si}, and the interface trap capacitance C_{it} and resistance R_{it}, respectively. This circuit can be simplified to (b) with C_p' and G_p' expressed by,[108]

$$C_p' = C_{Si}' + \frac{C_{it}'}{1 + (\omega\tau_{it})^2} \qquad [42]$$

$$\frac{G_p'}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \qquad [43]$$

Note that the capacitance and conductance densities are shown, i.e., $C_p' = C_p/A$ and $G_p' = G_p/A$. The interface trap capacitance density C_{it}' is equal to qD_{it} and the angular frequency ω is $2\pi f$. The interface trap time constant, i.e., $\tau_{it} \equiv R_{it}C_{it}'$, can be expressed as,

$$\tau_{it} = \left[v_{th}\sigma_p N_A^- \exp(-q\Psi_S / kT)\right]^{-1} \qquad [44]$$

where v_{th} is the thermal velocity, and σ_p is the capture cross section.[108]

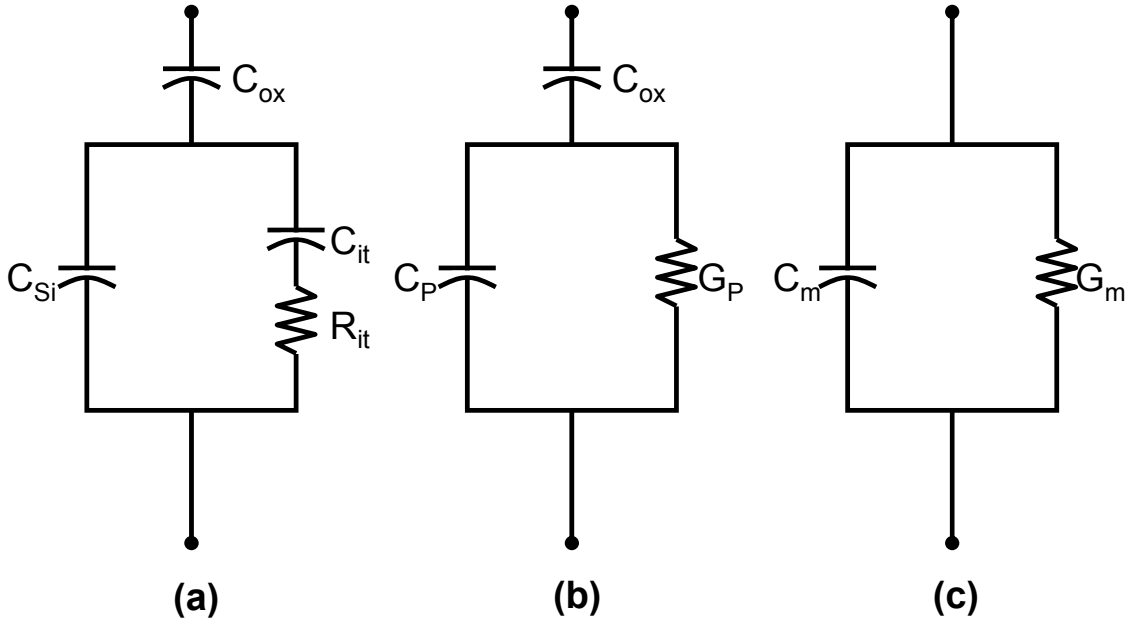

Figure 24. (a) An equivalent circuit of an MOS device with interface traps in the gate dielectric; (b) a simplified model of (a); (c) the model for real C-V measurements in the parallel mode.[108]

Eqs. 42 and 43 are only valid for a simplified case, i.e., assuming a single energy level for all interface traps.[108] Most of the gate dielectrics, however, have a continuous D_{it} distribution inside the Si energy bandgap.[126] The charge capture and emission by the interface traps mainly occur above and below a few kT/q of the Fermi level. Therefore, the corrected conductance becomes,[108]

$$\frac{G_p^{'}}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] \qquad [45]$$

Based on Eq. 43 or 45, the plot of $G_p^{'}/\omega$ versus ω gives a maximum, either at $\omega = 1/\tau$ for Eq. 43 or at $\omega \sim 2/\tau_{it}$ for Eq. 45. In other words, the conductance method gives $D_{it} = 2(G_p^{'}/\omega)/q$ with a time constant $\tau_{it} = 1/\omega$ for a single trap energy level, or $D_{it} = 2.5(G_p^{'}/\omega)/q$ with $\tau_{it} \sim 2/\omega$ for a continuous trap level distribution.

The concept of the conductance method can be visualized in the following way.[126] At a very low probe frequency, the interface traps change occupancy in phase with the small AC signal. The equilibrium is maintained and no energy loss occurs, so $G_p^{'}$ is minimized. As the frequency increases, some of the interface traps can no longer respond in time but lag behind, resulting in the increased energy loss and $G_p^{'}$. However, when the frequency increases further, most of the interface traps can not change occupancy at all, so the energy loss and $G_p^{'}$ start to decrease. At a very high frequency, none of the interface traps can respond and change occupancy, so the energy loss and G_p' are again minimized. As a result, there is a peak showing at a medium frequency.

Figure 25 shows an example of the conductance method with the inset showing the plot of $G_p^{'}/\omega$ versus ω. In general, a capacitance meter such as the HP 4284A

assumes the MOS device under testing has a parallel combination of capacitance C_m and conductance G_m, as shown in Fig. 24(c). G_p'/ω can be expressed in terms of C_m' and G_m' as,[108]

$$\frac{G_p'}{\omega} = \frac{\omega G_m' C_{ox}'^{\,2}}{G_m'^{\,2} + \omega^2 \left(C_{ox}' - C_m'\right)^2} \qquad [46]$$

The AC probe frequency should be accurately determined and the signal magnitude should be no larger than 50 mV, as explained earlier in the section for the high frequency C-V measurement.

To end this section, we compared the D_{it} distributions extracted by different techniques, as shown in Figure 26, which included Terman, high-low frequency C-V, conductance, and Lehovec methods. The sample for the illustration had an 8 nm-thick 40W Zr-doped TaO_x dielectric layer with an Al gate electrode. A 700°C-O_2 post-deposition annealing and a 300°C-forming gas post-metal annealing were performed. As expected, Fig. 26 shows that the conductance and Terman methods had better sensitivities. Due to the film leakage current that was not totally compensated for the quasistatic C-V measurement, the obtained low-frequency capacitance was slightly larger than the real value. This resulted in a higher D_{it} if the high-low frequency C-V method was used.[108] As for the conductance and Terman methods, where the film leakage had minor effect, as long as the high-frequency C-V and G-V were correctly measured, better sensitivity could be expected.

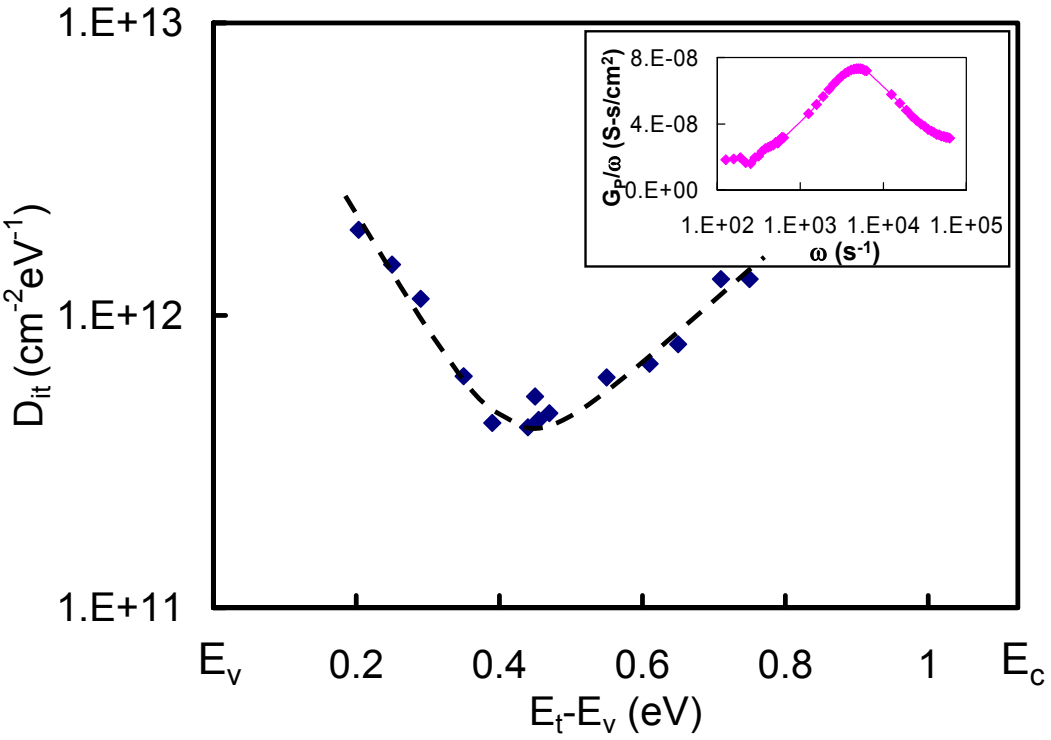

Figure 25. D_{it} distribution of an 8 nm 700°C-annealed 20 W Zr-doped TaO_x film determined by the conductance method. The inset shows the frequency-corrected conductance (G_p'/ω) as a function of angular frequency (ω). An Al gate was used.

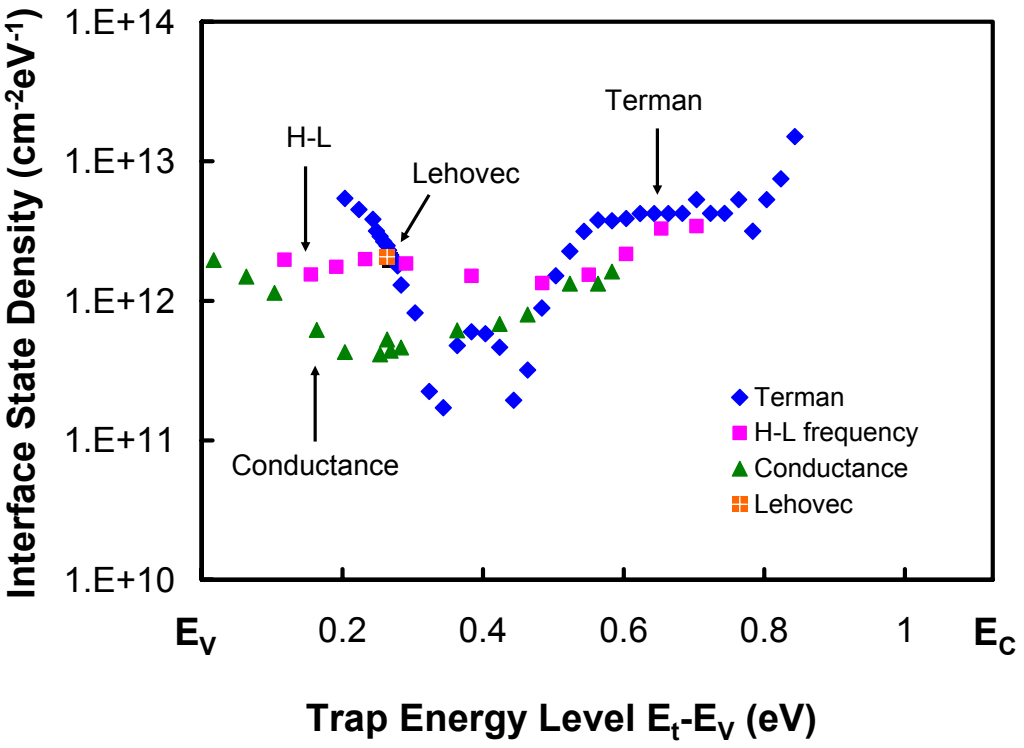

Figure 26. Comparison among Terman method (diamond), high-low frequency C-V method (square), conductance method (triangle), and Lehovec method at V_{FB} (cross). The sample had an 8 nm-thick 40 W Zr-doped TaO_x dielectric layer, which was annealed at 700°C for 10 minutes in O_2. An Al gate was used.

2.6 Process Optimization

In this study, countless experimental parameters could be varied. To name a few, the following parameters could be taken into consideration: dopant concentration, substrate pre-treatment, sputtering power, deposition temperature, deposition pressure, gun to sample distance, post-deposition thermal treatment (gas type, pressure, temperature, duration), gate electrode, etch chemistry, and so on.[9,46,106] Within a limited time frame, it is impossible to cover them all. Therefore, some of these parameters had to be optimized first and remained fixed throughout the entire study. For the next two sections, two parameter optimizations will be presented, i.e., the sputtering gas composition and the O_2-annealing pressure. Electrical characteristics such as dielectric constant, current density, and defect density were measured.

2.6.1 Sputtering Gas Composition Optimization

The reactive sputtering technique, unlike chemical vapor deposition, can deposit non-stoichiometric films. The sputtering gas composition is a key factor to control the film's composition.[46,146] For example, it was found that a non-conductive TaO_x film could be deposited by a reactive sputtering with a minimum O_2 content of 2.5% (97.5% Ar); however, a stoichiometric Ta_2O_5 film needs to be deposited from an Ar/O_2 mixture with at least 10% O_2. Above 10%, only the oxygen concentration close to the film surface was changed without changing the bulk concentration.[147] Of course, this experimental condition only served as a guideline because it varies with different instrumental setups and deposited materials. The O_2 pressure at the initial stage of the

reactive sputtering plays a dominant role in determining the film leakage and dielectric breakdown through the influence on the interface thickness and composition.[148] It has been theoretically confirmed that there exists a critical O_2/Ar ratio at a given sputtering power (or ion current) below which Ta in the film is not fully oxidized.[146]

In this study, the sputtering gas composition, i.e., $O_2/(Ar+O_2)$, was systematically varied. While other deposition parameters during reactive sputtering were kept fixed, i.e., total gas flow = 40 sccm, total operation pressure = 5 mTorr, Zr co-sputtering power = 40 W, Ta co-sputtering power = 100 W, and deposition time = 5 minutes, the gas flow rate ratios of $O_2/(Ar+O_2)$ were varied among 33%, 50%, and 80%. The deposited films, after a 700°C-O_2 post-deposition annealing, were made into MOS capacitors to investigate the electrical properties. WN gate electrodes with a 400°C-N_2 post-gate annealing were used here. Finally, a 400°C-forming gas annealing was performed after the devices were finished. The measured C-V and I-V curves are shown in Figure 27(a)-(f). For the C-V curves, it was observed that increasing the O_2 concentration during sputtering reduced the frequency dispersion among 100 kHz, 10 kHz, and 1 kHz, but degraded the hysteresis in the depletion region. For the I-V curves, however, the breakdown voltage (V_{BD}) was slightly decreased with the increased O_2 concentration.

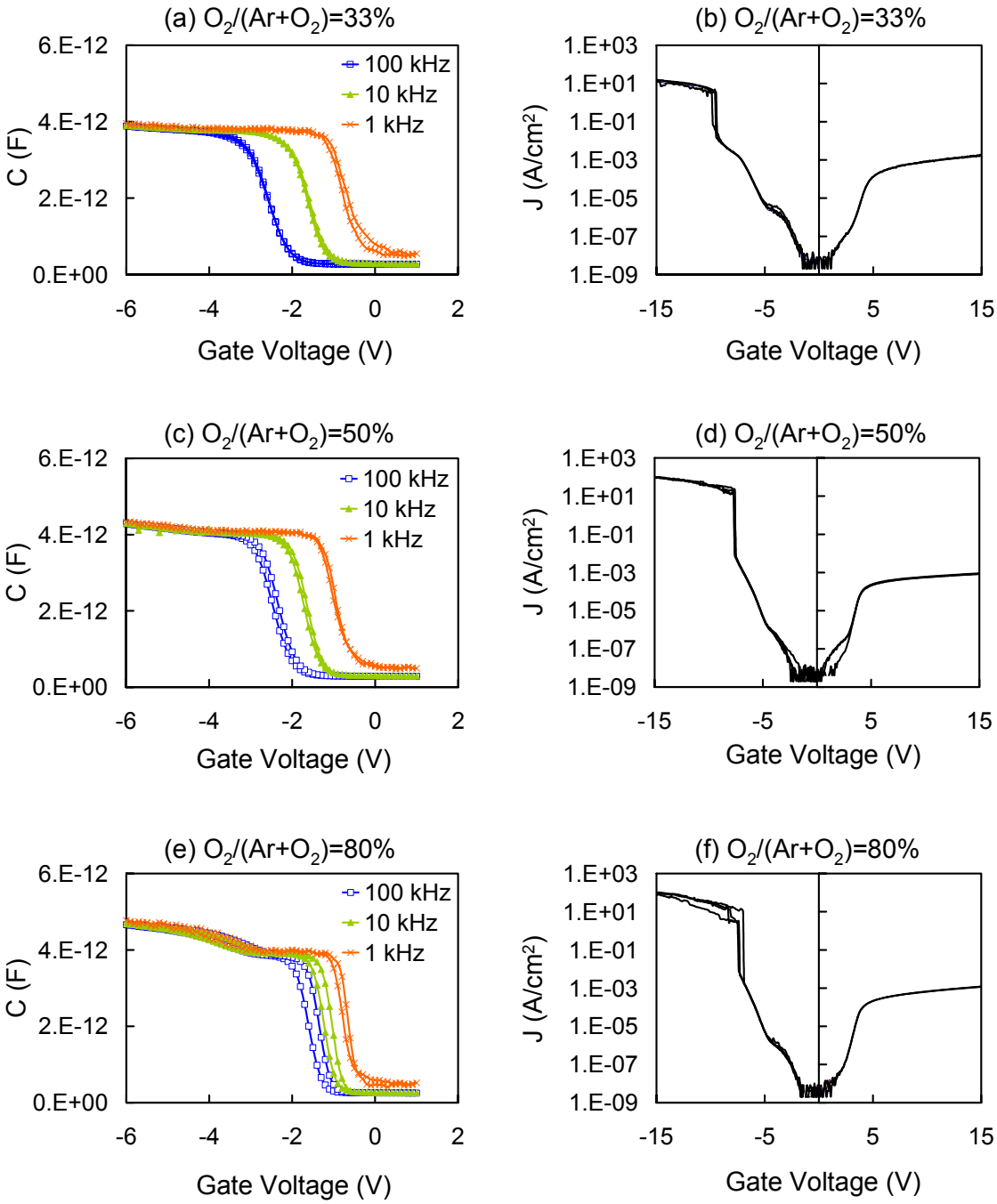

Figure 27. C-V and I-V curves of the 40 W Zr-doped TaO_x films. The $O_2/(Ar+O_2)$ ratios during sputtering were (a) and (b): 33%. (c) and (d): 50%. (e) and (f): 80%.

Figure 28(a)-(g) summarize this O_2 concentration influence on the electrical properties. Fig. 28(a) shows that the EOT decreased as the O_2% was increased. There were two possible explanations: (i) the film physical thickness was decreased, and (ii) the film dielectric constant was increased.[4,46] Fig. 28(b) shows that the current density was also decreased with the increased O_2 content, possibly due to a more complete oxidation and a denser film.[148] In (c) and (d), the breakdown strength and the flatband voltage decreased slightly with the increase of the O_2 content. However in (e), the hysteresis increased about five times as the O_2 content was increased from 33% to 80%. Actually, this detrimental degradation of the hysteresis became the determining factor for choosing an optimal O_2 concentration during sputtering. Finally, the frequency dispersion decreased slightly while the interface state density remained constant as the O_2 concentration was increased, as shown in Fig. 28(f) and (g), respectively.

Having taken all of the effects into account, a sputtering gas composition of O_2/(O2+Ar) = 50% was chosen as our optimal benchmark condition. This composition has worked quite well for all of the Zr dopant concentrations in this study. There is one point worth mentioning: all of the Zr-doped TaO_x films were annealed at 700°C for 10 minutes in an O_2 ambient (200 Torr). Even with this post-deposition O_2 annealing, the difference in electrical properties due to the sputtering gas composition could not be compensated. Therefore, the sputtering gas composition definitely affects the film's composition as well as the interface properties.

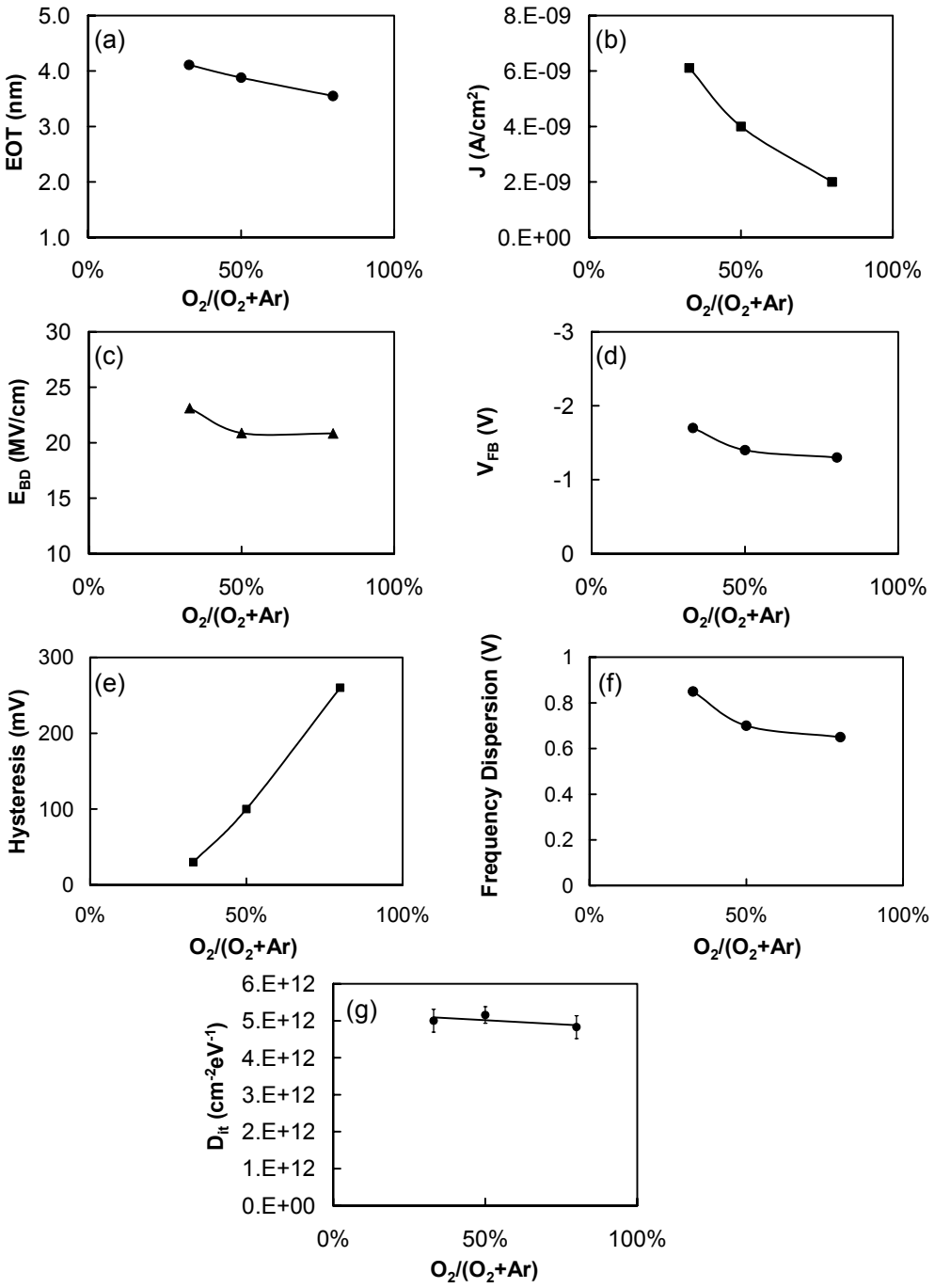

Figure 28. (a) EOT, (b) J, (c) E_{BD}, (d) V_{FB}, (e) hysteresis, (f) frequency dispersion, and (g) D_{it}, as a function of the O_2 content. WN gates were used for fabricating capacitors.

2.6.2 Oxygen-Annealing Pressure Effects

The post-deposition annealing serves many functions, such as compensation for oxygen vacancies, amends of plasma damages, densification of films, and introduction of dopants.[4,44,46,87,149-151] However, detrimental effects are also expected. The excessive growth of the interface layer and the inter-diffusion of impurities are two infamous examples.[21,84,152,153] Therefore, the annealing conditions, including gas type, pressure, temperature, and duration, have to be carefully optimized. Inert annealing gases, e.g., N_2 and Ar, have been applied for defect amendment and film densification.[70,130,154,155] However, they might not be effective for a sputter-deposited film, which needs oxygen to further oxidize.[46,146,147] Actually, even under an inert gas annealing ambient, a certain amount of O_2 is still present.[21] In this study, a pure O_2 ambient at a low pressure was used for post-deposition annealing.

The O_2 pressure is the key to the optimization of the bulk and interface properties for gate dielectric applications. For example, Stemmer et al. studied the O_2 partial pressure on the thermal stability of ZrO_2 on Si.[156] It was found that the ZrO_2/Si interface thickness and composition were strongly influenced by the pressure. When the annealing temperature was fixed at 900°C, about 1 nm of interface oxide layer was found at $O_2 = 10^{-5}$ Torr, but the interface was degraded to silicide ($ZrSi_2$) at $O_2 = 10^{-7}$ Torr.[156]

Figure 29 shows the C-V curves of the 40 W Zr-doped TaO_x films, i.e., Zr/(Ta+Zr) = 0.33, annealed at 700°C for 10 minutes in O_2. Three different annealing pressures were investigated: (a) 200 Torr, (b) 100 Torr, and (c) 50 Torr. The 200 Torr-O_2 annealing resulted in a well-behaved C-V curve with a negligible hysteresis, indicating a

low density of defects.[7,108] The annealing pressure of 100 Torr, however, showed a larger hysteresis, suggesting a substantial amount of electron traps. A further reduction of the O_2 pressure, i.e., 50 Torr, showed a very large hysteresis and frequency dispersion, indicating a serious increase of defect density close to the interface.[89,157] The corresponding I-V curves of the same samples are shown in Figure 30. Compared to the obvious degradation of C-V behavior, the reduction of the O_2 annealing pressure at 700°C only slightly increased the breakdown voltage.

Figure 31 compares the O_2 annealing pressure effect on (a) the EOT, (b) the current density, and (c) the dielectric breakdown. Increasing the O_2 pressure reduced the EOT, i.e., from 5.84 nm at 50 Torr to 4.35 nm at 200 Torr; however, the current density was degraded from 1.2×10^{-8} A/cm^2 to 4.5×10^{-8} A/cm^2 under gate injection (V_{FB}-1 V)and 1.2×10^{-8} A/cm^2 to 5×10^{-8} A/cm^2 under substrate injection (V_{FB}+1 V). Breakdown characteristics, i.e., V_{BD} and E_{BD}, did not vary too much with the O_2 pressure. Figure 32 shows the O_2 annealing pressure effect on defect densities: (a) V_{FB} and frequency dispersion, (b) hysteresis, and (c) D_{it}. Although the bulk properties of the Zr-doped TaO_x films did not change significantly with the O_2 annealing pressure, as shown in Fig. 31, the defect related properties regarding the interface did show tremendous differences. Fig. 32(a) shows that both the V_{FB} and frequency dispersion were drastically decreased as the O_2 pressure was increased, indicating a better fixed charge and interface qualities. The hysteresis and interface state density were also improved, as shown in Fig. 32(b) and (c), by increasing the O_2 pressure. Conclusively, O_2 = 200 Torr was chosen as the optimized annealing pressure in this study.

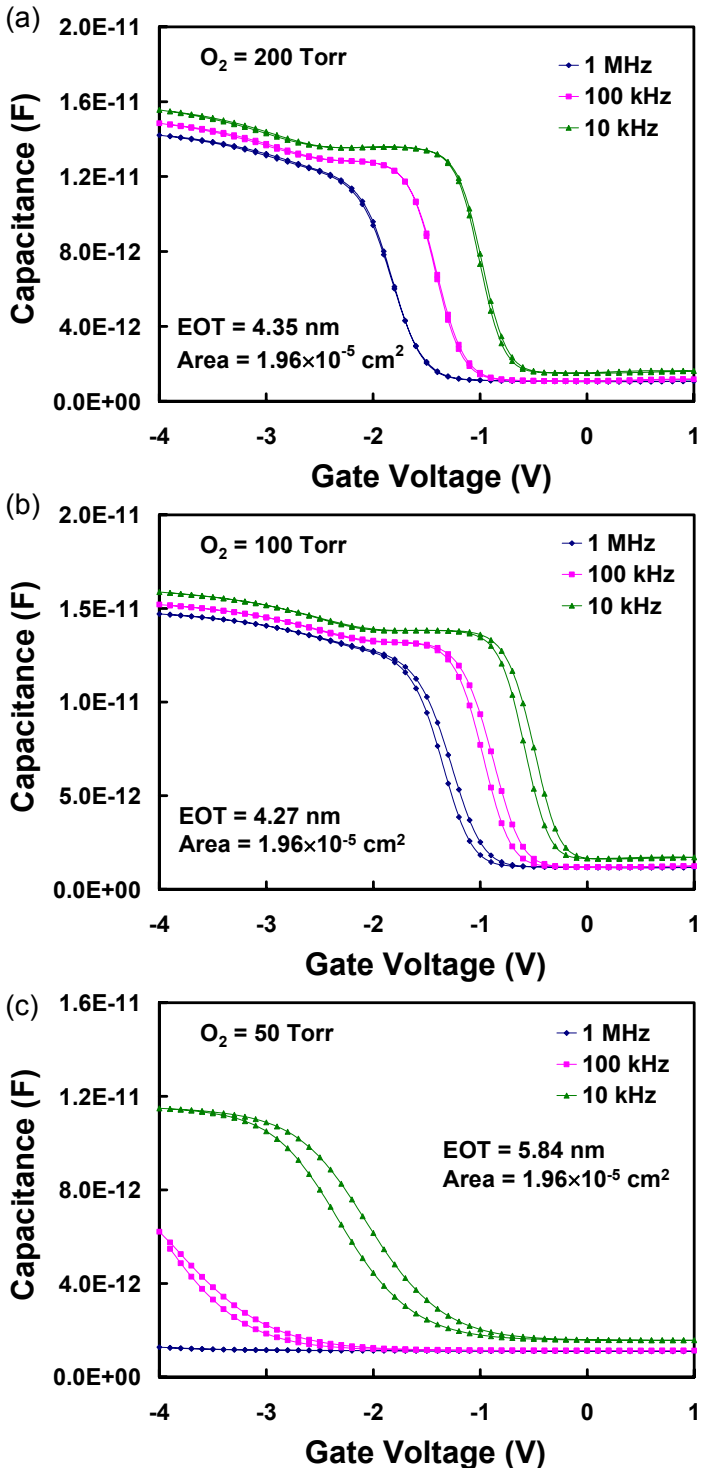

Figure 29. C-V curves of the 40 W Zr-doped TaO_x films with a 700°C-10 minute O_2 annealing at (a) 200 Torr, (b) 100 Torr, and (c) 50 Torr. Mo gates were used.

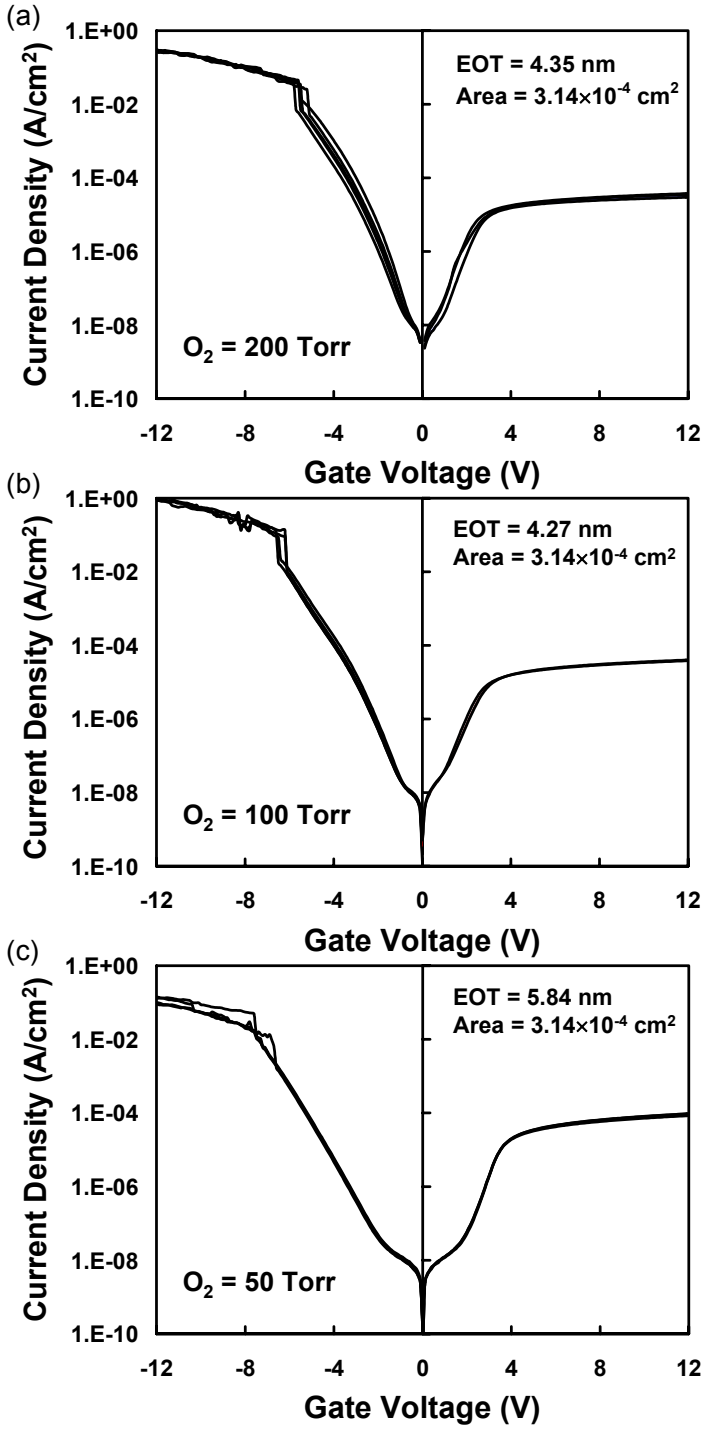

Figure 30. I-V curves of the 40 W Zr-doped TaO_x films with a 700°C-10 minute O_2 annealing at (a) 200 Torr, (b) 100 Torr, and (c) 50 Torr. Mo gates were used.

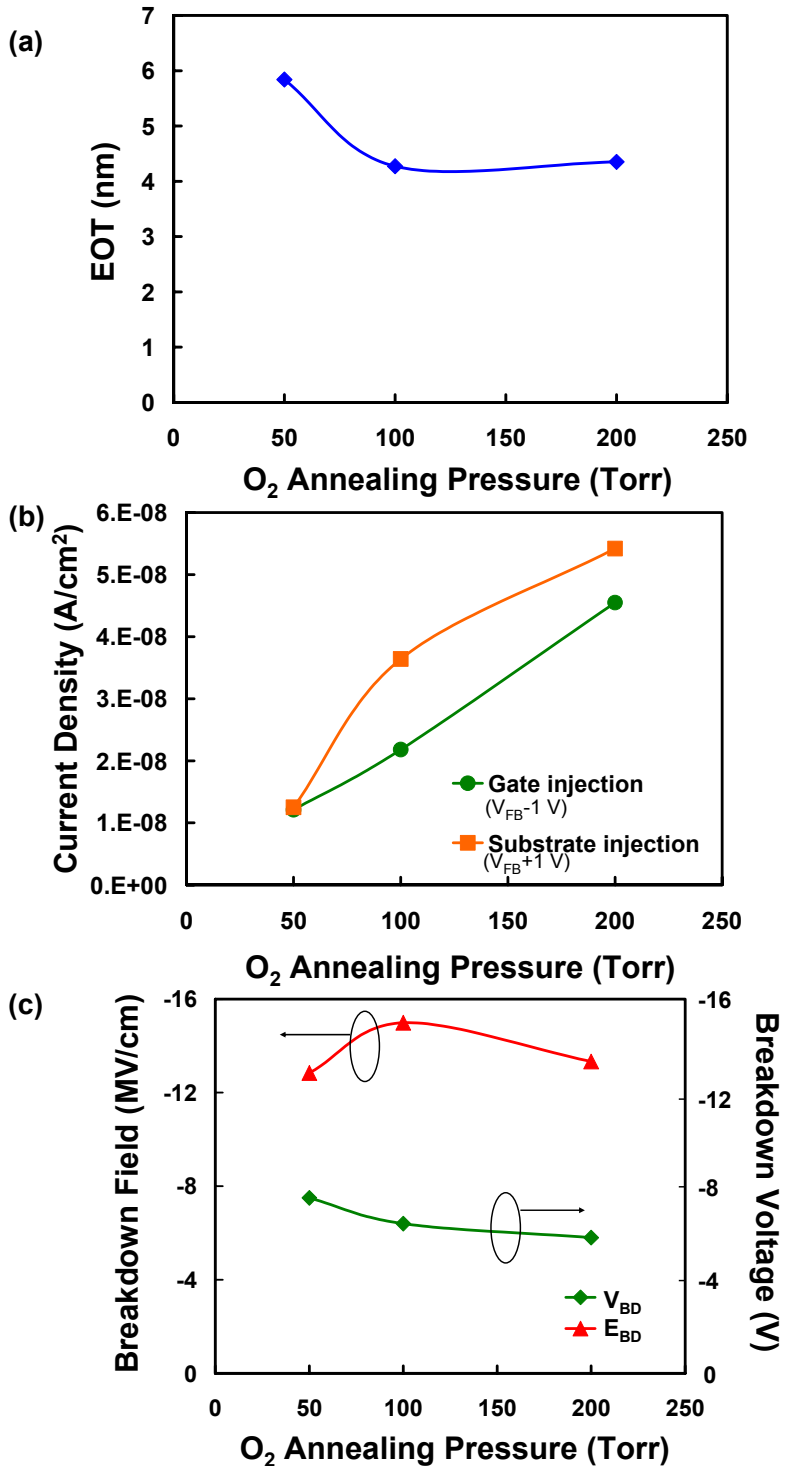

Figure 31. (a) EOT, (b) current density, and (c) breakdown strength, as a function of the O_2 annealing pressure.

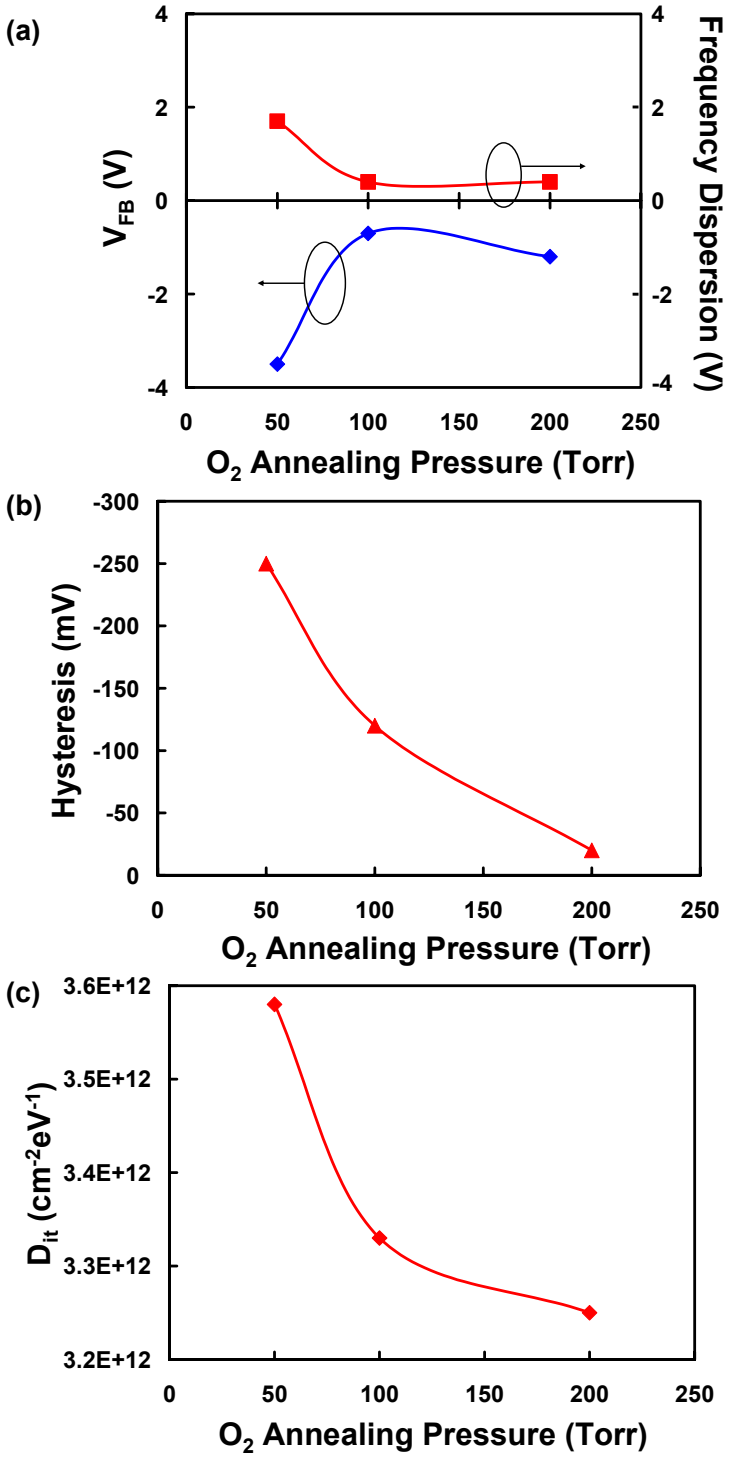

Figure 32. (a) V_{FB} and frequency dispersion, (b) hysteresis, and (c) interface state density, as a function of the O_2 annealing pressure.

2.7 Gate Electrode Area Effects

Different gate areas were used to characterize the MOS capacitor properties. Circular gates with diameters 25 μm to 400 μm were used, which offered gate areas in the range of 10^{-6} to 10^{-3} cm^2. The influence of the gate area on the electrical characterizations has to be identified first to prevent the measurements from extrinsic errors induced by high resistance of the gate and the substrate.[108,158] Figure 33 shows the electrical characterization results as a function of gate area: (a) frequency dispersion of accumulation capacitance, (b) calculated EOT based on the accumulation capacitance at 100 kHz, (c) frequency dispersion in the depletion region defined as the C-V shift at flatband, and (d) C-V hysteresis.

The measured capacitance C_m was strongly influenced by the gate area, which was proportional to the real capacitance C. The relation can be expressed by the following formula,[108,158]

$$C_m = \frac{C}{(1 + r_s G)^2 + (\omega r_s C)^2} \qquad [47]$$

where the real capacitance $C = \varepsilon_0 kA/d$, which is proportional to the gate area A. In Eq. 47, r_s is the device series resistance, which originates from the gate electrode and the Si substrate; G is the dielectric film conductance. Notice that extrinsic factors such as series resistance and gate area have a strong impact on the measurement.[15] The measured capacitance values have to be corrected to extract meaningful physical data.

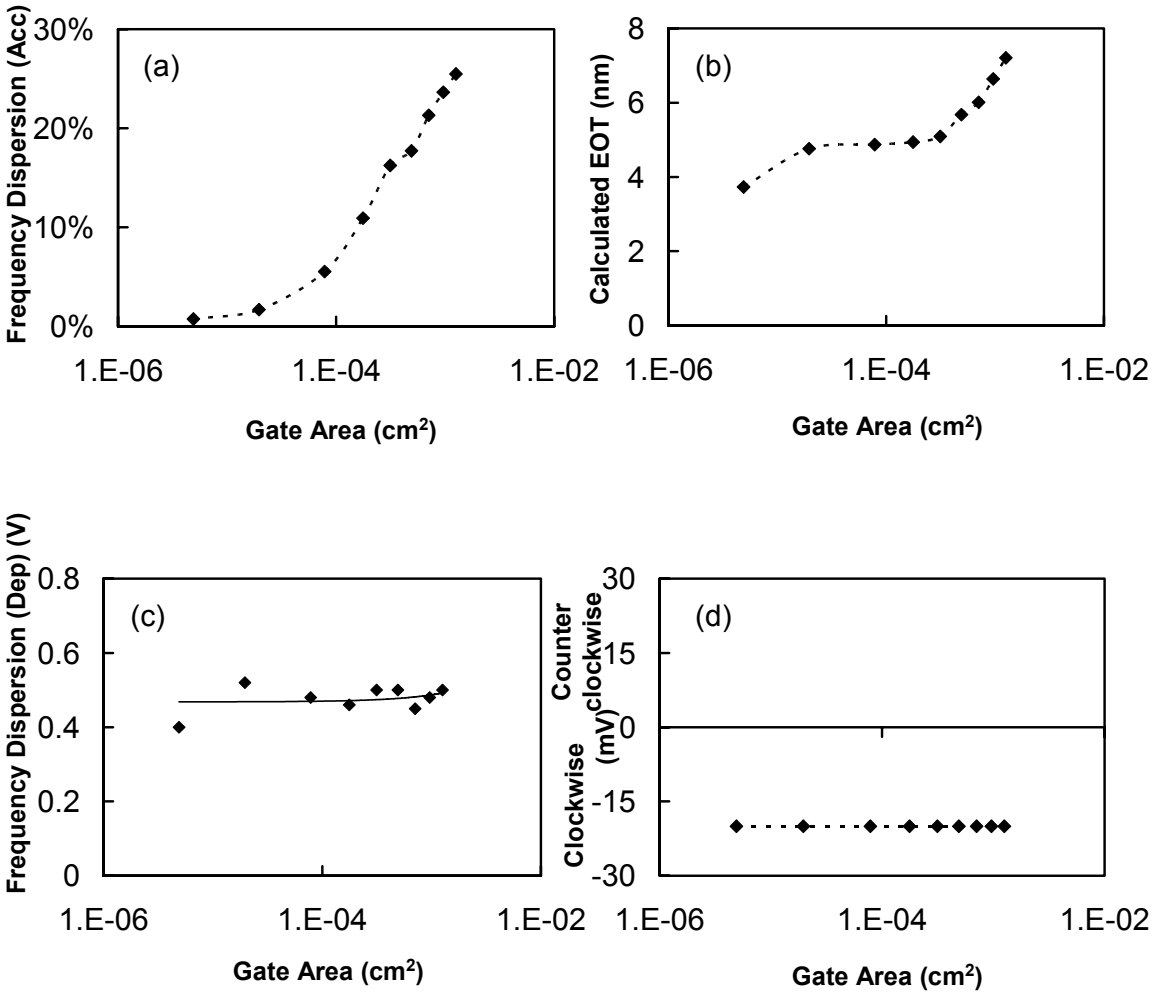

Figure 33. (a) Frequency dispersion of accumulation capacitance, i.e., (C_{100kHz}-C_{1MHz})/C_{100kHz}, (b) calculated EOT from C_{100kHz}, (c) frequency dispersion in depletion, i.e., V_{FB}(100kHz)-V_{FB}(1MHz), and (d) hysteresis, of the 40 W Zr-doped TaO_x film (EOT = 4 nm) as a function of gate area. Mo metal gates were used.

In Eq. 47, the first term in the denominator is composed of the product of r_sG, indicating that the film leakage magnifies the impact of the series resistance. The second term contains the product of the true capacitance C and the angular frequency ω, which also magnifies the influence of r_s. Note that both terms reduce the true capacitance C with the second power in the denominator. To solve the problem, a Si wafer with a low resistivity should be used to minimize this effect. A small gate electrode area with a high conductivity material should be used as well. Performing the C-V measurement at a lower probe frequency helps to obtain the real capacitance; however, the low frequency introduces more noise.[7] Conclusively, the smallest gate area available should be used. Fig. 33(a) and (b) confirmed this conclusion. Except for the measured capacitance, the frequency dispersion in the depletion region and the C-V hysteresis did not show a noticeable change in the gate area, as shown in Fig. 33(c) and (d).

Figure 34 shows the I-V curves with different gate diameters of the same sample, i.e., a 40 W Zr-doped TaO_x film with EOT = 4 nm. Mo metal gate electrodes were used for the MOS capacitor fabrication. Obviously, by increasing the gate diameter, the current density decreased at the same gate voltage and the entire I-V curve shifted downward. To investigate this phenomenon, Figure 35 plots the current densities at $V_{FB}\pm1$ V as a function of (a) gate diameter and (b) gate area, respectively. The reduction of current density with the increase of the gate diameter might be due to the edge effect.[7,121] With a smaller gate perimeter, the electric field at the sharp edge is higher than the center and produces a higher current. Therefore, a larger gate diameter should be used to avoid this extrinsic edge effect. On the other hand, a larger area has a higher

probability to have extrinsic defects, such as pinholes and weak points.[7] These defects can cause the early dielectric breakdown, i.e., the B mode dielectric breakdown.[7,105,108] These two opposite effects associated with the gate area need to be balanced. It has been found in our experiments that the gates with D = 200 μm produced the best I-V curves with reasonable breakdown statistics. The device with D > 200 μm showed more scattered dielectric breakdown voltages.

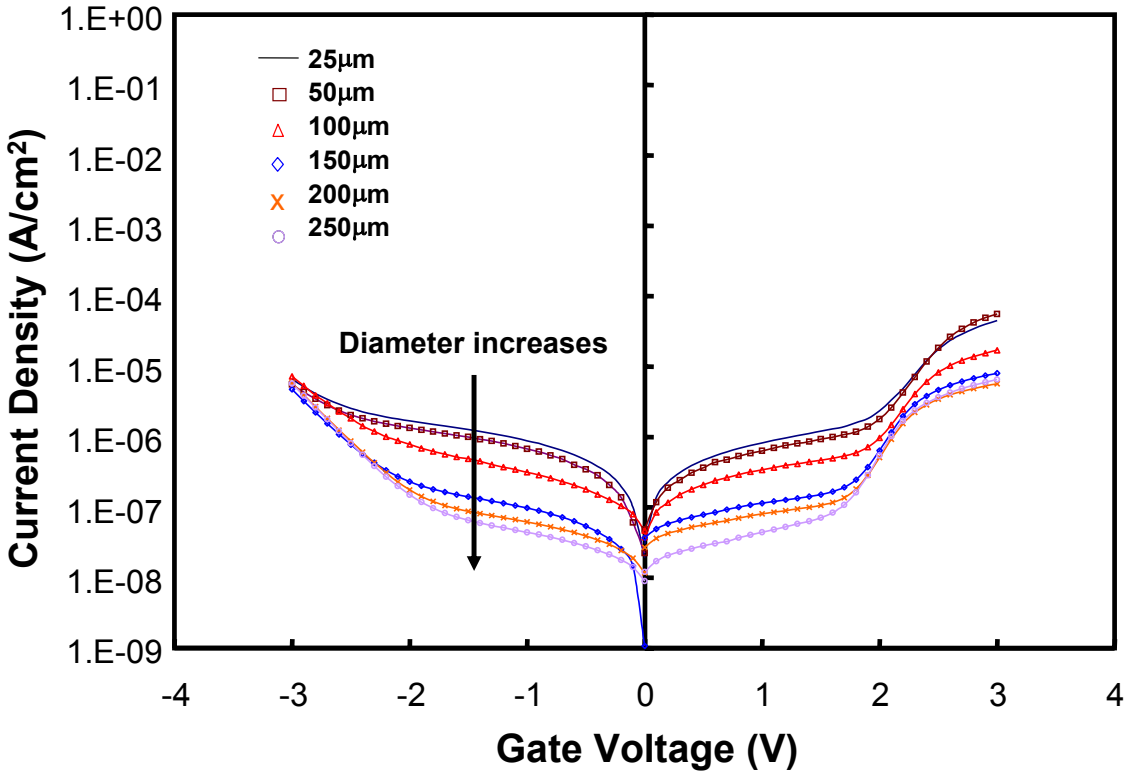

Figure 34. I-V curves of the 40 W Zr-doped TaO_x film (EOT = 4 nm) with different gate diameters.

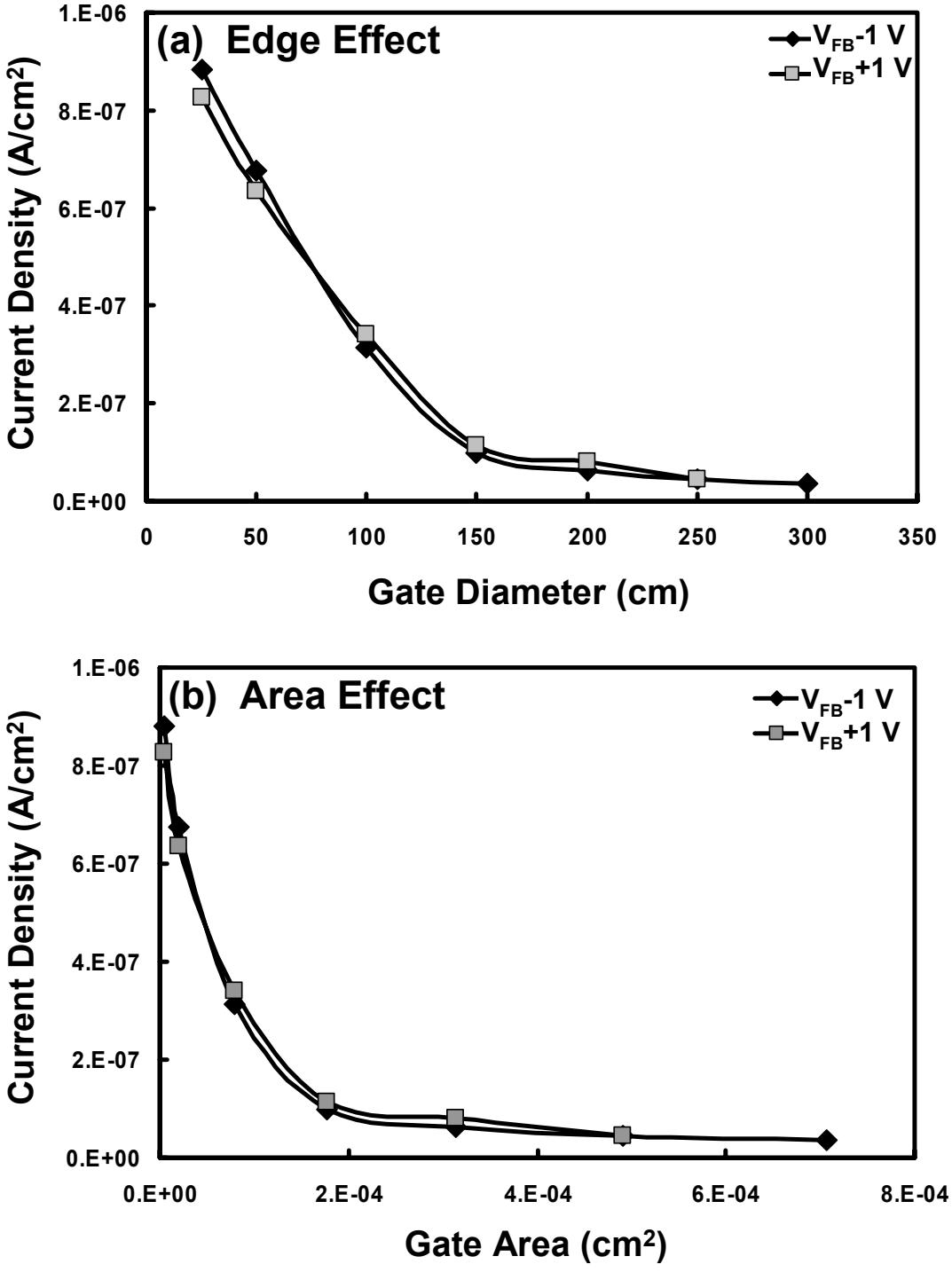

Figure 35. Current densities of the 40 W Zr-doped TaO_x film (EOT = 4 nm) as a function of (a) gate diameter, and (b) gate area. Mo gates were used.

2.8 Summary

In this chapter, a detailed discussion of the experimental methods was presented. The first part gave the introduction about the fabrication process flow of the Zr-doped TaO_x films. The Zr dopant was introduced and controlled by the reactive co-sputtering with two metallic targets, i.e., Ta and Zr. The pre-deposition substrate cleaning and the post-deposition annealing were discussed. Gate metallization was done and finished with a forming gas annealing at 300-400°C.

The second part of this chapter focused on the structural and electrical characterizations. SIMS, ESCA, XRD, and TEM were applied on the Zr-doped TaO_x films for physical and chemical analyses, while C-V and I-V curves were used for device performance investigations. Interface state density extraction techniques, which were useful to study the interface optimization, were presented in detail with the corresponding theories.

The third part talked about the process optimization, including the sputtering gas composition and the O_2 annealing pressure. The optimal experimental conditions were suggested, i.e., the sputtering gas composition of $O_2/(Ar+O_2)$ = 50% and the post annealing pressure of O_2 = 200 Torr.

The last section optimized the gate electrode areas for the C-V and I-V measurements based on the reduction of the extrinsic errors, e.g., series resistance and edge effect. The gates with D = 25 μm were chosen for the C-V measurement and those with D = 200 μm were chosen for the I-V measurement.

CHAPTER III

ZIRCONIUM-DOPED TANTANUM OXIDE GATE DIELECTRICS: PROCESS WITH ALUMINUM GATE ELECTRODE*

3.1 Introduction

This chapter is aimed to provide a comprehensive discussion of the structural and electrical characterizations of Zr-doped TaO_x films. The film thickness in this chapter was between 10 and 100 nm. The details of the fabrication process and characterization techniques were given in the last chapter. Chemical and physical properties, such as chemical bonding, film composition, morphology, and interface layer structure, were systematically analyzed. The effects of the Zr dopant concentration and annealing temperature on various electrical properties, i.e., dielectric constant, current density, conduction mechanism, flatband voltage shift, and hysteresis of C-V curves, were thoroughly investigated. An Al gate electrode was used for the MOS capacitor fabrication. The high film conductivity and well-defined work function (4.1 eV) of the Al gate facilitated the electrical characterizations for the intrinsic properties of the Zr-doped TaO_x film.[3] Conclusions will be drawn at the end of the chapter.

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3.2 Chemical and Physical Properties of Zr-Doped TaO_x

3.2.1 Relationship between Zr Co-Sputtering Power and Zr Dopant Concentration

Figure 36 shows the relationship between the atomic ratio of Zr/(Zr+Ta) in the doped film, which was determined from the ESCA data, and the Zr co-sputtering power. For all films, the Ta co-sputtering power was fixed at 100 W. In the figure, the relationship between the Zr/(Zr+Ta) ratio and the Zr co-sputtering power is slightly non-linear. The Zr co-sputtering powers are between 20 W and 100 W, which correspond to the Zr/(Zr+Ta) ratio in the range of 0.194 to 0.606. When the ratio was above 0.606, a phase separation phenomenon was observed after a 700°C-O_2 annealing, which caused uniformity problems in the film thickness and dielectric property. In addition, the amorphous-to-crystalline transition temperature of the film was lowered, which will be discussed in a following section. Therefore, the film with a high Zr dopant concentration may not be proper for the gate dielectric application. In this chapter, only films with Zr co-sputtering powers between 20 W and 100 W were studied.

It should be noted that the ESCA technique is a surface analysis tool, which can only investigate the composition of the top ~5 nm of the film.[108] Therefore, the variation of the atomic ratio Zr/(Zr+Ta) was expected in this study, as suggested by SIMS. An in situ etching technique that complements ESCA can be used to analyze the film composition along the depth. This will be presented in the next chapter.

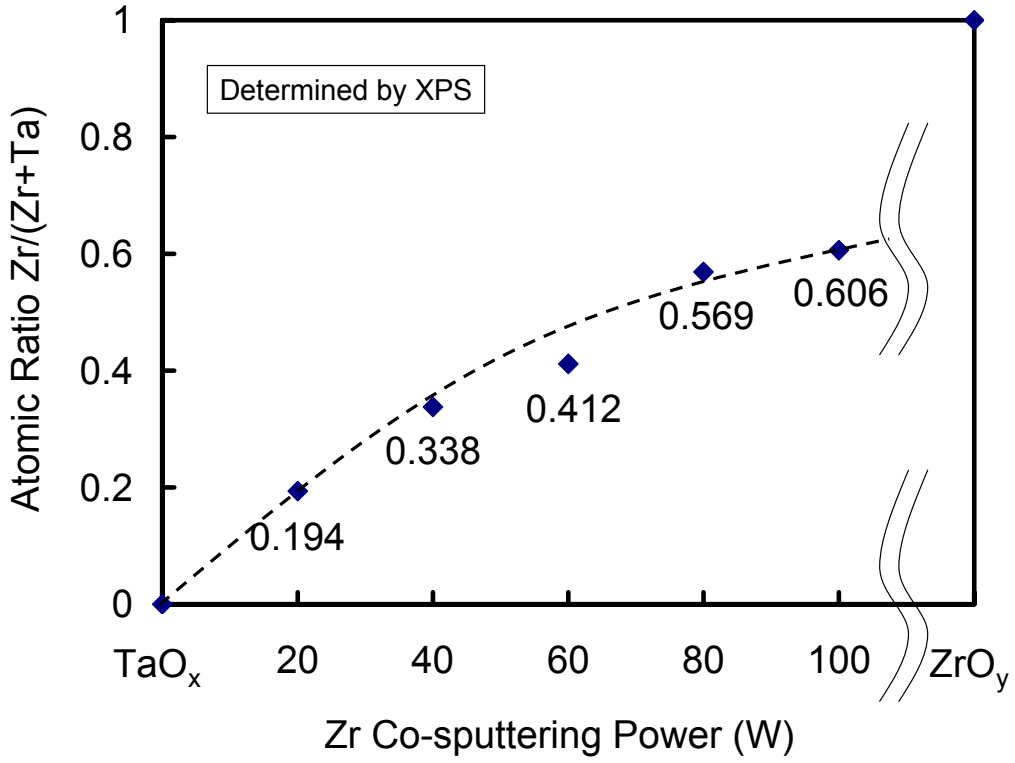


Figure 36. Atomic ratios of Zr/(Zr+Ta) of the Zr-doped TaO_x films as a function of the Zr co-sputtering power.

3.2.2 Chemical Structures of Zr-Doped TaO_x Films

Figure 37 shows the normalized ESCA spectra of 15 nm-thick Zr-doped TaO_x films after being annealed at 700°C under an O_2 atmosphere (200 Torr) for 10 minutes. Core levels of (a) Ta_{4f}, (b) Zr_{3d}, and (c) O_{1s} are shown. The Zr co-sputtering powers of the doped films were 20, 40, 60, and 80 W, which corresponded to the Zr/(Zr+Ta) atomic ratios of 0.194, 0.338, 0.412, and 0.569, respectively. The Ta and Zr atoms in these films were fully oxidized since no metallic states could be deconvoluted in the spectra. For example, Figure 38 shows a typical Ta_{4f} spectrum of a TaO_x sample of which Ta was not fully oxidized. By deconvoluting the Ta_{4f} spectrum, a metallic state, which has a lower binding energy than the oxide state, could be detected.[159,160] In Fig. 37, all three core levels in the Zr-doped TaO_x films, i.e., Ta_{4f}, Zr_{3d}, and O_{1s}, shift to lower binding energy states when the Zr/(Zr+Ta) ratio increases. This shifting was due to the existence of dissimilar metal atoms, i.e., Zr vs. Ta.[161-164] Binding energies in these films were strongly influenced by the charge transfer mechanism that involved all three constituent elements, i.e., Ta, Zr and O.[161] The electronegativities of both Ta (1.50) and O (3.44) were larger than the dopant Zr (1.33). As a result, the charge transfer between Ta and O and that between Zr and O decreased when the Zr dopant concentration was increased. The decrease of the charge transfer reduced the binding energies, which showed up in the ESCA spectra.

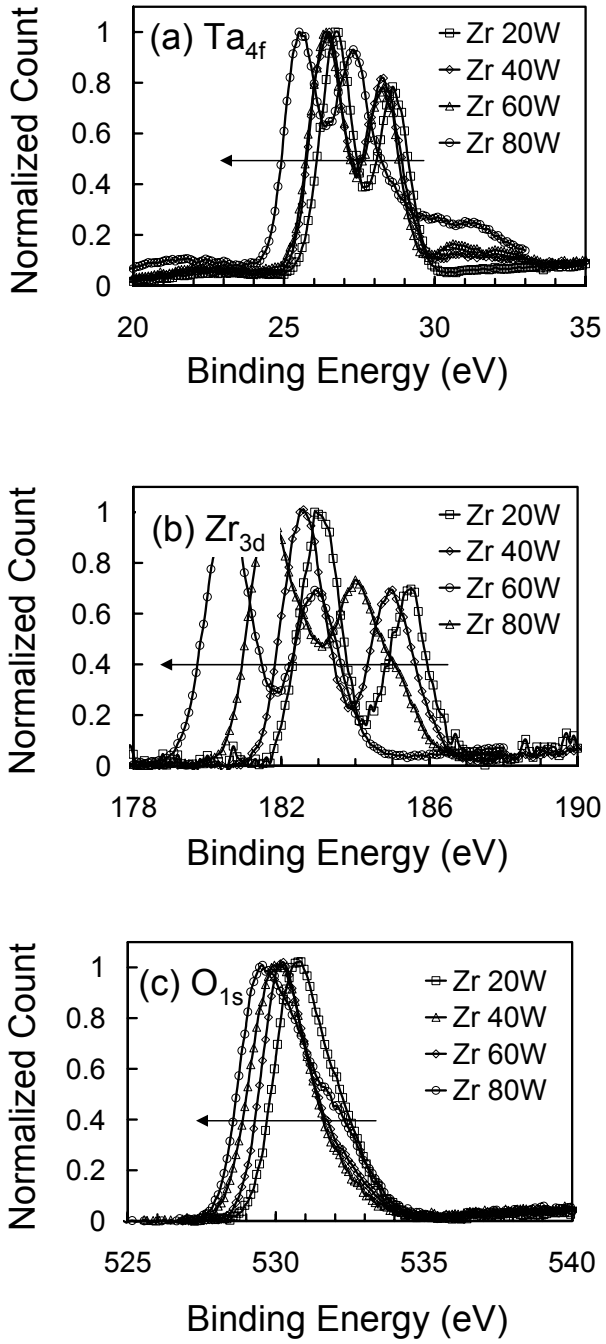


Figure 37. Normalized ESCA spectra of the 15 nm Zr-doped TaO_x films after a 700°C-10 minute O_2 annealing step. Core levels of (a) Ta_{4f}, (b) Zr_{3d}, and (c) O_{1s} are shown. The arrows indicate the direction of increasing the Zr co-sputtering powers.

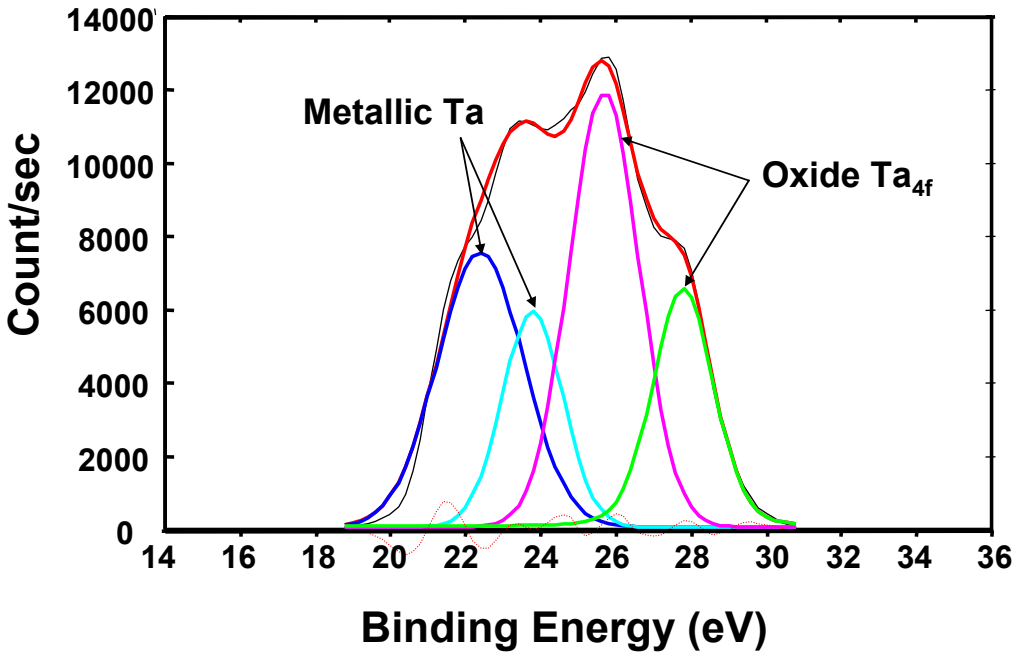


Figure 38. A typical Ta_{4f} ESCA of the Ta_2O_5 sample that was not fully oxidized. The spectrum could be deconvoluted into an oxide state (higher binding energy) and a metallic state (lower binding energy).

3.2.3 Compositional Profiling of Zr-Doped TaO_x Film

Figure 39(a) shows the SIMS compositional profile of an undoped TaO_x film after a 700°C-10 min O_2 annealing. A strong signal of the Si-O ion cluster was detected at the interface, which confirms the formation of the SiO_x interface layer between TaO_x and Si.[22,46,165] This Si-O signal in Fig. 39(a) is about three times stronger than those in Fig. 39(b)-(d), i.e., ~15×10^4 counts vs. ~5×10^4 counts, which are films containing Zr atoms. Therefore, Si atoms prefer to react with the undoped TaO_x film rather than with the Zr-doped TaO_x or the pure ZrO_y film, which is consistent with the thermodynamics prediction.[22] In the insets of Fig. 39(b)-(d), each Si-O signal was deconvoluted into two sub-signals: (i) SiO, which did not contain Zr, and (ii) ZrSiO, which contained Zr. This deconvolution indicated that the Zr-doped TaO_x films formed a silicate interface layer, i.e., Zr_xSi_yO. The area ratios of ZrSiO to SiO are shown in these figures. In Fig. 39(c) and (d), the ratio of (ZrSiO : SiO) with a 60 W Zr co-sputtering power is 0.35 : 1 and that with 100 W is 0.95 : 1, respectively. This suggested that the composition of the interface layer is directly related to that of the bulk film. In Fig. 39(a) for the undoped TaO_x film, the Ta signal decreased from the bulk to the interface with a local maximum peak located before the maximum peak of the (Si-O) signal. This indicates that the reaction between the Si substrate and the TaO_x film excluded the Ta atoms from the interface region. Therefore, the interface layer formed between TaO_x and Si is Ta-deficient. The same phenomenon is also observed in the Zr-doped TaO_x films, as shown in Fig. 39(c) and (d).

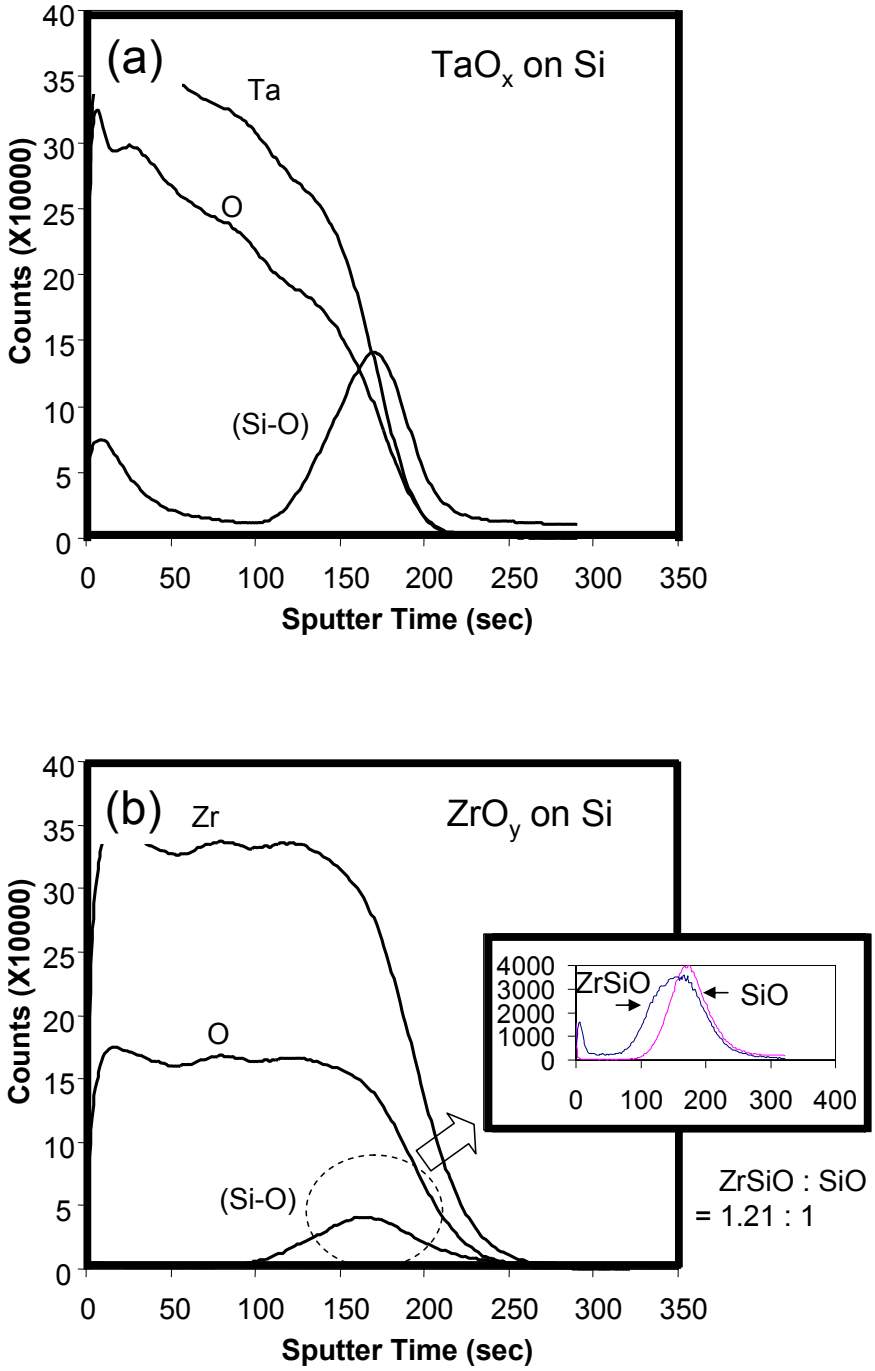


Figure 39. SIMS compositional profiles of (a) the undoped TaO_x, (b) the pure ZrO_y, (c) the 60 W Zr-doped TaO_x, and (d) the 100 W Zr-doped TaO_x. The films were 15 nm thick and annealed at 700°C for 10 minutes in an O_2 ambient.

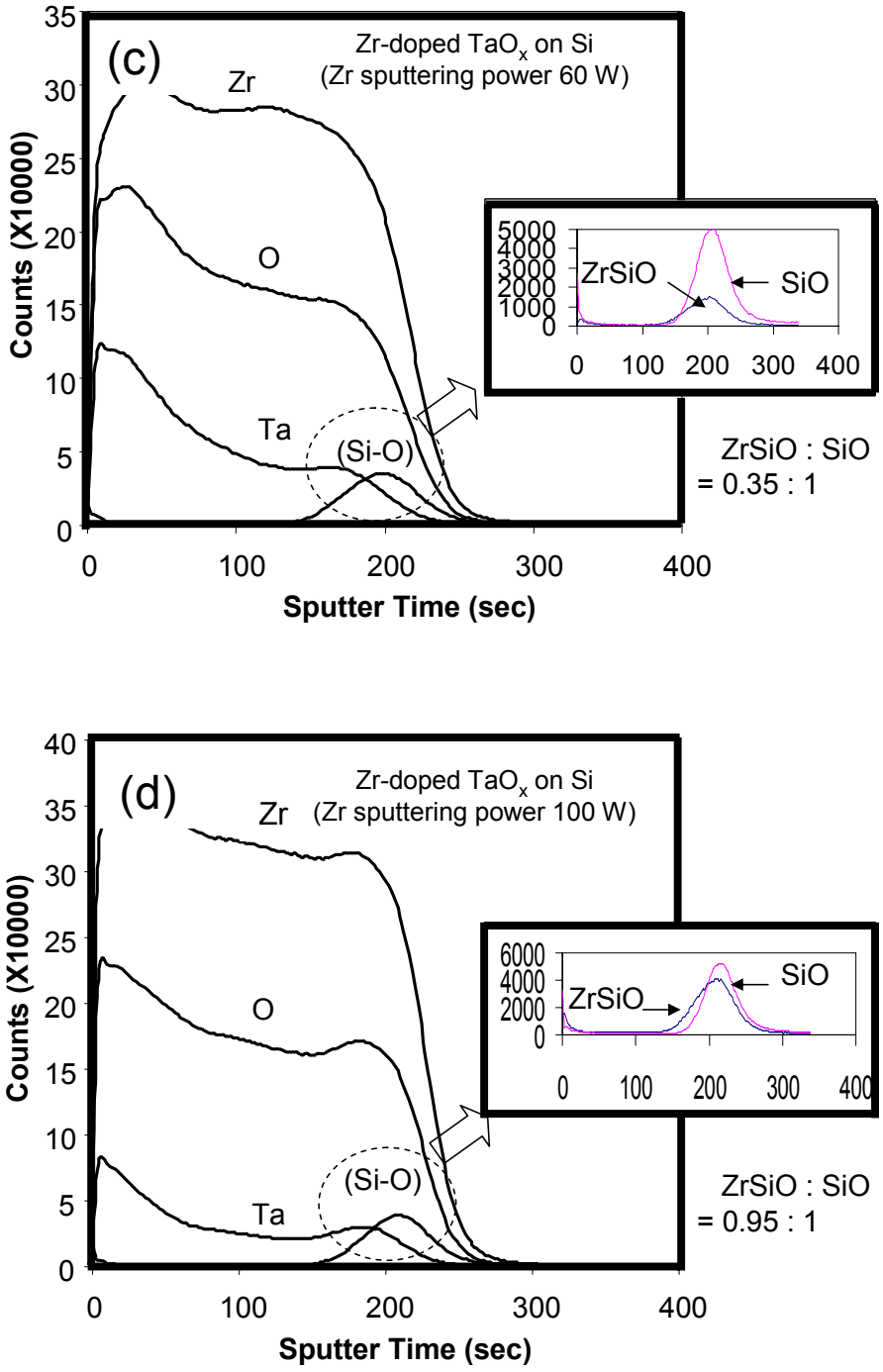


Figure 39. Continued.

Zr atoms pile up at the interface, as shown in Fig. 39(d), which is attributed to the over-saturation of Zr at the interface silicate phase.[41] After a high temperature annealing step, the excessive Zr atoms segregate from the homogeneous silicate phase and form a separate Zr-rich phase.[41] The 100 W Zr co-sputtered film contains a high Zr concentration, i.e., Zr/(Ta+Zr) = 0.606, as shown in Fig. 36. When this sample was annealed at 700°C, the Zr atoms at the interface exceeded the solid solubility limit of silicate and were released to form another Zr-rich phase, which appeared as a pileup peak in the SIMS spectrum. With the 60 W Zr co-sputtering power, on the other hand, the Zr concentration was below the solid solubility limit of the interface silicate. Therefore, no pileup of Zr atoms was observed in Fig. 39(c).

The formation of a Zr_xSi_yO interface layer after a high temperature annealing, i.e., Zr reacted with the interfacial SiO_x, had been confirmed with ESCA by other researchers.[33,152,166] The Zr diffusion constants in SiO_2 were $\sim 1\times10^{-19}$ cm^2/s at 750°C and $\sim 1\times10^{-18}$ cm^2/s at 900°C, respectively, where the diffusion mechanism is the same as that from a constant surface concentration.[166] However, as the temperature was increased to 1000°C, the Zr diffusion mechanism changed to that from a fixed source.[166] This indicated that the Zr incorporation into the interface layer is influenced by the annealing temperature. Comparing the Zr and Ta profiles in Fig. 39, it is obvious that the Zr atoms penetrate deeper into the Si substrate than the Ta atoms. The incorporation of Zr in Si produces multiple energy levels, both acceptor and donor states, within the Si bandgap due to its d-shell electrons.[167] These are electrically active states that seriously reduce the carrier lifetime (τ), which can be expressed as,[167]

$$\tau = \frac{1}{cN_t} = \frac{L^2}{D} \quad [48]$$

where N_t is the defect (impurity) concentration, c is the capture coefficient for the electron or hole, L is the diffusion length, and D is the carrier diffusion coefficient. For electrons, D is 33.5 cm^2/s and for holes, D is 12.4 cm^2/s. The carrier lifetime can be measured to confirm the Zr incorporation in the Si substrate, which was suggested by physical characterization methods such as SIMS, ESCA, and RBS.[36,37,152,167] For example, a low-frequency C-V characteristic starts to show up in the inversion region at a high probe frequency such as 10 kHz, indicating that the carrier lifetime becomes so short that the inversion electrons can be generated fast enough to contribute to the C-V curve.[7] This recovery of inversion capacitance at a high frequency is an evidence of serious impurity incorporation in the Si substrate. In this experiment, some of the Zr-doped TaO_x samples actually showed this phenomenon (data not shown here). Finally, Zr was found to be a faster diffuser than Hf, which was consistent with our results.[37,152]

There was a report that showed a different conclusion on the interface layer formation mechanism and composition.[168] By depositing a layer of oxygen-deficient HfO_x ($x < 2$) on a thermal SiO_2 thin layer, Wang et al. claimed that this nonstoichiometric HfO_x layer actually consumed the SiO_2 film underneath, instead of forming an additional interface, to become fully oxidized at 700°C. Their result was proven by XPS data. They presented a reaction model of:[168]

$$2\ SiO_2 + Hf \rightarrow HfO_2 + 2\ SiO\uparrow\ (\Delta G = -48.0\ kcal/mol) \quad [49]$$

If there was a silicate interface existing, i.e., Hf was incorporated into the interface, the silicate could dissociate to oxidize Hf as well,[168]

$$HfSiO_4 + Hf \rightarrow 2\ HfO_2 + Si \qquad [50]$$

Their TEM images showed that no interface layer was formed between the HfO_2 layer and the Si substrate after the SiO_2 thin layer was completely consumed. Inspired by their conclusion, our system of reactive co-sputtering might also induce an oxygen deficient condition because the Zr dopant grabbed oxygen from the base material, i.e., Ta_2O_5, during the deposition. Another group reported a similar phenomenon by studying the Hf and Zr metal gate electrodes on a SiO_2 MOS capacitor.[169] The thinning of SiO_2 was observed after a 400°C-30 min forming gas annealing, which was attributed to the formation of HfO_2 or ZrO_2 by consuming the SiO_2 layer. This again was due to the large negative enthalpy of oxidation, as suggested by Eq. 49, and the high oxygen solubility.[169] Si atoms released from the dissociated SiO_2 could either form the SiO gas, as proposed by Wang et al.[168], or react with Hf or Zr to form a silicide.[40,169]

From a thermodynamics point of view, as suggested by Fig. 5 and Table II in Chapter I, it is possible that ZrO_2 (or HfO_2) could be in direct contact with the Si substrate without forming a transitional interface layer.[22] However, the interface formation is closely related to the deposition process of the dielectric film. In most cases, a thin SiO_x-like interface formation is unavoidable. It may actually favor the device performance.[4,7,8,10,20,21]

3.2.4 Film Morphology and Interface Layer

The morphology of the high-k gate dielectric films is extremely important for device applications. The film has to remain in an amorphous state for two reasons: (a) a polycrystalline phase is leakier due to grain boundaries, and (b) the grain orientation affects the dielectric properties.[4] There are two common techniques to investigate the film morphology, i.e., X-ray diffraction (XRD), and high-resolution TEM (HRTEM).[108] While the XRD detects the crystal orientation, the HRTEM image can actually see the crystal grains in a crystallized film by means of image contrast.

The HRTEM image not only gives the morphology of the dielectric bulk region, but also offers a powerful tool to investigate the interface layer such as thickness and morphology. For example, Figure 40 shows a TEM image of a 40 W Zr-doped TaO_x film that experienced a post-deposition O_2 annealing at 700°C for 10 minutes. The bulk region film thickness was observed to be ~16 nm, while an extra ~3 nm-thick interface layer was also found between this bulk region and the Si substrate. The interface layer thickness and composition, analyzed with the SIMS compositional profiling in the last section, were strongly dependent on the Zr dopant concentration as well as the fabrication process. For example, the Si surface pretreatment and the post-deposition annealing condition are important factors.[4,8] In this study, the interface layer thicknesses of the Zr-doped TaO_x films on Si were around 2-3 nm from TEM pictures.

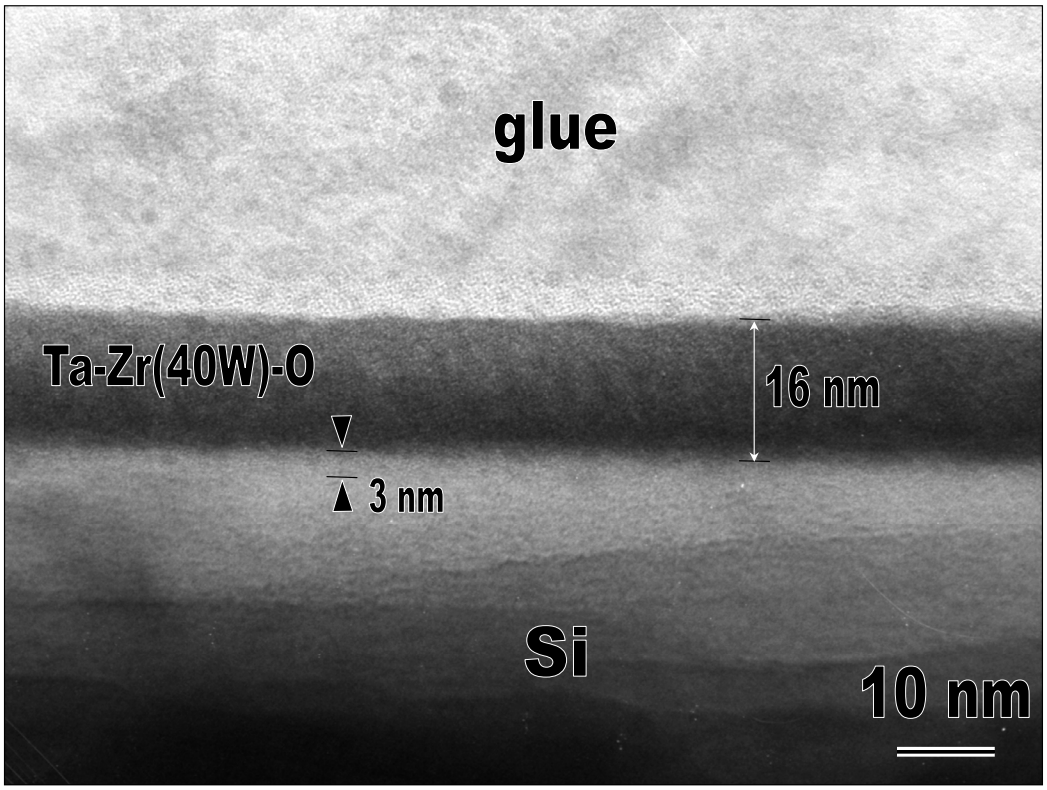


Figure 40. The TEM image of a 40 W Zr-doped TaO_x film on the (100) Si substrate.

3.2.5 Microstructures of Zr-Doped TaO_x Film

Microstructures of undoped Ta_2O_5 and ZrO_2 films

Figure 41 shows the XRD patterns of (a) TaO_x and (b) ZrO_y films with the thicknesses of 10 and 100 nm and the annealing temperatures of 600 and 700°C, respectively. The sharp peak at $2\theta = 33°$ was due to the Si substrate, as confirmed in Figure 42.[118] This occurred because the high-k film was very thin, i.e., 10-100 nm, compared to the Si wafer thickness, i.e., 600-700 μm. The X-ray beam can easily be transmitted through the high-k layer and be diffracted by the single crystal Si underneath. This Si peak could be missing due to a slight misalignment.[117] However, it did not affect the detection of the polycrystalline phase in the high-k film.

The film crystallinity was influenced by the thickness.[51] In Fig. 41(a), the 600°C-annealed TaO_x film was amorphous at both thicknesses. However, the 10 nm TaO_x film was amorphous after a 700°C annealing, while the 100 nm film was crystallized. Two opposite factors affect the thin film crystallization, i.e., surface energy and grain growth.[170] The surface energy constraint dominates over the grain growth when the film is thin and hinders the crystallization. As the film gets thicker, however, the surface energy is loosened and the grain growth begins to accelerate. This film thickness influence on crystallization is consistent with the literature, which reported that a thin Ta_2O_5 film (<20 nm) remained amorphous up to 800°C.[170] Other factors such as annealing gas, impurity, stress, and substrate surface might also contribute to this suppressed crystallinity. For example, the Si diffusion from the substrate into the Ta_2O_5

film is enhanced in the thinner film than in the thicker film, which can increase the amorphous-to-crystalline transition temperature.[171-173]

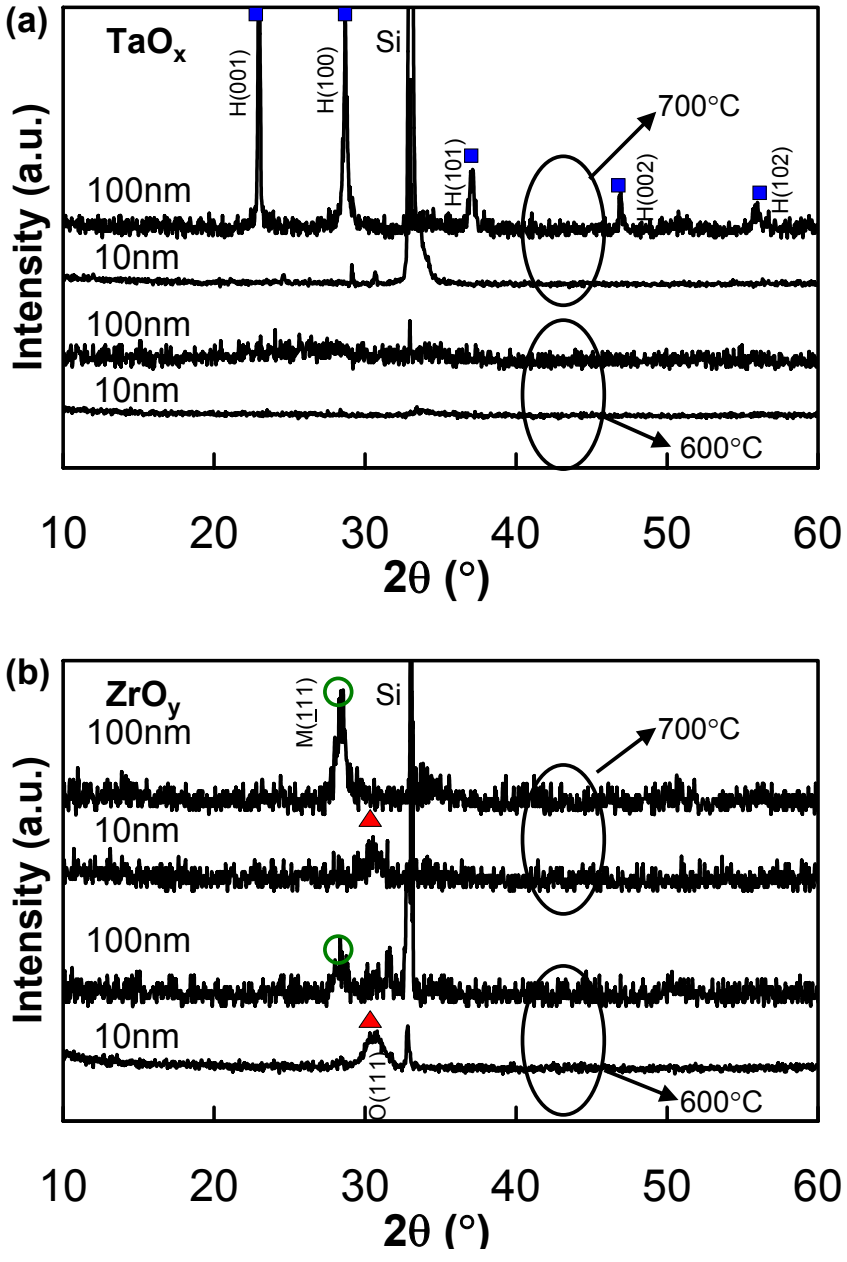


Figure 41. XRD patterns of (a) pure TaO_x and (b) pure ZrO_y films.

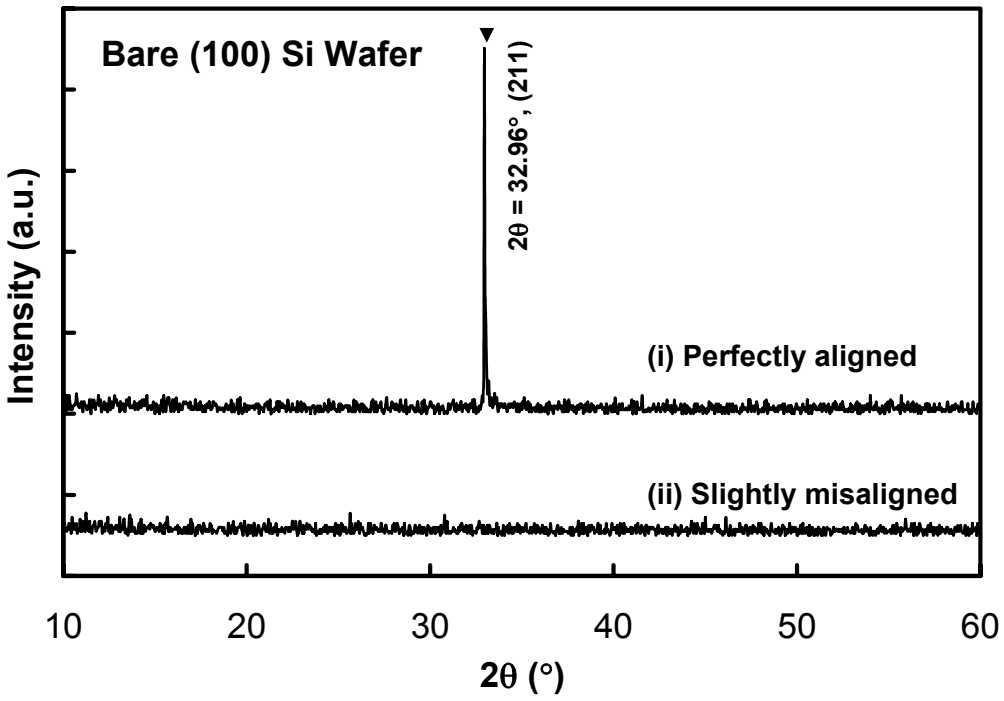


Figure 42. XRD patterns of a bare Si substrate, which was either (i) perfectly aligned or (ii) slightly misaligned.

Most of the literature reported that the pure Ta_2O_5 film crystallized at 650-700°C, regardless of the deposition methods.[47,65] An orthorhombic β-Ta_2O_5 phase was preferentially formed if the film was deposited by LPCVD or sputtering, while a hexagonal δ-Ta_2O_5 phase was observed when the film was deposited by PECVD.[46,91,130,174] The sputter-deposited TaO_x films in this study showed a hexagonal phase instead of an orthorhombic phase, possibly due to the high annealing temperature, e.g., at 700-900°C.[46] Since the XRD patterns of these two crystal structures are very similar, this method alone may not be enough to distinguish them clearly.[45,118]

Both the 10 nm- and 100 nm-thick ZrO_y films were crystallized after a 600°C annealing, as shown in Fig. 41 (b). However, the film crystallinity was strongly dependent on the film thickness, as in the case of the pure TaO_x film. For example, the 10 nm-thick ZrO_y film showed an orthorhombic O(111) peak, while the 100 nm-thick film showed a monoclinic M($\underline{1}$11).[118] This result agreed with the literature that reported that a thick film (~100 nm) of ZrO_2 usually contained a monoclinic phase after a 500°C annealing, with the strongest peaks of M($\underline{1}$11) and M(111).[41] In Fig. 41 (b), a higher annealing temperature, i.e., 700°C vs. 600°C, increased the film's crystallinity, but the crystal structure, as suggested by XRD patterns, remained unchanged. Since the film thickness plays an important role in determining the crystal structure, the XRD results of the Zr-doped TaO_x films will be divided into two categories, i.e., a thicker film (~100 nm) and a thinner film (~10 nm). Detailed discussion will be given in the following sections.

Microstructures of 100 nm Zr-doped TaO_x films

Figure 43(a)-(e) show the XRD patterns of the 100 nm Zr-doped TaO_x films with different Zr dopant concentrations and annealing temperatures. In Fig. 43(a) with the Zr/(Ta+Zr) ratio = 0.19, the doped film remained amorphous up to 800°C. Above 800°C, the film showed a Ta_2O_5 hexagonal (H) phase with (001), (100), (101), (002), and (102) orientations. The strongest peak was H(001). The peak intensity did not show a noticeable increase from 800°C to 900°C, possibly due to the small sample sizes.[117] When the Zr/(Ta+Zr) ratio was increased to 0.33, the film crystallization temperature increased to 900°C with H(100) of Ta_2O_5 as the strongest peak, as shown in Fig. 43(b). When the Zr/(Ta+Zr) ratio was 0.6, the doped film did not show any Ta_2O_5 pattern even after the 900°C annealing. However, a ZrO_2 orthorhombic O(111) orientation showed up at the 800°C annealed film, as shown in Fig 43(e). The peak intensity increased with the increase of the annealing temperature. From Fig. 43, the Zr-doped films showed much higher crystallization temperatures than the undoped TaO_x or ZrO_y films. The Zr dopant concentration affected not only the film crystallization temperature, but also the crystal structure. The film crystallization was suppressed because the added dopant disturbed the molecule alignment of TaO_x at a high temperature.[72] For example, Si, N, and Al are known to show this effect.[41,52,172,173,175] However, if the Zr dopant concentration was too high, a separate ZrO_2 crystal phase was formed, which degraded this effect. Figure 44 summarizes the amorphous-to-crystalline transition temperature as a function of Zr dopant concentration for these 100 nm Zr-doped TaO_x films. As shown in the figure, a moderate Zr concentration maximized the increase of the crystallization temperature.

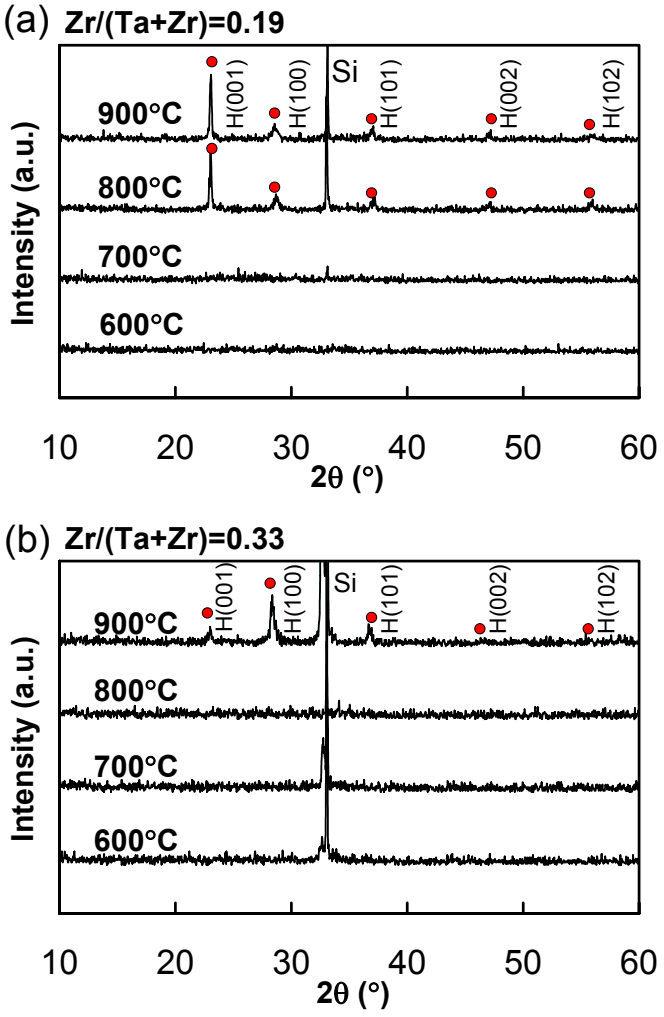


Figure 43. XRD patterns of the 100 nm Zr-doped TaO_x films with various Zr dopant concentrations: (a) Zr/(Ta+Zr) ratio = 0.19, (b) Zr/(Ta+Zr) ratio = 0.33, (c) Zr/(Ta+Zr) ratio = 0.40, (d) Zr/(Ta+Zr) ratio = 0.56, and (e) Zr/(Ta+Zr) ratio = 0.60.

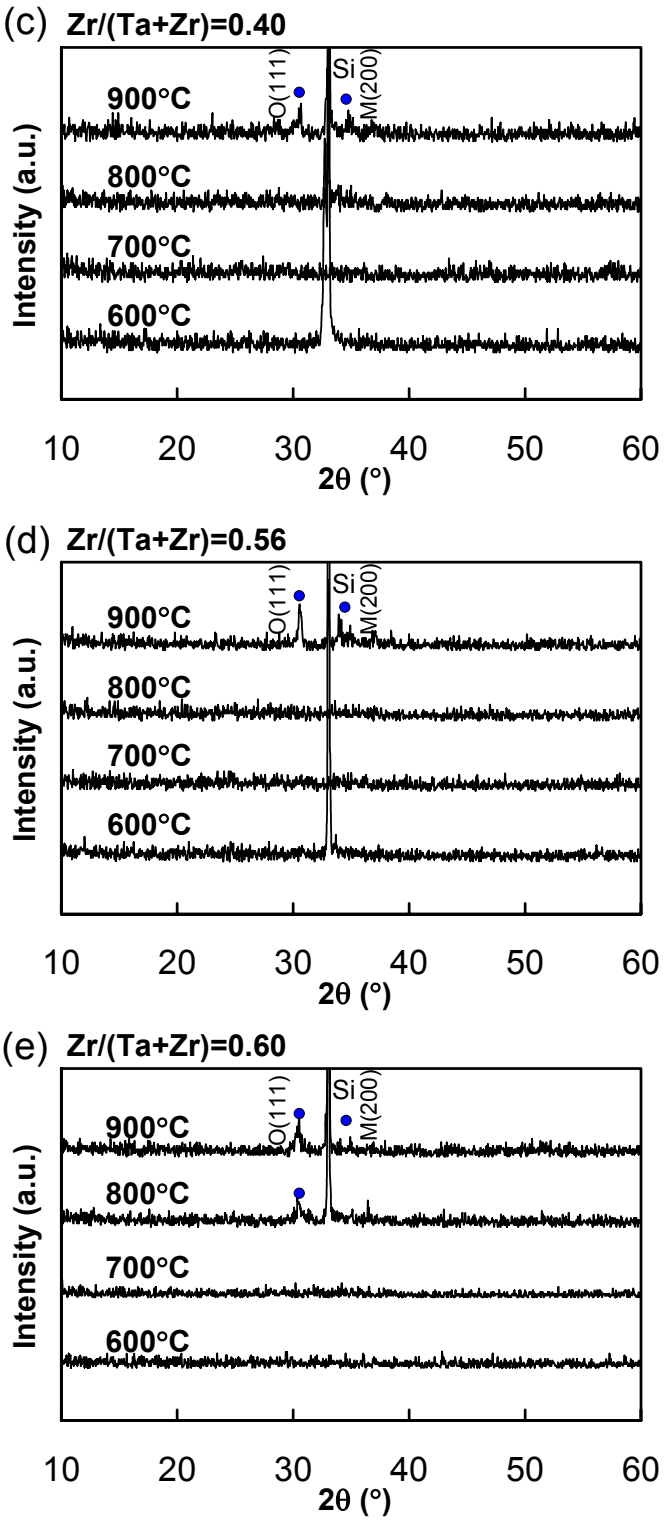


Figure 43. Continued.

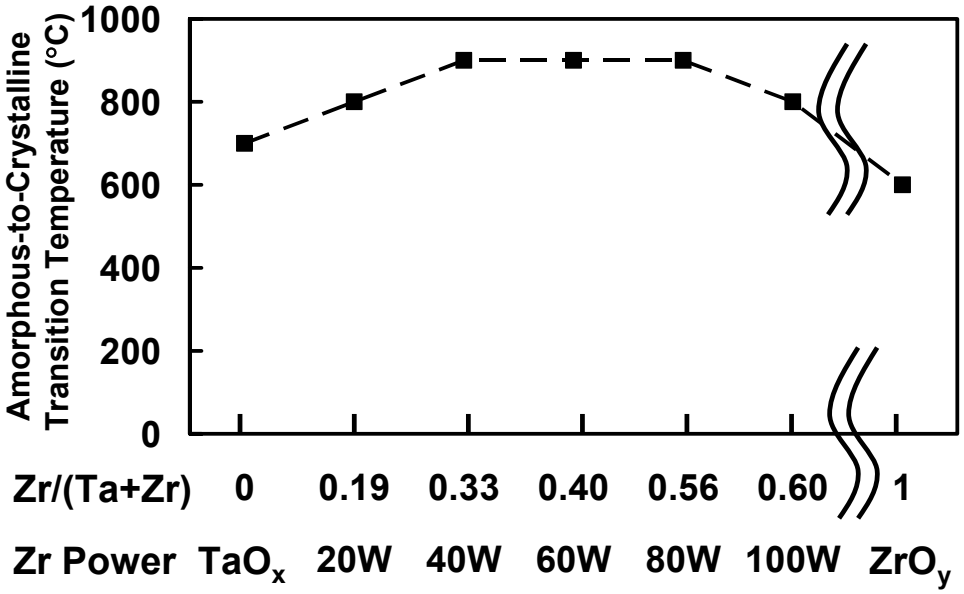


Figure 44. Amorphous-to-crystalline transition temperatures of the 100 nm Zr-doped TaO_x films as a function of the Zr dopant concentration. The Zr co-sputtering powers corresponding to the dopant concentrations are also shown.

Figure 45 compares the XRD patterns of the Zr-doped TaO_x films with different Zr dopant concentrations. All of the films were annealed at 900°C for 10 minutes in an O_2 ambient (200 Torr). The Zr dopant concentration strongly influenced the crystal structures of the doped films. For example, when the Zr/(Ta+Zr) ratio was below 0.33, the films contained the hexagonal Ta_2O_5 phase. Three crystal orientations of the hexagonal phase, i.e., (001), (100) and (101), were observed. The intensity of the strongest peak, i.e., H(001), decreased when the Zr dopant concentration was increased; however, the intensity of H(101) increased. On the other hand, if the Zr/(Ta+Zr) ratio was above 0.40, the Ta_2O_5 crystal phase completely disappeared, while a ZrO_2 orthorhombic O(111) peak showed up. The ZrO_2 phase dominated the crystal structure in the films with high Zr dopant concentrations. The pure ZrO_y film had an monoclinic M ($\underline{1}11$) peak, which was different than the Zr-doped TaO_x film.[41,106,114,118]

The Zr dopant concentration also affected the crystallite (grain) sizes in the doped films. The grain sizes of the 100 nm Zr-doped TaO_x films as a function of Zr dopant concentration are shown in Figure 46. In the figure, all of the films were annealed at 900°C for 10 minutes in O_2. Scherrer's equation was used to estimate the grain sizes (t),[117]

$$t = \frac{0.9\lambda}{B\cos\theta_B} \qquad [51]$$

where λ is the X-ray wavelength (1.5418 Å), B is the full width at half maximum (FWHM) of the XRD peak, and θ_B is the peak location.

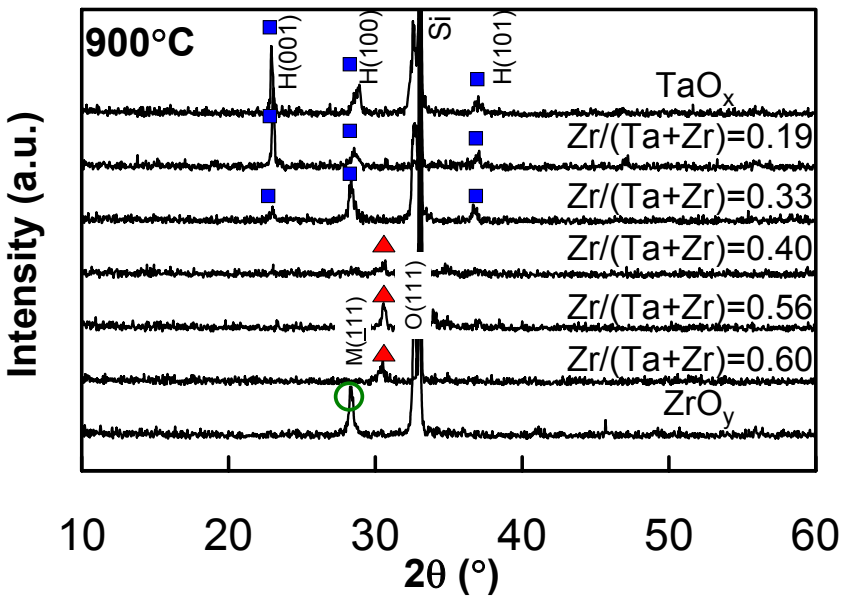


Figure 45. XRD of the 100 nm Zr-doped TaO_x films after annealed at 900°C.

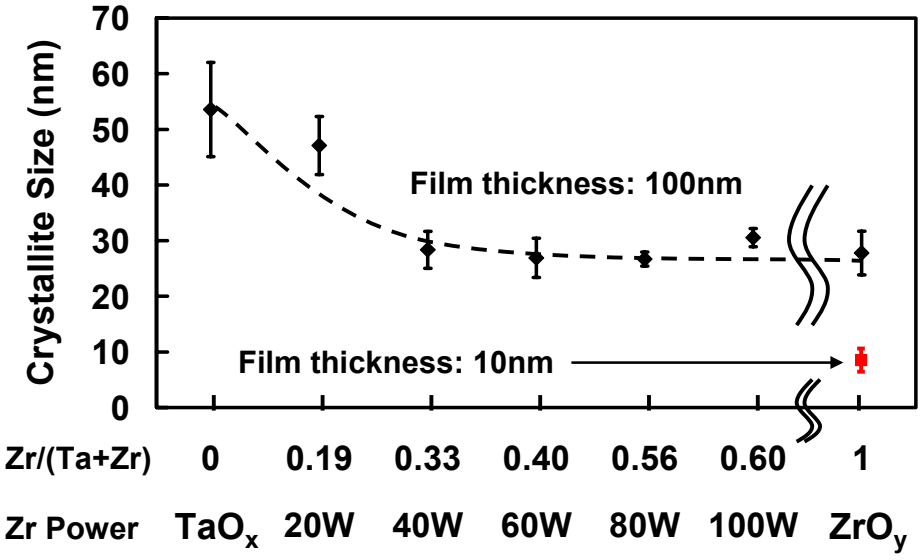


Figure 46. Crystallite sizes of the Zr-doped TaO_x films after annealed at 900°C.

In Fig. 45, the strongest XRD peaks were used to calculate the crystallite sizes shown in Fig. 46. Specifically, H(001) of Ta_2O_5 was used in films with Zr/(Ta+Zr) = 0-0.33, while O(111) of ZrO_2 was used in films with Zr/(Ta+Zr) = 0.40-0.60. The M($\underline{1}$11) was used for the pure ZrO_y film. Obviously, the increase of the Zr dopant concentration reduced the grain sizes, e.g., from 55 nm to 30 nm, indicating the suppression of the film crystallization process. The pure ZrO_y film has large grain sizes, especially when it is very thin such as 10 nm. The grain size reduction and the crystallization temperature increase confirmed the effectiveness of the Zr doping technique. It is well known that grain boundaries inside the crystallized high-k gate dielectrics increase the leakage current.[4,36] By suppressing the film crystallization process, the current leakage is decreased, which makes the film suitable for MOS transistor applications.

Microstructures of 10 nm Zr-doped TaO_x films

Figure 47 shows the XRD patterns of the 10 nm Zr-doped TaO_x films after an 800°C-10 min O_2 annealing step at 200 Torr. As the figure showed, the amorphous-to-crystalline transition temperatures, as well as the crystal structures, were very different from the 100 nm doped films shown in Fig. 43. The Zr-doped TaO_x films with higher dopant concentrations, i.e., Zr/(Ta+Zr) = 0.40-0.60, were crystallized at 800°C showing only the ZrO_2 peaks.[41,118] Both orthorhombic and monoclinic phases of ZrO_2 were observed, including the orientations of M(011), M($\underline{1}$11), and O(111) in Fig. 47. However, no Ta_2O_5 crystal phases were observed. When the O_2 annealing temperature was increased to 900°C, as shown in Figure 48, almost all of the films were crystallized

except for the one with Zr/(Ta+Zr) = 0.33, or the Zr co-sputtering power = 40 W. At 900°C, both Ta_2O_5 and ZrO_2 crystal phases were observed. The crystal structures and orientations were identified and tabulated in the figure.[118] The Ta_2O_5 crystals contained both hexagonal (H) and orthorhombic (O) phases, which were also reported by other groups.[46] Compared with Fig. 45, the strongest peak of H(001) in the 100 nm-thick undoped Ta_2O_5 film was absent from the 900°C-annealed 10 nm-thick Zr-doped TaO_x films. Instead, the strongest Ta_2O_5 peak appeared to be H(100) here. However, this peak could also be ZrO_2 M($\underline{1}$11) since the locations of these two peaks were very close, i.e., 28.3512 vs. 28.2728.[118] For the ZrO_2 crystals, the monoclinic phase was common for a thin film.[41] The observed orthorhombic peak O(111) in the Zr-doped TaO_x films might be due to the strain induced by the Ta atoms, which is rarely reported. For the film with Zr/(Ta+Zr) = 0.33, there was some trace of crystallinity signified by the ZrO_2 M($\underline{1}$11) and Ta_2O_5 H(102) peaks, although it was not yet fully crystallized. In general, the peaks belonging to the ZrO_2 crystals, which were marked by letters, were much stronger than those belonging to the Ta_2O_5 crystals, which were marked by numbers. This observation indicated that the ZrO_2 structure dominated the crystal phase of the film.

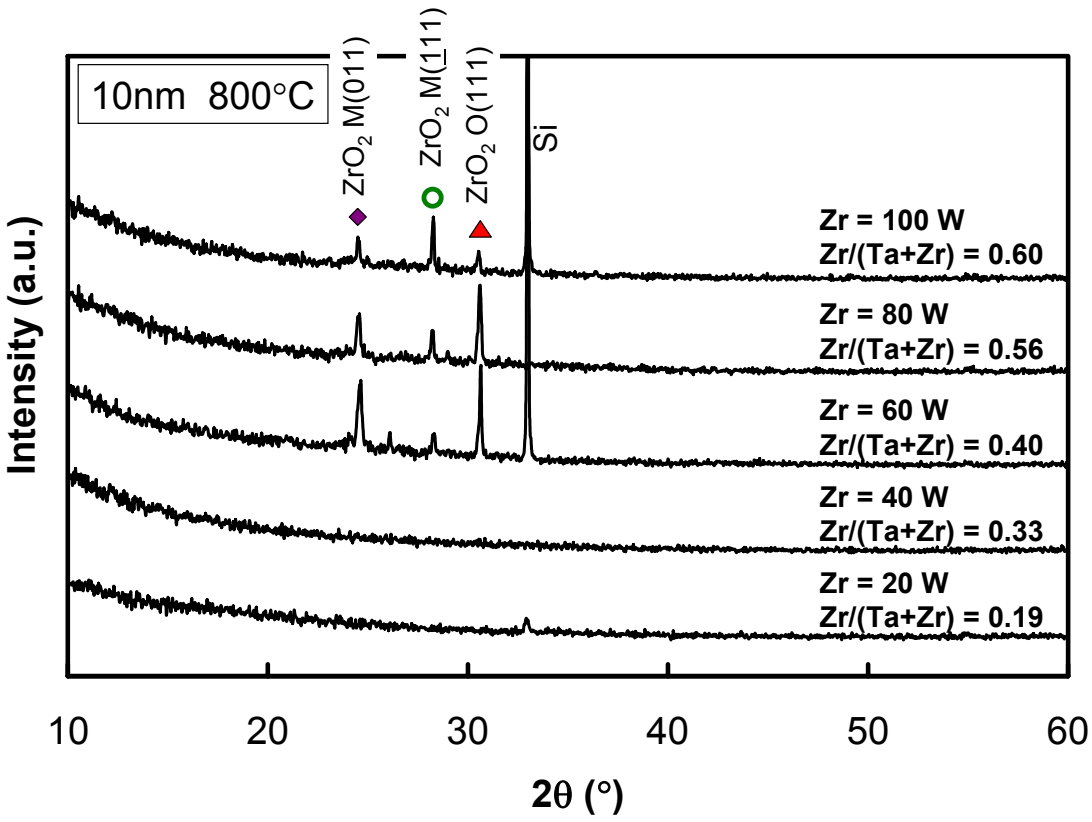
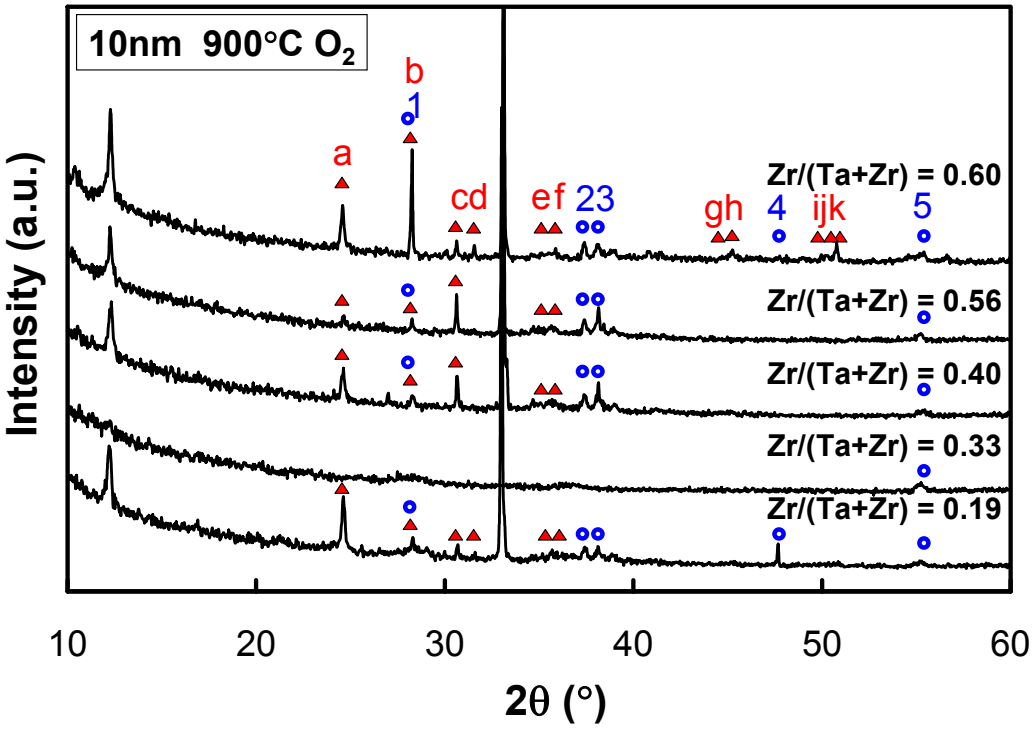


Figure 47. XRD patterns of the 10 nm-thick Zr-doped TaO_x films after an 800°C-10 minute, 200 Torr O_2 annealing step. In the figure, "O" indicates an orthorhombic phase and "M" indicates a monoclinic phase.



Ta_2O_5			ZrO_2		
ID	2θ(◦)	Plane	ID	2θ(◦)	Plane
1	28.3512	H(100)	a	24.5869	M(011)
2	37.4092	H(101)	b	28.2728	M(111)
3	38.2326	O(211)	c	30.6255	O(111)
4	47.6827	H(002)	d	31.6058	M(111)
5	55.4075	H(102)	e	34.1234	M(200)
			f	35.8977	M(020)
			g	44.7000	M(211)
			h	45.2908	M(202)
			i	49.3002	M(220)
			j	50.1988	M(022)
			k	50.5011	M(221)

Figure 48. XRD patterns of the 10 nm Zr-doped TaO_x films with several Zr dopant concentrations. The crystal orientations are tabulated.

Figure 49 summarizes the amorphous-to-crystalline transition temperatures for both 10 nm and 100 nm Zr-doped TaO_x films, as a function of the Zr dopant concentration. In the figure, the trends of the amorphous-to-crystallization transition temperatures were different between the 10 nm and 100 nm films. For example, the 10 nm films with the Zr co-sputtering powers of 20 and 40 W showed higher crystallization temperatures than their 100 nm counterparts, which is expected from the surface energy domination point-of-view.[170] However, the 10 nm films with the Zr powers of 60 W and 80 W had lower crystallization temperatures than the 100 nm films. This unusual trend occurred at the higher Zr dopant concentrations, i.e., the films crystallized at a lower temperature when they became thinner, possibly because they transformed into a different crystal structure than the thicker films. The thin films have a lower amorphous-to-polycrystalline transition temperature than the thick films. This phenomenon is supported by Fig. 41(b), in which the pure ZrO_2 films showed different crystal structures at different thicknesses. Therefore, the crystal structures of the 10 nm Zr-doped TaO_x films that had lower crystallization temperatures than their 100 nm counterparts were dominated by ZrO_2. On the other hand, the crystal structures of the 10 nm-thick films that had higher crystallization temperatures than the 100 nm films were dominated by the Ta_2O_5 crystal, which did not change crystal structures as shown in Fig. 41(a). From Fig. 45 and Fig. 48, it can be concluded that Zr-doped TaO_x films have different XRD patterns at different thicknesses.

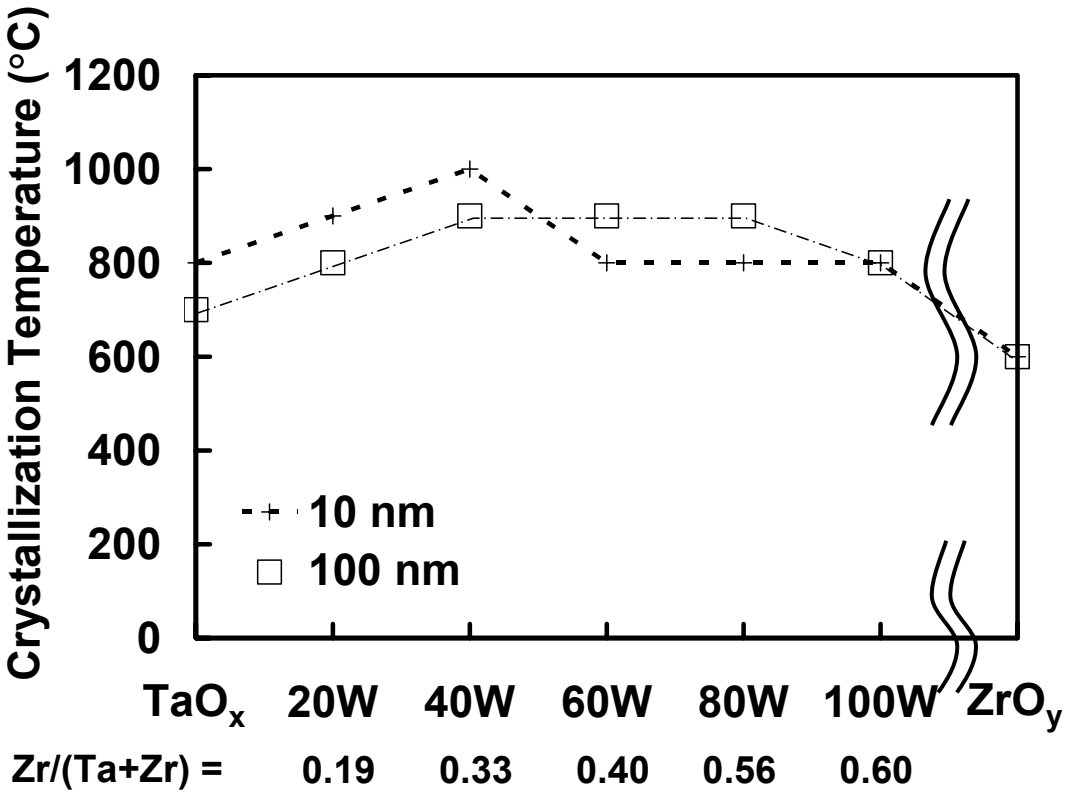


Figure 49. Crystallization temperatures of the 10 nm- and 100 nm-thick Zr-doped TaO_x films as a function of the Zr dopant concentration.

Figure 50 shows the XRD patterns of 10 nm Zr-doped TaO_x films that were annealed in vacuum (1×10^{-2} Torr) at 900°C for 10 minutes. Compared to films annealed in the oxygen ambient (200 Torr) at the same temperature, as shown in Fig. 48, the XRD patterns were totally different. The most obvious change is that there was no ZrO_2 phases observed in the diffraction patterns. For example, strong peaks such as M(011), M($\underline{1}$11), and O(111) in Fig. 48 disappeared in these vacuum-annealed films. On the other hand, Ta_2O_5 crystals, such as hexagonal H(011), H(100), and H(101), were detected again just like the 100 nm samples. It was suspected that the Zr atoms in the Zr-doped TaO_x films had reacted with the Si substrate to form $ZrSi_2$, which consumed the ZrO_2 phase.[86,176,177] ZrO_2 was known to form a silicide phase above 900°C in the vacuum.[50,156] The $ZrSi_2$ grain size might be too small for the XRD to detect.[178] The $ZrSi_2$ formation will seriously degrade the application of the high-k gate dielectrics since it is a conductor instead of an insulator.[179] Therefore, in order to avoid the film silicidation, the Zr-doped TaO_x films should not be annealed in the vacuum above 900°C. A noble gas, such as helium (He), can be used to anneal the ZrO_2 films without degrading into $ZrSi_2$.[180] Helium can easily diffuse through the ZrO_2 film and reach the SiO_x interface due to its small size. The high vibrational energy of Zr-O or Si-O bonds at high annealing temperature can be transformed into the kinetic energy of He atoms, i.e., quenching, which diffuse out of the film afterwards. Thus, the bonds of Zr-O and Si-O remain intact without forming the $ZrSi_2$ layer. Other noble gases, such as Ne and Ar, can also be used for quenching. However, the result is not as effective as He due to their larger atomic sizes.[178]

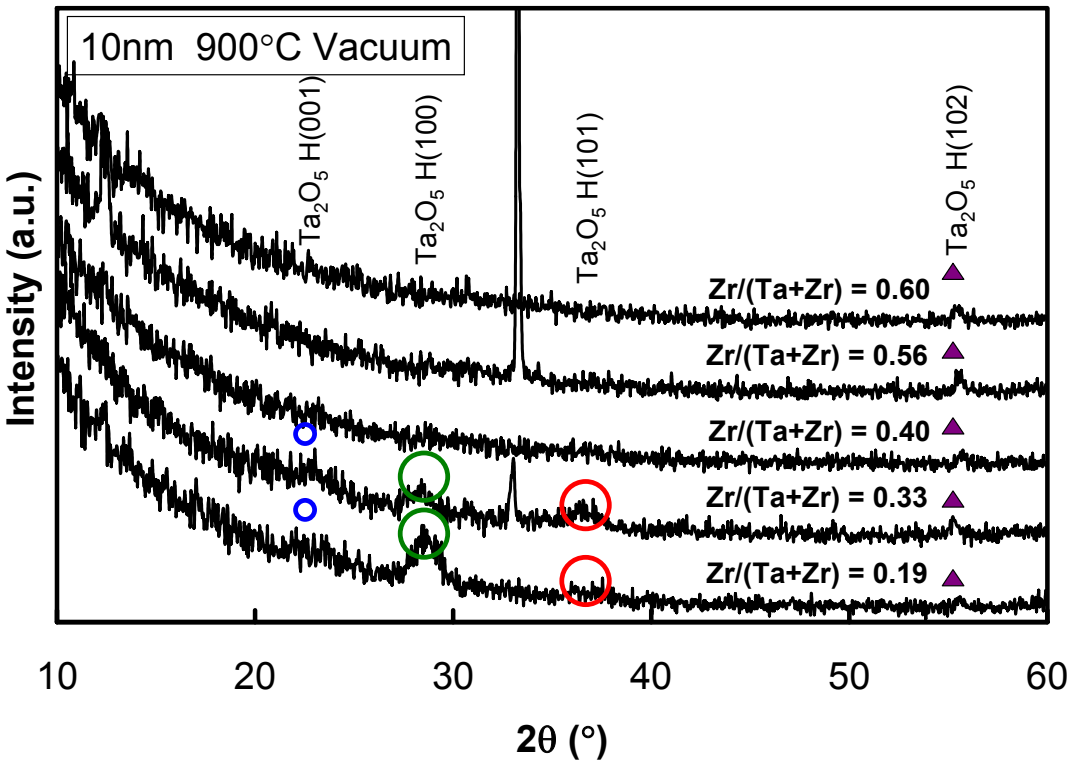


Figure 50. XRD patterns of the 10 nm Zr-doped TaO_x films after a 900°C-10 minute annealing in the vacuum.

3.3 Electrical Properties of Zr-Doped TaO_x

3.3.1 Influence of Zr Dopant on Current Density

Figure 51 shows the I-V curves of the 15 nm Zr-doped TaO_x films with two different annealing conditions: (a) at 600°C for 60 minutes and (b) at 700°C for 10 minutes. This post-deposition annealing was performed in an O_2 ambient at 200 Torr. To compare the Zr doping effect on the doped films, the I-V curves of the undoped TaO_x and ZrO_y films are also shown. The Zr co-sputtering power, which can be easily converted to the Zr dopant concentration shown in Fig. 36, is used in the figure as a reference for each I-V curve.

First, all the I-V curves under positive biases were saturated at high electric fields. This saturation was attributed to the insufficient minority carriers, i.e., electrons in our p-type Si wafer, which were generated in the depletion region (space charge region) of the Si substrate.[181-183] The leakage current through the gate dielectric layer resulted in a loss of electrons from the Si inversion layer. As the electric field increased, the leakage current became larger. If the electron generation rate in the depletion region could not make up for the electron loss, the leakage current became saturated.

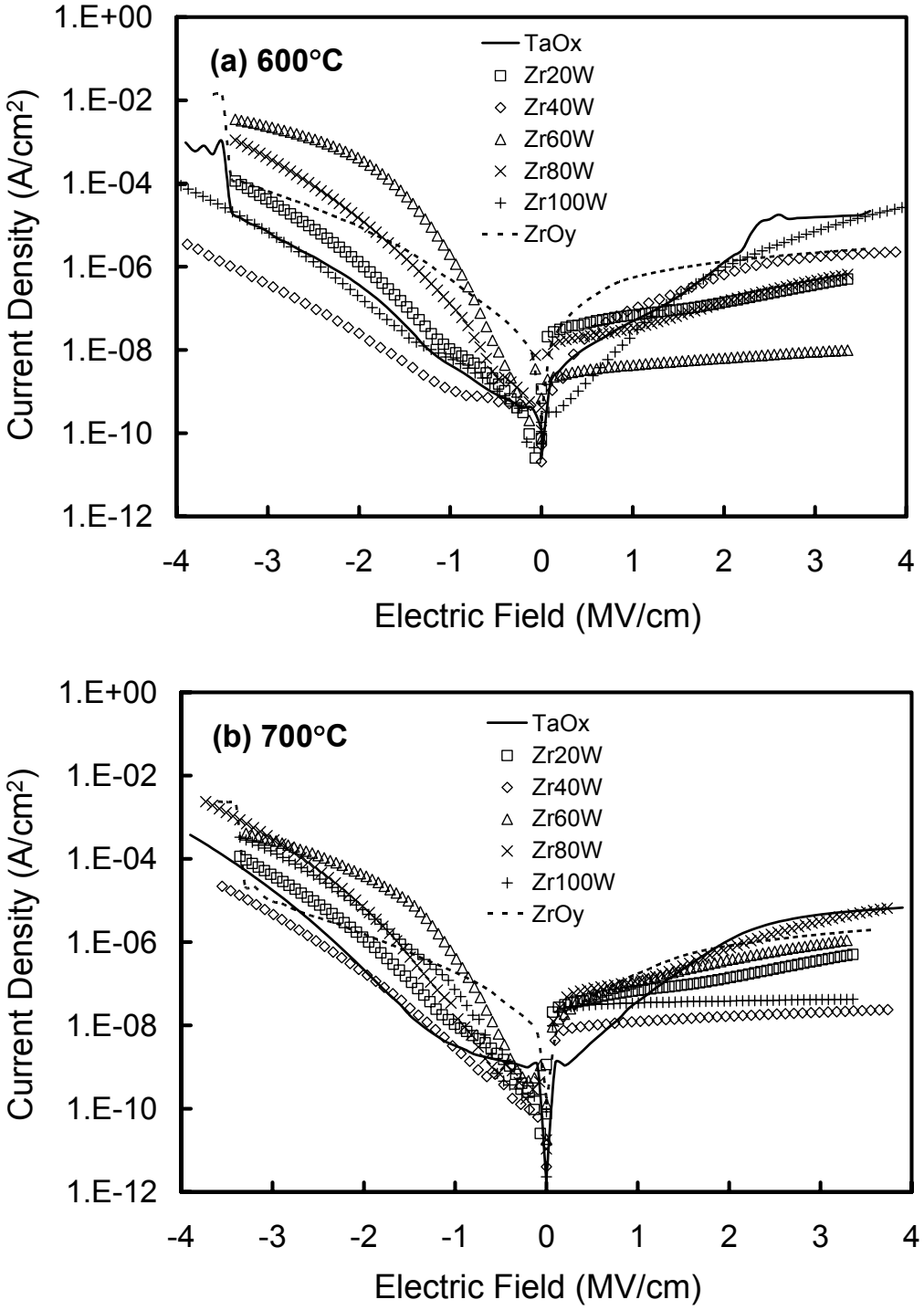


Figure 51. I-V curves of the Zr-doped TaO_x films with an O_2 annealing at (a) 600°C for 60 minutes, and (b) 700°C for 10 minutes.

The generation rate of the minority carrier (G_m) can be expressed by the following equation:[184]

$$G_m = \frac{n_i}{\tau_n + \tau_p} \quad [52]$$

where n_i is the intrinsic carrier density of Si (~10^{10} cm^{-3} at room temperature), while τ_n and τ_p are the electron and hole lifetimes, respectively. From Eq. 52, increasing n_i and/or decreasing τ_n and τ_p increases G_m and the saturation current under inversion. The intrinsic carrier density n_i can be effectively increased by raising the testing temperature or by performing the test under a light source, both of which enhance the thermal electron-hole generation rate.[3,121] The electron and hole lifetimes, τ_n and τ_p, are related to the trap density and the capture cross section in the depletion region, which are affected by the deposition condition of the gate dielectrics.[33,152,167] Eq. 48 in a previous section can be used to estimate their values.[167] These electrically active defects include oxygen precipitates and metallic contaminants.[167] The interface reaction between the high-k layer and the Si substrate creates structural defects, e.g., dangling bonds, which aggravate the impurity diffusion.[21] For example, Zr atoms have been reported to aggressively diffuse into the Si channel region.[33,152,167] These structural defects and metal contaminants function as the generation and recombination centers for electrons and holes, reducing their lifetimes.[3]

Fig. 51 shows that the I-V curves of the undoped TaO_x films were different from those of the Zr-doped TaO_x films in the inversion regions. For example, the current density of the 600°C-annealed TaO_x film increased gradually with the increase of the

electric field until the breakdown occurred at ~2 MV/cm. After the breakdown, the current density was saturated at ~10^{-5} A/cm^2. In the accumulation region, however, the breakdown of TaO_x occurred at -3.3 MV/cm. This dielectric breakdown range, i.e., 2-3 MV/cm, agrees with the literature where the films were deposited by reactive sputtering or LPCVD.[45] On the other hand, the 700°C-annealed TaO_x film did not show a breakdown under either inversion or accumulation, which indicated that the defects responsible for the early breakdown were effectively removed.[46] In Fig. 51, however, the current densities of all the Zr-doped TaO_x films, including the pure ZrO_y films, increased more rapidly than the undoped TaO_x films, especially at low positive electric fields. For example, when the electric field was below 0.3 MV/cm, the current densities of the Zr-doped films were about one order of magnitude higher than the undoped TaO_x film. On the other hand, the current densities of the Zr-doped films were saturated much quicker at higher electric fields. This difference in the I-V behavior between the doped and undoped TaO_x films under positive biases was mainly due to the interface difference between the high-k layer and the Si substrate.[30,70,153] The positive gate bias in our case corresponds to the substrate injection. The interface layer between the bulk TaO_x layer and the Si substrate was basically silicon suboxide (SiO_x), while that for the bulk ZrO_y layer was zirconium silicate (Zr_xSi_yO). This was described in a previous section about the compositional profiling. Energy band diagrams for both Ta_2O_5 and ZrO_2 as the high-k gate dielectrics are shown in Figure 52(a) and (b). Al gate electrodes are used here. Numerical values in these two energy diagrams are cited from Table III.[4,20,54]

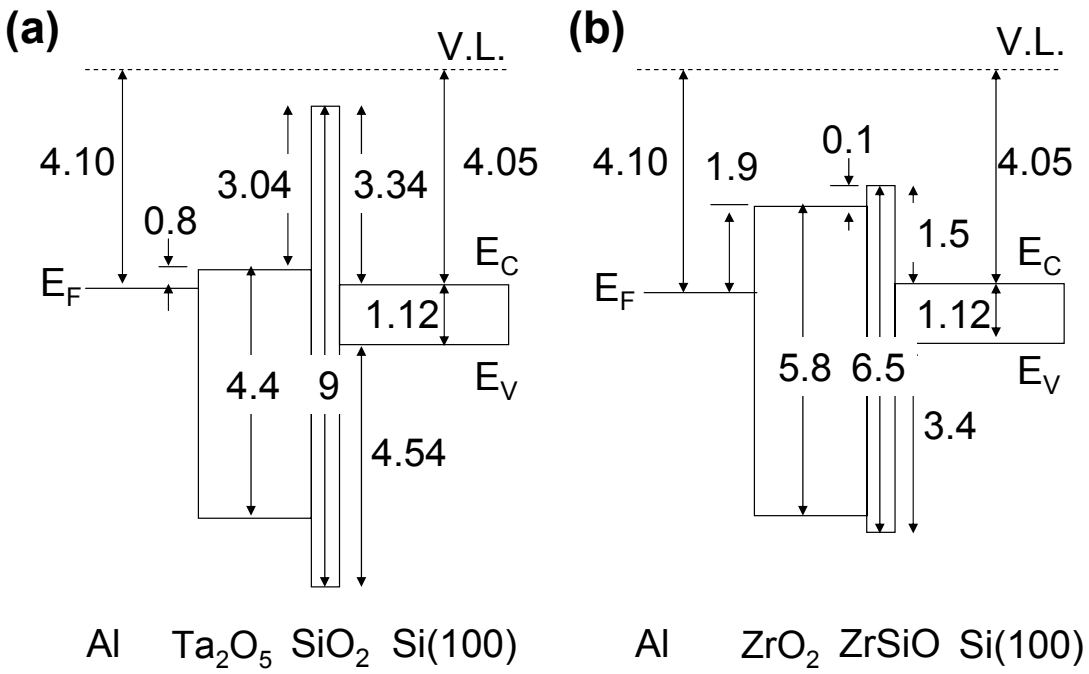


Figure 52. Energy band diagrams of (a) Ta_2O_5 and (b) ZrO_2 gate dielectrics in contact with Si substrates and Al gate electrodes. Numerical values in the band diagrams were cited from Table III. V.L. indicates the vacuum energy level, E_C and E_V are the conduction and valence band edges of Si, respectively, and E_F is the Fermi level of the Al gate.

In Fig. 52, the Ta_2O_5 film has a smaller bandgap (E_g = 4.4 eV) as well as a small electron barrier height with the (100) Si substrate (Φ_{Be} = 0.3 eV). However, the ZrO_2 film has a slightly larger E_g (5.8 eV) and a much larger Φ_{Be} (1.4 eV). If there was no interface layer with Si, the bulk Ta_2O_5 film should be more susceptible to the substrate injection than the ZrO_2 film under a positive bias. However, the SiO_2 layer at the Ta_2O_5/Si interface changes the mechanism of the electron injection from the substrate. SiO_2 layer is a better insulator (E_g = 9 eV and Φ_{Be} = 3.34 eV) than ZrSiO (E_g = 6.5 eV and Φ_{Be} = 1.5 eV), which is formed at the interface between ZrO_2 and Si. Electrons injected from the Si substrate have to first penetrate the interface layer before reaching the bulk high-k gate dielectric. Assuming a similar interface layer thickness for both cases, the SiO_2 layer is much more effective in blocking the electron transport than the ZrSiO silicate layer. For example, the silicate interface is closer to a ZrO_2 layer and is much easier to breakdown than SiO_2.[4,54,172] As a result, the higher current density observed for the pure ZrO_y film at low electric fields, as shown in Fig. 51, was possibly attributed to this early breakdown of the silicate interface. On the other hand, no early breakdown of the pure TaO_x film was observed at the same electric field range. The Zr-doped TaO_x film had a similar interface layer, i.e., Zr_xSi_yO, as seen from SIMS in Fig. 39. Therefore, they also showed higher current densities at low electric fields. It should be mentioned that the numerical values in Fig. 52 might vary with the film composition and fabrication technique. The film bulk composition influenced the interface properties. In other words, Fig. 52 only served as a qualitative illustration. In addition, the experimental results showed that a higher annealing temperature transformed the

interface layer towards a stoichiometric silicon dioxide (SiO_2) layer, regardless of the original interface composition, i.e., SiO_x or Zr_xSi_yO.[70,153]

The I-V curves in Fig. 51 were not symmetric under negative and positive biases, i.e., under accumulation and inversion conditions. This was due to two reasons: (i) the difference in the carrier barrier height, and (ii) the difference in the electric stress. Table III and Fig. 52 showed that for both Ta_2O_5 and ZrO_2, the hole barrier heights (Φ_{Bp}) were much larger than the electron barrier heights (Φ_{Be}). This difference made the hole injection, from the Si substrate into the high-k gate dielectric film, less likely in comparison to the electron injection. Furthermore, only the electron injection had to be considered for the gate injection since only free electrons existed in the metal gate. Therefore, only the electron injection and the corresponding barrier heights had to be taken into account in the case of high-k gate dielectrics.

Obviously, the barrier heights for the gate injection and the substrate injection were very different. In addition, there was an extra interface layer located at the contact with the Si substrate. As in the case of Ta_2O_5, the electrons injected from the Al gate encountered a barrier height of 0.8 eV, but encountered a larger barrier of 3.34 eV if injected from the substrate due to the SiO_x interface. This I-V asymmetry phenomenon had been studied by Houssa et al. using an intentionally deposited SiON interface layer between a ZrO_2 film and a Si substrate.[8,158] Different metal gate electrodes, such as Pt and Al, were used to investigate the gate injection impact. Their results showed that this I-V asymmetry was mainly attributed to the asymmetry of the injection energy barriers, which agreed with our conclusion.

The electrical stress asymmetry might also play a role in the I-V asymmetry, especially when a low quality interface layer existed. The electrical stress mechanism in the inversion region was different from that in the accumulation region. Under inversion, the reverse bias generated a wide depletion region in the Si substrate, which created a large band bending.[3] This band bending consumed a substantial gate voltage. On the contrary, the band bending in the accumulation region was negligible due to a large density of majority carriers (holes), which accounted for a negligible voltage drop. When the same gate voltage was applied under accumulation and inversion, the electrical stress experienced by the high-k gate dielectric layer was much smaller under the inversion condition than under the accumulation condition.

In view of kinetic stress of the injected electrons, the situation is the opposite. Within a reverse-biased Si substrate, the electrons, which were generated in the wide depletion region, were able to obtain a high kinetic energy due to the large band bending and the strong corresponding electric field. These energetic electrons bombarded the high-k/Si interface layer and created defects, such as fixed charges and interface traps.[7,89,157] If the density of defects at the interface accumulated to a threshold level as the electric field increased, an early breakdown occurred as mentioned above. This kinetic energy stress with a forward bias, however, is almost negligible due to the small band bending. Therefore, the electrons did not possess a high kinetic energy to bombard the gate/high-k interface. However, these electrons suffered a higher electric field inside the high-k dielectric layer, as discussed above. To summarize, the electrons under the

substrate injection and gate injection experienced totally different stress mechanisms that resulted in the I-V asymmetry.

Figure 53 compiles the current densities of the Zr-doped TaO_x films measured at -1 MV/cm under accumulation. Two film thicknesses, i.e., 15 nm and 30 nm, are shown together for comparison. The post-deposition annealing was performed in a 200 Torr O_2 ambient at either 600°C or 700°C. The thicker films, i.e., 30 nm, showed lower leakage current densities than the thinner ones, i.e., 15 nm, especially for higher Zr dopant concentrations.[46,165] The difference in the annealing condition did not show a noticeable influence on the current density. There are three key factors that determined the current leakage of a high-k gate dielectric layer: (i) morphology, (ii) bandgap, and (iii) barrier height.[4,12] The bandgap of high-k dielectrics mainly determined the electron-hole generation inside the high-k layer. The introduction of Zr dopant should increase the bandgap since ZrO_2 had a larger bandgap (5.8 eV) than Ta_2O_5 (4.4eV), as shown in Fig. 52. The conduction energy barrier, which was basically the product of the barrier height and the conduction length (thickness), was much larger for the thicker film. Therefore, the 30 nm films showed less leakage currents than their 10 nm counterparts. The difference in current density was much larger for the films with higher dopant concentrations, i.e., $Zr/(Zr+Ta) \geq 0.41$, which might be due to the morphology difference. It was shown in Fig. 49 that the thinner Zr-doped TaO_x films showed lower amorphous-to-polycrystalline transition temperatures than the thicker films when the $Zr/(Zr+Ta) \geq 0.41$. These crystallized films contain grain boundaries that are electrical short paths for current conduction. However, the thicker films, i.e., 30 nm, remained amorphous.

Therefore, the current densities in different doped films are similar. The 100 W Zr-doped TaO_x and the pure ZrO_y films showed much higher current densities than the others, which is due to the formation of polycrystalline phases. Since the current densities were measured under gate injection in Fig. 53, the high-k/Si interface played a minor role, as discussed previously. The barrier height difference at the interface had a minor impact to the current density here.

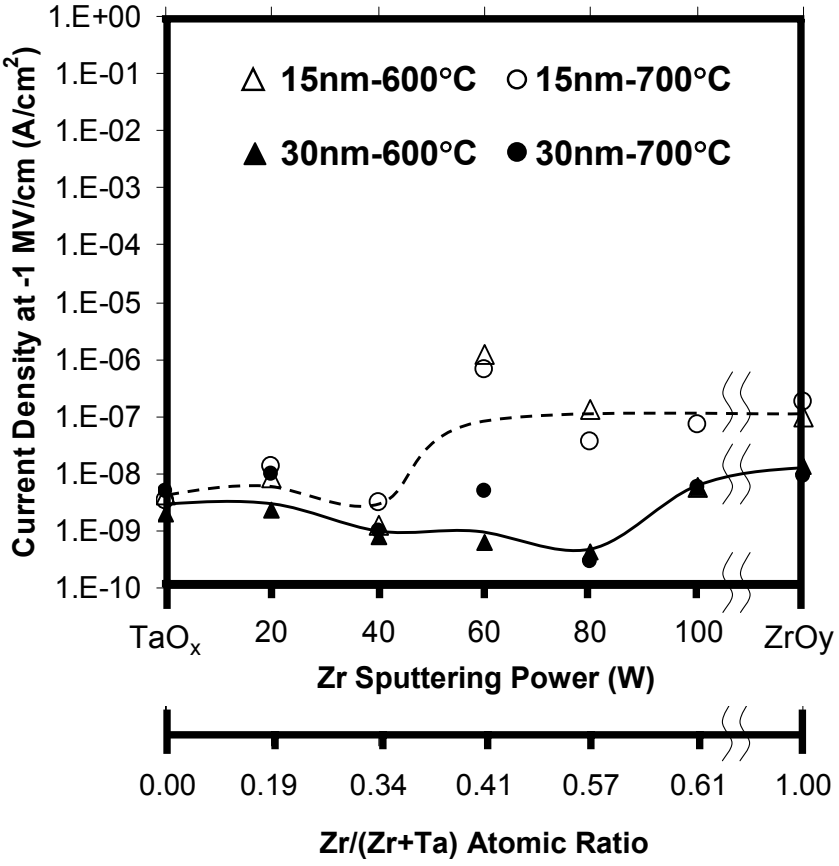


Figure 53. Current densities of the Zr-doped TaO_x films at -1 MV/cm (in accumulation).

In Fig. 53, the Zr dopant concentration in the Zr-doped TaO_x film has a strong influence on the current density. For the 15 nm samples, films with higher Zr co-sputtering powers, i.e., 60, 80 and 100 W, had larger current densities than that of the undoped TaO_x film. However, samples deposited with lower Zr powers, i.e., 20 and 40 W, showed similar current densities as the undoped film. Every 15 nm film had a current density $<10^{-7}$ A/cm^2, except for the film deposited with a 60 W Zr co-sputtering power, i.e., current density $\sim10^{-6}$ A/cm^2. The current density with 40 W was exceptionally low, i.e., $\sim10^{-9}$ A/cm^2. On the other hand, the current density of the 30 nm samples monotonically decreased with the increase of the Zr co-sputtering power up to 80 W. These results could be explained by the film morphology and bandgap difference as discussed before. The change of leakage current due to the introduction of a dopant into the film has been observed in other types of dopants, such as Ti, Si, Al, and Hf.[34,35,37,84] These dopants changed the TaO_x film's morphology, bandgap, and barrier height.[84]

3.3.2 Influence of Zr Dopant on Current Conduction Mechanism

Figure 54 shows four typical current conduction mechanisms for a thin gate dielectric layer under an electrical stress: (a) direct tunneling, (b) Fowler-Nordheim tunneling, (c) Poole-Frenkel emission, and (d) Schottky emission.[4,7,46,121] The direct tunneling occurs in a very thin gate oxide at a low electric field where the carriers can penetrate the insulator directly from one electrode to the other. The Fowler-Nordheim (F-N) tunneling, however, occurs in a thicker film at a higher electric field.[28] The carriers with the F-N mechanism do not get through the whole insulator, but tunnel into

the bended band edge of the insulator and move along this band edge. The main differences between these two tunneling mechanisms are the film thickness and the electric field. Because of that, the direct tunneling transports the carriers through a trapezoidal energy barrier, while the F-N tunneling transports the carriers through a triangular energy barrier. The formula for the direct tunneling is:[7]

$$J = \frac{A}{d^2}\{(\phi_B - \frac{V}{2}) \cdot \exp(-Bd\sqrt{\phi_B - \frac{V}{2}}) - (\phi_B + \frac{V}{2}) \cdot \exp(-Bd\sqrt{\phi_B + \frac{V}{2}})\} \qquad [53]$$

in which,

$$A = \frac{q^2}{2\pi h} \qquad [54]$$

$$B = \frac{4\pi\sqrt{2m^* q}}{h} \qquad [55]$$

where h is Plank's constant (4.135×10^{-15} eV-s), m* is the effective mass of the carrier in the gate dielectric, V is the voltage drop across the gate dielectric, d is the film thickness, and ϕ_B is the barrier height. The formula for the Fowler-Nordheim tunneling is:[7,121]

$$J = \frac{A}{4\phi_B} E_i^2 \cdot \exp(-\frac{2B\phi_B^{3/2}}{3E_i}) \qquad [56]$$

where E_i is the electric field, i.e., V/d.

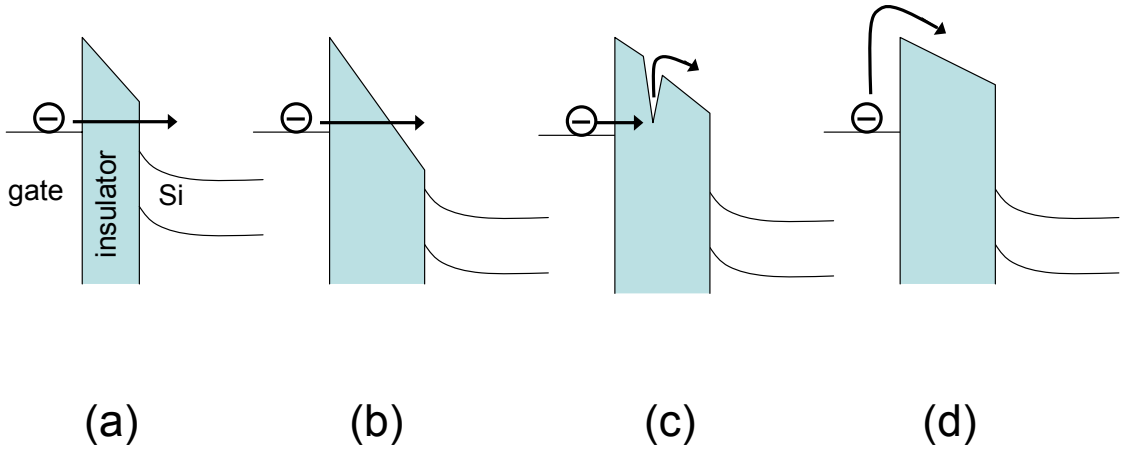


Figure 54. Schematic illustrations for the conduction mechanisms of: (a) direct tunneling, (b) Fowler-Nordheim tunneling, (c) Poole-Frenkel emission, and (d) Schottky emission.

In general, the direct tunneling dominates when the film thickness is under 5 nm because the tunneling current increases exponentially with the decrease of the film thickness, as shown in Eq. 53.[7,8] The Fowler-Nordheim tunneling, however, only dominates when the gate dielectric layer is thick and defect-free; in addition, the interface barrier height is very high, such as for SiO_2. In other words, the F-N mechanism conducts much less current than the other mechanisms. In the case of a deposited high-k dielectric film, unlike thermally grown SiO_2, the film is full of defects, i.e., at least one order of magnitude higher, and the interface barrier height, i.e., Schottky barrier height, is much lower. Therefore, it is almost universally true that either the trap-assisted Poole-Frenkel emission or the electrode-limited Schottky emission is the dominant conduction mechanism.[4,45,46]

In Figure 55(a)-(h), the I-V curves of the 15 nm Zr-doped TaO_x films were fitted with both the Poole-Frenkel and Schottky emissions. The I-V curves were measured under negative biases, i.e., gate injection. The P-F emission could be expressed by the following equation,[7,46]

$$J \propto E_i \cdot \exp\{-\frac{\phi_B - 2\sqrt{E_i / C}}{(kT/q)}\} \qquad [57]$$

while the Schottky emission could be expressed as:

$$J \propto T^2 \cdot \exp\{-\frac{\phi_B - \sqrt{E_i / C}}{(kT/q)}\} \qquad [58]$$

where T is the absolute temperature in Kelvin (K), the lumped parameter C is $4\pi\varepsilon_0 n^2/q$, ε_0 is the vacuum permittivity (8.85×10^{-14} F/cm), k is the Boltzmann constant (8.616×10^{-5}

eV/K), and q is the charge of one electron (1.6×10^{-19} C). For a perfect fitting with either the Poole-Frenkel or Schottky emission, the extracted dynamic dielectric constant, i.e., n^2 should be equivalent to the square of the film's refractive index (n).[46] Two theoretical I-V curves for the Poole-Frenkel emission and the Schottky emission mechanisms respectively were calculated with Eqs. 57 and 58. Fig. 55(a) and (b) show that the measured I-V curves of the doped films with a 40 W Zr co-sputtering power are closer to the Schottky emission I-V curve than the Poole-Frenkel curve at 600°C and 700°C, respectively. On the other hand, Fig. 55(c) and (d) show that the measured I-V curves with an 80 W Zr co-sputtering power do not fit either mechanism. The 700°C-O_2 annealing, however, shifted the measured I-V curve towards the Poole-Frenkel curve, possibly indicating a higher trap density after a 700°C annealing.[46,185] These traps were possibly located in the proximity of the Al gate electrode, since the current was measured under the gate injection. The electrons from the Al gate could tunnel into these traps without surpassing the metal-dielectric Schottky barrier, and were re-emitted from the traps to the conduction band of the gate dielectric to conduct current.

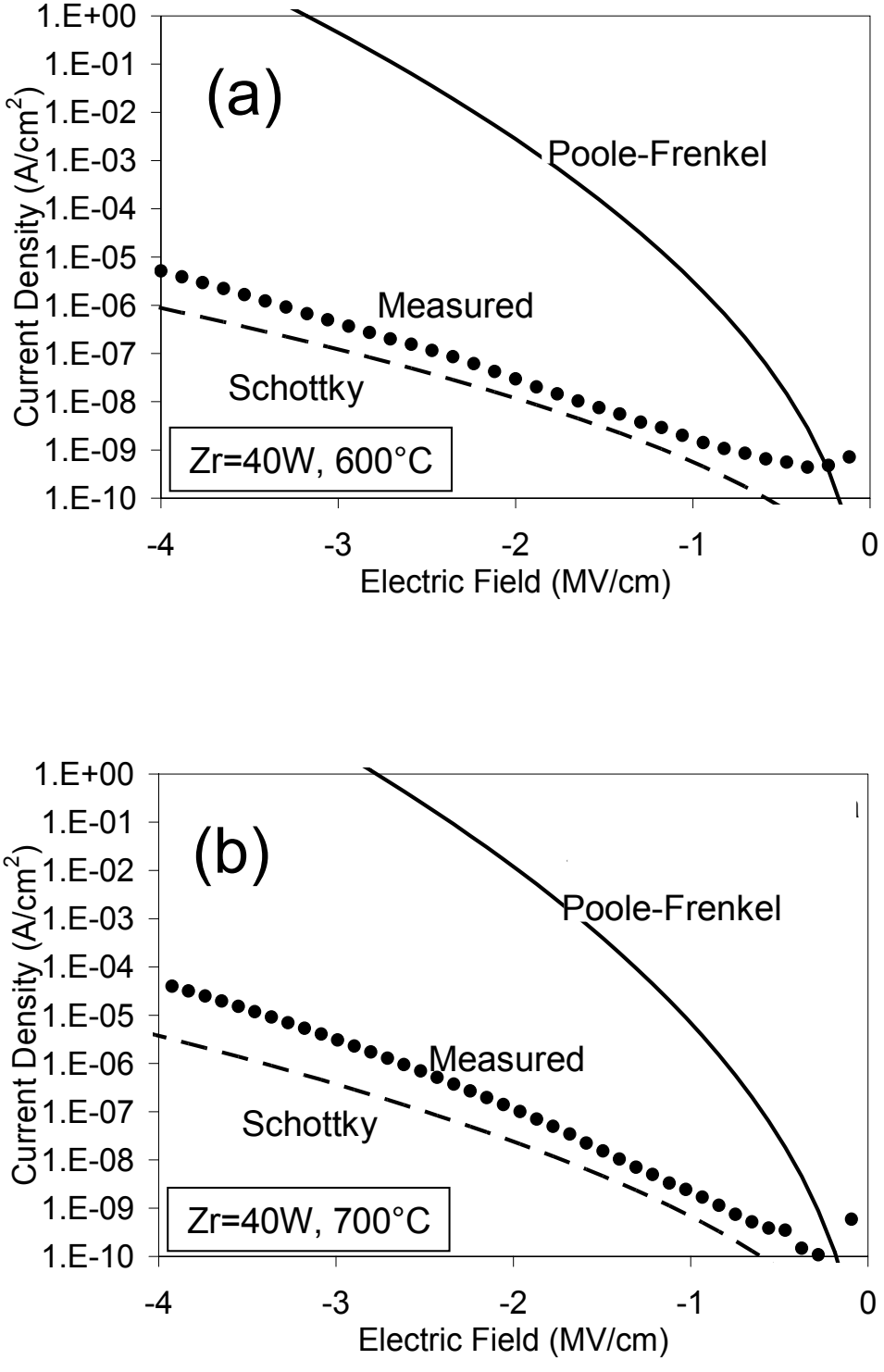
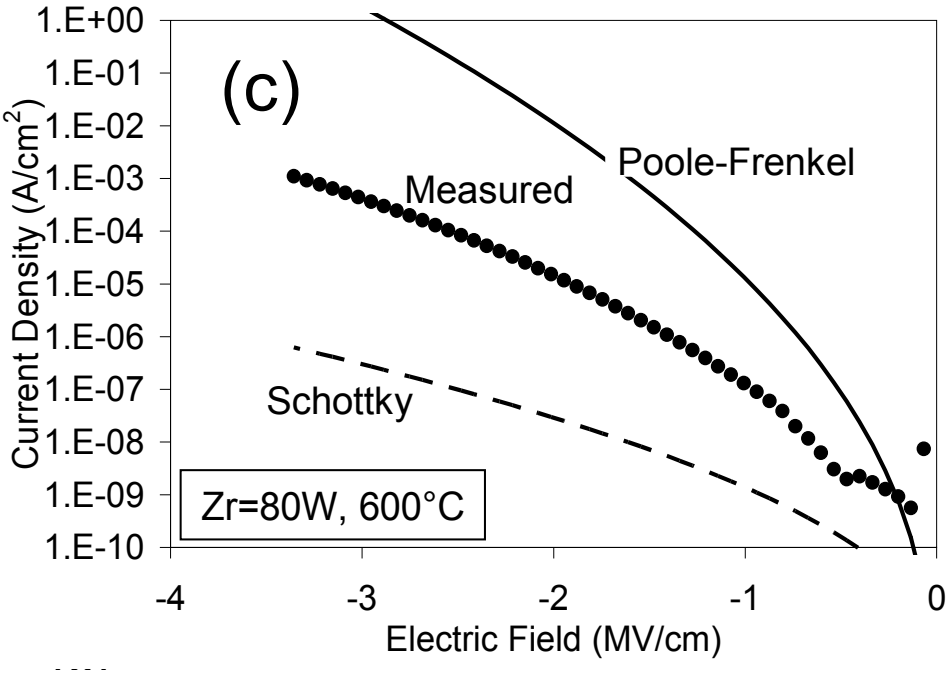


Figure 55. Conduction mechanism analyses of the 15 nm Zr-doped TaO_x films.



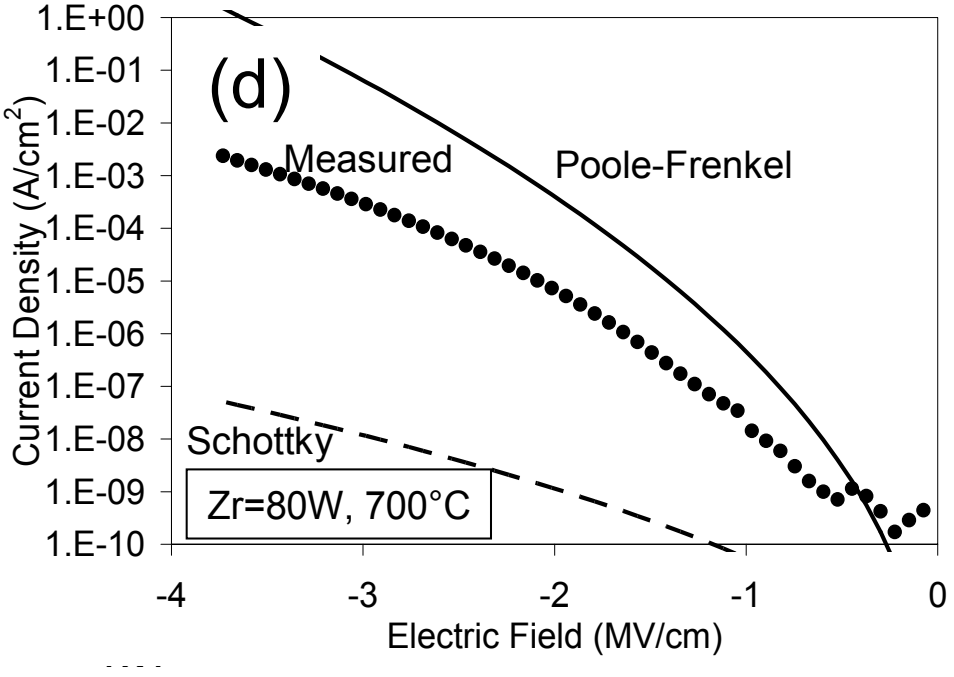


Figure 55. Continued.

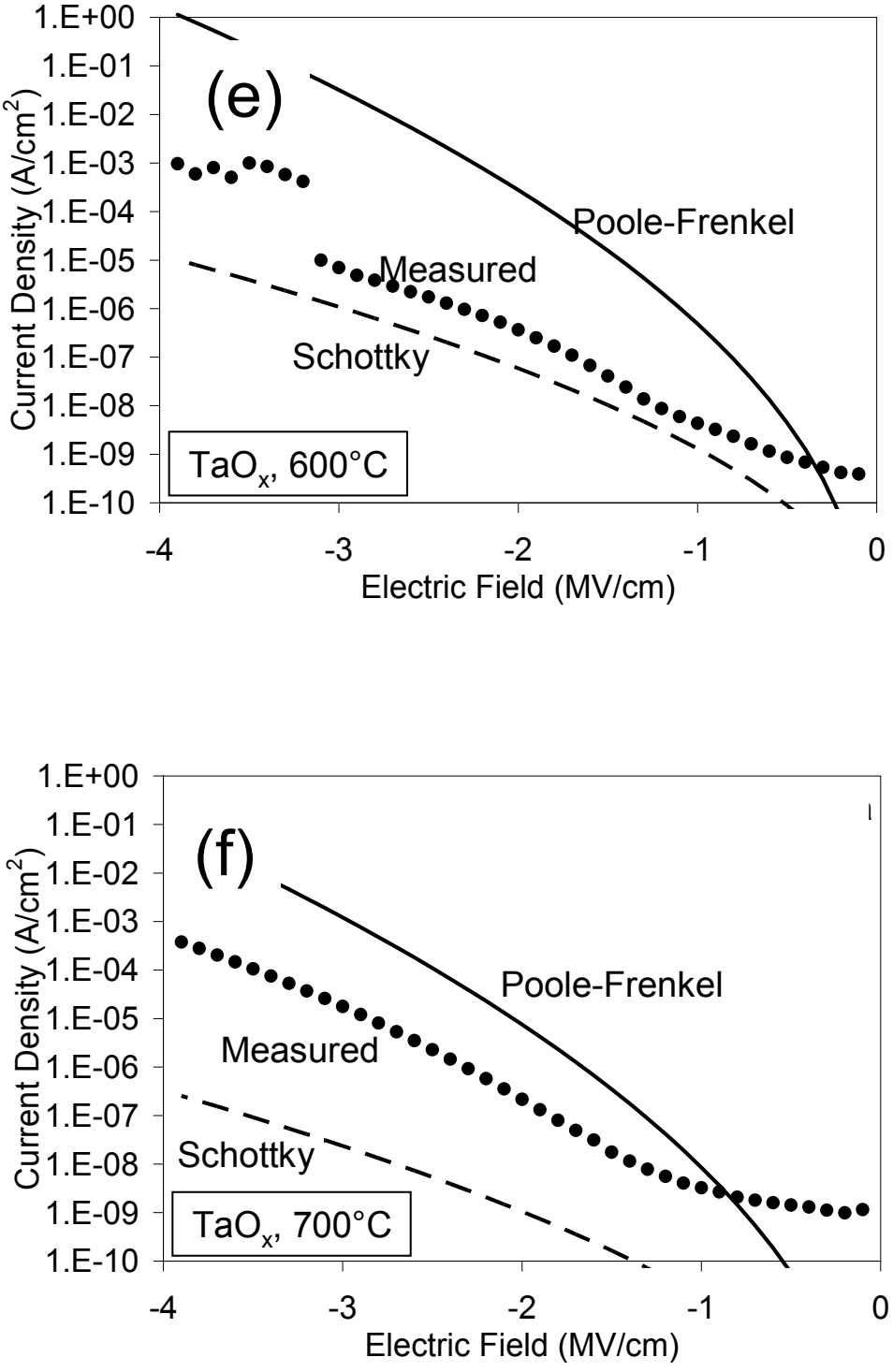


Figure 55. Continued.

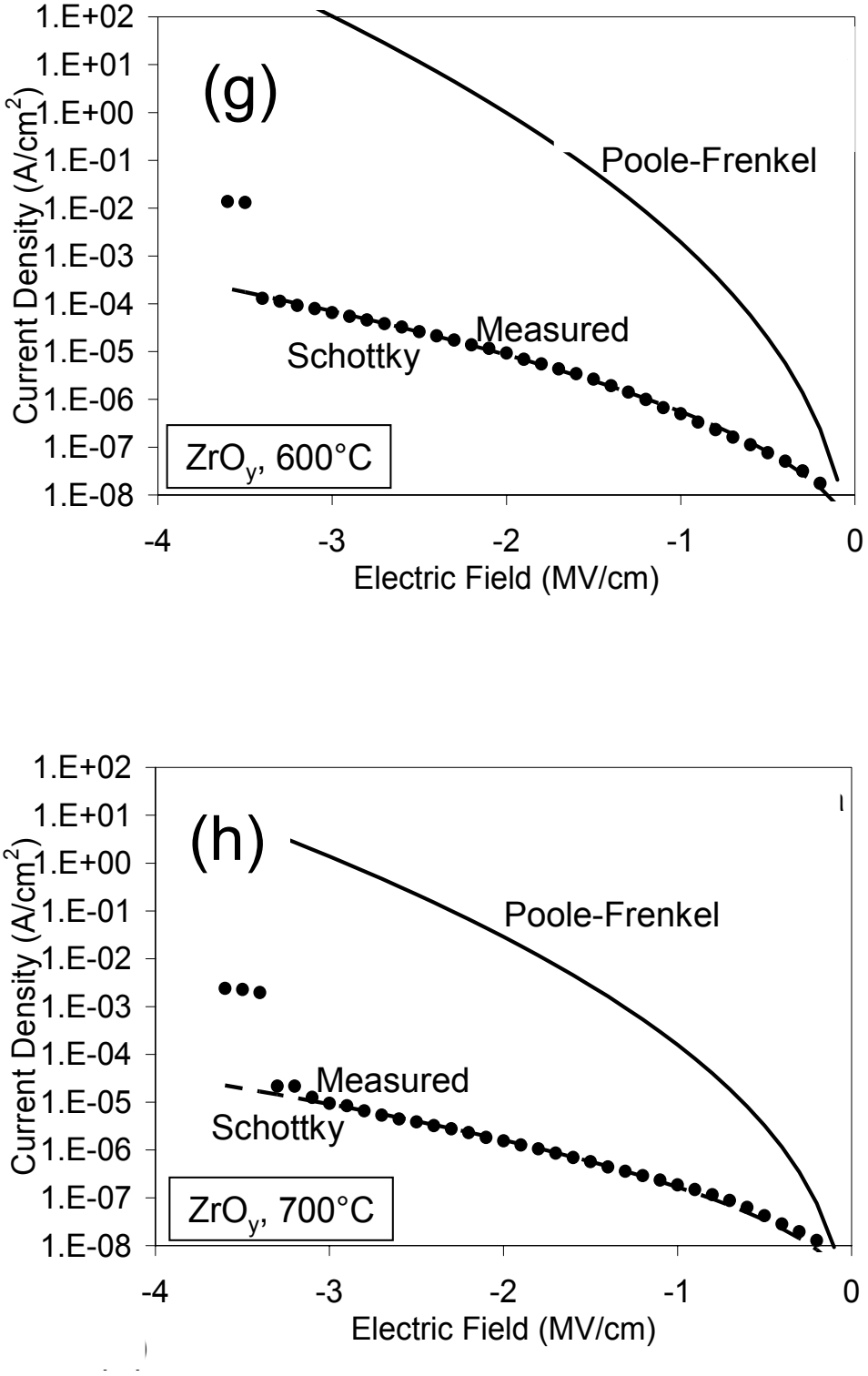


Figure 55. Continued.

There are three possible explanations for the change of the conduction mechanism due to the increased trap density when the annealing temperature was raised from 600°C to 700°C. The first explanation is the phase separation in the film, which roughens the Al/high-k interface.[81] Cava et al. reported that at a very high temperature (>1200°C), the excessive Zr dopant concentration in the doped Ta_2O_5 film caused the solid solution to separate into two phases: a low TaO_x-containing phase (Zr-rich) and a stoichiometric Ta_6ZrO_{17} phase.[81] The second explanation is the Zr silicidation, which transforms ZrO_2 into $ZrSi_2$.[176,179,186] The $ZrSi_2$ formation created the island-like nucleation sites and degraded the top interface. In addition, $ZrSi_2$ is a good conductor instead of an insulator. The third explanation is the film polycrystallization that results in the surface non-uniformity and creates defects.[46,106,114] Salam et al. studied the dominant conduction mechanism of the Ta_2O_5 thin film (deposited by MOCVD) doped with Ti or W. It was found that the Poole-Frenkle conduction, instead of the Schottky emission, was the dominant mechanism under an electrical stress.[82] A temperature dependence test of the I-V curve was used in their study to support their conclusion.

Fig. 55(e) and (f) show the I-V curves of the undoped TaO_x. The 600°C-annealed film fits the Schottky emission better, but the 700°C-annealed film moves towards the Poole-Frenkel mechanism, which is similar to the result of the 80 W Zr-doped TaO_x film. Atanassova et al. claimed that a higher temperature annealing reduced the defect density of Ta_2O_5, such as oxygen vacancies and dangling bonds, which minimized the Poole-Frenkel conduction.[165] The disagreement between our result and the above report is due

to the film's phase transformation phenomenon, i.e., the undoped Ta_2O_5 film crystallizes at around 650°C.[187]

Finally in Fig. 55(g) and (h), the Schottky emission dominates the conduction mechanism of the pure ZrO_y films at both 600°C and 700°C. Since the Schottky emission is an electrode-controlled conduction mechanism, the results suggests that the amount of defects at the Al/ZrO_y interface might be insufficient for the Poole-Frenkel emission to conduct. Therefore, the carriers had to pass the interface barrier height to conduct the current. This result agreed with the literature.[187]

To summarize, both the Zr dopant concentration and annealing temperature affect the conduction mechanism. The Zr dopant concentration changes the film morphology and the defect density near the interface. The annealing step densifies the film as well as roughens the interface. Therefore, the current conduction mechanism analysis is a good method to investigate and optimize the high-k film fabrication process.

3.3.3 Influence of Zr Dopant on Dielectric Constant

Figure 56 shows the effective dielectric constants of the Zr-doped TaO_x films as a function of the Zr dopant concentration. A post-deposition O_2 annealing was done at either 600°C or 700°C. The 100 nm-thick films are used as references because the impact of the low-k interface on the thick film is much less than that on the thin film.[4,8,36,45,46,153] The dielectric constants of the 100 nm TaO_x and ZrO_y films are about 18 and 20, which agree with the literature reports.[46,70,165,188] The interface layer thickness of the Zr-doped TaO_x film is about 2-3 nm, as shown by the TEM image in Fig. 40. This

interface layer has a significant effect on the effective dielectric constant of the 15 nm-thick sample.[8,36,153] The effective dielectric constant of the 15 nm film, which takes the interface layer into account, is about half of that of the 100 nm film.

The O_2 post-deposition annealing temperature, i.e., 600°C or 700°C, does not seem to make a noticeable difference on the dielectric constant. This indicates that the film's morphology and quality did not change significantly to alter the dielectric polarizability. The Zr dopant concentration, on the other hand, showed a strong influence. For example, Fig. 56 shows that the 700°C-annealed films had a maximum dielectric constant occurring at 60 W of Zr co-sputtering power, i.e., the atomic ratio of Zr/(Zr+Ta) = 0.41. The maximum value of the dielectric constant is ~15 for the 15 nm-thick film and ~22 for the 100 nm-thick film. As for the 600°C-annealed samples, however, the maximum dielectric constant of the 15 nm-thick films shifts to a lower Zr co-sputtering power, i.e., 40 W, with a value of ~13. The shift of the maximum dielectric constant might be due to the film morphology change with the annealing temperature, as discussed earlier in this chapter.

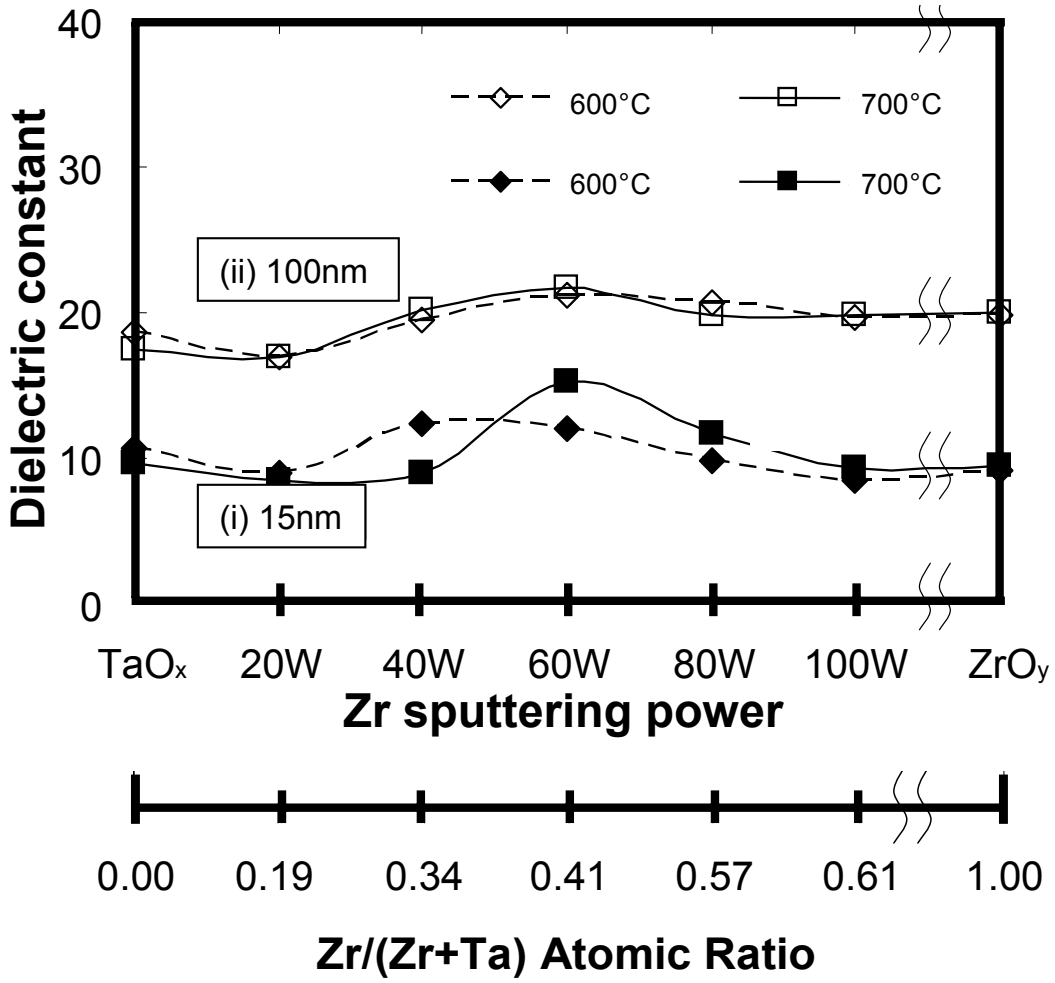


Figure 56. Dielectric constants of Zr-doped TaO_x films as a function of the Zr dopant concentration.

The improvement of the dielectric constant with the dopant introduction has been widely reported.[34-37,79-81,84] For example, Cava et al. reported a very high dielectric constant of ~50 for a very thick Zr-doped Ta_2O_5 ceramic film (1.25 cm).[81] This large k value possibly came from a high degree of crystallinity due to a high sintering temperature of >1400°C. Devine et al. proposed a model to predict the concentration dependence of the dielectric constant in the doped metal oxide by taking the effective molecular polarizability and molecular volume change into account.[189] However, the anomalous maximum of the dielectric constant at some optimized dopant concentrations could not be explained by this model. Lucovsky proposed that the introduction of the Zr atoms into a metal oxide may break the metal-oxygen bonds, which are aligned locally with the added Zr atoms under the applied electric field and enhance the polarization.[162,190-192] However, if the Zr dopant concentration is too high, the excessive Zr-O bonds will compete with the original metal-oxygen bonds and will dominate the polarization, which in turn eliminates this local alignment effect. Therefore, a maximum dielectric constant occurs in the medium range of the Zr dopant concentration.

3.3.4 Influence of Zr Dopant on Charge Defect

Figure 57 shows the normalized C-V curves of the 15 nm Zr-doped TaO_x films, annealed at 600°C or 700°C, with several Zr dopant concentrations. The direction of hysteresis loop is counterclockwise, as shown by the arrows, indicating the existence of electron traps.[7,108] From the C-V curves, the flatband voltage (V_{FB}) and hysteresis can be easily extracted, which are shown in Figure 58(a) and (b). The ideal flatband voltage

ΔV_{FB}^{0} was assumed to be -0.8 V, which was calculated from the Al work function (4.1 eV) and the p-type Si wafer with a doping concentration of ~10^{15} cm^{-3}.[3] The 700°C-annealed samples has a smaller hysteresis than the 600°C-annealed film, as shown in the upper part of Fig. 58(a). This occurs because a high annealing temperature is more effective in removing defects, such as electron traps, dangling bonds, and oxygen vacancies than the low annealing temperature.[185] Mobile ion charge contamination, especially the sodium ions (Na^{+}), is also possible to create C-V hysteresis.[108,185] However, the hysteresis loop should be clockwise if the mobile charge effect dominated. The 600°C-annealed samples also showed a larger negative V_{FB} than the 700°C-annealed samples. We can convert the data into the flatband voltage shift based on the ideal value (ΔV_{FB}), as shown in Fig. 58(b). With the increase of the Zr concentration, the temperature influence on the ΔV_{FB} is minimized. At a low Zr dopant concentration, i.e., Zr/(Zr+Ta) < 0.40, the 600°C-annealed sample shows a negative $\Delta V_{FB,}$ while the 700°C-annealed sample shows the opposite trend. The ΔV_{FB} is reduced to <50 mV when the Zr/(Zr+Ta) ~0.41 for both annealing temperatures. The flatband voltage shift can be related to the fixed charge Q_f in the gate dielectric layer, which can be expressed by the following equation,[4,7,108]

$$\Delta V_{FB} = -\frac{Q_f}{C_{ox}'} = -\frac{qN_f}{C_{ox}'} \qquad [59]$$

With Eq. 59, the fixed charge density N_f was found to be less than 10^{12} cm^{-2}.

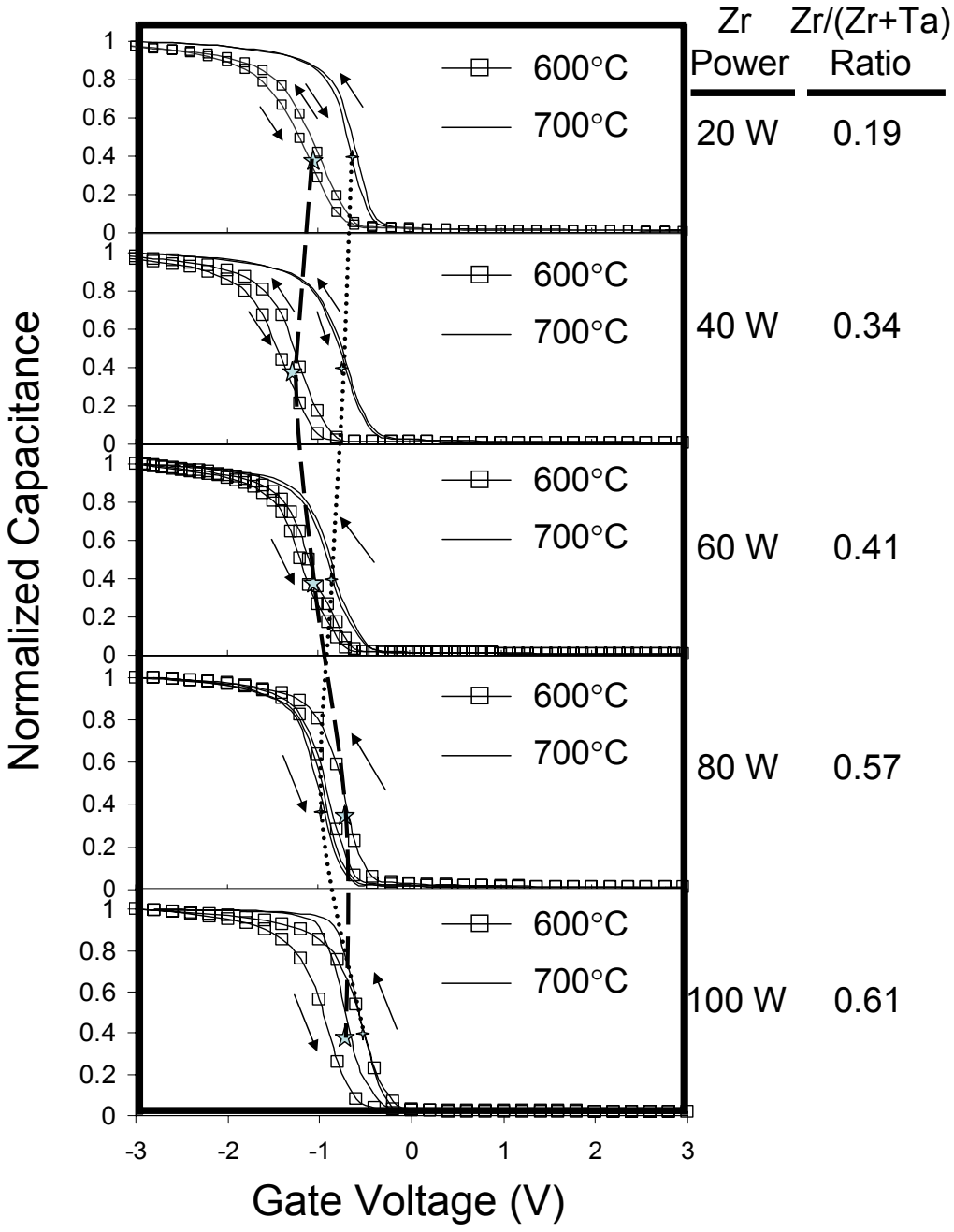


Figure 57. Normalized C-V curves of the 15 nm-thick Zr-doped TaO_x films.

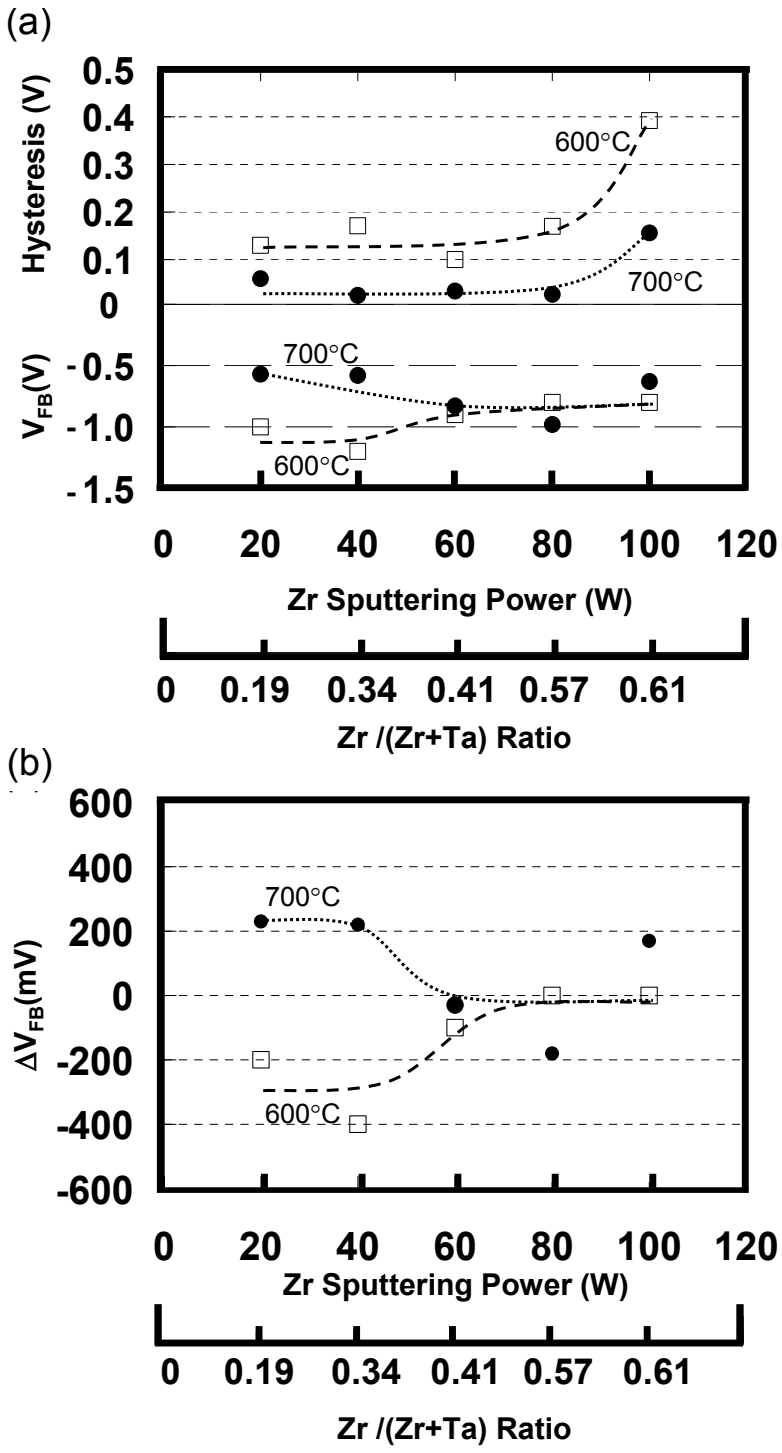


Figure 58. (a) Hysteresis and V_{FB} extracted from the normalized C-V curves; (b) the corresponding flatband voltage shift (ΔV_{FB}).

For the ZrO_2 gate dielectric, it was claimed that the O_2 annealing temperature could affect not only the density of the fixed charge but also the charge polarity.[185] For a thermally oxidized Ta_2O_5 film, the oxidation temperature had a similar effect.[109] This explains why the flatband shift (ΔV_{FB}) had different polarities for 600°C and 700°C annealing in Fig. 58(b). The higher Zr dopant concentration reduces the fixed charge density due to the charge compensation.[4,36] For example, the Al dopant shifts the flatband voltage to the positive direction and compensates the negative flatband shift.[4,8,20] It is also shown that, by applying the constraint theory, there exists a certain range of dopant concentrations at which the film is more stable and contains a lower defect density.[193,194]

3.4 Summary

Zr-doped TaO_x films, prepared by RF reactive co-sputtering, have been characterized physically and electrically in this chapter. An aluminum gate electrode was used to study the MOS capacitor properties. Influences of process parameters, such as the Zr co-sputtering power, post-deposition annealing condition, and film thickness, to the structural and electrical properties were investigated. Compared with the undoped TaO_x and ZrO_y films, the moderately Zr-doped film showed improved characteristics, such as a higher dielectric constant and a lower leakage current. A film with a small flatband voltage shift and a small hysteresis was obtained by carefully adjusting the experimental parameters. The conduction mechanism of the Zr-doped TaO_x film falls between the Poole-Frenkel conduction and the Schottky emission mechanisms,

depending on the Zr dopant concentration and the O_2 annealing temperature. A zirconium silicate, i.e., Zr_xSi_yO, interface layer was formed between the Zr-doped TaO_x film and the Si substrate, as confirmed by the SIMS depth profiling. The XPS results showed that with the addition of Zr in the film, all three binding energies of the core levels, i.e., Ta_{4f}, Zr_{3d} and O_{1s}, shifted to lower values. This observation was attributed to the partial charge exchanges among these three composing elements of the doped film. The amorphous-to-polycrystalline transition temperature of the TaO_x film was increased by the addition of the Zr dopant. This transition temperature, i.e., crystallization temperature, was increased by 300°C with a medium Zr concentration in the film, e.g., Zr/(Ta+Zr) ratio between 0.33 and 0.56. The grain sizes and texture orientations inside the crystallized film were functions of the Zr dopant concentration, annealing temperature, and film thickness. The addition of the Zr dopant possibly changed the surface energy constraint and the grain growth mechanism, which suppressed the amorphous-to-polycrystalline phase transformation.

CHAPTER IV

ZIRCONIUM-DOPED TANTANUM OXIDE GATE DIELECTRICS: PROCESS WITH TANTALUM NITRIDE INTERFACE LAYER*

4.1 Introduction

It has been reported that the incorporation of nitrogen (N) atoms at the gate dielectric/Si interface can effectively suppress the formation of the low-quality SiO_x interface layer.[23,26,73,87] In addition, advantages are achieved such as:[7]

1. A better resistance against dopant or impurity penetration due to the chemically stable SiO_xN_y layer
2. A high dielectric constant
3. An improved resistance to high electric stress
4. A radiation hardness

Conventionally, the N atoms are introduced in the form of either silicon nitride (SiN_x) or silicon oxynitride (SiO_xN_y) by a deposition or nitridation step. In this chapter, a different method of introducing nitrogen into the interface, i.e., depositing a thin tantalum nitride (TaN_x) layer before the high-k film deposition, was studied.[195]

*Part of the data reported in this chapter is reprinted with permission from "Influence of the 5 Å TaN_x Interface Layer on Dielectric Properties of the Zr-doped TaO_x High-k Film" by Jun-Yen Tewg and Yue Kuo, *Physics and Technology of High-k Gate Dielectrics II*, PV 2003-22, p. 25 (2003). Copyright 2004 The Electrochemical Society.

Figure 59 shows the structural models of the high-k gate dielectric film (a) without and (b) with the TaN_x interface layer deposition. Without the TaN_x interface layer, the effects of diffusion and intermixing between the high-k gate dielectric region and the Si substrate are serious. With the TaN_x interface layer, however, these detrimental effects are reduced due to the incorporated N atoms.[94]

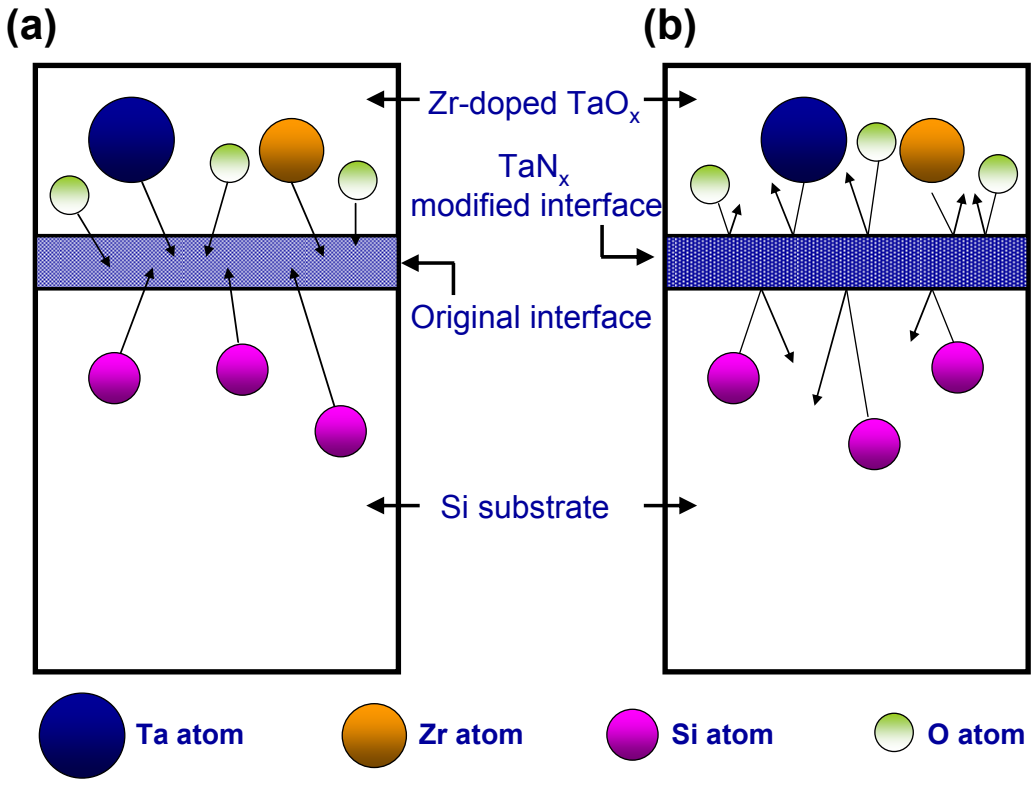


Figure 59. Models of the Zr-doped TaO_x/Si interfaces (a) without and (b) with a TaN_x layer.

A 5 Å TaN_x film was sputter-deposited on a p-type (100) Si substrate after a standard pre-cleaning step. A metallic Ta target was sputtered in a N_2/Ar (4 : 1) mixture at 5 mTorr. An 8 nm Zr-doped TaO_x film was deposited afterwards using both Ta and Zr targets in an O_2/Ar (1 : 1) mixture without breaking the vacuum. The Zr co-sputtering power was varied while the Ta power was fixed at 100 W to adjust the Zr dopant concentration. Electrical properties such as dielectric constant and leakage current were improved by the TaN_x insertion. The influence of the TaN_x interface layer to the compositional and chemical properties was also analyzed.

4.2 Chemical and Structural Properties of Zr-Doped TaO_x with TaN_x Interface Layer

The inserted interface layer of TaN_x was found to transform to tantalum oxynitride, i.e., TaO_xN_y.[23,26] The interface transformation was proven by the ESCA analysis of the Ta_{4f} core level, which detected a signal between TaN and Ta_2O_5.[93,196,197] The formation of the TaO_xN_y interface occurred because of the intermixing between the thin (~5 Å) TaN_x layer and the bulk high-k Zr-doped TaO_x film during sputter-deposition. It was also possible that the TaN_x layer was oxidized during the oxygen post-deposition annealing step because oxygen has a high diffusion coefficient at the high annealing temperature.[21,46,87] TaO_xN_y is proposed to be a better insulator than TaN_x.[23,26] It also has a higher dielectric constant.[93,197] Therefore, the transformation from TaN_x to TaO_xN_y is crucial for the high-k gate dielectric applications.[196]

Figure 60 shows the compositional depth profiling with the ToF-SIMS technique.[108] The tested samples were: (a) the undoped, (b) 20 W, and (c) 100 W Zr-

doped TaO_x films with an inserted 5 Å TaN_x layer. All of them were annealed at 700°C for 10 minutes in an O_2 ambient.

In Fig. 60(a), the nitrogen (N) ion signal is locally focused near the interface with a slight shift toward the bulk high-k region. This interface localization of the N atoms was also reported on the SiN_x interface layer case.[198] This observation might indicate a limited N diffusion into the high-k or SiO_2 gate dielectric layer. Both Si and N signals are maximized roughly at the same location, implying the possible existence of Si-N bond. In addition, the full width at half maximum (FWHM) of the Si signal is slightly larger than that of the N signal, indicating that a decent number of Si atoms associated with the N atoms exist at the interface. It was claimed that due to a large atomic size of N, its incorporation at the interface could effectively minimize the inter-diffusion and reaction between O and Si.[87] Based on our SIMS analysis, indeed, the Si-contained interface layer, i.e., SiO_x or Zr_xSi_yO, was reduced but not eliminated. The decrease of the Si signal towards the substrate is probably due to the instrumental artifact, i.e., the matrix effect.[108,113] The sputtering rate within the single crystal substrate was much slower than within the amorphous film. Since the SIMS spectrum was plotted along the time domain instead of the depth, the ion counts per second by the spectroscopy detector would decrease once it reached the substrate. The above discussion is also applicable to the Zr-doped TaO_x samples in Fig. 60(b) and (c).

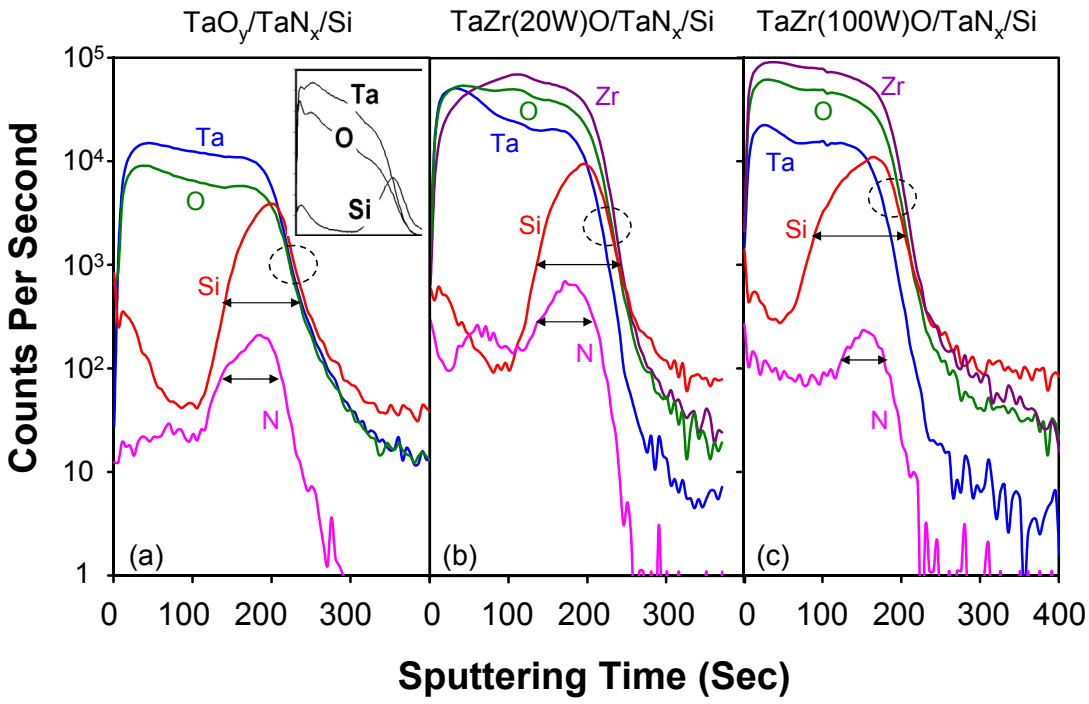


Figure 60. SIMS depth profiles of (a) $TaO_y/TaN_x/Si$, (b) $TaZr(20W)O/TaN_x/Si$, and (c) $TaZr(100W)O/TaN_x/Si$. The samples were annealed at 700°C for 10 minutes in O_2. The film thickness of the Zr-doped TaO_x layer was ~8 nm.

In Fig. 60(b) and (c), the Zr ion signals were added in the spectra. Compared to the Zr and O signals, the Ta signal descended much faster. It also dropped to a lower value than both Zr and O. This indicated that the Ta element was excluded from the substrate; in other words, the Ta atoms did not diffuse toward or react with the substrate as Zr and O did. A similar phenomenon was observed on samples without the inserted TaN_x layer, which was discussed in Chapter III. From the thermodynamics point of view, ZrO_2 is more stable than Ta_2O_5 when in contact with the Si substrate.[22] The Zr diffusion coefficient in SiO_2 and Si are larger than Ta.[166] Both factors induced this "Ta-pushing away" effect. Without the Zr dopant in the film, as shown in Fig. 60(a), this "Ta-pushing away" effect was not observed. As the Zr dopant concentration was increased, i.e., from 20 W to 100 W, the Ta atoms were pushed further away from the interface. Therefore, the interface layer only contains Zr, O, Si, and N. The Ta-rich region, i.e., TaO_xN_y, probably exists between the high-k bulk region and the above interface layer.[23,26,195]

The inset of Fig. 60(a) gives the depth profile of the undoped TaO_y sample without a TaN_x layer. It was noticed that the Ta signal descended before the peak of the Si signal. By comparing this to the depth profile with the TaN_x layer, as shown in Fig. 60(a), it was concluded that the TaN_x layer actually stabilized the Ta atoms at the interface. In other words, the formation of a Ta-N bond prevented the Ta atoms from being pushed away and forming a low-k SiO_x layer. Without any Zr dopant at the interface, a layer containing TaO_xN_y with certain amount of Si was in direct contact with the Si substrate.

4.3 Electrical Properties of Zr-Doped TaO_x with TaN_x Interface Layer

4.3.1 Influence of TaN_x Interface Layer on Current Density

Figure 61 shows the current densities, measured at V_{FB}-1 V in the accumulation region, of the Zr-doped TaO_x films. The influence of the TaN_x interface layer on the film leakage was investigated. Current densities of all the Zr-doped TaO_x films are reduced roughly by an order of magnitude with the insertion of the TaN_x interface layer. The same interface effect was reported on the Hf-doped TaO_x films.[23,26] It is known that incorporating a SiN_x or SiON interface layer could effectively decrease the current density through a high-k gate dielectric film.[52,87,94] The N atoms at the interface block the carrier transport and compensate for the interface stress, which reduced the film leakage.[87,199,200] However, this current reduction phenomenon was also explained by a compromise between an increase of the interface thickness and a decrease of the energy bandgap.[28]

Another possible explanation for the leakage reduction is the increase of the interface dielectric constant.[21,46] Assuming an interface layer with a thickness d_i and a dielectric constant k_i, the electric field experienced by this interface layer (E_i) can be expressed,[46]

$$E_i = \frac{V}{\frac{k_i}{k} d + d_i} \qquad [60]$$

where V is the total gate voltage, and d and k are the thickness and dielectric constant of the dielectric bulk region. In Eq. 60, the increase of k_i results in a reduction of E_i. In our

study, the interface layer had a higher dielectric constant, which produced a lower electric field at the interface and decreased the leakage current.

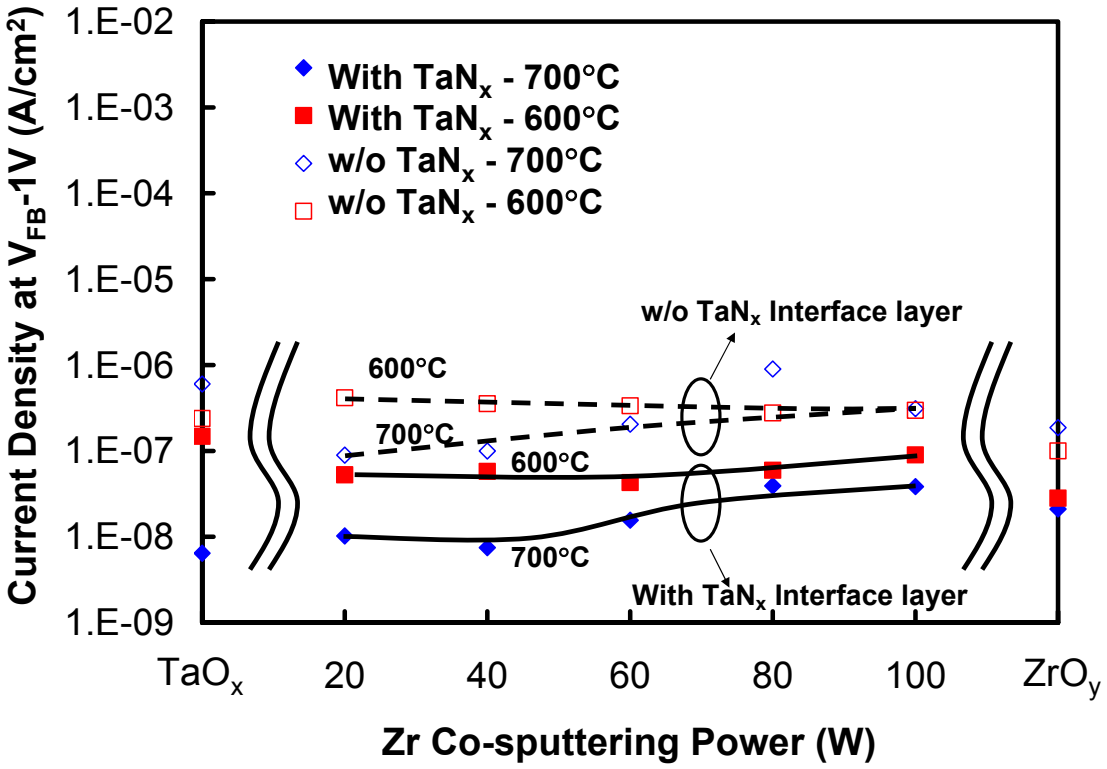


Figure 61. Current densities (at V_{FB}-1 V) of 8 nm-thick Zr-doped TaO_x films, with or without a 5 Å TaN_x layer, as a function of the Zr co-sputtering power.

In Fig. 61, the 700°C annealing reduced the film leakage current, regardless of the TaN_x layer. This was due to the densification of the film and reduction of the defects.[4,46] Compared to Fig. 53, the current density did not have a drastic variation as a function of the Zr dopant concentration. Previously, the change of the film morphology, i.e., amorphous to polycrystalline transition, was applied to explain the current variation. Therefore, the indifference of the current density with the TaN_x layer indicated the lack of film morphology variation. This occurred because the N atoms could slightly diffuse into the thin Zr-doped TaO_x film, which increased its crystallization temperature.[24,43,201] Therefore, all of the Zr-doped TaO_x films might remain amorphous regardless of the Zr dopant concentration. In addition, the films without the TaN_x layer in Fig. 61 also had much less variation of the current density than those in Fig. 53. This might be due to their much smaller thickness, i.e., 8 nm, compared to those in Fig. 53, i.e., 15 nm. A doped film at this thickness range was much more difficult to crystallize because of the surface energy hindrance.[170] On the other hand, the 700°C-annealed films without TaN_x did show a slightly larger increase in the leakage at Zr power = 60, 80, and 100 W, indicating that a small portion of the film might be crystallized.[195]

4.3.2 Influence of TaN_x Interface Layer on Conduction Mechanism

Figure 62(a) shows the I-V curves of 40 W Zr-doped TaO_x films with a TaN_x layer. The measurements were performed at many different temperatures to study the temperature effect. A Poole-Frenkel (P-F) plot, based on Eq. 57 in Chapter III, is shown in Fig. 62(b).[46,121] If $-\ln(J/E_i)$ was plotted as a function of 1/T, a good linearity among

the data points would suggest a dominant P-F conduction mechanism, which was our case. The I-V curve at 170°C showed an obvious degradation as the gate voltage exceeded -1.2 MV/cm, as shown in Fig. 62(a). For the further confirmation, a Schottky plot, based on Eq. 58, was conducted by plotting $\ln(J/T^2)$ versus $E^{1/2}$ at different temperatures, as shown in Figure 63.[46,121] However, no definite linearity was observed at all testing temperatures, which led to the abandonment of the Schottky mechanism.

In Chapter III, it was found that the conduction mechanism of the Zr-doped TaO_x film was strongly influenced by the Zr dopant concentration and annealing temperature. It shifted between the Schottky emission (electrode limited) and Poole-Frenkle emission (trap-assisted bulk limited). However, with the insertion of a TaN_x interface layer, the conduction is dominated by the Poole-Frenkel mechanism. This indicates that the defect density induced by TaN_x is sufficiently high for the P-F mechanism to dominate. In addition, the energy levels associated with these traps must be shallow enough inside the high-k dielectric film for the carriers to emit and conduct.[8] The introduction of the TaN_x interface layer increased the density of defects, such as fixed charges and interface states, which will be discussed later in this chapter.

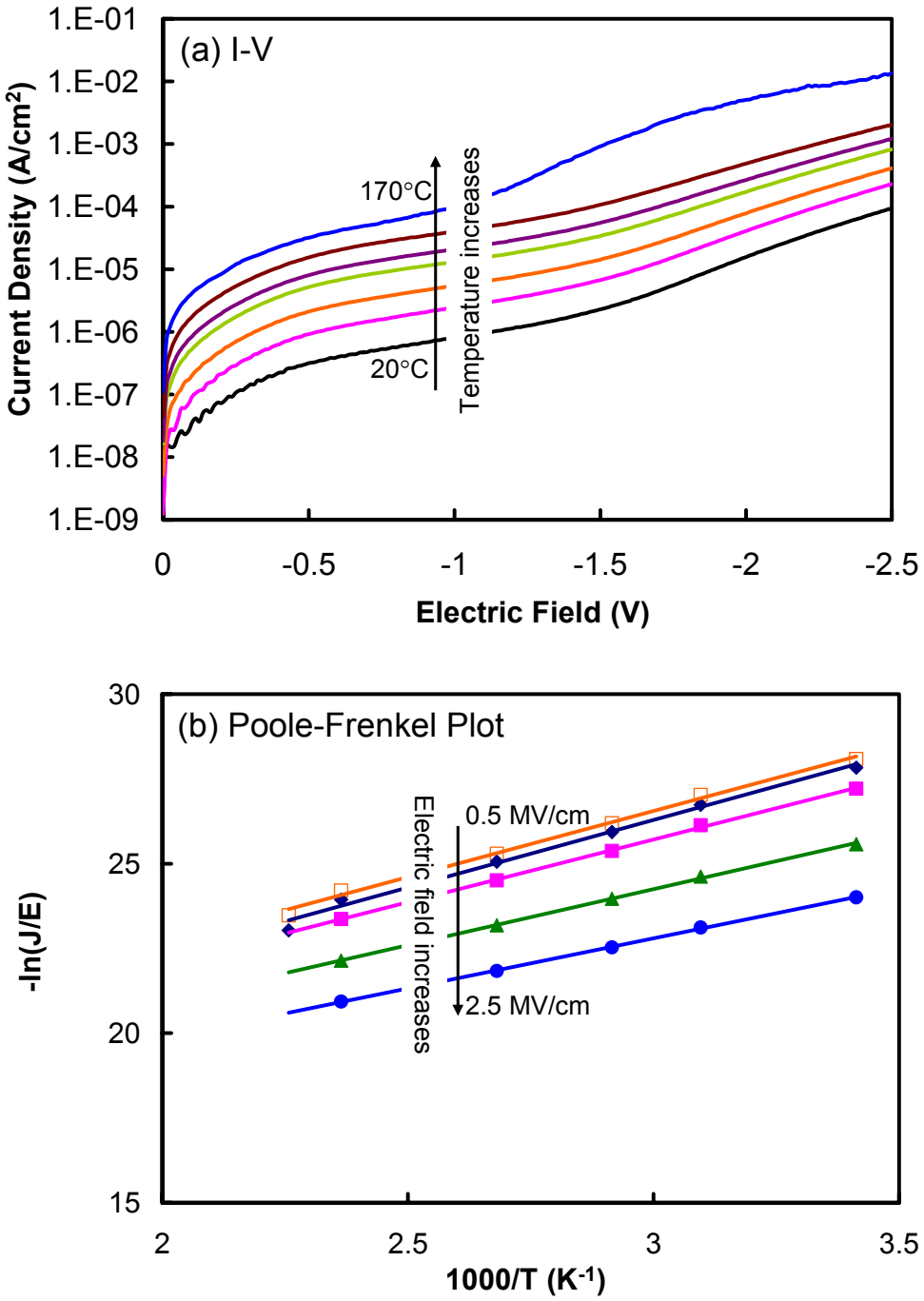


Figure 62. (a) I-V curves of an 8 nm-thick 40 W Zr-doped TaO_x film with a TaN_x interface layer. The measurements were done at 20, 50, 70, 100, 120, 150, and 170°C. (b) A Poole-Frenkel plot, i.e., -ln(J/E) vs. 1/T, conducted at 0.5, 1, 1.5, 2, and 2.5 MV/cm.

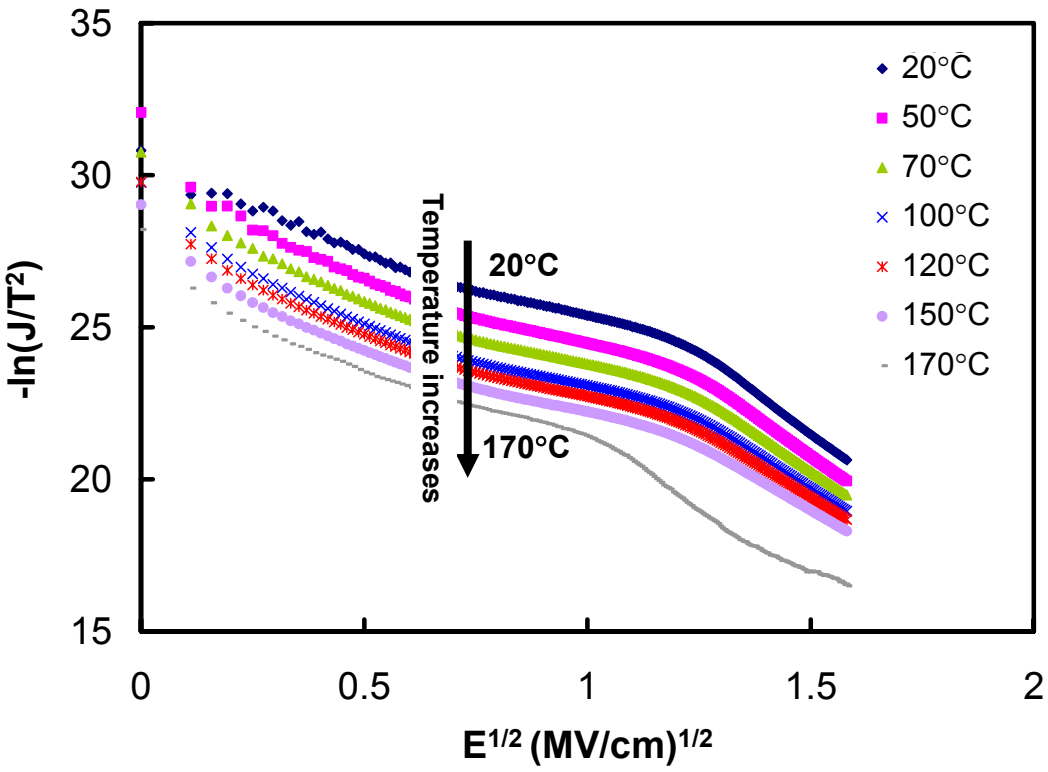


Figure 63. A Schottky plot of the 8 nm-thick 40 W Zr-doped TaO_x film with a TaN_x interface layer. The measurements were conducted at temperatures = 20, 50, 70, 100, 120, 150, and 170°C.

4.3.3 Influence of TaN_x Interface Layer on Breakdown Strength

Figure 64 shows the dielectric breakdown electric field (breakdown strength) of the Zr-doped TaO_x film as a function of the Zr co-sputtering power, the TaN_x interface layer, and the annealing temperature. The breakdown strength was extracted from the I-V curves in the accumulation region in order to avoid the lack of conducting carriers.[182,183] The calculation of the electric field was based on the total physical thickness of the stacked high-k gate dielectric film, i.e., ~ 8 nm. Without the TaN_x layer, the films' breakdown occurred between -5 MV/cm and -7 MV/cm. The insertion of a 5 Å TaN_x interface layer increased the breakdown strength roughly by 1 MV/cm. This phenomenon is consistent with previous reports of the Hf-doped TaO_x film.[23,26] There are two possible explanations for the breakdown improvement. First, the sputter-deposited TaN_x layer was oxidized to an oxynitride layer (TaO_xN_y).[93] This oxynitride interface could relax the excess compressive stress that existed between the high-k film and the Si substrate. Second, a Si-N bonding was formed at the interface.[93,197,202-204] This Si-N bonding, either in the form of Si_2=N-O or Si_3=N, could release the strain present at the interface and minimize the strain-induced defects.[203]

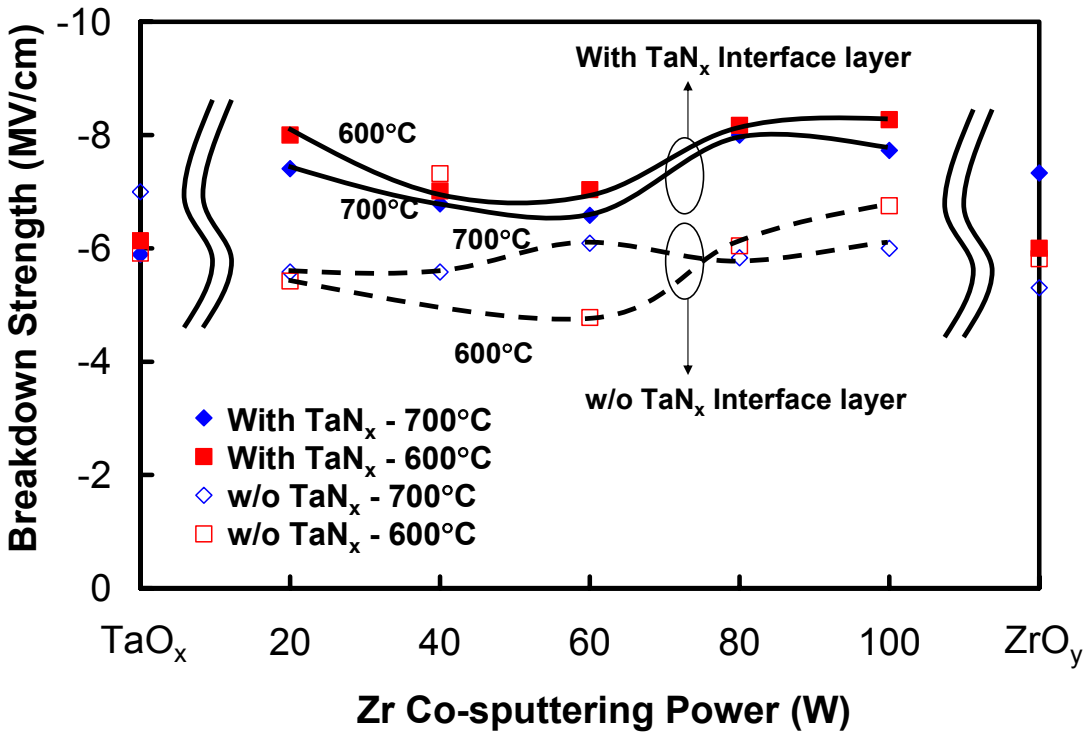


Figure 64. Breakdown strength of the 8 nm Zr-doped TaO_x films, with or without a TaN_x interface layer, as a function of the Zr co-sputtering power. The breakdown was measured under accumulation.

4.3.4 Influence of TaN_x Interface Layer on Dielectric Constant

Figure 65(a) shows the effective dielectric constants of the Zr-doped TaO_x films. With the insertion of the TaN_x layer, the dielectric constant was consistently increased by ~4, which reduced the EOT roughly by 5 Å, as shown in Fig. 65(b). The 20 W Zr-doped TaO_x films had the highest dielectric constants regardless of the TaN_x layer. The film without a TaN_x layer possessed a dielectric constant of 13 and 17 with the TaN_x layer. The EOTs of these two films were 2.5 and 2.0 nm, respectively. The improved dielectric constants might be attributed to the TaO_xN_y layer, which had a high dielectric constant of ~26.[93,197,205] In addition, the N atoms might be also incorporated into the high-k bulk film.[23,24,43,204]

The stacked structure of the high-k dielectric/Si can be expressed as a double-layer model, as shown in Figure 66(a). The interface dielectric constant can be estimated by,[4,46]

$$\frac{d}{k} = \frac{d_1}{k_1} + \frac{d_2}{k_2} \qquad [61]$$

where d_1 and k_1 are the thickness and dielectric constant of the bulk film, while d_2 and k_2 are those of the interface layer. The total thickness (d) is equal to $d_1 + d_2$ while the effective dielectric constant (k) can be measured. Assuming the bulk high-k film has a dielectric constant $k_1 = 20$, the interface layer has a $k_2 = \sim 4$ without the TaN_x layer, and a $k_2 > 8$ with the TaN_x layer. This is shown in Fig. 66(b). The calculated interface dielectric constants indicate that a substantial amount of Si was incorporated at the interface layer, which has been shown with the SIMS profiles in section 4.2.

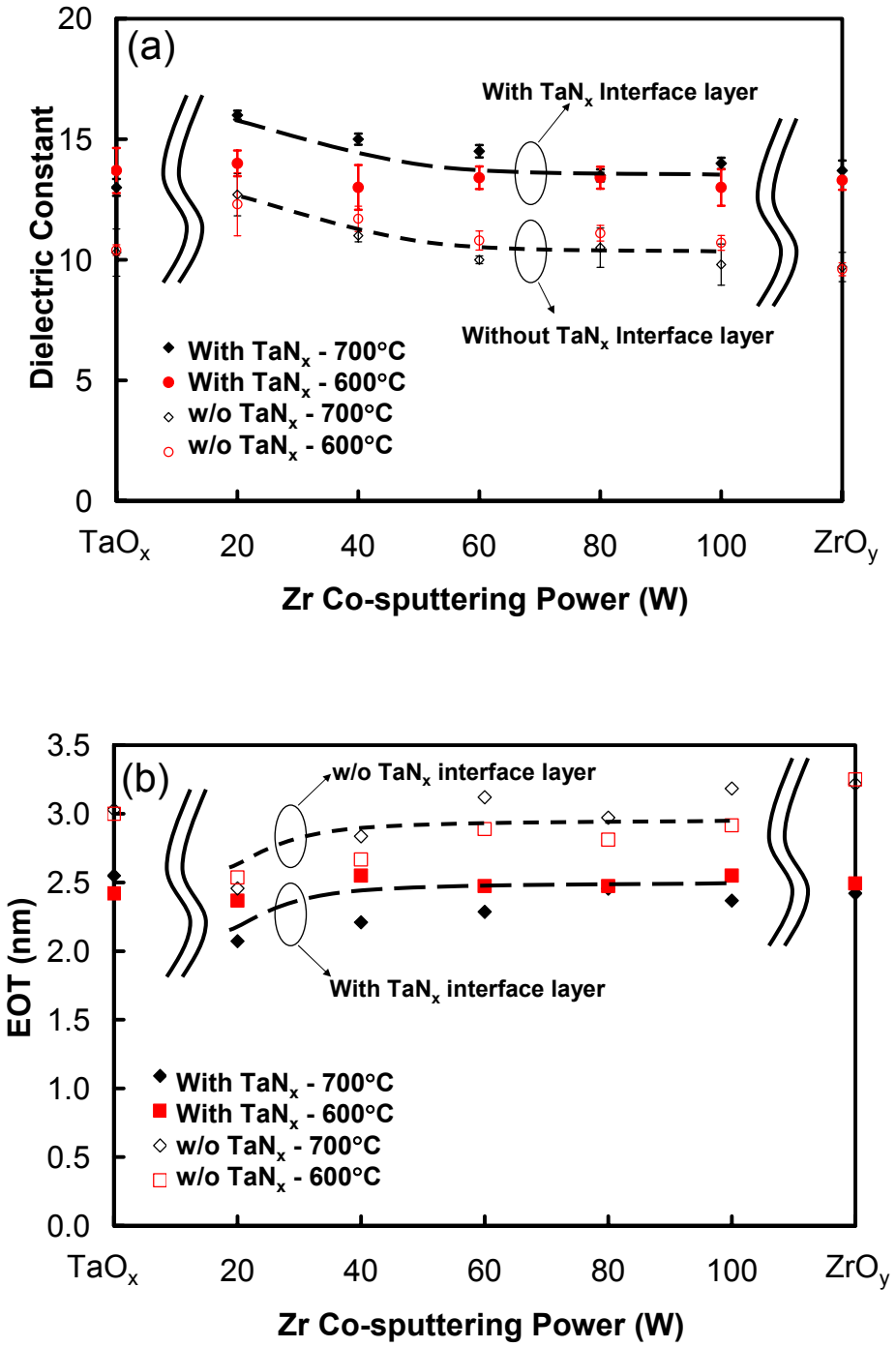


Figure 65. (a) Dielectric constant and (b) EOT of the 8 nm Zr-doped TaO_x film, with or without a TaN_x interface layer.

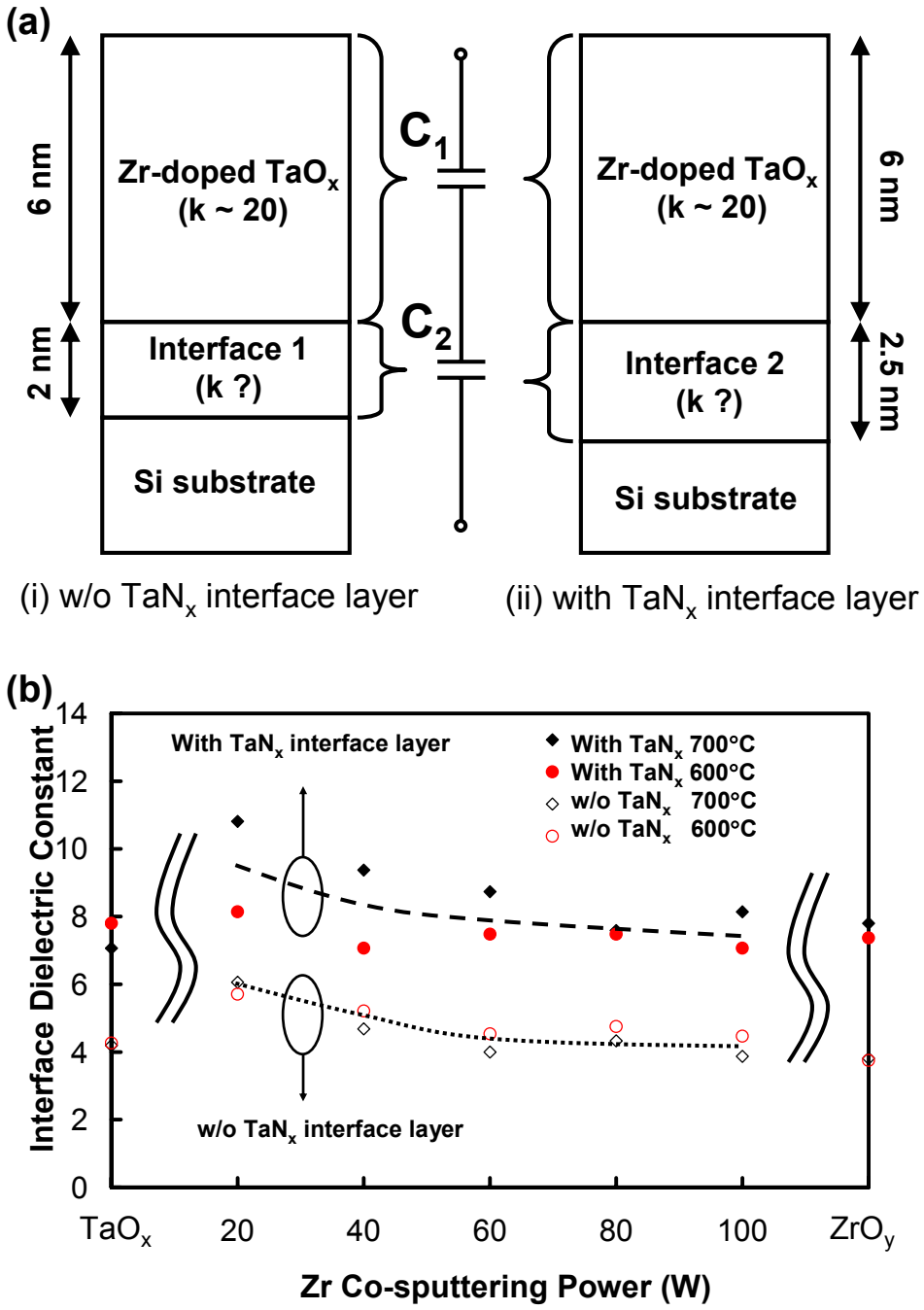


Figure 66. (a) Double-layer models of the stacked high-k gate dielectrics; (b) calculated interface dielectric constants.

4.3.5 Influence of TaN_x Interface Layer on Charge Defect

Flatband voltage shift

The fixed charge density (Q_f) inside a dielectric film is usually extracted by measuring the flatband voltage shift (ΔV_{FB}) from the ideal value (V_{FB}^0), which is determined from the metal gate work function and the Si substrate's Fermi level. The experimental flatband voltage (V_{FB}) could be determined from a high-frequency C-V curve, as discussed in Chapter II.[4,108] Eq. 59 was then used to relate Q_f and ΔV_{FB}. Figure 67 shows the ΔV_{FB} of the Zr-doped TaO_x films as a function of the Zr co-sputtering power and annealing temperature.

First, it was observed that all of the samples showed a negative shift ($\Delta V_{FB} < 0$), which indicated the positive fixed charges, as seen in Eq. 59.[4,108] However, the higher O_2 annealing temperature (700°C) reduced the ΔV_{FB} significantly in comparison to the lower temperature (600°C). This occurred because the higher temperature was more effective in annealing out the bond imperfections such as dangling bonds and oxygen vacancies.[46,150] These bond imperfections, especially those located in the proximity of the high-k/Si interface, functioned as positive charges and shifted the C-V curve negatively. When a TaN_x layer was inserted at this interface, the ΔV_{FB} became more negative, indicating more bond imperfections. The degradation of ΔV_{FB} due to the TaN_x insertion was found for the Hf-doped TaO_x films as well.[23,26] Cho et al. reported that a bulk TaO_xN_y film had a larger negative ΔV_{FB} roughly by 0.17 V than a bulk Ta_2O_5 film, under the same fabrication condition.[93] Jeon et al. also reported that the N incorporation into a ZrO_2 film shifted the flatband voltage negatively by 0.2-0.4 V.[92]

As shown in Fig. 67, the ΔV_{FB} degradation due to the TaN_x introduction could be effectively minimized by increasing the Zr dopant concentration and annealing temperature. For example, the ΔV_{FB} of the 600°C-annealed undoped TaO_x film with the TaN_x insertion was as large as -1.2 V. By increasing the Zr co-sputtering power to 100 W and the annealing temperature to 700°C, the ΔV_{FB} value dropped to -0.3 V. The pure ZrO_y has the lowest ΔV_{FB} value, indicating the lowest fixed charge density.[187,206]

The reduction of the ΔV_{FB} degradation with the increase of the Zr dopant concentration has been discussed in Chapter III, which is attributed to the charge compensation effect of Zr atoms in the TaO_x film.[4,8,36] The flatband voltage shift, i.e., the fixed charge polarity and density, of the ZrO_2 film is strongly dependent on the fabrication condition.[4] Therefore, the negative fixed charges introduced by the Zr doping can neutralize the positive fixed charges inside the TaO_x film and reduce the net fixed charge density. For example in Fig. 67, the undoped TaO_x film without the TaN_x interface layer has a ΔV_{FB} of -0.2 V after being annealed at 700°C. However, the introduction of Zr dopant effectively reduces ΔV_{FB} to about -0.1 V.

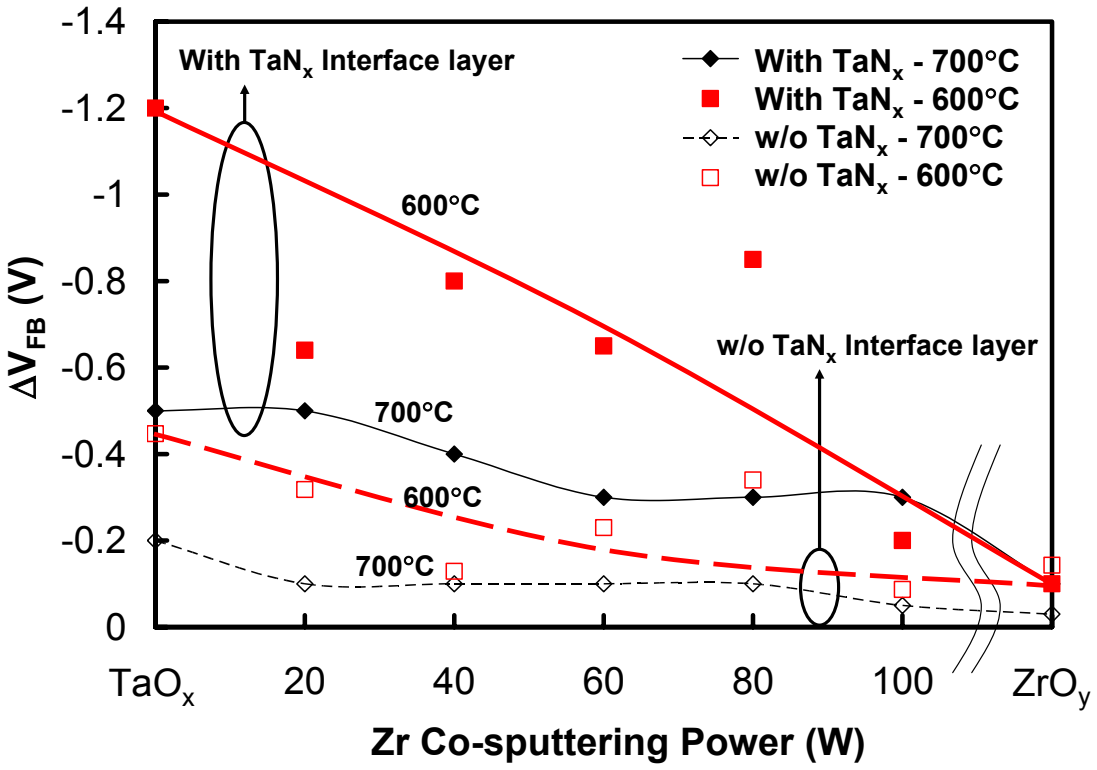


Figure 67. Flatband voltage shifts (ΔV_{FB}) of the 8 nm Zr-doped TaO_x films, with or without the insertion of a TaN_x layer, as a function of the Zr co-sputtering power.

Hysteresis

Electron traps in a high-k gate dielectric film can be extracted by means of the magnitude of the counterclockwise hysteresis of the C-V curve.[108] By trapping the negative charges that were injected during the gate bias scan, the C-V curve shifted toward the positive direction and caused hysteresis. Figure 68 shows the counterclockwise hysteresis as a function of the Zr dopant concentration and the annealing temperature. The gate voltage sweep used for the hysteresis characterization ranged from -4 V to +2 V, and then back to -4 V. This voltage range was roughly symmetric about the ideal flatband voltage, i.e., -0.8 V. The insertion of the 5 Å TaN_x interface layer did not show a noticeable effect on the hysteresis; however, the annealing temperature had a strong influence. In general, the 700°C annealing reduced the hysteresis by 50-100 mV compared to the 600°C annealing, which might be due to the defect removal.[28] The hysteresis was also reduced by increasing the Zr doping concentration, which is likely attributed to the charge compensation, as discussed in Chapter III.[4,8] The magnitude of the counterclockwise hysteresis is an indirect measurement of electron trapping.[7,108] The above result indicated that the insertion of the TaN_x interface layer did not increase the trap density of the whole high-k stack.

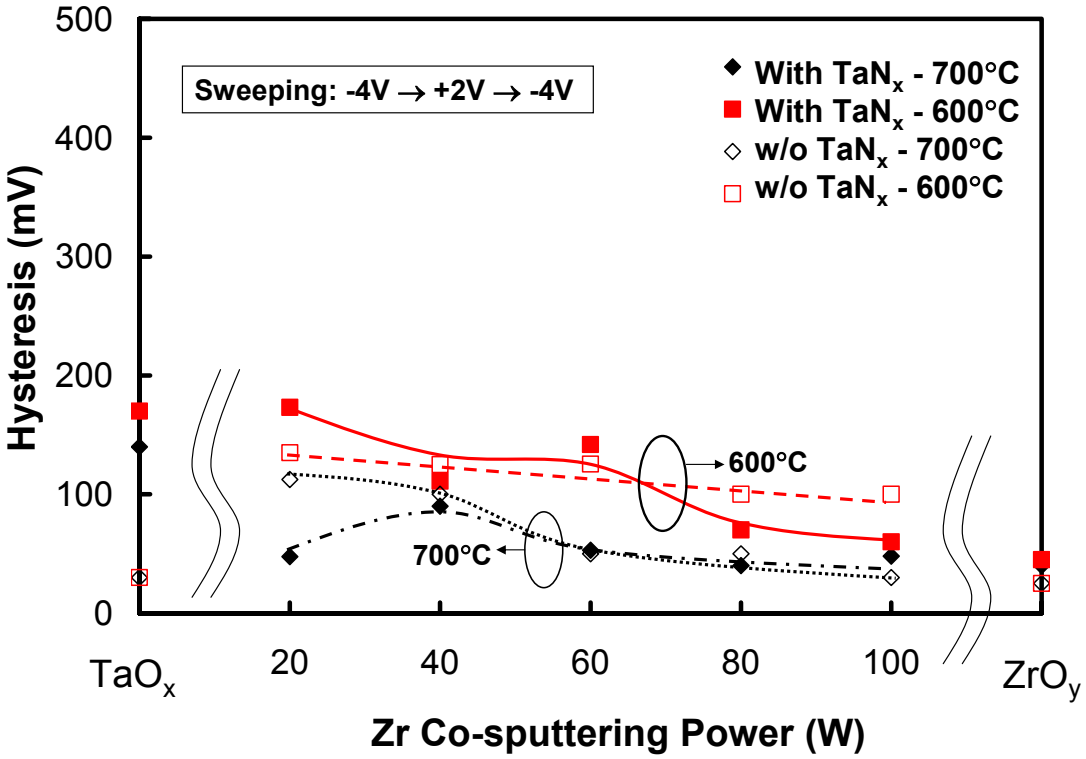


Figure 68. Hysteresis of the 8 nm Zr-doped TaO_x films, with or without a 5 Å TaN_x layer, as a function of the Zr co-sputtering power. The gate voltage was swept from -4 V to +2 V and then back to -4 V.

Interface state density

Figure 69 shows the interface state density (D_{it}) of the Zr-doped TaO_x film at the Si midgap level. The D_{it} values were estimated by using Terman method, as mentioned in Chapter II.[141] In the figure, the insertion of the TaN_x interface layer increased the D_{it} by about one order of magnitude, i.e., from ~10^{11} to ~10^{12} $cm^{-2}eV^{-1}$. This degradation of the interface state density was attributed to the introduced N atoms, which was common in the Si_3N_4 and SiON films.[52,73,207] The higher annealing temperature in an O_2 ambient, i.e., 700°C vs. 600°C, seemed to slightly reduce the D_{it}. The Zr dopant concentration or Zr co-sputtering power also affects the D_{it}, especially for the films without the TaN_x layer. For example, while the lightly doped films (Zr power = 20 and 40 W) have a D_{it} higher than 5×10^{11} $cm^{-2}eV^{-1}$, the heavily doped films (Zr power = 60, 80, and 100 W) have a D_{it} of ~1×10^{11} $cm^{-2}eV^{-1}$. This probably occurs because of a reduction of the interface stress by the Zr atoms.[36,208] However, the insertion of the TaN_x layer might partially block the Zr incorporation into the interface region. Therefore, the interface stress can not be completely relaxed.

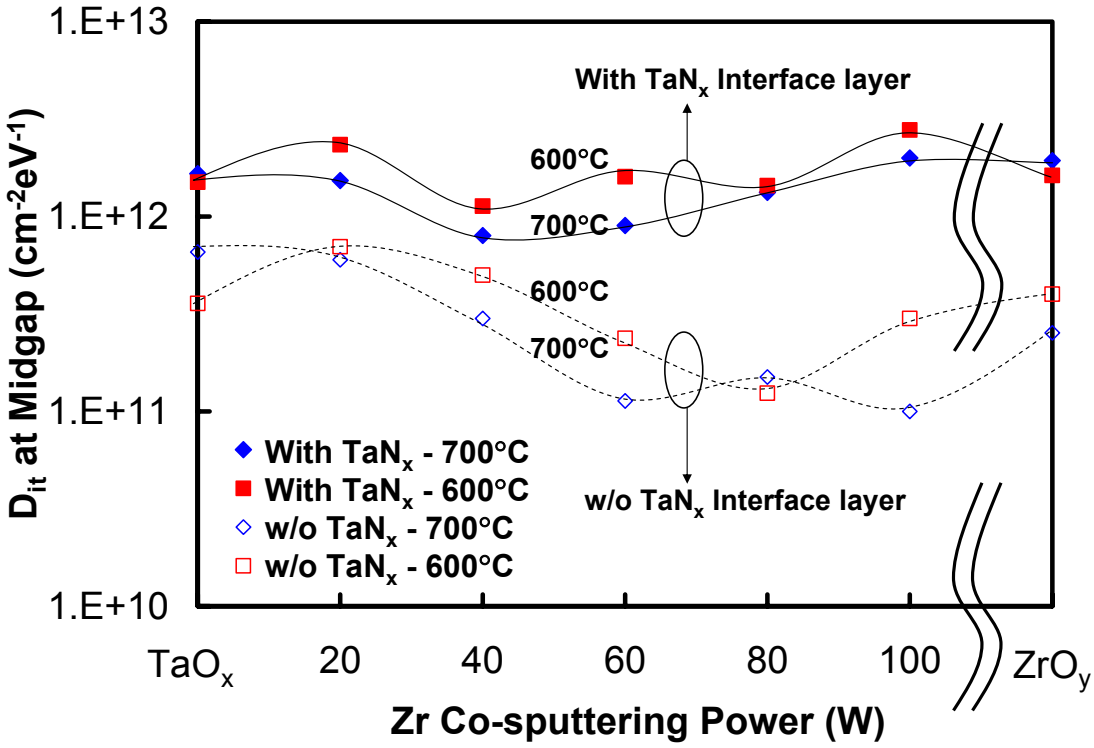


Figure 69. Interface state density at midgap of the 8 nm Zr-doped TaO_x film, with or without a TaN_x layer, as a function of the Zr co-sputtering power.

Frequency dispersion

The C-V curve behavior has to be measured at several probe frequencies to investigate the frequency dispersion in the accumulation and depletion regions.[209] For a good gate dielectric film, the frequency dispersion in the accumulation region is solely attributed to the series resistance effect, which comes from resistances of the Si substrate and the gate electrode.[8,158] This extrinsic C-V dispersion can be corrected in many ways.[210-212] The frequency dispersion in the depletion region, on the other hand, is commonly attributed to the existence of interface traps.[8,29,89] Figure 70 shows the frequency dispersion of the C-V curves measured at 1 MHz and 10 kHz. The frequency dispersion of an undoped TaO_x film, as shown in Fig. 70(a), is quite large in both the accumulation and depletion regions, indicating a high series resistance and a large amount of interface traps. With the doping using a 40 W Zr co-sputtering power, as shown in Fig. 70(b), the frequency dispersion is reduced significantly compared to the undoped film. The insertion of a TaN_x interface layer also reduces the frequency dispersion in the depletion region, as shown in Fig. 70(c), even without the Zr doping. However, the accumulation region of the C-V curve at 10 kHz does not saturate well compared to the Zr-doped TaO_x film.

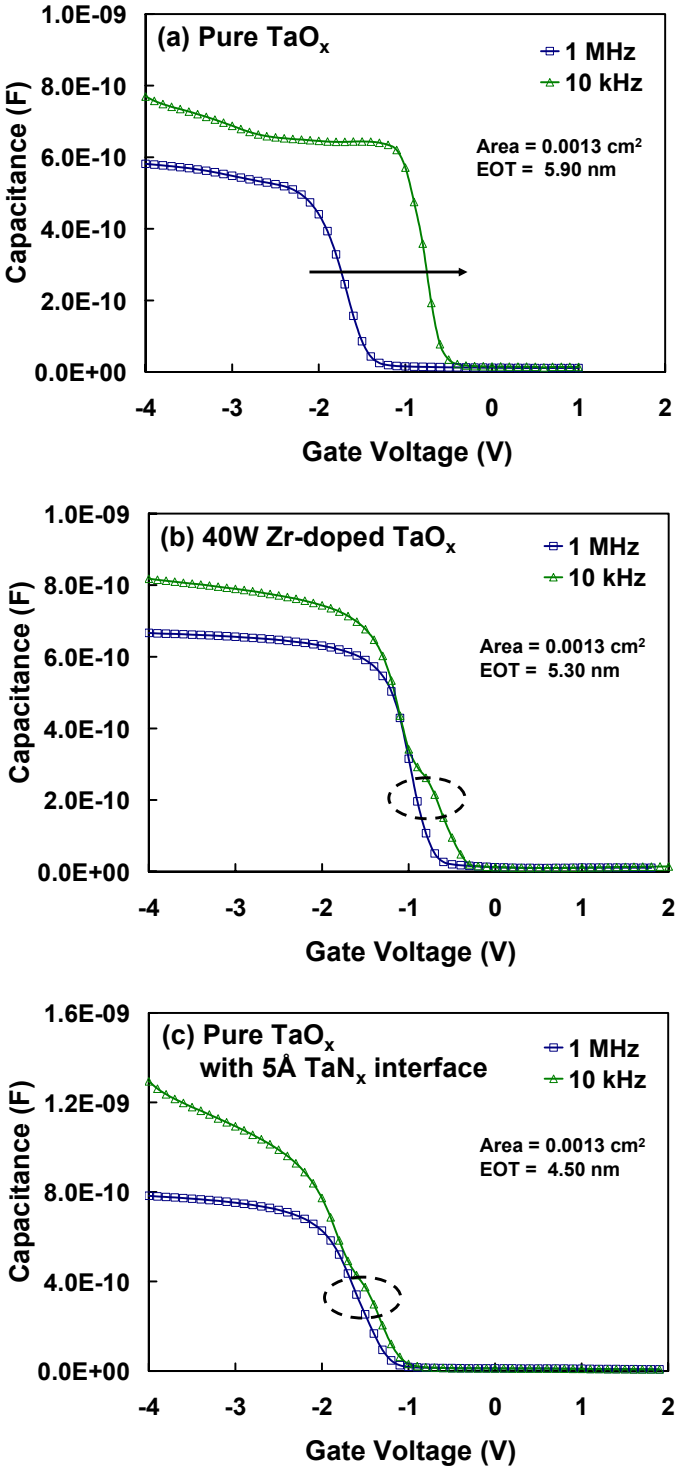


Figure 70. Frequency dispersions of (a) an undoped TaO_x film, (b) a 40 W Zr-doped TaO_x film, and (c) an undoped TaO_x film with a 5 Å TaN_x interface layer.

Except for the Zr-doped TaO_x sample shown in Fig. 70(b), both of the undoped TaO_x films, i.e., with and without the TaN_x interface layer, do not have a perfectly saturated accumulation region in the C-V curves at a low frequency of 10 kHz. Ramanathan et al. attributed this non-saturated low-frequency C-V curve to a defective metal oxide structure.[209] The metal oxide dielectric film that contained a significant amount of oxygen vacancies showed this unusual accumulation frequency dispersion, which could not be explained solely by the series resistance effect. The apparent dielectric constant calculated from this unsaturated accumulation capacitance would be too large for that expected from the electronic and ionic polarizations. This effect could be qualitatively explained by the Maxwell-Wagner space-charge induced polarization.[213] Wagner analyzed a bulk dielectric film that consisted of both perfect regions and defective regions containing charge defects. He found out that as the volume ratio of the defective region to the perfect region increased, the measured dielectric constant changed more profoundly when the probe frequency varied. Based on his theory, the pure TaO_x films, with or without a TaN_x interface layer, showed a more noticeable space charge-induced polarization compared to the Zr-doped TaO_x film. This indicates that a substantial volume of defective region containing oxygen vacancies exists inside the dielectric film. Finally, Ramanathan also pointed out that the accumulation C-V non-saturation was especially serious if the oxygen vacancies were mainly located close to the top metal gate electrode.[209]

4.4 Summary

In this chapter, a 5 Å TaN_x layer was inserted between the 8 nm-thick Zr-doped TaO_x film and the Si substrate in order to improve the dielectric properties for the gate dielectric application. Compared with the film without the inserted TaN_x layer, the new stacked structure has several advantages, such as a higher dielectric constant, a lower leakage current, and a larger breakdown field. However, the flatband voltage shift and interface state density are slightly degraded. The hysteresis did not vary significantly with this TaN_x layer. Both the Zr dopant concentration and annealing condition have significant impacts on these dielectric properties. The SIMS and ESCA results show that the structure of the inserted TaN_x interface layer was modified after a high temperature annealing. For example, a TaO_xN_y interface layer was formed and Si atoms were also included in this interface structure. Table IV summarizes the electrical and physical properties of the Zr-doped TaO_x films compared with a thermally grown SiO_2 at EOT = 2 nm.[4,7,33] The Zr-doped films were annealed at 700°C in an O_2 ambient. Compared to the thermal SiO_2, the TaN_x-inserted gate dielectric stack had a larger dielectric constant, i.e., by 4 times, and a smaller current density, i.e., by 5 orders of magnitude. However, the flatband voltage, hysteresis, and interface state density were inferior.

Table IV. Comparison among gate dielectric materials at EOT = 2 nm.[4,7,33]

Properties	Thermally grown SiO_2	(20 W) Zr-doped TaO_x without TaN_x	(20 W) Zr-doped TaO_x with TaN_x
k	3.9	~12.5	~16
J at V_{FB}-1 V	1×10^{-3} A/cm^2	~1×10^{-7} A/cm^2	~1×10^{-8} A/cm^2
E_{BD}	>10 MV/cm	~6 MV/cm	~7 MV/cm
ΔV_{FB}	-20 mV	-100 mV	-500 mV
Hysteresis	20 mV	120 mV	50 mV
D_{it} at midgap	5×10^{10} cm^{-2}eV^{-1}	6×10^{11} cm^{-2}eV^{-1}	1×10^{12} cm^{-2}eV^{-1}
Crystallization	>1100°C	~900°C	~900°C
Interface	SiO_x	Zr_xSi_yO	Zr-Si-O-N

CHAPTER V

ZIRCONIUM-DOPED TANTANUM OXIDE GATE DIELECTRICS: PROCESS WITH METAL NITRIDE GATE ELECTRODES

5.1 Introduction

The continued scaling of the channel length and gate oxide thickness of the complementary metal oxide semiconductor (CMOS) transistor has achieved higher performance and increased circuit density. However, it has reached a point where a number of obstacles have arisen. Potentially major issues include a high gate tunneling leakage current, polysilicon gate depletion, high gate resistance, boron penetration into the gate dielectric, polysilicon gate incompatibility with the high-k gate dielectrics, and reliability.[4,10,14,214,215]

In principle, many of these issues may be reduced or eliminated by replacing the poly-Si gate with a metal gate.[10] For example, with a poly-Si gate electrode, there are three components that are responsible for the capacitance equivalent thickness (CET) of the gate stack: (a) the contribution from the Si substrate due to quantum mechanical effect, (b) the dielectric layer itself, and (c) the carrier depletion layer in the poly-Si gate.[216] The replacement of the poly-Si gate with a metal gate could eliminate the poly depletion, and thus reduce the CET by 3-5 Å without a substantial increase in leakage current.[10] In addition, the gate resistivity can be reduced. Without the boron-doped poly-Si gate, the boron penetration problem does not exist.

It was reported that the electrical characteristics of the high-k gate dielectric film actually depend on the properties of the gate electrode material, such as work function and interface thermal stability.[101,217] Therefore, the requirements for a silicon compatible gate electrode are stringent. The work function of the gate material, defined as the energy needed to remove an electron from the Fermi level to the vacuum level, has to be within a certain range. For an NMOSFET, the metal gate needs a work function of 4.1-4.3 eV; for a PMOSFET, it needs to be 5.0-5.2 eV. In other words, both of the work functions need to be within ~0.2 eV from either the Si conduction or valence band edge in order to reduce the transistor's threshold voltage.[218] Other requirements of the gate electrode material include thermal stability for the gate dielectrics, ease of hydrogen diffusion for the dielectric interface passivation, and deposition method.[104,219]

The theoretical studies showed that the gate work function could vary significantly with the bulk metal's microstructure, the metal/dielectric interface chemistry, and even the underneath gate dielectric properties.[122,220-222] Mo was shown to be compatible with a dual-gate CMOS process.[220,222] The work function of Mo is between 4.1 and 4.6 eV.[122] It has also been proven to be compatible with some gate dielectrics such as SiO_2, Si_3N_4, ZrO_2, and $ZrSiO_4$.[122,220-222] Mo has a very low resistivity (5×10^{-6} Ω-cm) and high melting point (>2600°C). Best of all, it has been reported that its work function can be significantly reduced by a high-dose N implantation process.[220,222] MoN, WN, and TaN are good diffusion barriers for Cu as well as interconnect materials.[223-226] They have high conductivity, high thermal stability, and are resistant to impurity diffusion. They can be easily deposited by reactive sputtering.[224]

Matsuhashi and Nishikawa investigated the gate electrode effects of metal (Mo, W, Ti, and Ta) and their nitrides (MoN, WN, TiN, and TaN) on the leakage current of Ta_2O_5 film.[101] They proposed that Mo and MoN were the best choices for a high temperature process (>800°C). Although TiN has been reported to be an ideal gate electrode at a low temperature (<400°C), it is easily oxidized at a higher temperature, which degrades its resistivity. A thin capping layer, such as poly-Si, has to be deposited above it to prevent the oxidation.[97]

In this chapter, three different gate electrode materials, i.e., Mo, MoN, and WN, were extensively studied with the Zr-doped TaO_x films as the high-k gate dielectric layer.

5.2 Experimental Procedures of Gate Electrode

5.2.1 Gate Electrode Layer Deposition

Transition metal and their nitride gates, such as MoN and WN, are easily deposited with either PVD or CVD.[223,224] In this study, the metal and metal nitride gate electrodes were deposited by the RF sputtering on the 40 W Zr-doped TaO_x films. The 40 W Zr-doped TaO_x film was deposited using a Zr/Ta alloy target with the atomic ratio of Zr/(Ta+Zr) = 0.33. This was different from that in the two previous chapters, in which two separate metallic targets, i.e., Ta and Zr, were co-sputtered. The specific alloy target was chosen because the deposited film has a composition close to that of the film co-sputtered using Zr power of 40 W and Ta power of 100 W, which yielded the optimal dielectric properties as discussed in previous two chapters.

After the gate dielectric deposition, the sample was annealed in a 200 Torr O_2 ambient at 700°C for 10 minutes using an in-situ annealing chamber without breaking vacuum. The annealed sample was transferred back to the sputtering chamber for the gate electrode deposition. For the Mo metal gate, an approximately 600 nm-thick film was deposited in Ar at 5 mTorr. For the MoN and WN gate depositions, approximately 300 nm-thick films were deposited in a mixture of Ar/N_2, which will be discussed in the next section. After deposition, the gate was patterned with photolithography. The Mo gate was etched with a solution of $H_3PO_4 : HNO_3 : CH_3COOH : H_2O = 16 : 1 : 1 : 2$. The etch process was finished within 5 seconds. The photoresist was stripped with acetone and cleaned with isopropyl alcohol and DI water. The gate size was 10^{-6} to 10^{-3} cm^2. The MoN and WN gates were reactive ion etched (RIE) with a CF_4-containing chemistry.[227,228] In this study, the MoN gate layer was RIE etched at a rate of 800 Å/min using CF_4 gas at 70 mTorr and RF power of 500 W. The same recipe was also used to etch the WN gate layer with a higher etch rate of 1500 Å/min.

5.2.2 Nitrogen Content Effects on Nitride Properties

As for metal nitride gates, the adjustment of the N contents during sputtering was required to optimize the gate conductivity, work function, and film density.[102,220,222,228,229] Figure 71(a)-(c) shows the resistivities of various metal nitride gate electrode materials as a function of the sputtering gas composition, i.e., $N_2/(N_2+Ar)$.

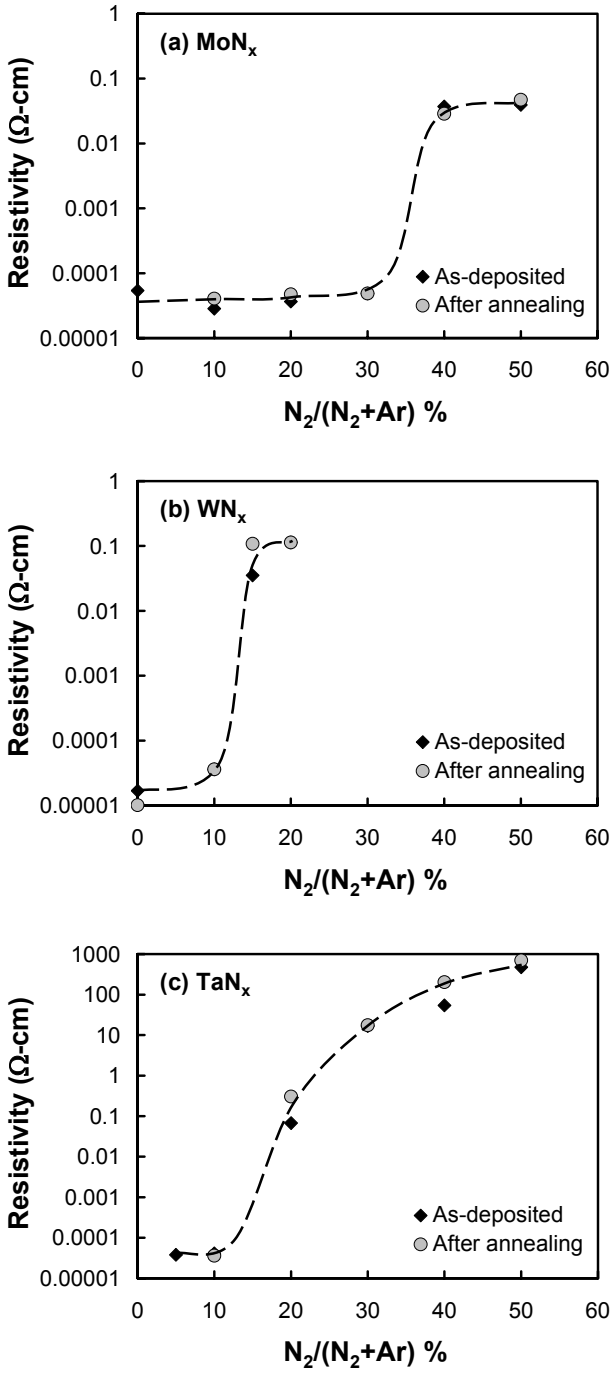


Figure 71. Resistivities of (a) MoN, (b) WN, and (c) TaN films as a function of $N_2/(N_2+Ar)$ during sputter-deposition. The post-deposition annealing was done at 400°C for 1 minute in a N_2 ambient (10 Torr).

The nitride film was deposited on a bare Si substrate without a high-k gate dielectric layer. The comparisons were made before and after a 400°C-N_2 annealing. However, this low temperature annealing seemed to have little influence on the measured resistivity.[229,230] On the other hand, the amount of N_2 introduced during the sputtering showed a strong influence, which agreed with the literature.[230] The post-metal thermal treatment in N_2 before the final forming gas annealing is a common practice for the PVD nitride gates, since the sputter-deposited nitride films are not dense enough.[29] For MoN, the resistivity was unchanged, i.e., $<10^{-4}$ Ω-cm, with the increase of the N_2 concentration up to 30%. For WN and TaN, however, the resistivity increased drastically when the N_2 percentage reached 10%.

Properties of the reactive sputtered MoN_x film with various N contents ($0 \leq x \leq 0.35$) were studied by Shen.[231,232] It was demonstrated that the most likely composition was Mo_2N. Once the Mo_2N phase was formed, the film properties, such as density, microstructure, and bonding feature, were independent of experimental conditions.[231,232] This is probably the reason why the resistivity of MoN in Fig. 71(a) was constant in the $N_2/(N_2+Ar)$ range of 10-30%.

The resistivity of the WN film is insensitive to the N content if it is amorphous, but the resistivity increases drastically with the N content when it is in crystal form.[226] The WN films in this study, either as-deposited or after annealing, are polycrystallized and their resistivities are dependent on the N concentration in the film. The resistivity of the WN film is also thickness-dependent, i.e., the thin film has a higher resistivity than the thick film.[226]

In Fig. 71(c), the resistivity of TaN increases quickly with the increase of the N content, which is similar to the WN case. Among these three materials, the MoN gate electrode deposition has a much wider process window.

Based on Fig. 71, we determined the optimal sputtering gas composition for these three nitride gate electrodes, i.e., 10% N_2 (90% Ar) for MoN, 2.5% N_2 for WN, and 5% N_2 for TaN, respectively. The nitride gate film thickness was fixed at about 250-300 nm. Figure 72 shows the resistivity of the gate electrodes on top of a 40 W Zr-doped TaO_x film. These metal nitride films on the dielectric layer showed much higher resistivities than those deposited on the Si substrate, i.e., 2×10^{-2} Ω-cm vs. 2×10^{-5} Ω-cm for MoN, 0.1 Ω-cm vs. 2×10^{-5} Ω-cm for WN, and 10 Ω-cm vs. 2×10^{-5} Ω-cm for TaN. It is possible that the nitride gate electrode reacted with the high-k dielectric film during deposition, which has been reported in the literature.[4] Among these three, the TaN gate had the highest resistivity, which was almost as large as that of the p-type Si substrate underneath, i.e., 10-80 Ω-cm. It was found that the capacitor with the TaN gate did not show good C-V characteristics, e.g., the accumulation capacitance did not saturate and the depletion region stretched out over a large range. Therefore, the TaN gate electrode effect was not studied in this dissertation.

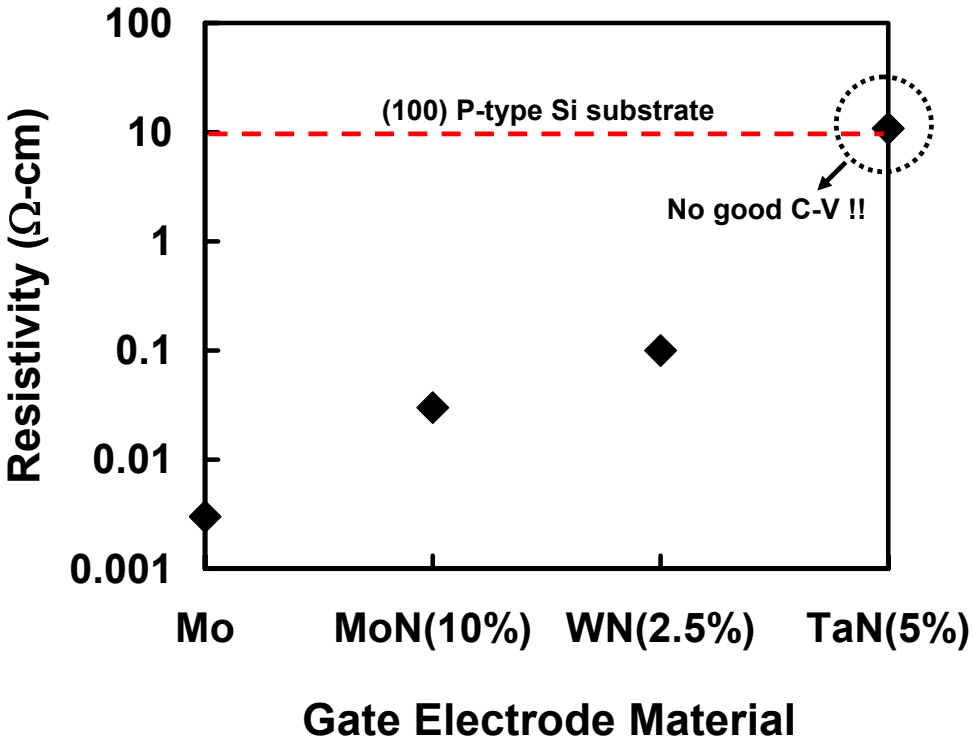


Figure 72. Resistivities of different gate electrodes on the Zr-doped TaO_x layers. The percentages in the parentheses were the N_2 concentrations during sputter-deposition.

5.2.3 Microstructures of Gate Electrodes

The microstructures of the nitride gate electrodes were investigated by XRD to test their thermal stability. Figure 73(a)-(c) show the XRD patterns of the Mo, MoN, and WN films. All films were deposited on a 10 nm-thick Zr-doped TaO_x film and annealed at 400°C in forming gas (10% H_2 + 90% N_2 at 200 Torr). Crystalline phases were observed in all samples. In Fig. 73(a), the Mo film shows a body-centered cubic (bcc) structure with a (110) orientation, which is consistent with the literature.[102,222,233] This (110) texture has a columnar structure perpendicular to the film surface.[102] Mo with the columnar structure has a p-type gate work function of ~5 eV, which was confirmed by our result in a later section.[122,222,234] It was also reported that N atoms could be implanted into the Mo gate to modify its work function from a p-type gate (~5.0 eV) to an n-type gate (~4.4 eV). This adjustment of the Mo work function is dependent on the N concentration, implant power, and annealing condition.[102,220,222] However, the XRD of the N-implanted Mo film was very similar to that of the un-implanted Mo film due to the negligible amount of N ($<1\times10^{16}$ cm^{-3}) in the film. In our case, the MoN film has a very different XRD pattern from the Mo film, e.g., Fig. 73(b) vs. 73(a).

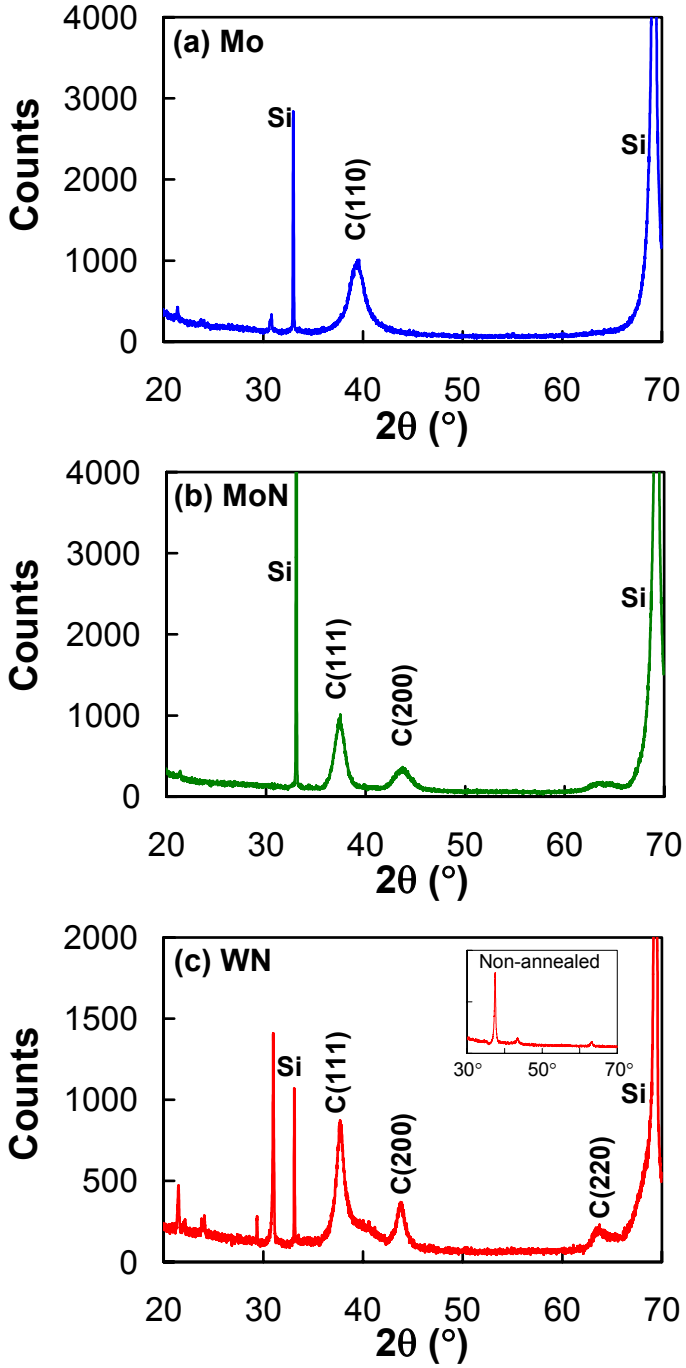


Figure 73. XRD patterns of (a) Mo, (b) MoN, and (c) WN films on the 10 nm Zr-doped TaO_x films after a 400°C forming gas annealing. The inset of (c) shows the XRD pattern of a non-annealed WN film.

In Fig. 73(b), the MoN film shows a face-centered cubic (fcc) structure with (111) and (200) orientations, which correspond to the Mo_2N structure.[231,232] The reactively sputter-deposited MoN film in an Ar/N_2 ambient was reported to have a high stress, with its polarity, i.e., tensile or compressive, depending on the sputtering pressure.[228,231,232] In the low pressure range of 2-6 mTorr, the deposited MoN film has a high compressive stress (up to 1.38 GPa). When the pressure is increased, the stress changed from compressive to tensile (up to 1.42 Gpa). Above 12 mTorr, the film stress starts to decrease again and a minimum stress occurs at the pressure around 40 mTorr.[232] This film stress is related to its microstructure.[232] For example, the compressive MoN film has a dense non-columnar microstructure, while the tensile film shows a columnar microstructure. Since the MoN sputtering pressure in this study was 5 mTorr, it should have a high compressive stress and a dense non-columnar microstructure. This high stress had been suspected to cause an adhesion problem with the underneath high-k film, which was observed during the patterning step. A post-metal annealing at 400°C for 1 minute in the N_2 ambient was used to improve the adhesion, which was proven successful in our case. Introducing a small amount of O_2 during the sputtering was reported to help releasing the stress due to the reduction of the lattice parameters and amorphisizing the film. However, the film's conductivity was degraded by the introduction of oxygen.[231]

The WN film also showed a cubic structure with (111), (200), and (220) orientations, which agreed with the literature.[223] It was also reported that WN could be deposited as an amorphous-like film by PECVD if an appropriate W/N ratio was

obtained, i.e., 2-19.[226] However in this study, the as-deposited WN film was crystallized with a cubic structure, as shown in the inset of Fig. 73(c). This phenomenon could be explained by the high ion bombardment energy in the sputtering process, which enhanced the diffusion of atoms and the crystalline phase formation. In Fig. 73(c), the XRD peaks of (111), (200), and (220) suggested that the deposited film has a stoichiometric W_2N structure.[226] Since no metallic W peaks were observed, e.g., at 2θ = 40° and 58°, the film was fully nitridized.

5.3 Electrical Properties of Zr-Doped TaO_x with Metal Nitride Gate Electrodes

5.3.1 Influence of Gate Electrode on EOT

Figure 74 shows the correlation between the sputter-deposition time of the Zr-doped TaO_x film and the calculated EOT with Mo, MoN, and WN gate electrodes. Three samples with the 700°C-thermally grown SiO_2 gate oxide fabricated with dry O_2 at 200 Torr, which used different gate electrode materials respectively, are also shown in the figure for comparison. Their thicknesses are about 3 nm, as indicated at deposition time of zero in the figure. Even though the physical thicknesses of the high-k layers were the same, the gate electrode has obvious effects on the EOT value. In the figure, the MoN gate resulted in the largest EOT while the Mo gate showed the smallest EOT. This might be attributed to the higher gate resistivity and the interface reaction.[216]

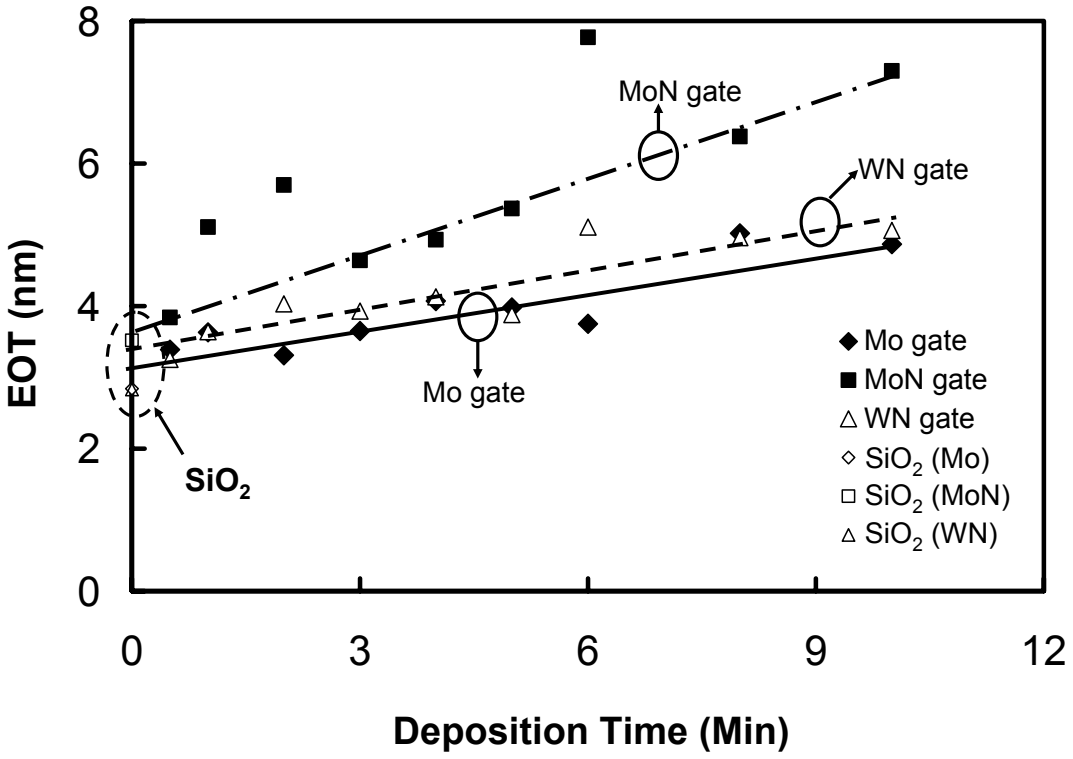


Figure 74. EOTs of the Zr-doped TaO_x films as a function of sputter-deposition time and gate electrode material. EOTs of the 700°C-thermally grown SiO_2 are also shown.

5.3.2 Influence of Gate Electrode on Current Density

Figure 75 shows the current density of the Zr-doped TaO_x film as a function of the EOT. Different gate materials, i.e., Mo, MoN, and WN, were used to fabricate these capacitors. The current was measured at 1 V away from the flatband voltage (V_{FB}), i.e., (a) V_{FB}-1 V for accumulation, or (b) V_{FB}+1 V for inversion. The post-metal annealing step was performed at 400°C for 30 minutes in a forming gas ambient (10% H_2 + 90% N_2) after the gate patterning was finished. In this study, the thermal SiO_2 film was grown at 700°C under dry O_2 ambient (200 Torr). The current densities of these SiO_2 capacitors with Mo, MoN, and WN gate electrodes are shown in the figure. In addition, the current densities of thermally grown SiO_2 films with $POCl_3$-doped poly-Si gates were taken from literature and shown in the figure for comparison.[94,235,236] For both (a) gate injection and (b) substrate injection in Fig. 75, the Zr-doped TaO_x film showed a much lower current density than the SiO_2 films, either grown in this experiment or from the literature, with the same EOT. The current density is dependent on the gate electrode material. For example, while the WN gate capacitor of the Zr-doped TaO_x film has a current density about two orders of magnitude lower than that of the SiO_2 film from the literature, the MoN gate capacitor has a current density about one order of magnitude lower than that of SiO_2. The SiO_2 films with metal and nitride gates have lower current densities than that with the poly-Si gate, which is due to the elimination of poly-depletion effect.[216] The current density of the Mo gate capacitor with the same EOT is between those of MoN and WN gate capacitors.

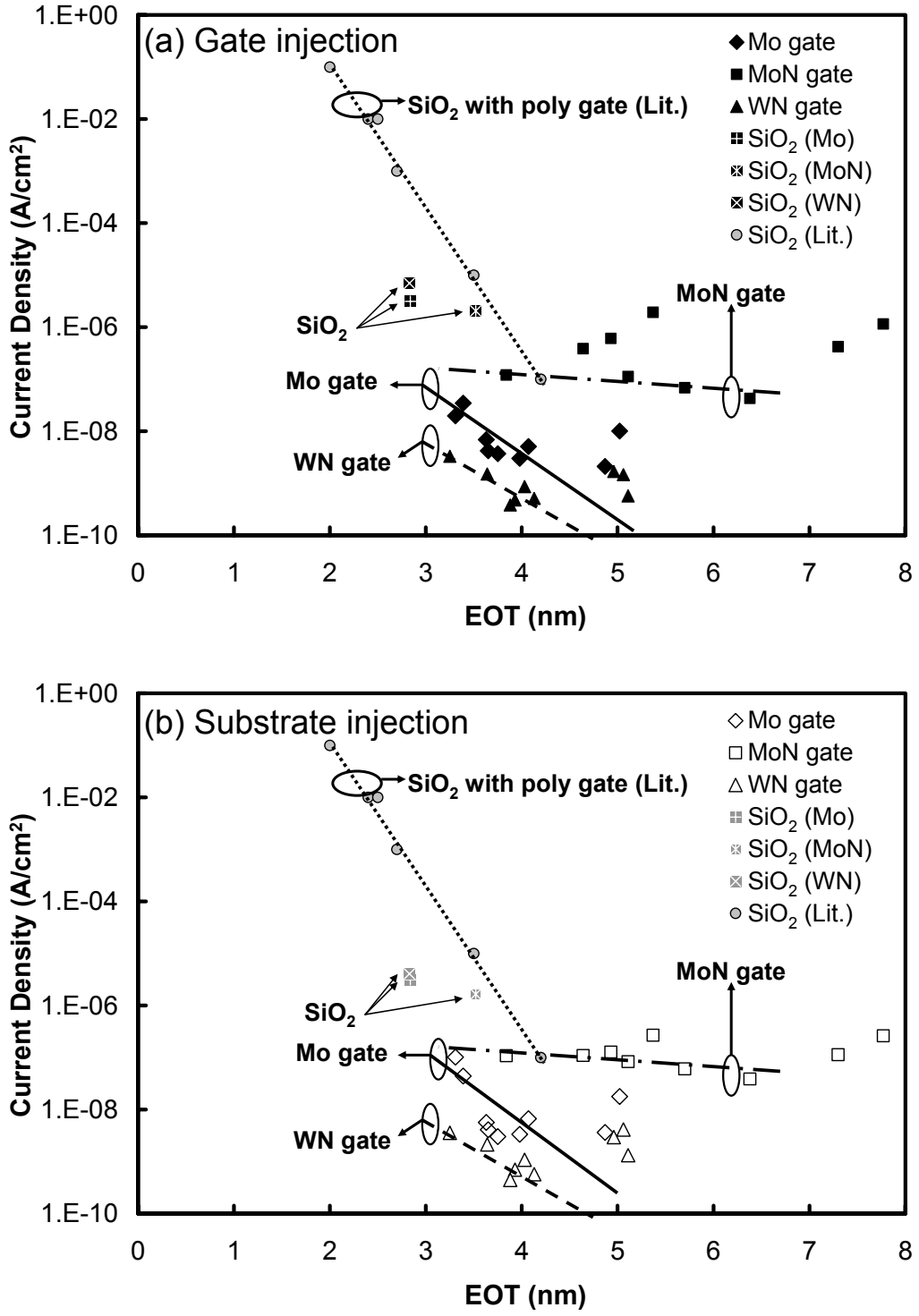


Figure 75. Current densities at (a) V_{FB}-1 V and (b) V_{FB}+1 V of the 40 W Zr-doped TaO_x films with different gate electrode materials. Current densities of SiO_2 are also shown.

The variation of current density with the gate material indicates an electrode-limited conduction mechanism, i.e., Schottky emission.[45,46] The order of the current density with different gate electrodes could be related to the order of the conduction band barrier height. For example, the current densities in Fig. 75(a) and (b) are in the order of MoN > Mo > WN, which indicates the order of the gate/Zr-doped TaO_x barrier height (Φ_{Be}) as WN > Mo > MoN. The barrier height is related to the electrode work function, i.e., $\Phi_{Be} = \Phi_m - \chi_{high\text{-}k}$, where $\chi_{high\text{-}k}$ is the electron affinity of the high-k layer, as shown in Fig. 52. Therefore, the work function should follow the same order as that of the barrier height, i.e., WN > Mo > MoN. In a later section, we will show that the work function extracted from the flatband voltage actually has the order of Mo > MoN > WN. Therefore, Schottky emission may not be the only dominant conduction mechanism.[46] Since switching the gate bias polarity did not affect the current density significantly, as shown in Fig. 75(a) and (b), the current conduction might be bulk-limited, e.g., Poole-Frenkel mechanism.[237]

Matsuhashi et al. deposited different gate electrode materials on the CVD Ta_2O_5 gate dielectric and studied the electrical characteristics.[101] They found out that not only the gate electrode, but also the annealing temperature, influenced the device leakage current. For example, the leakage current of the Ta_2O_5 film with different gates was in the order of TaN > MoN > WN > TiN before annealing; however, the order changed to TaN > WN > MoN > TiN after a 400°C-N_2 annealing and TaN > TiN > WN > MoN after an 800°C-N_2 annealing.[101] The TiN gate was seriously degraded above 400°C, but the MoN gate performance was improved after a high temperature annealing step.

Therefore, the thermal stability of the gate electrode is a concern. The order of the current density in their study is different from our results. There are several possible explanations. The gate dielectric films are different, i.e., the Zr-doped TaO_x film vs. the CVD Ta_2O_5 film. The interaction between the gate dielectric and the gate electrode are different, which would change the current conduction mechanism. In addition, Matsuhashi et al.[101] attributed the current dependence of the gate electrode to the gate work function, i.e., a Schottky conduction current. This is different from our observation.

In Fig. 75(a) and (b), capacitors with the WN gate show much lower leakage currents than capacitors with other gate materials, which is similar to the result on the Ta_2O_5 gate dielectric film reported by Lee et al.[238] The deposition method for the same gate electrode material also affects the leakage current. For example, with the same SiO_2 dielectric layer, the TiN gate electrode deposited by the atomic layer deposition (ALD) method has a lower leakage current than that deposited by the sputtering method.[239] The plasma-free ALD process induced much less damages than the sputtering process.[8]

It was reported that the Mo gate capacitors with 30-60 nm-thick MOCVD ZrO_2 dielectric layers had similar dielectric constants as the Al gate capacitors with the same ZrO_2 dielectric layers; however, the energy loss, i.e., loss tangent, of the former is about one order of magnitude higher than the latter.[4,240] The former also has a slightly higher leakage current and lower dielectric breakdown strength than the latter. The reaction between Mo and the high-k dielectric layer, for example, the formation of a MoO or a MoON interface, could be responsible for the change of conduction mechanism and the increase of leakage current.[4,240]

5.3.3 Influence of Gate Electrode on Breakdown Strength

Figure 76(a) and (b) show the breakdown voltages and breakdown fields of the Zr-doped TaO_x films with various electrode materials. The EOT was used instead of physical thickness for the electric field calculation at the breakdown. For all of the gate electrodes, the breakdown voltage monotonically decreases with the decrease of the EOT, while the breakdown electric field is almost constant. The Mo gate has slightly higher dielectric breakdown strength than the WN or MoN gates. The SiO_2 film with the same gate electrode showed a slightly lower breakdown strength than the Zr-doped TaO_x film, possibly because SiO_2 was formed at a low temperature of 700°C.[7] The dependence of the breakdown strength on the EOT is inconsistent with the literature reports. It is strongly dependent on the fabrication method of the gate dielectric layer.[45,241] For example in Fig. 76(b), the breakdown field with the MoN gate increases slightly with the decrease of EOT, but the opposite result occurs with the Mo gate. The dielectric breakdown only occurred in the accumulation region, i.e., gate injection, in this study. No breakdown in the inversion region was observed possibly due to the large band bending of the Si deletion region, which reduced the electric stress in the gate dielectric layer.[3] In the meantime, the lack of the conducted electrons due to the insufficient carrier generation resulted in a reduced kinetic bombardment at the interface, which was discussed in Chapter III.[181-183] These effects suppress the dielectric breakdown process in the inversion region.

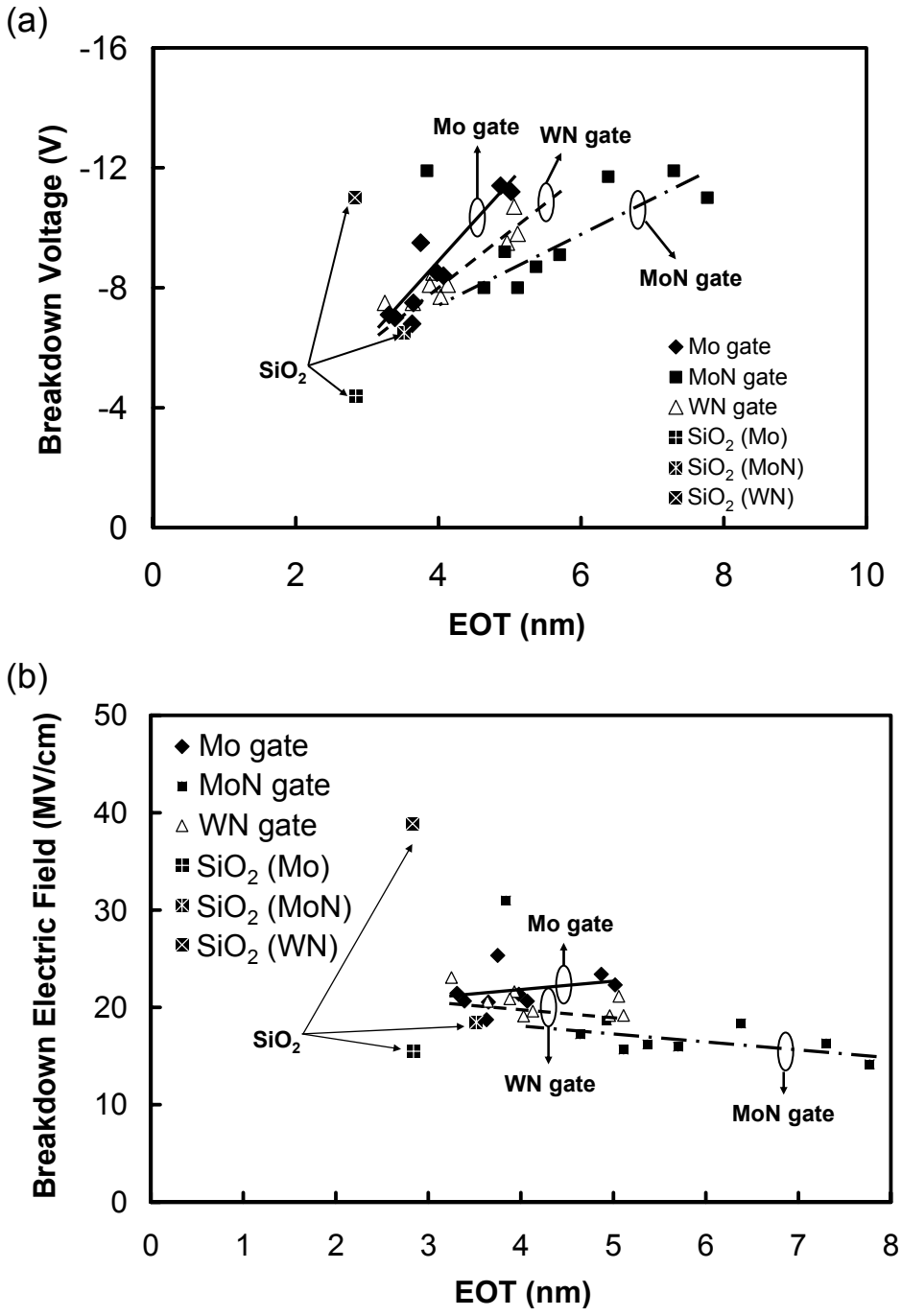


Figure 76. (a) Breakdown voltage and (b) breakdown electric field of the Zr-doped TaO_x films with various gate electrode materials and EOTs. The 700°C-thermally grown SiO_2 are also shown for comparison.

5.3.4 Influence of Gate Electrode on Flatband Voltage

Figure 77 shows the flatband voltage (V_{FB}) of the Zr-doped TaO_x dielectric layer as a function of the gate electrode material. The V_{FB} decreases with the reduction of the EOT, which is consistent with literature reports.[108] This can be explained by the fixed charge concentration close to the high-k dielectric/Si interface. The relation between charge density Q_f and the flatband shift (ΔV_{FB}) was,[3]

$$V_{FB} - (\Phi_m - \Phi_{Si}) = \Delta V_{FB} = -\frac{Q_f}{C_{ox}'} = -\frac{Q_f(EOT)}{\varepsilon_0(3.9)} \quad [62]$$

where Φ_m is the gate electrode's work function, Φ_{Si} is the Si substrate's work function, and ε_0 is the vacuum permittivity (8.85×10^{-14} F/cm). This expression is based on two assumptions: (i) the fixed charges are the only defects responsible for the flatband shift, and (ii) the fixed charge density Q_f remains constant when the film thickness or EOT varies. With Eq. 62, the intercept of the V_{FB} line at EOT = 0 is the ideal flatband voltage (V_{FB}^0), which is the work function difference between the gate electrode and the Si substrate.[108] However, Eq. 62 is not exactly applicable to the high-k gate dielectric that has a large density of oxide trapped charges, which are distributed across the whole high-k film. These defects contribute to the flatband voltage shift.[8] It was predicted that the equation of the flatband shift with the charge density should be in the quadratic form instead of the linear form.[3] In this study, only the simple linear model as shown in Eq. 62 was used for the convenience.

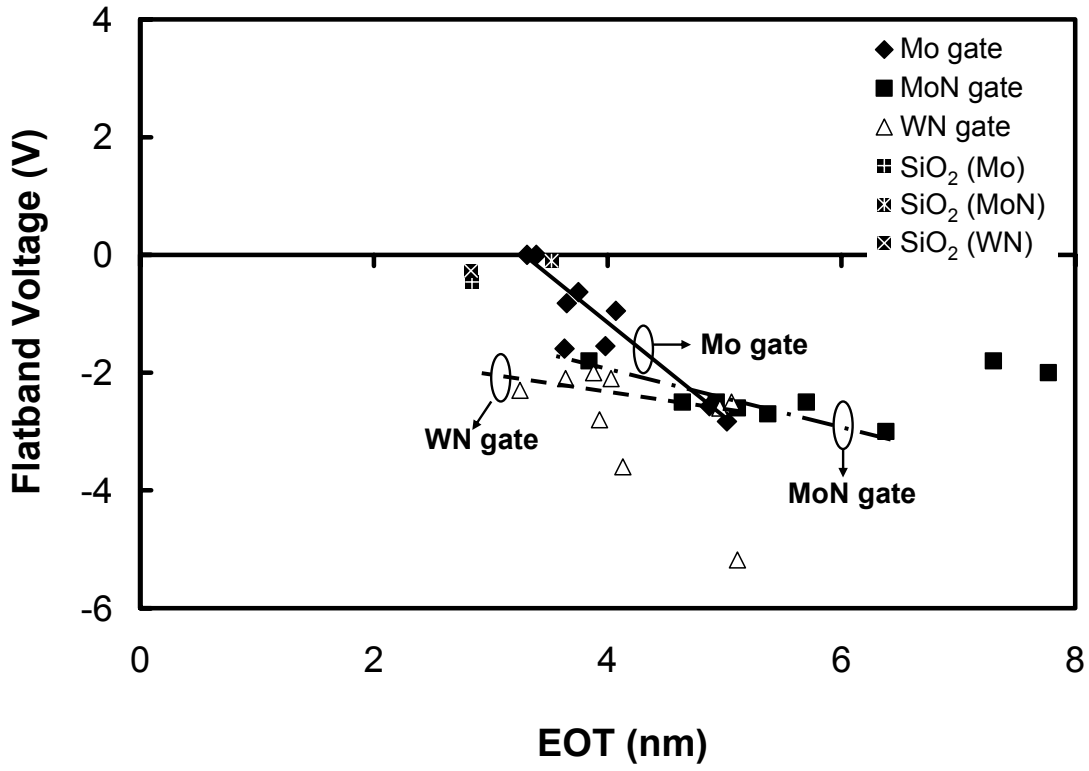


Figure 77. Flatband voltages of the Zr-doped TaO_x films with different gate electrode materials. The values of 700°C-thermally grown SiO_2 films are shown for comparison.

Based on the trend in Fig. 77, the order of the work function is Mo > MoN > WN. For comparison, Table V shows the gate work functions reported by Matsuhashi et al. with Ta_2O_5 as the gate dielectric layer.[101] These values were measured after different post-gate annealing temperatures in N_2, i.e., 400°C and 800°C. The annealing time was 30 minutes. The values of gate work function are strongly dependent on the annealing temperature, i.e., MoN (5.33 eV) > Mo (4.64 eV) without annealing, MoN (4.89 eV) > Mo (4.78 eV) after 400°C annealing, and Mo (4.94 eV) > MoN (4.70 eV) after 800°C annealing. It was also reported that Mo has a p-type metal gate work function of ~5 eV when it is on a thermally grown SiO_2.[218] However, when N atoms were ion-implanted into the Mo gate to form MoN_x, its work function changes to an n-type metal gate.[220-222] In other words, the work function of Mo is larger than MoN_x on the thermal SiO_2. This is inconsistent with Matsuhashi's result in Table V, but consistent with our result in Fig. 77. Therefore, it is possible that the work function of a gate electrode could be altered not only by the fabrication process, e.g., annealing temperature, sputtering, and ion implantation, but also by the adjacent gate dielectric material, e.g., Ta_2O_5, SiO_2, and Zr-doped TaO_x. For example, the Mo gate has a work function of 5.05 eV on SiO_2, 4.94 eV on ZrO_2, 4.79 eV on $ZrSiO_4$, and 4.76 eV on Si_3N_4.[122] In Fig. 77, the same gate electrode shows different V_{FB} values with the SiO_2 dielectric or with the Zr-doped TaO_x dielectric even with the same EOT. This is attributed to different gate work functions and/or fixed charge densities associated with different gate dielectric materials.[108] In addition, Fig. 77 shows that the work functions of Mo, MoN, and WN are 4.45 eV, 4.81 eV, and 4.64 eV, respectively, on the SiO_2 films by assuming a negligible fixed charge density in Eq. 62.

These samples were annealed at 400°C for 30 minutes in forming gas (10% H_2 + 90% N_2) after gate deposition. These values of work function are consistent with the ones that were after a 30 minute, 400°C-N_2 post-metal annealing, i.e., 4.78 eV, 4.89 eV, and 4.76 eV, in Table V.[101]

Table V. Work functions of different gate electrode materials on top of Ta_2O_5.[101]

Electrode Materials	Work Function Φ_m (eV)		
	As-deposited	400°C-N_2 annealing	800°C-N_2 annealing
Mo	4.64	4.78	4.94
MoN	5.33	4.89	4.70
W	4.75	4.74	4.77
WN	5.00	4.76	4.83
Ti	4.17	3.91	—
TiN	4.95	4.80	4.81
Ta	4.25	4.33	4.72
TaN	5.41	4.55	—

5.3.5 Influence of Gate Electrode on Defect Density

Hysteresis

Figure 78 shows the hysteresis values of the Zr-doped TaO_x films. With different gate materials, the hysteresis shows different trends. For example, the WN gate has a counterclockwise hysteresis, while the Mo and MoN gates have a clockwise hysteresis. When the EOT is decreased, the hysteresis with the WN gate is increased up to ~50 mV and stabilized, but those with the Mo and MoN gates are actually decreased.

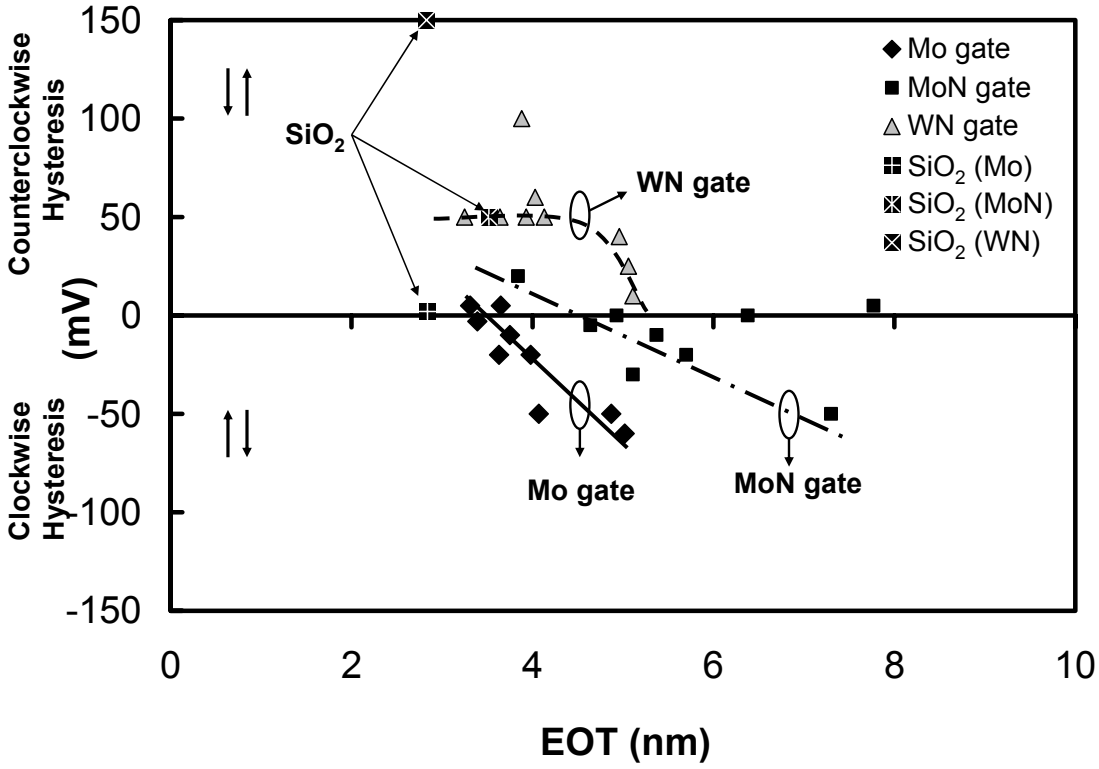


Figure 78. Hysteresis of the Zr-doped TaO_x films with different gate electrode materials. The 700°C-thermally grown SiO_2 films are shown for comparison.

The decrease of hysteresis with the reduction of the EOT, e.g., in the Mo and MoN gates, could be explained by an interface layer model.[242] As the gate voltage is swept, the injected carriers (electrons or holes) are trapped inside a thin interface layer between the high-k dielectric film and the Si substrate. This thin interface layer in this case could be either a SiO_x or Zr_xSi_yO layer, as discussed in Chapter III. We can assume that this trapping interface layer has a fixed thickness. When the total film thickness, i.e., bulk + interface, is increased, the relative distance of this interface as compared to the total dielectric thickness, i.e., interface / (bulk + interface), becomes closer to the Si substrate, which results in a larger hysteresis of the C-V curve.[242] As for the WN gate electrode, on the other hand, the decrease of EOT does not reduce the hysteresis. It is possible that the traps are located close to the WN gate. By increasing the film thickness, the influence of these traps near the gate is minimized. Therefore, the hysteresis value is reduced, as shown in Fig. 78.

The counterclockwise hysteresis observed in the WN gate capacitors indicates the existence of electron traps. The clockwise hysteresis shown by the Mo and MoN gates might be from mobile charge-type defects.[108] It is possible that Mo ions might easily diffuse into the high-k gate dielectric and move around under a electric field.[243]

Interface state density

The gate electrode material and the deposition technique are known to affect the interface state density of SiO_2 and high-k gate dielectrics on an MOS structure.[229,239] For example, a TiN gate electrode fabricated by atomic layer deposition (ALD) resulted in a

lower D_{it} on SiO_2 than that deposited by sputtering.[239] Figure 79 shows the interface state density (D_{it}) of the Zr-doped TaO_x films with different gate electrode materials. The conductance method was used for the D_{it} extraction, as discussed in Chapter II.[126] For comparison purposes, the interface state density of the 700°C-thermally grown SiO_2 films with the same gate electrodes are also shown. The three SiO_2 samples show the lowest D_{it} regardless of the gate electrode materials.[7] All of the Zr-doped TaO_x samples have D_{it} between 1×10^{12} and 6×10^{12} $cm^{-2}eV^{-1}$. The WN gate had the highest D_{it}, while the MoN gate had the lowest. As the EOT is decreased, the D_{it} value increases slightly. The gate electrode is closer to the high-k/Si interface when the thickness is decreased. Therefore, the gate has stronger influence on the interface states. The D_{it} values extracted from the Mo gate are between those of the WN and MoN gates. It was reported that a PVD process, such as sputtering, resulted in a larger interface state density because of the plasma damage, which could not be completely repaired by a high temperature forming gas annealing.[244] It is also possible that the metal atoms in the gate electrode penetrate into the high-k/Si interface and raise the D_{it}.[243,244]

The conductance method could also offer information about the interface trap time constant.[126] The time constant is inversely proportional to the capture cross section of the defect. According to the interface trap time constant within the Si bandgap, the dominant interface states in the high-k gate dielectric film are similar to SiO_2, which indicates that a SiO_x-like interface layer is formed between the high-k dielectric film and the Si substrate.[125]

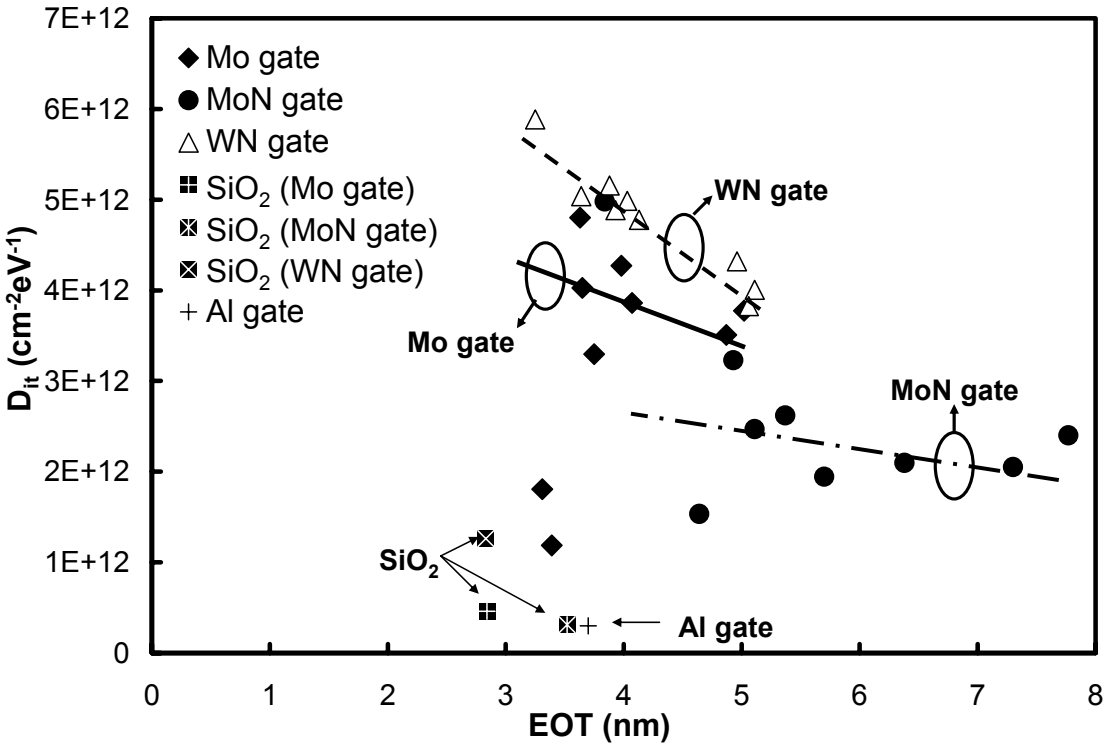


Figure 79. Interface state density (D_{it}) of the 40 W Zr-doped TaO_x films with different gate electrode materials.

The Zr-doped TaO_x sample with the Al gate electrode has the lowest D_{it} in comparison with those with the other gate materials. It is possible that the Al gate deposition process induced a very small number of defects to the high-k dielectric/Si interface. Another possibility is that the post-metal forming gas annealing is more

effective with the Al gate. For example, it was reported that the atomic hydrogen (H), which was generated by the reaction between Al and the moisture, was actually responsible for the dangling bond passivation at the interface.[16,245] This H-generation reaction also produced a very thin layer of Al_2O_3 as the by-product. This statement has been supported by the fact that the same forming gas annealing was ineffective for the D_{it} reduction on a nonreactive metal gate such as Au.[16] In addition, when a Si_3N_4 layer was present to block the atomic H diffusion, no obvious reduction of D_{it} was observed.[245]

Frequency dispersion

The gate electrode has a strong influence on the C-V frequency dispersion, as shown in Figure 80 with (a) Mo, (b) MoN, and (c) WN gates. All samples had EOT ~3.5 nm. The frequency dispersion in the accumulation region is due to the extrinsic factors other than the dielectric layer property. For example, the series resistance resulted from the gate resistivity and the Si doping concentration could seriously degrade the accumulation capacitance at a high frequency. However, the degradation is reduced at a low frequency. This difference in frequency causes a vertical shift along the capacitance axis, which is especially obvious in the accumulation region because of its larger capacitance value. Fortunately, this extrinsic effect could be corrected by many methods.[8,210-212] This accumulation frequency dispersion is also affected by the MOS gate area, which is another extrinsic factor. As long as the accumulation capacitance is saturated, we could ignore this effect.

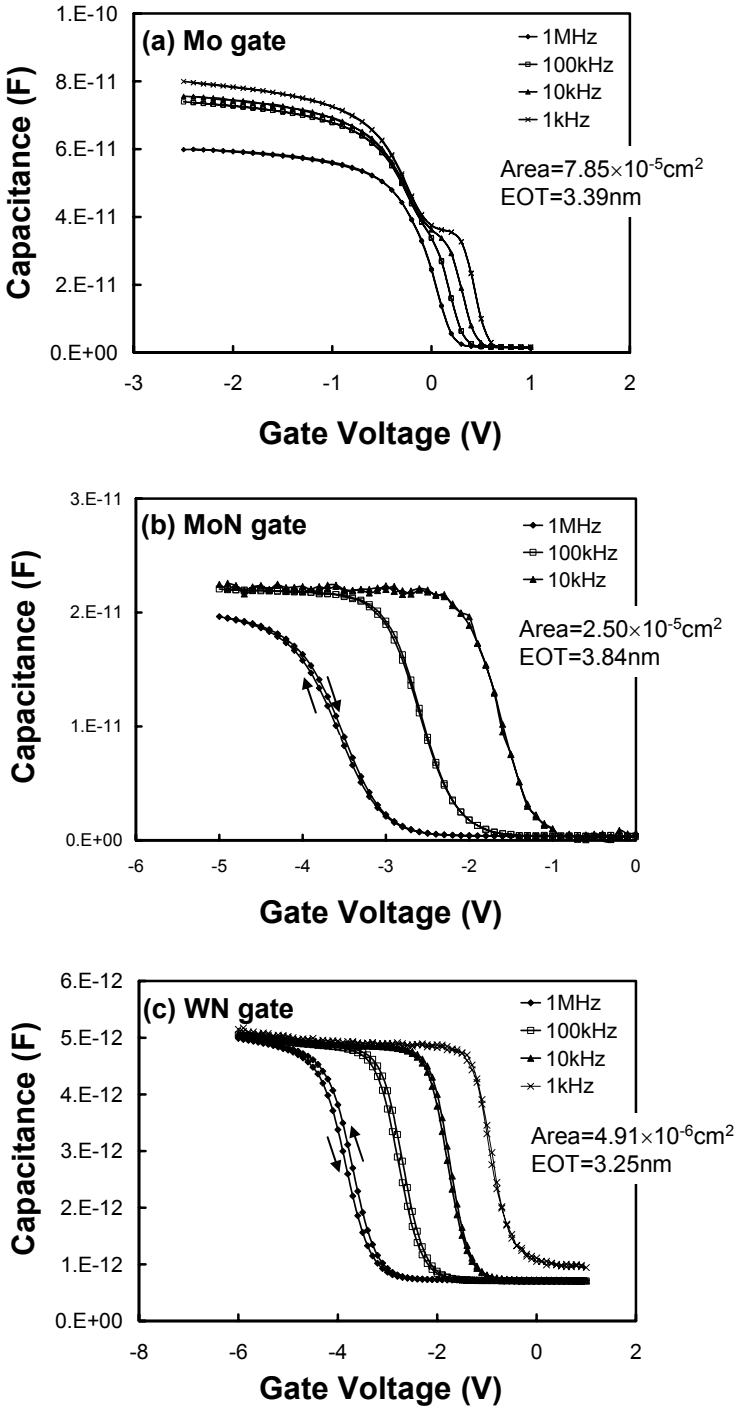


Figure 80. C-V curves of the 40 W Zr-doped TaO_x films with (a) Mo, (b) MoN, and (c) WN gate electrodes. Frequency dispersion is observed.

Frequency dispersion in the depletion region, however, is due to the existence of the interface states, which has been discussed in detail in Chapter II.[8] In Fig. 80(a)-(c), the Mo gate shows the smallest frequency dispersion in the inversion region, and the MoN gate shows the largest. Figure 81 shows the C-V curve of the Zr-doped TaO_x film with an Al gate, which showed the smallest frequency dispersion in the depletion region compared with the Mo, MoN, and WN gates.

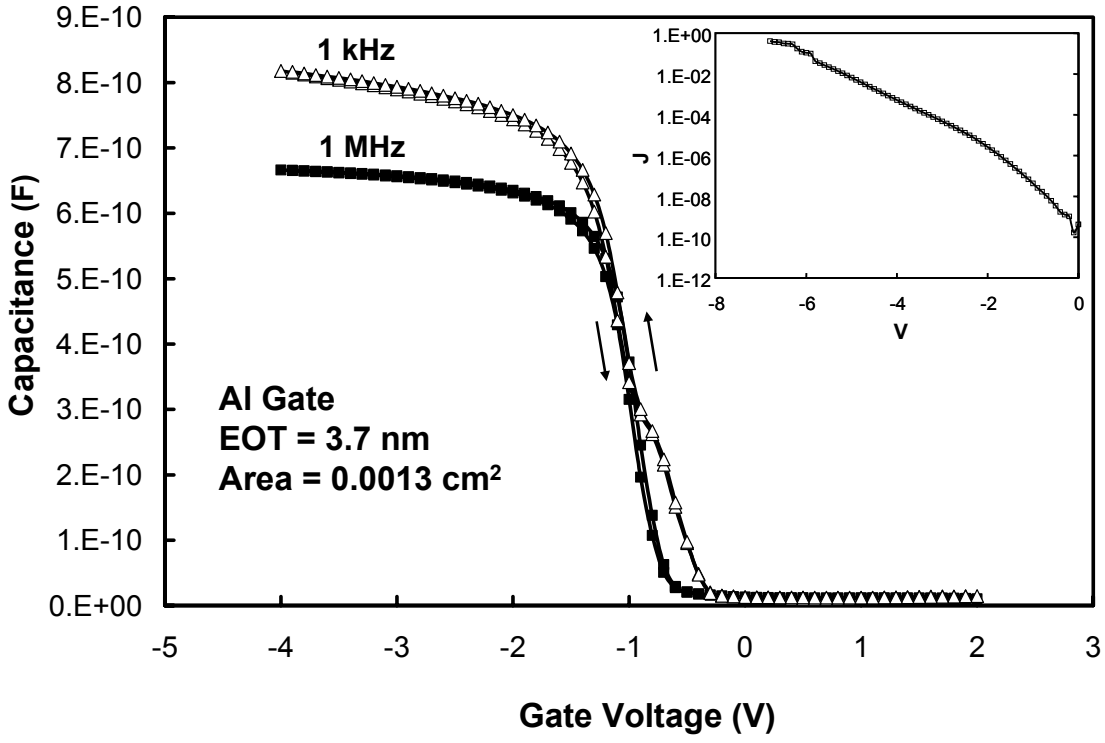


Figure 81. C-V curves of the Al gate capacitor with a 40 W Zr-doped TaO_x film (EOT = 3.7 nm). The inset shows the I-V curve in accumulation (gate injection).

Figure 82 shows the C-V curves of the 700°C thermally grown SiO_2 films with (a) Mo, (b) MoN, and (c) WN gate electrodes. Compared with the Zr-doped TaO_x film in Fig. 80(a)-(c), the SiO_2 film shows much smaller frequency dispersion in the depletion region, indicating a much lower interface state density. Figure 83 shows the frequency dispersion of the Zr-doped TaO_x films as a function of the EOT with different gate electrode materials. In general, the Mo gate has the smallest frequency dispersion, while the MoN gate has the largest dispersion. Fig. 79 shows that the interface state density with different gates has an order of WN > Mo > MoN, which is obviously different from the results of frequency dispersion. Therefore, there must have been reasons other than interface states that caused this large frequency dispersion.[8] Extensive work has to be done in the future to answer this question.

There is a possible explanation for the higher frequency dispersion with MoN and WN gates. The MoN and WN gates were etched by RIE, while the Mo gate was etched by a wet solution. It is known that the plasma damage of RIE could induce more defects in the bulk film and the interface. If these damages are not removed by the post-metal annealing step, it might result in the unusually large frequency dispersion in the MoN and WN gates.[245]

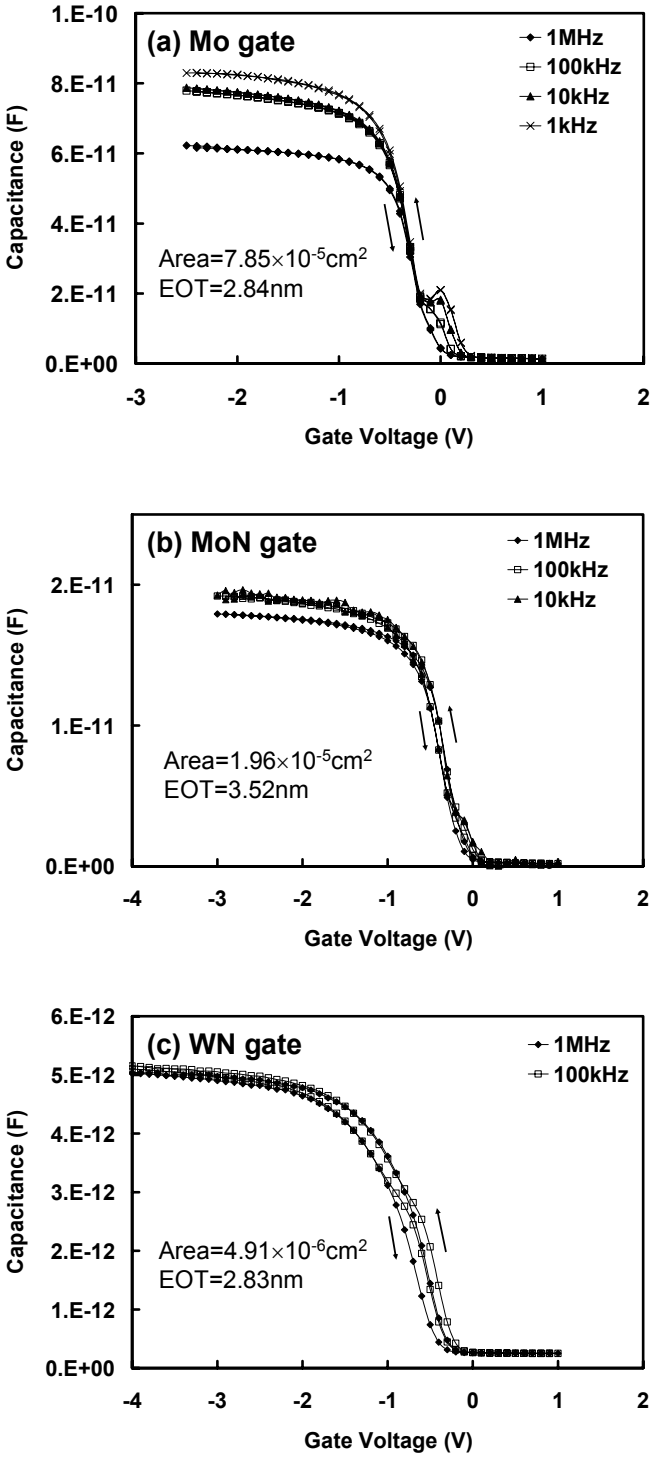


Figure 82. C-V curves of the 700°C-thermally grown SiO_2 with (a) Mo, (b) MoN, and (c) WN gate electrodes.

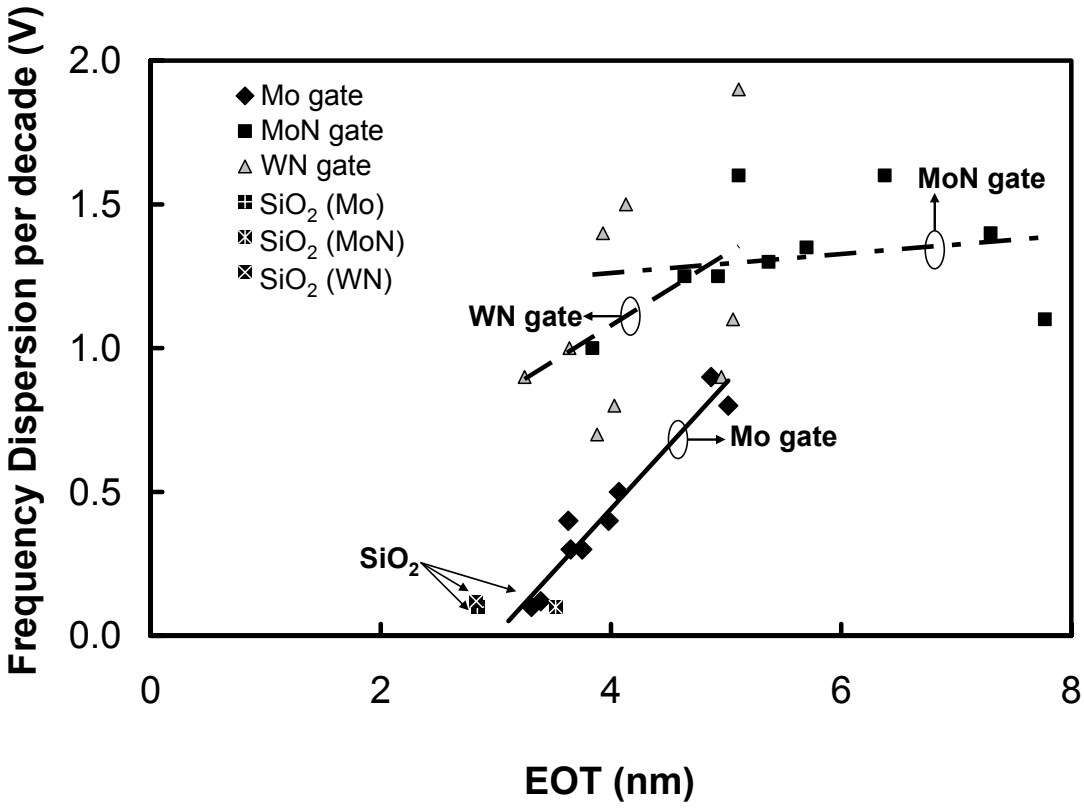


Figure 83. Frequency dispersion of the Zr-doped TaO_x films with different gate electrode materials. The 700°C-thermally grown SiO_2 films are also shown for comparison.

5.4 Summary

This chapter discussed the gate electrode compatibility with the Zr-doped TaO_x gate dielectrics. First, the depositions of the metal nitride gate, i.e., MoN, and WN, were optimized by adjusting the $N_2/(N_2+Ar)$ ratio during reactive sputtering. By measuring the film resistivity, it was found that the optimal $N_2/(N_2+Ar)$ ratios for MoN and WN were 10% and 2.5%, respectively. Secondly, the microstructures of all three gates, i.e., Mo, MoN, and WN, were investigated by the XRD. It was found that the as-deposited films were already highly crystallized. The 400°C-N_2 annealing step increased the crystallinity without changing the crystal structure. The Mo film showed a cubic phase with the orientation of (110). The MoN film had cubic (111) and (200), while the WN film had cubic (111), (200), and (220).

The electrical characterizations of the Zr-doped TaO_x film with these three gates were analyzed. The measured MOS capacitor properties were EOT, current density, breakdown strength, flatband voltage, work function, hysteresis, interface state density, and frequency dispersion. Compared to the dielectric characteristics with an Al gate, the most significant difference when using these three gates, i.e., Mo, MoN, or WN, was the large frequency dispersions, as shown in Figs. 80 and 81. Other than that, good electrical properties were obtained. Therefore, the Zr-doped TaO_x film is a possible candidate for the high-k gate dielectric applications when a proper metal or metal nitride gate electrode is used.

CHAPTER VI

SUMMARY AND CONCLUSIONS

A novel high-k gate dielectric material, i.e., zirconium-doped tantalum oxide (Zr-doped TaO_x), has been thoroughly studied for future MOSFET applications. Extensive studies on the fabrication process and device characteristics have been accomplished. Promising results were obtained. This dissertation was arranged in the following way. The first and second chapters (Chapter I & II) included background knowledge of high-k gate dielectrics and detailed fabrication processes and characterization techniques. The third chapter (Chapter III) was for the study of the structural and electrical properties of the Zr-doped TaO_x films. The fourth chapter (Chapter IV) was focused on the device characteristics of the Zr-doped TaO_x film with an inserted thin TaN_x interface layer. Finally, the fifth chapter (Chapter V) included the characteristics of capacitors composed of the Zr-doped TaO_x film and various metal and metal nitride gate materials.

In Chapter I, one of the most urgent problems confronted by the semiconductor industry, i.e., the silicon dioxide (SiO_2) scaling for MOSFET, was discussed. A potential solution to this problem was to replace SiO_2 with a high-k dielectric material for many practical benefits. There are many requirements that need to be satisfied before the new material is acceptable in industry. For example, new high-k gate dielectrics require thermodynamic stability when in contact with Si, a high amorphous-to-transition temperature, a large electrical bandgap, and a large energy band barrier with Si. A

doping technique, i.e., adding Zr into TaO_x, was proposed to improve the material and electrical properties.

In Chapter II, the fabrication methods, characterization techniques, and corresponding working theories were presented in detail. The first part of the chapter introduced the deposition process of the Zr-doped TaO_x films. The Zr dopant was introduced into the TaO_x film by a reactive co-sputtering method using two metallic targets, i.e., Ta and Zr. The pre-deposition substrate cleaning and the post-deposition thermal treatment were discussed. Gate metal was annealed in forming gas at 300-400°C. The second part involved the structural and electrical characterizations. SIMS, ESCA, XRD, and TEM characterized the films. C-V and I-V curves were used to characterize the electrical properties. Interface state density extraction methods including related theories were examined. The third part was focused on process optimization, including the sputtering gas composition and the O_2 annealing pressure. Based on the electrical measured results, it was identified that the optimum film was deposited using gas composition of $O_2/(Ar+O_2)$ = 50% and annealed in O_2 at 200 Torr.

In Chapter III, the fabricated Zr-doped TaO_x films were characterized. An aluminum (Al) gate electrode was used in all capacitors. The influences of process parameters, such as the Zr co-sputtering power, post-deposition annealing condition, and film thickness, were studied. Compared with the undoped TaO_x or ZrO_y film, the moderately Zr-doped TaO_x film showed several advantages, such as a higher dielectric constant and a lower leakage current. A film with small flatband voltage shift and hysteresis could be obtained by carefully adjusting the experimental parameters, such as

Zr doping concentration and annealing temperature. The conduction mechanism of the Zr-doped TaO_x film was analyzed, which was found to fall between the Poole-Frenkel and Schottky emission mechanisms, depending on the dopant concentration and annealing condition. A zirconium silicate interface (Zr_xSi_yO) was formed between the Zr-doped TaO_x film and the Si substrate. The ESCA results showed that when Zr was added into the TaO_x film, binding energies of Ta_{4f}, Zr_{3d} and O_{1s} shifted to lower values due to the decrease of the partial charge exchanges among these three composing elements. The amorphous-to-polycrystalline transition temperature of the film was raised due to the existence of Zr. With a medium Zr dopant concentration, i.e., the Zr/(Ta+Zr) ratio of 0.33-0.56, an increase of the transition temperature as high as 300°C was achieved. For those crystallized films, the grain size and orientation are functions of the dopant concentration, annealing temperature, and film thickness. The addition of dopant varied both the surface energy constraint and the crystal growth mechanism, which are responsible for the suppression of crystallinity.

In Chapter IV, a ~5 Å TaN_x layer was inserted between an 8 nm-thick Zr-doped TaO_x film and the Si substrate in order to study the material and electrical properties. Compared to a film without the inserted TaN_x layer, the new stacked structure showed several advantages, such as a higher dielectric constant, a lower leakage current, and a higher breakdown field. However, the flatband shift due to fixed charges and the interface state density were slightly degraded. Hysteresis of the C-V curve did not vary significantly. Both the Zr dopant concentration and the annealing condition have large impacts on the dielectric properties. SIMS and ESCA were used to analyze this inserted

TaN_x interface layer, which was found to oxidize into an oxynitride, i.e., TaO_xN_y. Si atoms diffused from the substrate to the interface, too. Compared to a thermally grown SiO_2 film with the same EOT, the TaN_x-inserted Zr-doped TaO_x film had a 4 times higher dielectric constant and a 5 orders of magnitude lower leakage current density. On the other hand, the flatband shift, hysteresis, and interface state density were deteriorated.

Chapter V investigated the compatibility of the Zr-doped TaO_x gate dielectrics with various types of metal and metal nitride gate electrodes. First, the fabrication process of the metal nitride gate, i.e., MoN, and WN, was optimized by adjusting the $N_2/(N_2+Ar)$ ratio during the reactive sputtering. By analyzing the film resistivity, it was concluded that the optimal $N_2/(N_2+Ar)$ ratios for MoN and WN were 10% and 2.5% respectively. Second, the microstructures of Mo, MoN, and WN gates were investigated by XRD. The as-deposited as well as the 400°C-N_2 annealed films were crystallized. The Mo film showed a cubic structure with a preferred orientation of (110). The MoN film had cubic (111) and (200) orientations, while the WN film had cubic (111), (200), and (220). Electrical characteristics of the Zr-doped TaO_x films with these gates were analyzed. EOT, current density, breakdown strength, flatband voltage, hysteresis, interface state density, and frequency dispersion were all highly dependent on the gate electrode. For example, while a Zr-doped TaO_x film with a WN gate reduced the leakage current by four orders of magnitude compared to the SiO_2 film at the same EOT, the one with a MoN gate only reduced by about 100 times. Compared to the device performance with an Al gate, the Mo, MoN, and WN gate capacitors had much larger frequency dispersion. This indicated that the ionic impurities from the Mo, MoN, or WN gate

electrode might diffuse through the gate dielectric layers. In general, promising electrical properties were achieved using these gate electrodes. Therefore, the Zr-doped TaO_x film is a promising candidate for the future high-k gate dielectric applications.

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