A WIDEBAND FREQUENCY SYNTHESIZER FOR BUILT-IN SELF TESTING OF ANALOG INTEGRATED CIRCUITS

A Thesis

by

WENJIAN YAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2004

Major Subject: Electrical Engineering

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Approved as to style and content by:

Jose Silva-Martinez (Chair of Committee)	Duncan Walker (Member)
Aydin Karsilayan (Member)	Frederick Strieter (Member)
Chanan Singh (Head of Department)	

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ABSTRACT

A Wideband Frequency Synthesizer for Built-in Self Testing

of Analog Integrated Circuits.

(August 2004)

Wenjian Yan, B.S., Texas A&M University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

The cost to test chips has risen tremendously. Additionally, the process for testing all functionalities of both analog and digital part is far from simple. One attractive option is moving some or all of the testing functions onto the chip itself leading to the use of built-in self-tests (BISTs). The frequency generator or frequency synthesizer is a key element of the BIST. It generates the clock frequencies needed for testing.

A wide-band frequency synthesizer is designed in the project. The architecture of a PLL is analyzed as well as the modifications carried out. The modified structure has three blocks: basic PLL based frequency synthesizer, frequency down-converter, and output selector. Each of these blocks is analyzed and designed. This frequency synthesizer system overcomes challenges faced by the traditional PLL based frequency synthesizer.

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1 INTRODUCTION

Today's integrated circuit (IC) market is soaring with increasing demands from industries such as information technology, communications, and automotive electronics [1]. Traditionally, digital and analog circuits are implemented on separate chips with external on-board interconnects joining the two. The need to reduce cost, area and power consumption has leaded the way for mixed-signal and System-on-Chip (SoC) architectures.

SoC is a major revolution that integrates many functionalities or components such as ASIC, DSP and memory on a single chip. The steady improvements in the silicon technology are allowing more and more blocks to be combined and placed on a single chip. Comparing to board level systems, SoC has many advantages. First of all, higher volumes can be produced which implies lower cost for consumer applications. Secondly, there is also higher flexibility due to programmable components on a SoC. Also, the implementation of both analog and digital circuitries on the same chip has the advantage of having shorter delays between blocks leading to higher inter-block communication bandwidth.

Unfortunately, testing of such chips is more difficult and expensive than standalone analog and digital chips. The cost to test chips has risen tremendously. Not only so, the process for testing all functionalities of both analog and digital part is far from simple. While mature testing procedures and equipments are available for standalone digital and analog chips, mixed signal chips do not have such luxury [2].

This thesis follows the style of *IEEE Journal of Solid-State Circuits.*

Test busses and scan circuitries may be used to access the analog part. However, since signals have to travel through long wires and transmission gates, they can be corrupted [1]. Unlike digital circuits, there is no Boolean expression or high level language simulating all facets of analog signals. While the digital part of the chip may be tested by using standard methods (automatic test pattern generation, scan chains, and fault coverage), the analog part does not have a set of standard methodologies for testing.

1.1 Background and Motivation

There are mixed-signal testers available in the market. These testers are equipped with high performance capabilities to be able to test both digital and analog parts on the chip. However, the exceedingly high cost of mixed-signal testers pushes the search for alternative testing methods. One attractive option is moving some or all of the testing functions onto the chip itself leading to the use of built-in self-test (BIST).

BIST is not an entirely new concept. BIST has been used for many years on digital circuits for fault detection. Within the past decade, BIST shifted over from digital testing to analog testing. The use of BIST is desirable due to its capability to test high volume production hence decreasing the cost of testing per chip. Since BIST is located close to the device-under-test (DUT) without using external busses or components, BIST not only decreases the cost for testing it can also reduce measurement errors. In most cases, the testing done in BIST is used to convert analog signals to digital format in order to employ sophisticated and expensive test equipment [3]. BIST typically operates in the following fashion: BIST receives some kind of stimulus and converts the stimulus into

digital format. The digitized stimulus is passed to the DUT. The results are then analyzed via a cheaper external digital tester.

An example BIST architecture used for mixed-signal testing is shown in Figure 1 [4]. The architecture has three main building blocks: stimulus generator, which can be a signal generator or a DAC; ADC; and a digital processor. The stimulus generator produces a set of frequencies. Many BIST tests for linear analog circuits such as amplifiers, filters and data converters need a stimulus source of certain frequency range. This set of frequencies feeds into a smoothing filter to minimize noise. The design of such frequency generator, or frequency synthesizer, is an open problem that is addressed in this work.

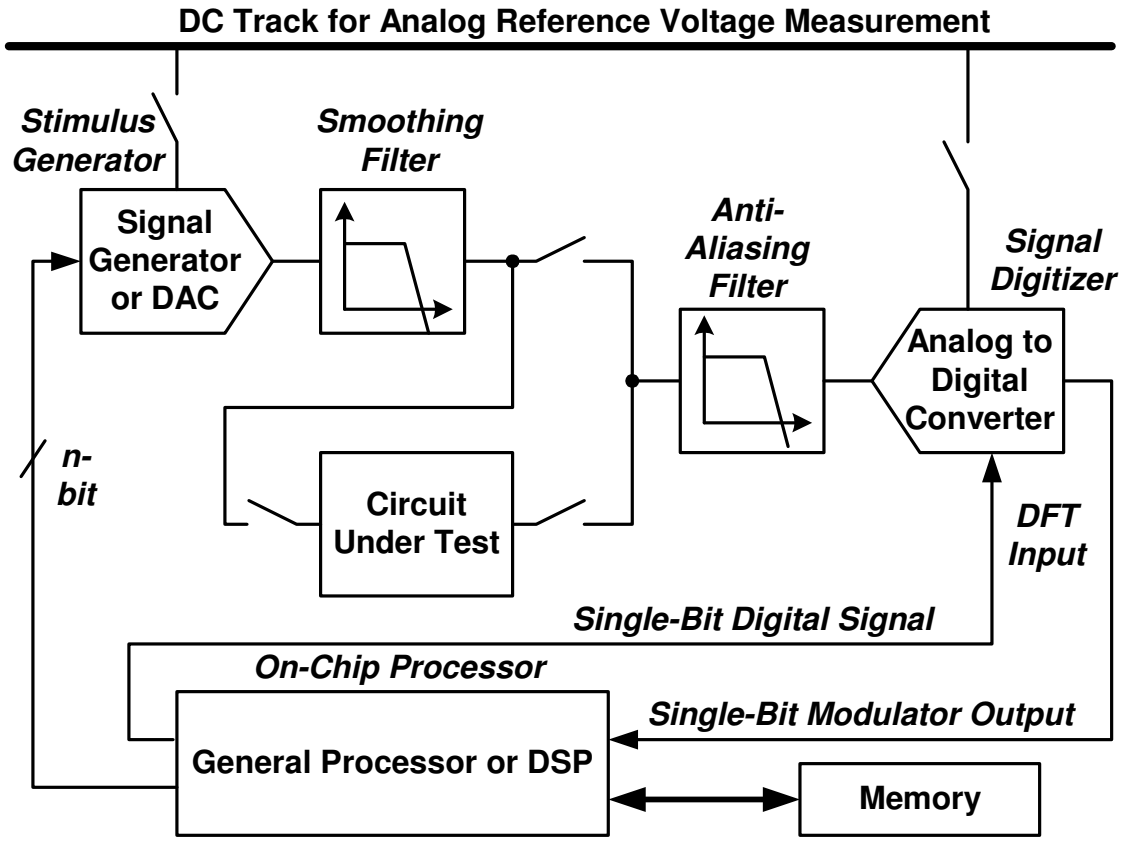


Figure 1 Mixed-Signal BIST Architecture

The signal feeds into the circuit-under-test (CUT) or DUT as an input. The output of the CUT goes into an anti-aliasing filter before it is digitized and modulated through the signal digitizer. The signal is then processed by a processor or a DSP. The output of the DSP offers the test results.

The above BIST architecture is only an example of the many architectures typically used. Another architecture that uses an on-chip spectrum analyzer [5] is shown in Figure 2.

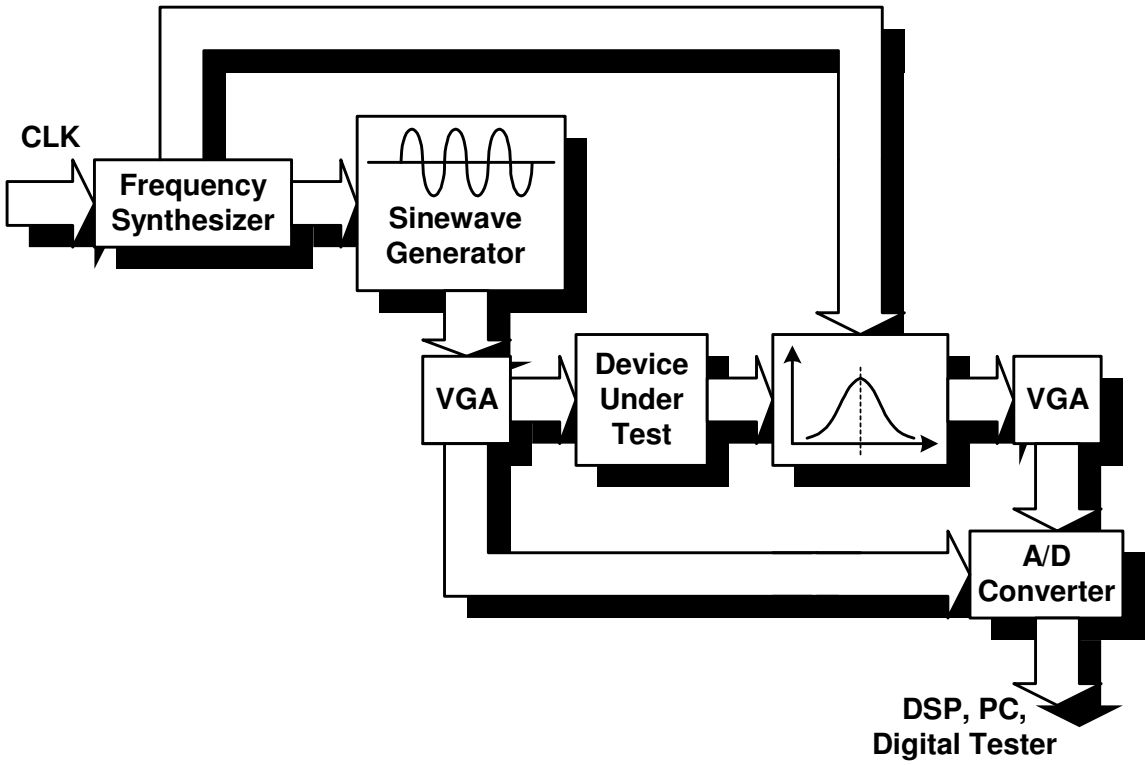


Figure 2 On-Chip Spectrum Analyzer

The frequency synthesizer feeds the clock of the sine wave generator as well as the bandpass filter. The output of the sine wave generator, through a variable gain

amplifier (VGA), is applied to the DUT. The output from the DUT goes through a switched-capacitor bandpass filter that is clocked by the frequency synthesizer. The filtered signal then goes through another VGA and is converted to digital form and sent to the external digital tester.

The frequency generator or frequency synthesizer is a key element of the BIST. There are several techniques reported for signal generation: sigma-delta, switched capacitor and phase locked loop [6]. Each of these techniques has advantages and disadvantages. They will be discussed in the next section.

1.2 Challenges and Requirements

Although BIST offers improvement to mixed-signal chip testing, there are many challenges in the design of the BIST generator circuit. A major concern is the area overhead caused by the extra circuitries. The silicon area of the generator needs to be as small as possible so that it is economically practical. Another concern is the complexity of the high quality signal generator and analysis circuitry. The quality of the test signal needs to exceed that of the DUT. Otherwise, the accuracy of the test is degraded [7]. A delicate balance exists between cost and complexity.

Sigma-delta technique is used for DAC and ADC stimulus generation. Sigma-delta modulation utilizes over sampling techniques. While this technique is robust against process variation and easier to manipulate the digital results, the major drawback for this technique is its complexity. FFT transformation is needed to process the output digital signal. This is a complex procedure that takes a large amount of memory and processing power which over shadows the advantage of this method [4].

There are some basic requirements for the stimulus generation. A typical requirement is that the BIST circuit is entirely on-chip. Any external components such as capacitors and resistors will degrade signal quality and increase the cost of the product due to extra pins. Another requirement is the complexity of the circuit. If the circuit is too complex, the power consumption and time for testing increases.

In the next few sections, the design of a phase locked loop (PLL) based frequency synthesizer is described. Section 2 will cover background information of signal generation and the two common techniques used in the industries. Several structures are proposed for different motivations. One final structure is chosen with the most advantages overall.

Section 3 outlines the system specifications and also analyzes the frequency synthesizer structure for a number of considerations. Stability and phase noise performance are analyzed at the system level. This section also analyzes each building block of the system following the signal flow.

Section 4 further analyzes the system stability for this particular frequency synthesizer. A detailed design procedure is given. Final calculation and simulations results are given. The system generates two bands of frequencies of 10KHz -1MHz and 1MHz -100MHz with a resolution of 10KHz and 1MHz, respectively. The phase noise of the overall system is -50dBc/Hz at 1MHz offset for frequencies 1MHz – 100MHz, and -90dBc/Hz at 10KHz offset for frequencies 10KHz – 1MHz.

Section 5 concludes the project with comments on the system as well future work to be done on the system.

2 SIGNAL GENERATION

2.1 Signal Generation Techniques

There are many techniques to designing a signal generator. As mentioned in the previous section, there are some limitations to the implementation of the signal generator due to its BIST application. A major concern is the area overhead caused by the extra circuitries. Another concern is the complexity of the high quality signal generator and analysis circuitry. The quality of the test signal needs to exceed that of the DUT. A delicate balance exists between cost and complexity. Below is a list of common techniques used for frequency generation. However, this list is by no means comprehensive.

2.1.1 Direct Digital Synthesizer

The Direct Digital Synthesizer (DDS) is a popular technique for many reasons [8]. It uses digital components to generate a range of frequencies from a single reference clock. The concept is simple: A sinusoidal waveform is generated from a lookup table that is controlled by a phase accumulator. Figure 3 shows an example of a tunable DDS. A precision reference clock supplies a fixed frequency to the phase accumulator. The phase accumulator is essentially a counter that gives an address to the lookup table. A sine wave lookup table is stored in a programmable read-only memory (PROM). The DAC generates a sinusoidal output from the lookup table. The output frequency of the DDS depends on both the reference clock and the sine wave step size of the lookup table stored in the PROM. Intuitively, the faster the reference clock, the faster the output

frequency. The larger the PROM, the more data can be stored leading to finer the step frequency, or resolution.

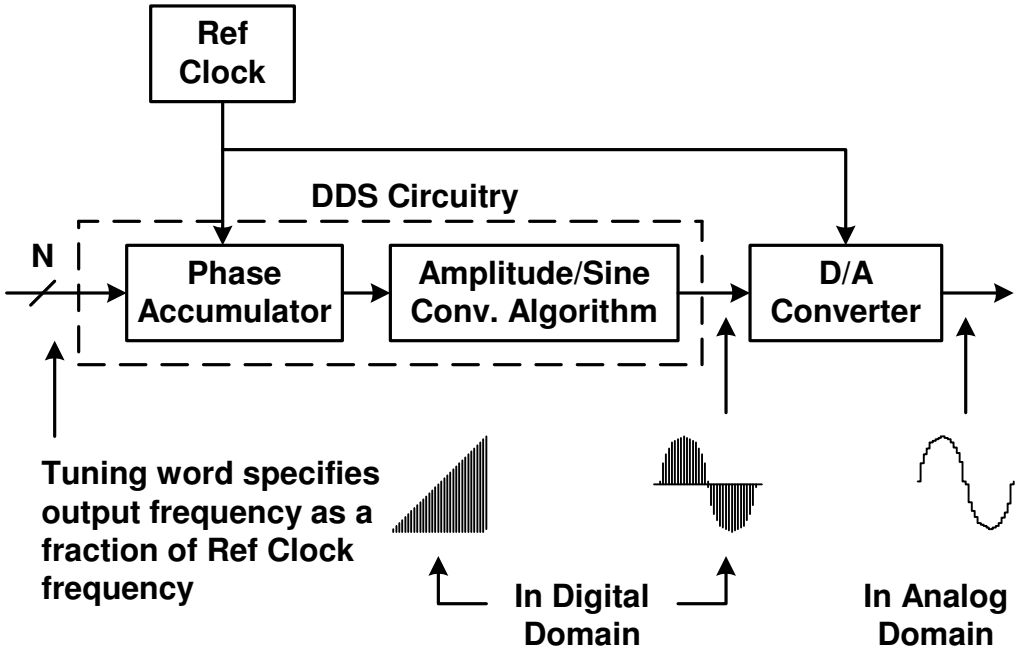


Figure 3 Frequency Tunable DDS

This technique has many desirable features. One advantage of this structure is that all signal processing is controlled digitally. The system does not suffer from temperature and process variations like analog circuits do. Another advantage of this structure is the tuning resolution. A very fine resolution may be attained if the PROM is large. Yet another advantage is the speed of which the output could "hop" from one frequency to another without overshoot or undershoot.

Despite the many advantages of this structure, the negative aspect of this structure is the PROM. In order to achieve a fine resolution, a large memory is needed. This could cause the area overhead to be too large to be economically viable.

2.1.2 Phase Locked Loop (PLL) Based Synthesizer

A third option is a PLL based frequency synthesizer. PLL based frequency synthesizers are relatively simple in concept and do not require a high speed reference clock. The main purpose of the PLL is to generate stabilized output frequency signals from a fixed low frequency reference. There are three main components in a PLL: phase detector, low pass filter and a voltage controlled oscillator (VCO) shown in Figure 4. The phase detector senses any phase error between the reference frequency and the output frequency from the feedback. The phase detector produces an output voltage proportional to the phase error. The error translated voltage is sent to the VCO through a low pass filter. The filter cleans the VCO control voltage by filtering out high frequency noise spurs and unwanted higher harmonics. The VCO frequency increases or decreases according to the input voltage. The system is "locked" when the frequency of the output equals the input and the phase error reaches zero or settles to a constant value.

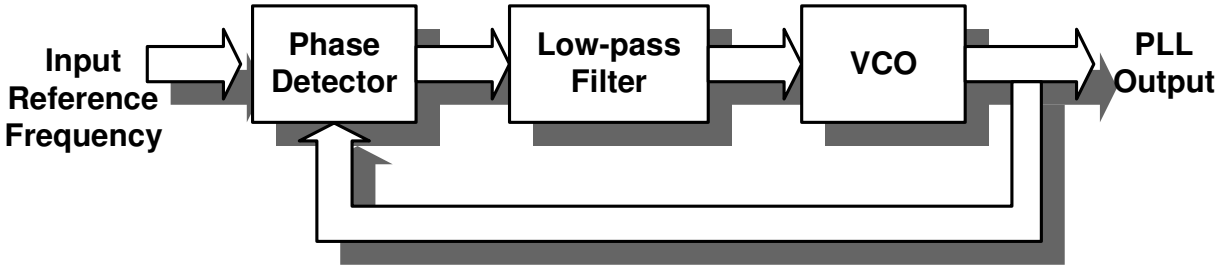


Figure 4 Phase Locked Loop

PLL based synthesizers are relatively straightforward. They do not require additional memory like the DDS, which take up a large area. Therefore, a PLL based frequency synthesizer will be chosen for this frequency synthesizer design. The idea of a PLL based synthesizer is explored further in section 2.2.

2.1.3 Switched-Capacitor Based Sine Wave Generator

The switched-capacitor based sine wave generator is used after the frequency synthesizer to convert the digital output form into sinusoidal form [9]. Figure 5 shows the implementation of a variable gain amplifier (VGA) used for sine wave generation.

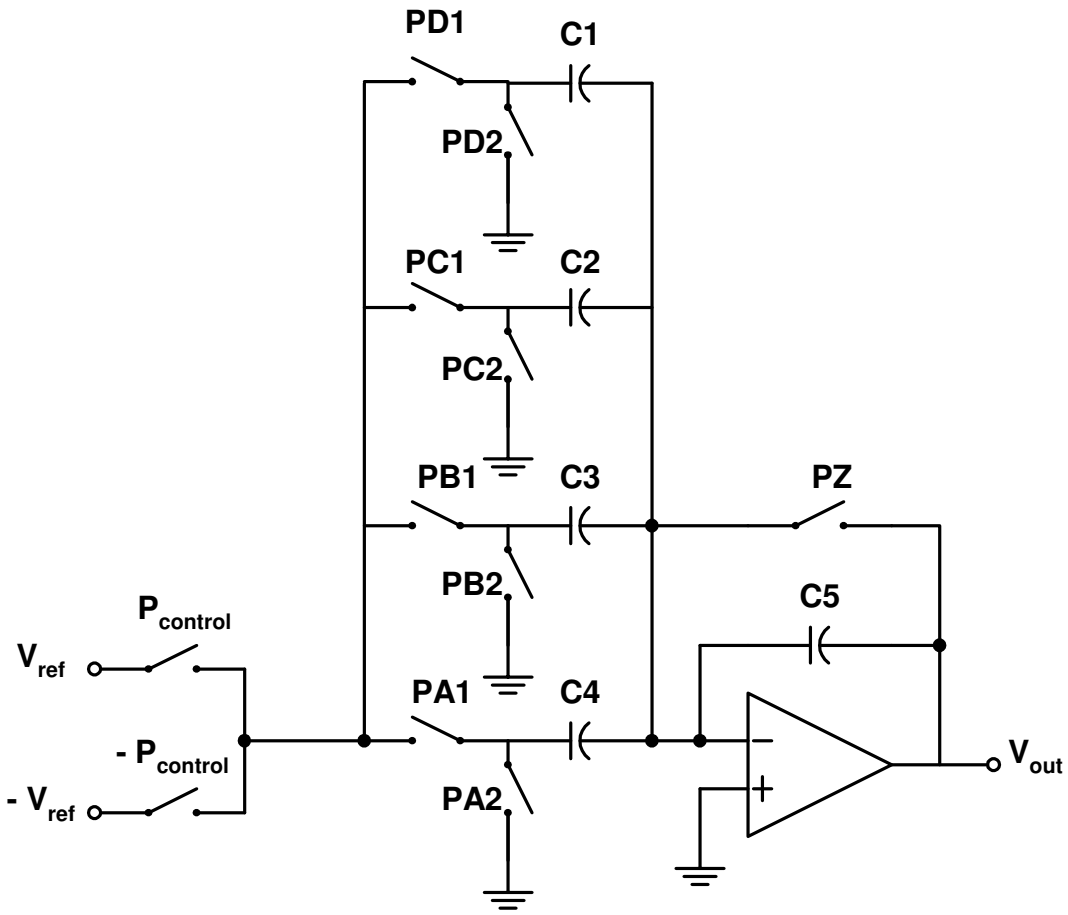


Figure 5 Variable Gain Amplifier for Sine Wave Generation

The main advantage of this technique is its simplicity. The VGA has 4 gain stages that generate 16 steps per sinusoid period. The switches are closed sequentially from PA1

to PD1 to generate a quarter of the sine wave, the switches then close in the opposite direction to generate the second quarter of the wave. To create the second part of the waveform, the input switches from +Vref to –Vref. Pure sinusoidal waveforms are generated from the clock signals that are generated from the frequency synthesizer. The reference frequency needs to be at least 16 times the sinewave frequency. The control logic for the switches needs non-overlapping phases. Also, the maximum operation frequency is limited by the maximum operable frequency of the opamp.

2.2 Phase Locked Loop Architectures

There are two main architectures for the implementation of a PLL-based frequency synthesizer: integer-N and fractional N. N is the division ratio in the feedback path. Other hybrid architectures exist that are based on the two basic structures.

2.2.1 Integer-N Structure

The integer-N architecture is the simplest form of a PLL-based frequency synthesizer. It has all the components of a PLL with an additional integer divider in the feedback path, as shown in Figure 6.

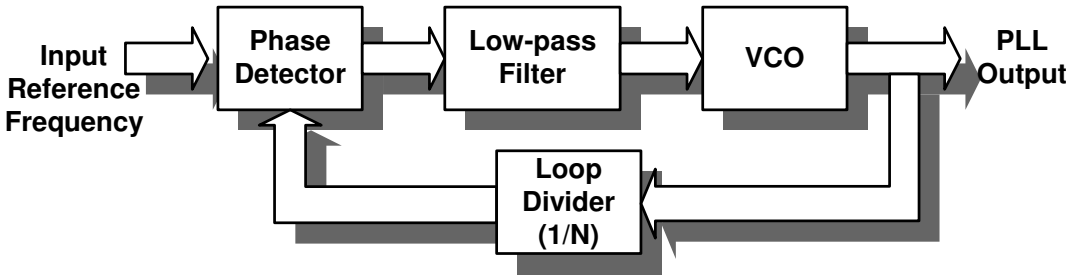


Figure 6 PLL-Based Frequency Synthesizer

The output of the PLL has a direct relationship with the input reference frequency in such a way that the output frequency is the input reference frequency times the programmable loop divider ratio N.

$$f_{out} = Nf_{ref} \tag{1}$$

As N varies, the output frequency varies proportionally. This structure has many advantages. The PLL structure gives accurate and robust output when the system is locked. The feedback structure ensures that once the system is locked, the output is exactly N times the input. It generates different frequencies from a single input reference frequency.

Although this is a simple and robust structure, there are some negative aspects to consider. Phase noise is one of the most important matters of a frequency synthesizer. In the integer-N PLL-based frequency synthesizer, the phase noise at the output is degraded by $\log_{10} N$ from the input. In order to have small phase noise, N needs to be sufficiently small. A second consideration is stability. A PLL-based frequency synthesizer is at least a second order system due to poles introduced by the VCO and the loop filter (analysis is given in the next section). If N varies greatly, stability of the system will be affected due

to loss of phase margin as well as the loop gain variation. Another issue to consider is the resolution or frequency step of the system. Since the output of the frequency synthesizer is N times the input, the smallest resolution is the input reference frequency. If the frequency synthesizer specification demands small frequency steps in a large frequency range, a large N range is needed, which might cause the system to be unstable. A long locking time may also occur due to the small reference frequency and narrow loop bandwidth.

2.2.2 Fractional-N Structure

Fractional-N structure is created to reduce phase noise and increase resolution for a fixed input reference [10]. It is based on the simple PLL structure with a fractional division ratio rather than an integer N. For the same specification of a small frequency step in a large frequency range, the fractional-N frequency synthesizer is able to overcome the problems in an integer-N PLL structure. Instead of dividing the output frequency by an integer, a fractional number is used. Smaller frequency steps may be achieved and hence increases the resolution of the system. A Sigma-Delta structure is commonly used for the fractional-N architecture (see Figure 7).

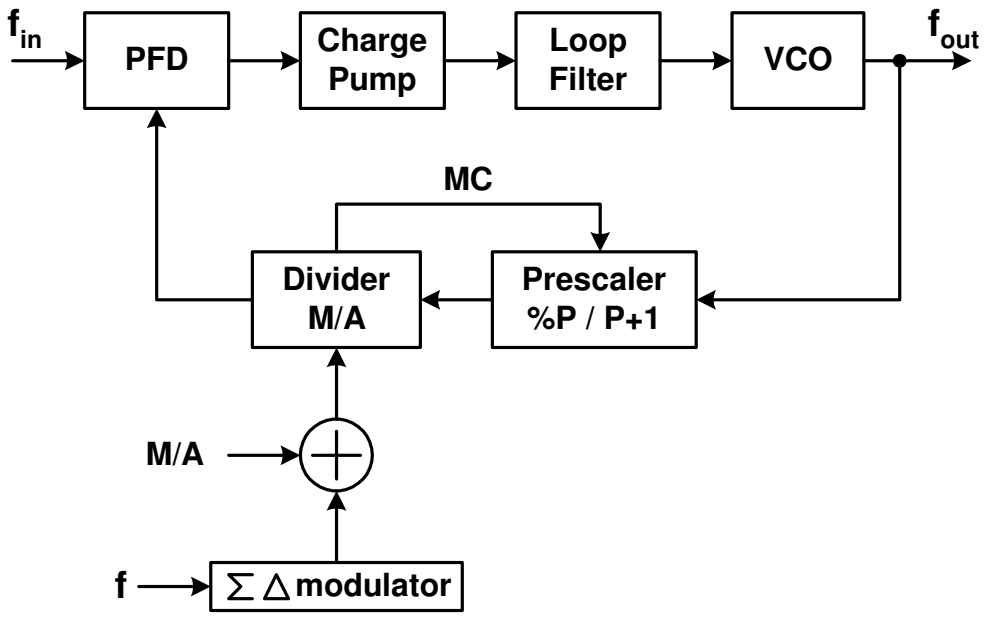


Figure 7 Sigma-Delta Fractional PLL Frequency Synthesizer

A dual-modulus prescaler and a programmable divider are employed. The ΣΔ modulator is used to randomize the instantaneous divider ratio. It effectively divides between two integers (P and P+1) and the division ratio is dynamically switched between the two numbers. The output of the system is given as:

$$f_{out} = f_{in} \times (M \cdot P + A + f) \qquad (2)$$

M and A are programmable integers and f is a programmable fraction.

Although the fractional-N structure has many attractive qualities, it has two major drawbacks. The ΣΔ modulator is a complex circuit that takes a large amount of area. The fractional-N structure also has large fractional spurs at an offset frequency of the fractional part of the division and possibly its harmonics.

2.3 Frequency Synthesizer Architecture

Despite the many advantages of the fractional-N such as finer resolution, faster settling time and reduced phase noise, the architecture requires much complexity and a large area. Considering the application of the frequency synthesizer, which is for built-in self-test, the drawbacks of the fractional-N structure are too costly.

The architecture chosen for the frequency synthesizer is based on the integer-N PLL structure. However, a simple integer-N structure can not be used by itself. Since the output frequency is N times of the input frequency for an integer-N PLL based frequency synthesizer structure, the frequency step is the input frequency. If the input frequency is 10KHz, the frequency range of this synthesizer covers four decades. If the integer-N structure is used without modification, the value of the loop divider, N, would have to vary from 1 to 10^4. This means that the loop gain of the system will change by a factor of 10000 causing the system to be potentially unstable. Also, the implementation of this loop divider will need a large chip area due to the large number of digital components.

The application of this frequency synthesizer requires that all components of the system are on-chip. If the input frequency of the PLL equals the resolution of 10KHz, the loop filter needs to have a cutoff frequency less than 10KHz which leads to a large time constant of at least100μs. The implementation of a simple passive resistor and capacitor structure that will meet this time constant will not fit on a chip. This means that the implementation of the loop filter is an issue. Another issue is that the phase noise of this system at the output degrades approximately $20\log(N) = 80dB$ from the noise performance of the input reference. Although there is not a phase noise specification, a signal needs to be distinguishable from noise. An 80dB degradation of the input reference

signal would cause the output to have a very small signal to noise ratio. Also, the design and implementation of the voltage controlled oscillator (VCO) is difficult due to the limitations on the charging and discharging of capacitors.

The proposed architecture utilizes the traditional PLL-based architecture and includes additional components to overcome the issues described, it is shown in Figure 8.

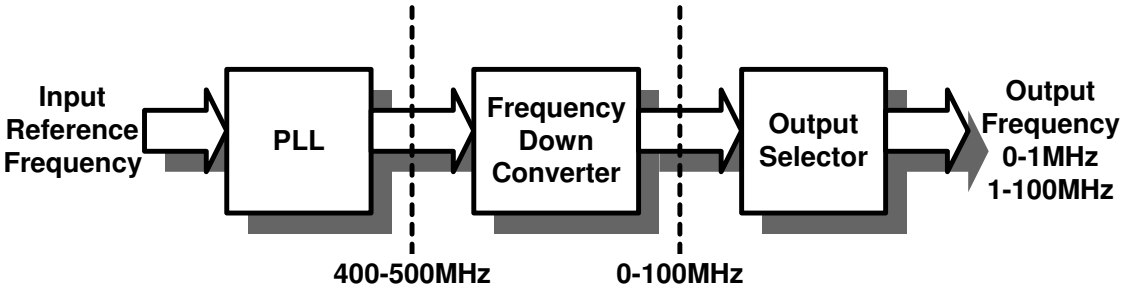


Figure 8 Frequency Synthesizer Architecture

The PLL generates a band of frequencies that is much higher than the desired output frequencies (400-500MHz). The higher frequency output minimizes stability issues because the tuning range (100MHz) is only 25% of the smallest output frequency (400MHz).

The frequency down converter is composed of a mixer and a lowpass filter that down converts the output of the PLL (400-500MHz) to the desired output frequencies (10KHz-100MHz). The filter then filters out the high frequency components.

The issue of the large RC constant still exists. Simply moving the output frequencies to a higher range does not decrease the bandwidth of the loop filter. A capacitive scaling approach could possibly implement the filter. However, the settling time will take at least five times the time constant, which is 500μs. This settling time is too large. In order to resolve the issue of large RC constant without compromising the

settling time, the input reference frequency is increased from 10KHz to 1MHz. This increase of 100 in frequency increases the loop bandwidth also by 100. The time constant then decreases to 1μs. A 1μs time constant is much easier to implement on-chip than a 100μs time constant. This solves the issue of the filter implementation.

Although the output of the frequency down converter covers the desired frequency range of 0-100MHz, the resolution is much larger than specified due to the increase of input reference frequency (1MHz). One solution is to divide the output of the down converter by the same fixed factor of 100 as from the input frequency increase to recover the desired frequency step of 10KHz. The output can achieve the 10KHz resolution from DC to 1MHz. There are now two possible outputs for the system: DC-1MHz with a resolution of 10KHz, and 1-100MHz with a resolution of 1MHz. An output selector can choose from the two different output frequency ranges. One output signal comes directly from the previous block and is converted into a square wave; another output is from the previous block through a fixed digital divider of 100.

A more complex adjustable divider is another option where the division ratio is adjustable instead of fixed to 100. For the same frequency of 0-100MHz, larger division ratio leads to finer resolution. However, the frequency range of the finer resolution changes also. The finer the resolution is, the smaller the frequency range will be. For a resolution of 1KHz, output of the down converter is divided by 1000, and the output of the system will be 1-100KHz or 1-100MHz with a resolution of 1KHz and 1MHz, respectively. Frequencies between 100KHz and 1MHz are not generated. Since the system only requires a resolution of 10KHz, the adjustable divider is not necessary. However, this degree of freedom may be useful for other applications.

This structure can give an output of 10KHz to 1MHz with a resolution of 10KHz and an output of 1-100MHz with a resolution of 1MHz. It overcomes the stability issue by decreasing the range of the division ratio, N, from between 1 and 10^4 to between 400 and 500 in variation and stabilizes the system. The proposed structure also has less phase noise due to a smaller division ratio. The structure also overcomes the overhead area needed from a loop bandwidth of 10KHz as well as decreases the settling time. However, there is one drawback, the resolution of the system is not uniform.

Although the resolution is not uniform for the entire frequency spectrum, it can be justified. If the number of points within a range of frequencies is fixed, then larger the frequency range means larger the frequency step. The resolution is inversely proportional to the number of points in the range. The range of DC-1MHz has the same number of points as the range of 1-100MHz. With this assumption, the output frequency resolution is acceptable.

3 MODIFIED PLL IN FREQUENCY SYNTHESIZER

3.1 Specifications

A recent report [6] describes a frequency synthesizer with a tuning range of 38-167MHz, resolution of 1MHz in the TSMC 0.35µm standard CMOS technology. The objective for this project is to design and implement a wideband frequency synthesizer in a 0.5µm nwell CMOS process. The operating frequency ranges from 10KHz to 100MHHz with a frequency resolution of 10KHz using a 3V power supply. No external components are permitted due to the BIST application.

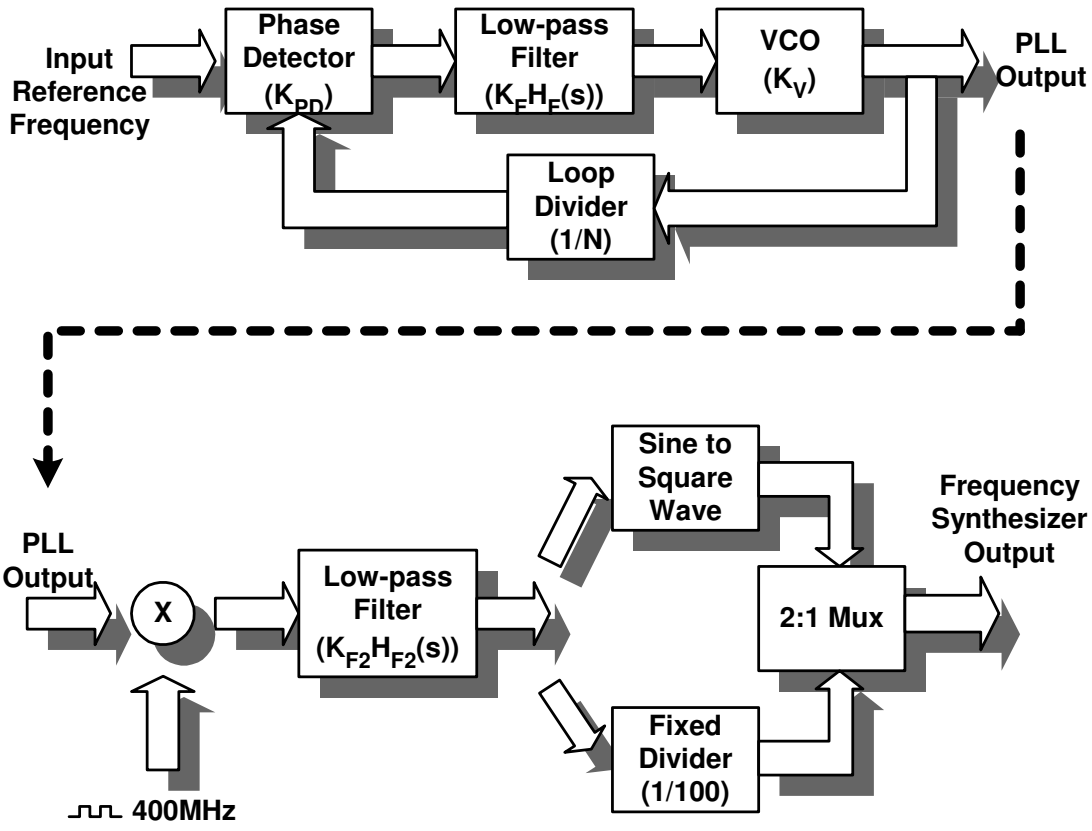


Figure 9 Frequency Synthesizer Structure

Figure 9 shows the block diagram of the implementation of the frequency synthesizer. It is divided into two parts: the top part is an integer-N PLL and the bottom part consists of all other blocks. Each individual block is analyzed in the sections below.

3.2 PLL Analysis

3.2.1 Linear Loop Analysis

The linear loop analysis is performed under the assumption that the loop is in lock (i.e. the output frequency is equal to the input frequency). The PLL generates different frequencies from the same input reference frequency by varying the value of N, where N is the value of the programmable divider. Linear analysis also assumes the input and output of the PLL are in phase, not in frequency.

K_{PD}, K_F, and K_V are the gain of the phase detector, filter and VCO, respectively. The open loop transfer function can be obtained as:

$$H_{ol}(s) = \frac{K_{PD} K_F H_F(s) K_V}{Ns} \tag{3}$$

The closed loop transfer function can be obtained by adding the feedback in the loop as:

$$H_{cl}(s) = \frac{\theta_o}{\theta_i} = \frac{K_{PD} K_F H_F(s) K_V / s}{1 + K_{PD} K_F H_F(s) K_V / Ns} \tag{4}$$

The filter is a critical part of the PLL because it suppresses noise from the control line of the VCO. If the low pass filter has one pole at DC and a stabilizing capacitor providing a zero, then the filter can be expressed as:

$$F(s) = K_F \frac{\left(1 + \frac{s}{\omega_z}\right)}{s} \tag{5}$$

where ω_z is the frequency of the zero. By substituting the transfer function of the filter into the PLL, it gives the following phase transfer function:

$$\frac{\theta_o}{\theta_i} = \frac{(s + \omega_z)\left(\frac{K_{PD} K_V K_F}{\omega_z}\right)}{s^2 + s\left(\frac{K_{PD} K_V K_F}{\omega_z N}\right) + \frac{K_{PD} K_V K_F}{N}} \tag{6}$$

The error transfer function indicates the difference between the input and the output phase. The transfer function is as follows:

$$\frac{\theta_e}{\theta_i} = \frac{\theta_i - \theta_o}{\theta_i} = \frac{s}{s^2 + s\left(\frac{K_{PD} K_V K_F}{\omega_z N}\right) + \frac{K_{PD} K_V K_F}{N}} \tag{7}$$

From the standard control system format, the denominator of the phase transfer function can be expressed as:

$$D(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{8}$$

where the natural frequency, ω_n, and the damping factor, ζ, are defined as:

$$\omega_n^2 = K_{PD} K_V K_F / N \tag{9}$$

$$\zeta = \frac{\sin(PM)}{2\sqrt{\cos(PM)}} = \frac{\omega_n}{2\omega_z} \tag{10}$$

ω_n is the location of the pole and ζ is a measure of stability, where ζ is a function of phase margin, PM. If ζ is zero, then the poles of the system lie on the imaginary axis resulting

steady oscillation at frequency ω_n. As the damping factor increases, the poles move to the left hand plane and the system becomes stable.

The impulse and step response of the PLL also test the stability of the system. Since the natural frequency, ω_n, changes proportional to $\sqrt{1/N}$, and the bandwidth changes proportional to N, stability is checked.

Frequency Impulse Response

A step variation in phase is an impulse variation in frequency. The input phase changes according to the following expressions in time domain:

$$\theta_i = (\Delta\theta)u(t) \tag{11}$$

By taking the Laplace transformation,

$$\theta_i(s) = \frac{\Delta\theta}{s} \tag{12}$$

So the output phase of the PLL becomes

$$\theta_o = \frac{\omega_n^2\left(1+\frac{s}{\omega_z}\right)}{s^2 + s(2\xi\omega_n) + \omega_n^2} \cdot \frac{\Delta\theta}{s} \tag{13}$$

The error output of the PLL becomes:

$$\theta_e = \frac{s^2}{s^2 + s(2\xi\omega_n) + \omega_n^2} \cdot \frac{\Delta\theta}{s} \tag{14}$$

Using the *Final Value Theorem*, the limit of the error output can be seen as:

$$\lim_{t\to\infty}\theta_e(t) = \lim_{s\to 0}(s\theta_e(s)) = 0 \tag{15}$$

It is obvious from the above equation that the error introduced from a step in phase or a frequency impulse at the input reaches zero eventually.

Frequency Step Response

A step variation in frequency is a ramp variation in phase. The input frequency changes according to the following expressions in time domain:

$$f_{in} = f_o + (\Delta f)u(t) \tag{16}$$

$$\theta_i = (\Delta\omega)t \tag{17}$$

By taking the Laplace transformation, the input phase can be expressed in s domain as:

$$\theta_i(s) = \frac{\Delta\omega}{s^2} \tag{18}$$

The output phase of the PLL can be stated as

$$\theta_o = \frac{\omega_n^2\left(1+\frac{s}{\omega_z}\right)}{s^2 + s(2\xi\omega_n) + \omega_n^2} \cdot \frac{\Delta\omega}{s^2} \tag{19}$$

The error output of the PLL becomes:

$$\theta_e = \frac{s^2}{s^2 + s(2\xi\omega_n) + \omega_n^2} \cdot \frac{\Delta\omega}{s^2} \tag{20}$$

Using the *Final Value Theorem*, the limit of the phase error can be expressed as:

$$\lim_{t\to\infty}\theta_e(t) = \lim_{s\to 0}(s\theta_e(s)) = \frac{\Delta\omega}{K_{PD}K_V K_F \omega_z} \tag{21}$$

It is clear that the limit does not go to zero. This means that the error introduced from a frequency step or a phase ramp at the input does not reach zero at the output. Instead, it settles to the value $\frac{\Delta\omega}{K_{PD}K_V K_F \omega_z}$.

3.2.2 Phase Frequency Detector

The Phase Frequency Detector (PFD) senses the difference between the reference frequency and the output in both phase and frequency. The PFD outputs are put across as controls to the charge pump. When the reference signal is larger than the output, the PFD signals the charge pump to inject more charge to the loop filter thus creating a larger control voltage for the VCO; when the reference signal is smaller, current is extracted. Since the operating frequency of the phase detector is relatively low, a digital circuit can be used. There are several architectures for the implementation of the PFD.

The simplest architecture is an XOR gate where the output of the gate checks if the inputs are equal. This is an excellent phase detector for quadrature signals due to its simplicity. However, it can not differentiate between lead and lag phases. Therefore, this is not a good phase detector for the PLL.

Another architecture is a sequential phase detector that is composed of the set-reset (SR) flip-flop (Figure 10). A transition on one input sets the flip-flop and another transition on the other input resets it. The gain for this detector is $K_D = \frac{VDD}{2\pi}$ [11]. This phase detector detects a 180-degree phase difference in lock. Some times a 0-degree phase difference in lock is needed.

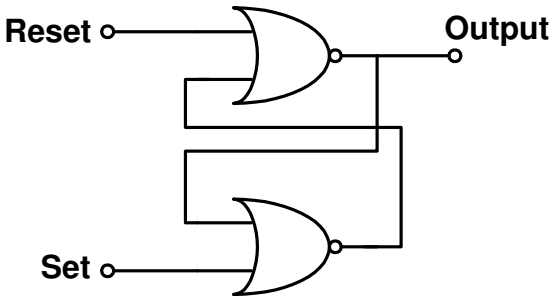


Figure 10 Set-Reset Flip-Flop

The PFD used for the design of this frequency synthesizer is composed of two D-flip flops with an AND gate in the feedback path. This phase frequency detector has a 0-degree difference in lock as well as a larger input range of 4π. The phase detector gain, however, remains the same as the SR flip-flop phase detector of $K_D = \frac{VDD}{2\pi}$. However, this structure has a dead zone at zero. Ideally, the phase detector is expected to detect every small phase difference. In reality, the circuit can not detect these small differences around zero. A dead zone occurs. When the loop operates in the dead zone, the PFD stop responding to the phase difference and the VCO effectively operates in open loop. This can be avoided by adding more delays to the feedback path (see Figure 11) such that when the phase error is zero, there is no charge injecting into the loop filter.

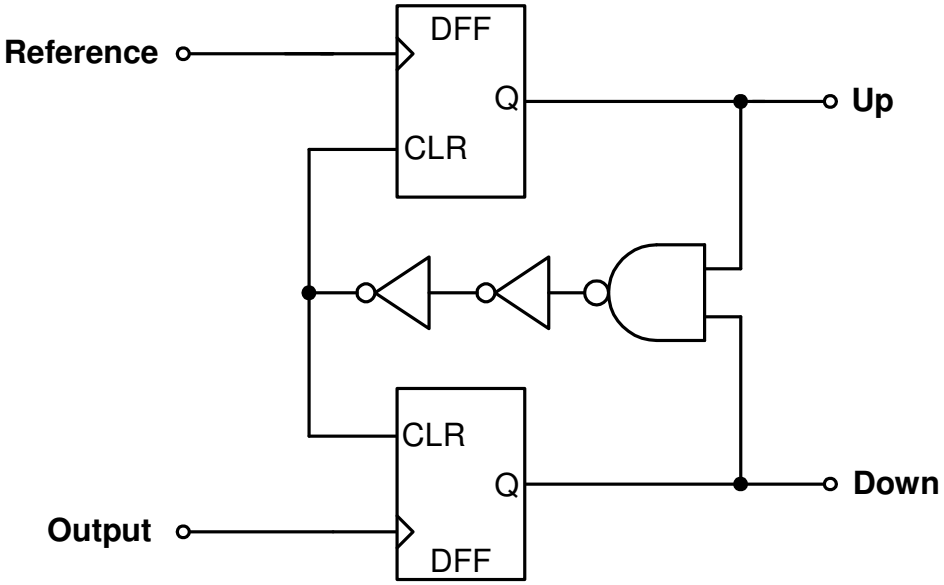


Figure 11 Phase Frequency Detector

The phase detector controls the amount of charge injected to or extracted from the loop filter. When the reference phase leads the divider output, the output *Up* switches on high and *Down* switches to low, effectively injecting more charge to the loop filter and creating a larger control voltage for the VCO. A larger control voltage increases the output frequency of the VCO, thus reduces the phase difference between the two inputs. Similarly, when the divider output phase leads the reference, the PFD switches *Down* on high and *Up* to low so charge will be extracted from the loop filter, decreasing the control voltage for the VCO which decreases the VCO output frequency. When the system is in lock, phase and frequency match, the NAND gate outputs low and resets the DFFs. This generates small pulses at the output of the PFD. The setup of the PFD, the charge pump and the loop filter is shown in Figure 12.

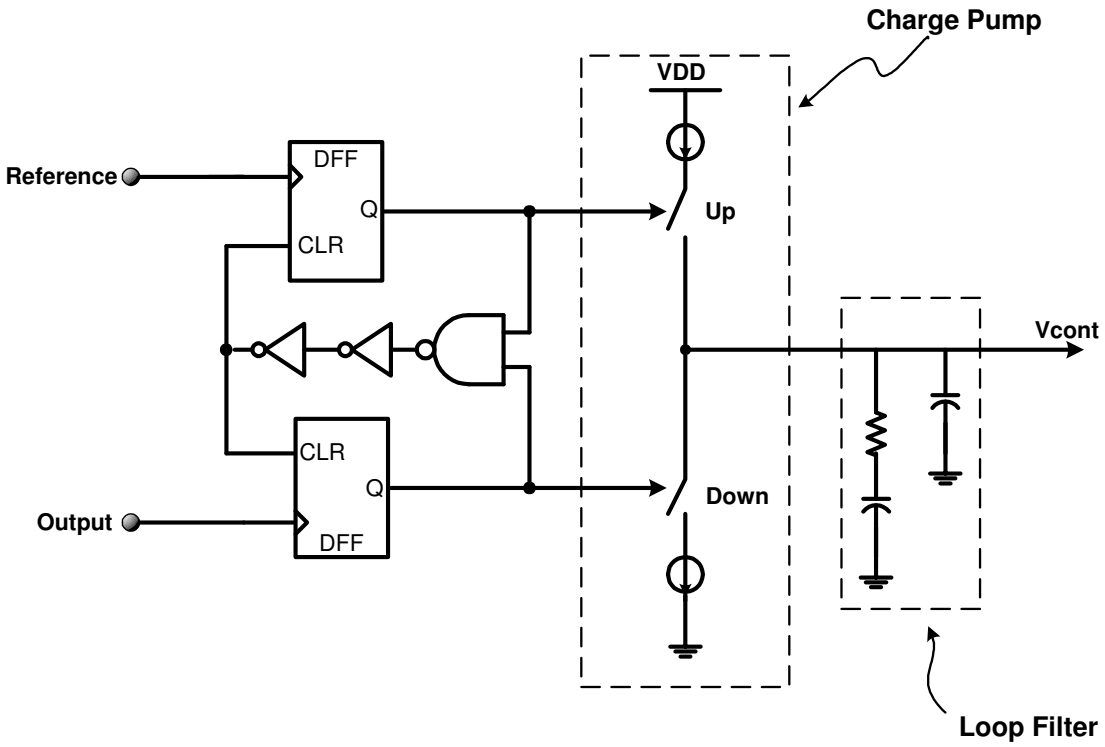


Figure 12 PFD, Charge Pump and Loop Filter

3.2.3 Charge Pump

A charge pump produces a current that is proportional to the phase difference between *Reference* and *Output* inputs of the PFD in both magnitude and sign. It has several critical parameters. First, the output voltage range needs to be maximized in order to obtain maximum VCO tuning range. However, this parameter is limited by the supply voltage of the system. Second, the charge pump needs to have high output resistance for the *Up* and *Down* current sources. Any mismatch between these currents will generate spurs at the output.

The design of the charge pump starts with the selection of the charge pump current. A reasonably current (>5μA) is needed for the simple charge pump. If the current is small, the noise would be large at the output. However a different structure altogether could help with the noise performance and help reduce the charge pump current.

The simple charge pump structure (Figure 13a) has many shortcomings. It has low output resistance, low PSRR and poor isolation between UP/DN and the output. A cascade structure (Figure 13b) has higher output resistance and higher PSRR but has the drawbacks of poor isolation and reduced output dynamic range.

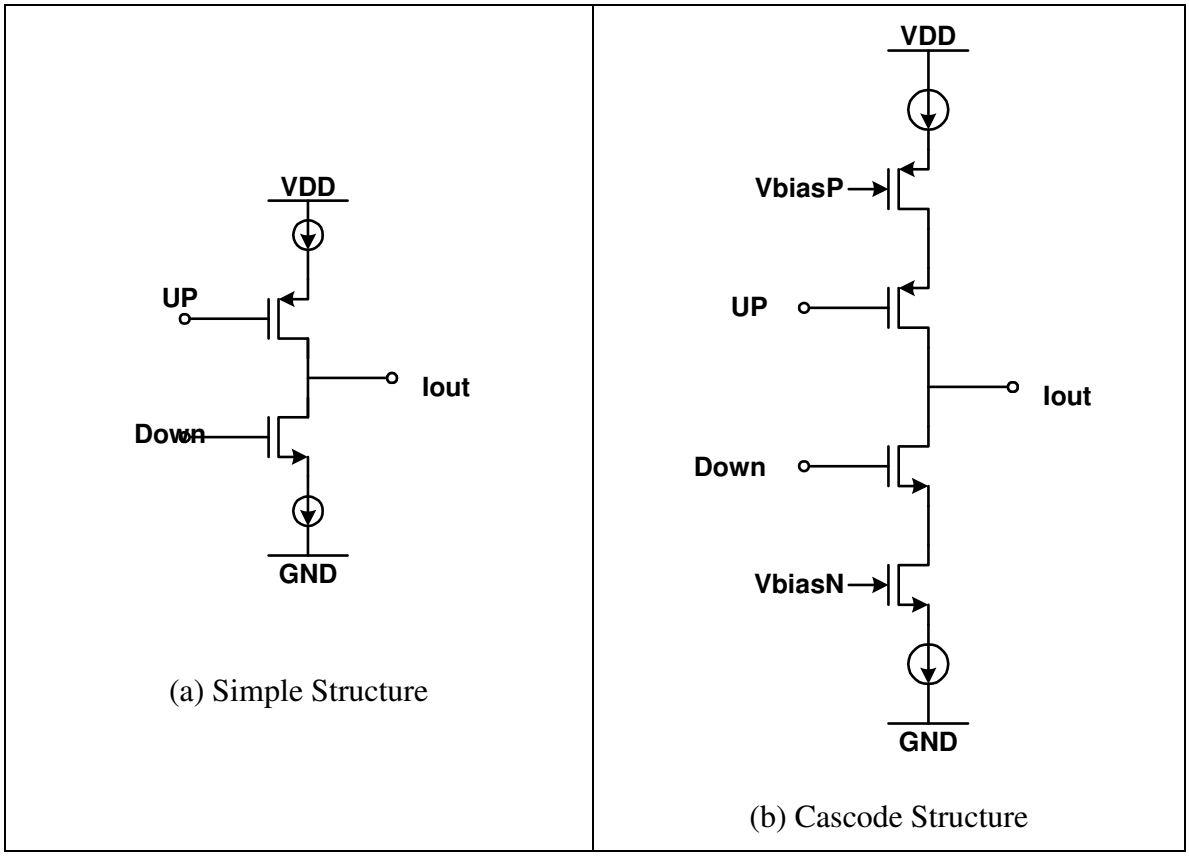


Figure 13 Charge Pump Structures

The third architecture is used in the implementation of the frequency synthesizer designed (see Figure 14) [12]. This charge pump is able to handle all the shortcomings listed above. However, it a smaller output swing due to the cascode structure. The cascode mirror at the output reduces the dependence of the output voltage to the current thus reduces the phase noise. The cascode current mirror structure may not be necessary since phase noise is not a major issue. Further analysis is needed to examine the structure without the cascode current mirror. Due to the time limitation on the project, the structure is used without modification. Details for the design will be given in the next section.

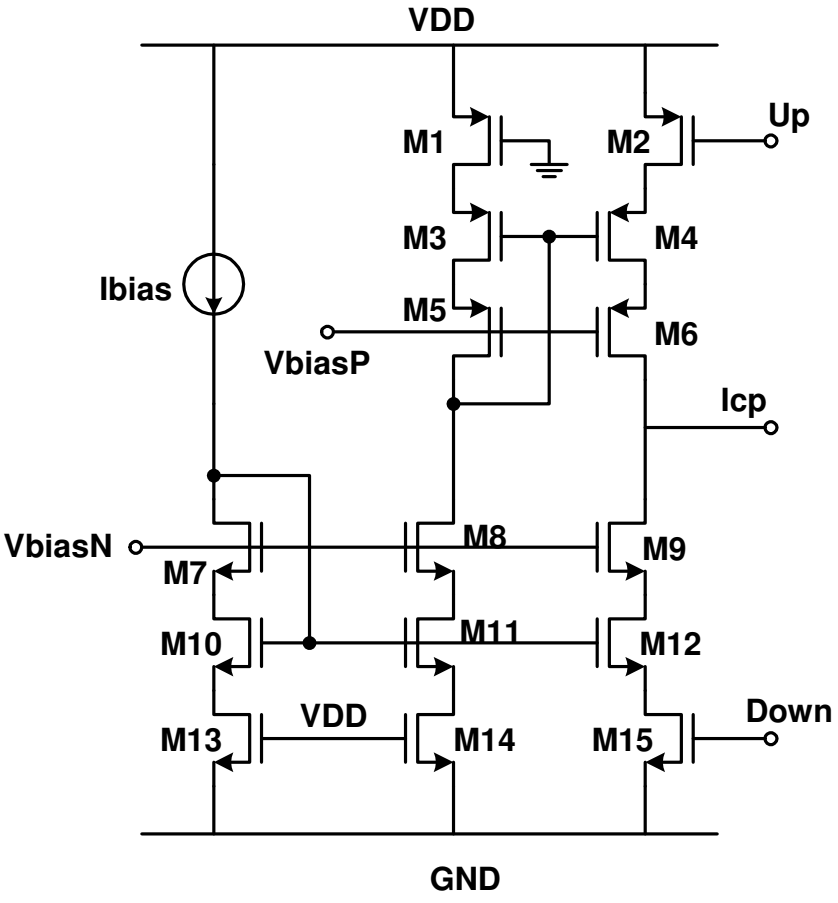


Figure 14 Charge Pump Implemented

3.2.4 Loop Filter

The loop filter is a critical building block because it determines the loop dynamics as well as the stability of the loop. The structure shown in Figure 15 is traditionally used for the loop filter.

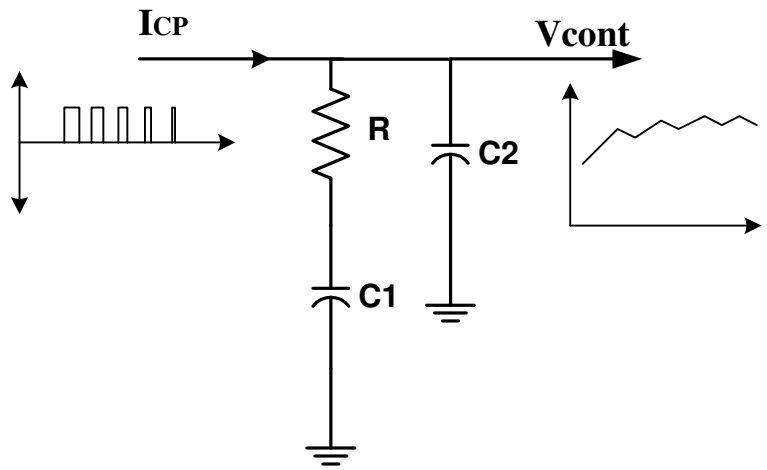


Figure 15 Traditional Low Pass Filter Structure

This structure has many advantages. The most significant is that there is no direct DC path to ground. Therefore, the current leakage is zero, and the DC gain is infinite. Ideally, if the DC gain of the filter is infinite, then the phase error at steady state is zero. The resistor in this structure determines the damping factor and also adds a zero for stability purposes.

The transimpedance of the filter can be expressed as:

$$Z(s) = \frac{V_{CONT}}{I_{CP}} = \frac{R(1 + sRC_1)}{s\left[R^2 C_1 C_2 s + R(C_1 + C_2)\right]} \tag{22}$$

A zero is located at:

$$\omega_z = \frac{1}{RC_1} \tag{23}$$

One pole is located at DC and the other one at:

$$\omega_{p2} = \frac{1}{R\dfrac{C_1 C_2}{C_1 + C_2}} \tag{24}$$

The second pole can be approximated to $1/RC_2$ if $C_1 >> C_2$.

A typical plot of the transimpedance is seen in Figure 16

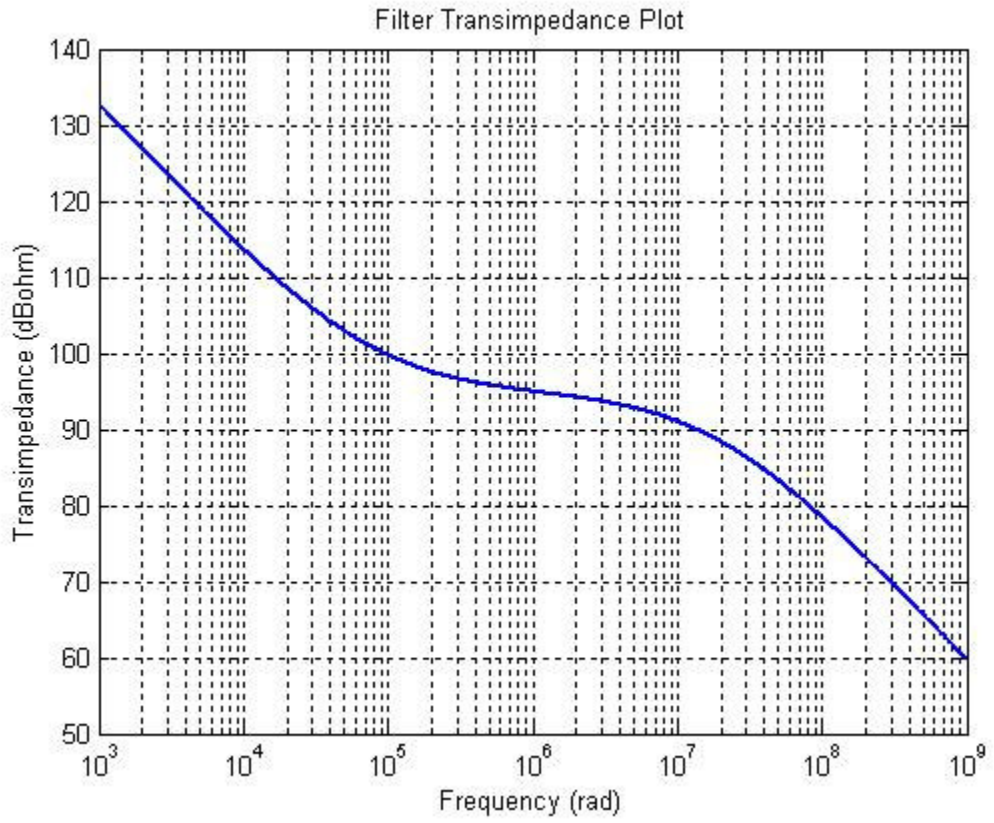


Figure 16 Second Order Loop Filter Transimpedance Plot

The closed loop equation given in (6) along with (9) and (10) can be re-written as:

$$H(s) = \frac{N\left(2\zeta\omega_n s + \omega_n^2\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (25)$$

The phase margin of the loop is found as:

$$PM = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \qquad (26)$$

where ω_c is the crossover frequency and it can be shown that the maximum phase margin can be achieved when the following condition is met [12]:

$$\omega_c = \sqrt{\omega_z \cdot \omega_{p2}} = \omega_z \sqrt{\frac{C_1}{C_2} + 1} \tag{27}$$

Setting the closed-loop transfer function $\left|H_{cl}(j\omega)\right|^2 = \frac{1}{2}$, the 3dB bandwidth of the PLL relating to ω_n is as follows:

$$\omega_{3dB} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{\frac{1}{2}} \tag{28}$$

The system needs to have a phase margin of greater than 45º to be stable. In Figure 2.20 of [12], the relationship between maximum PM and C_1/C_2 ratio is plotted. A higher PM denotes less overshoots and peaking. The optimum transient response can be achieved at a phase margin of 65º. For a phase margin of ~65º, $C_1/C_2 = 20$. However, it also demands larger capacitor values which require larger silicon areas. A phase margin of 55º is chosen to minimize capacitor size and the system is still stable. The same plot shows that $C_1/C_2 = 10$ for a PM of 55º. This C_1/C_2 ratio means that the second pole is located at more than 1 decade away from the zero.

When finding the value for the filter components, the filter needs to be analyzed with the charge pump. For a first order approximation, the transfer function of the charge pump from the input of the charge pump to the output of the PLL is derived as follows:

$$H_{cp}(s) = \frac{\theta_{out}(s)}{\theta_{cp}(s)} = \frac{K_{PD}K_v R\left(s + \frac{1}{RC_1}\right)}{s^2 + s\frac{K_{PD}K_v R}{N} + \frac{K_{PD}K_v}{NC_1}} \tag{29}$$

Since $K_{PD} = \frac{I_{cp}}{2\pi}$, where I_{cp} is the charge pump current, the charge pump transfer function becomes:

$$H_{cp}(s) = \frac{\theta_{out}(s)}{\theta_{cp}(s)} = \frac{\frac{I_{cp}}{2\pi} K_v R\left(s + \frac{1}{RC_1}\right)}{s^2 + s\frac{I_{cp} K_v R}{2\pi N} + \frac{I_{cp} K_v}{2\pi N C_1}} \tag{30}$$

From above equations, it can be seen that

$$\omega_n = \sqrt{\frac{I_{cp} K_v}{2\pi N C_1}} \tag{31}$$

$$\zeta = \frac{\omega_n R C_1}{2} \tag{32}$$

The above equations are used in the next section to find the values of C_1, C_2, and R.

3.2.5 Voltage Controlled Oscillator

There are several considerations for the design of this VCO. One concern is that the VCO needs to have differential outputs. In order to minimize LO frequency feed through for the mixer, the balanced Gilbert cell structure is used (discussed in the next section). The Gilbert cell structure requires that the input from VCO to be differential. Another concern is the gain of the VCO. Intuitively, if the VCO gain is too large, any small variation in the control voltage (from noise and reference feedthrough) can put the system out of lock and increase further both phase noise and spurs. By looking at the following equation, $K_v = \frac{2\pi(Frequency\_Range)}{Input\_Voltage}$ the gain of the VCO depends on the input control voltage. The larger the input control voltage range is, the smaller the gain of

the VCO will be. However, the input control voltage range is limited by the power supply.

There are many different options available for the structure of a VCO. LC-tank oscillators are widely used for their low phase noise performance. However, the tuning range for a LC oscillator is limited to +/- 15%. The LC oscillator also requires the layout of an inductor. Since the system designed is to be used as part of an on-chip BIST structure, an inductor would take a large area. Another structure is the ring oscillator based VCO. The ring oscillator is favored for many PLL applications due to its simplicity, low power consumption and wide tuning range. The VCO tuning range is 100MHz which is 25% of 400MHz. In order to reach such a large turning range, a ring oscillator structure is used. The drawback to using this structure is that it can produce a large phase noise. However, since the phase noise does not affect the application of the frequency synthesizer, it is not relevant.

The basic ring oscillator structure is shown in Figure 17.

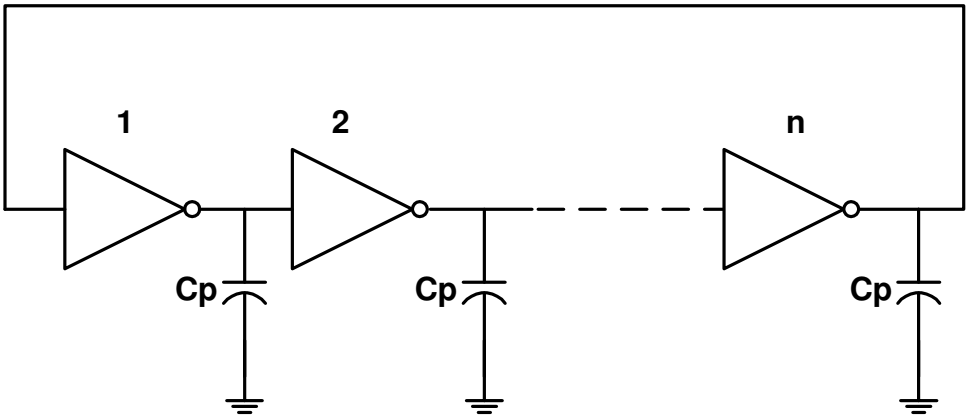


Figure 17 Ring Oscillator

Each inverter acts as a delay and n is the number of stages. For a single-ended structure, n is an odd integer; for a differential structure, n is any integer. The frequency of oscillation is inversely proportional to the delay of each cell. The capacitors drawn are parasitic capacitances.

The closed loop transfer function is seen as:

$$H_{v,cl}(s) = \frac{H_{v,ol}(s)}{1 - H_{v,ol}(s)} \tag{33}$$

The oscillation occurs when the open loop gain is 1:

$$\left|H_{v,ol}(s)\right| = 1 \tag{34}$$

The open loop gain of the VCO is the product of all the delay cells (inverters). If all delay elements are identical, the overall open loop transfer function is:

$$H_{v,ol}(s) = \left[H_d(s)\right]^n \tag{35}$$

where $H_d(s)$ is the transfer function of a single delay cell.

The oscillator will oscillate if:

$$\left|H_d(j\omega_{osc})\right| = (-1)^{1/n} \tag{36}$$

A one-pole delay cell has the following transfer function:

$$H_d(j\omega) = \frac{A_o}{1 + \frac{j\omega}{\omega_p}} \tag{37}$$

where A_o is the gain of the delay cell and ω_p is the pole, then

$$\frac{A_o}{1+\frac{j\omega_{osc}}{\omega_p}} = e^{\pm\frac{j\pi}{n}} \tag{38}$$

The ratio of ω_{osc} and ω_p relates to the phase as follows:

$$\frac{\omega_{osc}}{\omega_p} = \tan\left(\frac{\pi}{n}\right) \tag{39}$$

For a 5-stage oscillator, the gain of the delay cell can be calculated as:

$$A_o^2 = 1+\left(\frac{\omega_{osc}}{\omega_p}\right)^2 \Rightarrow A_o \approx 1.23 \tag{40}$$

The gain of the delay cell needs to be greater than 1.23 in order for the system to oscillate.

If τ_d is the delay of a single element, then the oscillation frequency is found as [13]:

$$f_{osc} = \frac{1}{2n\tau_d} \tag{41}$$

The delay needs to be between 0.25 and 0.2ns for a 5-stage VCO output between 400-500MHz.

Since the VCO is required to have differential outputs, a simple inverter design will need to be modified. The delay element illustrated in Figure 18 [14] that has a source coupled NMOS pair with active PMOS resistive loads called symmetric loads.

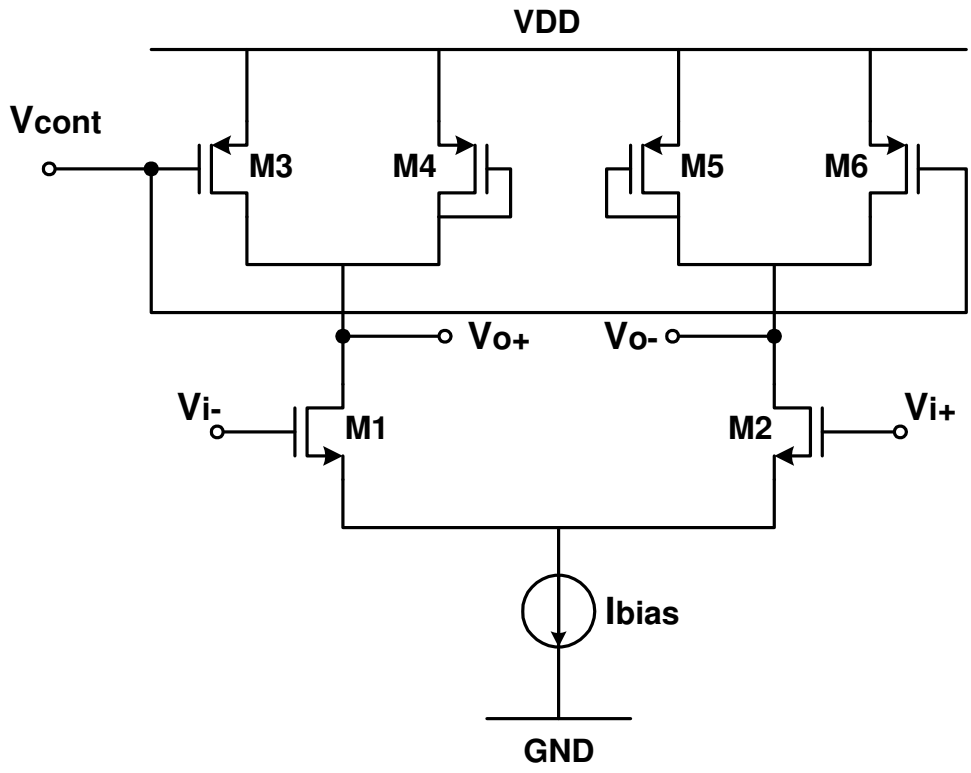


Figure 18 CMOS Delay Element

The structure is fully differential and the following analysis is performed on one side of the structure comprised of transistors M1, M3-4. The analysis of transistors M2, M5-6 will be similar. The loads are composed of a diode-connected PMOS transistor, M4, in parallel with another PMOS device M3 that is controlled by the VCO control voltage. The diode-connected PMOS M4 gives an equivalent output resistance of $\frac{1}{g_m}$. The currents through transistor M3 and M4 sum up to the current flowing through transistor M1, which is half of the bias current when the inputs are equal. When V_{cont} changes, the V_{GS} of transistor M3 also changes causing the current of M4 to change. Since the gm of M4 is directly proportional to the square root of the current flowing through the transistor, the gm also changes. The total resistance and capacitance at the

output node controls the oscillation frequency. It is shown in the next section that if the gm of M4 changes, the total output resistance changes, thus the oscillation frequency changes. The design of the delay element is discussed in section 4.

The implementation of the VCO is shown in Figure 19, where all delay elements are identical and use the architecture from above.

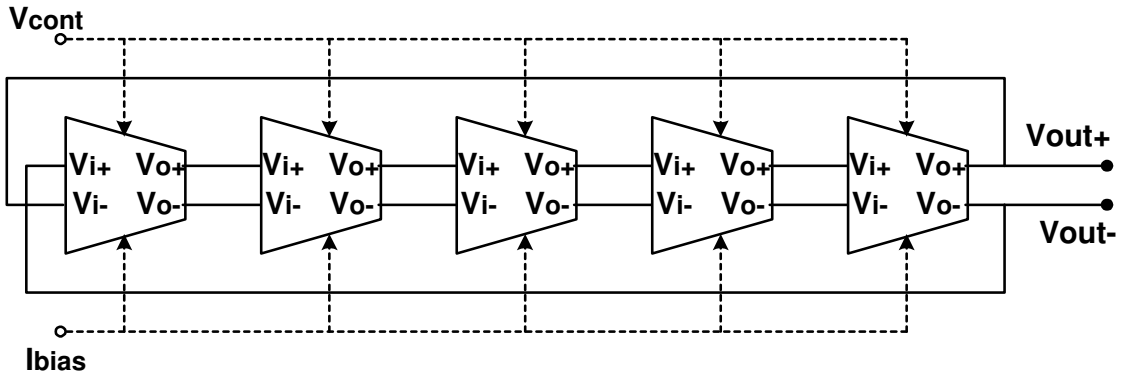


Figure 19 Implementation of VCO

3.2.6 Loop Divider

The output frequency of the PLL is N times the input reference frequency. In order to compare the phase and frequency of the reference and the PLL output, a programmable loop divider is used. The loop division ratio, N, is programmable. A common design of the integer loop divider is the pulse swallow frequency divider [15] shown in Figure 20.

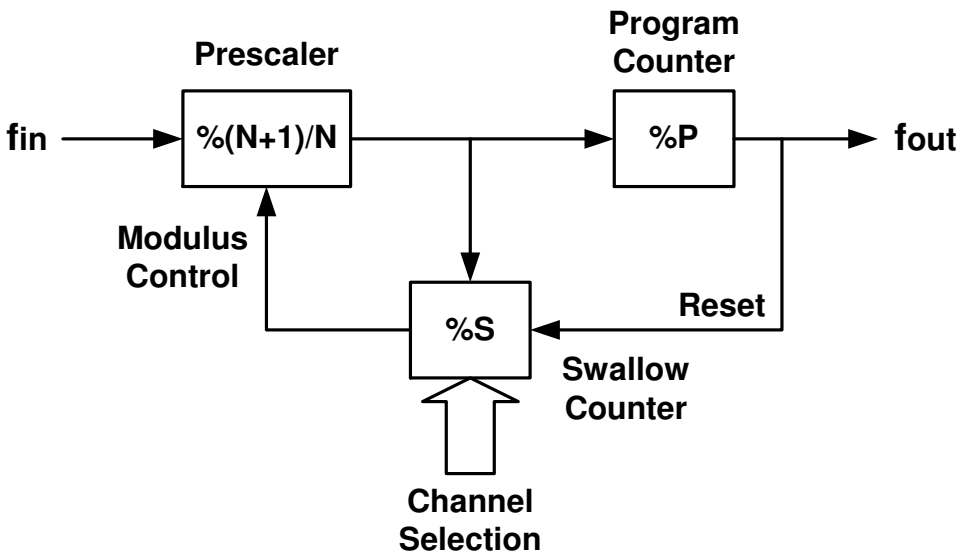


Figure 20 Pulse Swallow Frequency Divider

After the counter is reset, the prescaler divides the input by N+1. The output of the prescaler is then divided by both the program counter and the swallow counter until the swallow counter counts S pulses. The prescaler then divides the input by N until the program counter is full. Since the program counter already counted S pulses before the prescaler division changed, only P-S pulses are required before the program counter is full. The counter is then reset and the operation continues. The divider outputs one complete cycle for every $(N+1)S+(P-S)N = NP+S$ cycles from the input. The pulse swallow frequency divider generates the output as:

$$f_{out} = (NP+S)f_{in} \tag{42}$$

The operation of the programmable divide-by-N counter can be described as follows. The number of divide-by-two counter is the number of bits needed to represent the largest loop divider number. The programmable input is represented in binary number as $B_nB_{n-1}\ldots B_1B_0$. The output of all such counters is fed to an end-of-counter (EOC)

detector. The counter counts down from a certain given number, N, until it reaches zero. When the counter reaches zero, the EOCB is the invert of EOC and it signals a reset circuit to initialize the counter back to N (Figure 21).

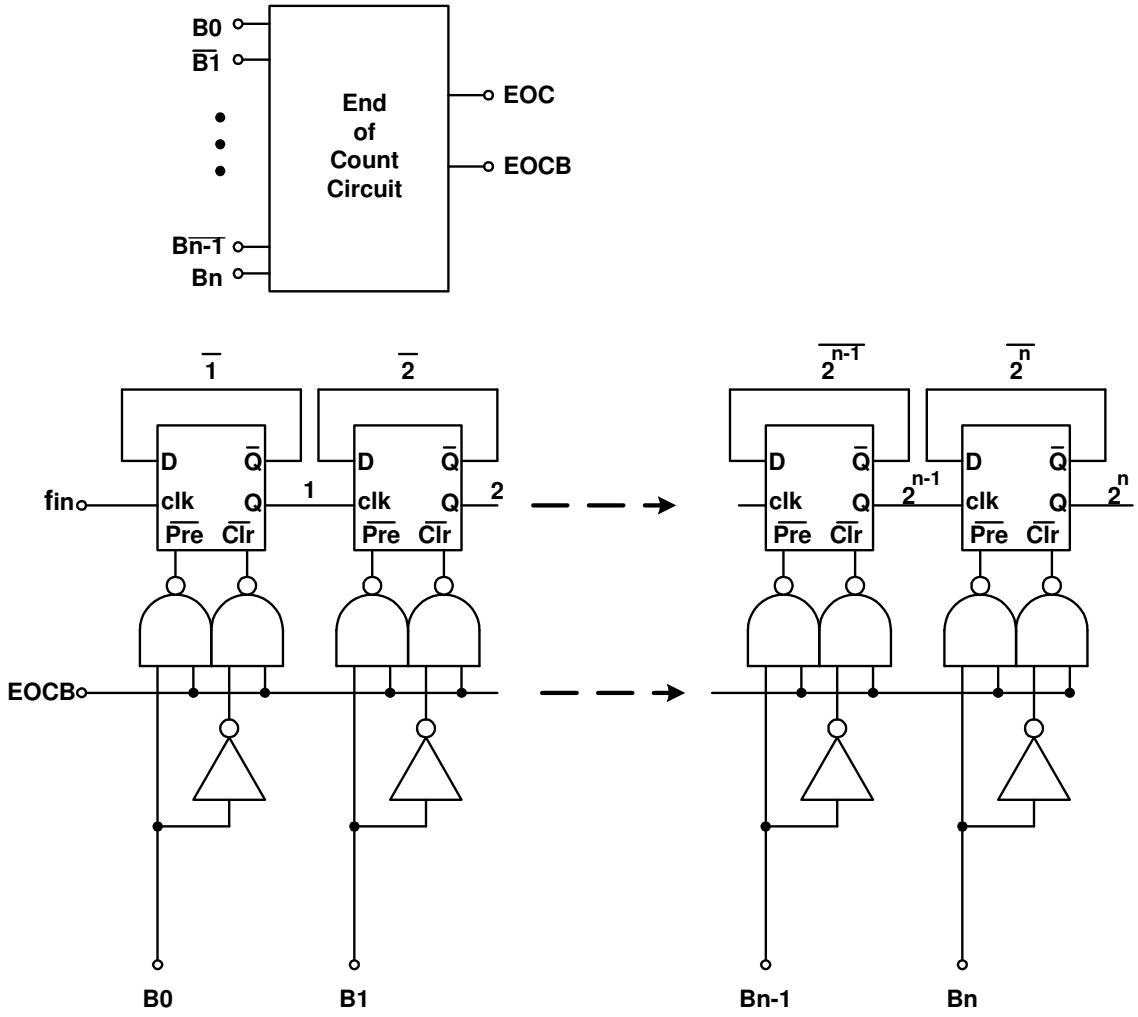


Figure 21 n-bit Programmable Counter

There are two main problems to implementing the EOC circuit: number of inputs needed and speed of operation. N-input AND gates, where N>2, have lousy performance in terms of speed. Multiple 2-input NAND and NOR gates are used instead to increase

the speed. The actual implementation of the EOC also includes an extra 1-bit register. The EOC detects when the count reaches below 2. The circuit detects the 00…00x state instead of the 00…00 state. The reset signal is triggered before the count reaches to 0 to speed up the operation [16]. The implementation of the counter is shown in Figure 22.

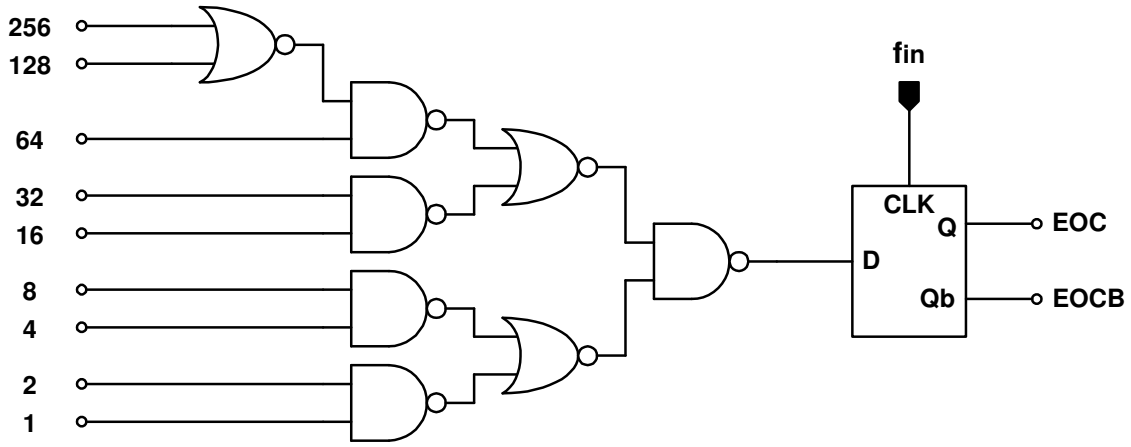


Figure 22 End of Count Circuit

An unexpected problem occurred when designing the counter at the frequency which the digital components of the loop divider are working. The loop divider needs to divide the PLL output that is between 400-500MHz by N. The minimum dimension digital transistors in the 0.5µm technology can not run up to that speed. A solution to this problem is to add a divide-by-2 prescaler to slow down the divider input frequency. However, the prescaler changes the overall loop division ratio. If the output of the VCO remains at 400-500MHz and the programmable divider is running at 400-500, then the overall loop divider ratio is increased to twice the programmable divider ratio of 800-

1000. The relationship between the reference and the output of the PLL is seen in (1), where the output frequency is N times the input frequency. In order to keep the frequency step as 10kHz, and the PLL output frequency as 400-500MHz, the input reference needs to be decreased by a factor of 2 to 500KHz. The change of the input reference frequency can change the entire loop dynamics. The overall loop stability analysis is performed in section 4.

3.3 Additional Blocks

3.3.1 Frequency Down-Converter

The output of the PLL has a frequency range of 400-500MHz. The desired frequency is from 10K-100MHz. A frequency down-converter is needed. A common frequency down-converter is a mixer. A mixer performs frequency translation by multiplying two signals. The RF port receives the signal to be down-converted (PLL output) and the LO port receives the signal from an oscillator (400MHz).

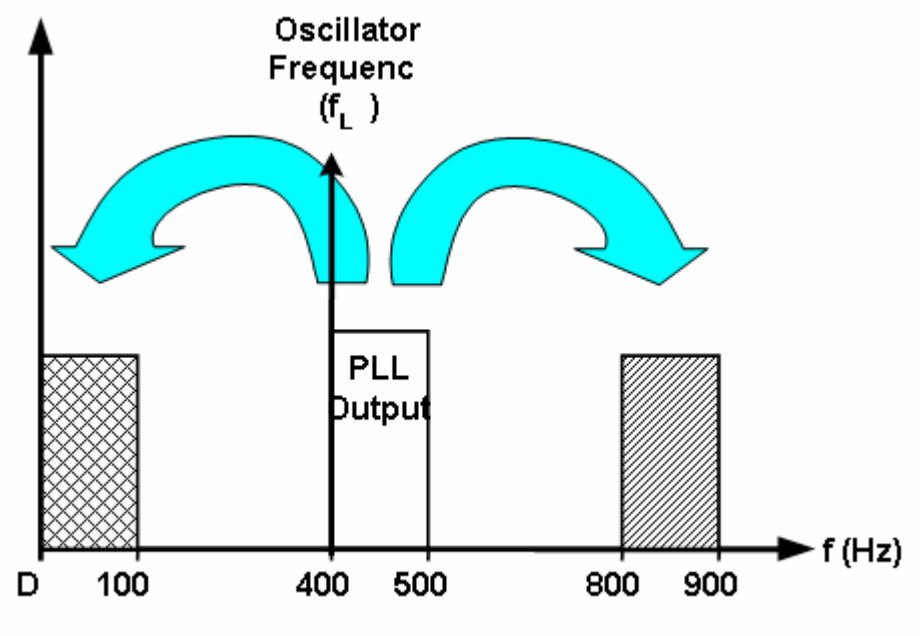


Figure 23 Frequency Spectrum of Mixer Operation

Figure 23 illustrates the down-conversion by the mixer. To see the operation of the down-conversion, the harmonics are neglected. The PLL output frequency is mixed with a fixed oscillator frequency of 400MHz. The band of frequencies is down-converted to DC-100MHz as well as up-converted to 800-900MHz.

Since the down-conversion is a single-side band act (the desired signal spectrum is located on one side of the LO frequency) [15], the down conversion itself causes the signal to noise ratio to decrease by 3dB. For illustration purpose, assume a noiseless mixer. Figure 24 demonstrates the relations of the input spectrum and the output spectrum.

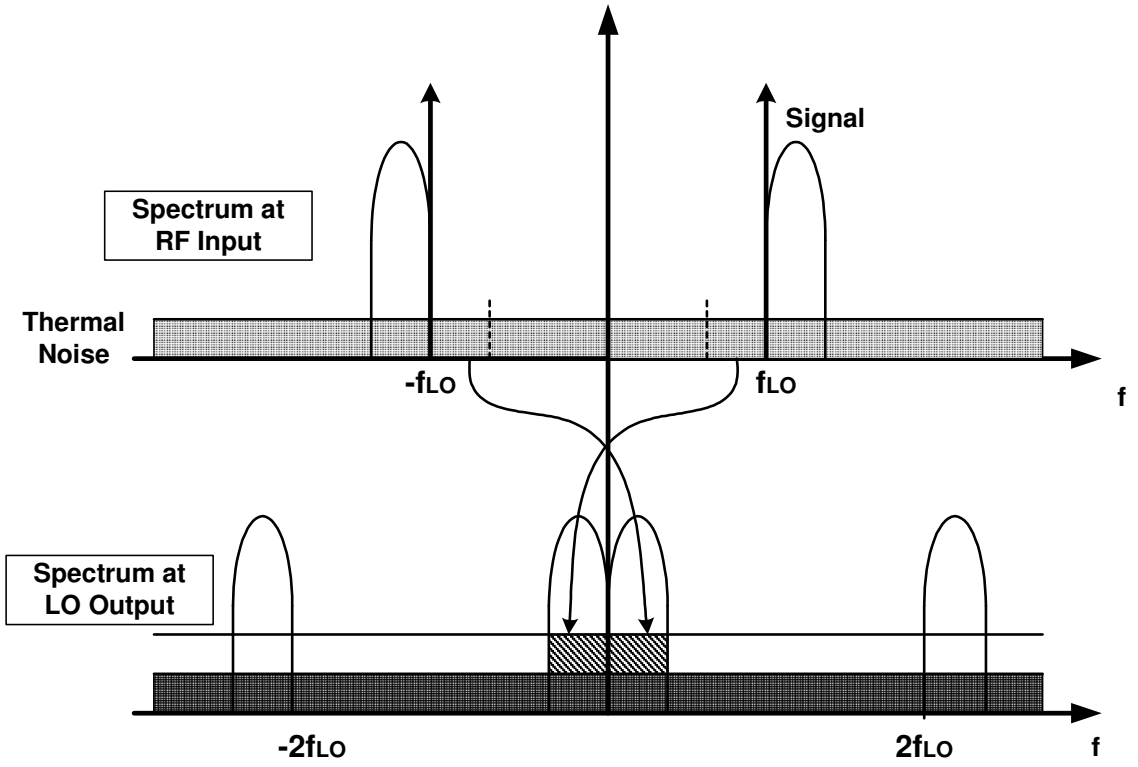


Figure 24 Folding of RF and Image Noise into IF Band

When the signal is translated into the IF frequency, the thermal noise from both the signal band and the image band are translated to the IF frequency and the total thermal noise doubles. The signal to noise ratio, SNR, is defined as the power of the signal divided by the power of the noise. If the noise density doubles and the signal stays constant, the output SNR degrades by 3dB.

The output of the VCO will have a frequency range of 400-500MHz. Since the desired system output frequency is between 10KHz and 100MHz, the intermediate frequency (IF) range will be set to between DC and 100MHz and the LO frequency is fixed to 400MHz.

There are two configurations of mixers: single-balanced and double-balanced. In a single-balanced structure, a MOS transistor converts the RF input to a current and feed

into a pair of differential transistors act as switches. The switching pair, driven by the differential LO signal, steers the current created by the RF transistor to one side or the other then amplifies the LO signal. The result is a mixing of the RF and LO frequencies. [16] gives a qualitative analysis of a single-balanced mixer. It also shows that a single-balanced structure displays less input referred noise than a double-balanced structure for a given power dissipation. Ideally, this structure should give only the IF frequencies. However, due to non-instantaneous switching of the currents, f_{LO} will also show up at the output. This is called a LO-IF feedthrough. In order to mitigate the affect of this feedthrough, a double-balanced structure (Gilbert cell) is used (Figure 25).

This structure is essentially two single-balanced structures with the RF transistors in parallel and the LO transistors connected according to the sign. Transistors M1 and M2 convert the RF signal to currents and the currents then flow to M3-M6. Transistors M3-M6 switch the currents from one side to another providing opposite phases. Transistors M7-8 are active loads. If LO is a square wave with 50% duty cycle, the symmetry causes even-order harmonics to cancel and drop out of the LO spectrum, thereby achieving a first-order frequency cancellation.

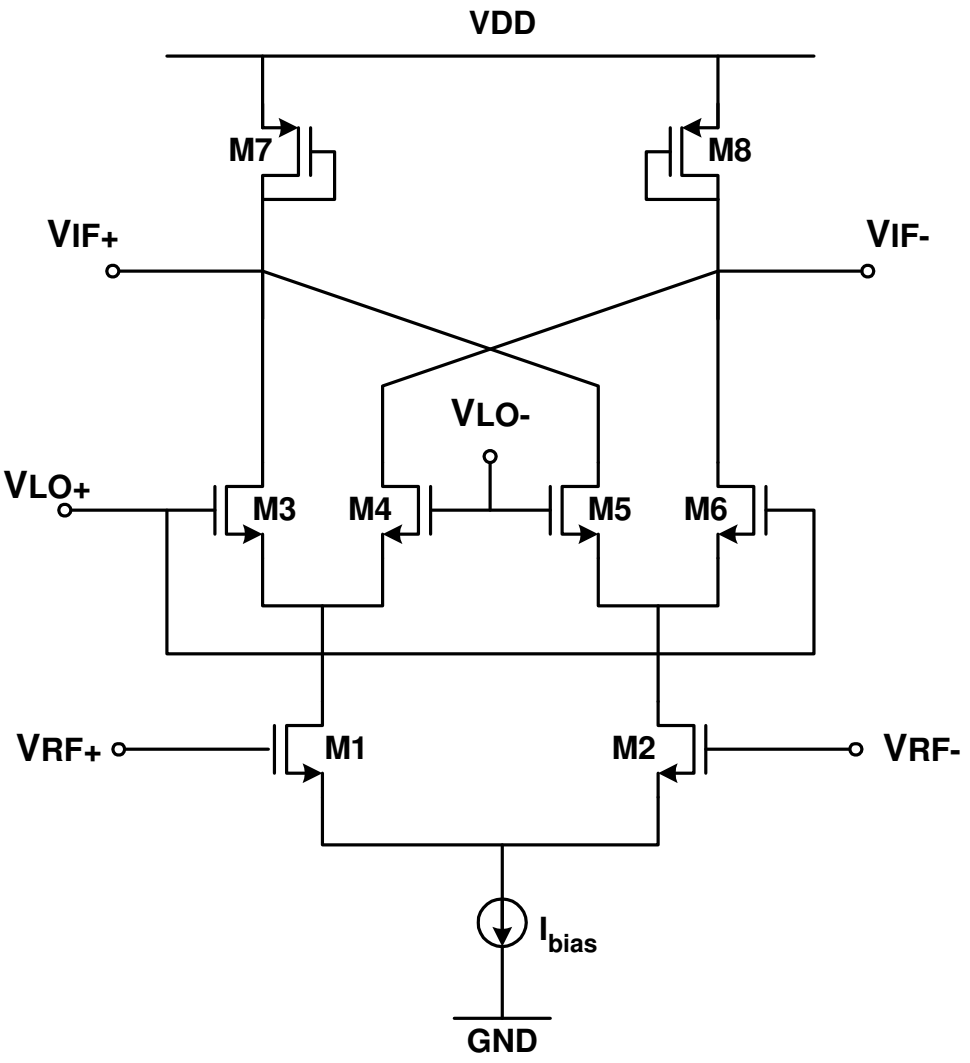


Figure 25 Gilbert Cell Mixer Structure

The desired output from the system is the first band of frequencies. Therefore a low-pass filter is needed to eliminate the unwanted frequencies. A low pass filter is placed at the output of the mixer to remove frequencies higher than 100MHz. A simple second order passive RC filter (Figure 26) is used.

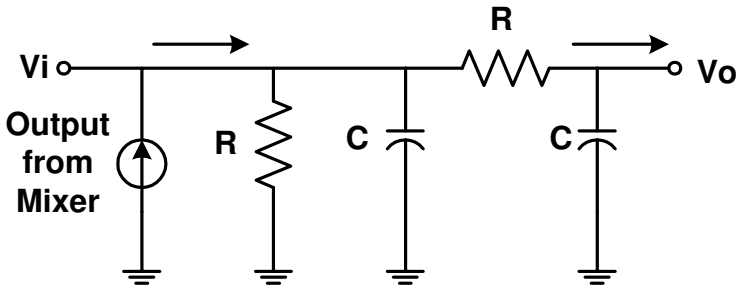


Figure 26 Second-order RC Low Pass Filter

This filter has the following transfer function:

$$H_{LP2}(s) = \frac{V_o}{V_i} = \frac{\frac{1}{(RC)^2}}{s^2 + \frac{3}{RC}s + \frac{1}{(RC)^2}} \tag{43}$$

Clearly, this filter has two poles and gives a -40dB/dec attenuation. When mixing the VCO signal with a 400MHz signal, we will get a (f_{vco}+400MHz) component and a (f_{vco}-400MHz) component plus harmonics. Since the (f_{vco}+400MHz) component will be at least 800MHz, it will be attenuated by close to 40dBs. This attenuation will be sufficient in suppressing the unwanted component. RF and LO frequencies will still be present at much weaker signal strength. Since both frequencies are above 400MHz, they will also be attenuated.

3.3.2 Output Selector

The output selector receives the output of the down-converter and sends to two different paths (Figure 27).

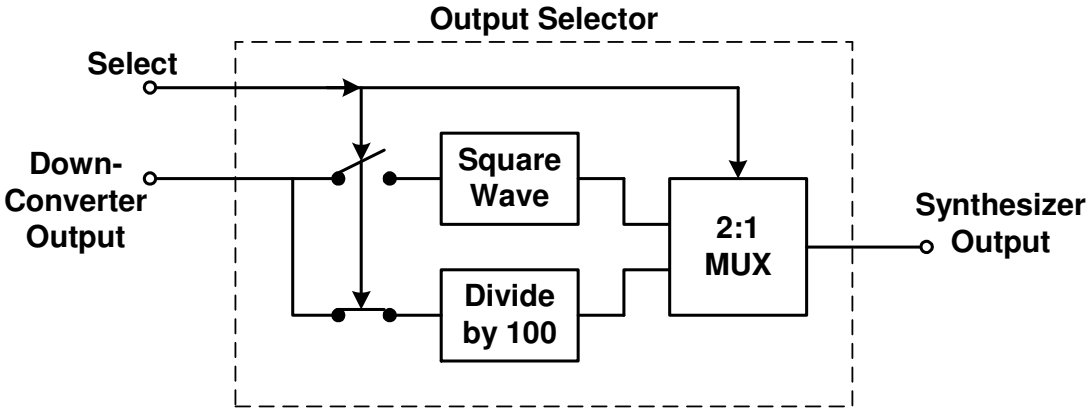


Figure 27 Output Selector Block Diagram

The input *Select* chooses the output to be either greater than or less than 1MHz. The top signal path goes through a square wave converter that changes the sine wave of from the down-converter output to a square wave by using inverters. It gives a frequency range of 1-100MHz with a resolution of 1MHz. The bottom signal path goes through a divide-by-100 fixed digital divider. The output is a square wave form of frequency range 10KHz-1MHz with a resolution of 10KHz. The 2:1 MUX chooses from the two signal paths controlled by input signal *Select*. The output of the 2:1 MUX is the output of the frequency synthesizer. The following block diagram illustrates the complete structure of the frequency synthesizer.

4 DESIGN CONSIDERATIONS AND SIMULATED RESULTS

4.1 Stability Analysis

There are several parameters that need to be established before performing the stability analysis. First of all, the VCO tuning range needs to be determined. For this frequency synthesizer, the frequency range of the PLL is set to be between 400MHz and 500MHz. As stated in section 3, if the VCO gain is too large, the system is more sensitive to phase noise. In order to allow some margin at both ends of the spectrum, the actual operating VCO frequency range is set to 350-550MHz. The control voltage is set to 1.6V to allow enough overhead for the transistors to be in the saturation region. The gain of the VCO can be calculated as:

$$K_v = \frac{2\pi(200MHz)}{1.6V} = 750Mrad/sV \tag{44}$$

Secondly, the loop division ratio needs to be determined. The value of N in the loop analysis affects the stability. Since the value of N varies about 25%, a mean value can be used providing both ends of the range are checked as well to insure stability.

$$N_{mean} = \sqrt{N_{\min} N_{\max}} = 894 \tag{45}$$

The loop filter is a critical part of the PLL because it controls the loop dynamic as well as the stability of the system. Due to the constraint of the high division ratio, the loop crossover frequency is set to less than 10% of the reference frequency [11]. A 25% lower loop bandwidth is used to allow sufficient margins for process and temperature variations.

$$\omega_{3dB} = (0.75)(2\pi)(0.1)(500KHz) = 235.6krad/s \tag{46}$$

ω_n is calculated from 33 as $\omega_n/2.06$.

$$\omega_n = \frac{\omega_{3dB}}{2.06} = 114.4krad/s \tag{47}$$

The charge pump current is set to 10μA, and the loop filter components are calculated as:

$$C_1 = \frac{I_{CP} K_{VCO}}{2\pi N \omega_n^2} = 227\,pF \tag{48}$$

$$R = \frac{2\zeta}{\omega_n C_1} = 54.4K\Omega \tag{49}$$

$$C_2 = \frac{C_1}{10} = 27.7\,pF \tag{50}$$

Using Matlab (see details in Appendix A), the open-loop frequency response is plotted in Figure 28.

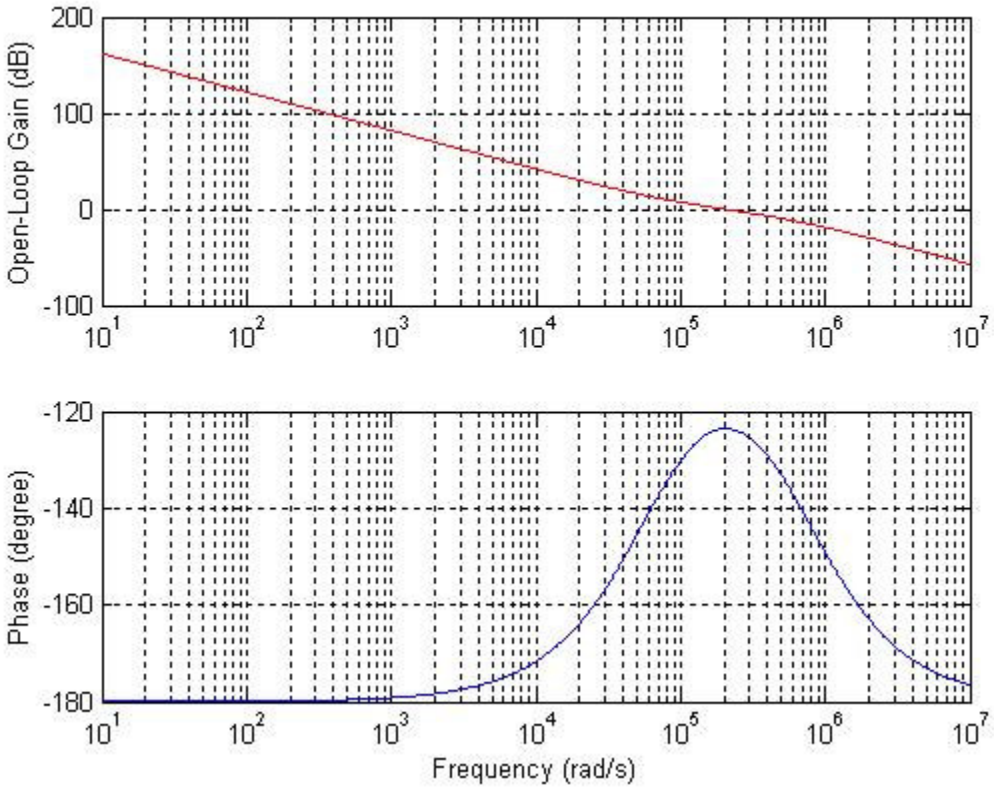


Figure 28 Open-Loop Response

The above plot shows the open-loop frequency response. The x-axis shows the frequency in rad/s; the y-axis on the top shows the open-loop gain in dB and the bottom y-axis shows the phase in degrees. The crossover frequency (which is the frequency where the open-loop gain crosses over 0dB gain) is ~115Krad/s and the phase margin (180degrees minus the phase of the loop at crossover frequency) is 55° as calculated previously. Since the phase margin is greater than 45 degrees, and the gain of the feedback is large, the system is stable. The step and impulse response are still performed to check the settling of the system.

The frequency impulse and step response are plotted using Matlab (see details in Appendix B). A step variation in phase is an impulse variation in frequency. From Section 3, it is demonstrated that the error introduced from a step in phase or a frequency impulse at the input reaches zero eventually and the system is stable. The phase step (frequency impulse) response plotted below in Figure 29. The x-axis is time and the y-axis is the magnitude of the error. The final error of the PLL settles to 0 with a settling time of approximately 100μsec.

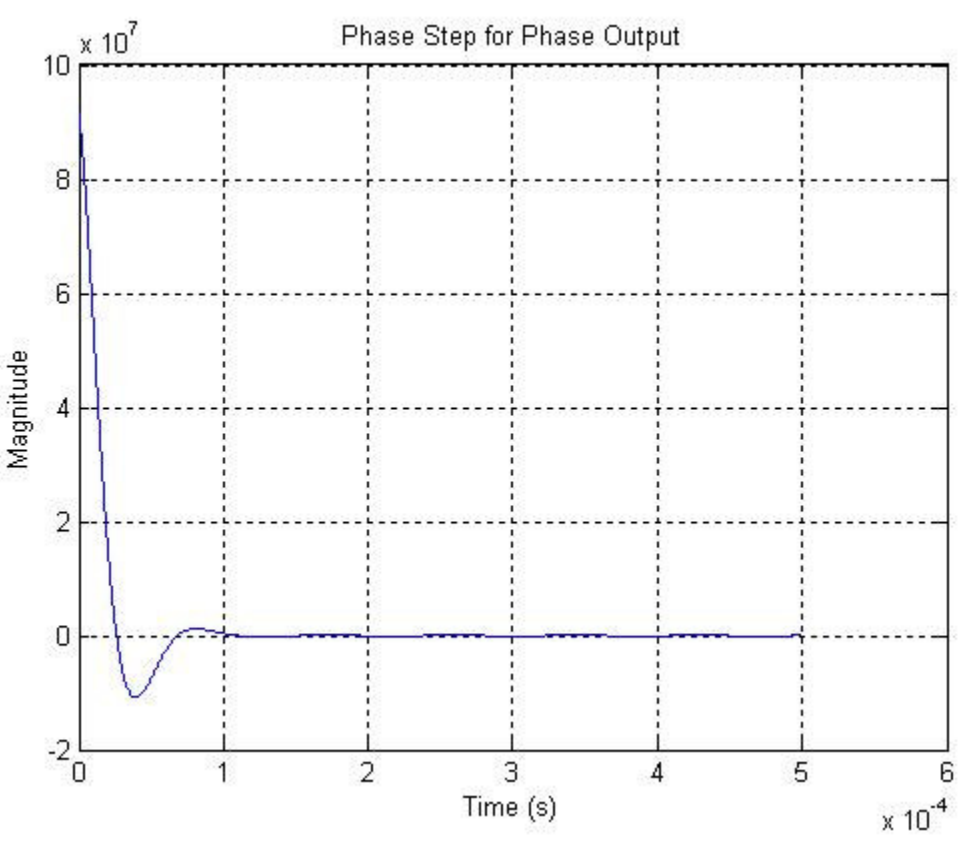


Figure 29 Phase Step Response for Fref=500KHz

A step variation in frequency is a ramp variation in phase. It is also demonstrated in Section 3 that the error introduced from a ramp input in phase or a frequency step settles to the non-zero value of $\frac{\Delta\omega}{K_{PD}K_V K_F \omega_z}$. The phase ramp frequency step response plotted below in Figure 30 such that the final error of the PLL follows the shape of the input ramp and never reaches zero.

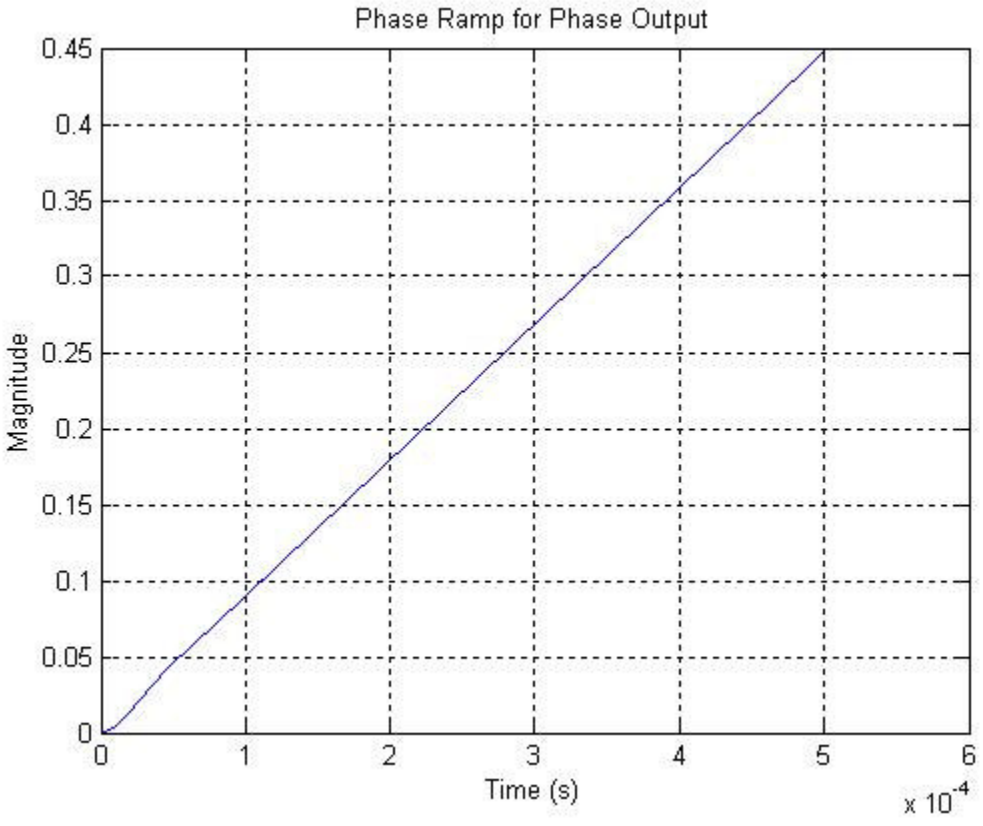


Figure 30 Phase Ramp Response for Fref=500KHz

4.2 PLL Design

The design of all transistors use the following parameters found in the AMI05 process:

$K_n = 58.1\mu A/V$
$K_p = 18.8\mu A/V$

$V_{Tn} = 0.7V$
$V_{Tp} = -0.9V$

$C_{OX} = 2.45 \times 10^{-3} F/m^2$

4.2.1 Phase Detector

The phase detector is composed of all digital elements. A slightly modified common PFD architecture (see Figure 11) is used. The D-flip flops are identical and implemented in Figure 31.

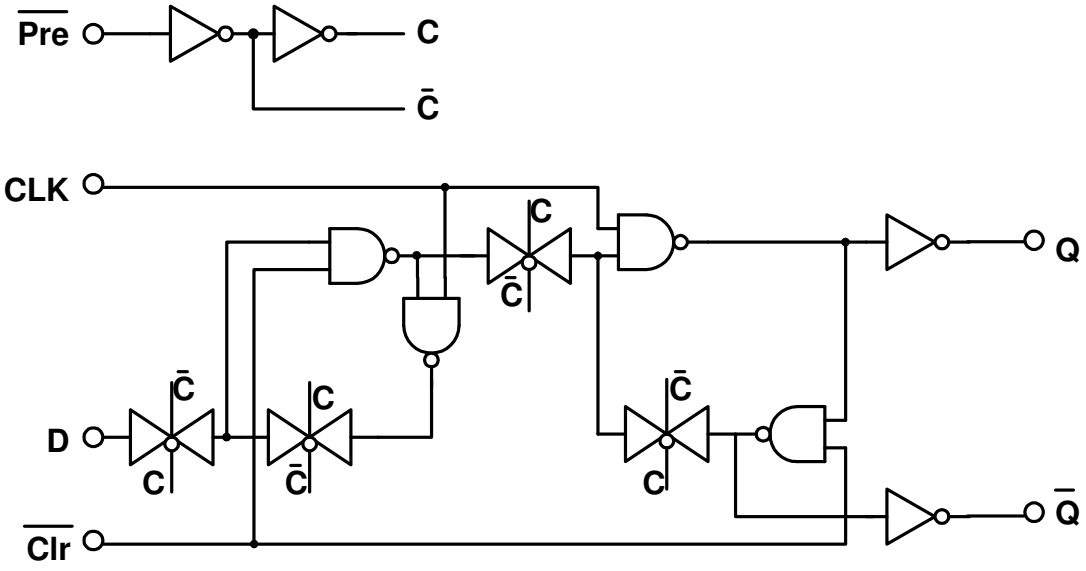
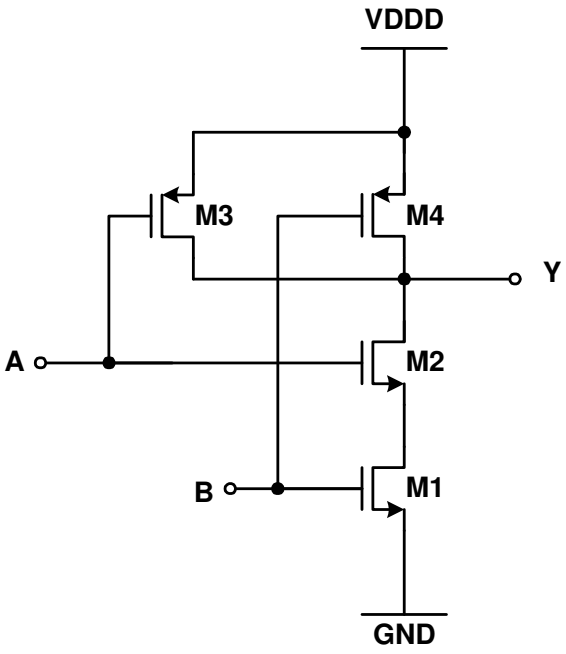
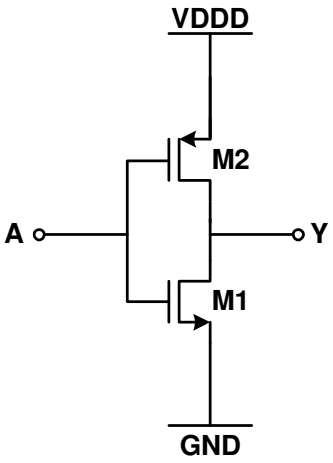


Figure 31 D-Flip Flop Implementation

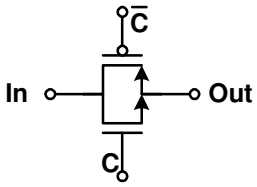
The NAND gates, inverters, and transmission gates are implemented in Figure 32.



a) NAND



b) Inverter



C) Transmission

Figure 32 Digital Gate Implementation

All NMOS transistors have minimum dimensions of W/L = 1.5/0.6µm and PMOS transistors have dimensions of W/L = 4.5/0.6µm to compensate for lower mobility and cause the rising time approximately equal to the falling time. The simulation below shows the output of the PFD with an input reference of 500KHz.

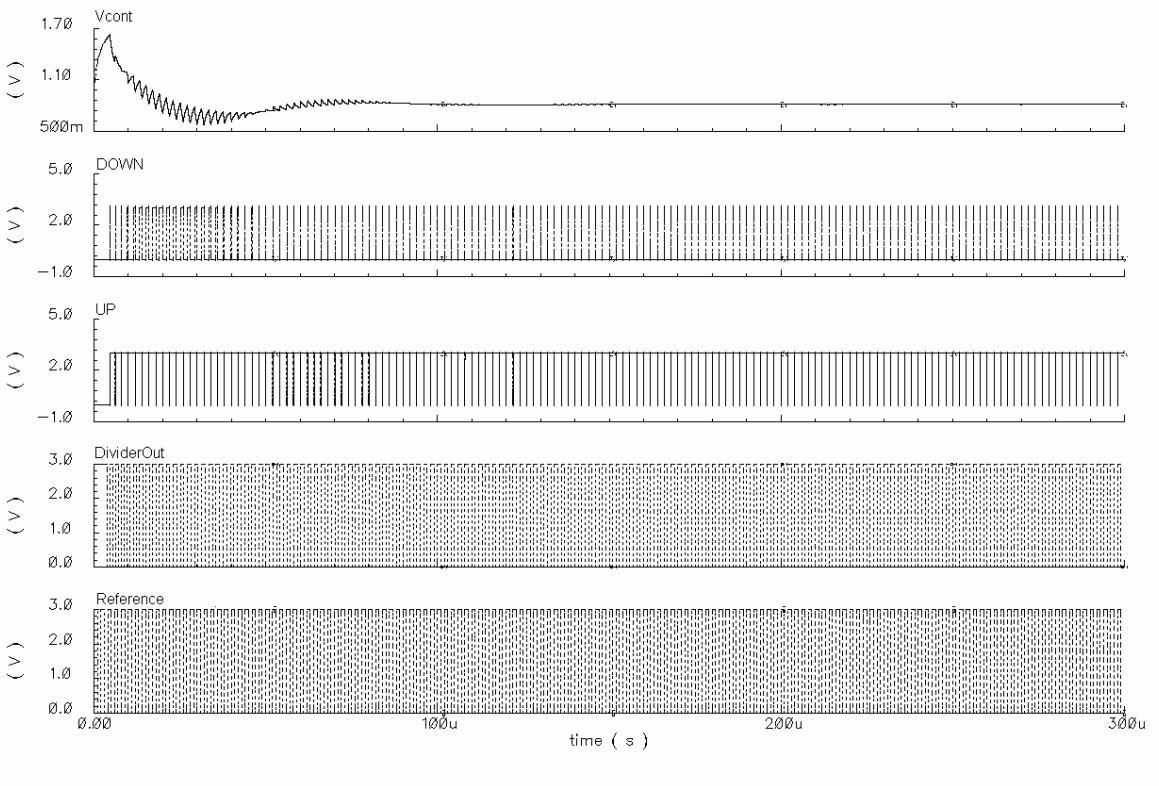


Figure 33 PFD Output

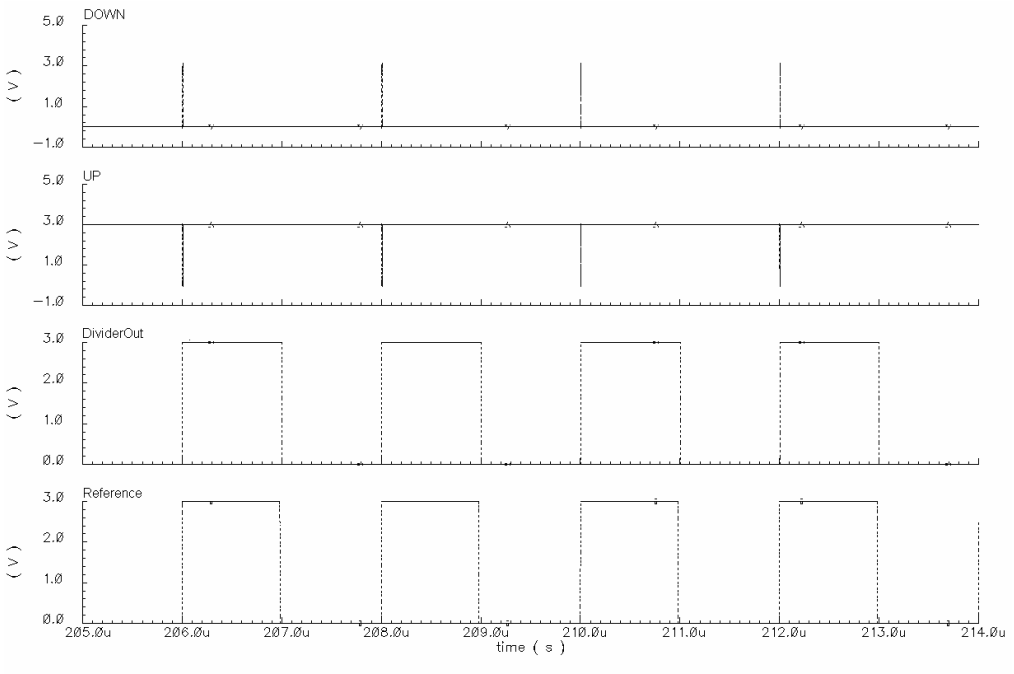


Figure 34 Zoomed PFD Output When Loop Is Locked

When the reference phase leads the divider output, the output *Up* switches on high. Similarly, when the divider output phase leads the reference, the PFD switches *Down* on high. Figure 33 shows that the system settles after 100µs. Figure 34 is a zoomed depiction of the PFD output when the system is locked. A short pulse is generated when the reference input aligns with the divider output in both phase and frequency. The narrow pulses from UP and DOWN prevent dead zone when the system is locked.

4.2.2 Charge Pump

The charge pump implemented in this PLL overcomes the drawbacks of a traditional charge pump that has low output resistance, low PSRR and poor isolation between UP/DN and the output [12]. The structure is shown in Figure 14.

A length of 1.2µm is used in order to reach larger output resistance. The Up/Down switches are located close to the rails to ensure that the switch resistance is very small when "on" for faster switching time. The V_{DSAT} of the transistors is set to 0.2V in order to maximize the output voltage and the current is 10µA. Using (51) below, W/L ratios are computed as $\left(\frac{W}{L}\right)_n \approx 4$ and $\left(\frac{W}{L}\right)_p \approx 12$.

$$V_{DSAT} = \sqrt{\frac{I_D}{\frac{K}{2}\cdot\frac{W}{L}}} \qquad (51)$$

Through simulations, the switches are sized such that the Up and Down branch have similar speed. Table 1 shows the dimensions of the transistors.

Table 1 Charge Pump Transistor Dimensions

	M1-M2	**M3-M6**	**M7-M12**	**M13-M15**
W(µm)	6.3(x2)	6.3(x2)	2.85(x2)	1.8(x2)
L(µm)	0.6	1.2	1.2	0.6

Ibias = 10µA

4.2.3 Voltage Controlled Oscillator

Figure 18 gives the architecture of a single delay element. The overall transfer function of the delay element is found as:

$$H_d(s) = \frac{V_o}{V_i} = \frac{g_{m1}}{g_{o1} + g_{o3} + g_{m4} + sC_T} \tag{52}$$

where the frequency of the pole is given as:

$$\omega_p = \frac{g_{o1} + g_{o3} + g_{m4}}{C_T} \tag{53}$$

Since the output conductance g_{o1} is much smaller than g_{o3} and g_{m4}, it can be neglected during the first order approximation. The relationship between the pole frequency and the oscillation frequency is given in 38. The pole frequency may be calculated as follows:

$$\begin{aligned} \omega_{osc} &= 2\pi \times 400MHz \Rightarrow \omega_p = 3.89 \times 10^9 \, rad/s \\ \omega_{osc} &= 2\pi \times 500MHz \Rightarrow \omega_p = 4.32 \times 10^9 \, rad/s \end{aligned} \tag{54}$$

When M3 is operating in saturation, $g_{o3} << g_{m4}$, and the oscillation frequency is 500MHz because all of the current from M1 goes to M4. ω_p can be approximated as:

$$\omega_p \approx \frac{g_{m4}}{C_T} \tag{55}$$

This equation can be expressed in terms of drain current and transistor dimension as:

$$\omega_p \approx \frac{2I_D}{(V_{GS} - V_T)} \cdot \frac{1}{2/3 \, C_{ox} WL} \tag{56}$$

Assume V_{GS}-V_T is 0.4V for transistor in saturation. Drain current is half of bias current of 1.8mA, which is estimated for a total parasitic capacitance, C_T, of 1pF. The W and L dimensions can be found from 55 as:

$$\begin{aligned} W &= 106\mu m \\ L &= 0.6\mu m \end{aligned} \tag{57}$$

When M3 is operating in the triode region, the output conductance g_{o3} is comparable with g_{m4}, ωp then can be expressed as:

$$\omega_p \approx \frac{g_{o3} + g_{m4}}{C_T} \tag{58}$$

The ratio of the output conductance can be used to approximated as:

$$\begin{aligned} \frac{g_{m4}}{g_{o3} + g_{m4}} &= \frac{4.32\times10^9}{3.89\times10^9} \\ g_{o3} &= 0.11 g_{m4} \end{aligned} \tag{59}$$

Since the transistor M3 is in linear region, the conductance can be expressed as:

$$g_{o3} = \mu C_{ox}\left(\frac{W}{L}\right)_3 \left|V_{DD} - V_{cont} - V_T\right| \tag{60}$$

The relationship between the output conductance go3 and the control voltage is linear, which leads to a linear correlation to the oscillation frequency. This structure linearizes the control voltage to the oscillation frequency by transistors M3 and M4. The dimension of the transistor M3 is found as:

$$\begin{aligned} W &= 10.5\mu m \\ L &= 0.6\mu m \end{aligned} \tag{61}$$

Transistor M1 is assumed to have the same dimension as M4 for a first order approximation. Multipliers are used for common-centroid layout to minimize the effect of process variation. Through simulation, the final dimension of the transistors are shown in Table 2.

Table 2 Transistor Dimensions for VCO Delay Element (Figure 18)

	M1	**M2**	**M3**	**M4**	**M5**	**M6**
W(µm)	39(x4)	39(x4)	4(x2)	30(x2)	30(x2)	4(x2)
L(µm)	0.6	0.6	0.6	0.6	0.6	0.6

Ibias = 1.8mA

Simulation in *Cadence* shows the performance of the VCO as see in Figure 35.

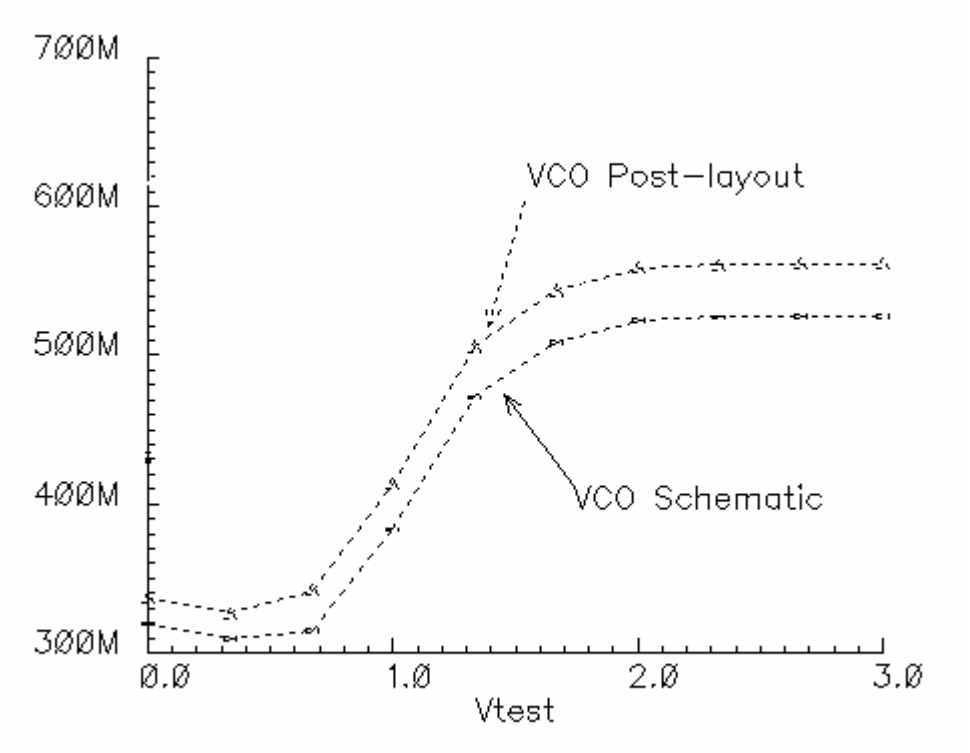


Figure 35 VCO Output Simulation

Both schematic simulation and post-layout simulation are shown in the above figure. For both simulations, the oscillation frequency is mostly linearly proportional to the control voltage (Vtest in the figure). Since the transistor level simulation is only a first order approximation and due to the use of multipliers in the layout, the simulation over-compensated for more parasitic capacitance than present in the layout. Since the oscillation frequency is inversely proportional to the parasitic capacitance, the actual post-layout VCO simulation has slightly larger oscillation frequencies for the same control voltages. The post-layout simulation shows that the desired frequency range of 400-500MHz is entirely in the linear region therefore causing the gain of the VCO to increase slightly.

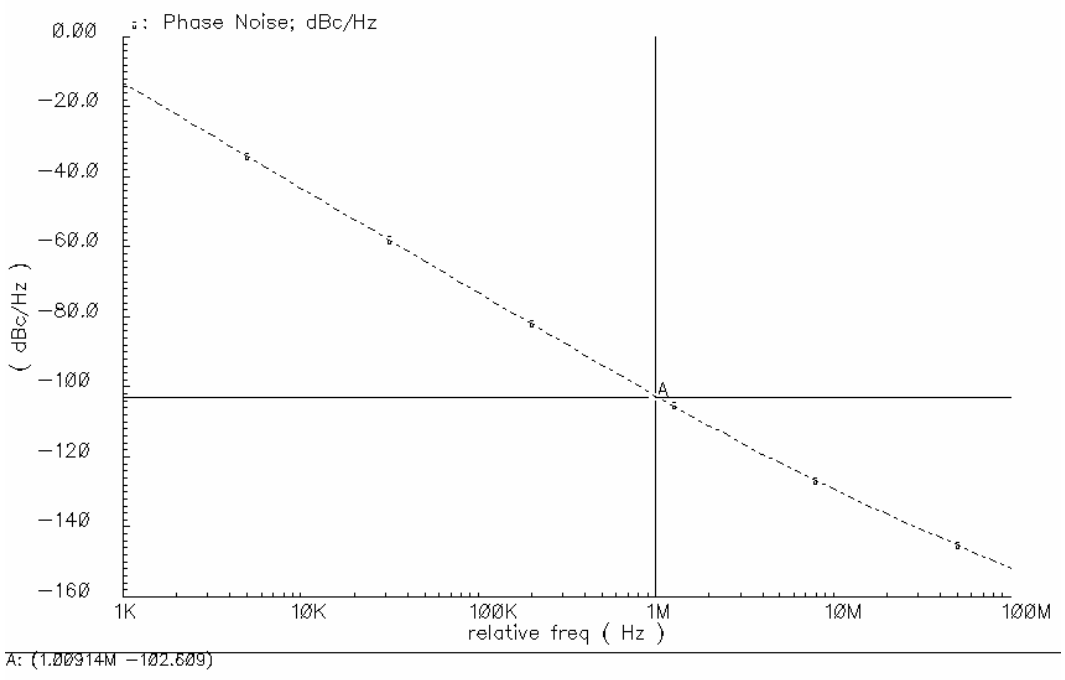


Figure 36 VCO Phase Noise Performance at 1MHz Offset

The phase noise of the VCO is also simulated. Figure 36 shows a phase noise of -102 dBc/Hz at 1MHz offset.

4.3 Frequency Down-Converter Design

4.3.1 Mixer

The double-balanced Gilbert cell mixer structure is chosen for the mixer for less feedthrough from the LO port (Figure 25). The output of the VCO feeds the differential RF ports. An external waveform generator is used to generate a 400MHz square wave to feed the differential LO port.

The DC bias for the RF and LO input transistors needs to be set. The output of the VCO is biased at a DC voltage of 1.5V. The signal has an amplitude of less than 300mV. A minimum overdrive of 0.3V is needed to ensure that the LO switches M3-M6 can be in the proper region. A 1.8V DC bias is set for the LO input. Since the structure is fully differential, only one side is needed for a first approximation analysis.

If transistors M3-4 are identical and the commutating switching is instantaneous, only one branch of current is flowing to the output at a time. The conversion gain of the mixer can be found as [17]:

$$A_V = \frac{2}{\pi} g_{m1} R_L \tag{62}$$

where R_L is the load resistance of the mixer and is expressed as:

$$R_L = \frac{1}{g_{m7}} \| r_{O3} \tag{63}$$

If the equivalent resistance of M7 is smaller than the output resistance of M3, the total conversion gain can be re-stated as:

$$A_V = \frac{2}{\pi} \cdot \frac{g_{m1}}{g_{m7}} \tag{64}$$

A conversion gain of 2 V/V or 3dB makes the transconductance of M1 π times less than M7. Since K_p is approximately 3 times K_n, transistors M1 and M7 have approximately the same dimension. A current of 100μA and an overhead voltage of 0.5V for the bias current source is used to determine the DC bias and the transistor size of M1.

The current through M1 is half the biasing current due to the fully differential structure. Since only one of M3 and M4 is on at a time, the current flowing through the M3 or M4 is the same as the current flowing through M1. Consider the case where transistor M3 is on and M4 is off. Transistor M3 is in saturation when $V_{DS} > V_{GS} - V_T$, the dimension of M3 can be found through the drain current equation where V_{GS}-V_T is approximated as 0.3V for saturation:

$$I_D = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)_3 (V_{GS} - V_T)^2 \tag{65}$$

$$\begin{aligned} W &= 16\mu m \\ L &= 0.6\mu m \end{aligned} \tag{66}$$

Multipliers are used for common-centroid layout to minimize the effect of process variation, the final dimension of the transistors are shown in Table 3.

Table 3 Transistor Dimensions for Mixer

	M1	M2	M3	M4	M5	M6	M7	M8
W(μm)	12(x2)	12(x2)	5.1(x4)	5.1(x4)	5.1(x4)	5.1(x4)	8.1(x2)	8.1(x2)
L(μm)	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6

Ibias = 100μA

4.3.2 Filter

A simple two-pole passive RC filter shown in Figure 26 is used at the output of the mixer with transfer function given in 43. The 3dB frequency, $\omega_{-3dB} = 2\pi\frac{1}{RC}$, is 25% larger than 100MHz to ensure frequencies equal to or less than 100MHz are not attenuated. The filter component values are found as below with a 125MHz -3dB frequency:

$$\begin{aligned} R &= 1.3k\Omega \\ C &= 1pF \end{aligned} \tag{67}$$

4.4 Output Selector Design

4.4.1 Fixed Divider

A fixed divider ratio of 100 is needed to achieve the resolution specification of 10KHz at the output. The divider is composed of two D-flip flops and two divide-by-5 circuits where the D-flip flops act as divide-by-2 blocks ($100 = 2\times2\times5\times5$). The divide-

by-5 circuit is designed using digital state logic where 5 states are needed. Table 4 shows the truth table of the state logic where CBA represents the current state in binary and CnBnAn denotes the next state. The circuit is essentially a counter. The state is the number of clock cycles. Next state is current state plus one until the current state reaches 4, then the next state resets back to zero. No external inputs are needed. The circuit is clocked by the input reference frequency.

Table 4 Divide-by-5 Truth Table

Current State			**Next State**		
C	**B**	**A**	**Cn**	**Bn**	**An**
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0

The expressions of next state are realized using Karnaugh map through NOR gates as:

$$\begin{aligned} An &= \overline{A + C} \\ Bn &= \overline{A + \overline{B}} + \overline{B + \overline{A}} \\ Cn &= \overline{\overline{A} + \overline{B}} \end{aligned} \tag{68}$$

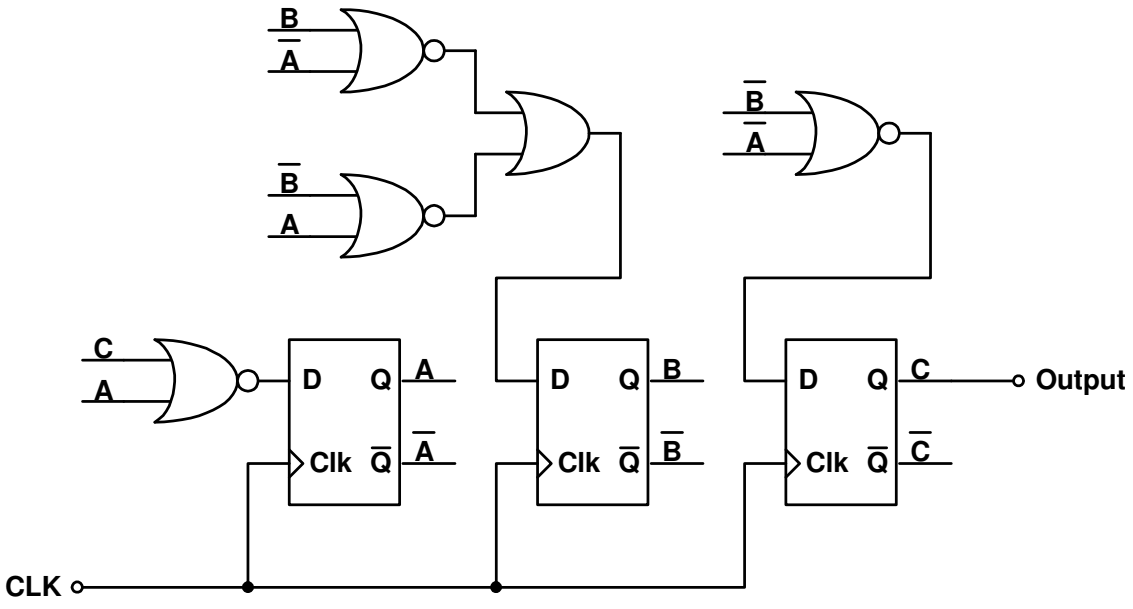


Figure 37 Divide-by-5 Implementation

Figure 37 shows the of the Divide-by-5 implementation. Three D-Flip Flops used in the divide-by-5 circuit are used to hold the output from the previous stage and align the clock edges. The output of the last D-Flip Flop gives a pulse every 5 clock cycles.

Figure 38 shows the implementation of the whole divide-by-100 circuit where two D-flip flops are cascaded with two divide-by-5 circuits.

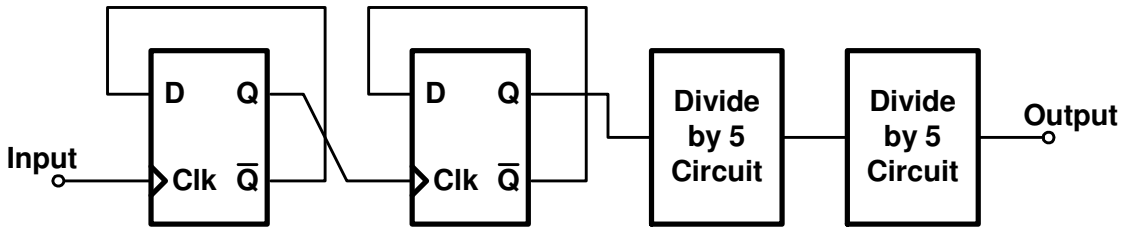


Figure 38 Fixed Divide-by-100

The output of the fixed divider is the product of all the divider ratios as:

$2 \times 2 \times 5 \times 5 = 100$.

4.4.2 2:1 Multiplexer

A 2-input 1-output multiplexer is used to select between the two frequency range. A general multiplexer structure is used (see Figure 39).

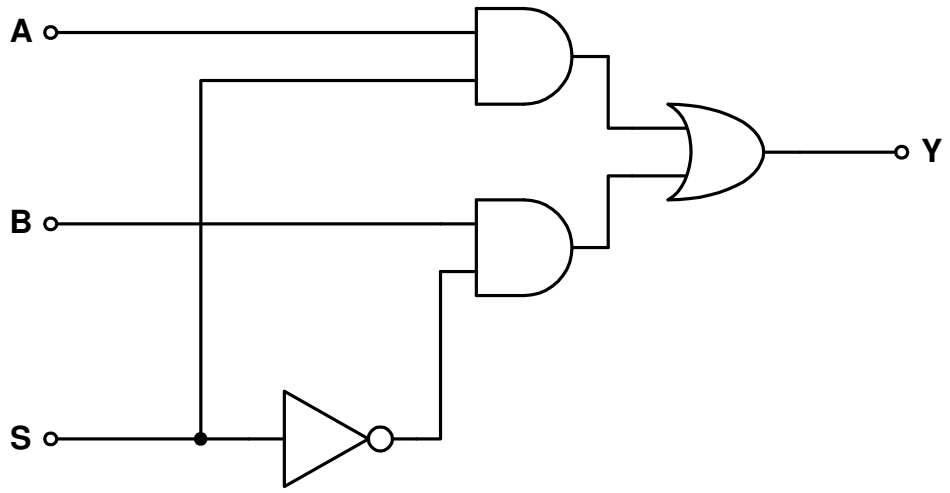


Figure 39 2-to-1 Multiplexer

A truth table can shows the operation of the multiplexer where S is the select that is controlled externally and Y is the output. The output receives the value of B when S is 0 and the value of A when S is 1.

4.5 Frequency Synthesizer Simulation

After transistor level design, the entire system is laid out in the standard AMI05 CMOS technology. Figure 40 is a captured image of the chip layout.

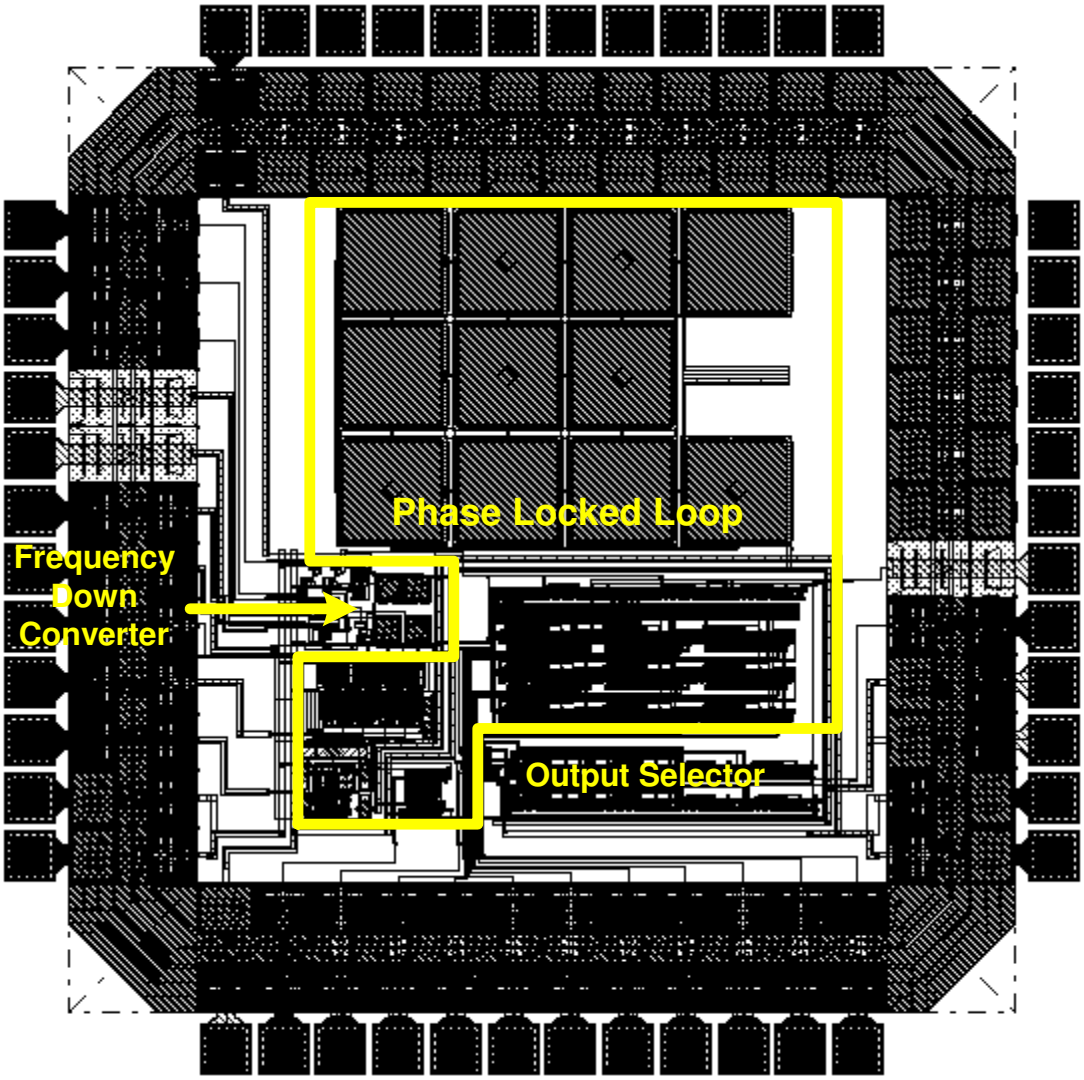


Figure 40 Frequency Synthesizer Chip Layout

The total area including bonding pads is $1681\mu m \times 1680\mu m$. The active circuit area is $1200\mu m \times 1200\mu m$. There are 48 pins in this layout with 31 functional I/O pins. The package type is LPCC which is a plastic package. It is clear that the additional blocks added little area (<20%) to the basic PLL based frequency synthesizer.

The system is set up as in Figure 41 and simulated in *Cadence*.

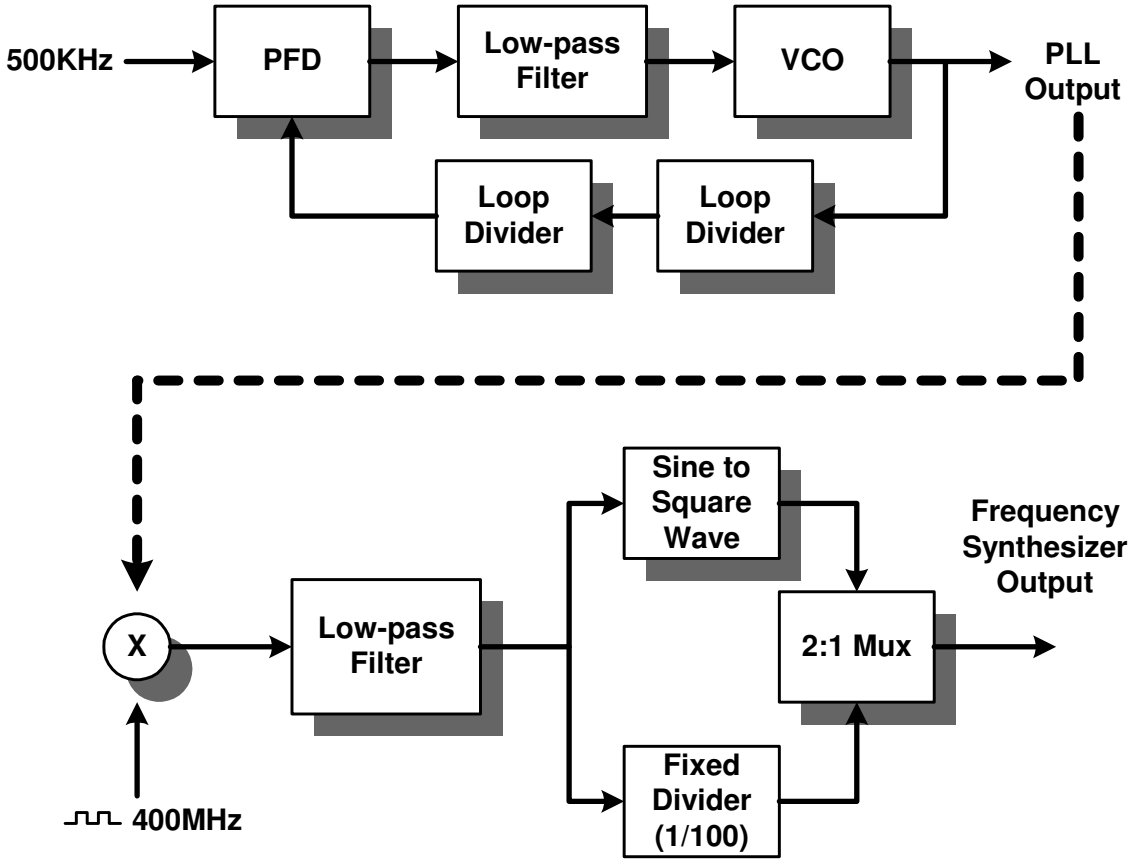
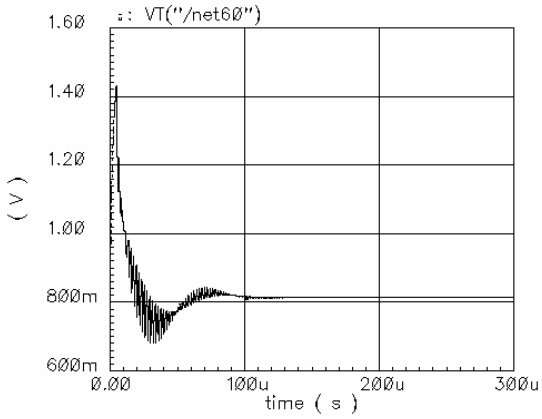
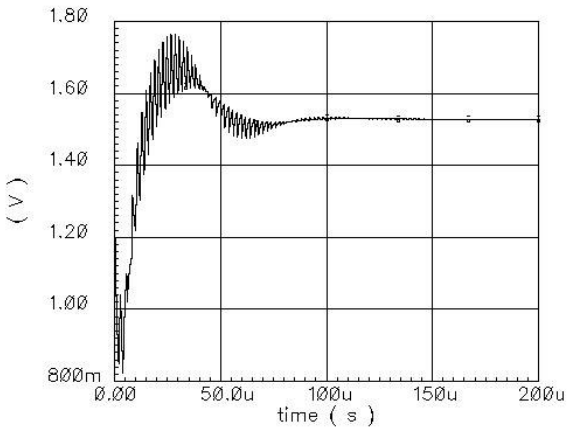


Figure 41 Frequency Synthesizer Setup

The simulation results are shown below:

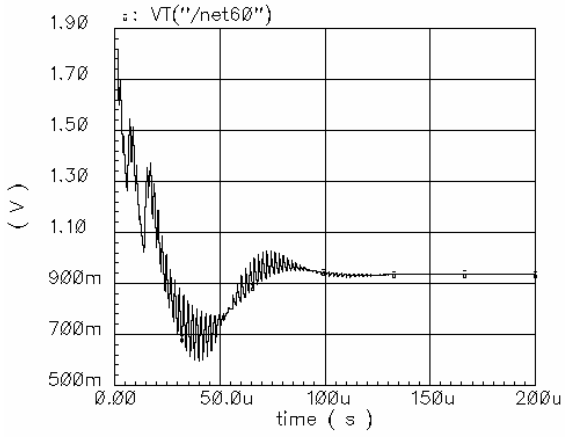


VCO Control Voltage Settles to 0.8V for N=802

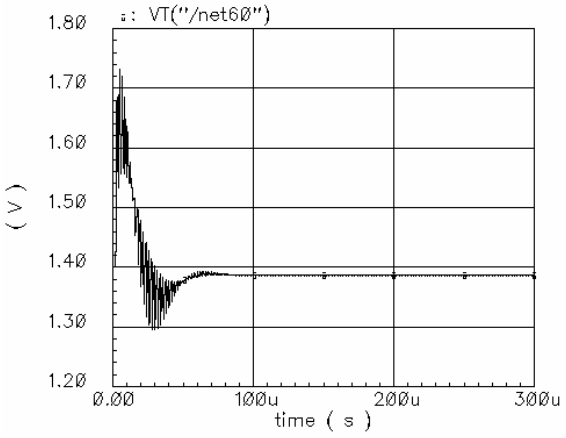


VCO Control Voltage Settles to 1.5V for N=1000

Figure 42 VCO Control Voltage



VCO Control Voltage Settles to 0.9V for N=802



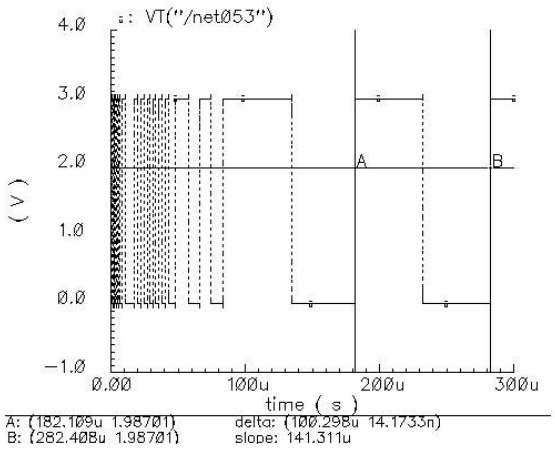
VCO Control Voltage Settles to 1.4V for N=1000

Figure 43 Postlayout VCO Control Voltage

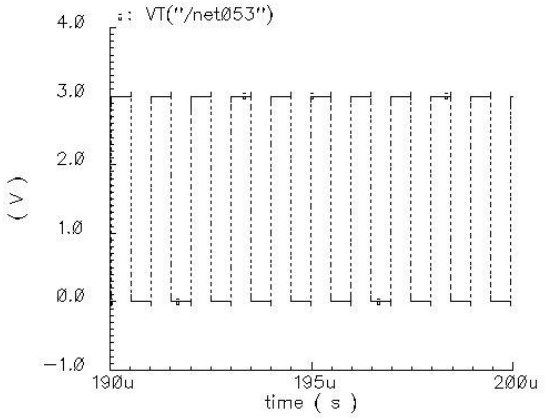
Figures 42-43 show the control voltages of the VCO in the frequency synthesizer. The system is stable and settles for both the minimum and maximum value of N=802 and N=1000, respectively. N is the overall division ratio in the feedback path. The settling time is less than 100µsec for both N values. The control voltage for transistor level

simulation settles to 800mV when N=802 and 1.5V when N=1000; the control voltage for post-layout simulation settles to 900mV when N=802 and 1.4V when N=1000. The values of the VCO control voltage are consistent with the plot shown in Figure 35 where the frequencies of the post-layout simulations are slightly higher than the frequencies of the schematic simulations due to parasitic capacitor approximations.

The following plots show the output of the frequency synthesizer at the upper and lower boundary conditions where N=802 and N=1000.



a) Frequency Synthesizer Output =10KHz



b) Frequency Synthesizer Output=1MHz

Figure 44 Frequency Synthesizer Output for N=802

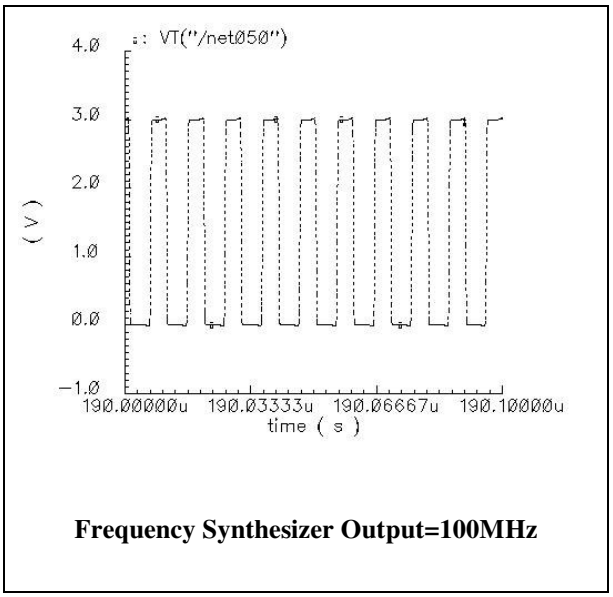
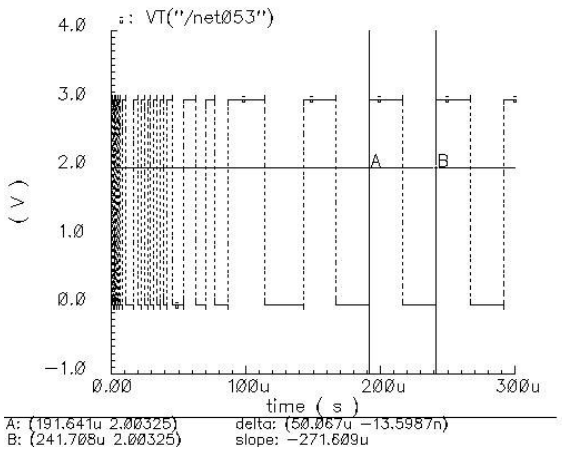


Figure 45 Frequency Synthesizer Output for N=1000

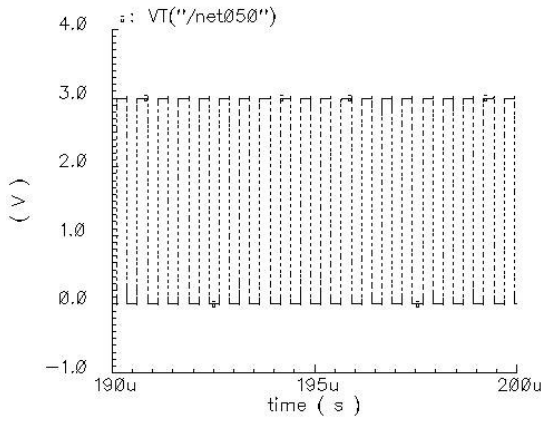
Post layout simulations show the output of the frequency synthesizer above in Figures 44-45. Note that when N=1000, the output from the fixed divider of 1MHz overlaps the frequency output of the square wave generator when N=802.

The outputs are square waves that cover from rail to rail. For a N value of 802, the Δt =100.298µs giving an output frequency of $1/\Delta t$ = 10KHz. For the same value of N, a Δt =1.003µs is also achieved to give an output frequency of 1MHz. Figure 45 shows the output for N=1000, where Δt =10.02ns to provide an output frequency of 100MHz.

In order to illustrate the frequency step (resolution), the next smallest N value of 804, is simulated in the frequency synthesizer. N increases by 2 to provide an increase of twice the input reference frequency of 500KHz to produce a step of 1MHz at the output of the PLL. The output of the PLL then passes through the frequency down-converter and the output selector to produce the following plots:



a) Frequency Synthesizer Output =20KHz



a) Frequency Synthesizer Output=2MHz

Figure 46 Frequency Synthesizer Output for N=804

Both plots from Figure 46 show the output of the frequency synthesizer for N=804. Figure 46a shows Δt =50.067µs which gives an output frequency of 19.97KHZ. Looking at Figure 44a, this achies a frequency step of 10KHz. Figure 46b shows that Δt =500.7ns gives an output frequency of 1.997MHz, which is a frequency step of 1MHz from Figure 44b.

When a divider is placed in the forward path, the phase noise improves by a factor of 20logN. Therefore, the worst case output performance happens at 100MHz since the output is not divided by the fixed divider. The output is shown in Figure below.

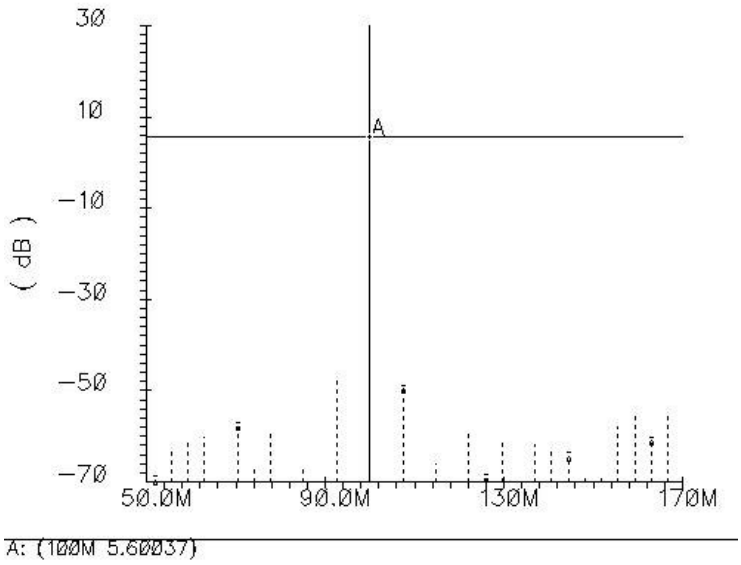


Figure 47 Frequency Synthesizer Output of 100MHz

Figures 47 shows that the output signal desired is at least 50dB larger than the unwanted harmonics and spurs.

Table 5 Frequency Synthesizer Results

	Proposed Architecture	**Current State-of-the-Art for BIST**
Frequency Range	10KHz-100MHz	38MHz -167MHz
Resolution	10K-1MHz: 10KHz 1-100MHz: 1MHz	1MHz
Phase Noise	10K-1MHz: -80dBc/Hz@10KHz 1-100MHz: -40dBc/Hz@1MHz	-80dBc/Hz@1MHz
Active Area	1200µm x 1200µm	200µm x 1000µm
Power Consumption	4mW	72.6mW

Table 5 shows the final results of the frequency synthesizer. It also compares the results with the current state-of-the-art for BIST application. Most of the specifications are better than or comparable with the state-of-the-art frequency synthesizer. The frequency range is much wider for this proposed architecture. It can also achiever finer resolution for a specific range of 10K-1MHz. The phase noise is comparable and the power consumption is much less. However, the active area of the proposed architecture is larger. This can be contributed to two aspects: first, capacitive scaling is used for the current state-of-the-art frequency synthesizer, but not for the proposed architecture. Capacitive scaling may be used for the proposed architecture to decrease the total area. The second reason is that the technology used for the proposed architecture has much larger dimensions than the current-state-of-the-art frequency synthesizer.

5 CONCLUSIONS

A wide-band frequency synthesizer is designed in the project. The architecture of a PLL is analyzed as well as the modifications carried out. The modified structure has three blocks: basic PLL based frequency synthesizer, frequency down-converter, and output selector. Each of these blocks is analyzed and designed.

The basic PLL is composed of a digital phase frequency detector that detects phase frequency error between the input reference frequency and the loop divider output; an on-chip passive low pass filter; a VCO; and a loop divider. This block generates a band of frequencies of 400-500MHz.

The frequency down-converter is composed of a mixer and a lowpass filter that down converts the output of the PLL (400-500MHz) to the desired output frequencies (10KHz-100MHz). The filter then filters out frequencies larger than the maximum frequency desired including harmonics.

The output of the frequency down-converter splits into two paths. On one path, a square wave generator converts the output from a sinusoid to a square wave form with no frequency alteration. The other path takes the output frequency of the down-converter (10K-1MHz) and divides the frequency by 100 as well as converts the waveform into a square wave. The output selector then chooses between the two paths with *Select* as an external control.

After the system is design, it is laid out in the standard AMI05 technology. The total active area is $1200\mu m \times 1200\mu m$ where the additional blocks introduce less than 20% of the total area. The proposed frequency synthesizer gives an output frequency range of 10KHz to 1MHz with a resolution of 10KHz and an output of 1-100MHz with a

resolution of 1MHz. The phase noise of the frequency synthesizer is -80dBc/Hz at 10KHz offset for the frequency band of 10K-1MHz; and -40dBc/Hz at 1MHz offset for the frequency band of 1-100MHz. The power consumption is less than 4mW.

Future work of this project may include building a PCB in order to test the fabricated chip. Also, capacitive scaling may be implemented for the next version of the frequency synthesizer to decrease the area needed. A better technology may be used for smaller dimensions.

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APPENDIX A

Open-Loop PLL Linear Analysis

```
Wi=1e6*2*pi;           % Reference frequency = 1MHz
Kvco=166.7e6*2*pi;     % VCO gain (rad/V)
Icp=10e-6;             % Charge Pump current
M=447;                 % Mean division factor
b=10;                  % For PM = 60  b=C1/C2
Wc4=0.75*Wi/1.82;              % For more than 60dB attenuation of spurs

T=sqrt(b+1)/Wc4;       % T=R1C1; From   3.23

C1=230e-12;
R1=55e3;
C2=23e-12;

Z1=1/T/2/pi
P2=1/(C2*R1)/2/pi
Wc=Wc4/2/pi

% Open loop transfer function
f=logspace(1,6,1000);
w=2*pi*f;
s=j*w;

LTN=1*(1.+s*T)*(Icp*Kvco)/(2*pi*M)*(b/(b+1));
LTD=(s.^2).*C1.*(s.*(T/(b+1))+1);

LT=LTN./LTD;

HLT=20*log10(abs(LT));
PhLT=angle(LT)/(pi)*180;

Figure(1)
subplot(2,1,1)
semilogx(f,HLT,'r')
grid

subplot(2,1,2)
semilogx(f,PhLT)
grid
```

APPENDIX B

Stability Analysis

```
% PLL linear model
close all
Icp=10e-6;                          % Charge pump current
Kpd=Icp/(2*pi);                     % Phase detector gain
Kv=166.7e6*2*pi;                    % VCO gain
N=447*2;                            % Loop division N
d=sqrt(2)/2;                        % Damping factor
Wref=2*pi*0.5e6;                    % Reference frequency
W3dB=0.75*(Wref/10);                % Loop filter frequency
Wn=W3dB/2.06                        % Natural frequency

% Filter components
C1=230e-12;
R=55e3;
T=1/(R*C1)                          % Time constant

numo=[Kpd*Kv*R Kpd*Kv*R*T];         % Numerator of H(s)
nume=[1 0 0];                       % Numerator of error function E(s)
den=[1 Kpd*Kv*R/N Kpd*Kv/(N*C1)];   % Denominator of H(s) and E(s)
Ho=tf(numo,den)                     % creating phase transfer function
He=tf(nume,den)                     % creating error transfer function

f=logspace(2,5,1000);
W=2*pi*f;
mago=20*log10(abs(freqs(numo,den,W)));  % magnitude of phase transfer function
mage=20*log10(abs(freqs(nume,den,W)));  % magnitude of error transfer function
phi=angle(freqs(numo,den,W))/pi*180;    % phase of phase transfer function

% Figure of magnitude, phase and error function
Figure(1);
subplot(2,1,1)
semilogx(W,mago)                    % Plot closed loop transfer function
ylabel('Magnitude (dB)')
title('Phase Transfer Function')
subplot(2,1,2)                      % Plot phase vs. frequency
semilogx(W,phi)
xlabel('Frequency W')
ylabel('Phase (degree)')
title('Phase Transfer Function')

% Figure of phase pulse (frequency step) functions
```

```
Figure(2);
t=[0:0.1e-7:5e-4]';
Ho_impulse = (impulse(Ho,t));                % Create impulse function
plot(t,Ho_impulse);                          % Plot impulse response
xlabel('Time (s)')
ylabel('Magnitude')
title('Phase Step for Phase Output')

% Figure of phase ramp (frequency impulse) functions
den_r = [1 Kpd*Kv*R/N Kpd*Kv/(N*C1) 0]; % Multiply denominator by ‘s’
Ho_r=tf(numo,den_r)                          % Create ramp function

x=t';
Ho_ramp = (step(Ho_r,t));

Figure(3);
plot(t,Ho_ramp);                             % Plot ramp response
grid
xlabel('Time (s)')
ylabel('Magnitude')
title('Phase Ramp for Phase Output')
```

VITA

Wenjian Yan received her Bachelor of Science degree in computer engineering, electrical engineering track from Texas A&M University, College Station, Texas in 2001. Since then she continued on to work towards her Master of Science degree in electrical engineering at the Analog and Mixed Signal Center, at Texas A&M University. She received her M.S. in 2004. Her current field of research is in the design and fabrication of analog and mixed-signal circuits and frequency synthesizers for built-in self test. She can be reached through the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843.